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571-272-7822

Paper 7
Entered: April 22, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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MEDIATEK, INC. and MEDIATEK USA, INC.,
Petitioner,

v.

REDSTONE LOGICS LLC,
Patent Owner.

_____

IPR2025-00085
Patent 8,549,339 B2

_____

Before JEFFREY W. ABRAHAM, STEPHEN E. BELISLE, and ANDREW L. NALVEN, *Administrative Patent Judges*.

NALVEN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

MediaTek Inc. and MediaTek USA, Inc. (collectively, "Petitioner") filed a Petition (Paper 1, "Pet.") requesting *inter partes* review of claims 1–6, 8–11, 14 and 21 of U.S. Patent No. 8,549,339 B2 (Ex. 1001, "the '339 patent"). Redstone Logics LLC ("Patent Owner") filed a Preliminary Response (Paper 6, "Prelim. Resp.").

We have authority under 35 U.S.C. § 314 and 37 C.F.R. § 42.4(a). Pursuant to 35 U.S.C. § 314(a), an *inter partes* review may not be instituted "unless . . . there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." For the reasons that follow, we determine that Petitioner has not demonstrated a reasonable likelihood of prevailing in demonstrating the unpatentability of any of the challenged claims. Accordingly, we do not institute an *inter partes* review.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies MediaTek Inc. and MediaTek USA, Inc. as real parties-in-interest. Pet. 1. Patent Owner identifies Redstone Logics LLC as real party-in-interest. Paper 4, 1 (Patent Owner's Mandatory Notice).

B. Related Proceedings

The parties identify the following related cases: *Samsung Electronics Co., Ltd. v. Redstone Logics LLC,* IPR2024-00974 (P.T.A.B. May 29, 2024); *Redstone Logics LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc.*, Case No. 2:23-cv-00485 (E.D. Tex.); *Redstone Logics LLC v. NXP Semiconductors N.V., NXP B.V., and NXP USA, Inc.*, Case No. 7:24-cv-00028 (W.D. Tex.); *Redstone Logics LLC v. MediaTek,*

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Inc. and MediaTek USA, Inc., Case No. 7:24-cv-00029 (W.D. Tex.); and *Redstone Logics LLC v. Qualcomm Inc. and Qualcomm Technologies, Inc.*, Case No. 7:24-cv-00231 (W.D. Tex.). *See* Pet. 1; Paper 4, 1.

C. The '339 Patent

The '339 patent describes a multi-core processor including two or more independent processor cores arranged in an array. Ex. 1001, 1:6–7. The '339 patent describes providing a dynamic supply voltage and clock speed control to allow the processor to operate at high power and high clock speed when needed and low power and low clock speed when the computational requirements are reduced. *Id.* at 1:10–14.

Figure 1, reproduced below, illustrates a configuration of the multi-core processor. Ex. 1001, 1:26–27.

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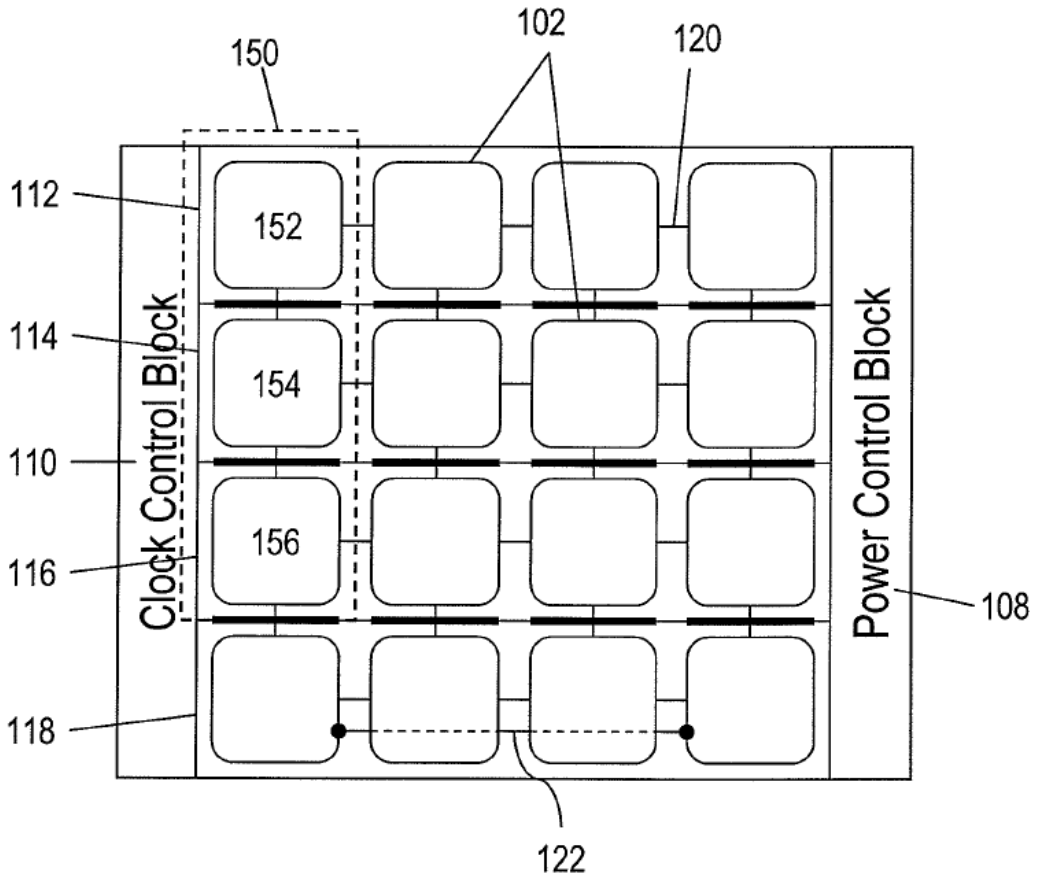

FIG. 1

Figure 1 depicts multi-core processor 100 including multiple processor cores 102 arranged in a 2-dimensional array. *Id.* at 2:4–9. Interface circuit 120 couple adjacent processor cores 102. *Id.* at 2:9–10. Figure 1 further depicts multi-core processor 100 divided into regions arranged as stripes 112, 114, 116, and 118. *Id.* at 2:20–26. According to the '339 patent, each stripe is powered by supply voltage from power control block 108 and associated with an independent clock domain provided by clock control block 110. *Id.* at 2:26–31.

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Figure 3, reproduced below, illustrates a set of processor cores interfacing using a synchronizer. Ex. 1001, 1:31–33.

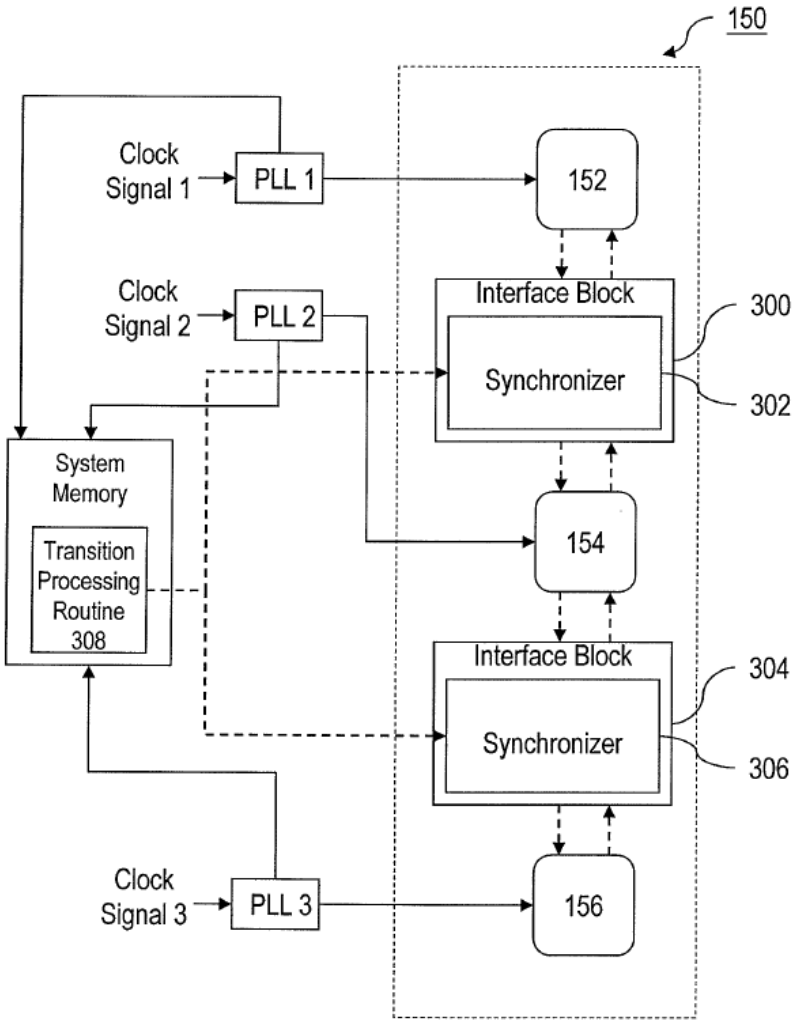

FIG. 3

Figure 3 depicts processor cores 152, 154, and 156 driven by clock signal 1, clock signal 2, and clock signal 3 respectively. *Id.* at 4:1–10. Phase lock loop ("PLL") 1, 2, and 3 provide stable clock signals to respective processor cores 152, 154, and 156 and synchronizers 302 and 306. *Id.* at 4:10–13, 4:64–5:6. Synchronizers 302 and 306 synchronize clock signals between

adjacent cores to allow for communication between the processor cores. *Id.* 5:1–8.

D. Illustrative Claim

Petitioner challenges claims 1–6, 8–11, 14 and 21 of the '339 patent, where claims 1 and 21 are independent claims. Claim 1 is illustrative of the claimed invention and is reproduced below with Petitioner's labeling of elements.

1. 1[pre] A multi-core processor, comprising:

1[a1] a first set of processor cores of the multi-core processor,

1[a2] wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;

1[b1] a second set of processor cores of the multi-core processor,

1[b2] wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input,

1[b3] wherein the first supply voltage is independent from the second supply voltage, and

1[b4] the first clock signal is independent from the second clock signal; and

1[c1] an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores,

1[c2] wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

Ex. 1001, 7:53–8:5; Ex. 1017, 1.

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E. Asserted Challenges to Patentability

Petitioner challenges claims 1–6, 8–11, 14 and 21 of the '339 patent as follows. Pet. 15–95.

Claims Challenged	35 U.S.C. §[1]	References/Basis
1, 5, 8–10, 14, 21	103(a)	Knoth,[2] Allarey[3]
2–4	103(a)	Knoth, Allarey, Flautner[4]
6	103(a)	Knoth, Allarey, Wolfe,[5] Kumar[6]
11	103(a)	Knoth, Allarey, Wolfe
1–3, 5, 8–10, 14, 21	103(a)	Naffziger,[7] Allarey
4	103(a)	Naffziger, Allarey, Flautner
6	103(a)	Naffziger, Allarey, Wolfe, Kumar
11	103(a)	Naffziger, Allarey, Wolfe

In support of its challenge, Petitioner relies on the Declaration of Dr. R. Jacob Baker (Ex. 1003).

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 103 effective March 16, 2013. Because the application from which the '339 patent issued claims priority before this date, the pre-AIA version of § 103 applies.
[2] Knoth, U.S. Publ'n No. 2009/0158078 A1, published June 18, 2009 ("Knoth," Ex. 1005).
[3] Allarey et al., U.S. Patent 8,122,270 B2, issued February 21, 2012 ("Allarey," Ex. 1006).
[4] Flautner, U.S. Publ'n No. 2005/0034002 A1, published February 10, 2005 ("Flautner," Ex. 1007).
[5] Wolfe et al., U.S. Publ'n No. 2011/0153984 A1, published June 23, 2011 ("Wolfe," Ex. 1008).
[6] Kumar et al., U.S. Publ'n No. 2007/0080696 A1, published April 12, 2007 ("Kumar," Ex. 1009).
[7] Naffziger et al., U.S. Publ'n No. 2010/0122101 A1, published May 13, 2010 ("Naffziger," Ex. 1010).

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III. DISCUSSION

A. Principles of Law

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring *inter partes* review petitions to identify "with particularity . . . the evidence that supports the grounds for the challenge to each claim")). This burden of persuasion never shifts to the patent owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A claim is unpatentable under § 103(a) "if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a); *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).[8]

We consider Petitioner's asserted challenges with the above-noted principles in mind.

[8] Neither party presents evidence of secondary considerations at this stage.

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B. Claim Construction

Only those claim terms that are in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). For purposes of this decision, we determine that no term requires express construction.

C. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art ("POSITA") would have had "at least a bachelor's degree in electrical engineering, computer engineering, computer science, or a similar field, and at least two years of industry or academic experience designing or analyzing electronic circuits, semiconductors, processors, or power management, and related firmware and software, or the equivalent." Pet. 6–7 (citing Ex. 1003 ¶ 29). Patent Owner does not challenge Petitioner's proffered definition as to the level of ordinary skill in the art. Prelim. Resp. 4.

For purposes of this Decision, we adopt Petitioner's assessment, which is consistent with the level of skill reflected in the specification and asserted prior art.

D. Ground 1: Alleged Obviousness over Knoth and Allarey

Petitioner asserts that claims 1, 5, 8–10, 14 and 21 of the '339 patent would have been obvious over Knoth and Allarey. Pet. 15–52. For the reasons explained below, we determine that Petitioner fails to demonstrate a reasonable likelihood of prevailing in showing that claims 1, 5, 8–10, 14 and 21 of the '339 patent are obvious over Knoth and Allarey.

Before addressing the parties' arguments, we provide an overview of the Knoth and Allarey references.

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1. Overview of Knoth

Knoth describes a multiprocessor digital system including at least two processor cores 110. Ex. 1005 ¶ 23. Knoth describes a first digital circuit, e.g., a first processor core, operates at a first rate determined by a first clock signal and a second digital circuit, e.g., a second processor core, operates at a second rate determined by a second clock signal. *Id.* ¶ 4. A clock ratio controller provides dynamic voltage and frequency control including adjusting the frequency of the first and second clock signals in response to a power management signal. *Id.* at Abstract.

Figure 1A, reproduced below, depicts a multiprocessor system with two processor cores. Ex. 1005 ¶ 23.

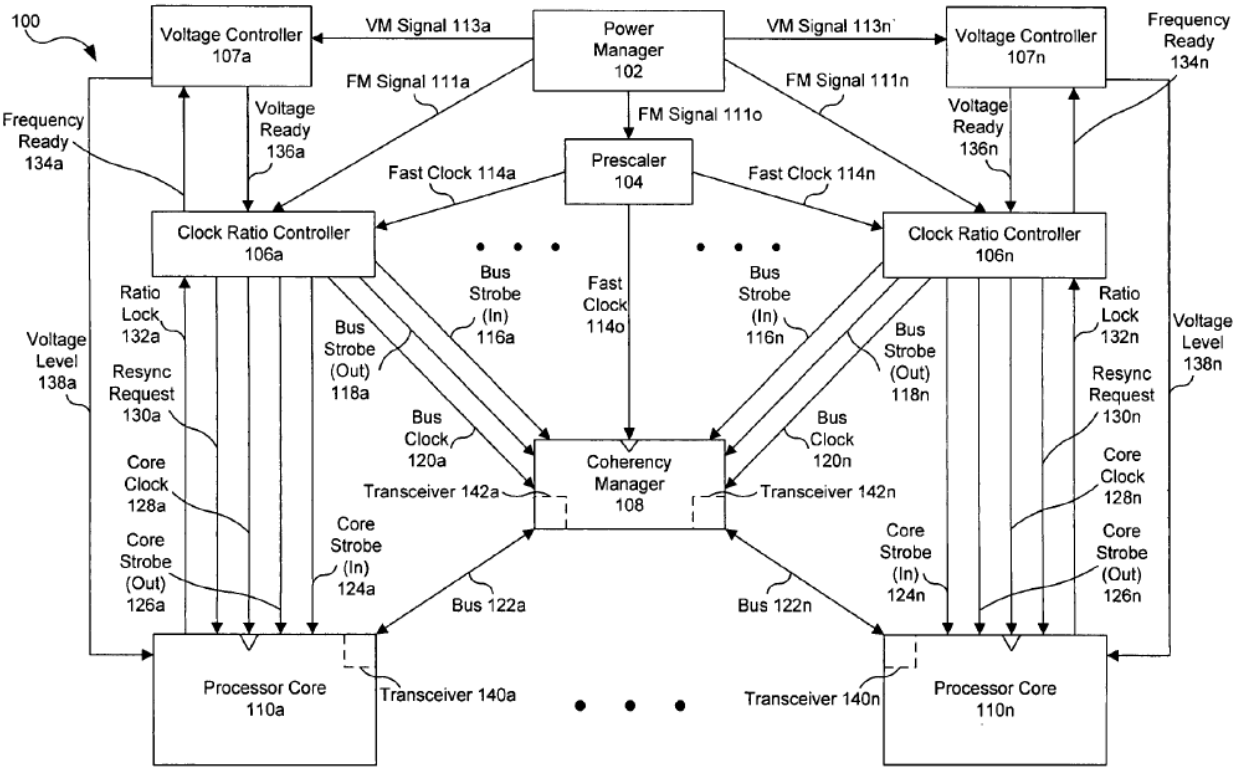

FIG. 1A

Figure 1A depicts, in pertinent part, digital system 100 including power management unit 102, prescaler 104, a plurality of clock ratio controllers

106a–n, plurality of voltage controllers 107a–n, coherency manager 108, and a plurality of processor cores 110a–n. *Id.* ¶¶ 22–23.

According to the '339 patent, power management unit 102 determines when to adjust the voltage and/or a frequency of one or more of processor cores 110 to affect power consumption and/or heat generation. Ex. 1005 ¶ 24. Clock ratio controllers 106a–n generate the clock signal used to control processor cores 110a–n and data communications on busses 122a–n. *Id.* ¶ 27.

Figure 2A, reproduced below, illustrates the elements of clock ratio controller 106. Ex. 1005 ¶ 11.

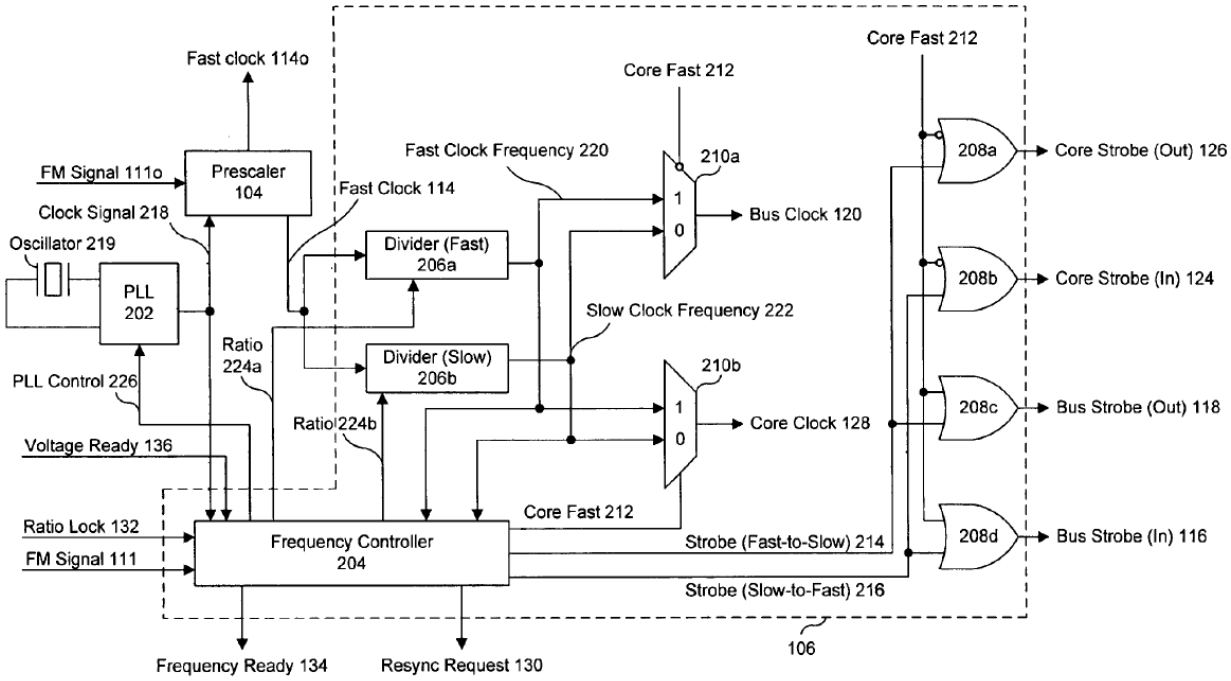

FIG. 2A

Figure 2A depicts clock ratio controller 106 including, in pertinent part, frequency controller 204, fast clock signal divider 206a, and slow clock signal divider 206b. *Id.* ¶ 44. Clock ratio controller 106, indicated by the dotted box, is coupled to PLL 202 and prescaler 104 of digital system 100.

Id. ¶ 41. PLL 202 outputs clock signal 218 based on timing pulses generated by oscillator 219. *Id.* ¶ 42.

2. Overview of Allarey

Allarey is directed to "stabilizing voltage supplied to a multi-core processor during a clock signal frequency locking process." Ex. 1006, 1:6–9. Figure 1, reproduced below, depicts an embodiment of the apparatus to stabilize a supplied voltage during a clock signal frequency locking process. *Id.* at 1:31–33.

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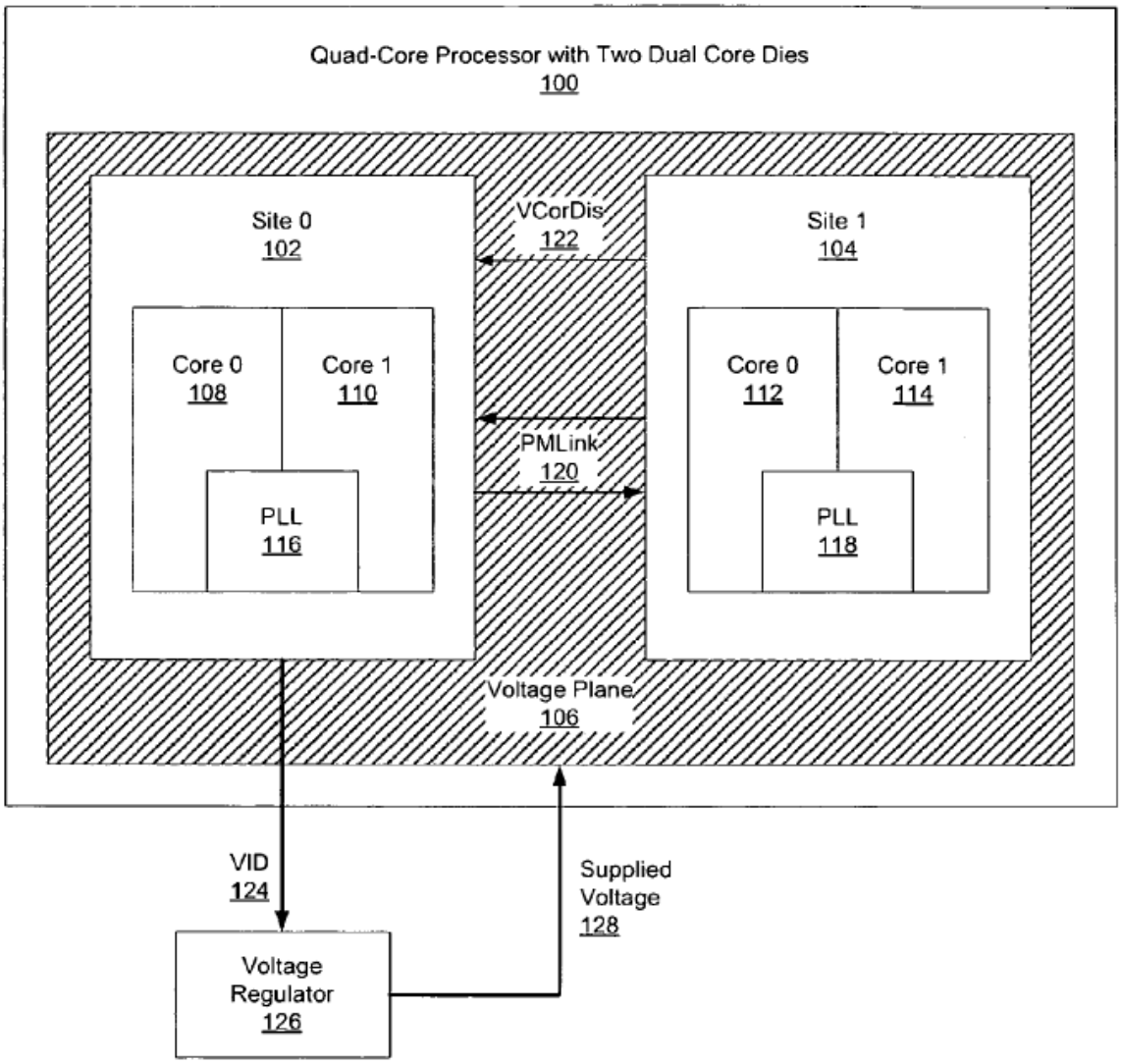

FIG. 1

Figure 1 depicts quad-core processor with two dual core dies 100. *Id.* at 2:41–42. Processor 100 includes site 0 and site 1 coupled to voltage plane 106. *Id.* at 2:42–44. Site 0 includes processing core 108, processing core 110, and PLL 116. Site 1 similarly includes processing core 112, processing core 114, and PLL 118. *Id.* at 2:43–46. PLL 116 and PLL 118 generate a clock signal for their respective sites to use as a reference clock

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and may change the frequency of the clock signal through a relocking process. *Id.* at 2:52–55.

3. Analysis of Independent Claims 1 and 21

a. Petitioner's Contentions

Independent claim 1 recites, *inter alia*,

> 1[a2] . . . the first set of processor cores is configured to dynamically receive . . . a first output clock signal of a first phase lock loop (PLL) *having a first clock signal as input*;
>
> 1[b2] . . . the second set of processor cores is configured to dynamically receive . . . a second output clock signal of a second PLL *having a second clock signal as input*,
>
> 1[b4] *the first clock signal is independent from the second clock signal*.

Ex. 1001, 7:53–8:5 (emphasis added). Independent claim 21 recites substantially similar limitations. *Id.* at 10:15–37.

We first address Petitioner's contentions in pertinent part as follows. Petitioner contends that Knoth discloses a multiprocessor digital system that includes at least two processor cores. Pet. 18–19 (citing Ex. 1005 ¶ 23, Fig. 1A). Petitioner asserts that Knoth's "processor cores 110a-n operate independently through dedicated power and frequency management." *Id.* at 19 (citing Ex. 1005 ¶¶ 25–27, 31).

Petitioner contends that each processor core receives a clock signal from its respective clock ratio controller 106a-n. Pet. 22 (citing Ex. 1005 ¶¶ 27, 31). According to Petitioner, "each of clock ratio controllers 106a-n includes a phase locked loop (PLL) (for ease of discussion, referred to as PLL 202a-n corresponding to clock ratio controller 106a-n) (highlighted in

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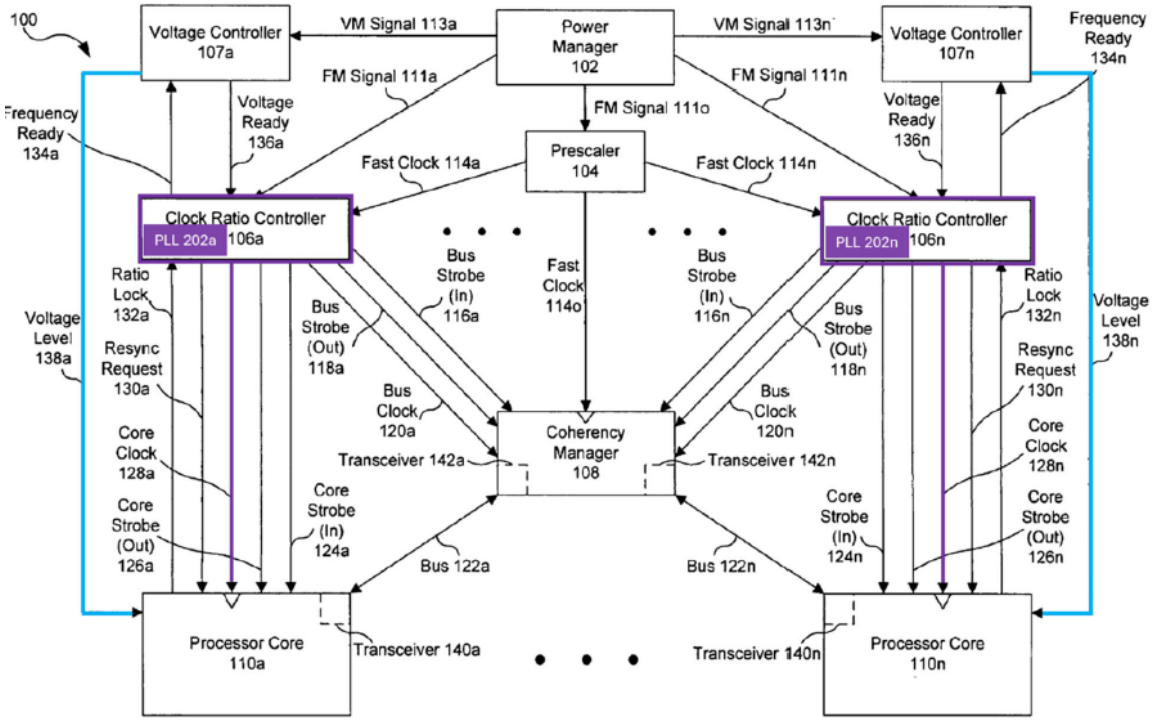
purple)."[9] *Id.* Petitioner depicts this arrangement in annotated Figure 1A of Knoth.



Petitioner's annotated Figure 1A depicts Knoth's multiprocessor digital system with clock ratio controllers 106a-n providing a clock signal to the respective processor cores 110a-n. *Id.* Petitioner annotates Figure 1A by adding a corresponding PLL 202a-n to each respective clock ratio controller 106a-n. *Id.*

Petitioner provides two alternatives as to how Knoth discloses a first PLL having a first clock signal as input and a second PLL having a second clock signal as input. Pet. 23. First, Petitioner contends that oscillator 219 provides timing pulses to a respective PLL. *Id.* (citing Ex. 1005 ¶¶ 41–42). Specifically, Petitioner asserts that an oscillator 219a-n would provide a

[9] We note that Knoth does not designate any individual PLL 202 as PLL 202a-n and instead describes only a single PLL 202. *See* Ex. 1005 ¶¶ 41–42, 49, 58, 61, 73, Fig. 2A.

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timing pulse to its corresponding clock ratio controller 106a-n.[10] *Id.* Alternatively, Petitioner contends that "each PLL within clock ratio controller 106 receives as input a 'PLL control signal 226' (for ease of discussion, referred to as PLL control signal 226a-n corresponding to clock ratio controller 106a-n."[11] *Id.* (citing Ex. 1005, Fig. 2A).

In sum, Petitioner asserts that Knoth discloses processor core 110a receiving a first output clock signal (core clock 128a) from PLL 202a. *Id.* at 24. Petitioner further asserts that PLL 202a receives a first clock signal as input from oscillator 219a or PLL control signal 226a. *Id.* at 24 (citing Ex. 1003 ¶ 116). Petitioner contends that processor core 110n similarly receives a core clock signal 128n from PLL 202n which receives a second clock signal as input from oscillator 219n or PLL control signal 226n. *Id.* at 24–25.

Petitioner further relies on Allarey as disclosing two PLLs with input clocks. Pet. 25 (citing Ex. 1003 ¶¶ 117–121). Specifically, Petitioner asserts that Allarey discloses that processor cores in site 0, cores 108 and 110, receive a clock signal generated by PLL 116. *Id.* (citing Ex. 1006, 2:38–3:3). Petitioner further asserts that processor cores in site 1, cores 112 and 114, receive a clock signal generated by PLL 118. *Id.* Petitioner contends that Allarey discloses that "[e]ach site includes a phase locked loop

[10] We note that Knoth does not designate an individual oscillator as 219a-n and instead describes only a single oscillator 219. *See* Ex. 1005 ¶ 42, Fig. 2A.

[11] We note that Knoth does not designate an individual PLL control signal 226 as 226a-n and instead describes only a single PLL control signal 226. *See* Ex. 1005 ¶¶ 42, 55, 61, Fig. 2A.

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(PLL) clock signal generation circuit" and "[e]ach PLL is capable of generating a clock signal." *Id.* at 26–27 (quoting Ex. 1006, 2:41–58).

Turning to element 1[b4], Petitioner contends that each of Knoth's clock ratio controller 106a-n operates independently because each receives "'individual frequency management (FM) signals 111a-n' that are 'used to individually control/scale the frequency of each processor core 110a-n.'" Pet. 28 (citing Ex. 1005 ¶ 25). Petitioner asserts that because the clock ratio controllers operate independently, "the first clock signal of the first PLL within clock ratio controller 106a is independent from the second clock signal of the second PLL within clock ratio controller 106n." *Id.* (citing Ex. 1003 ¶ 130). Relying on the declaration testimony of Dr. Baker, Petitioner contends that a POSITA "would read Knoth to include independent first and second PLLs within clock ratio controllers 106a and 106n, respectively, receiving the first and second clock signals (the timing pulses generated by oscillators 219a and 219n) that are independent from each other." *Id.* at 28–29 (citing Ex. 1003 ¶¶ 131–132).

Similarly, Petitioner contends that PLL control signals 226a and 226n are independent input clock signals. Pet. 29 (citing Ex. 1003 ¶ 133). According to Petitioner, each PLL control signal 226 is generated based on an independent voltage ready signal 136a-n and FM signal 111a-n. *Id.* (citing Ex. 1005 ¶¶ 25, 31, 55).

Finally, Petitioner contends that Allarey also discloses the first clock signal is independent from the second clock signal. Pet. 29 (citing Ex. 1003 ¶¶ 135–136). Specifically, Petitioner contends that Allarey discloses a separate PLL for each site. *Id.* (citing Ex. 1006, 2:41–58). As a result,

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Petitioner, relying on the declaration testimony of Dr. Baker, asserts that the PLLs are independent of each other. *Id.* (citing Ex. 1003 ¶ 136).

b. Patent Owner's Arguments

Patent Owner argues that the Petition fails to demonstrates how Knoth and Allarey disclose "a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal." Prelim. Resp. 5.

First, Patent Owner argues that the Petition fails to sufficiently show that Knoth discloses a first PLL receiving a first input clock signal and a second PLL receiving a second input clock signal. Specifically, Patent Owner argues that the Petition's identification of PLL 202a and PLL 202n of Knoth as the claimed first and second PLL fails because Knoth discloses only a single PLL 202. Prelim. Resp. 6. Patent Owner argues that PLL 202a and PLL 202n are not disclosed in Knoth, but are instead creations of Petitioner's expert Dr. Baker. *Id.* at 6, 8 (citing Ex. 1005 ¶ 41). Rather than multiple PLLs, Patent Owner argues that Knoth discloses a single PLL 202 coupled to a plurality of clock ratio controllers 106a-n. *Id.* at 8 (citing Ex. 1005 ¶¶ 22, 41). Patent Owner further argues that although Allarey discloses two PLLs, Petitioner does not sufficiently explain how or why Allarey's PLLs could be implemented in Knoth. Prelim. Resp. 9.

Second, Patent Owner argues that the Petition fails to sufficiently show that either Knoth or Allarey teaches or suggests the first input clock signal being independent from the second input clock signal. Prelim. Resp. 11–13. In particular, Patent Owner argues that Knoth teaches only a single PLL 202 with a single oscillator 219 providing a single input clock signal. *Id.* at 11 (citing Ex. 1005 ¶ 42). Further, Patent Owner argues that "[n]either

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the Petition nor Dr. Baker's declaration explain why it would be obvious or inherent or would be a [PHOSITA]'s reading that multiple PLLs, oscillators, or sets of timing pulses could or would be used." *Id.* at 14. With regard to Allarey, Patent Owner further argues that although Allarey discloses two PLLs, Petitioner has not shown that Allarey discloses any clock signals as inputs to its PLLs and thus further fails to show independent clock inputs for each PLL. *Id.* at 13 (citing Ex. 1006, 2:52–54; Ex. 1003 ¶ 121).

c. Analysis

For the following reasons, we agree with Patent Owner that Petitioner fails to sufficiently show that Knoth and Allarey teaches or suggests a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal, as claim 1 and 21 requires. Prelim. Resp. 5.

Having considered the evidence and arguments presented, we determine that Petitioner has not sufficiently shown that Knoth or Allarey disclose two independent clock signals. First, we are not persuaded that Petitioner has shown sufficiently that Knoth includes a PLL in each clock ratio controller. Instead, we agree with Patent Owner that Knoth discloses clock ratio controllers 106a-n coupled to a single PLL 202 where PLL 202 receives a single clock input from oscillator 119. Prelim. Resp. 6–8 (citing Ex. 1005 ¶¶ 22, 41, Fig. 2A). Figure 2A, reproduced above, clearly delineates clock ratio controller 106 within a dotted line separate from PLL 202 and oscillator 119. Further, as noted by Patent Owner, Knoth explicitly describes a plurality of clock ratio controllers and processor cores designated as a-n, but only describes a single PLL 202 and oscillator 119. *Id.* at 8, 11 (citing Ex. 1005 ¶¶ 22, 41–42). Because Petitioner has not shown that

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Knoth discloses two PLLs, Petitioner fails to show a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal.

Petitioner's reliance on Knoth's PLL control signals 226a and 226n fails for the same reasons. However, we further note that this reliance is further misplaced because control signal 226 is not a clock signals. Prelim. Resp. 12. Moreover, as with Petitioner's contentions regarding PLL 202, although Petitioner asserts Knoth discloses control signals 226a-n, Petitioner has not directed us to any disclosure in Knoth that describes a control signal other than a single PLL control signal 226. Pet. 29 (citing Ex. 1005 ¶ 55; Ex. 1003 ¶ 133).

Petitioner's position further relies on the declaration testimony of Dr. Baker who states a POSITA "would read Knoth to include independent first and second PLLs within clock ratio controllers 106a and 106n, respectively, receiving the first and second clock signals (the timing pulses generated by oscillators 219a and 219n) that are independent from each other." Pet. 28–29 (quoting Ex. 1003 ¶ 132, citing *id.* ¶¶ 111, 131). We do not credit Dr. Baker's testimony on this point because it lacks sufficient explanation and is inconsistent with the disclosure of Knoth as detailed above. 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight"); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (PTAB Aug. 24, 2022) (precedential). Dr. Baker's testimony appears premised on the assertion that each clock ratio controller 106a-n operate independently from each other. Ex. 1003 ¶ 130. However, Dr. Baker does not explain why

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independently operating clock ratio controllers teach or suggest that each clock ratio controller would receive an independent input clock signal.

We are further not persuaded by Petitioner's reliance on Allarey as disclosing a first clock input signal independent from a second clock input signal. Pet. 29 (citing Ex. 1006, 2:41–58; Ex. 1003 ¶¶ 135–136). Petitioner asserts that Allarey discloses sites 0 and 1 where each site includes an independent PLL and "[t]herefore, the first PLL clock signal generation circuit is independent from the second PLL clock signal generation circuit." *Id.* We are not persuaded by Petitioner's contention because Petitioner has not directed to us any disclosure in Allarey describing two independent input clock signals. *See* Pet. 26–27, 29. At best, Petitioner references Allarey's generation of a clock signal rather than an input clock signal thereto by stating that "[e]ach PLL is capable of generating a clock signal." Pet. 27 (citing Ex. 1006, 2:41–58).

Petitioner further relies on Dr. Baker who testifies that

> The PLL clock signal generation circuits are independent of each other since "each PLL can change the frequency of the clock signal through a relocking process." [Ex. 1006, 2:41–58]. When the PLL frequency is changed, the PLL clock signal generation circuit is also modified. Therefore, the first PLL clock signal generation circuit is independent from the second PLL clock signal generation circuit.

Ex. 1003 ¶ 136. Here again, we do not credit Dr. Baker's testimony because it does not provide sufficient explanation. In particular, Dr. Baker does not sufficiently explain why "the first PLL clock signal generation circuit [being] independent from the second PLL clock signal generation circuit" would teach or suggest that any input clock signals to the PLLs would be independent as claimed. Prelim. Resp. 14–15.

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For these reasons we agree with Patent Owner that the Petition fails to sufficiently demonstrate that Knoth and Allarey teach "a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal," as required by claims 1 and 21. Accordingly, we determine that the Petition fails to show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claims 1 and 21 in view of Knoth and Allarey.

4. Summary

For the foregoing reasons, Petitioner has not shown a reasonable likelihood of prevailing with respect to independent claims 1 or 21 for the asserted ground based on Knoth and Allarey. Petitioner's additional contentions regarding dependent claims 5, 8–10, and 14 do not cure these deficiencies regarding claim 1 and fail for the same reasons.

E. Ground 2: Alleged Obviousness over Knoth, Allarey, and Flautner

Petitioner asserts that claims 2–4 of the '339 patent would have been obvious over Knoth, Allarey, and Flautner. Pet. 52–58. Having reviewed the Petition, we find that Petitioner's reliance on Flautner does not cure the above-noted deficiencies with respect to independent claim 1. Accordingly, Petitioner does not show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claims 2–4 as obvious in view of Knoth, Allarey, and Flautner.

F. Ground 3: Alleged Obviousness over Knoth, Allarey, Wolfe, and Kumar

Petitioner asserts that claim 6 of the '339 patent would have been obvious over Knoth, Allarey, Wolfe, and Kumar. Pet. 58–64. Having reviewed the Petition, we find that Petitioner's reliance on Wolfe and Kumar does not cure the above-noted deficiencies with respect to independent claim

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1. Accordingly, Petitioner does not show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claim 6 as obvious in view of Knoth, Allarey, Wolfe, and Kumar.

G. Ground 4: Alleged Obviousness over Knoth, Allarey, and Wolfe

Petitioner asserts that claim 11 of the '339 patent would have been obvious over Knoth, Allarey, and Wolfe. Pet. 64–65. Having reviewed the Petition, we find that Petitioner's reliance on Wolfe does not cure the above-noted deficiencies with respect to independent claim 1. Accordingly, Petitioner does not show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claim 11 as obvious in view of Knoth, Allarey, and Wolfe.

H. Ground 5: Alleged Obviousness over Naffziger and Allarey

Petitioner asserts that claims 1–3, 5, 8–10, 14 and 21 of the '339 patent would have been obvious over Naffziger and Allarey. Pet. 65–91. For the reasons explained below, we determine that Petitioner has failed to demonstrate a reasonable likelihood of prevailing with respect to claims 1–3, 5, 8–10, 14 and 21.

Before addressing the parties' arguments, we provide an overview of the Naffziger reference.

1. Overview of Naffziger

Naffziger describes a method for controlling power consumption in a processor. Ex. 1010 ¶ 7. Naffziger discloses a processor including one or more processor cores and a power control unit. *Id.* ¶ 8. Figure 5, reproduced below, illustrates a processor having a power control unit and a plurality of processor cores. *Id.* ¶ 18.

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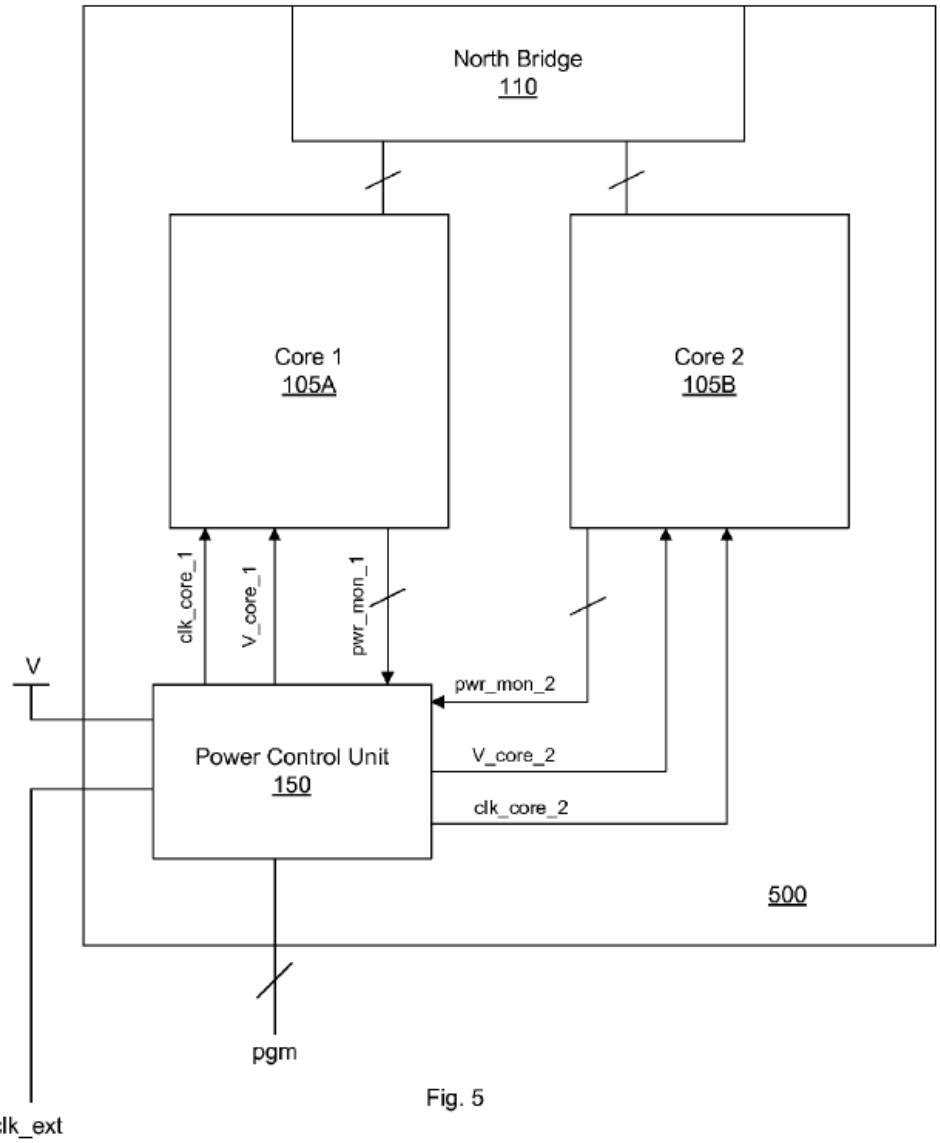

Fig. 5

Figure 5 depicts a processor 500 having first processor core 105A and second processor core 105B. *Id.* ¶ 53. Power control unit 150 monitors the power of processor cores 105A and 105B and may assign operation of either core to a high or lower performance state by changing the frequency of clock signals clk_core_1 and clk_core_2 provided to respective processor cores 105A and 105B. *Id.*

Figure 2, reproduced below, illustrates power control unit 150. Ex. 1010 ¶ 15.

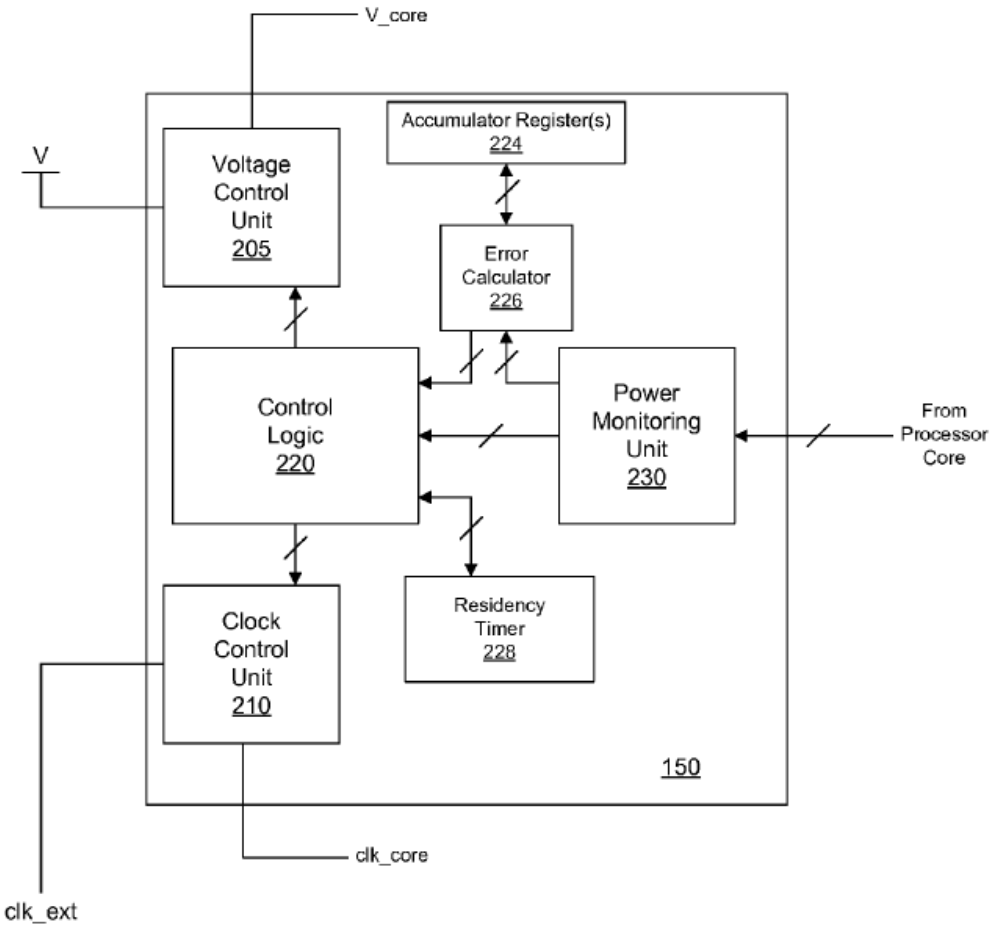

Fig. 2

Figure 2 depicts power control unit 150 including voltage control unit 205, clock control unit 210, control logic 220, accumulator register 224, error calculator 226, residency timer 228, and power monitoring unit 230. *Id.* ¶ 26. Clock control unit 210 may be implemented using a PLL. *Id.* ¶ 33.

2. Analysis of Claims 1 and 21

a. Petitioner's Contentions

As with Ground 1, we first address Petitioner's contentions with respect to limitations 1[a2], 1[b2], and 1[b4]. Petitioner's contentions are substantially similar for corresponding limitations in claim 21. Pet. 87–90. Petitioner relies on Allarey in the same manner as above in Ground 1. *See*

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id. at 71, 73, 75. Petitioner further contends Naffziger discloses a first processor core 105A receiving a first voltage supply and a first output clock signal of a PLL of power control unit 150. Pet. 68–69 (citing Ex. 1010 ¶ 55, Figs. 2, 5; Ex. 1003 ¶¶ 248–253). Petitioner further asserts that Naffziger discloses a second processor core 105B receiving a second voltage supply and a second output clock signal of a PLL of a second power control unit 150. *Id.* at 72–73 (citing Ex. 1010 ¶ 32, Figs. 2, 5; Ex. 1003 ¶¶ 256–260). Petitioner contends that "Naffziger discloses a power control unit 150 with separate, independent supply voltage and clock signal control planes, or alternatively, multiple power control units each associated with a corresponding process core, that regulates their core supply voltage and core clock frequency." *Id*. at 67–68 (citing Ex. 1010 ¶¶ 22–23, 30, 54, 55); *see id.* at 69 (citing Ex. 1010 ¶ 55). Petitioner further addresses the second power control unit asserting that a

> PHOSITA reading Naffziger would have understood that the multi-core processor 500 includes more than one power control unit 150 each associated with a corresponding core—a first power control unit 150 corresponding to the first core 105A (for ease of discussion, referred to as the "first power control unit 150A") and a second power control unit 150 corresponding to the second core 105B (for ease of discussion, referred to as the "second power control unit 150B").

Id. at 69 (citing Ex. 1003 ¶ 250).

Petitioner further asserts that "[e]ach power control unit 150 including the first power control unit 150A further includes the clock control unit 210 that 'us[es] a phase locked loop (PLL) . . . for adjusting the frequency of a clock signal.'" Pet. 70–71 (citing Ex. 1010 ¶ 33, Figs. 2, 5). Petitioner contends that each power control unit 150 dynamically provides a core clock signal to a processor core. *Id.* Petitioner asserts that "[t]he PLL of clock

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control unit 210 of the first power control unit 150A receives as an input 'an external clock signal, clk_ext.'" *Id.* at 71, 73 (citing Ex. 1010 ¶¶ 22, 33, Figs. 2, 5).

Petitioner further contends that Naffziger discloses first and second power control units receiving "first and second clock signals that are independent from each other." Pet. 74–75 (citing Ex. 1003 ¶ 264). Petitioner, relying on the declaration testimony of Dr. Baker, contends that "[a] PHOSITA would read Naffziger to include independent first and second power control units receiving the first and second clock signals that are independent from each other." *Id.*

d. Patent Owner's Arguments

Patent Owner argues that the Petition fails to demonstrates how Naffziger and Allarey disclose "a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal." Prelim. Resp. 15–16, 20–23. In particular, Patent Owner argues that Allarey fails for the reasons described above in Ground 1 and provides specific arguments as to Naffziger as follows. *Id.* at 23.

Patent Owner argues that Petitioner identifies only one clock input signal in Naffziger and thus fails to show two independent clock input signals as claimed. Prelim. Resp. 20–21 (citing Pet. 69, 72; Ex. 1010 ¶ 22). Specifically, Patent Owner contends that Naffziger discloses a "power control unit is coupled to receive an external clock signal, clk_ext, from a source external to processor 100." *Id.* at 21 (quoting Ex. 1010 ¶ 22, Fig. 5). Based on this disclosure and the arrangements depicted in Figures 2 and 5 reproduced above, Patent Owner argues that Naffziger discloses only a

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single clock input signal. *Id.* Therefore, Patent Owner argues that Petitioner improperly relies on the same clock input signal clk_ext as both claimed the first and second clock input signals. *Id.* at 21 (citing Pet. 69, 72; Ex. 1010, Fig. 5). Patent Owner further argues that Petitioner's reliance on Dr. Baker's testimony is insufficient because it fails to explain why a second power control system would include a separate independent external clock signal. *Id.* at 23.

e. Analysis

For the following reasons, we agree with Patent Owner that Petitioner fails to sufficiently show that Naffziger and Allarey teaches or suggests a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal, as claim 1 and 21 requires.

Petitioner asserts that Naffziger discloses a first processor core 105A and second processor core 105B receiving first and second output core clock signals from a PLL of power control unit 150. Pet. 68–69, 72–73 (citing Ex. 1010 ¶¶ 32, 55, Figs. 2, 5; Ex. 1003 ¶¶ 248–253, 256–260). Figure 5, depicts this arrangement with two processor cores coupled to a single power control unit 150. Ex. 1010, Fig. 5. In this embodiment, a single power control unit 150, depicted in Figure 2 above, includes a single clock control unit 210 in the form of a PLL receiving an input clock signal clk_ext. *Id.*

As noted by Petitioner, Naffziger contemplates an embodiment where the multi-core processor includes multiple power control units. Pet. 67–68 (citing Ex. 1010 ¶ 55). Naffgizer states:

> Another embodiment is contemplated wherein a multi-core processor includes multiple power control units, each of which is associated with a corresponding one of a plurality of

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> processor cores. In such an embodiment, each power control unit may separately control the states of operation of its corresponding core. The power control unit for each core may also monitor power consumption of the processor as a whole, which may be used, along with one or more power error terms, as a basis for determining the operational state of its corresponding processor core.

Ex. 1010 ¶ 55. Hence, Naffziger contemplates using two power control units to separately control operation of a corresponding core. *Id.* However, notably absent from this discussion is any explanation regarding input clock signal clk_ext. *See id.*

As noted by Patent Owner, Petitioner does not identify a second input clock signal in either Naffziger or Allarey. Prelim. Resp. 21–23. Instead, Petitioner relies on the declaration testimony of Dr. Baker who testifies that "[a] PHOSITA would read Naffziger to include independent first and second power control units receiving the first and second clock signals that are independent from each other." Pet. 74–75 (citing Ex. 1003 ¶ 264). Dr. Baker's testimony appears premised on the assertion that Naffziger discloses separate, independent power control units associated with the cores and thus a POSITA would understand that the power control units would receive independent input clock signals. *Id.* Here again, we do not credit Dr. Baker's testimony because it does not provide sufficient explanation. Instead, we agree with Patent Owner that Dr. Baker's testimony lacks adequate explanation as to why separate, independent power control units, each including a PLL, would necessarily receive separate independent input clock signals clk_ext. Prelim. Resp. 23. Indeed, as noted by Patent Owner, Naffziger's single PLL embodiment receives a single input clock signal clk_ext and provides separate output core clock signals to separate cores.

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Prelim. Resp. 9, 21 (citing Ex. 1010 ¶ 22, Fig. 5). In sum, although Petitioner demonstrates that Naffziger discloses using two PLLs, Petitioner has failed to adequately show that two PLLs receive separate, independent input clock signals.

For these reasons we agree with Patent Owner that the Petition fails to sufficiently demonstrate that Naffziger and Allarey teach "a first and second PLL with respective first and second clock signals as inputs where the first clock signal is independent from the second clock signal," as required by independent claims 1 and 21. Accordingly, we determine that the Petition fails to show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claims 1 and 21 in view of Naffziger and Allarey.

3. Summary

For the foregoing reasons, Petitioner has not shown a reasonable likelihood of prevailing with respect to independent claims 1 or 21 for the asserted ground based on Naffziger and Allarey. Petitioner's additional contentions regarding dependent claims 2–3, 5, 8–10, and 14 do not cure these deficiencies regarding claims 1 and 21, and fail for the same reasons.

I. Ground 6: Alleged Obviousness over Naffziger, Allarey, and Flautner

Petitioner asserts that claim 4 of the '339 patent would have been obvious over Naffziger, Allarey, and Flautner. Pet. 91–92. Having reviewed the Petition, we find that Petitioner's reliance on Flautner does not cure the above-noted deficiencies with respect to independent claims 1 and 21. Accordingly, Petitioner does not show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claim 4 as obvious in view of Naffziger, Allarey, and Flautner.

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J. Ground 7: Alleged Obviousness over Naffziger, Allarey, Wolfe, and Kumar

Petitioner asserts that claim 6 of the '339 patent would have been obvious over Naffziger, Allarey, Wolfe, and Kumar. Pet. 92–95. Having reviewed the Petition, we find that Petitioner's reliance on Wolfe and Kumar does not cure the above-noted deficiencies with respect to independent claims 1 and 21. Accordingly, Petitioner does not show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claim 6 as obvious in view of Naffziger, Allarey, Wolfe, and Kumar.

K. Ground 8: Alleged Obviousness over Naffziger, Allarey, and Wolfe

Petitioner asserts that claim 11 of the '339 patent would have been obvious over Naffziger, Allarey, and Wolfe. Pet. 95. Having reviewed the Petition, we find that Petitioner's reliance on Wolfe does not cure the above-noted deficiencies with respect to independent claims 1 and 21. Accordingly, Petitioner does not show that there is a reasonable likelihood that it would prevail in establishing unpatentability of claim 11 as obvious in view of Naffziger, Allarey, and Wolfe.

IV. CONCLUSION

For the foregoing reasons, we determine that Petitioner has not demonstrated on the record a reasonable likelihood that it will prevail in showing at least one of the challenged claims of the '339 patent is unpatentable.

V. ORDER

For the reasons given, it is

ORDERED that the Petition is *denied* as to all challenged claims, and no trial is instituted.

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