

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

NXP USA, INC. and QUALCOMM INCORPORATED,

Petitioners

v.

REDSTONE LOGICS LLC,

Patent Owner

Case: IPR2025-00485
U.S. Patent No. 8,549,339

**QUALCOMM INCORPORATED'S OPPOSITION TO
REDSTONE'S REQUEST FOR DISCRETIONARY DENIAL**

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Exhibit	Short Name	Description
EX1001	'339 Patent	U.S. Patent No. 8,549,339
EX1002	Annavaram Declaration	Declaration of Dr. Murali Annavaram
EX1003	Annavaram CV	<i>Curriculum Vitae</i> of Dr. Murali Annavaram
EX1004	Elgebaly	U.S. Patent App. Pub. No. 2007/0096775
EX1005	'339 Prosecution History	File History of U.S. Patent No. 8,549,339
EX1006	White	U.S. Patent No. 7,263,457
EX1007	Talwar	U.S. Patent App. Pub. No. 2009/0271646
EX1008	Williams	Williams et al., "Low Latency Clock Domain Transfer for Simultaneously Mesochronous, Plesiochronous and Heterochronous Interfaces," 13 th IEEE International Symposium on Asynchronous Circuits and Systems, 2007.
EX1009	RESERVED	RESERVED
EX1010	Cho	U.S. Patent App. Pub. No. 2010/0073068
EX1011	Vajda	U.S. Patent App. Pub. No. 2012/0060170
EX1012	RESERVED	RESERVED
EX1013	Ozer	U.S. Patent App. Pub. No. 2008/0209133
EX1014	NXP Complaint	Doc. No. 1, Complaint, <i>Redstone Logics LLC v. NXP Semiconductors N.V., et al.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1015	Qualcomm Complaint	Doc. No. 1, Complaint, <i>Redstone Logics LLC v. Qualcomm Inc., et al.</i> , No. 7:24-cv-00231-ADA (W.D. Tex.)

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EX1016	MediaTek Complaint	Doc. No. 1, Complaint, <i>Redstone Logics LLC v. MediaTek, Inc., et al.</i> , No. 7:24-cv-00029-DC-DTG (W.D. Tex.)
EX1017	NXP Opening Claim Construction Brief	Doc. No. 39, Defendant NXP USA Inc.'s Opening Claim Construction Brief, <i>Redstone Logics LLC v. NXP USA, Inc.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1018	Redstone Responsive Claim Construction Brief	Doc. No. 41, Plaintiff's Responsive Claim Construction Brief, <i>Redstone Logics LLC v. NXP USA, Inc.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1019	Kaxiras Textbook	S. Kaxiras, Computer Architecture Techniques for Power-Efficiency, 2008.
EX1020	Fryman	U.S. Patent No. 8,312,225
EX1021	Capps	U.S. Patent No. 7,584,369
EX1022	Pelley	U.S. Patent No. 7,777,330
EX1023	Intel Multi-Core Processor White Paper	R. Ramanathan, Intel multi-core processors: Making the move to quad-core and beyond, Technology@Intel Magazine, December 2006.
EX1024	Panov Paper	Y. Panov, Design Considerations for 12-V/1.5-V, 50-A Voltage Regulator Modules, Power Electronics, IEEE Transactions on. 16. 10.1109/APEC.2000.826080.
EX1025	Flautner	U.S. Patent App. Pub. No. 2005/0034002
EX1026	Liptay 1968	J.S. Liptay, Structural aspects of the System/360 Model 85, II. The cache, IBM Systems Journal, Vol. 7, No. 1, 1968.
EX1027	Gold	U.S. Patent App. Pub. No. 2009/0063888

Exhibit	Short Name	Description
EX1028	Cesky	U.S. Patent No. 7,538,625
EX1029	Kim Paper	W. Kim, System Level Analysis of Fast, Per-Core DVFS using On-Chip Switching Regulators, 14 th International Symposium on High Performance Computer Architecture, February 2008.
EX1030	Stenstrom Paper	P. Senstrom, A Survey of Cache Coherence Schemes for Multiprocessors, Computer, Volume 23, Issue 6, June 1990.
EX1031	Campbell	U.S. Patent No. 10,482,952
EX1032	Crandall	U.S. Patent No. 4,873,703
EX1033	Kato	U.S. Patent App. Pub. No. 2004/0210738
EX1034	Redstone / NXP Infringement Chart	Doc. No. 1-2, Exhibit 2 to Redstone's Complaint, <i>Redstone Logics LLC v. NXP Semiconductors N.V., et al.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1035	Redstone / Qualcomm Infringement Chart	Doc. No. 14-2, Exhibit 2 to Redstone's Second Amended Complaint, <i>Redstone Logics LLC v. Qualcomm Inc., et al.</i> , No. 7:24-cv-00231-ADA (W.D. Tex.)
EX1036	Ishimi	U.S. Patent No. 8,200,878
EX1037	Vajda PCT	WO 2010/138031
EX1038	Williams Paper IEEE Webpage	IEEE Webpage for Williams et al., "Low Latency Clock Domain Transfer for Simultaneously Mesochronous, Plesiochronous and Heterochronous Interfaces," 13 th IEEE International Symposium on Asynchronous Circuits and Systems, 2007. https://ieeexploreonorthbridgare.ieee.org/document/4137045 (last accessed on January 17, 2025).

Exhibit	Short Name	Description
EX1039	Tran Level Shifter Paper	C. Tran et al., “Low-power high-speed level shifter design for block-level dynamic voltage scaling environment,” International Conference on Integrated Circuit Design and Technology, 2005.
EX1040	Williams Paper PDF Metadata	Screenshot of EX1008’s pdf metadata, generated by Dr. Annavaram on January 20, 2025.
EX1041	NXP Return of Summons	Doc. No. 7, Proof of Service, <i>Redstone Logics LLC v. NXP Semiconductors N.V., et al.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1042	Motion to Stay NXP Litigation	Doc. No. 61, Joint Motion to Stay All Deadlines and Notice of Resolution, <i>Redstone Logics LLC v. NXP Semiconductors N.V., et al.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1043	Order Granting Stay of NXP Litigation	Doc. No. 62, Order Staying All Deadlines, <i>Redstone Logics LLC v. NXP Semiconductors N.V., et al.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1044	Motion to Dismiss NXP Litigation	Doc. No. 64, Joint Motion to Dismiss, <i>Redstone Logics LLC v. NXP Semiconductors N.V., et al.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1045	Order Dismissing NXP Litigation	Doc. No. 65, Order of Dismissal With Prejudice, <i>Redstone Logics LLC v. NXP Semiconductors N.V., et al.</i> , No. 7:24-cv-00028-DC-DTG (W.D. Tex.)
EX1046	Qualcomm Proof of Service	Doc. No. 7, Proof of Service for Qualcomm Incorporated, <i>Redstone Logics LLC v. Qualcomm Inc., et al.</i> , No. 7:24-cv-00231-ADA (W.D. Tex.)
EX1047	Judge Albright Time to Trial	Spreadsheet Compiling Time-to-Trial Data for Judge Albright, Western District of Texas, and Supporting Documents
EX1048	Joint Claim Construction Statement	Doc. No. 32, Joint Claim Construction Statement, <i>Redstone Logics LLC v. Qualcomm Inc., et al.</i> , No. 7:24-cv-00231-ADA (W.D. Tex.)

Exhibit	Short Name	Description
EX1049	Redstone <i>Markman</i> Brief	Doc. No. 28, Plaintiff's Responsive Claim Construction Brief, <i>Redstone Logics LLC v. Qualcomm Inc., et al.</i> , No. 7:24-cv-00231-ADA (W.D. Tex.)
EX1050	Snapdragon 835	<i>Qualcomm Details Snapdragon 835: Kryo 280 CPU, Adreno 540 GPU, X16 LTE</i> , AnandTech (Jan. 3, 2017) (archived Jan. 5, 2017 at: https://web.archive.org/web/20170105044350/https://www.anandtech.com/show/10948/qualcomm-snapdragon-835-kryo-280-adreno-540)

Discretionary denial is not warranted. Qualcomm filed its Petition within four months of being served with Redstone’s Complaint. Qualcomm has provided a full *Sotera* stipulation and agreed to forego reliance on any co-extensive system art. And concrete evidence shows that the Board would almost certainly issue its final written decision *before* the litigation reaches trial. The timing and Qualcomm’s stipulation “ensure[] that an inter partes review is a ‘true alternative’ to the district court proceeding.” *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 at 19 (PTAB Dec. 1, 2020) (designated Precedential Dec. 17, 2020). The two most important of the *Fintiv* factors thus weigh strongly in favor of institution, and the Board’s workload management factors do not suggest a different result. The Board should therefore advance Qualcomm’s petition to the merits panel.

I. The *Fintiv* Factors weigh in favor of institution.

Fintiv Factors 2 (timing) and 4 (lack of overlap) weigh strongly in favor of institution. *Fintiv* Factor 6 (other factors) also weighs in favor of institution. *Fintiv* Factors 1 (potential stay of litigation) and 3 (minimal investment in litigation) are, at worst, neutral. *Fintiv* Factor 5 (Qualcomm is the defendant in the litigation) does not outweigh the other factors. Thus, the *Fintiv* Factors favor institution.

A. *Fintiv* Factor 1: A stay has not yet been sought or ruled upon.

Qualcomm has not yet requested a stay of the litigation. The Board should “decline to infer, based on actions taken in different cases with different facts, how

the District Court would rule should a stay be requested by the parties in the parallel case here.” *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 12 (PTAB May 13, 2020) (designated Informative Jul. 13, 2020). As such, “[t]his factor does not weigh for or against discretionary denial in this case.” *Id.*

Further, Judge Albright has granted opposed motions to stay—even after conducting a *Markman* hearing—where, as here, (1) a petitioner agreed to be bound by the full scope of Section 315 estoppel, and (2) a final written decision invalidating all asserted claims would nullify Redstone’s infringement claims in the district court. *See Kirsch Research & Dev., LLC v. IKO Indus., Inc.*, No. 6:20-cv-00317-ADA (W.D. Tex. Oct. 4, 2021) (granting stay where petitioner “agree[d] to be estopped under the full scope of § 315(e)”); *Sonrai Memory Ltd. v. Western Digital Techs., Inc.*, No. 6:21-cv-01168-ADA (W.D. Tex. Aug. 14, 2022) (granting motion to stay filed post-*Markman*, even though case was “no longer in its early stages,” because breadth of estoppel would simplify issues and institution decision indicated a reasonable likelihood of invalidating multiple claims). Redstone’s arguments regarding the probability of a stay should therefore be disregarded.

This factor is therefore neutral.

B. *Fintiv* Factor 2: A Final Written Decision will likely precede trial.

Redstone concedes that “only the Qualcomm Litigation is relevant for *Fintiv* considerations.” Paper 7 at 4, n.2; *see also* Paper 8. Qualcomm filed its Petition on

January 22, 2025 (Paper 1), *less than four months* after receiving service of the Complaint. EX1046. Nearly two months later, the Board issued its Notice According Filing Date on March 12, 2025 (Paper 4), which sets a deadline of September 12, 2025, for institution and, if instituted, a deadline of September 12, 2026, for a Final Written Decision.

While trial in the litigation is currently scheduled for June 22, 2026 (EX2002, 5/5), over the past two years, *every* patent case reaching jury selection before Judge Albright has done so *after* the date initially set for scheduled jury selection. EX1048. Thus, the scheduled trial date just 21 months after filing is likely to be extended, and multiple datapoints suggest that any trial would occur after the Final Written Decision. First, the median 27.2 month time to trial over the past six years for the Western District of Texas is instructive. Paper 7 at 6 (citing EX2005). This alone would put the likely trial date for the litigation in late December 2026, which would be *three months after* a Final Written Decision in this proceeding.

Reflecting his very large patent docket, Judge Albright's median and average times to patent trial are even longer than the Western District median time to trial. *See* EX1047.¹ Specifically, over the past four years, the *median* time to trial for

¹ Patent infringement cases in which Judge Albright was the Article 3 Judge for all substantive work that ultimately reached trial, compiled with Docket Navigator and

patent cases in Judge Albright's court has trended upward from 27.1 months over the past four years, to 28.6 months over the past three years, to 30.2 months over the past two years, and to 32.9 months over the past one year. *See id.* Similarly, the *average* time to trial for patent cases reaching jury selection has trended upward from 28.9 months over the past four years, to 30.3 months over the past three years, to 32.3 months over the past two years, and to 33.9 months over the past one year. *See id.* Of these, even the number most favorable to Redstone—27.1 months median time-to-trial over the past four years—would also indicate a trial in the litigation around December of 2027, ***three months after*** a Final Written Decision here.

Ultimately, if the litigation does not reach trial by September 2026—*i.e.*, within 24 months of filing, then a Final Written Decision will beat trial. *See id.* Over the past two years, 21 out of 22 (95% of) patent cases reaching jury selection before Judge Albright took *at least* 25 months to do so, and 100% of those cases reached jury selection *after* the date initially set, *see* EX1047. Thus, the Board's final written decision here would almost certainly issue before the litigation reaches trial.

This factor therefore weighs strongly in favor of institution.

PACER. As indicated in the notes within the exhibit, the calculated mean and average time to trial numbers do not include cases that were not originally assigned to Judge Albright for substantive work but were later transferred to him.

C. *Fintiv* Factor 3: The parties have not invested sufficient resources in the litigation to weigh against institution.

The parties' and the Court's investment in the litigation has been minimal. Although the Court's *Markman* hearing preceded institution, Redstone omits that the parties requested construction of only three terms, one on substantive grounds and two that Qualcomm contended were indefinite. EX1048 (PO seeking "plain and ordinary meaning"). Ultimately, the modest investment in the construction of a single term is far from substantial enough to weigh in favor of discretionary denial.

Redstone's suggestion that "fact discovery will be nearing completion" is belied by the Court's order that fact discovery is only now open, following the *Markman* hearing. EX2002, 3/5 ("6/10/2025 Fact Discovery opens..."). Although fact discovery is currently scheduled to close on January 12, 2026, given the scheduling realities noted above, this date is very likely to be extended. Even under the current schedule, virtually all fact discovery and all expert discovery will remain to be done as of institution.

Redstone further stretches credulity by suggesting undue delay in filing the Petition. Paper 7 at 9. Redstone argued that "Qualcomm is taking advantage of their counsel's work for NXP and thus could have easily filed much sooner." *Id.* But this is speculation on the part of Redstone's counsel, and nonsensical speculation at that. Indeed, there would have been no benefit to Qualcomm in delaying the filing of the Petition. Redstone's speculation of delay is undercut by Redstone's concessions that

(1) “only the Qualcomm district court case is relevant for *Fintiv* considerations” (Paper 7 at 4, n.2) and (2) NXP’s invalidity contentions did ***not*** include all references on which the Petition’s grounds rely. Paper 7 at 9. Qualcomm moved forward diligently with its own searching, identification of prior art, decision to prepare a petition, and ultimate filing of the instant Petition, all in ***less than four months*** after service of the Complaint. That NXP was ultimately a co-petitioner does not support an inference that Qualcomm in any way delayed preparing and filing the Petition, and Redstone’s concessions objectively confirm that Qualcomm was diligent and prompt in its filing.

Given that fact discovery will have opened just a few months before institution, the deliberate speed of preparing and filing the Petition, and Qualcomm’s investment of resources in doing so, this factor weighs in favor of institution.

D. *Fintiv* Factor 4: Qualcomm’s full *Sotera* stipulation mitigates any risk of overlap or conflicting decisions.

Qualcomm provided a *Sotera* stipulation (EX1012), and an agreement to forgo use at trial of any system art that is coextensive with grounds that could have been raised in Qualcomm’s Petition (EX1021). Yet Redstone complains that substantial overlap ***might*** exist between the Petition’s grounds and the art Qualcomm may rely on in the litigation. Paper 7 at 10. But Redstone scrupulously avoids the details of Qualcomm’s *Sotera* stipulation, which is plainly broader than what might

have been allowed under the Federal Circuit’s decision in *Ingenisco Inc. v. IOENGINE, LLC*, No. 2023-1367, 2025 WL 1318188, at *7 (Fed. Cir. May 7, 2025).

The Board already rejected Redstone’s argument that the language in Qualcomm’s stipulation is “‘unclear’ as to whether Petitioner reserves the right to proceed based on other references cited in the invalidity contentions.” *Sotera*, IPR2020-01019, Paper 12 at 18. Here, as in *Sotera*, “Petitioner’s stipulation here mitigates any concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions.” *Id.* at 19.

Redstone’s reference to *Ingenico* is a red herring. First, Redstone’s suggestion that it “requested Petitioners clarify” their stipulation because it was made “before the Federal Circuit’s clarification [in *Ingenico*]” is misleading. *See* Paper 7 at 12. Qualcomm provided clarification on April 20, *before* the May 7 *Ingenico* decision. Second, rather than shirking or hedging, Qualcomm confirmed the full scope of its *Sotera* stipulation, *i.e.*, that it “is intended to cover the full extent of estoppel that would exist under 35 U.S.C. §315(e)(2) upon entry of a Final Written Decision.” EX2021. Qualcomm expressly “commit[ted] to follow the standard that Judge Albright set forth in *Hafeman v. LG Elecs., Inc.*, 2023 U.S. Dist. LEXIS 119846, *3 (W.D. Tex. April 12, 2023) ... that system art where there is no substantive difference between a printed publication and the system art is included in 35 U.S.C. 315(e)(2) estoppel.” *Id.* (nested quotations omitted). Notably, Qualcomm has not

rescinded or otherwise limited that commitment following the Federal Circuit’s recent decision, meaning *Ingenico* in no way undermines the extent of the *Sotera* stipulation here. Redstone’s remaining speculation is just that. Judge Albright is willing and able to address such issues, just as in *Hafeman*.

“Accordingly, Petitioner’s broad stipulation ensures that an inter partes review is a ‘true alternative’ to the district court proceeding.” *Sotera*, IPR2020-01919, Paper 12 at 19. As in *Sotera*, this factor therefore “weighs strongly in favor of not exercising discretion to deny institution under 35 U.S.C. § 314(a).” *Id.*

E. *Fintiv* Factor 5: That Qualcomm is a defendant, standing alone, does not outweigh the remaining factors.

Though outweighed by the rest of the factors, the Board has previously found that when, as here, Petitioner is the defendant in the litigation, “this factor weighs in favor of discretionary denial.” *Fintiv*, IPR2020-00019, Paper 15 at 12.

F. *Fintiv* Factor 6: Other factors also weigh in favor of institution.

Redstone makes passing reference here to the Board’s workload management factors. Paper 7 at 14-15. For the reasons detailed below in Section II, those factors also weigh strongly in favor of institution.

II. The Board’s workload management factors weigh in favor of institution.

A. Neither the PTAB nor any court has adjudicated the validity of the challenged claims.

None of the proposed grounds were before the Examiner during prosecution. Only a single prior art reference (White) was cited in an information disclosure

statement, but it was not a part of any rejection. White included disclosure of a particular claim feature—independent clock sources—that the Examiner mistakenly concluded was not in the prior art of record. Thus, the Examiner did *not* consider the Petitions’ proposed grounds. Even if the Board were to proceed to the second step of the *Advanced Bionics* framework, the Examiner erred in overlooking material disclosure in White, the only one of the proposed grounds’ seven references to have been included in an IDS. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (designated Precedential Mar. 24, 2020) (establishing two-part framework to evaluate the exercise of discretion).

The recent *Ecto World* decision addressed the *Advanced Bionics* framework where all art relied on for proposed grounds was before the Examiner during prosecution. *Ecto World, LLC v. RAI Strategic Holdings, Inc.*, IPR2024-01280, Paper 13 at 4, 5-6 (PTAB May 19, 2025) (designated Precedential May 19, 2025); *id.*, Paper 9 at 35 (“all of the Petition’s cited references were before the Examiner during prosecution [via IDS]”). In those circumstances, “[c]hallenging the claims using the same prior art that was previously presented in an IDS is sufficient to satisfy the first part of the *Advanced Bionics* framework,” even when “the Examiner did not apply the reference.” *Id.* at 4 (citing *Advanced Bionics*, IPR2019-01469, Paper 6 at 7-8. *Ecto World* does not, however, stand for a new and broad proposition

that the first part of the *Advanced Bionics* framework is necessarily met where merely ***one of*** a petition’s multiple prior art references was cited in an IDS.

If the first part of the *Advanced Bionics* framework is met, “a petitioner must explain, with reference to *Becton Dickinson* factors (c), (e), and (f), how the Examiner erred in overlooking the prior art. *Ecto World*, IPR2024-01280, Paper 13 at 5. “For example, a petitioner may argue that it satisfies the second part of *Advanced Bionics* because the asserted prior art was not a basis for rejection during examination, is not substantially the same as prior art the Examiner applied, and includes specific teachings that ‘impact the patentability of the challenged claims.’” *Id.* (citing *Advanced Bionics*, IPR2019-01469, Paper 6 at 8, n.9). Even if the first part of the *Advanced Bionics* framework were met for any of the ***proposed grounds*** in the Petition—which Qualcomm does not concede—the second part is met and discretionary denial is not appropriate.

1. The Examiner did not consider Elgebaly-Ozer (Grounds 4-7).

Elgebaly and Ozer were not before the Examiner during prosecution. *See* EX1001 at 1/12. Redstone does not assert that either is substantially the same as any art considered by the Examiner. *See* Paper 7 at 16-20. They are not. For example, the applicant distinguished the art relied upon by the Examiner as not “having ***sets of processor cores*** configured to receive multiple and independent clock signals.” EX1049, 8/21 (quoting EX1005, 84/194). In contrast, Elgebaly discloses multiple

reference clocks sources providing independent clock signals to respective sets of cores. *See* Paper 1 at 51-54. Moreover, the applicant also distinguished the art relied upon by the Examiner as ***not*** “disclos[ing] or teach[ing] a first set of processor cores and a second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, respectively.” EX1005, 82/194. In contrast, Elgebaly discloses ***sets of cores*** receiving ***respective supply voltages*** that may be ***independently set*** for each such set of cores. *See* Paper 1 at 54-55 (citing EX1004, [0033]); EX1002, ¶144).

Thus, the first part of the *Advanced Bionics* framework is not met for Elgebaly and Ozer, individually or in combination.

2. The Examiner did not consider *White-Talwar (Grounds 1.3)*.

(a) *Advanced Bionics Part 1: the White-Talwar combination* was not before the Examiner.

There is no dispute that Talwar was not before the Examiner, and therefore could not have been considered. White alone was cited in an IDS, but it was not addressed by the Examiner. *See* Paper 1 at 5-6; *see also Ecto World*, IPR2024-01280, Paper 13 at 4, 5-6. Talwar also discloses claimed features that, as the applicant argued and the Examiner agreed, were not present in the art that was addressed. Redstone nevertheless contends that (1) even if White was not considered, Kim discloses a similar architecture and was considered; and (b) Talwar discloses nothing more than Jacobowitz, which was considered by the Office. *See* Paper 7 at 18-20.

But Talwar is not substantially the same as Jacobowitz and, therefore, the first part of the *Advanced Bionics* framework is not met because the White-Talwar combination was not before the Examiner.

(1) *White is not substantially the same as Kim.*

White is materially different than Kim. White's explicit disclosure teaches or at least directly suggests multiple PLLs receiving as input independent clock signals from "multiple clock sources." Kim does not, as argued by the applicant during prosecution and highlighted by Redstone in its recent *Markman* briefing. *See* Paper 7 at 19; EX1049, 4/21 (quoting EX1005, 83-84/194). Yet Redstone contends that "[a]s the Petition describes White, it mirrors the relevant architecture of Kim." But Redstone does so based on the false premise that both references disclose only a single main PLL feeding additional PLLs at individual cores. Paper 7 at 19-20. Redstone overlooks *at least* what the Petition explains as the first and second of three configurations disclosed or directly suggested by White's explicit disclosure:

First Configuration: Frequency regulator 140 includes "multiple clock sources" in the form of multiple crystal "oscillators" "in order to supply multiple, independent clock signals of different frequencies" (EX1006, 7:40-45), each feeding "a phase-locked loop (PLL)" at one of logic cores 120A or 120B (*id.*, 9:62-65). EX1002, ¶62.

Second Configuration: Frequency regulator 140 includes "multiple clock sources" in the form of *multiple PLL's*, each fed by a corresponding crystal "oscillator" "in order to supply multiple,

independent clock signals of different frequencies” (EX1006, 7:40-45), each feeding “a phase-locked loop (PLL)” at one of logic cores 120A or 120B, or directly feeding the cores themselves (*id.*, 9:62-65). EX1002, ¶63; EX1008, FIG. 1, Section VII.C

This highlights a key substantive difference between the disclosure of Kim and the disclosure of White—namely that Kim is limited to “a [single] main PLL 260” fed by a single “clock source 270.” Paper 7 at 19 (quoting EX2018, ¶[0025]). Indeed, Applicant focused on this during prosecution:

Kim also fails to disclose or teach a first set of processor cores and a second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal [as input], respectively. ... ***Instead***, Kim discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) ***having a single clock source (i.e., 170 in FIG. 1 or 270 in FIG. 2).***

EX1005, 83-84/194. Elsewhere in its request for discretionary denial, Redstone confirms that this difference is material via its argument that MediaTek’s IPR failed because “there was no disclosure of two PLLs as claimed.” Paper 7 at 17.²

² Redstone does not attempt any substantive comparison of the art cited in Qualcomm’s Petition to the art cited in the MediaTek petition. Paper 12 at 17. Instead, Redstone contends in passing that “[t]he instant Petition suffers from the

(2) *Talwar is not substantially the same as Jacobowitz.*

“Talwar discloses a multi-core processor design in which ‘[t]he cores and voltage sources are divided into clusters, whereby multiple cores in a cluster receive power from a single voltage source’ and ‘[e]ach cluster may have a different cluster frequency,’ but ‘all the cores in a cluster [operate] at the same frequency.’” Paper 1 at 24-25 (citing EX1007, [0011], [0018]-[0019]). Jacobowitz does not disclose such clusters, according to both the applicant during prosecution and Redstone in its recent *Markman* briefing. See Paper 7 at 20; EX1049, 8/21 (quoting EX1005, 84/194).

Yet Redstone here contends that “[g]iven all the Petition points to Talwar for is clusters of cores, ... and Jacobowitz provides sets of ‘four cores 102,’ ..., Talwar is not a source for anything new.” Paper 7 at 20 (citing Paper 1 at 24-25; EX2019, [0025]). Redstone’s characterization conflicts with its reliance in the litigation on the prosecution argument that “neither Jacobowitz nor Kim discloses having sets of processor cores configured to receive multiple and independent clock signals.”

same deficiencies, there is no disclosure of two PLLs as claimed and expert testimony otherwise is entirely conclusory.” *Id.* But that is demonstrably wrong. See, e.g., Paper 1 at 11-13 (citing, *inter alia*, EX1008, Figure 1), 21-23 (explaining in detail why White discloses or at least directly suggests multiple PLLs).

EX1049, 8/21 (quoting EX1005, 84/194). Redstone's characterization of the Petition's reliance on Talwar is also not supported by any particular language of either.

Likewise, even a cursory comparison of Talwar and Jacobowitz belies Redstone's assertion that the two are coextensive. For example, independent claim 1 was rejected as anticipated by Jacobowitz (not a combination of Jacobowitz and Kim). *See* EX1005, 82-85/194. In response, the applicant argued:

Jacobowitz fails to disclose or teach a first set of processor cores and a second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, respectively. In addition, the first supply voltage is independent from the second supply voltage, as required in the independent claims 1 and 21. ... In other words, *Jacobowitz* is silent with respect to least the recited different sets of processor cores configured to receive independent supply voltages.

EX1005, 82/194. During prosecution, the applicant also argued that Kim also lacked any disclosure of clusters of cores each receiving independent voltages: "Instead, *Kim* discloses having each core, not a set of processor cores, received a [voltage]...." EX1005, 83. Thus, in addition to being distinct from Jacobowitz, the teachings of Talwar are not substantially the same as any of the art relied upon by the Examiner.

In the litigation, Redstone highlighted the prosecution history argument that "neither Jacobowitz nor Kim discloses having ***sets of processor cores*** configured to receive multiple and independent clock signals." EX1049, 8/21 (quoting EX1005,

84/194). Redstone cannot make that same argument against Talwar because, as explained in the Petition, Talwar plainly does disclose sets of processor cores configured to receive multiple and independent clock signals:

Talwar discloses a multi-core processor design in which “[t]he cores and voltage sources are divided into clusters, whereby multiple cores in a cluster receive power from a single voltage source” and “[e]ach cluster may have a different cluster frequency,” but “all the cores in a cluster [operate] at the same frequency.” EX1007, [0011], [0018]-[0019]. The values of: (a) the “single voltage source” for the cluster, and (b) “the frequency of all cores in a cluster” can be adjusted “[d]uring power management.” *Id.*, [0011]-[0012], [0018-0019], [0021-0025], [0030] (“The cores in a cluster ... can be independently controlled from other clusters.”). Providing one voltage and clock source *per cluster* enables “maximum power savings” by efficiently performing DVFS on each cluster in “stark contrast to conventional multi-core chips” with only a single voltage source. *Id.*, [0012], [0021]; EX1002, ¶69.

Paper 1 at 24-25.

Talwar therefore presents material disclosure—of sets of processor cores dynamically receiving respective, independent supply voltages—that was not before the Office during prosecution. Thus, the first part of the *Advanced Bionics* framework is *not* met because neither the White-Talwar combination nor the substance thereof were before the Office during prosecution.

(b) *Advanced Bionics* Part 2: Examiner materially erred by overlooking White’s disclosure of multiple, independent clock sources.

Should the Board determine that the substance of White-Talwar was before the Office, the Examiner materially erred by not relying on their respective disclosures of multiple sources for generating independent clock signals and clusters of cores with independent voltage sources. The relevant *Becton Dickinson* factors are: “(c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;” “(e) whether a Petitioner has pointed out sufficiently how the Examiner erred in its evaluation the asserted prior art,” and “(f) the extent to which additional evidence and facts presented in the Petitioner warrant reconsideration of the prior art or arguments.” *Advanced Bionics*, IPR2019-01469, Paper 6 at 9, fn.10.

As to factor (c), White was not the basis of any rejection, nor is there any suggestion in the record that White was discussed by the Examiner or the applicant.

As to factor (e), as explained in Section II.A.2(a)(1) above, White’s explicit disclosure describes or at least directly suggests the “multiple clock sources” in the form of crystal oscillators or PLLs that generate independent clock signals for corresponding PLLs (*see* Paper 1 at 22-23) that Redstone contends was missing from Kim, which is instead limited to “a [single] main PLL 260” fed by a single clock source. Paper 7 at 19 (quoting EX2018, ¶[0025]). The Examiner materially erred by

overlooking White's disclosure and apparently agreeing with the applicant's assertion that "neither Jacobowitz nor Kim discloses having sets of processor cores configured to receive multiple and independent clock signals." EX1049, 8/21 (quoting EX1005, 84/194, 11/29/2012 OA Response); *see* EX1005, 59/194 (2/14/2013 Notice of Allowance following 11/29/2012 OA Response).

As to factor (f), the Petition presents additional prior art references that were not before the Examiner during prosecution. For example, as explained above, Talwar, Elgebaly, or Ozer were not cited in prosecution. Indeed, the Petition presents proposed grounds based on prior art combinations that were not considered by the Examiner. Those combinations plainly disclose and explicitly suggest elements of every challenged independent claim that the Examiner concluded were not present in the prior art cited during prosecution. Finally, the Petition also presents additional evidence of the state of the art, as of the filing date of the application leading to the challenged patent, that shows that dynamic voltage and frequency scaling (DVFS), including in multi-core processors with sets of cores receiving independent clock signals and voltages, was already known in the art. *See, e.g.*, Paper 1 at 9-15. Thus, to the extent the Board may be concerned that the White reference was before the Examiner and is sufficient to meet part one of the *Advanced Bionics* framework, part two of the *Advanced Bionics* framework would also be met.

B. There are no relevant changes in the applicable law.

The Petition's proposed grounds do not rely on any intervening change in law.

C. The proposed grounds are strong, and the expert testimony on which the proposed grounds rely is appropriate in scope.

For the reasons explained above, each of the Petition's White-Talwar combination and Elgebaly-Ozer combination explicitly discloses and suggests features of the independent claims that the Examiner incorrectly concluded were not found in the prior art. And the Petition's proposed grounds are supported by reasoned expert testimony that meticulously finds support in additional prior art evidence. Despite the evidence to the contrary, Redstone erroneously contends that the Petition has "severe facial flaws, many related to its reliance on expert testimony." Paper 7 at 22. But Redstone can only do so by recasting the proposed grounds and offering only attorney argument to dispute reasoned expert opinions. Ultimately, Redstone's objections fall flat.

1. The White-Talwar grounds are strong and rely appropriately on Dr. Annavaram's reasoned testimony.

For Ground 1 based on White and Talwar, after exploring relevant aspects of the state of the art generally (Paper 1 at 9-15) and the particular teachings of White and Talwar individually (Paper 1 at 21-25), the Petition explains that "[a] POSITA would be motivated to apply Talwar's DVFS 'clustering' of processor cores to White's DVFS implementation in order to achieve the goal common to White and

Talwar—DVFS in a multicore processor below the chip level—while meeting practical chip constraints.” Paper 1 at 25 (citing EX1002, ¶71). The Petition goes on to explain that, based on White’s explanation “that a device may ‘include *any number of logic cores* configured to operate at independent voltages and/or frequencies,’” but that a POSITA “would have understood such a design would need to be adapted as the number of cores increases due to chip space constraints associated with adding an additional voltage and clock control and supply circuitry for each additional core.” Paper 1 at 24-25 (citing EX1002, ¶¶73-74 (citing EX1029, 3-4/12, EX1019, 52-53/219)). Nevertheless, Redstone recasts the preceding sentence as “the only basis the Petition enumerates for making such a modification.” Paper 7 at 22. As highlighted above, the White-Talwar combination is a logical and obvious application of their express teachings.

The Petition and Dr. Annavaram explain the context of the art and the reasons that a POSITA reading the explicit teachings of White and Talwar, would have been motivated to combine them in a way that includes clusters of cores receiving independent clock sources and voltages. Moreover, Dr. Annavaram’s explanation of the particular “space constraints” point is supported by objective, documentary evidence explaining both (a) the tradeoffs between implementing DVFS at more-granular levels (per-core) and less-granular levels (per-chip), and (b) the well-known

space constraints that would have motivated a POSITA to utilize Talwar's clustered approach. EX1002, ¶¶33-36, 73-74.

Redstone, on the other hand, repeatedly offers only attorney argument to disagree with Dr. Annavaram's reasoned explanations. *See* Paper 7 at 22-30. Lacking substantive objection to Dr. Annavaram's testimony, Redstone resorts to characterizing the references supporting Dr. Annavaram's explanation as merely "academic," "tertiary," or themselves "not part of any ground." *See, e.g.*, Paper 7 at 23, 28. Redstone seems to imply that these "academic" and "tertiary" references are the sole support for applying DVFS to clusters of cores, and then fault those references for failing to explicitly disclose that point. *See, e.g.*, Paper 7 at 23-26. But Talwar itself expressly discloses different core clusters on the same chip receiving respective voltages and frequencies. *See* Paper 1 at 24-25. Thus, each of Redstone's criticisms of Grounds 1-3 fail.

2. The Elgebaly-Ozer grounds are strong and rely appropriately on Dr. Annavaram's reasoned testimony.

The Elgebaly-Ozer grounds also address the claim elements—*i.e.*, sets of cores receiving independent clock signals and voltages—that the Examiner mistakenly concluded were not disclosed or suggested in the prior art. After exploring relevant aspects of the state of the art generally (Paper 1 at 9-15), the Petition addresses the particular teachings of Elgebaly and Ozer individually. Paper 1 at 50-59. Those teachings of Elgebaly include the elements that the Examiner

mistakenly concluded were not taught or suggested in the prior art, including (a) adaptive voltage scaling (AVS) to provide independent voltages to different cores and *sets of cores*, and (b) a plurality of PLLs with respective oscillators to provide multiple, independent clock signals to *sets of cores*. Paper 1 at 50-56 (quoting EX1004, [0033] (“multiple processing cores may share a common clock and/or a common supply voltage that may be jointly set for these cores”)). Redstone responds that Dr. Annavaram fills gaps in the prior art references themselves and that his testimony is entitled to little weight. Both criticisms are mistaken.

(a) Dr. Annavaram’s opinions are fully supported.

First, Dr. Annavaram provides detailed explanations of his opinions and cites to objective, documentary evidence for support. The Petition follows that testimony closely. Redstone cites *Xerox Corp. v. Bytemark, Inc.* for the proposition that similarity between expert testimony and a petition counsels in favor of giving the expert opinion little weight. *See, e.g.*, Paper 7 at 28 (citing *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-17 (PTAB August 24, 2022) (designated Precedential Feb. 10, 2023)). But *Xerox* addresses only “conclusory assertion[s]. Where an expert provides a reasoned explanation supported by documentary evidence, as Dr. Annavaram does here, that the petition says the same means only that the expert testimony closely supports the grounds.

(b) Elgebaly discloses or at least directly suggests a plurality of PLLs with respective oscillators generating independent clock signals.

Second, the Petition and Dr. Annavarum explain that Elgebaly discloses a plurality of PLLs each controlling a respective oscillator to generate multiple, independent clock signals. Paper 1 at 52-53 (citing EX1004, [0032]-[0033], [0028]); *see also* EX1002, ¶¶141-142. The Petition and Dr. Annavaram then explain that “a POSITA would have understood Elgebaly’s disclosure of one or more PLLs and external circuitry including plural ‘crystals’ to include known clock distribution channels; specifically, multiple PLLs each receiving a distinct clock signal from a different external oscillator crystal and, in turn, outputting one of the desired clock signals.” Paper 1 at 53 (citing EX1002, ¶141). *Alternatively*, the Petition and Dr. Avarranam explain that “[a]t the very least, such a configuration was an obvious design choice that would have allowed a POSITA to implement multiple, independently-settable clock signals and thereby achieve Elgebaly’s flexibility and potential power savings.” Paper 1 at 53 (citing EX1002, ¶142).

Redstone does not challenge the explanation that Elgebaly expressly discloses “multiple PLLs each receiving a distinct clock signal from a different external oscillator crystal and, in turn, outputting one of the desired clock signals.” Paper 1 at 53 (citing EX1002, ¶141). For purposes of Redstone’s request for discretionary denial, that disclosure therefore stands unchallenged.

To the extent Redstone had argued against that explicit disclosure, the Petition also explained that “such a configuration using separate oscillators and PLLs was known, as explained in Section VII.C [of the Petition].” Paper 1 at 53 (citing, *inter alia*, EX1027, [0005] (“[t]he simplest way to implement multiple clock signals is to provide multiple oscillators.”); EX1008 (“Williams illustrates such a configuration with two external crystal oscillators each fed into a separate PLL:”); EX1002, ¶¶33-40. Redstone responds that this is insufficient because the Petition does not cite one individual reference using multiple PLLs to generate independent clock signals to *sets* of cores, and therefore cannot show that doing so was a “known technique.” Paper 7 at 28. But Redstone’s arguments conflate obviousness and anticipation. Redstone does not dispute that Elgebaly discloses generating multiple independent clock signals. Paper 1 at 52. And Redstone does not dispute Elgebaly’s teaching of core clusters: “multiple processing cores may share a common clock and/or a common supply voltage that may be jointly set for these cores.” Paper 1 at 54 (quoting EX1004, [0033]). To the extent Elgebaly even arguably lacks an explicit disclosure of using multiple PLLs with respective oscillators to generate independent clock signals (Paper 1 at 53), that that is precisely what the Petition and Dr. Annavaram show was known in Section VII.C of the Petition. Paper 1 at 11-12. Redstone’s objections on this point therefore fail.

(c) Elgebaly discloses or at least directly suggests core clusters receiving independent clocks and voltages.

Third, the Petition and Dr. Annavarum explain that Elgebaly discloses that its “ASIC 120 may include ... any number of processor cores.” Paper 1 at 54 (citing EX1004, [0030]. The Petition and Dr. Annavarum also explain that Elgebaly discloses that “multiple processing cores may share a common clock and/or a common supply voltage that may be jointly set for these cores.” Paper 1 at 54 (citing EX1004, [0033]); *see also* EX1002, ¶144. The Petition and Dr. Annavarum further explain that “Elgebaly therefore discloses *or* at least renders obvious a chip with four processor cores where: the first two of the processor cores share a first common clock, a first common supply voltage, and a first AVS Unit, and where the other two of the processor cores share a second common clock, a second common supply voltage, and a second AVS Unit....” Paper 1 at 54.

Redstone does not challenge the explanation that Elgebaly expressly “discloses ... a chip with four processor cores where: the first two of the processor cores share a first common clock, a first common supply voltage, and a first AVS Unit, and where the other two of the processor cores share a second common clock, a second common supply voltage, and a second AVS Unit....” Paper 1 at 54. For purposes of Redstone’s Request for Discretionary Denial, that disclosure therefore stands unchallenged.

To the extent Redstone had argued against that explicit disclosure, the Petition also explained that “Elgebaly ... at least renders obvious a chip with four processor cores where: the first two of the processor cores share a first common clock, a first common supply voltage, and a first AVS Unit, and where the other two of the processor cores share a second common clock, a second common supply voltage, and a second AVS Unit....” Paper 1 at 54. The Petition and Dr. Avarannam further explain that “[a] POSITA would have also understood that this type of core grouping was a well-known approach to balancing competing design factors.” Paper 1 at 55 (citing EX1002, ¶145). And the Petition and Dr. Annavaram support this proposition with reference to Talwar, which “disclos[es] that clusters of cores were known in the art.” Paper 1 at 56 (citing EX1007, [0011]-[0012]). Ultimately, Redstone does not take issue with the *quality* of that evidence, but the *quantity*, contending that “one example [Talwar] hardly establishes a ‘known technique to address a known problem.’” Paper 7 at 29-30. But Redstone does not address the bedrock principle that a POSITA is presumed to be aware of the prior art, and fails to provide any competing standard of “*known-ness*.” Redstone’s concession that Talwar discloses the known configuration thus sounds the death knell for Redstone’s sole substantive complaint about Ground 4.

The rest of Redstone’s objections to the Elgebaly-Ozer combination again, solely via attorney argument, attempt to dismiss objective, documentary evidence

supporting Dr. Annavaram’s opinions as merely “tertiary.” Redstone highlights as much with its promise to *eventually* support its arguments: “But individual cores and a single group of cores does not teach subdivisions larger than individual cores as will be further explored by Redstone’s expert.” Paper 7 at 29. At base, the Petition and Dr. Annavaram’s testimony speaks for itself, and Redstone fails to raise any meaningful challenges to their substance.

D. The challenged patent was not asserted until 2023.

The ’339 Patent was not asserted against Qualcomm until 2024, and was not asserted against anyone until 2023. Thus, the length of time it has been in force should not weigh in favor of discretionary denial. To find otherwise would implicitly demand that parties speculatively expend resources to challenge the validity of patents that *might* eventually be relevant to a product a company *might* eventually offer. That is not a workable solution, and would fly in the face of the efficiency Congress sought to promote with the America Invents Act. Taken to its logical conclusion, parties would speculatively divert resources away from research, innovation, and technology leadership into challenging patents that *might* be asserted, potentially overwhelming the Office with challenges to patents that are not the subject of any actual dispute between a patentee and the patent challenger.

Redstone contends that “the ’339 Patent has been in force since 2013” and that “of the three parties that have now challenged the ’339 Patent in an IPR, two are

in the process of settling their infringement of the '339 Patent.” Paper 30 at 30 (citing EX2023, EX2024). Of these two propositions, the second is objectively meritless. Redstone provides no factual details regarding these settlements or whether they were in any way merits-driven. Even if it had, Federal Rule of Evidence 408 plainly prohibits the use of a settlement to prove the validity of a disputed claim. FRE 408. It stands to reason that the settlement of *a third party*—on unknown terms for unknown reasons—can fare no better. Were it otherwise, the settlements could reasonably suggest that Redstone seeks to *avoid* defending validity of its patent at trial. But Redstone would of course object to such an inference.

Redstone’s first argument about the length of time the '339 Patent has been in force is but a myopic view of the overall picture of settled expectations. Indeed, Redstone accuses Qualcomm of infringing the '339 Patent via the Snapdragon 835 Mobile Platform, *which was publicly launched in 2016*. See EX1050. Yet Redstone does not address the impact of that delay on the “settled expectations” of the parties or provide any explanation of its yearslong delay in asserting the '339 Patent against these products. Redstone also glosses over the fact that the Petition’s art explicitly discloses elements of the challenged independent claims that the Examiner mistakenly concluded were not known in the prior art.

To rely solely on the length of time a patent has been in force would create a perverse incentive for patent owners, and particularly nonpracticing entities, to bide

their time before raising accusations of infringement, knowing that their own delay strengthens an impediment to AIA challenges (often while simultaneously increasing potential damages). That result would be facially nonsensical. As such, Redstone has not identified any settled expectations that might otherwise counsel against institution.

E. Economic interests also weigh in favor of institution.

Creating a forum for expeditious and economical adjudication of validity of patents that are simultaneously asserted in litigation is a principal function of the America Invents Act. Qualcomm does not seek to avoid litigating the validity of the '339 Patent; it merely seeks to do so in the efficient, purpose-built venue for patent validity trials. Doing so gives Redstone a full and fair opportunity to defend its patent, without having to address the same challenges in two different venues, while *also* respecting Qualcomm's ability to prioritize its investments in innovation.

Redstone's comments on the remaining PTAB workload factors merely rehash the rest of its brief. Redstone first relies on alleged "serious efficiency concerns under *Fintiv*." Paper 7 at 31. But, as explained above, these are fully mitigated by Qualcomm's full *Sotera* stipulation and the fact that a Final Written Decision is almost certain to issue months before the litigation reaches trial. Second, Redstone falsely states that "*half* the grounds are the same or substantially the same as those considered in prosecution." Paper 7 at 31. Not only is Redstone incorrect

on this point (*see* §II.A above; *see also* Paper 1 at 5-6), Redstone does not and cannot contend that *all* of the proposed grounds are the same or substantially the same as those considered during prosecution. *See* Paper 7 at 31. Third, Redstone argues that the proposed grounds fail to meet a “*substantial* likelihood of success” standard that is improper on its face. *See* Paper 7 at 31; *see also* 35 U.S.C. § 314 (“reasonable likelihood”). Accordingly, Redstone’s comments on this factor do not outweigh the remaining factors that weigh in favor of institution.

III. Conclusion

For the foregoing reasons, the Board should deny Redstone’s Request for Discretionary Denial.

Dated: June 12, 2025

Respectfully submitted,

/Eagle H. Robinson/

Eagle H. Robinson (Reg. No. 61,361)

*Lead Counsel for Co-Petitioner
Qualcomm Incorporated*

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned certifies that on June 12, 2025, copies of Co-Petitioner Qualcomm Incorporated's Opposition to PO's Request for Discretionary Denial, and EX1046-EX1050, were served on Patent Owner via email (by consent) to:

rmirzaie@raklaw.com
rak_redstone@raklaw.com
nrubin@raklaw.com
cconkle@raklaw.com
ptong@raklaw.com

/Eagle H. Robinson/
Eagle H. Robinson (Reg. No. 61,361)