

# EXHIBIT 17

**IN THE UNITED STATES DISTRICT COURT  
FOR THE WESTERN DISTRICT OF TEXAS  
AUSTIN DIVISION**

CONCURRENT VENTURES, LLC AND  
XTREAMEDGE, INC.,

Plaintiffs,

v.

ADVANCED MICRO DEVICES, INC. AND  
PENSANDO SYSTEMS, INC.,

Defendants.

Civil Action No. 1:24-cv-335-ADA

**Declaration of Bill Lin Regarding the '943 and '753 Patents**

I, Bill Lin declare as follows:

1. My name is Bill Lin. I am a Professor in the Department of Electrical and Computer Engineering at UC San Diego. I am over 18 years of age and competent to make this declaration. I make this declaration based upon my own personal knowledge and, if called upon to testify, would testify competently to the matters contained within. My background and qualifications can be found in section IV. My understanding of the legal principles concerning claim construction can be found in section V.

2. I have been retained as an expert by Defendants Advanced Micro Devices, Inc. and Pensando Systems, Inc. to offer my opinions concerning the proper construction of claim terms in U.S. Patent Nos. 10,985,943 and 10,873,753. I may offer additional opinions based on further review of materials in this case, including opinions and testimony of other expert witnesses.

3. I am being compensated at my standard customary hourly rate for time spent on this matter. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study, the substance of my testimony, or the outcome of this case. I have no personal or financial stake, nor any interest in the outcome of this proceeding.

**I. '943 Patent**

**A. Level of Ordinary Skill in the Art and Relevant Time Period**

4. From my review of the specification and the claims, it is my opinion that the relevant field of art for the '943 patent is PLDs and data processing systems. The specification discusses the need to improve prior art systems “for many data flow and data processing applications.” '943 pat., 1:6-21. “Video processing is one such data processing application....”

*Id.* PLDs are recited in each claim and discussed extensively in the embodiments. *E.g., id.*, 3:8-12, 4:27-47, 6:37-45, 5:25-38. The '943 patent is titled "Hardware Defined Anything..." which I understand is a reference to the user-definable hardware discussed in the patent's claims and specification. Embodiments of the alleged invention include "a platform for data flow processing" and "[a] programmable device for data flow processing." *Id.*, 1:23-44. The specification further explains that it provides "a variety of flexible features for hardware-defined and software-defined functionality in data streaming and data processing systems, including video." *Id.*, 2:47-3:20.

5. It is also my opinion that the level of ordinary skill in the field of art of the '943 patent would have been a person with a bachelor's degree in computer engineering, electrical engineering, or a similar major with at least two years of experience in the field (described above) or a person with a master's degree in computer engineering, electrical engineering, computer science, or a similar field with a specialization in the field (described above). A person with less education but more relevant practical experience may also meet this standard.

6. The '674 application that issued as the '943 patent was filed on July 15, 2018, claiming priority to itself. Accordingly, I have analyzed the claim terms in the '943 patent from the perspective of a POSITA as of July 15, 2018.

## **B. Technical Background**

7. Programmable logic devices ("PLDs") are a class of integrated circuit ("IC") devices that provide areas of logic circuits that users can configure after manufacturing. By changing the interconnection pattern of PLD circuits, users were able to create custom circuits that performed custom functions directly in hardware. This is in contrast to conventional ICs whose circuits are fixed when the IC is manufactured and cannot be changed by the users. For

example, the CPU in a PC or other computing device is fixed at manufacturing. Since the circuits inside the CPU cannot change, and the hardware functionality of the CPU is fixed, the PC is programmed using software programs that run on the CPU.

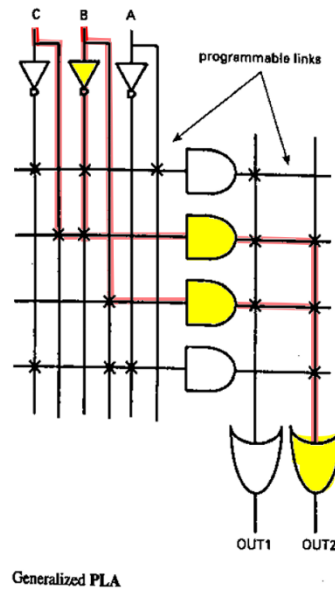
8. PLDs have been widely used in the art for decades and include a variety of device types including programmable read-only-memory (programmable ROM), programmable array logic (PAL), programmable logic arrays (PLA), complex programmable logic devices (CPLD), and Field Programmable Gate Arrays (FPGAs), among others. PLAs were common by the 1980s, and FPGAs were common by the 1990s. By the late 1990s, it was common for undergraduate EE courses to teach PLD programming, and related subject matter was covered in textbooks for courses such as digital design and computer architecture.

9. In general, PLDs include programmable interconnections between arrays of logic gates and other circuit elements. By altering the connection pattern of the circuits, users chose the electric paths over which signals were carried and the logic gates that they passed through. Because these circuits were based on logic gates that provide binary outputs, they were typically connected in digital circuits to perform logical (Boolean) functions, also referred to as combinational logic. In this way, PLDs, allowed users to create custom circuits directly in hardware that performed custom logic functions at hardware speeds.

10. Below, I will walk through several detailed examples of PLDs from textbooks and dictionaries. The common characteristic of these examples—and for PLDs generally—is that the user can alter the connection pattern of circuits inside the PLD.

11. The following figure from the Penguin Dictionary of Electronics provides a simplified diagram as an example of combinational array logic inside a PLD, where the user

alters the connection pattern using programmable links to create custom circuits and logic functions in the PLD.:



CV-AMD0017592 (enhanced for legibility and annotated). In greater detail, three input signals (A, B, and C) arrive at the top of the figure. Each passes through a NOT gate (triangle symbol) to invert the signal, leading to the opposite of each input ( $\bar{A}$ ,  $\bar{B}$ , and  $\bar{C}$ ).<sup>1</sup> As an example, I highlighted the path for signals for the logical equation  $B \text{ OR } (\bar{B} \& C)$  that is output at OUT2. In the first array of programmable links, fuse points (marked by “X”) create connections into an array of AND gates. In my highlighted example, the upper AND gate outputs the logical result of  $(C \& \bar{B})$ . The lower AND gate has B as its input and output. The outputs from the AND gates then pass through a second array of programmable links that connect signals to an array of OR gates. In my highlighted example, the signals for B and  $(\bar{B} \& C)$  are connected to an OR gate, creating the function  $(B \text{ OR } (\bar{B} \& C))$  on OUT2.

<sup>1</sup> The bar above a variable notes negation, that is the inverse of its value.

12. As another example, the figure below is a textbook illustration of PLD circuits in a programmable ROM. The table on the left shows three desired logical functions based on inputs A and B.<sup>2</sup> The figure on the right implements those functions by fusing certain connection points to alter the connection pattern of the circuits in the PLD:

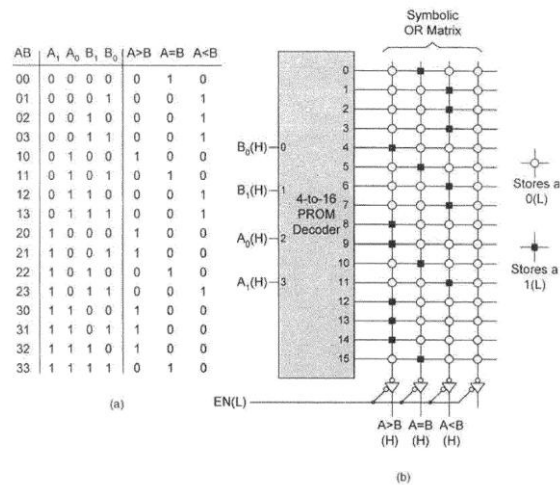


**FIGURE 7.4**  
PROM implementation of a noncascadable 2-bit comparator. (a) Canonical truth table. (b) Decoder and symbolic representation of fusible bit position patterns in the OR memory section.

AMD-CV-0008933 (Fig. 7.4, annotated).

13. The following is another textbook example, Table 7.6 shows the inputs and desired output functions:

**Table 7.6**  
PAL Programming Table

| Product Term | AND Inputs |   |   |   |   | Outputs                   |
|--------------|------------|---|---|---|---|---------------------------|
|              | A          | B | C | D | w |                           |
| 1            | 1          | 1 | 0 | — | — | $w = ABC' + A'B'CD'$      |
| 2            | 0          | 0 | 1 | 0 | — |                           |
| 3            | —          | — | — | — | — |                           |
| 4            | 1          | — | — | — | — | $x = A + BCD$             |
| 5            | —          | 1 | 1 | 1 | — |                           |
| 6            | —          | — | — | — | — | $y = A'B + CD + B'D'$     |
| 7            | 0          | 1 | — | — | — |                           |
| 8            | —          | — | 1 | 1 | — |                           |
| 9            | —          | 0 | — | 0 | — | $z = w + AC'D' + A'B'C'D$ |
| 10           | —          | — | — | — | 1 |                           |
| 11           | 1          | — | 0 | 0 | — |                           |
| 12           | 0          | 0 | 0 | 1 | — |                           |

<sup>2</sup> There are four inputs: the first two represent the two bits of a number A, while the second two represent the two bits of a number B.

Figure 7.17 shows how those output functions are implemented in a PLD by altering the connection pattern of circuits in the PLD. Here, the user blows fuses to break electrical connections, similar to a fuse box or circuit breakers in home electrical systems, and thereby isolate perpendicular wires from each other:

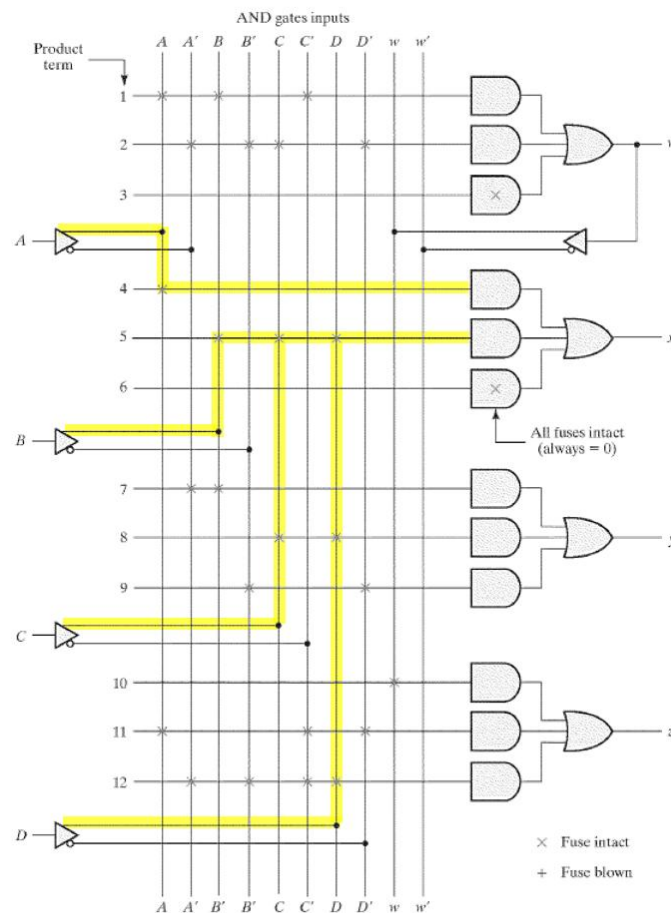


FIGURE 7.17  
Fuse map for PAL as specified in Table 7.6

AMD-CV-0008837 (Fig. 7.17, annotated). I highlighted the preceding figure to show the signal paths for inputs at A, B, C, and D on their way to the AND gates for output x, which calculates the equation  $x = A + BCD$ . Here, intact fuses (marked with “X”) create connection points in

circuits.<sup>3</sup> Input A passes to the first AND gate as-is. Signals B, C, and D are input to the second AND gate, which outputs their product (B & C & D), meaning it outputs 1 only when all three inputs are 1. The result of the two AND gates are then passed to an OR gate, creating output  $x = A + BCD$  because “+” indicates logical OR. In this way, users create custom logic functions in the PLD by altering the connection pattern of circuits in the PLD.

14. In each of the above examples, the programming of circuit connections was achieved by blowing fuses or other mechanisms that alter physical circuits in the PLD to perform custom logic functions. These examples featured one-time programmable PLDs where users could alter the circuits one time, but after that, the resulting circuits were hard-wired and could not be reverted or changed. One type of PLD, known as an FPGA, was often reprogrammable. In an FPGA, the user still created custom logic functions directly in hardware by altering the interconnection pattern of circuits, but those patterns could be reprogrammed multiple times. Like other PLDs, the distinguishing factor for FPGAs was the ability of the user to alter the circuits inside the FPGA.

### **C. Background of the '943 Patent**

15. The '943 patent aims to overcome the limitations of “[s]oftware-based systems” and fixed-function hardware. “Software-based systems” are not as fast as “dedicated electronic hardware,” but “redesigning” and manufacturing dedicated hardware for each application is expensive. '943 pat., 1:8-21. The '943 patent seeks to provide the speed of dedicated hardware while avoiding the need to design and manufacture a new hardware chip for each application. *Id.*

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<sup>3</sup> The fuses here are described as intact because in this device, all connections are intact at manufacture. Fuses are blown to break connections and separate wires. Some fuses (also called anti-fuses) work in the opposite way, where they are blown to create connections rather than break them. Regardless, fuses and antifuses in PLDs provide mechanisms for users to alter the connection pattern of the circuits in the PLD.

16. To accomplish these goals, the '943 patent uses a type of integrated circuit called a "programmable logic device (PLD)." '943 pat., 1:36-44. As stated in the file history, "PLD is a term of art referring to a specific type of integrated circuit that has user programmable electronic circuits." CV-AMD000308-310. Unlike a conventional IC with hardware circuits that are fixed at manufacturing, PLDs have programmable circuits that users can alter to create custom functions, as explained above. The '943 patent uses customizable circuits in PLDs to provide dedicated hardware functionality without having to manufacture custom ICs for each application—the patent features "sandboxes" where the user can define the programmable circuits inside the sandbox to perform custom functions in hardware. '943 pat., Abstract, 5:19-29, 1:36-44, 3:8-13, Claim 1.

**D. "programmable logic device" (Claims 1 and 10)**

17. I understand that Defendants have proposed that "programmable logic device" should be construed as "an integrated circuit where the user can alter the connection pattern of the circuits." I understand that Plaintiffs have proposed a construction of "[p]lain and ordinary meaning, that is 'a device with electronic circuitry capable of being configured or reconfigured.'"

18. Based on my review of the claims, specification, and file history of the '943 patent, it is my opinion that a POSITA would have understood that "programmable logic device" means an integrated circuit where the user can alter the connection pattern of the circuits. This is further confirmed by the extrinsic evidence cited by *both* parties.

19. A POSITA would have found Plaintiffs' construction to be incorrect because it broadens PLD to encompass devices where the software is programmable but the circuits are not. Plaintiffs' construction redefines PLD to encompass "a device with electronic circuitry" (which

would be any IC) where the device is “capable of being configured or reconfigured” to run different software. This would include any IC that can run software, such as conventional x86 processors in PCs going back to the 1980s. But Plaintiffs are contradicted by the claim language, file history, the patent specification, and extrinsic evidence.

20. **Claim Language.** The claims require a PLD to include “sandboxes” where the user can define the programmable circuits within the PLD. Independent claims 1 and 10 each recite a “programmable logic device,” having first and second regions. ’943 pat., Claims 1 & 10. The second region further comprises “one or more sandboxes with user-definable programmable electronic circuits of the PLD.” *Id.*

21. Therefore, the claims confirm Defendants’ position—that the PLD must include circuits that users can alter—while refuting Plaintiffs’ construction, which would expand “PLD” to include an IC with circuits that cannot be changed by the user. Plaintiffs’ construction would expand “PLD” to encompass devices where the user cannot define a single circuit inside the PLD, in direct contradiction to the claims.

22. **Specification.** The specification refers to “a PLD ... or other programmable device that can configure electronic circuitry.” ’943 pat., 4:30-47, 1:36-44, 3:8-13, 5:19-25. Therefore, the specification confirms that users can configure the electronic circuits inside the PLD.

23. The specification further explains how sandboxes inside an FPGA (a type of PLD) address the patent’s goal of providing the speed of dedicated hardware: “[t]he use of FPGAs 122, and especially with the introduction of sandboxes 132, support the ‘*hardware defined everything*’ concept[.]” ’943 pat., 13:14-17. As explained above, the ’943 patent aims to provide the speed of dedicated electronic hardware without having to redesign and manufacture a

new IC for each application. '943 pat., 1:8-21. Since users can alter circuits inside the PLD, PLDs allow users to define custom hardware circuits to perform any function or application—this is what the patent means by “hardware defined everything.” Therefore, the patent confirms that user-definable programmable circuits inside the sandboxes allow the user to define “hardware” functionality inside the PLD (*id.*), rather than simply software.

24. I further note that the specification discusses hardware modules and software modules. '943 pat., Fig. 2. The '943 patent claims user-definable hardware modules (PLDs), while the related '753 patent—which shares an identical specification—claims both “user-definable hardware modules” and “user-definable software modules.” '753 pat., Claim 1. The shared specification also states that “processors 136 are available for software modules 112.” '943 pat., 6:46-6:64. This shows that the patentee knew how to describe and claim software modules, but specifically claimed PLDs with user-definable programmable electronic circuits for the '943 patent.

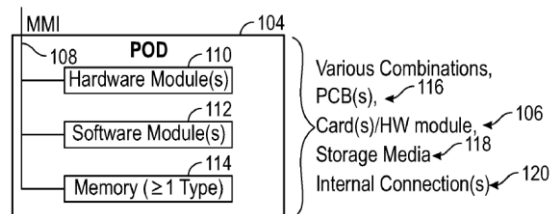


FIG. 2

25. The specification ends with generic paragraphs about computer-readable code and other boilerplate language that does not appear to be specific to the '943 patent. '943 pat., 16:11-17:37. One paragraph has boilerplate regarding “components [that] may be described or claimed as ‘configured to’ or ‘configurable to’ perform a task[.]” *Id.*, 16:57-17:22. This discussion does not mention PLDs and is not relevant here because the dispute is not about generic language for performing a task; it is about whether PLDs have circuits the user can configure.

26. The key requirement—reiterated in the claims, file history, and specification—is that a PLD must include circuits that the user can alter. Whether the PLD also runs software or not is irrelevant. For example, since the circuits of the PLD can be configured to perform any hardware function, those circuits can be configured into a processor. ’943 pat., 7:15-20 (suggesting possibility of a “softcore” processor). As the specification notes, “in some versions” a PLD can “includ[e] one or more processors or controllers.” ’943 pat., 4:27-39, 3:8-13 (PLD may “*optionally* includ[e] processors”) (emphasis added). Alternatively, PLDs can include fixed circuit processors in addition to programmable circuits. But regardless of whether software is executed or not, the defining feature of a PLD is the presence of circuits that the user can alter. If the user turns those circuits into a processor for running software, it does not change the fact that the PLD included circuits that the user altered into a processor.

27. **Prosecution History.** During prosecution, the Applicant acknowledged that “[p]rogrammable logic device, or PLD, *is a term of art* referring to a specific type of integrated circuit that has user programmable electronic circuits.” CV-AMD000308-310 (emphasis added). The ’943 patent was allowed after a single non-final office action rejecting the claims as obvious and anticipated by prior art of record. CV-AMD000317-324, CV-AMD000275-289. In the only office action, the Examiner rejected claims 1-4 and 6 as anticipated by the prior art reference Earl (CV-AMD000278-281) and claims 1, 3-4, and 7 as anticipated by the prior art reference Gerszberg (CV-AMD000281-282). The examiner rejected claim 2 as obvious over Gerszburg in view of another prior art reference Shur, and claim 7 as obvious over Earl in view of Gerszburg. CV-AMD000283-285.

28. To overcome the anticipation and obviousness rejections, claim 1 was amended to specify the electronic circuits of the one or more sandboxes comprised the programmable electronic circuits of the PLD:

1. (currently amended) A programmable device for data flow processing in a user-configurable server with swappable pods or cards, comprising:
  - a programmable logic device (PLD) having a first region and a second region; the first region comprising a hardware-based or firmware-based router with a port enabling communication between the router and the second region; and
  - the second region comprising one or more sandboxes with user-definable programmable electronic circuits of the PLD.

CV-AMD000303 (text formatting as in original).

29. In connection with this amendment, Applicant argued that the cited prior art “is silent regarding a programmable logic device.” CV-AMD000308-310. In particular, Applicant emphasized that “[p]rogrammable logic device, or PLD, is a *term of art* referring to a specific type of integrated circuit that has *user programmable electronic circuits*.” CV-AMD000308 (emphasis added).

30. The file history confirms two things. First, “PLD” is a term of art, not a generic term that could cover nearly any IC as Plaintiffs contend. Second, PLD refers to an IC with programmable circuits, as made clear in Defendants’ construction, rather than a fixed device whose circuits cannot be altered by the user, as encompassed by Plaintiffs’ construction, discussed below.

31. **Extrinsic Evidence.** Extrinsic evidence from both Defendants and Plaintiffs confirm that “programmable logic device” or “PLD” was a term of art referring to an IC where the user can alter the connection pattern of the circuits. Defendants’ construction is consistent with the conventional meaning of the term, and a POSITA with experience in the field would have recognized this term of art.

32. First, the prominent standards organization JEDEC reinforces Defendants’ construction by defining the term “programmable logic device (PLD)” as “[a]n integrated circuit consisting of an array of logic elements *whose interconnection pattern can be programmed* (either mask-programmed or user-programmed) *to perform specific logic functions.*” AMD-CV-0008781 (7th Ed. of JEDEC Dictionary of Terms for Solid-State Technology). JEDEC further explains that, in the context of PLDs, programming or configuring refers to “modify[ing] the logic connections inside a programmable device, causing its functions to change.” AMD-CV-0008781 (entry for “program; configure”). A POSITA would have known of JEDEC and recognized its role in the semiconductor industry. Operating since 1958, JEDEC is an industry association and a leading global standardization body in the microelectronics industry. JEDEC’s corporate members include practically all major semiconductor manufacturers, as well as household names in consumer electronics. JEDEC publishes a dictionary of technical terms as they are used in JEDEC standards and in the semiconductor industry, which is what I cited above. Therefore, a POSITA would naturally have looked to the JEDEC Dictionary for common terms of art, and the Dictionary confirms that a PLD was a term of art referring to an IC where the user can alter the connection pattern of the circuits.

33. Second, a POSITA would have recognized “PLD” as a term of art because this class of devices is taught as a basic concept in digital circuit design. At U.C. San Diego, I teach

such classes, including a design project class in which students learn how to use FPGAs to implement their design projects. At the undergraduate level, digital logic design courses typically cover PLDs for programming logic circuits. Multiple undergraduate textbooks confirm this. For example, Tinder’s Engineering Digital Design is a textbook intended for a “*first course of study*” on the “basics and background fundamentals” of digital circuit design. AMD-CV-0008888 (emphasis in original). Tinder provides a glossary with an entry for PLD:

**Programmable logic device (PLD):** any two-level, combinational array logic device from the families of ROMs, PLAs, PALs or FPGAs, etc,

AMD-CV-0008921 (bolding in original). Here, Tinder explains that PLDs have combinational array logic, referring to an array of logic circuits that can be configured to perform combinational (Boolean) logic, as was commonly known. *See* AMD-CV-0008830; *see also* AMD-CV-008904 (definition of “array logic”), AMD-CV-0008934, AMD-CV-0008940. Several examples of combinational array logic are explained below, from Tinder and other sources. Tinder elaborates on an example of an FPGA designed and produced by Actel:

To achieve the status of an FPGA, Actel enmeshes hundreds of these *modules in a matrix of programmable interconnections*. A segment of the ACT-1 interconnect architecture is illustrated in Fig. 7.25, courtesy of the Actel Corporation. Here, dedicated vertical tracking lines connect with each input to and output from a logic module. while other vertical tracking lines function as feedthrough between channels. Connections between horizontal and vertical tracking lines are made by “blowing” the cross fuses at intersections in accordance with the required fuse pattern program.

AMD-CV-0008953 (emphasis added). Tinder provides example illustrations of an FPGA-type PLD, which I have annotated to show exemplary circuit patterns after fuses are blown. *See also* AMD-CV-0008954 (Fig. 7.25):

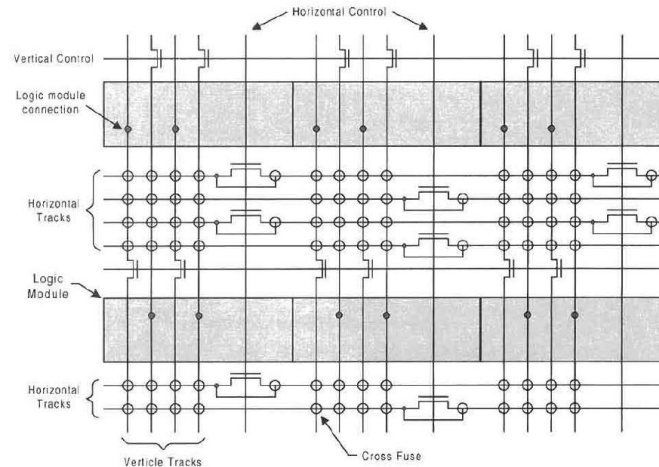


**FIGURE 7.25**  
Interconnect architecture for ACT-1 family of FPGAs. Source: *ACT Family Field Programmable Gate Array Databook*, Actel Corp., Sunnyvale, CA, 1991.

In a chapter explaining programmable logic devices, Tinder explains how the electronic circuits, rather than software, are programmed by the user with examples showing how the logic connections are changed in various types of PLDs. AMD-CV-0008930 (Fig. 7.2), AMD-CV-0008932-8933 (Figs. 7.3 & 7.4), AMD-CV-0008936-8937 (Fig. 7.6 & 7.7), AMD-CV-0008939 (Fig. 7.10), AMD-CV-0008941 (Fig. 7.11); *see generally id.*, AMD-CV-0008928-8962.

34. As another example, Mano's *Digital Design* is an undergraduate textbook (AMD-CV-0008801) that likewise discusses programmable logic devices that were known in the art, such as "FPGAs." AMD-CV-0008806, AMD-CV-0008830–8855. Mano describes an example of how the connection patterns of hardware circuits are programmed in certain exemplary types of PLDs:

A PLD is an integrated circuit with internal logic gates connected through electronic paths that behave similarly to fuses. In the original state of the device, all the fuses are intact. Programming the device involves blowing those fuses along the paths that must be removed in order to obtain the particular configuration of the desired logic function.

AMD-CV-0008808–8809.

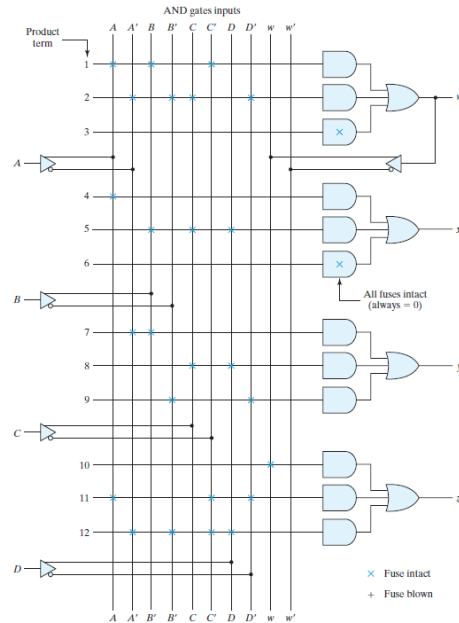


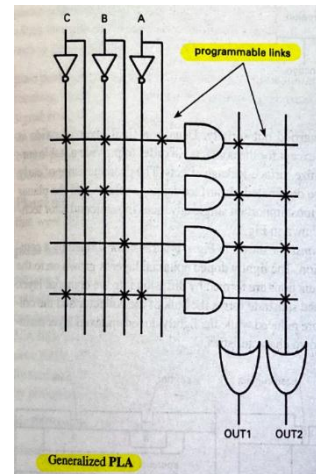
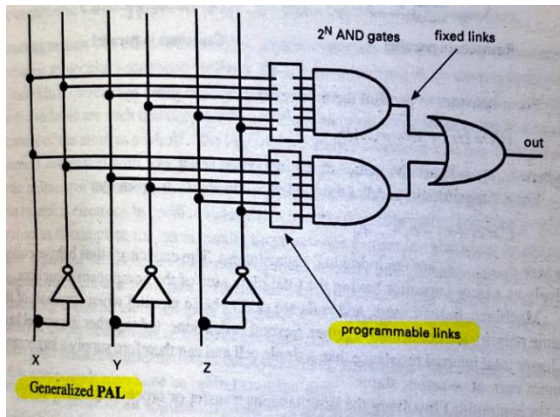
FIGURE 7.17  
Fuse map for PAL as specified in Table 7.6

AMD-CV-0008837 (Fig. 7.17). Circuits in PLDs could be configured in different ways, for example by blowing fuses (discussed above) or with electronic switches that connect or disconnect circuits. Mano discusses the latter example for “CMOS FPGAs[ that] are configured by downloading a stream of bits into the device to *configure transmission gates to establish the internal connectivity required by a specified logic function* (combinational or sequential).” AMD-CV-0008809 (emphasis added). This FPGA configuration process altered the connection pattern of the circuits inside the FPGA by using “programmable interconnect points” that connect a “grid of two layers of metal segments.” AMD-CV-0008845; *id.*, Fig. 7.23.

35. Third, evidence submitted by Plaintiffs supports *Defendants’* construction. Plaintiffs cite the Penguin Dictionary of Electronics, which confirms that PLDs require the user to program the logic circuits inside the device:

**PLD** *Abbrev. for* programmable logic device. A logic device where the designer must program the function required into the device. Such devices include >ROM, >PALs, >PLAs, and >FPGAs.

CV-AMD0017593. The Penguin Dictionary refers to PALs and PLAs as exemplary PLDs and includes diagrams showing how, in those PLDs, the user alters the connection pattern of the circuits using “programmable links.” CV-AMD0017591-92 (annotated):



36. Plaintiffs also cite the Electrical Engineering Dictionary published by CRC Press. But this definition confirms that PLDs were ICs where the user (also referred to as the “designer”) programmed circuits. CV-AMD0017676 (“**programmable logic device (PLD)** an integrated circuit able to implement ... digital functions defined by the designer and *programmed into this circuit.*”) (emphasis added). Similarly, Plaintiffs’ other cited evidence confirms that PLDs were programmed by configuring the connection patterns of their circuits. CV-AMD0017624 (EDACafe, *PROGRAMMABLE ASICS*) (“An IC foundry produces FPGAs with some connections missing. ... You then connect a computer to the chip and *program the chip to make the necessary connections.*.... the designer uses custom software ... to design and implement the programmable connections. The logic cells and *interconnection scheme*, in turn, determine the design of the input and output circuits as well as the programming scheme.”); CV-AMD0017561 (Adsantec, *All About ASIC*) (“PLDs ... are used when there is fast turn around and *programmable interconnect is required.* FPGAs ... have customized logic converters []

along with programmable interconnect.”); CV-AMD0017589 (Penguin Dict. of Elecs.) (“**FPGA** ... An array of logic cells placed in an infrastructure of interconnections....”). Thus, all of the extrinsic evidence confirms that “PLD” was a term of art that referred to a specific type of IC where the user can alter the connection pattern of the circuits.

37. **Plaintiffs’ Proposed Construction.** Plaintiffs’ construction is contrary to the claims, file history, and specification because it expands “PLD” from a term of art referring to a specific type of IC with user-programmable electronic circuits into a general term that encompasses ICs with fixed circuits that users cannot change.

38. Plaintiff’s proposed construction for PLD repurposes language from the specification but uses passive voice to break the connection between PLD and configurable circuits, even though that connection is explicit in the claims and specification of the ’943 patent. In Plaintiffs’ construction, a device can be a PLD, even if its circuits are fixed and cannot be changed by the user, so long as it has electronic circuitry (as all ICs do) and is “capable of being configured or reconfigured” to run software.<sup>4</sup>

39. However, the ’943 patent specification is clear: electronic *circuits* must be configurable in a PLD. ’943 pat., 4:30-47 (“a PLD ... or other programmable device that can *configure electronic circuitry*”). As I explained above, the claims and file history also require circuits to be configurable. This is consistent with the known meaning of PLD, which, as I explained above, refers to a family of ICs where the user can alter the connection pattern of the

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<sup>4</sup> This is reflected in Plaintiffs’ infringement contentions, which accuse a specialized network-processing ASIC with software running on P4 and ARM CPU cores as infringing claim 1 of the ’943 patent. See Plaintiffs’ Oct. 11, 2024 Preliminary Invalidity Contentions (Ex. D), 000002-15, 000027.

circuits. It is also the point of the '943 patent, which uses “sandboxes” inside the PLD where the user can alter the circuits inside the sandbox to perform custom functions ('943 pat., 5:19-29, Claim 1), thereby accomplishing the patent’s stated goal of providing the speed of dedicated hardware without having to design and manufacture a new IC. *Id.*, 1:8-21.

Furthermore, to the extent Plaintiffs argue that “PLD” encompasses ICs where the user cannot alter any of its circuits, this would make “PLD” indefinite because a POSITA would not be able to discern the boundaries of the term. Under Plaintiffs’ construction, a POSITA would not be able to determine what would constitute a PLD and what would not.

## **II. '753 Patent**

### **A. Level of Ordinary Skill in the Art and Relevant Time Period**

40. From my review of the specification and the claims, it is my opinion that the relevant field of art for the '753 patent is data processing and streaming architectures including user-defined hardware and software modules. The specification discusses the need to improve prior art systems “for many data flow and data processing applications.” '753 patent, 1:6-21. The specification further explains that it provides “a variety of flexible features for hardware-defined and software-defined functionality in data streaming and data processing systems, including video.” '753 patent, 2:47-3:20. The '753 patent summarizes its alleged invention as “[a] platform for data flow processing...having...user-definable hardware modules or user-definable software modules.” '753 patent, Abstract. The '753 patent is titled “Hardware defined anything in a platform with swappable pods, message interface, sandboxes and memory superposition” which I understand is a summary of the techniques reflected in the patent’s claims and specification to configure data flow processing architectures.

41. It is also my opinion that the level of ordinary skill in the field of art of the '753 patent would have been a person with a bachelor's degree in electrical engineering, computer engineering, or a similar major with at least two years of experience in the field (described above) or a person with a master's degree in electrical engineering, computer engineering, or a similar field with a specialization in the field (described above). A person with less education but more relevant practical experience may also meet this standard.

42. The '675 application that issued as the '753 patent was filed on July 15, 2018, claiming priority to itself. Accordingly, I have analyzed the claim terms in the '753 patent from the perspective of a POSITA as of July 15, 2018.

**B. “interleaved memory”**

43. I understand that Defendants have proposed a construction of “interleaved memory” as “an arrangement of different types of memory that are alternately accessed to achieve an average access bandwidth.” I understand that Plaintiffs have proposed a construction of “blended different types of memory.”

44. Based on my review of the claims and specification of the '753 patent, it is my opinion that a POSITA would have understood that “interleaved memory” means an arrangement of different types of memory that are alternately accessed to achieve an average access bandwidth. This follows the claims and specification of the '753 patent.

45. **Claim Language.** The '753 patent claims list “interleaved memory” as one of severable selectable arrangements of “the plurality of types of memory” in a “memory superposition.” '753 patent, Claims 4, 7, & 15.

4. The platform of claim 1, further comprising:

at least one of the one or more swappable pods or cards having a plurality of types of memory and *memory superposition with selectable arrangement of the plurality*

*of types of memory* as multilevel cache, *interleaved memory*, swapped memory over a specified address range, and memory allocated to specified address ranges according to parameterized task needs.

'753 patent, Claim 4 (emphasis added).

46. As explained below, Plaintiffs' construction removes "interleaved memory" as a distinct claim limitation by making it redundant of other claim limitations. Therefore, the claims support Defendants' construction.

47. **Specification.** Similarly, the specification starts off by stating that, "[f]or memory superposition...*two or more types of memory* are made available for a data flow or other data processing operation." '753 patent, 7:1-9 (emphasis added). In its only discussion of interleaved memory, the specification explains:

"[a]nother arrangement of memory superposition 140 is *interleaved memory*, to achieve an average access bandwidth. Input bandwidth, output bandwidth, or power could be blended among *different types of RAM or drives* such as rotational or disk drives versus solid-state drives, storage media modules, and different drive interfaces."

*Id.*, 8:35-40 (emphasis added). By alternating (interleaving) access between different types of memory, interleaved memory achieves an access bandwidth that is a blend (or average) of each type of memory. *Id.* For example, when DRAM and solid-state drives are used as interleaved memory, access to these memories would be alternated, and as a result, the average access bandwidth would be the average between the bandwidth of DRAM and the solid-state drive. *See id.* Therefore, the cited portions of the specification confirm that "interleaved memory" refers to an arrangement of different types of memory that are alternately accessed to achieve an average access bandwidth.

48. The specification explains how interleaved memory results in bandwidth and power characteristics being blended among the different types of memory. ’753 pat., 8:35-40. When access is interleaved between different types of memory, access bandwidth becomes a blend (or average) of the bandwidth for each type of memory. *Id.* Therefore, the bandwidth characteristic becomes blended. The specification uses “blend” to describe a blend of *characteristics* that results from interleaved memory, but it does not refer to a “blend” of different types of memory.

49. **Plaintiffs’ Proposed Construction.** Plaintiffs introduce the notion of “blended” types of memory, but as I just explained above, the ’753 patent describes blended memory *characteristics*—such as blended bandwidth—that result from interleaved memory, rather than a blend of memories themselves. Therefore, Plaintiffs’ construction misreads the specification.

50. Plaintiffs’ proposed construction is further incorrect because it reads the term “interleaved memory” out of the claims. By redefining “interleaved memory” to be a blend of different types of memory, Plaintiffs render that term superfluous, effectively removing “interleaved memory” as one of the selective arrangements required by the claim. The claims separately recite a “memory superposition” with “a plurality of types of memory” selectively arranged in various ways, including as interleaved memory. Therefore, the claims already require different types of memory to be used together in a memory superposition. Plaintiffs’ construction redefines “interleaved memory” to be duplicative of other claim language. Therefore, Plaintiffs’ construction is incorrect.

**C. “swapped memory over a specific address range”**

51. It is my understanding that Defendants proposed a construction of “swapped memory over a specific address range” as “memory with a specified address range where

information is moved between the memory and non-volatile storage.” It is my understanding that Plaintiffs proposed “plain and ordinary meaning.”

52. Based on my review of the claims and specification of the ’753 patent, and considering the known use of the term in the art, it is my opinion that a POSITA would have understood that “swapped memory” means memory with a specified address range where information is moved between the memory and non-volatile storage. As explained below, the claims and specification provide little guidance as to the meaning of “swapped memory.” Instead, the patent relies on a POSITA’s knowledge of this term. Defendants’ construction tracks the well-known meaning of this term of art.

53. **Claim Language.** The claims of the ’753 patent recite this term without further guidance as to its meaning, other than listing it as one of the claimed selectable arrangements of “memory superposition.” ’753 patent, Claims 4, 7, & 15.

54. **Specification.** The written description is likewise brief, simply stating that “swapped memory over a specified address range” is “another arrangement of memory superposition.” ’753 patent, 8:41-42; *see also id.*, 14:25-31. Because it is an arrangement of memory superposition, the term at least involves the use of “two or more types of memory” (’753 pat., 7:1-9), but the specification does not provide any additional detail.

55. **Extrinsic Evidence.** Swapped memory is a term of art that a POSITA would have recognized in the context of computer memory. The term “swapped memory” has been used for decades. For example, Microsoft Windows supported swap memory natively since Windows version 3.0, which was released in 1990. Windows 3.0 included the tool swapfile.exe which allowed a user to configure virtual memory settings, including the size and location of the swap file on a hard disk. The widespread adoption of Windows 95 made swapped memory a

common feature in households all around the world. Unix-based operating systems also widely supported swapped memory. For example, Linux has supported swapping virtual memory to a disk since version 0.12, which was released in 1992.

56. Several dictionaries confirm this well-known meaning for swapped memory. For example, the Microsoft Computing Dictionary explains that swapping “involves moving blocks of information in units known as pages between memory and disk as they are needed during the execution of the application.” AMD-CV-0008708. This technique was used in connection with a “swap file” on non-volatile storage. *Id.* (“swap file *n* (*comput*) an area of the hard disk of a computer into which any information not immediately required may be moved, thus maximizing the available memory.”). Similarly, the Chambers Dictionary explains that non-volatile storage is used for swapping memory, defining “an area of the hard disk of a computer into which any information not immediately required may be moved, thus maximizing the available memory” as the swap file. AMD-CV-0008704.

57. These definitions were consistent with the conventional use of the term “swapped memory” and its use in the ’753 patent, which explains that swapped memory involves the use of two or more types of memory. Given the ’753 patent’s absence of further explanation, a POSITA with experience in the field would have understood “swapped memory” based on its customary meaning in the art. Specifically, the claims recite “swapped memory over a specified address range,” and therefore, a POSITA would recognize this to refer to memory with a specified address range where information is moved between the memory and non-volatile storage, such as disk. This would be the plain and ordinary meaning of the term.

**D. “one or more swappable pods or cards” / “the plurality of swappable pods or cards” – Claims 1, 2, 3, 4**

58. It is my opinion that claim 1 is indefinite because its internal inconsistencies make it unclear whether the claim can be satisfied by *one* swappable pod or card.

59. Claim 1 recites “*one or more* swappable pods or cards.” Subsequently, claim 1 refers back to this term as “*the plurality* of swappable pods or cards.”<sup>5</sup> Some dependent claims (2 and 4-6) recite “one or more,” while claim 3 recites both “the one or more” and “the plurality” of swappable pods or cards.

60. Here, “*the plurality* of swappable pods or cards” refers back to the swappable pods or cards introduced earlier in claim 1. However, that earlier recitation stated *one or more* swappable pods or cards” rather than a plurality. The inconsistent use of plural and singular forms renders the claims indefinite because it is uncertain whether the claims can be satisfied by just *one* swappable pod or card.

61. The specification is similarly confusing, referring to “*one or more* swappable pods or cards,” but referring to the one or more of “*the plurality* of swappable pods or cards” in the discussion that immediately follows. ’753 pat., 1:25-35, Abstract. In sum, a POSITA would not have been able to understand whether the claims can be satisfied by one swappable pod or card, or not.

**III. Materials Considered**

62. I have been asked to consider the claim terms in the ’753 and ’943 patents discussed in this Declaration based on my review of the intrinsic record and on my background and experience as detailed in this Declaration and my curriculum vitae (Attachment A),

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<sup>5</sup> A “plurality” refers to two or more. Therefore, a plurality of swappable pods or cards refers to two or more swappable pods or cards.

including more than three decades of experience with data processing architectures, including high-speed packet processors and hardware accelerators.

63. As part of my analysis, I have reviewed the '753 and '943 patents and their respective file histories. A complete list of the materials I have considered for this declaration, organized for my opinions for each patent, is included as Attachment B to this declaration.

#### **IV. Background and Qualifications**

64. I was a person of at least ordinary skill in the art for the '943 and '753 patents by July 15, 2018. I received a B.S. in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in 1985. I received an M.S. in Electrical Engineering and Computer Sciences in 1988 and a Ph.D. in Electrical Engineering and Computer Sciences in 1991, both from the University of California, Berkeley.

65. I have specialized education and work experience in (1) PLDs and data processing systems, and (2) data processing and streaming architectures including user-defined hardware and software modules. For example, After my Ph.D., I joined Interuniversity Microelectronics Centre ("IMEC") in Belgium, a world-renowned international research and development organization, where I was the Head of the Systems Control and Communications Group. I worked on the development system design automation tools that were applied to advanced chip designs for data processing including digital communications and networking. I am currently a Full Professor of Electrical and Computer Engineering ("ECE") at the University of California, San Diego ("UCSD"), where I have been on the faculty since 1997. I am also the current Associate Dean for Strategic Programs at the Jacobs School of Engineering at UCSD, and I was previously the Chair of the ECE Department at UCSD. At UCSD, my teaching and research has focused on the design of computer systems, including techniques and methodology for hardware

programmability in data processing architectures, including high-performance switches and routers, high-speed packet processors, wireless networks, data networks, and various hardware accelerators for networking and communications applications. During my career, I have received or worked on research efforts that received millions of dollars in research funding from both government agencies and industry, including funding for research in packet processing, computer networks, network measurements, wireless communications, processor design, and hardware/software co-design.

66. In addition, I have authored numerous publications, including books, chapters in books, and journal papers, and I have presented numerous invited lectures and keynote presentations around the world. In total, I have authored or co-authored over 200 journal articles and conference papers. My publication record encompasses work relevant to the fields of the '943 and '753 patents. For example, I published a paper entitled "Hardware compilation for FPGA-based configurable computing machines," which presented a new programming environment for the development of applications on a new class of configurable computing machines based on FPGAs starting from a software-like algorithmic specification. I also published a paper entitled "Embedded architecture co-synthesis and system integration," which explored solutions to address the need for rapid prototyping of application-specific embedded system architectures integrating different combinations of programmable processors and hardware components. In another example, I published a paper entitled "Hardware/Software Communication and System Integration for Embedded Architectures" that was published in the journal Design Automation for Embedded Systems that address the design complexities of system architectures where different combinations of programmable processor components, library hardware components, and customized hardware components. A number of my

publications have received best paper awards or distinguished paper citations, including best paper awards in IEEE Transactions on VLSI Systems, and ACM/IEEE sponsored conferences related to semiconductor design automation such as DAC and ICCAD. I have also given numerous invited and keynote talks around the world.

67. I have also been awarded five patents and I have served as an Associate or Guest Editor for several prestigious journals published by the Association for Computer Machinery (“ACM”) and the Institute of Electrical and Electronics Engineers (“IEEE”), including serving as an Associate Editor for the ACM Transactions on Design Automation of Electronics Systems and on the Editorial Board of the International Journal of Embedded Systems. Further, I have served as General Chair of several ACM/IEEE conferences, and on the Organizing or Steering Committees of many ACM/IEEE conferences, including the ACM/IEEE Symposium on Architectures for Networking and Communication Systems (ANCS) and the ACM/IEEE Symposium on Networks-on-Chips (NOCS). I have served on the Technical Program Committees of over 45 ACM/IEEE conferences.

68. A detailed description of my professional qualifications is contained in my curriculum vitae, attached as Attachment A.

## **V. Legal Principles**

69. I am not a patent attorney and do not have any formal legal training. But I have been informed of the following principles related to claim construction:

70. I understand that in construing patent claims, the terms should be accorded the meaning they would have to a person of ordinary skill in the art at the time of the invention. In assessing how a person of ordinary skill in the art at the time of the alleged invention (a “POSITA”) would understand a claim term, one must consider the claim language, the patent’s

specification, and the patent's prosecution history, which are collectively called the "intrinsic evidence." The "prosecution history" of a patent is also called the "file history." Based on the intrinsic evidence (i.e., the claim language, specification, and file history of the patent), one should try to come to a conclusion about how a POSITA would understand the term in the context of the patent as of the effective filing date, i.e., priority date, of the patent application.

71. I understand that a POSITA reads the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. One must consider the specification to determine whether the inventor has employed any terms or words in a manner that is inconsistent with their plain and ordinary meaning.

72. I understand that in addition to the claims and the specification, one must review the patent's prosecution history, which is the complete record of all the proceedings before the Patent and Trademark Office, including any express representations made by the applicant regarding the scope of the claims. A patent applicant can limit claims during prosecution by, for example, altering claim language to overcome an examiner's rejection, clearly and unambiguously arguing to overcome or distinguish a reference, or clearly and unambiguously disavowing claim coverage.

73. I understand that in assessing how a POSITA would understand a claim term, it is permissible, and sometimes helpful, to consult other evidence that is not part of the "intrinsic evidence," such as expert and inventor testimony, dictionary definitions and technical treatises. This type of evidence is called "extrinsic evidence."

74. I understand that the plain and ordinary meaning of a claim term is the meaning that the term would have to a POSITA as of the effective filing date, i.e., priority date, of the patent application.

75. I understand that a patent applicant may serve as his or her own lexicographer. In doing so, the applicant may rebut the presumption that the plain and ordinary meaning applies to claim terms if the applicant explicitly provides his or her own unique definition separate and apart from the plain and ordinary meaning. If the applicant explicitly defines a claim term, the applicant's definition will be controlling for that term. When a patent applicant chooses to act as his or her own lexicographer, the use of that claim term in the larger context of the specification may further inform the meaning of the term.

76. I understand that a patent term may be considered indefinite. A term is to be considered indefinite if a POSITA reading the term, in light of the specification and prosecution history of the patent, is not informed about the scope of the invention with reasonable certainty. Absolute precision, however, is not required—some amount of uncertainty about the meaning of the term is acceptable. But a patent must be precise enough to afford clear notice of what is claimed, thereby apprising the public of what is still open to them.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Executed on April 19, 2025

A handwritten signature in black ink, appearing to be 'Bill Lin', written over a light blue horizontal line.

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BILL LIN

# **Attachment A: Curriculum Vitae of Bill Lin**

**BILL LIN**

Curriculum Vitae  
Tel: 858.531.2441  
Email: billmbox@gmail.com

**EDUCATION**

- **Ph.D.**, Electrical Engineering and Computer Sciences  
University of California, Berkeley, May 1991
- **Masters of Science**, Electrical Engineering and Computer Sciences  
University of California, Berkeley, May 1988
- **Bachelor of Science**, Electrical Engineering and Computer Sciences  
University of California, Berkeley, May 1985

**PROFESSIONAL EXPERIENCE**

1/1997 – present

**University of California, San Diego**  
Department Chair, Electrical and Computer Engineering  
Professor, Electrical and Computer Engineering

2/1992 – 12/1996

**IMEC, Leuven, Belgium**  
Group Head, Systems Control and Communications Group

**AREAS OF EXPERTISE**

- All aspects of computer networks and computer architecture problems, including the design of data networks, high-performance switches and routers, high-performance packet monitoring and measurements, wireless communications and mobile computing, multimedia and graphics systems, many-core processors, and systems-on-chip designs.

**PROFESSIONAL ACTIVITIES**

- Served or serving as Editor on 3 ACM or IEEE journals, as General Chair on 4 ACM or IEEE conferences, on the Organizing or Steering Committees for 6 ACM or IEEE conferences, and on the Technical Program Committees of 45 ACM or IEEE conferences.

**SELECTED PROFESSIONAL ACTIVITIES**

- General Chair, ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), 2010
- Chair of Steering Committee, ACM/IEEE Symposium on Architectures for Networking and Communications Systems (ANCS), 2012-present
- Guest Editor, IEEE Transactions on Network and Service Management (TNSM), 2012-2013
- General Co-Chair, ACM SIGMETRICS, 2015
- General Chair, ACM/IEEE International Symposium on Quality-of-Service (IWQoS), 2011
- Steering Committee, ACM/IEEE International Symposium on Quality-of-Service (IWQoS), 2011-2015
- Associate Editor, ACM Transactions on Design Automation and Electronics Systems (TODAES), 2010-2015
- Editorial Board, International Journal of Embedded Systems, 2003-present
- General Chair, ACM/IEEE Symposium on Networks-on-Chips (NOCS), 2009

- Steering Committee, ACM/IEEE Symposium on Networks-on-Chips (NOCS), 2009-present

## **PUBLICATIONS**

- Published over 200 journal articles and conference papers in top-tier venues and publications.

## **PATENTS**

- Mitigating Low-Rate Denial-of-Service Attacks in Packet-Switched Networks. United States Patent 8,443,444. Issued in May 14, 2013.
- Systems and Methods for Proactive Surge Protection. United States Patent 7,860,004. Issued in December 28, 2010.
- Method and Apparatus for Scan Block Caching. United States Patent 7,672,005. Issued in March 2, 2010.
- Design Environment and a Design Method for Hardware/Software Co-Design. United States Patent 5,870,588. Issued in February 9, 1999.
- System and Method for Generating a Hazard-Free Asynchronous Circuit. United States Patent 5,748,487. Issued in May 5, 1998.

**EXPERT WITNESS HISTORY (BILL LIN)**

I have served as an expert witness in 41 engagements (most engagements involved multiple patents in suit and multiple matters), of which I wrote expert reports or declarations in 34 engagements, analyzed source code in 16 engagements, was deposed 25 times, testified at trial 4 times, and scheduled to testified at 2 upcoming trials. The specific engagements and services provided are as follows:

1. Vizio, Inc. v. LG Electronics, Inc. and LG Electronics USA Inc., Civil Action No. 09-cv-1481-BEL
  - Expert witness on behalf of Vizio, Inc.
  - Law firm: Jones Day.
  - Services provided: Provided expert report, analyzed source code.
  - Technologies: Digital TV.
2. Vizio Inc. v. LG Electronics, Inc. and LG Electronics USA Inc., In the Matter of CERTAIN FLAT PANEL DIGITAL TELEVISIONS AND COMPONENTS THEREOF, U.S. International Trade Commission Inv. No. 337-TA-733
  - Expert witness on behalf of Vizio, Inc.
  - Law firm: Jones Day.
  - Services provided: Provided expert report, analyzed source code.
  - Technologies: Digital TV.
3. Vizio Inc. v. Coby Electronics Corp., Curtis International Ltd., E&S International Enterprises, Inc., MStar Semiconductor, Inc., ON Corp US, Inc., Renesas Electronics Corporation, Japan, Renesas Electronics America, Inc., Sceptre, Inc., and Westinghouse Digital, LLC, In the Matter of CERTAIN DIGITAL TELEVISIONS AND COMPONENTS THEREOF, U.S. International Trade Commission Inv. No. 337-TA-789
  - Expert witness on behalf of Vizio, Inc.
  - Law firm: Jones Day.
  - Services provided: Provided expert reports, was deposed, analyzed source code.
  - Technologies: Digital TV.
4. Linex Technologies Inc. v. Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless, In the Matter of CERTAIN WIRELESS COMMUNICATION DEVICES AND SYSTEMS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME, U.S. International Trade Commission Inv. No. 337-TA-775
  - Expert witness on behalf of Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless
  - Law firms: Covington & Burling, K&L Gates, Morrison & Foerster, Lewis Roca & Rothgerber.
  - Services provided: Provided expert reports, was deposed, analyzed source code.
  - Technologies: WiFi networks.
5. MOSAID Technologies, Inc. v. Dell, Inc., Qualcomm Atheros, Inc., et al., Case No. 2:11-cv-00179-TJW
  - Expert witness on behalf of Qualcomm Atheros, Inc.
  - Law Firm: McDermott Will & Emory.
  - Services provided: Provided expert analysis.
  - Technologies: WiFi networks.
6. Hitachi Consumer Electronics Co. Ltd., et al. v. Top Victory Electronics (Taiwan) Co. Ltd., et al., Civil Action No. 2:10-cv-260-JRG.
  - Expert witness on behalf of Vizio, Inc.
  - Law Firm: Akin Gump Strauss Hauer & Feld
  - Services provided: Provided expert reports, analyzed source code.
  - Technologies: Digital TV.

7. United States International Trade Commission (USITC) Investigation Number: 337-TA-853 and Technology Properties Limited, LLC v. Kyocera Corporation and Kyocera Communications, Inc. in the Northern District of California, Case No. 3:12-cv-03860-JSC
  - Expert witness on behalf of Kyocera Corporation and Kyocera Communications.
  - Law firm: Morrison & Foerster.
  - Services provided: Provided expert analysis.
  - Technologies: Cell phones, microprocessors.
8. Netgear, Inc. v. Ruckus Wireless, Inc., Case No. 1:10-cv-00999-SLR / D. Del.
  - Expert witness on behalf of Ruckus Wireless, Inc.
  - Law firms: Lewis Roca & Rothgerber, Orrick.
  - Services provided: Provided expert report, analyzed source code, was deposed, and testified at trial.
  - Technologies: WiFi networks.
9. Sonics, Inc. v. Arteris, Inc., Case No. 11 CV-05311 SBA, and Arteris S.A.S. v. Sonics, Inc., Case No. C 12-00434 (WHA)
  - Expert witness on behalf of Arteris, Inc. and Arteris S.A.S.
  - Law firm: DLA Piper.
  - Services provided: Retained as an expert.
  - Technologies: Systems-on-Chips (SoCs).
10. Linex Technologies Inc. v. Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless, U.S. District Court, Northern District of California, C 13-00159 CW
  - Expert witness on behalf of Hewlett-Packard Company, Apple Inc., Aruba Networks, Inc., Meru Networks, and Ruckus Wireless
  - Law firms: Covington & Burling, Milbank, K&L Gates, Morrison & Foerster, Lewis Roca & Rothgerber.
  - Services provided: Provided expert reports, analyzed source code.
  - Technologies: WiFi networks.
11. Frontier Communications Corp. v. Google, C.A. No. 10-545 (D. Del)
  - Expert witness on behalf of Frontier Communications Corp.
  - Law firm: Steese, Evans & Frankel
  - Services provided: Provided source code analysis.
  - Technologies: Voice over IP.
12. U.S. Ethernet Innovations LLC v. Acer, Inc. et al., Case No. 10-cv-3724 (N.D. Cal.)
  - Expert witness on behalf of Qualcomm Atheros, Inc., Sigma Designs, Inc., and AT&T Services, Inc.
  - Law firms: Reed Smith LLP, Pillsbury Winthrop Shaw Pittman LLP, and Vinson & Elkins LLP.
  - Services provided: Provided expert reports, was deposed, analyzed source code.
  - Technologies: Intelligent network interfaces, data center networks.
13. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Netgear, Inc. and Belkin International, Inc.
  - Law firm: Reed Smith LLP.
  - Services provided: Provided declaration for IPR petition.
  - Technologies: Wireless networks.
14. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Arista Networks.
  - Law firm: Fish & Richardson.
  - Services provided: Provided declarations for IPR petitions, deposed 3 times.

- Technologies: Network routers, data center networks.
15. Invalidity Expert Witness.
    - Expert witness on behalf of Intel Corp.
    - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
    - Services provided: Provided expert analysis.
    - Technologies: WiFi networks, bluetooth networks.
  16. Parthenon Unified Memory Architecture LLC v. HTC Corporation et al., Case No. 2:14-CV-690-JRG-RSP (E. D. Texas).
    - Expert witness on behalf of HTC Corporation and HTC America, Inc.
    - Law firm: Sidley Austin LLP.
    - Services provided: Retained as an expert.
    - Technologies: Memory architectures.
  17. System Architecture Information Technology dba SAI Technology, Inc. v. Qualcomm Inc.
    - Expert witness on behalf of Qualcomm Inc.
    - Law firm: McDermott Will & Emory.
    - Services provided: Retained as an expert, provided reports, analyzed source code, was deposed, and testified at trial.
    - Technologies: WiFi networks.
  18. Inter Partes Review of U.S. Patents.
    - Expert witness on behalf of Sandvine Corp.
    - Law firm: Erise IP.
    - Services provided: Provided declarations.
    - Technologies: Network monitoring and measurements.
  19. Inter Partes Review of U.S. Patents.
    - Expert witness on behalf of Intel Corp., Cavium Inc., and Dell Inc.
    - Law firms: Weil, Gotshal & Manges LLP, Duane Morris LLP, Alston & Bird LLP.
    - Services provided: Provided declarations for IPR petitions, deposed 3 times.
    - Technologies: Intelligent network interfaces, data center networks, memory management.
  20. Expert Witness.
    - Law firm: Covington & Burling.
    - Services provided: Retained as an expert.
    - Technologies: WiFi networks.
  21. Qualcomm Inc. v. Apple Inc., Inv. No. 337-TA-1065 (ITC)
    - Expert witness on behalf of Apple Inc. and Intel Corp.
    - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
    - Services provided: Provided expert reports/declarations, analyzed source code, was deposed.
    - Technologies: Mobile systems, application and modem processors, inter-processor communications, embedded software, processor and bus power management, memory management.
  22. Qualcomm Inc. v. Apple Inc., Civ. Action No. 3:17-cv-01375-JAH-MDD (S.D. Cal.)
    - Expert witness on behalf of Apple Inc. and Intel Corp.
    - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
    - Services provided: Provided expert reports/declarations, analyzed source code, deposed 2 times, and testified at trial.
    - Technologies: Mobile systems, application and modem processors, inter-processor communications, embedded software, processor and bus power management, memory management.

23. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Panasonic Avionics Corp.
  - Law firm: Haynes and Boone LLP.
  - Services provided: Provided declarations for IPR petitions.
  - Technologies: Network security.
24. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Intel Corp.
  - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
  - Services provided: Provided declarations for IPR petitions, deposed 4 times.
  - Technologies: Mobile systems, application and modem processors, inter-processor communications, embedded software, power management, memory management.
25. Expert Witness.
  - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
  - Services provided: Retained as an expert.
  - Technologies: Inter-processor communications and security.
26. Bell Northern Research LLC v. Coolpad Technologies, Inc. et al., Civil Action No. 3:18-cv-01783-CAB-BLM (S.D. Cal.)
  - Expert witness on behalf of Coolpad Technologies, Inc. and Yulong Computer Communications
  - Law firm: Perkins Coie LLP.
  - Services provided: Provided expert reports, analyzed source code, deposed.
  - Technologies: Processors, wireless communications, power management.
27. Inter Partes Review and Ex Partes Review of U.S. Patents.
  - Expert witness on behalf of Google LLC.
  - Law firm: Paul Hastings LLP.
  - Services provided: Provided declarations for IPR and Ex Partes Review petitions.
  - Technologies: Computer networks, wireless communications.
28. In the Matter of CERTAIN ROUTERS, ACCESS POINTS, CONTROLLERS, NETWORK MANAGEMENT DEVICES, OTHER NETWORKING PRODUCTS, AND HARDWARE AND SOFTWARE COMPONENTS THEREOF, U.S. International Trade Commission Inv. No. 337-TA-1227.
  - Expert witness on behalf of Hewlett Packard Enterprise, Netgear, and CommScope
  - Law firm: Morgan, Lewis & Bockius LLP.
  - Services provided: Provided expert reports, analyzed source code, deposed, and testified at trial.
  - Technologies: WiFi networks.
29. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Intel Corp.
  - Law firm: Desmarais LLP.
  - Services provided: Provided declarations for IPR petitions.
  - Technologies: Computer systems.
30. PACT XPP Schweiz AG v. Intel Corp. 1:19-cv-1006-RGA (D. Del.).
  - Expert witness on behalf of Intel Corporation
  - Law firm: Kirkland & Ellis.
  - Services provided: Provided expert report, deposed.
  - Technologies: Multiprocessors, reconfigurable processors, power management.

31. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Intel Corp.
  - Law firm: Wilmer Cutler Pickering Hale and Dorr LLP.
  - Services provided: Provided declarations for IPR petitions, deposed 1 time.
  - Technologies: Mobile systems, application and modem processors, embedded software, memory management.
32. Ex Partes Review of U.S. Patents.
  - Expert witness on behalf of Rapid7, Inc., and CrowdStrike Holdings
  - Law firm: Erise IP.
  - Services provided: Provided declarations for Ex Partes Review petitions.
  - Technologies: Computer networks and network security.
33. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Google LLC.
  - Law firm: Paul Hastings LLP.
  - Services provided: Provided declarations for IPR petitions, deposed 1 time.
  - Technologies: Telephony and teleconferencing.
34. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Google LLC.
  - Law firm: Paul Hastings LLP.
  - Services provided: Provided declarations for IPR petitions.
  - Technologies: Computer networks, wireless communications.
35. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of AMD.
  - Law firm: Sheppard Mullin.
  - Services provided: Provided declarations for IPR petitions.
  - Technologies: Electronic design automation and reconfigurable computing.
36. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Oracle.
  - Law firm: Sheppard Mullin.
  - Services provided: Provided declarations for IPR petitions.
  - Technologies: Networking, mobile systems, computer systems.
37. Expert Witness.
  - Expert witness on behalf of Synopsys Inc., Socionext America, and NXP USA/B.V./Semiconductors
  - Law firm: Willkie Farr & Gallagher.
  - Services provided: Retained as expert.
  - Technologies: Electronics Design Automation, IC design.
38. Inter Partes Review of U.S. Patents.
  - Expert witness on behalf of Cadence Design Systems.
  - Law firm: Sheppard Mullin.
  - Services provided: Provided declarations for IPR petitions.
  - Technologies: Electronics Design Automation, IC design.
39. Correct Transmission, LLC v. Nokia Corp. 2:22-cv-00343 (Eastern District of Texas)
  - Expert witness on behalf of Nokia.
  - Law firm: Alston & Bird.

- Services provided: Provided expert report, analyzed source code, deposed, scheduled for trial.
- Technologies: Networking, computer systems.

40. Lionra Technologies Ltd. v. Palo Alto Networks, Inc. 2:22-cv-00214 (Eastern District of Texas)

- Expert witness on behalf of Palo Alto Networks.
- Law firm: Erise IP.
- Services provided: Provided expert report, deposed, scheduled for trial.
- Technologies: Networking, computer systems.

41. Expert Witness.

- Expert witness on behalf of Alphabet Inc. and Google.
- Law firm: Latham and Watkins.
- Services provided: Retained as expert.
- Technologies: Networking, multimedia transmission.

# **Attachment B**

### Materials Considered

|                                                                                                                   |
|-------------------------------------------------------------------------------------------------------------------|
| <b>Materials considered for the '753 patent</b>                                                                   |
| U.S. Patent No. 10,873,753 (“’753 patent”)                                                                        |
| Prosecution History of the ’753 patent                                                                            |
| Microsoft, Microsoft Computer Dictionary (5th Ed., 2002)                                                          |
| Chambers Dictionary (13th Ed., 2014)                                                                              |
| Exhibit C to Plaintiffs’ Oct. 11, 2024 Preliminary Infringement Contentions (excerpts)                            |
| Plaintiffs’ Jan. 23, 2025 Proposed Preliminary Claim Constructions                                                |
| <b>Materials considered for the ’943 patent</b>                                                                   |
| U.S. Patent No. 10,985,943 (“’943 patent”)                                                                        |
| Prosecution History of the ’943 patent                                                                            |
| Penguin, Dictionary of Electronics (excerpts)                                                                     |
| Tinder, <i>Engineering Digital Design</i> (“Tinder”)                                                              |
| U.S. Patent No. 10,873,753 (“’753 patent”)                                                                        |
| JEDEC, <i>JEDEC Dictionary of Terms for Solid-State Technology</i> , 7th Ed. (“JESD88F”)                          |
| Mano, <i>Digital Design</i> (“Mano”)                                                                              |
| CRC Press, Electrical Engineering Dictionary (excerpts)                                                           |
| EDACAFE “Programmable ASICs” [webpage]                                                                            |
| Adantec “All About Application-Specific Integrated Circuits (ASIC)” [webpage]                                     |
| Exhibit D to Concurrent Ventures’ and XstreamEdge’s Oct. 11, 2024 Preliminary Infringement Contentions (excerpts) |
| U.S. Patent App. No. 2011/0107398A1 to Earl                                                                       |
| U.S. Patent No. 6,307,839 to Gerszberg                                                                            |
| U.S. Patent No. 5,809,233 to Shur                                                                                 |
| Plaintiffs’ Jan. 23, 2025 Proposed Preliminary Claim Constructions                                                |