

Exhibit A

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION**

CONCURRENT VENTURES, LLC and
XTREAMEDGE, INC.,

Plaintiffs,

v.

ADVANCED MICRO DEVICES, INC. and
PENSANDO SYSTEMS, INC.

Defendants.

**CIVIL ACTION NO. 1:24-cv-335-
ADA**

JURY TRIAL DEMANDED

DECLARATION OF DR. PAUL MIN

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I. INTRODUCTION

1. I have been retained as an expert witness by Concurrent Ventures, LLC and XtreamEdge, Inc. (collectively, “CV”) and have been asked to provide my expert opinions regarding U.S. Patent Nos. 8,924,596 (the “’596 Patent”); 9,529,767 (the “’767 Patent”), 10,873,753 (the “’753 Patent”), 10,985,943 (the “’943 Patent”), and 10,944,634 (the “’634 Patent”). Specifically, I have been asked to determine how a person of ordinary skill in the art would understand certain terms in the claims of these patents.

2. I am being compensated for my time spent on this matter at my standard rate. My compensation is in no way based on the outcome of my analysis, my opinions, or this case, or on the substance of this declaration. I have no personal or financial stake in the outcome of this matter.

II. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

3. I summarize in this section my educational background, career history, publications, and other relevant qualifications.

4. My complete qualifications and professional experiences are described in my curriculum vitae, provided as Appendix A, describing my education and work experience. Appendix A also includes a list of my publications

5. I received a B.S. degree in Electrical Engineering in 1982, an M.S. degree in Electrical Engineering in 1984, and a Ph.D. degree in Electrical Engineering in 1987 from the University of Michigan in Ann Arbor. I received several academic honors, including my B.S. degree with honors, a best graduate student award and a best teaching assistant award during my M.S. study, and a best paper award from a major international conference for reporting results from my Ph.D. thesis.

6. After receiving my Ph.D., I worked at Bellcore in New Jersey from August 1987 until August 1990. At Bellcore, I was responsible for evolving the public switched telephone

network (PSTN) into a multi-services voice and data network that incorporated packet switches, optical technologies, and wireless technologies.

7. In September 1990, I joined the faculty at Washington University in St. Louis. In July 1996, I was promoted to an Associate Professor of Electrical Engineering with tenure. I am currently a Senior Professor of Electrical and Systems Engineering at Washington University. I have also served as the Chair of the Graduate Curriculum (2000-2002) and the Chair of the Undergraduate Curriculum (2011-2014) for the Department of Electrical and Systems Engineering.

8. At Washington University, I have conducted research in communications, computing, and related electronic hardware and software. My research group pioneered a new paradigm for designing electronic circuits that can alleviate the speed and performance mismatch against optical technology. I have received several grants from U.S. Federal Agencies, including the National Science Foundation and the Defense Advanced Research Project Agency, and numerous contracts from companies and organizations around the world.

9. Specifically related to the technology matters in this litigation, I have extensive experience in the design and development of various processors and task allocation amongst multiple processing cores in the processors. For example, I have developed network processors and security processors, each of which includes multiple processing cores and designed task allocation methods among the processors. I have also designed a number of chassis-based equipment that were used for switching, routing, security processing, servers, etc. In addition, since mid-1990s, I have designed and developed a number of semiconductor chips that incorporated the state of art technology. In my work with the design and development of semiconductor chips, I have interacted closely with the semiconductor foundries in terms of selection of chip packages.

This is because many of the integrated circuit chips I designed and developed were highly I/O (input/output) limited (as many communication chips are) and packing and I/O configuration were critical issues.

10. As a faculty member at Washington University, I have taught a number of courses in electronics, communication, and computing at both the undergraduate and graduate levels. For example, I have taught communication theory (Washington University ESE 471), transmission and multiplexing (Washington University ESE 571), and signaling and control of communication networks (Washington University ESE 572). In particular, Washington University ESE 572 covers various protocol processing architectures for the network packets, for which the Data Processing Units (DPUs) would be highly suited. In addition, Washington University ESE 571 covers a variety of packet processing schemes, again for which the Data Processing Units (DPUs) would be highly suited.

11. I have supervised numerous graduate students, many of whom received a doctoral degree under my guidance. A number of doctoral theses that I supervised relate specifically to wireless technology. My students and I have published a number of peer-reviewed articles on resource allocation, scheduling, modulation, mobility management, and multiplexing. Several of these articles received accolades in the field. For example, in 2011, we received a best paper award in 3G WCDMA and 4G LTE related mobility and resource management at the prestigious Mobility 2011 international conference. Many of the doctoral research I supervised included the study of high speed, high performance processing of network protocols, and various DPU types would be used to process them.

12. In addition to my responsibilities as a university faculty member, I have founded two companies. In May 1997, I founded MinMax Technologies, Inc., a fabless semiconductor

company that developed switch fabric integrated circuit chips for the Internet. In March 1999, I founded Erlang Technology, Inc., a fabless semiconductor company that focused on the design and development of integrated circuit chips and software for the Internet. One of Erlang's products received a best product of the year award in 2004 from a major trade journal for the electronics industry.

13. Outside my own start-up companies, I have also served in various technology and business advisor roles for other companies and organizations around the world. I was the main technical author for one of two winning proposals to the Korean government for CDMA wireless service licenses (1996). I was responsible for designing a commercial scale IS-95 CDMA cellular network, which I understand to be one of the earliest such networks deployed in the world. I worked with numerous engineers and scientists around the world to implement this commercial scale cellular network before IS-95 CDMA was widely accepted. This provided me with extensive insight into various components of cellular technology, which by and large are used in today's 3G and 4G networks. I have also been involved in a semiconductor company that specializes in semiconductor memories, such as flash EEPROMs, as a board member and as a technical advisor (2007- 2011).

14. I am a named inventor on eleven U.S. patents, many of which are related to switching, routing, protocol processing, resource allocation, framing, timing control, power control, packet processing, and network designing. I have extensively published technical papers in international journals and at international conferences as well as technical memoranda and reports, and I have given a number of seminars and invited talks around the world. I have organized several international conferences and served as an international journal editor.

15. I am a member of, and have been actively involved in, a number of professional organizations. For example, I have served as the Chair of the St. Louis Section of the IEEE, which has more than 3,000 members (2014), and a member of the Eta Kappa Nu Honor Society for electrical engineers. I have also been an Ambassador of the McDonnell International Scholars Academy (2007-2013).

16. In my over 30 years of experience with communications and electronic technology, I have acquired significant knowledge about telecommunications systems industry standards and standard setting organizations such as 3GPP, IEEE, and Bellcore. Through my professional experience, I have gained significant experience in use of different processor architecture and use of multiple processing cores working together.

III. LEVEL OF ORDINARY SKILL IN THE ART

17. Counsel for CV has informed me that a person of ordinary skill in the art is a hypothetical person who is presumed to have known the relevant art at the time of the invention. In my opinion, the relevant field of art for the patents-in-suit is that of computer architecture and high performance computing.

18. For the purpose of this Declaration, counsel for CV has instructed me to assume that, for the '596 and '767 Patents, the time of the invention is December 2013; and for the '753, '634, and '943 Patents, the time of the invention is July 2018. However, I understand that the conception dates of the inventions disclosed in each patent may have been earlier than those dates. Any earlier conception date does not alter my opinion regarding a person of ordinary skill in the art.

19. I have been informed by counsel for CV that the person of ordinary skill is generally familiar with the type of problems encountered in the field and the prior art solutions to those problems and possesses an ordinary level of creativity.

20. In my opinion, a person of ordinary skill in the art of the patents-in-suit would include someone who had a bachelors or graduate degree in computer science, electrical engineering, computer engineering, or a similar discipline together with knowledge of computer architecture, with approximately two years of experience in the field relating to high performance computing. The required levels of educational and industry experience are on a sliding scale relative to each other. For example, a person of ordinary skill could potentially have no educational degree but more industry experience or, conversely, could have something higher than an undergraduate degree with fewer years of industry experience.

IV. MATERIALS CONSIDERED

21. Materials that I have reviewed and considered include the '596, '767, '753, '943, and '634 Patents and their file histories, the parties' Preliminary Proposed Claim Constructions, Defendants' April 22, 2023 Opening Claim Construction Brief including the exhibits thereto and the declarations of Drs. Baker, Long, Lin, and Jeffay, and all other documents cited herein.

V. LEGAL STANDARDS

22. Counsel for CV has informed me of the legal principles that apply in this proceeding.

23. I understand that the words of a claim are generally given their ordinary and customary meaning, which I understand is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention. I understand that the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.

24. I understand that claim construction focuses on the "intrinsic evidence," which consists of the claims themselves, the specification, and the prosecution history. I understand that

the claims can provide helpful context for how the claim term is used. I understand that the specification is highly relevant to the claim construction analysis and usually dispositive concerning the meaning of a claim term. I further understand, however, that it is inappropriate to import limitations from preferred embodiments recited in the specification into the claim language.

25. I understand that “extrinsic evidence” may also be considered when determining the meaning of a claim. I understand that there are different sources of extrinsic evidence, including dictionaries, inventor testimony, expert testimony, and learned treatises. I understand that intrinsic evidence is generally favored over extrinsic evidence, and that extrinsic evidence may not be used to contradict the meaning of the claim term when read in light of the intrinsic evidence.

26. I understand that a patent claim may be expressed using functional language. I understand that under 35 U.S.C. § 112(f), a structure may be claimed as a “means ... for performing a specified function” and that an act may be claimed as a “step for performing a specified function.” I understand that not all functional language is subject to Section 112(f). I understand that there is a rebuttable presumption that § 112(f) applies when the claim language includes “means” or “step for” terms, and that it does not apply in the absence of those terms. I further understand that § 112(f) does not apply when the claim language, read in light of the specification, would be understood by a person of ordinary skill in the art to have sufficiently definite structure.

27. I understand that if a claim term does not contain the word “means,” there is a presumption that it is not governed by § 112(f). I understand that a claim term is only governed by § 112(f) if the term as a whole merely contains functional language without describing the structure to perform that function. I understand that if a person of ordinary skill in the art would

understand that a claim term refers to particular class of structures, that claim term would not be governed by § 112(f).

28. I understand that when it applies, § 112(f) limits the scope of the functional term “to only the structure, materials, or acts described in the specification as corresponding to the claimed function and equivalents thereof.” I understand the first step is a determination of the function of the means-plus-function limitation, and the next step is to determine the corresponding structure disclosed in the specification and equivalents thereof. I understand that a structure disclosed in the specification is corresponding structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim.

29. I understand that the words of a claim are generally given their ordinary and customary meaning as understood by a person of ordinary skill in the art when read in the context of the specification and prosecution history. I understand that an exception to this rule is where a patentee acts as a lexicographer to set out a definition of a claim term. I understand that to act as a lexicographer, a patentee must clearly set forth a definition of the disputed claim term other than its plain and ordinary meaning. I understand that to find lexicography, the patentee must clearly express an intent to redefine the term.

VI. OPINIONS PERTAINING TO THE '596 PATENT

A. “queue implemented in hardware”

30. Defendants propose the following construction: “queue implemented in physical circuits without software intervention” or alternatively, “indefinite under Plaintiffs’ infringement theories.” For the reasons set forth below, it is my opinion that Defendants’ proposed definition is improperly limiting and confusing and that no construction is necessary for this term. It is also my opinion that a person of ordinary skill in the art would understand the scope of “queue implemented in hardware.”

31. From the perspective of a person of ordinary skill in the art (“POSITA”), no construction is necessary for this term. The ’596 Patent relates to techniques for dividing and synchronizing a processing task across multiple pricing elements and processors in hardware. One element of the asserted claims refers to input queues implemented in hardware and output queues implemented in hardware. A POSITA would understand that the claim language surrounding the “input queue” and “output queue” terms requires software intervention. Specifically, claims 7 and 13 state that “computer storage storing instructions” issues commands to the input queue and receives a response corresponding to the command from the output queue. A POSITA would understand that “computer storage storing instructions” refers to software, which can be thought of as computer instructions. *See also* ’596 Patent at 7:59-67, 8:34-50. Thus, the claims require software (“computer storage storing instructions”) to “issue[] said command to said input queue on behalf of said first processing element” and “receives a response corresponding to said command from said output queue.” From this, a POSITA would understand that the claims themselves demonstrate that input and output queues implemented in hardware can be implemented with software intervention.

32. Moreover, many (if not most) queues use pointers to optimize the usable memory space, and the processing of queue pointers is a software process. Such a technique is well-known in the art. Many queues are implemented in hardware but still have software that processes memory allocation through pointer processing. Thus, a POSITA would be aware that the well-understood meaning of a “queue implemented in hardware” does not exclude interaction of software. As an additional reference, the ’943 Patent, which lists the same inventors as the ’596 Patent, states that the hardware implementation and the software implementation for a device can coexist in a single device.’943 Patent at 5:1-8 ([T]he MMI router 124 is hardware-based, that is it lacks a processor.

In other embodiments, the MMI router 124 is firmware-based, that is it has a dedicated processor with dedicated software that is not otherwise user programmable nor part of an operating system. In some embodiments, the MMI router 124 has both hardware-based and software based implementation.”). This further reinforces that in the eyes’ of the inventors, the fact that something is hardware-based does not preclude the use of software generally.

33. The claim language aligns with the specification which explains that software issues commands to the hardware modules. The specification explicitly states that “[t]he invention considers the case where software must issue commands to a hardware module.” ’596 Patent at 3:11-12. In several instances, the specification describes instances where software is used in the invention. ’596 Patent at 7:59-67 (referring to software that implements features and applications of the claimed invention); *id.*, at 8:34-50 (describing computer programs); *id.*, at 8:51-59 (explaining that the invention includes software, firmware, and hardware). Throughout the specification, several embodiments describe where the software intervenes in the hardware queues by issuing commands and receiving responses. ’596 Patent at 6:28-36 (“computer storage storing instructions, which when executed by one of the additional processing elements . . . issue the command to the input queue 408”), 7:23-32 (same). Taken together, in my opinion, a POSITA would not understand that a queue implemented in hardware must be implemented without software intervention.

34. I understand that Defendants also argue that the term “queue implemented in hardware” is indefinite based on CV’s infringement theories. As discussed above, queues implemented in hardware is a well-known concept (as opposed to queues defined by software only), and a POSITA would understand what that term means without difficulty. *See, e.g.*, Ex. D (CV-AMD0017565) (Microsoft Computer Dictionary) at 464 (defining “queue”); Ex. B (CV-

AMD0017608) (Modern Dictionary of Electronics) at 338 (defining “hardware” and “hardware buffer”), 609 (defining “queue”).

35. I reviewed the declaration of Dr. Baker and taken it into consideration in coming to my opinion. In my opinion, Dr. Baker does not consider the scenarios in which a queue is implemented in hardware but still has software intervention, and thus improperly limits the meaning of “queue implemented in hardware.” I have also reviewed the prosecution history of the ’596 Patent and taken it into consideration in coming to my opinion. Nothing within the prosecution history suggested that the plain and ordinary meaning “queue implemented in hardware” should be limited to excluding software intervention.

B. “register”

36. Defendants propose the following construction: “set of flip-flops that store a set of related bits.” For the reasons set forth below, it is my opinion that Defendants’ proposed definition is improperly limiting and confusing and that no construction is necessary for this term.

37. I understand that CV and Defendants both agree that the register must be implemented in hardware in the context of the claim language, “register implemented in hardware.” I dispute that a “register” should be defined as only including “flip-flops,” as Defendants assert. Fundamentally, a person of ordinary skill in the art would understand that a register is a storage area that can be addressed by name during the execution of software, and a “register implemented in hardware” is thus a “storage area implemented in hardware that can be addressed by name.” Defendants’ construction both misses the point (as it is reductive to define a “register” as simply a “set of flip-flops”) and incorrect (as a register can be implemented using other methods besides a “set of flip-flops that store a set of related bits”).

38. A required feature of a register is a known memory location that other aspects of the system, including software, can access while certain instructions are executed. It is well known

to a POSITA that a register is a type of computer memory built into a processor that stores data (i.e., values, storage addresses, etc.). This means that there are a variety of ways that the register can be implemented, such as usable Static Random Access Memory (SRAM), which provides rapid access to the processor while executing instructions. A POSITA would know that SRAM is generally not made of flip-flops. Rather, SRAM utilizes transistors connected to store information or data.

39. As noted above, a register stores a certain number of bits of data to be accessed by the processor executing instructions. While a set of flip flops can store these bits, the flip flops are not an efficient way to implement the registers. To start, typical flip-flops are two-input devices (“R” and “S” for RS flip-flops, “J” and “K” for JK flip-flops, D flip-flops implemented with “R” and “S” inputs tied together in RS flip-flops). I note that it is unnecessary to utilize two inputs for storing a single bit of information, as the flip-flops require. Moreover, a single flip-flop is made of multiple logic gates such as NAND/AND and NOR/OR gates, each of which is made of multiple transistors. These burdensome constraints associated with the flip-flops make the use of flip-flops as registers inefficient.

40. A book entitled, “Semiconductor Memories Technology, Testing, and Reliability” by Ashok K. Sharma, IEEE Press, 1997 (“Sharma”) (Exhibit I) describes various types of memories. At the time of the ’596 Patent invention, various types of semiconductor memories were well known to POSITAs (e.g., SRAM, Dynamic Random Access Memory, Electrically Erasable Programmable Read Only Memory (EEPROM), Flash memory).

41. In particular, Sharma states that SRAM “is classified as a volatile memory because it depends upon the application of continuous power to maintain the stored data” and that the SRAM “memory cells use active element feedback in the form of cross-coupled inverters to store a bit of information as a logic ‘one’ or a ‘zero’ state.” (Sharma, page 12.) POSITAs would have

known that SRAM, due to its “active element feedback,” extremely fast and reliable in reading from and writing to the memory cells.

42. The following are figures from Sharma that describe the basic architecture of the SRAM memory cell.

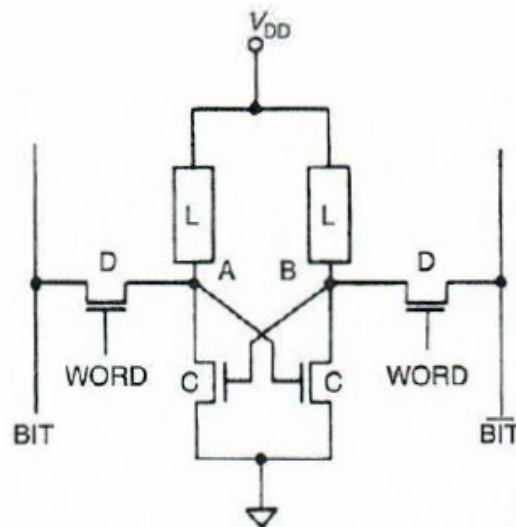


Figure 2-3. A general schematic of a SRAM memory cell.

Ex. I, Sharma, page 13.

43. Sharma states that “[t]he basic SRAM cell made up of cross-coupled inverters has several variations.” The following figure illustrates these “variations.”

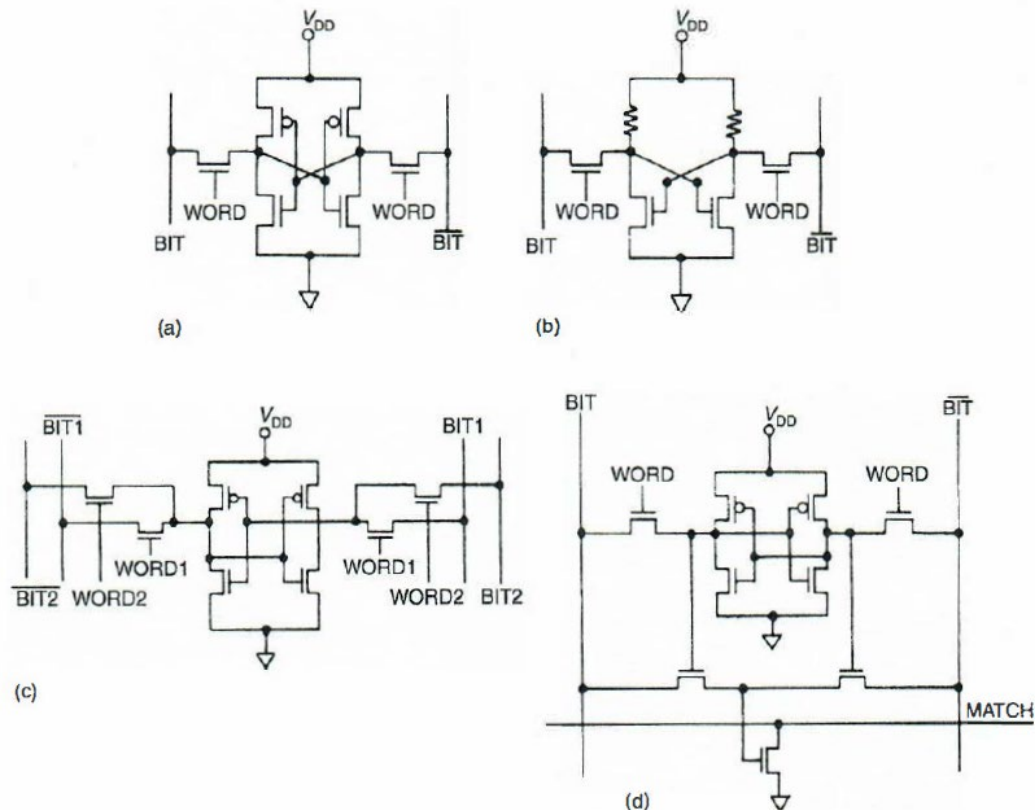


Figure 2-4. Various configurations of CMOS SRAM cells. (a) Six-transistor full CMOS. (b) Four transistors with R -load NMOS. (c) Dual-port with double-ended access. (d) Content-addressable memory (CAM).

Ex. I, Sharma, page 13.

44. As the figures above explain, SRAMs are not made of flip-flops, each requiring two inputs. An SRAM memory cell requires a single input, e.g., “D” in Figure 2-3 of Sharma. In addition, an SRAM memory cell is not made of multiple logical gates like the typical flip-flops — rather a minimum of two transistors, each performing an inverter function, and cross coupling one transistor output to the input of the other transistor.

45. Flip-flops, like memory, are a distinct circuit that can store one bit of data, like an SRAM memory cell. For example, one flip-flop can store one bit, and multiple flip-flops can store several bits. Registers can store several bits, and accordingly, can be made from several flip-flops. However, a register is not fundamentally defined as a collection of stored bits because, more

fundamentally, a “register” is a storage area that can be addressed by name in software through programming. Defendants’ construction requires the “register” to exist entire within the flip-flops, which fails to account for the additional functionality of registers, such as the additional logic to control data management, storing and manipulating data during program execution, addressing modes that support efficient memory access, and facilitating quick processing. For example, Patterson and Hennessy’s “Computer Architecture: A Quantitative Approach,” is one of the main computer architecture textbooks, and is considered a treatise in the area. Hennessy’s Computer Architecture consistently refers to registers by the register names (e.g., register-register, register-memory) and never defines registers as simply a set of flip flops. Ex. E, at 70-71. Hennessy’s Computer Architecture explains that registers are “faster than memory, easier for a compiler to use,” can “be used more effectively than other forms of internal storage,” and “can be used to hold variables.” Ex. E, at 70-71.

46. I have reviewed Dr. Baker’s declaration regarding this term, as well as the dictionaries and textbooks cited by Defendants and Dr. Baker, and they do not support Defendants’ argument that a register is comprised solely of flip-flops. For example, Ex. 4 (Dictionary of Electrical Engineering) AMD-CV-0008627 and Ex. 6 (Principles of Digital Design) (AMD-CV-0008677) state that a register contains flip-flops; Ex. 5 (Dictionary of Electrical Engineering) (AMD-CV-0008651) explains that the register includes flip-flops, as well as inputs and outputs; Ex. K (Digital Design Principles & Practices) AMD-CV-0008639 explains that a register contains flip-flops, “store[s] a collection of related bits,” and that “the only real constraint is that all of the bits are stored using the same clock signal;” Ex. 5 (Dictionary of Electrical Engineering) (AMD-CV-0008651) also states that a register contains a set of flip-flops; and Ex. 6 (Principles of Digital Design) AMD-CV-0008685 states that “a register . . . can be thought of as a bitwise extension of

a flip-flop” and that “a simple register has n inputs and n outputs in addition to the clock signal.” Two of their dictionaries state that registers include more than flip-flops, such as inputs, outputs, and the clock signal. Ex. L (The Art of Electronics) AMD-CV-0008602, Ex. 6 AMD-CV-0008685 (Principles of Digital Design). Defendants’ expert, Dr. Baker, states that registers are implemented using flip-flops. Baker Decl. ¶ 41 (“And hardware registers were well known in the art to be basic circuit components implemented using flip-flops”); *id.* ¶ 50 (“a register is a group of flip-flops that store a set of related bits, and they are taught to implement registers using a group of flip-flops.”). Dr. Baker thus acknowledges, at least implicitly, that a register can use flip-flops but is not confined to or defined by flip-flops.

47. I have also reviewed the prosecution history of the ’596 Patent and taken it into consideration in coming to my opinion. Nothing within the prosecution history suggested that the plain and ordinary meaning “register” should be limited to a “set of flip-flops that store a set of related bits.”

VII. OPINIONS PERTAINING TO THE ’767 PATENT

A. “abstraction protocol”

48. I understand that Defendants’ construction proposes that the term “abstraction protocol” does not provide a definitive structure, and thus is subject to 35 U.S.C. § 112(f). I also understand that Defendants propose that the function is “enabling communication of commands between master controllers and edge controllers for a storage media device.” I also understand that Defendants argue that the specification does not disclose any structure for the “abstraction protocol.” I disagree with all of Defendants’ assertions.

49. In my opinion, a person of ordinary skill in the art would understand that the “abstraction protocol” refers to a protocol by which details of underlying hardware and software are hidden to the programmer to accomplish a particular task in more generic manner. There are

many examples of abstraction protocols that are known in the art, such as the Transmission Control Protocol (“TCP”), which is one of the most widely used protocols for the Internet. TCP is an abstraction protocol as the commands and instructions associated with TCP do not concern the details of the underlying hardware and software. Another example is the protocol used by virtual machines (“VM”), which hides the underlying hardware and software across different machines/operating system implementations. This is exactly what the term used in the ’767 Patent is referring to—it hides details of the SATA/SAS devices from the host accessing the SATA/SAS devices. A POSITA would have easily understood exactly what “abstraction protocol” referred to.

50. As this term does not contain the word “means,” I understand that there is a presumption that it is not governed by § 112(f). I understand that this term is only governed by § 112(f) if the term as a whole merely contains functional language without describing the structure to perform that function. In my opinion, a person of ordinary skill in the art would understand that “abstraction protocol” is a widely known term that is used in the field of computer architecture and software programming. Abstraction protocols are thus known to and identifiable to POSITAs. “Abstraction protocol” is a well-known term among those skilled in the art and a POSITA would be able to discern with reasonable certainty the full scope of the term. *See, e.g.*, Ex. D (Microsoft Computer Dictionary) (CV-AMD0017595) at 11 (defining “abstraction” as “a means of shielding software from device dependencies or the complexities of underlying software. For instance, hardware abstraction enables programs to focus on a task, such as communications, instead of on individual differences between communications devices.”); Ex. B (Modern Dictionary of Electronics) (CV-AMD0017608) at 3 (defining “abstraction” as “[a] simplified description or specification of a system that emphasizes some of the system’s details or properties while suppressing others. A high level of abstraction or a highly abstract machine is one in which very

few machine details are apparent to a programmer, who sees only a broad set of machine concepts.”).

51. A POSITA’s understanding of the term “abstraction protocol” would be further reinforced by the specification, which lays out specific detail of what an “abstraction protocol” is. The claims require that the “abstraction protocol” be “a full-duplex protocol” and “support[] full command queuing for the at least one storage media device.” The specification also explains that the abstraction protocol is “performance-centric;” “supports common high-level read and write access to a pool of storage media devices;” “is link-agnostic;” and “may be carried via a multiplicity of direct attach or networked interfaces, including but not limited to PCIe, Ethernet (e.g., 1GbE, 10GbE, 40GbE, or 100GbE), Infiniband, ThunderBolt, Firewire, USB, and/or custom interfaces.” ’767 Patent at Abstract, 4:4-63.

52. An abstraction protocol refers to one singular term. Defendants try to parse the term into two discrete parts: abstraction and protocol. Then, Defendants argue about each term separately. A POSITA would not separately understand the term to abstraction protocol to refer to two separate techniques. Instead, they would understand that the full term has specific meaning. Both words together create the well-understood term “abstraction protocol.”

53. In particular, a protocol can be thought of as a sort of machine-readable language. Just as a language is a set of rules or conventions for how humans can communicate with each other, I agree with Dr. Long that a protocol is the same thing for computers: “a set of rules (or conventions) that define a procedure to follow when transmitting and receiving data between devices, including the format, ordering and timing of data.” Ex. 9, ¶11. An abstraction protocol then can be thought of as a sort of *lingua franca*—a language that is intelligible to a wide variety of devices even if they do not actually share an underlying language. See ’767 Patent at 4:4-7,

4:35-38 (“This abstraction protocol . . . supports common high-level read and write access to a pool of storage media devices, each of which may have a SATA or SAS [different storage protocols] interface.”). In the example given in the patent, devices can communicate with both SATA and SAS storage media, without needing to know whether the device is a SATA or a SAS device. *See* Ex. D (CV-AMD0017595) (Microsoft Computer Dictionary) at 11 (defining “abstraction” as “a means of shielding software from device dependencies or the complexities of underlying software. For instance, hardware abstraction enables programs to focus on a task, such as communications, instead of on individual differences between communications devices.”); Ex. B (CV-AMD0017608) (Modern Dictionary of Electronics) at 3 (defining “abstraction”).

54. Thus, a POSITA would well understand the term “abstraction protocol,” and that it generally refers to a protocol by which details of underlying hardware and software are hidden to the programmer to accomplish a particular task in more generic manner.

B. “storage media device interface”

55. Defendants propose the following construction: “a physical interface for transmitting and receiving commands and data between the edge controller and the storage media device.” For the reasons set forth below, it is my opinion that Defendants’ proposed definition is improperly limiting and confusing and that no construction is necessary for this term.

56. From the perspective of a person of ordinary skill, no construction is necessary for this term. The ’767 Patent relates to a packet-switched network that is supported by an abstraction protocol which handles complex tasks while hiding unnecessary details from the user. A POSITA would understand that storage media device interface is an interface that enables communication with the storage media device—as the name explains.

57. A POSITA would understand that “storage media device interface” does not have to be a hardware, or “physical” device. For example, a well-known term, application programming

interface (“API”), is not a physical interface. API is an interface that the software executing API exchanges messages with the API. *See, e.g.*, Ex. 10 at 3-4 (“The point at which a connection is made between two hardware devices, between a user and a program or operating system, or between two applications.”), (“Software interfaces are Application Programming Interfaces (APIs) and consist of the codes and messages used by programs to communicate behind the scenes.”); Ex. 14 at 2 (“In software, it is a standard format for exchanging data.”); Ex. 15 at 2 (“Software that logically interconnects two computers or a computer and another device and allows them to interoperate. Such software generally is characterized as performing a gateway function.”). There is no concept that hardware must exist between the software and the API or other software behind the API. One of ordinary skill in the art would know that interface, as recited in computer networking or distributed computing environments (such as that disclosed in the ’767 Patent) does not limit the interface to a physical interface.

58. A POSITA would also understand that the “storage media device interface” need not enable transmitting *and* receiving commands *and* data. In particular, by its plain terms, the “storage media device interface” need only enable some communication with the storage media device. Defendants’ additional limitations do not appear to come from any evidence.

59. Finally, a person of ordinary skill in the art would understand that the claims require the “storage media device interface” to enable communication between the edge controller and the storage media device. That is a possible embodiment, as is shown in, for example, Figures 4A and 4C of the specification, in which the “storage media device interface” is located inside of the edge controller. But equally as possible is that the “storage media device interface” enables communication between another element in the system and the storage media device. Defendants

have not pointed to any reason why the “storage media device interface” should be limited to communication between the edge controller and the storage media device

60. I have also reviewed the prosecution history of the ’767 Patent and taken it into consideration in coming to my opinion. Nothing within the prosecution history suggested that the plain and ordinary meaning “storage media device interface” should be limited as Defendants propose.

VIII. OPINIONS PERTAINING TO THE ’753 PATENT

A. “interleaved memory”

61. Defendants propose the following construction: “an arrangement of different types of memory that are alternately accessed to achieve an average access bandwidth.” For the reasons set forth below, it is my opinion that Defendants’ proposed definition is improperly limiting and confusing and that this term should be construed as “blended different types of memory.”

62. A person of ordinary skill in the art would understand that interleaved memory could be accessed both in parallel or staggered fashion. Conventional understanding and the specification do not require the “interleaved memory” to create a particular outcome. The interleaved memory could be accessed in parallel or alternately to improve overall memory bandwidth or reduce latency. For example, the “Electrical Engineering Dictionary” defines “interleaved memory as:

a memory system consisting of several memory modules (or banks) with an assignment of addresses that makes consecutive accesses fall into different modules. This increases the effective memory bandwidth, as several memory requests can be satisfied (concurrently by several modules) in the same time as it would take to satisfy one memory requests. For example, a simple arrangement (sequential interleaving), which favors sequential access, is to assign address k to memory bank $k \bmod N$, where N is the number of modules employed: the reference stride is 1, so consecutive requests are to different bands. There are other schemes for assigning addresses to banks, all of which schemes aim to (for non-unit strides) give the same performance as with a stride of 1. These include skewed addressing, which is similar to sequential

interleaving but with a fixed displacement (the skew) added to the chosen module number; dynamic skewed addressing, in which the skew is variable and determined at run-time; pseudo-random skewing, in which the module number is chosen on a pseudo-random basis; prime-number interleaving, in which the number of modules employed is prime relative to the degree of interleaving; and super-interleaving, in which the number of modules exceeds the degree of interleaving.

Ex. F (CV-AMD0017645) (Electrical Engineering Dictionary) at CV-AMD0017674 (definition of interleaved memory).

63. This definition establishes that Defendants’ construction is too narrow. Interleaved memory need not include “memory” that is “alternately accessed”—as sequential interleaving can also be used. And the definition notably does not define interleaved memory by its purpose as Defendants propose—“to achieve an average access bandwidth.”

64. Patterson and Hennessy’s “Computer Architecture: A Quantitative Approach,” further describes “interleaved memory” as one of the techniques used to improve memory performance. “[T]he purpose of interleaved memory is to try to take advantage of the potential memory bandwidth of *all* the DRAMs in the system.” Ex. E at 430-431. Interleaved memory, as explained in the Patterson and Hennessy treatise is simply using multiple memories blended together. Interleaved memory allows for simultaneous access, e.g., multiple memory modules or memory devices. There are many different ways to achieve network optimization, and the ’753 Patent includes “interleaved memory” which is used in a manner to achieve increased latency and bandwidth instead of a single type of memory. The method of achieving increased throughput and latency could be sequential concurrent access, and the ’753 Patent does not limit the form of access. When memory is interleaved, it results in using multiple types of memory so one is not overloaded, which provides an enhanced benefit to performance. But ultimately, a POSITA would understand that “interleaved memory” is defined by the method of blending different types of memory—not by any result of that process.

65. I have also reviewed the prosecution history of the '753 Patent and taken it into consideration in coming to my opinion. Nothing within the prosecution history suggested that the plain and ordinary meaning “interleaved memory” should be limited as Defendants propose.

B. “swapped memory over a specified address”

66. Defendants propose the following construction: “memory with a specified address range where information is moved between the memory and non-volatile storage.” For the reasons set forth below, it is my opinion that Defendants’ proposed definition is improperly limiting and confusing and that no construction is necessary for this term.

67. A person of ordinary skill in the art would understand that swapped memory simply refers to memory that has been moved (i.e., swapped) between locations. And a POSITA would understand “over a specified address range” refers to a specific defined range of memory addresses rather than the *entire* memory. A POSITA would further understand that such swapping can occur entirely within volatile memory, and does not have to occur between the memory and non-volatile storage. As a specific example, bank switching is a type of swapped memory (or memory swapping) which occurs within memory, and not between the memory and non-volatile storage. The following is from Defendants’ cited extrinsic evidence, and demonstrates that memory swapping is not limited to swapping between the memory and non-volatile storage.

bank switching *n.* A method of expanding a computer's available random access memory (RAM) by switching between banks of RAM chips that share a range of memory addresses, which is set aside before switching begins. Only one bank is directly accessible at a time; when a bank is not active, it retains whatever is stored in it. Before another bank can be used, the operating system, driver, or program must explicitly issue a command to the hardware to make the switch. Because switching between banks takes time, memory-intensive operations take longer with bank-switched memory than with main memory. Bank-switched memory typically takes the form of an expansion card that plugs into a slot on the motherboard.

Ex. G (Microsoft Computer Dictionary 5th Edition) at 51.

68. In my opinion, the meaning that Defendant propose for the term “swapped memory over a specified address” actually describes page swapping that takes place during execution of a program. Page swapping happens when the processor executing a program runs out of instructions in the SRAM or the DRAM, and then fetches more instructions from the non-volatile memory, such as disk drive, and swaps out of the instruction currently in the SRAM/DRAM. The ’753 Patent concerns storage in a “platform for data flow processing” generally, and a POSITA would understand it to be limited to that one specific example of swapped memory related to page swapping.

69. I have also reviewed the prosecution history of the ’753 Patent and taken it into consideration in coming to my opinion. Nothing within the prosecution history suggested that the plain and ordinary meaning “swapped memory over a specified address” should be limited as Defendants propose.

C. “one or more swappable pods or cards” / “the plurality of swappable pods or cards”

70. Defendants’ position is that the term is indefinite. For the reasons set forth below, it is my opinion that a POSITA would understand the terms and their scope.

71. A person of ordinary skill in the art would understand that “one or more swappable pods or cards” in claim 1 of the ’753 Patent is within “one or more chassis,” and has hardware or software modules. The claim then refers back to the “one or more swappable pods or cards,” and states that “the plurality of swappable pods or cards” have “a portion for user-definable hardware or software modules” and are “user-configurable.” From this, a POSITA would clearly understand that “the plurality” refers to the previous “one or more pods or cards” (or at least the more portion of this term) in the platform. The introduction of the word “plurality” would not create any confusion to a POSITA as to whether only “one” or “more pods or cards” is required, since the “plurality of pods or cards” explicitly refers back to the at least “more” part of this claim term. Moreover, this understanding is further reinforced by the claims’ reference to chassis, which can hold multiple pods or cards and, and can be paired together into multiple chassis in a platform for data flow processing. Again, a POSITA would understand that the reference to refer to “the plurality of swappable pods or cards” is a reference to the “one or more swappable pods or cards” in the chassis.

72. I have also reviewed the prosecution history of the ’753 Patent and taken it into consideration in coming to my opinion. Nothing within the prosecution history suggested that a POSITA would not be able to understand the plain and ordinary meaning of “one or more swappable pods or cards” or “the plurality of swappable pods or cards.”

IX. OPINIONS PERTAINING TO THE '943 PATENT

A. “programmable logic device”

73. Defendants propose the following construction: “an integrated circuit where the user can alter the connection pattern of the circuits.” For the reasons set forth below, it is my opinion that Defendants’ proposed definition is improperly limiting and confusing and that no construction is necessary for this term.

74. A person of ordinary skill in the art would understand that “programmable logic device” is a term of art. A person of ordinary skill in the art would understand that certain types of PLDs (e.g., FPGA) focus on configuring the connection pattern of the circuitry/functional blocks. But PLDs include more than just FPGAs, as the patent discloses. ’943 Patent at 4:30-35. A PLD can configure not only connection patterns of the circuitry or the functional blocks, but also the operational aspects within the circuitry or the functional blocks. In particular, an ASIC (which is another example of a PLD), can provide configurability of the circuitry in any variety of manner as the designer of the ASIC contemplates, including operational aspect of the circuitry themselves. *See, e.g.*, ’943 Patent at 4:30-35 (“The programmable device could be, for example, an FPGA...a PLD or an ASIC, or more than one of these, or some combination of these, or other programmable device that can configure electronic circuitry, in some versions including one or more processors or controllers.”). For example, ASIC implementing certain signal processing procedure (e.g., Fast Fourier Transform or FFT) can be programmed to perform differing number of inputs operating at different sample rates, through programming the state machines. This programmability is not associated with the connection patterns of circuitry or functional blocks – rather, it programs how the operation of this ASIC performs the required function.

75. A POSITA would also understand that the programmability of the PLDs can be achieved in many ways, including using software and firmware. For example, one of Defendants’

cited textbooks, Mano’s Digital Design, explains that “CMOS FPGAs” (which are a type of PLD) “are configured by downloading a stream of bits into the device to configure transmission gates to establish the internal connectivity required by a specified logic function (combinational or sequential).” Ex. 24 at 300. A POSITA would understand this to refer to an alternative method of programming the PLD, besides physically blowing fuses in the FPGA. This demonstrates that a POSITA would not understand that a PLD cannot be programmed using software and firmware.

76. I have also reviewed the prosecution history of the ’943 Patent and taken it into consideration in coming to my opinion. Nothing within the prosecution history suggested that the plain and ordinary meaning “programmable logic device” should be limited as Defendants propose.

X. OPINIONS PERTAINING TO THE ’634 PATENT

A. “network connected device”

77. Defendants’ position is that the term is indefinite. For the reasons set forth below, it is my opinion that a POSITA would understand the scope of the term.

78. A person of ordinary skill in the art would understand that a network connected device is, as the same says, a device that is connected to the network. Within a computing environment, network connected devices can be linked to a variety of other devices and perform various tasks throughout the network. For example, the specification states that “[t]he embodiments can also be practiced in distributed computing environments where tasks are performed by remote processing devices that are linked through a wire-based or wireless network,” ’634 Patent at 12:53-55, and the “[e]ndpoints and servers are described herein as network-connected (or connectable) devices that optimize network connections,” *Id.*, 2:50-52.

79. In particular, the specification explains that the “network connected device” (or “tuner server”) has a “higher level view of the network traffic and not only offloads the calculations

but can also incorporate knowledge of the higher level view of the network topology to enhance congestion control over/among the network(s).” ’634 Patent at 5:5-9. From this, a POSITA would understand that the tuner server can (through software or other forms of commands) control and take actions remotely at the endpoint devices and send parameters from the endpoint devices back to itself in order to process the parameters and data. Given that the purpose of the “network connected device” (or “tuner server”) is to exercise control and decision-making over the endpoints, it is not at all surprising or confusing that it must take actions at those endpoints to send data back to itself.

80. Further, the specification states that the tuning server can be co-located with an endpoint. ’634 Patent at 5:9-11 (“The tuning server 302 may then be locally co-located with various endpoints.”). In that embodiment, the “network connected device” (or “tuner server”) is located with the endpoint devices, which makes it even easier for it to control the endpoint devices to send data back to itself.

XI. CONCLUSION

81. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true and that such statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both.

Executed on May 14, 2025 in St. Louis, Missouri.



Dr. Paul Min

Appendix

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 St. Louis, MO 63130

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1987	The University of Michigan	Ph.D. in Electrical Engineering
1984	The University of Michigan	M.S. in Electrical Engineering
1982	The University of Michigan	B.S. in Electrical Engineering

Professional Experience

From: 1990
 To: Present
 Organization: Washington University, St. Louis

Summary:

2015 - Senior Professor - Department of Electrical Systems Engineering

2011 – 2014 Chair – Undergraduate Curriculum, Department of Electrical and Systems Engineering

2000 – 2002 Chair – Graduate Curriculum, Department of Electrical and Systems Engineering

2002 - 2014 Associate Professor - Department of Electrical and Systems Engineering

1997 - 2008 On leave from full-time duty at Washington University – as Presidents of MinMax Technologies and Erlang Technology.)

1996 - 2002 Associate Professor - Department of Electrical Engineering

1996 Promoted with Tenure

1990 - 1996 Assistant Professor - Department of Electrical Engineering

- Teaching Experience
- “Transmission System and Multiplexing,” Washington University, ESE 571
 - “Electrical Laboratory I,” Washington University, EE 250.
 - “Communication Theory,” Washington University, ESE 471.
 - “Reliability and Quality Control,” Washington University, ESE 405/505
 - “Signaling and Control of Communications Networks,” Washington University, ESE 572.
 - “Introduction to Electronic Circuits,” Washington University, ESE232
 - “Queueing Systems and Discrete Stochastic Processes,” Washington University, EE 536 / CS 567.
 - “Digital Computer,” Washington University, EE 260M / CS 260.
 - “Data Networks,” Washington University, EE 530.
 - “Electrical Circuit Analysis,” Washington University, ESE 230.
 - “Computer/Communications System Analysis I,” Washington University, EE 557/ CS 557.
 - “Computer/Communications System Analysis II,” Washington University, EE558 / CS 558.
 - “Digital Systems Laboratory,” Washington University, EE 455 / CS 455.

From: 1999
 To: 2008
 Organization: Erlang Technology, Inc., St. Louis, Missouri
 Title: Founder and President
 Summary: Up to 70 employees, \$40M in total capital raised from 5 VCs and 3 Corporations
 Received “Product of Year” Award from Analog Zone Magazine in 2004

From: 1997
 To: 1999
 Organization: MinMax Technologies, Inc., St. Louis, Missouri
 Title: Founder and President
 Summary: Fabless semiconductor company, designing high performance switching ASICs

From: September 1987
 To: August 1990
 Organization: Bellcore, New Jersey
 Title: Member of Technical Staff
 Summary: Member of New Network Architecture Development Group

From: 1983
 To: 1987

Organization: Department of Electrical Engineering, The University of Michigan
 Title: Graduate Instructor
 Summary: Instructor for senior level Electrical Engineering Laboratory Class. Received a Best “Best Graduate Instructor Award” from the Department of Electrical Engineering

Professional Affiliations, Achievements & Awards

- Technical Program Committee, COMCAS 2021, Tel Aviv, November 2021.
- Technical Program Committee, COMCAS 2019, Tel Aviv, November 2019.
- Technical Program Committee, COMCAS 2017, Tel Aviv, November 2017.
- Technical Program Committee, COMCAS 2015, Tel Aviv, October 2015.
- Past-Chair, Saint Louis Section of the Institute of Electrical and Electronics Engineers (IEEE), 2015.
- Member of Executive Committee, Saint Louis Section of the IEEE, 2010-2015.
- Chair, Saint Louis Section of the IEEE, 2014.
- Technical Program Committee, COMCAS 2013, Tel Aviv, October 2013.
- Vice Chair, Saint Louis Section of the IEEE, 2013
- Treasurer, Saint Louis Section of the IEEE, 2012.
- The Best Paper Award at MOBILITY 2011, October 2011, Barcelona, Spain.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2011.
- Award of Appreciation, Saint Louis Section of the Institute of Electrical and Electronics Engineers, 2011, for contribution to various activities of the Saint Louis Section the Institute of Electrical and Electronics Engineers.
- Secretary, Saint Louis Section of the IEEE, 2010.
- Counselor, Student Chapter of the Year, the Institute of Electrical and Electronics Engineers, 2010.
- Wall Street Journal Businessmen of Year, 2003.
- American Men and Women of Science, listed in 1997.
- Member, Eta Kappa Nu (Honor Society for Electrical Engineers), inducted in 1992
- Outstanding Achievement Award, Bellcore, 1990.
- 18th ISATA Award of Technical Excellence, the best paper award at ISATA 1988.
- Rockwell Fellow, Rockwell International, 1985, 1986.
- Outstanding Graduate Student Award, the University of Michigan, 1985.
- Outstanding Teaching Award, the University of Michigan, 1984, 1986.
- Member of Honor's College, the University of Michigan, 1979, 1980.

- Honor's Convocation, the University of Michigan, 1979.
- Outstanding Freshman Award, the University of Michigan, 1979.
- Woodhaven Rotary Club Scholarship, Woodhaven Rotary Club, 1978.
- Second Place Winner, the State of Michigan Mathematics Prize Competition, 1977.
- International Program Committee, *IASTED International Conference on Communications, Internet and Information Technology (CIIT 2005)*, Cambridge, Massachusetts from October 31-November 2, 2005.
- International Program Committee, *IASTED International Conference on Communications 2003*, Scottsdale, Arizona, 2003.
- International Program Committee, *Wireless and Optical Communications 2003*, Banff, Canada, 2003.
- International Program Committee, Session Chair, *Wireless and Optical Communications 2002*, Banff, Canada, 2002.
- Invited participant, *NSF Workshop on Enhancing International Cooperation in CS/CE Research and Education*, Portland, 1997.
- Session Chair, *the 1993 Conference on Information Sciences and Systems*, Baltimore, March 1997.
- Member, Board of Editors, *Journal of Network and Systems Management*, 1996-1998.
- Program Committee, *International Symposium on Integrated Network Management*, San Diego, 1997.
- Guest Editor, *Journal of Network and Systems Management, Special Issue on Routing in Broadband Networks*, December 1995 and June 1996.
- Invited participant, *ARPA Workshop on Survivability of Large Scale Systems*, Washington D.C., 1996.
- Special Event Organizer, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Organizing Committee, *International Symposium on Integrated Network Management*, Santa Barbara, 1995.
- Local Arrangements Chair, *IEEE Information Theory Workshop on Information Theory Multiple Access and Queueing*, St. Louis, 1995.
- Chair, *Communications Chapter, St. Louis Section of the IEEE*, 1995.
- Participant, *IEEE Information Theory Workshop on Information Theory, Multiple Access and Queueing*, St. Louis, 1995.
- Participant, *ARPA/AFOSR Non-Linear Optics and Communication Workshop*, Denver, 1994.
- Participant, *CNRI Giga Bit Network Workshop*, Washington D.C., 1993.
- Participant, *IFIP/IEEE International Workshop on Distributed Systems*, New Jersey, 1993.
- Program Committee, *International Conference on Computer Communications and Networks*, San Diego, 1992.
- Session Chair, *ISMM International Conference*, New Orleans, 1990.
- Senior Member, *IEEE*.

- Member, *IEEE Committee on Network Operations and Management*.
- Member, *IEEE Committee on Computer Communications*.
- Registered Specialist, *Hong Kong Research Grant Council*.
- Reviewer, *IEEE Transactions on Communications*.
- Reviewer, *IEEE Transactions on Networking*.
- Reviewer, *IEEE Journal on Selected Areas in Communications*.
- Reviewer, *Journal of Network and Systems Management*.
- Reviewer, *Telecommunication Systems*.
- Reviewer, *Computers and Electrical Engineering*.
- Reviewer, *ETRI Journal*.
- Reviewer, *IEEE Transactions on Automatic Control*.
- Reviewer, *IEEE Communications*.
- Book Reviewer, *Prentice Hall*.
- Book Reviewer, *Morgan Kaufmann Publishers, Inc.*
- Book Reviewer, *Irwin Publishing Co.*

University Activities:

- Undergraduate Studies Committee, School of Engineering and Applied Science (2012 – Present)
- Faculty Advisor for IEEE Student Chapter (2009 – Present)
- Ambassador for McDonnell International Scholar Academy (2007 – 2013)
- Web Development Committee (2006 – 2008)
- University Judicial Board (1998 - 2000)
- Resource Generation Committee (1994 - 1995)
- Top 20 Committee (1992 - 1995)
- Telecommunications Committee, Chair (1991 - 1997)
- Library Planning Committee (1991 - 1992)
- Computer Engineering Committee (1990 - 1996)
- Communications Curriculum Committee (1990 - 1992)
- Resources Committee (1990 - 1992)

Patents

<u>Patent No.</u>	<u>Date</u>	<u>Title</u>
10,623,323	04/14/20	Network Devices and a Method for Signature Pattern Detection
10,284,476	05/07/19	Hierarchical Pattern Matching Devices and Methods

7,110,411	09/19/06	Method of and Apparatus for WFQ Scheduling Using a Plurality of Scheduling Queues to Provide Fairness, High Scalability, and Low Computational Complexity
7,106,738	09/12/06	Method of and Apparatus for High Speed Packet Switching Using Train Packet Queuing and Providing High Scalability
6,859,455	02/22/05	Method of and Apparatus for Building and Using Multi-Dimensional Index Trees for Multi-Dimensional Data Objects
6,614,789	09/02/03	Method of and Apparatus for Matching Strings of Different Lengths
6,359,885	3/19/02	Multi-Channel Packet Switching Apparatus Having Traffic Flow Controlling and Checking Functions
6,128,292	10/03/00	Packet Switching Apparatus with Multi-Channel and Multi-Cast Switching Functions and Packet Switching System Using the Same
5,788,161	12/13/98	Network Designer for Communication Networks
5,526,352	06/11/95	Integrable Low Complexity Multi-Channel Switch
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- Hung, C.P., and Min, P.S., “Simple Web Application Framework.” Submitted for publication in the IEEE Transactions on Cloud Computing.
- Luo, Z., and Min, P.S., “Parallel Implementation of Energy-Based Target Localization Methods in Wireless Sensor Networks.” Proceeding of the 2014 IEEE SOUTHEASTCON.
- Yu, Q., Luo, Z., and Min, P.S., “Intrusion Detection in Wireless Sensor Networks for Destructive Intruder.” Proceeding of 2014 International Conference on Smart Computing (SMARTCOMP 2014).
- Luo, Z., and Min, P.S., “Survey of Target Localization Methods in Wireless Sensor Networks,” 19th IEEE International Conference on Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Deriving and Visualizing the Lower Bounds of Information Gain for Prefetch Systems,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Hung, C.P., and Min, P.S., “Access LUT without CAM - Improved Pearson Hashing for Collision Reduction,” 19th IEEE International Conference On Networks (ICON 2013), Singapore, December 11-13, 2013.
- Luo, Z and Min, P.S., “Target Localization in Wireless Sensor Networks for Industrial Control with Selected Sensors.” International Journal of Distributed Sensor Networks, Volume 2013 (2013), Article ID 304631.
- Hung, C.P., and Min, P.S. “Performance Evaluation of Distributed Mobile Application Virtualization Services,” International Journal on Advances in Internet Technology, Vol. 5, no. 3&4, 2012, pp. 65-83.

- Hung, C.P. and Min, P.S., “Performance evaluation of distributed application virtualization services using the UMTS mobility model,” *MOBILITY 2011 The First International Conference on Mobile Services, Resources, and Users*, 23-29 Oct. 2011.
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- Hung, C.P. and Min, P.S., “Application Virtualization Using UMTS Mobility Model,” *ICOMP'11*, September, 2011.
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Testimony Provided or Expected to Provide as Expert Witness

Matter: Patent Infringement for Cellular Communication
 Law Firm: Fish & Richardson, P.C.

Case Name: In the Matter of Certain Cellular Base Station Communication Equipment, Components Thereof, and Products Containing Same, ITC Investigation No. 337-TA-1388
Testifying Expert for Lenovo.
Completed in September 2024.
(Expert reports submitted, deposed, and testified in the hearing.)

Matter: Patent Infringement for Wireless Local Area Networks
Law Firm: Quinn Emanuel Urquhard & Sullivan LLP
Case Name: Certain Audio Players and Components thereof (II). U.S.I.T.C. Inv. No. 337-TA-1330.
Testifying Expert for Google Inc.
Completed in June 2023.
(Expert reports submitted, deposed, and testified in the hearing.)

Matter: Patent Infringement for Cellular Communication
Law Firm: Willkie Farr & Gallagher/Covington Burling/Fish & Richardson
Case Name: IPR against the validity of U.S. Patent No. 7,746,798
Testifying Expert for Lenovo.
Retained in August 2024.
(IPR declaration submitted.)

Matter: Patent Infringement for Wireless Communications
Law Firm: Alston & Bird
Case Name: Atlas Global Technologies LLC v. ASUSTek Computers Inc.USDC WD TX
Civil Action No. 6:21-cv-820
Testifying Expert for ASUSTek
Completed in November 2023
(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications
Law Firm: Perkins Coie
Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-cv-22706-SCOLA/GOODMAN (S.D. Fla.)
Testifying Expert for HMD
Completed in December 2023
(Expert report submitted. Deposed.)

Matter: Patent Infringement for Wireless Communications
Law Firm: LAW OFFICES S. J. CHRISTINE YANG
Case Name: Atlas Global Technologies LLC v. ZyXEL Communications Corp. et al., U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00355 Atlas Global Technologies LLC v. D-Link Corp. U.S.D.C., W.D.T.X., Waco Div., Case No. 6:22-cv-00520
Testifying Expert for ZyXel
Retained in March 2023.

(Expert report submitted.)

Matter: Patent Infringement for Wireless Communications
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Case Name: Bell Northern Research v. MeidaTek Inc.
Testifying Expert for MediaTek Inc.
Retained in August 2023.

Matter: Patent Infringement for Home Security System
Law Firm: Foley and Lardner LLP
Case Name: Alarm.com v. Vivint, Inc., AAA Arbitration Case. No. 01-22-0004-5525 and
U.S.D.C. Case No. 2:23-cv-00004-JRG-RSP (E.D. Tex.),
Testifying Expert for Vivint, Inc.
Completed in 2023.

Matter: Patent Infringement for Wireless Communications and Electronics
Law Firm: Perkins Coie
Case Name: Bell Northern Research, LLC v. HMD AMERICA, INC. et al., Case No.: 1:22-
cv-22706-SCOLA/GOODMAN (S.D. Fla.)
Testifying Expert for HMD
Completed in December 2023.

Matter: Patent Infringement for Network Switches
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC v. CouldFlare, Inc. U.S.D.C. WD Tx
Case No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.
Completed in January 2024.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Security
Law Firm: Fish and Richardson
Case Name: Finjan LLC v. Palo Alto Networks, Inc. – Case No. 4:14-cv-04908-PJH. USDC
ND CA, Oakland Division.
Testifying Expert for Finjan LLC.
Retained in September 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Management
Law Firm: Irell & Manella LLP
Case Name: SNMP Research, Inc. & SNMP Research International, Inc. v. Broadcom Inc.,
Brodcade Communications Systems LLC, & Extreme Networks, Inc. U.S.D.C.
E.D. Tennessee at Knoxville Case No. 3:20-CV-451
Testifying Expert for SNMP Research.
Retained in May 2022.

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for MediaTek
Retained in March 2023.

Matter: Patent Infringement for Network Switching
Law Firm: Baker Botts
Case Name: Corrigent Corp. v. Arista Networks, Inc., Case No. 1:22-cv-00497-UNA. USDC
Delaware
Testifying Expert for Arista
Retained in October 2022.

Matter: Patent Infringement for Mobile Devices
Law Firm: Fish and Richardson
Case Name: GComm v. Samsung, U.S.D.C. ED. TX. Case No.:2:22-cv-0078-JRG
Testifying Expert for Samsung
Completed in January 2024.

Matter: Patent Infringement for Wireless Networks
Law Firm: McKool Smith
Case Name: Certain Mobile Telephones, Tablet Computers with Cellular Connectivity, and
Smart Watches with Cellular Connectivity, Components Thereof, and Products
Containing Same. U.S.I.T.C. Inv. No. 337-TA-1299
Testifying Expert for Ericsson
Completed in July 2022.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Semiconductor Manufacturing
Law Firm: Kramer Levin
Case Name: Oasis Tooling, Inc. v. Siemens Indus. Software, Inc., 1:22-cv-151 (D. Del.), Oasis
Tooling, Inc. v. GlobalFoundries U.S. Inc., 1:22-cv-312 (D. Del.)
Testifying Expert for Oasis Tooling
Retained in June 2022.
(Expert reports submitted.)

Matter: Patent Infringement for Optical Networks
Law Firm: Duane Morris
Case Name: NextGen Innovations, LLC v. Infinera Corporation. U.S.D.C. ED. TX (Marshall)
Case No. 2:22-cv-00306-JRG-RSP / IPR
Testifying Expert for Infinera
Retained in April 2023.

Matter: Patent Infringement for Wireless Devices
Law Firm: King and Spalding LLP

Case Name: Intellectual Ventures, et. al. v. General Motors Company and General Company Motors, LLC, Case No. 6:21-CV-1088 pending in the Western District of Texas, Waco Division
Testifying Expert for General Motors
Completed in January 2023.
(Expert report submitted.)

Matter: Patent Infringement for Wireless Devices
Law Firm: Sterne Kessler
Case Name: Neo Wireless LLC v. Volkswagen Group of America, Inc. and Volkswagen Group of America Chattanooga Operations, LLC and related matters
Testifying Expert for Volkswagen
Completed in September 2023.
(Expert report submitted and deposited. IPR declarations submitted)

Matter: Patent Infringement for Wireless Networks
Law Firm: Covington & Burling LLP
Case Name: XR Communications, LLC v. D-Link Systems, Inc., No. 8:17-cv-00596 (Consolidated) (C.D. Cal.)
Testifying Expert for Hewlett Packard Enterprise
Completed
(Expert report submitted and deposited.)

Matter: Patent Infringement for USB Charging System
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Fundamental Innovation Systems International LLC v. TCT Mobile (US), TCT Mobile (US) Holdings, Inc., et al. U.S.D.C. Delaware No. 20-552-RGA-CJB
Testifying Expert for TCL
Completed in June 2022.
(Expert report submitted and deposited.)

Matter: Inter Parte Reexamination for Wireless Communications
Law Firm: Alston & Bird
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Nokia
Retained in May 2022.
(Expert report submitted.)

Matter: Patent Infringement for Network Management System
Law Firm: Morgan, Lewis & Bockius, LLP
Case Name: Certain Routers, Access Points, Controllers, Network Management Devices, Other Networking Products, and Hardware and Software Components Thereof, U.S.I.T.C. Inv. No. 337-TA-1227
Testifying Expert for Hewlett Packard, Netgear, and CommScope
Completed in August 2021.
(Expert report submitted, deposited, and testified during trial.)

Matter: Contract Dispute
Law Firm: Orrick, Herrington & Sutcliffe LLP
Case Name: Allied Telesis, Inc., et al vs. Micron Technology, Inc., Santa Clara County
Case No: 2015-1-CV-282977
Testifying Expert for Micron
Retained in 2021. Deposed in October 2021.
Completed in 2022

Matter: Patent Infringement for Security Systems
Law Firm: Forley and Lardner LLP
Case Name: Certain Residential Premises Security Monitoring and Automation Control
Panels, and Components Thereof (ITC Inv. No. 337-TA-1273) and ADT LLC et
al v. Vivint, Inc., Case No. 6:21-cv-00687 (W.D. Tex.)
Testifying Expert for Vivint, Inc.
Completed in April 2022.
(Expert report submitted, deposed, and testified during trial.)

Matter: Inter Parte Reexamination for Internet Communications
Law Firm: Perkins Coie
Case Name: Patent reexamination in front of the U.S.P.T.O.
Testifying Expert for Twitter
Retained in June 2020.
(Expert report submitted.)

Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd. v. Heathco LLC, U.S.D.C. Delaware No. 20-224-
LPS
Testifying Expert for Vaxcel
Retained in February 2021.
(Expert report submitted and deposed.)

Matter: Patent Infringement for Network Communication System
Law Firm: Charhon Callahan Robson & Garza, PLLC
Case Name: Sable Networks, Inc. and Sable IP, LLC, v. ClouFlare, Inc. U.S.D.C. WDTX,
Civil Action No. 6:21-cv-261
Testifying Expert for CloudFlare, Inc.,
Completed in January 2024.

Matter: Patent Infringement for Mobile Wireless Device
Law Firm: Pearl Cohen
Case Name: In the Matter Of Certain UMTS And LTE Cellular Communications Modules
And Products Containing The Same, U.S.I.T.C. Inv. No. 337-TA-1240
Testifying Expert for Telit Wireless Communication, Quectel, and Thales
Completed in March 2023.
(Expert reports submitted and deposed.)

Matter: Transactional Taxes for Internet Application
Law Firm: Ryan Rapp & Underwood, PLC
Case Name: ADP, LLC v. Arizona Department of Revenue (TX2018-000246),
Testifying Expert for ADP, LLC.
Completed in June 2020.
(Expert report submitted.)

Matter: Trade Secret Misappropriation in Digital Electronics
Law Firm: Goodwin Proctor LLP
Case Name: Guzik Technical Enterprises versus Keysight Technologies, Inc. Superior Court
of the State of California for the County of Santa Clara, Case No.: 19CV355879
Testifying Expert for Keysight Technologies, Inc.
Retained in August 2020.

Matter: Patent Infringement for Fiber Optic Devices
Law Firm: Cooley
Case Name: Certain High-Density Fiber Optic Equipment and Components Thereof,
U.S.I.T.C. Inv. No. 337-TA-1194
Testifying Expert for AFL Communications, Panduit, FS.Com, Wirewerk, and
Siemon
Completed in October 2020.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Optical Transport Networks
Law Firm: Venerble
Case Name: Huawei Technologies Co. Ltd v Verizon Communications, Inc., et. al., 2:20-cv-
0030
Testifying Expert for Verizon.
Retained in March 2020.
(IPR declarations submitted.)

Matter: Patent Infringement for Lighting System
Law Firm: Fisher Broyles
Case Name: Vaxcel International Co., Ltd., v. Jasco Products Company, LLC., (Case No.
USDC Western District of Oklahoma, 5:19-CV-00154-JD
Testifying Expert for Vaxcel.
Retained in August 2020.

Matter: Patent Infringement for Wireless Communication
Law Firm: McDermott Will & Emery
Case Name: Bell Northern Research LLC v. ZTE. (Case No. 3:18-cv-01786 - S.D. Cal)
Testifying Expert for ZTE.
Retained in July 2019.
(IPR declarations submitted.)

Matter: Patent Infringement for Wireless Communication
Law Firm: Jones Day
Case Name: Bell Northern Research LLC v. Kyocera Corp. (Case No. 3:18-cv-1785 - S.D. Cal)
Testifying Expert for Kyocera.
Completed in May 2019.
(Claim construction declaration submitted, and deposed.)

Matter: Patent Infringement for Electronic Payment Systems
Law Firm: Paul Hastings
Case Name: ID Tech Corp. v. Samsung Electronics Co., Ltd., et al. (Case No. No. 8:17-cv-1748-DOC-JDE (C.D. Cal))
Testifying Expert for Samsung.
Retained in January 2019.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Internet Switching
Law Firm: Maynard Cooper
Case Name: Parity Networks, LLC v. Juniper Networks, Inc., Case No. 6:17-CV-00495-RWS-KNM (U.S.D.C.E.D. Tx.)
Testifying Expert for Juniper.
Retained in April 2018.
(IPR declarations submitted.)

Matter: Patent Infringement for Internet Switching
Law Firm: Morgan Lewis
Case Name: Parity Networks, LLC v. Hewlett Packard Enterprise Company, Case No. 6:17-CV-00682 (U.S.D.C.E.D. Tx.)
Testifying Expert for Hewlett Packard Enterprise Company.
Retained in September 2018.
(IPR declarations submitted.)

Matter: Inter Parte Reexamination for Covered Business Method
Law Firm: Reed Smith LLP
Case Name: NASDAQ v. Miami International
Expert for Miami International.
Retained in February 2018.
(Expert declarations submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Qualcomm v. Apple, Case No. 3:17-cv-00108-GPC-MDD (U.S.D.C.S.D. Cal.)
Testifying Expert for Qualcomm.
Completed in April 2019.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Communication Devices
Law Firm: Venable
Case Name: Sycamore IP Holdings LLC v. Verizon Communications Inc, Case No. 2:16-cv-591-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Verizon and Level 3.
Completed in September 2017.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Alston Bird
Case Name: Huawei Technologies Co. Ltd. V. Nokia Solutions and Networks, Case No. 2:16-cv-0056-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Nokia.
Completed in December 2017.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Huawei Technologies Co. Ltd. V. Samsung Electronics C. Ltd, Case No. 3:16-cv-02787 (U.S.D.C. N.D. Cal)
Testifying Expert for Samsung.
Completed in March 2019.
(Expert reports submitted, and deposed.)

Matter: Arbitration for Licensing
Law Firm: Alston Bird
Case Name: Nokia v. LG Electronics, International Chamber of Commerce Arb. No. 21326
Testifying Expert for Nokia.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Ropes and Gray
Case Name: Godo Kaisha IP Bridge 1 v. TCL Communication Technology Holdings, Case No. 15-634-SLR-SRF (U.S.D.C.S.D. Delaware.)
Testifying Expert for IP Bridge.
Completed in October 2018.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Paul Hastings
Case Name: Odyssey Wireless, Inc., v. Samsung Electronics Co., Ltd., et al, Case No. 3:15-cv-1738-H-RBB (U.S.D.C.S.D. Cal.)
Testifying Expert for Samsung.
Completed in October 2016.
(Expert reports submitted.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Greenberg Traurig
Case Name: Mobile Telecommunications Technologies LLC v. Amazon.com, Inc., 2:13-cv-883-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for Amazon.
Completed in April 2015.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Mobile Devices
Law Firm: Mayer Brown
Case Name: Mobile Telecommunications Technologies LLC v. LG Electronics Mobilecomm U.S.A., Inc., 2:13-cv-947-JRG-RSP (U.S.D.C. E.D. Texas)
Testifying Expert for LG Electronics Mobilecomm.
Completed in February 2016.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Semiconductor Devices
Law Firm: Mayer Brown
Case Name: Inter Parte Reexamination for U.S. Patent Nos. 6,895,520 and 6,899,332
Expert for LG Electronics.
Completed in February 2016.
(Expert declaration submitted, and deposited.)

Matter: Patent Infringement in Vehicular Electronics
Law Firm: Gardner, Linn, Burkhardt & Flory, L.L.P
Case Name: *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:12-cv-00654 (Western District of Michigan), and relating to the action styled *Magna Electronics Inc. v. TRW Automotive Holdings Corp. et al.*, Civil Action No. 1:13-cv-00324 (Western District of Michigan).
Testifying Expert for Magna Electronics
Completed in February 2016.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement in Electronic Circuits
Law Firm: Ropes and Gray
Case Name: Certain Devices Containing Non-Volatile Memory and Products Containing the Same (USITC Inv. Nos. 337-TA-922)
Testifying Expert for Spansion Inc.
Completed in February 2015.
(Expert reports submitted.)

Matter: Trade Secret Misappropriation in Software Method for Cable Television Advertisement
Law Firm: Brownstein Hyatt Farber Schreck

Case Name: Cross MediaWorks v. EMT Holdings, USDC Southern District of New York,
Case No. 1:14-cv-00561-VSB
Testifying Expert for Cross MediaWorks.
Completed in April 2015.
(Testified during injunction hearing.)

Matter: Patent Infringement in Vehicular Electronics
Law Firm: Steptoe and Johnson
Case Name: Certain Vision-Based river Assistance System Cameras and Components Thereof
(USITC Inv. Nos. 337-TA-899 and 907)
Testifying Expert for Magna Electronics
Completed in February 2015.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Vehicular System
Law Firm: Susman Godfrey
Case Name: Eagle Harbor Holdings, LLC, and Mediustech, LLC, v. Ford Motor Company,
3:11-cv-05503-BHS (U.S.D.C. Western District of Washington at Tacoma)
Testifying Expert for Mediustech.
Completed in March 2015.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Communication Networks
Law Firm: Davis Polk & Wardwell LLP
Case Name: Sprint Communications Company L.P., v. Comcast Cable Communications, LLC,
Comcast IP Phone, LLC, and Comcast Phone of Kansas, LLC. 2:11-cv-02684-
KHV-DJW (U.S.D.C. Kansas)
Testifying Expert for Comcast.
Retained in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Communication Networks
Law Firm: Quinn Emanuel
Case Name: France Telecom S.A. v. Marvell Semiconductor, Inc., 12-Civ-4986 (S.D.N.Y.)
Testifying Expert for Marvell.
Completed in September 2014.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Wireless Image Distribution
Law Firm: Jones Day
Case Name: *Inter Partes* Review of U.S. Patent No. 8,437,797
Expert for Google Inc.
Completed in November 2014.
(Expert declaration submitted.)

Matter: Nonvolatile Semiconductor Memories

Law Firm: Jones Day

Case Name: *Inter Partes* Review of U.S. Patent Nos. 8,301,833 and 8,516,187
Expert for SanDisk.
Completed in May 2014.
(Expert declaration submitted.)

Matter: Communication Protocols for Wireless Device

Law Firm: Dorsey & Whitney, LLP

Case Name: Certain Point-To-Point Network Communication Devices and Products
Containing Same (USITC Inv. No. 337-TA-892)
Testifying Expert for Toshiba
Completed in May 2014.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Wireless Networks

Law Firm: Ropes and Gray

Case Name: In the Matter of Certain Wireless Devices With 3G and/or 4G Capabilities and
Components Thereof (USITC Inv. No. 337-TA-868) InterDigital Comms., Inc. v.
Huawei Techs. Co., Ltd., No. 13-00008 (D. Del., filed January 2, 2013),
InterDigital Comms., Inc. v. ZTE Corp., No. 13-00009 (D. Del., filed January 2,
2013), InterDigital Comms., Inc. v. Nokia Corp., No. 1:13-cv-00010 (D. Del.,
filed January 2, 2013), InterDigital Comms., Inc. v. Samsung Elec. Co., Ltd., No.
13-00011 (D. Del., filed January 2, 2013)
Testifying Expert for Joint Defense Group.
Completed in February 2014.
(Expert reports submitted, deposited, and testified during trials.)

Matter: Patent Infringement for Mobile Communication

Law Firm: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

Case Name: Certain Digital Media Devices, Including Televisions, Blu-Ray Disc Players,
Home Theater Systems, Tablets and Mobile Phones, Components Thereof and
Associated Software (USITC Inv. No. 337-TA-882)
Testifying Expert for LG Electronics, Inc.
Completed in February 2014.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Wireless Networks

Law Firm: Vinson & Elkins LLP

Case Name: Wi-LAN USA, Inc. and Wi-LAN, Inc. v. Telefonaktiebolaget LM Ericsson and
Ericsson, Inc. (USDC: Southern District of FL - Case #1: 12-cv-23569), Wi-LAN
USA, Inc. and Wi-LAN, Inc. v. Alcatel-Lucent USA, Inc. (USDC: Southern
District of FL - Case #1: 12-cv-23568-Altonaga/Simonton)
Testifying Expert for Wi-LAN.
Completed in May 2015.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Data Storage
Law Firm: Ropes and Gray, Weil Gotshal
Case Name: Summit Data Systems, LLC v. EMC Corporation., et al. 1:10-cv-00749-GMS
(U.S.D.C. Delaware)
Testifying Expert for EMC Corporation and Netapp, Inc.
Completed in December 2012.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Ashurst Australia
Case Name: Samsung v. Apple, Australian Federal Court Proceeding No. NSD 1243 of 2011
Testifying Expert for Samsung Electronics.
Completed in December 2012.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Wireless Mobile Devices
Law Firm: Quinn Emanuel
Case Name: Apple Inc. v. Samsung Electronics Co., Ltd., et al., 4:11-cv-01846-LHK (N.D. Cal.) and Samsung Electronics Co., Ltd., et al. v. Apple Inc., 4:11-cv-02079 (N.D. Cal.)
Testifying Expert for Samsung Electronics.
Completed in July 2012.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Wireless Mobile Device
Law Firm: Quinn Emanuel
Case Name: Certain Electronic Devices, Including Wireless Communication Devices, Portable Music And Data Processing Devices, And Tablet Computer, U.S.I.T.C. Inv. No. 337-TA-794
Testifying Expert for Samsung Electronics.
Completed in June 2012.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Portable Storage Device
Law Firm: White and Case
Case Name: CERTAIN UNIVERSAL SERIAL BUS (“USB”) PORTABLE STORAGE DEVICES, INCLUDING USB FLASH DRIVES AND COMPONENTS THEREOF, US International Trade Commission Investigation No. 337-TA-788
Testifying Expert Witness for Trek
Completed in May 2012.
(Expert reports submitted, and deposited.)

Matter: Copyright Infringement for Petroleum Processing Software
Law Firm: Osha Liang LLP
Case Name: Aspen Technology, Inc. v. Tekin A. Kunt and M3 Technology, Inc., Case Number: H-10-1127, US District Court, Texas, Houston Division.

Testifying Expert for M3 Technology, Inc.
Completed in May 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Trade Secret Misappropriation for DC-DC converter
Law Firm: Covington & Burling, Haynes Boone
Case Name: Certain DC—DC Controllers and Products Containing Same, US International
Trade Commission Investigation No. 337-TA-698
Testifying Expert for UPI.
Completed in March 2012.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Parallel Processor
Law Firm: Orrick, Herrington, & Sutcliffe. Kirkland and Ellis.
Case Name: BIAx Corporation v. Nvidia and Sony Civil Action No. 09-cv-01257-PAB-MEH
Testifying Expert for Nvidia and Sony
Completed in March 2012.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Duffy, Sweeney, and Scott. Foley Lardner.
Case Name: Ronald Katz Technology Licensing v. Citizens Financial Group 7-ML-1816-C
RGK (FFM)
Testifying Expert Witness for Citizens Financial Group.
Completed in 2011.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Storage Area Network
Law Firm: DLA Piper
Case Name: Network Appliance, Inc., v. Sun Microsystems, Inc., Case Number: C-07-06053
EDL, US District Court, Northern District of California, San Francisco Division.
Testifying Expert for Sun Microsystems, Inc.
Completed in 2010.
(Expert reports submitted, and deposed.)

Matter: Patent Infringement for Flat Panel Display Controller
Law Firm: Jones Day
Case Name: Certain Video Displays, Components Thereof, and Products Containing Same, US
International Trade Commission Investigation No. 337-TA-687
Testifying Expert for Vizio, Inc.
Completed in 2010.
(Expert reports submitted, deposed, and testified during trial.)

Matter: Patent Infringement for Call Center Technology
Law Firms: Foley Lardner
Case Name: Ronald Katz Technology Licensing v. US Bank 7-ML-1816-C RGK (FFM)

Testifying Expert Witness for US Bank
Completed in May 2009.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for USB to VGA Converter
Law Firm: Wang Hartmann, Gibbs, & Cauley, P.C.
Case Name: Displaylink Corporation v. Magic Control Technology Corporation, Case No. 5:07-CV-01998-RMW, US District Court, Northern District of California, San Francisco Division.
Testifying Expert for Magic Control Technology Corporation
Completed in 2009.
(Expert reports submitted, and deposited.)

Matter: Patent Infringement for Flash Memory
Law Firm: Jones Day and Wilson Sansini
Case Name: Certain Flash Memory Controllers, Drives, Memory Card, and Media Players and Products Containing Same. US International Trade Commission Investigation No. 337-TA-619
Testifying Expert for SanDisk Corporation.
Completed in 2008.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Semiconductor Packaging
Law Firm: Jones Day
Case Name: Certain Semiconductor Chips with Minimized Chip Package Size and Products Containing the Same. US International Trade Commission Investigation No. 337-TA-605
Testifying Expert for Freescale Semiconductor
Completed in 2008.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Automatic Switching System
Law Firms: Jones Day, and Heller Ehrman, LLP.
Case Name: ATEN International Co., Ltd and ATEN Technology, Inc. v. Belkin Corporation, Belkin Logistics, Inc. and Emine Technology Co., Ltd. US International Trade Commission Investigation No. Ltd 337-TA-589
Testifying Expert for Belkin Corporation, Belkin Logistics, Inc., and Emine Technology Co., Ltd.
Completed in 2007.
(Expert reports submitted, deposited, and testified during trial.)

Matter: Patent Infringement for Dual Mode Communication
Law Firm: Wilmer Cutler Pickering Hale and Dorr, LLP
Case Name: Broadcom Corporation v. Qualcomm Incorporated SACV05-467-JVS (RNBx)
Testifying Expert Witness for Broadcom Corporation
Completed in 2007.

(Expert reports submitted, deposed, and testified during trial.)