IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
AUSTIN DIVISION

CONCURRENT VENTURES, LLC AND XTREAMEDGE, INC., Plaintiffs, v. ADVANCED MICRO DEVICES, INC. AND PENSANDO SYSTEMS, INC., Defendants.	Civil Action No. 1:24-cv-335-ADA

Defendants Advanced Micro Devices, Inc. and Pensando Systems, Inc.'s Reply Claim Construction Brief

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1	79-2	Annotated U.S. Patent No. 8,924,596	
2	79-3	Declaration of R. Jacob Baker Regarding the '596 Patent ("Baker Decl.")	
3	79-4	Annotated excerpts from Plaintiffs' Suppl. Infringement Contentions for the '596 Patent (Dec. 20, 2024)	
4	79-5	Annotated excerpts from *Comprehensive Dictionary of Electrical Engineering* (2d ed. 2005)	AMD-CV-0008603-27
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11	79-12	Annotated excerpts from *Dictionary of Computing* (6th ed. 2010)	AMD-CV-0008721-23
12	79-13	Annotated Jeff Kramer, *Is Abstraction the Key to Computing?* (2007)	AMD-CV-0008990-95
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18	79-19	Annotated excerpts from *Microsoft Computer Dictionary* (5th ed. 2002)	AMD-CV-0008706-08
19	79-20	Annotated excerpts from *Chambers Dictionary* (13th ed. 2014)	AMD-CV-0008702-04
20	79-21	Annotated U.S. Patent No. 10,985,943	
21	79-22	Annotated excerpts from the File History of U.S. Patent 10,985,943	CV-AMD-0000184, 275-289, 302-324
22	79-23	Annotated excerpts from Richard F. Tinder, *Engineering Digital Design* (2d ed. 2000)	AMD-CV-0008872, 888-89, 904, 921, 928-55, 960
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24	79-25	Annotated excerpts from M. Morris Mano, *Digital Design* (2013)	AMD-CV-0008795, 801-809, 834-846
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26	79-27	Annotated U.S. Patent No. 10,944,634	
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33		Annotated copy of Plaintiffs' Proposed Preliminary Claim Constructions (Jan. 23, 2025)	
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Defendants' constructions are supported by the evidence and should be adopted. Plaintiffs repeatedly invoke plain and ordinary, without disclosing its meaning. Courts have faulted a party that "asserts [a] term 'should be given its plain and ordinary meaning' but fails to state what that meaning is." *Polaris PowerLED Techs., LLC v. Samsung Elecs. Am. Inc.*, No. 2:22-cv-496, 2024 Markman 3013293, at *10-11 (E.D. Tex. June 14, 2024) (rejecting patentee's argument in part due to lack of contrary evidence); *see also Regeneron Pharms., Inc. v. Mylan Pharms. Inc.*, No. 1:22-cv-61, 2023 WL 11891335, at *3 (N.D. W. Va. Apr. 19, 2023).

I. Level of Ordinary Skill in the Art

Defendants provided a clear definition of the level of skill for each patent. Plaintiffs did not specifically address those definitions, and those definitions are thus unrebutted.

II. U.S. Patent No. 8,924,596 ("the '596 patent")

A. "queue implemented in hardware" (Claims 1, 7, and 13)

Even though the claim language expressly requires that the queue must be "implemented in hardware," Plaintiffs attempt to broaden this term to also include queues implemented in software. *See* Pls. Br. 4 (arguing that software should be encompassed because "[m]ost queues use pointers, which are processed using software.").[1] Tellingly, Plaintiffs fail to describe any type of queue that would not be "implemented in hardware" under Plaintiffs' interpretation.

A "queue implemented in hardware" is different from a queue implemented in software. Defs. Br. 2. But under Plaintiffs' interpretation, any queue implemented in software would also be implemented in hardware because software runs on computer processors and memory. Defendants' construction prevents this overbroad reading by giving full effect to the claim term and explaining how the plain and ordinary meaning of a "queue implemented in hardware"

[1] All emphasis in this brief is added unless otherwise noted.

excludes software implementations. Even Plaintiffs' expert agrees, quoting a passage that a device being "hardware-based" means "it lacks a processor" to run software. Min Decl. ¶32.

Plaintiffs argue that the claims and specification require software intervention in queues. Not so. The cited passages only describe how software may use a queue by reading from or writing to it; they do not address how the queue is implemented. Plaintiffs conflate usage with implementation, shifting focus from the actual requirement that the queue is implemented in hardware. Whether software can access the queue is irrelevant. Defendants' construction correctly addresses implementation and does not preclude software from using the queue.

B. "register" (Claims 1, 7, 13)

The central dispute is whether "register implemented in hardware" includes a variable stored in memory. Without seeing Defendants' construction, Plaintiffs' originally proposed "register" to be "a memory location within a microprocessor used to store values and external memory addresses." Ex. 33 at 2. Plaintiffs still pursue their original construction, though they no longer request it. For example, they and their expert argue that a "required feature of a register is a known memory location that other aspects of the system, including software, can access while certain instructions are executed." Min Decl. ¶38; Pls. Br. 7 ("Fundamentally, a register is a storage area that can be addressed by name…"). Plaintiffs expand "register" to include random access memory (RAM). Pls. Br. 7 ("[A] register can also store bits in other ways, such as using Static RAM (SRAM)[.]"). Plaintiffs equate "register" with a memory location because it underpins their infringement theory. Compl. ¶40 (accusing "DRAM-based qstate record"). But it is clear, based on the plain meaning of "register" and the intrinsic record, that a register refers to concrete hardware—it cannot simply be a variable or location in memory.

The specification distinguishes between a "register implemented in hardware" and variables in memory, expounding on the disadvantages of using variables in memory. The patent

details at length how prior software techniques used an "available space count variable in memory," but this required "additional processing time, making this process non-optimal." '596 pat., 1:25-29. To overcome the disadvantages of variables in memory, the patent "provides a shared counter resource (e.g., a register) in the hardware representing how much free space there is in the command queue." *Id.*, 3:30-34. The use of a hardware register avoids the need for a variable in memory: "[t]here is no need for the software overhead of … a shared available space count variable in shared memory or otherwise." *Id.*, 4:16-19. Allowing the register to be a variable in memory would reintroduce the very issues the patent was trying to solve. And the specification describes an auto-decrementing hardware register that would not function if a register were merely a memory location. Defs. Br. 7.

Plaintiffs do not reconcile their interpretation with these passages. The claim language and specification thus provide ample support for excluding variables or memory locations from "register," which more than satisfies any requirement from *Polaris* or *Network-1* that a narrowing construction be supported by the intrinsic record. In any event, this is not a narrowing construction because it simply reflects the plain meaning of "register." Defs. Br. 7-8.

A construction that makes clear that a "register implemented in hardware" does not encompass variables stored in memory resolves the material claim construction dispute for this term. The remainder of Defendants' construction—such as references to flip-flops—describes what it means for a register to be implemented in hardware. But these details are tangential to the central dispute. Regardless of whether the Court adopts a construction involving flip-flops, a register cannot simply be a variable or location in memory.

Nonetheless, all evidence confirms that a register is a specific hardware structure built from flip-flops. Plaintiffs argue that registers do not require flip-flops but offer no alternative

implementation, other than unsupported expert testimony that a register could be a storage area in memory (RAM). Pls. Br. 7. As already explained, the intrinsic record forecloses equating registers with memory locations; expert testimony cannot be used to contradict the intrinsic record. *Genuine Enabling Tech. LLC v. Nintendo Co.*, 29 F.4th 1365, 1373 (Fed. Cir. 2022). Even Plaintiffs' extrinsic evidence contrasts registers with memory. Ex. E at 71 ("[R]egisters—like other forms of storage internal to the CPU—are faster than memory.").

Plaintiffs also argue that registers "are not solely composed" of flip-flops because they can also include other components. Pls. Br. 7-8. That is irrelevant; Defendants' construction simply requires that a register contains flip-flops, not that they are exclusive. Plaintiffs argue that a "register *includes* flip-flops, *as well as* inputs and outputs[.]" Pls. Br. 8 (emphasis in original). Of course registers have inputs and outputs to store and provide bits. This is entirely consistent with Defendants' construction.

III. U.S. Patent No. 9,529,767 ("the '767 patent")

A. "abstraction protocol" (Claims 1, 2, 4, 6 and 16)

Plaintiffs contend "abstraction protocol" should be given its plain and ordinary meaning, yet fail to prove its meaning in the field of computer storage, nor that it connotes structure. While contending abstraction protocol "is a widely known and used term" (Pls. Br. 10), Plaintiffs do not point to any patents, publications, or dictionaries that used the term. Instead, Plaintiffs rely solely on Dr. Min's opinion; however, he lacks relevant expertise because none of his recited qualifications even mention computer storage. Min Decl. ¶¶3-16.

Plaintiffs assert the term "refers to a class of conventional, publicly disclosed protocols" and that Dr. Min identifies "two examples of conventional, publicly disclosed abstraction protocols[.]" Pls. Br. 11. His first example is TCP. Min Decl. ¶49. Despite its age and renown, Dr. Min cannot point to an instance where the moniker "abstraction protocol" was applied to

TCP. His second example is even more suspect: an unnamed "protocol used by virtual machines." *Id.* Dr. Min further opines that the claimed abstraction protocol "hides details of the SATA/SAS devices from the host accessing the SATA/SAS devices." *Id.* Tellingly, Dr. Min provides no explanation of how either example hides details of SATA/SAS storage devices.

Plaintiffs argue the claim language and specification provide details for the abstraction protocol. Br. 11 & 13. But Defendants' expert explained how the cited portions merely recite features the abstraction protocol should have, without disclosing any implementation details, nor connoting a known structure. Long Decl. ¶¶16-17; Defs. Br. 11. Plaintiffs do not rebut Dr. Long because they rely on a conclusory opinion that does not explain how the cited portions reflect structural or implementation details. *Compare* Min Decl. ¶51 *with* Long Decl. ¶¶16-17.

Plaintiffs complain of parsing "abstraction protocol" into "abstraction" and "protocol." Pls. Br. 11-12. But their expert relies on definitions for "abstraction," not "abstraction protocol." Min Decl. ¶50. Because there are no definitions for "abstraction protocol," it is correct to start with the meaning of individual words to find their combined meaning. *Altiris, Inc. v. Symantec Corp.*, 318 F.3d 1363, 1372 (Fed. Cir. 2003) ("[S]imply because a phrase as a whole lacks a common meaning does not compel a court to abandon its quest for a common meaning and disregard the established meanings of the individual words."). Plaintiffs' cases are inapt. For example, in *Apex*, the court erred by isolating the word "circuit" without analyzing the limitation as a whole. *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1372 (Fed. Cir. 2003).

Plaintiffs' complaints about means and function also fail. Plaintiffs argue "abstraction protocol" is not a "means" to do anything because it "is a set of 'high-level access commands' (i.e., 'rules') that the various parts of the system can use to communicate[.]" Pls. Br. 9-10. But this rewrites the specification, which states that the "abstraction protocol provides high-level

access commands to storage media devices." '767 pat., 4:4-7. Thus, Plaintiffs improperly transform a statement of function (what the protocol provides) into a definition of what the protocol is. Continuing this flawed logic, they argue that a set of rules cannot perform a function, with an analogy to spoken English. Pls. Br. 10. Their analogy fails because the rules of English are functional – they provide a way for human communication. Plaintiffs also contend that relevant claim language shows "various controllers and the 'storage media device' communicate via the abstraction protocol." Pls. Br. 9. This further confirms that the "abstraction protocol" performs a function, which is enabling communication between controllers and storage devices. Long Decl. ¶¶18-20.

Next, Plaintiffs do not appear to dispute that "abstraction is a highly-subjective design process," but argue that fact does not mean that §112(f) applies. Pls. Br. 12. Plaintiffs' argument relies on *Personalized Media*, but the court found that "detector" is a structural term because it connotes a variety of known structures to those skilled in the art. *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 705 (Fed. Cir. 1998). "Abstraction protocol" does not connote any particular structure, let alone a variety of known structures.

B. "storage media device interface" (Claims 1 and 16)

Plaintiffs' construction is overly broad and contradicts the specification's description of the storage media device interface. Plaintiffs suggest that the interface could encompass non-hardware implementations and cite extrinsic evidence. Pls. Br. 15. But the extrinsic evidence is unavailing because the intrinsic record makes clear that the interface is physical. The specification states that the storage media device interfaces communicate with the storage media devices "via SATA and/or SAS links" ('767 pat., 5:38-40, 6:33-35), which are known physical, point-to-point links. For the storage media device interface to operate "via SATA and/or SAS links," it must be a physical interface.

Plaintiffs argue the construction's recitation of edge controller is redundant because claim 1 indicates the interface is located within the edge controller. Pls. Br. 15-16. Next, Plaintiffs contend that no such limitation applies to claim 16, asserting claim 16 "does not require 'storage media device interface' to be a part of any other component of the system." *Id*. Not so. Claim 16 recites a routable packet-switched network comprising "at least one host," "a first master controller," and "at least one first edge controller." '767 pat., 14:1-10. Following the semicolon and "and," the claim makes clear "at least one first edge controller" is the final element of the routable packet-switched network and that this element comprises additional components, including "at least one storage media device interface." This claim structure is reinforced by the file history. The indentations in original claim 17 (issued claim 16) indicate that "at least one host," "a first master controller," and "at least one first edge controller" are parallel elements, and "storage media device interface" is a subordinate element under "at least one first edge controller." Ex. 34 at 5-6. Thus, consistent with claim 1, claim 16 demonstrates that the "storage media device interface" is component of the "first edge controller."

The specification describes how the master controller communicates with the host and the edge controller ('767 pat., 4:64-5:4), while only the edge controller can communicate with storage media devices (*id*., 5:38-40, 6:32-35). Plaintiffs do not dispute that the specification identifies the storage media device interface as the only structure that enables communication with storage media devices. *Id*., 12:44-45; Defs. Br. 13. The interface must be located within the edge controller, otherwise the edge controller could not perform its exclusive role of communicating with the storage media devices. Every figure that includes the "storage media device interface" shows it positioned within the "edge controller." '767 pat., Figs. 4A and 4C.

IV. U.S. Patent No. 10,873,753 ("the '753 patent")

A. "interleaved memory" (Claims 4, 7, 15)

Plaintiffs argue Defendants' construction is not supported by intrinsic evidence. Pls. Br. 18. But it reflects the patent's sole description of interleaved memory, which states "[a]nother arrangement of memory superposition 140 is interleaved memory, to achieve an average access bandwidth." '753 pat., 8:35-40. Because memory superposition requires different types of memory, the correct construction of interleaved memory is an "arrangement of different types of memory that are alternately accessed to achieve an average access bandwidth."

The specification further states that bandwidth and power could be blended. *Id.* Defendants' construction captures this concept: when different types of memory are alternately accessed to achieve an average access bandwidth, their bandwidth and power characteristics are blended. Lin Decl. ¶¶47-48. Plaintiffs' construction does not give this statement effect because a mere blend of different types of memory together, without any particular organization or result, is insufficient to produce the stated blend of power and bandwidth characteristics.

Plaintiffs equate "interleaved" memory with blended memory, but the patent only refers to a "blend" of bandwidth and power characteristics, not a blend of the memory types themselves: "Input bandwidth, output bandwidth, or power could be blended among different types of RAM or drives …." '753 pat., 8:35-40. Plaintiffs alter this text by deleting bandwidth and power and restructuring the sentence to create "a 'blend[] among different types of' memory." Pls. Br. 18. The patent never refers to a "blend" of different types of memory, nor does it ever explain what that would mean. Plaintiffs likewise provide no explanation.

Moreover, Plaintiffs' construction is redundant of another claim term "memory superposition," which already uses "two or more types of memory" together. '753 pat., 7:1-9. Plaintiffs assert, without explanation, that this differs from two or more types of memory that are

"blended together," but they offer no meaningful distinction. *See* Pls. Br. 18.

Plaintiffs also take issue with "alternate" access, arguing it is unsupported. Pls. Br. 19. But Plaintiffs' own *Electrical Engineering Dictionary* defines interleaved memory as "a memory system with … an assignment of addresses that makes consecutive accesses fall into different modules." Pls. Ex. F (CV-AMD0017674). This supports Defendants' construction—that the different types of memories are "alternately accessed."

Plaintiffs criticize Defendants for "importing an outcome" of achieving average access bandwidth. Pls. Br. 18-19. But Defendants merely follow the patent's sole description of interleaved memory. Ironically, Plaintiffs rely on the very next sentence, which also describes blending bandwidth and power, but alter its meaning to suit their purposes as explained above. Plaintiffs' cited cases are inapposite because they involved constructions that added limitations not found in the specification or that rendered other claim language meaningless. *See United Therapeutics* at *1368-1369 (rejecting safety and efficacy limitations based on expert opinion because the claims already recited the effect); *Puma Biotechnologies* at *4 ("limiting the claims to administering an 'effective amount' would make the term 'unit dosage' meaningless").

Lastly, Plaintiffs distort the evidence to suggest that interleaved memory includes arrangements that do not alternate access. However, their cited dictionary definition of "interleaved memory" confirms that in "sequential interleaving," memory modules are organized so that sequential addresses are alternated to the next module for each address. Min. Decl. ¶62; Pls. Ex. F (CV-AMD0017674–5). Likewise, the other enumerated descriptions are consistent with alternating access. Plaintiffs speculate that interleaved memory can be accessed "in a staggered or parallel fashion" (Pls. Br. 19) but offer no explanation why these approaches would exclude alternating access. Their support—conclusory expert testimony, a dictionary, and a

textbook—does not mention "staggered" or "parallel." *See* Min Decl. ¶¶62-64.

B. "swapped memory over a specified address range" (Claims 4, 7, 15)

Plaintiffs' brief states their actual construction: "The plain and ordinary meaning of 'swapped memory over a specified address range' is … memory that has been swapped (or moved) between storage locations for a specified range of memory addresses." Pls. Br. 19-20. But Plaintiffs fail to explain what it would mean to swap or move memory (as opposed to data) between storage locations. It is unclear whether this requires physically replacing one memory for another or some other scheme not described by the patent. Consequently, interpreting the claim language in isolation, as Plaintiffs urge, leads to nonsensical results.

For this reason, the term "swapped memory" should be considered as a whole, consistent with its clear and well-established meaning in the art. Extrinsic evidence is important here because, as Plaintiffs admit, the specification mimics the claim language and provides no further guidance. This lack of explanation indicates this is a term of art with a specific, recognized meaning, and a "proper claim construction cannot be reached without the aid of extrinsic evidence." *Actelion Pharms. LTD v. Mylan Pharms. Inc.*, 85 F.4th 1167, 1173-1174 (Fed. Cir. 2023). Thus, construction would "assist the jury to understand the claims." *Tech Pharmacy Servs., LLC v. Alixa Rx LLC*, 2016 WL 6397358, at *15 (E.D. Tex. Oct. 28, 2016). Plaintiffs argue that extrinsic evidence cannot be used to change intrinsic meaning (Pls. Br. 20), but that is exactly the point: the patent provides no intrinsic meaning for "swapped memory."

In an attempt to support their broader construction, Plaintiffs cite an irrelevant example of "bank switching," which they claim is a type of "swapped memory" that moves memory between memory locations without requiring non-volatile storage. Pls. Br. 20. But Plaintiffs' cited dictionary entry for "bank switching" does not mention "swapping" at all. Pls. Ex. G at 51. And the dictionary definitions for swapping do not mention bank switching. Ex. 18 at 504; Ex.

19 at 1570. Moreover, "bank switching" merely switches between banks to access them one at a time; it does not move memory or data. Pls. Ex. G at 51. In contrast, Defendants' cited definitions specifically address the movement of information in memory. Defs. Br. 17.

Plaintiffs argue the cited dictionaries lack a separate entry for "swapped memory." However, the dictionaries define swap, swapping, and swap file in the context of memory (Ex. 18 at 504), confirming that "swap" has a recognized plain and ordinary meaning in this context.

C. "one or more swappable pods or cards" / "the plurality of …" (Claims 1-6)

Plaintiffs' argument is premised on the notion that the word "plurality" can mean one or more. But Plaintiffs cite cases that discuss plural forms of claim terms. None held that the word "plurality" itself means one. To do so would fly in the face of basic conventions of patent law and the English language. *See, e.g.*, *Dayco Prods., Inc. v. Total Containment, Inc.*, 258 F.3d 1317, 1328 (Fed. Cir. 2001) ("ordinary definition of 'two or more.'").

V. U.S. Patent No. 10,985,943 ("the '943 patent")

A. "programmable logic device" (Claims 1, 10)

According to Plaintiffs, "something qualifies as a PLD if the electronic circuitry can be programmable or reprogrammable." Pls. Br. 23. Implicit in Plaintiffs' argument is the assertion that circuits qualify as programmable simply because they can run software or firmware programs, even if the underlying circuits cannot be changed. Plaintiffs expand PLD to encompass devices with fixed hardware functions, treating them as user-programmable solely because a user can execute software or firmware programs on the device. *See* Pls. Br. 24-25 (emphasizing specification language referring to "processors or controllers" and positing that "a PLD 'can provide configurability of the circuitry in any variety of manner'").

Plaintiffs fail to address the lexicography in the file history, which defines "PLD" as "a specific type of integrated circuit that has user programmable electronic circuits." Ex. 21, CV-

AMD000308. The claims similarly require "user-definable circuits." Thus, a PLD must contain circuits the user can program (and thereby alter) to define the functionality of the hardware.

Judge Payne rejected a similarly broadening construction of PLD in *802 Systems*. Plaintiffs misrepresent Judge Payne's construction, arguing that it "allows the PLD to be 'reprogrammed with code' (i.e., software)." Pls. Br. 25-26. Judge Payne reached the opposite conclusion, holding "that what must be programmable is hardware" (emphasis in original) and rejecting the plaintiff's attempt "to capture ASIC systems … [where] the device 'allows updating' by way of software[.]" *802 Sys. Inc. v. Cisco Sys., Inc.*, 2021 WL 3403647, *5 (E.D. Tex Aug. 4, 2021). The "code" in *802 Systems* does not refer to software; it refers to hardware configuration data called "PLD code." *See* Ex. 35 (U.S. Pat. 7,013,482), 17:50-59 ("The logic of PLD … The PLD code"). Construction was needed in *802 Systems* and is equally needed here because Plaintiffs "would depart from the evidence of the known meaning of 'programmable logic device' in the art[.]" *802 Sys*. at *8.

Realtime supports Defendants' construction because the court construed "PLD" to mean "digital hardware component that is reconfigurable," confirming that a PLD must include hardware that is alterable. *Realtime Data, LLC v. Packeteer, Inc.*, 2009 WL 10742296, *24, *23-24 (E.D. Tex. June 22, 2009). *Altera* does not construe PLD; its background section merely discusses how PLD circuits are programmed, which both parties agree is irrelevant. *Altera Corp. v. Clear Logic, Inc.*, 424 F.3d 1079, 1081 (9th Cir. 2005).

Lastly, Plaintiffs point to portions of the specification describing processors and software. Pls. Br. 24-25. But Plaintiffs conflate the "programmable device" from the preamble with the claimed "programmable logic device" from limitation [1a]. These are separate claim terms, and Plaintiffs mistakenly cite a discussion of one for the other. *See* '943 pat., 4:27-39 ("The

programmable device could be, for example, an FPGA … a PLD or an ASIC, or more than one of these, or some combination of these, … in some versions including one or more processors or controllers."). This quotation simply states that the programmable device—which in some embodiments may contain a PLD—can optionally include processors or controllers. It does not mean that anything with a processor is automatically a PLD.

Fundamentally, a PLD must have circuits the user can alter. Whether it also runs software is irrelevant. Defs. Br. 21-22. The circuits inside a PLD can be changed into a processor that runs software. *Id.* For example, the patent refers to a "softcore" processor ('943 pat., 7:15-20) and notes that PLDs may "optionally includ[e] processors" apart from and in addition to user-definable circuits (*id*., 3:8-13). But even if some PLDs can be made to run software, not everything that runs software is a PLD. Plaintiffs' argument is a logical fallacy: some dogs have tails, but not everything with a tail is a dog.

Regarding Defendants' construction, Plaintiffs challenge three aspects. Pls. Br. 23-24. However, Plaintiffs are contradicted by the intrinsic record. *First*, Plaintiffs dispute whether PLDs have an alterable interconnection pattern of circuits. The lexicography supports defining PLDs as having "user-programmable circuits," meaning the user can alter the circuits, while the claims likewise require "user-definable circuits" in the PLD. Because an electronic circuit is a path (hence the term "circuit"), users define a PLD's function by changing the interconnection patterns of those circuits. *See* Ex. 23 at 171 ("[I]nterconnection pattern can be programmed (either mask-programmed or user-programmed) to perform specific logic functions").

Second, Plaintiffs argue that PLDs do not require physical alteration. Pls. Br. 23. But so long as the user can alter the PLD's circuits, the method used is irrelevant. Whether the circuits are changed by blowing fuses or by using a controller running specialized software or firmware

that alters circuitry, the essential point is that these techniques modify the actual connection patterns of circuits within the PLD. Defs. Br. 22-25. Thus, Plaintiffs' argument that software can be used to configure circuits misses the mark—what matters is that the user can change the underlying circuits, not the method used to do so.

Third, Plaintiffs argue that a PLD is not limited to an integrated circuit. Pls. Br. 24. Under Plaintiffs' construction, a PLD need only be "a 'logic device' (not just an 'integrated circuit,' as Defendants propose)[.]" Pls. Br. 25. The lexicography states that a PLD is an "integrated circuit." Ex. 21, CV-AMD000308.

VI. U.S. Patent No. 10,944,634 ("the '634 patent")

A. "geographical area" (Claims 1, 8, and 15)

Ample intrinsic and extrinsic evidence supports Defendants' construction. Plaintiffs concede a "geographical area" is a "synonym[]" of a "physical place[]." They fail to address the dictionaries cited by Defendants. Though Plaintiffs assert "geographical area" is "easily understood," they do not attempt to articulate what they "easily" understand the term to mean.

Lexicography or disclaimer is not required for claim construction to be proper. Moreover, Plaintiffs' argument that "examples should not limit claim scope" misses the point because Defendants' construction does not limit the term to any specific example. The examples in the construction exemplify "physical places" and are supported by the specification. Plaintiffs also do not dispute that the only examples of "geographical area" in the specification are physical places (rather than non-physical concepts such as an IP address). These undisputed facts support Defendants' construction. *See Kinetic Concepts, Inc. v. Blue Sky Med. Grp., Inc.*, 554 F.3d 1010, 1019 (Fed. Cir. 2009) (limiting "wound" to "skin wound," rather than allowing it to encompass "pus pockets," where all specification examples involved skin wounds).

"Even where prosecution history statements do not rise to the level of unmistakable

disavowal, they do inform the claim construction." *Personalized Media Commc'ns, LLC v. Apple Inc.*, 952 F.3d 1336, 1340 (Fed. Cir. 2020). Plaintiffs say that applicant's "failure to say something" does not qualify as disclaimer, but the applicant *did* say something—that "Cole is silent as to geographical area" even though Cole discloses IP connections. Defs. Br. 27-28. Plaintiffs did not dispute that a POSITA would have recognized Cole's disclosure of voice-over-IP calls and HTTP tests involves IP addresses. Jeffay Decl. ¶12. Moreover, it is incorrect as a matter of law to say that an applicant must specifically disclaim something for it to be excluded.

The parties' dispute regarding "geographical area" is a claim construction issue, not an infringement issue, and should be resolved at this juncture. Defendants ask the Court to decide whether to construe a "geographical area" as a "physical place such as an apartment complex, neighborhood, city, or state." The jury can decide whether such a construction encompasses an IP address in the context of Plaintiffs' infringement claims.

B. "network connected device" (Claims 16 and 20)

Plaintiffs argue that the network connected device "control[s]" the endpoints to perform operations. Pls. Br. 30. But this asks the Court to redraft the claims, e.g., from "send the parameter values … from the first endpoint device" to "<u>control</u> the first endpoint device to send the parameter values." However, "courts may not redraft claims, whether to make them operable or to sustain their validity." *Chef Am., Inc. v. Lamb-Weston, Inc.*, 358 F.3d 1371, 1374 (Fed. Cir. 2004). Even if the network connected device were to control the endpoint to perform the operations, this would contradict the claims' explicit requirement that the <u>network connected device</u> perform the operations. '634 pat., 15:40-42, 16:11, 16:15, 20, 41-42, 45-46. Further, the overhead caused by Plaintiffs' interpretation (e.g., communicating instructions for performing the operations in packets to endpoints) contradicts the patent's disclosure of offloading calculation from endpoints to a tuner server. *See* '634 pat., 4:35-37, 4:42-44, 4:55-5:2, 5:5-9.

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that on this 28th day of May, 2025, I electronically filed the foregoing **Defendants' Reply Claim Construction Brief (including exhibits and declarations)** with the Clerk of the Court using the CM/ECF system which will send notification of such filing to the following:

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