

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ADVANCED MICRO DEVICES, INC. AND PENSANDO SYSTEMS, INC.,

Petitioners,

v.

CONCURRENT VENTURES, LLC AND XTREAMEDGE, INC.,

Patent Owners.

Case No. IPR2025-00486
U.S. Patent No. 10,873,753

**PATENT OWNERS' PRELIMINARY RESPONSE TO PETITION FOR
INTER PARTES REVIEW**

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PATENT OWNERS' EXHIBIT LIST

Exhibit	Description
2001	Text Order Denying AMD/Pensando's Motion to Stay Case (Judge Robert Pitman) in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2002	First Amended District Court Scheduling Order (Dkt. 77) in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2003	Webpage printouts of Docket Navigator Time to Trial regarding the District Court for the Western District of Texas and Judge Alan D. Albright
2004	Webpage printout of "AMD Reports Fourth Quarter and Full Year 2024 Financial Results" dated March 4, 2025 (https://ir.amd.com/news-events/press-releases/detail/1236/amd-reports-fourth-quarter-and-full-year-2024-financial-results)
2005	AMD/Pensando's Invalidity Contentions (Cover Pleading) in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2006	AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2007	Declaration of Dr. R. Jacob Baker submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2008	Declaration of Darrell Long submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XstreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)

2009	Declaration of Bill Lin submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2010	Declaration of Kevin Jeffay submitted by AMC/Pensando in support of AMD/Pensando's Opening Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2011	CV/XE's Responsive Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2012	Declaration of Dr. Paul Min submitted by CV/XE in support of CV/XE's Responsive Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2013	AMD/Pensando's Reply Claim Construction Brief in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)
2014	CV/XE's Objection to the Report and Recommendation of the U.S. Magistrate Judge in <i>Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.</i> , No. 1-24-cv-00335 (W.D. Tex. 2024)

Concurrent Ventures, LLC (“CV”) and XtreamEdge, Inc. (“XE”) (collectively “CV/XE” or “Patent Owners”) respectfully submit this Patent Owners’ Preliminary Response (POPR) to the Petition for *Inter Partes* Review (“IPR”) of U.S. Patent No. 10,873,753 (“the ’753 patent”) filed by Advanced Micro Devices, Inc. (“AMD”) and Pensando Systems, Inc. (“Pensando”) (collectively “AMD/Pensando” or “Petitioners”).

I. INTRODUCTION

Patent Owners submitted their Brief in Support of Patent Owners’ Request for Discretionary Denial of Institution of *Inter Partes* Review (Paper 6, “Discretionary Denial Brief”) on June 4, 2025. The Director and Board should deny institution of AMD/Pensando’s Petition against CV/XE’s ’753 patent for all the reasons stated therein and thus need not reach the merits of the Petition (except as relevant to the discretionary denial analysis). Even if the Board does reach the merits, however, institution should still be denied. As explained below, none of the Petition’s obviousness grounds establishes a reasonable likelihood of prevailing against any challenged claim. Instead, Petitioners’ theories rely on hindsight-driven distortions of the prior art that overstate or outright misstate the contents of the prior art in key respects.

II. BACKGROUND

A. Overview of the '753 Patent

The inventors of the '753 patent recognized a problem in the art relating to data processing architectures as of the patent's effective filing date: software-based systems offered flexibility and ease of use but were often inferior to hardware-based systems with respect to processing power. EX1001, 1:8-11. Pure hardware-based systems, in contrast, offered superior processing speeds but were not a desirable alternative because "redesigning dedicated hardware each time a new data processing application or data formatting requirement comes up is an expensive proposition." *Id.*, 1:11-14. Further, "designing, debugging and manufacturing dedicated electronic hardware is time-consuming, especially when revision cycles are taken into account." *Id.*, 1:14-16.

To address this problem in the art, the inventors of the '753 patent developed an innovative hybrid data-processing platform that offers the processing speed advantage of hardware while retaining much of the flexibility of software-based systems. Specifically, the inventors conceived of an architecture that utilizes one or more swappable pods or cards that include a portion for user-definable hardware modules or user-definable software modules, with the pods or cards communicatively linked via a messaging interface network. This innovation is reflected in the claims of the '753 patent.

B. The Claims of the '753 Patent

The language of the three independent claims of the '753 patent is reproduced below. For convenience, Patent Owners have included the limitation labels used by Petitioners.

Claim 1:

1[pre] A platform for data flow processing, comprising:

[1a] one or more swappable pods or cards in one or more chassis,
coupled through a messaging interface network;

[1b] each of the one or more swappable pods or cards having one or more
hardware modules or one or more software modules;

[1c] one or more of the plurality of swappable pods or cards having a
portion for user-definable hardware;

[1d] the plurality of swappable pods or cards being user-configurable to
implement data flow processing architectures; and

[1e] a network coupled to the one or more swappable pods or cards and
supporting messaging-based communication using packets each having a header
with a chassis identifier, a board identifier, a module identifier, an instance
identifier, and a type identifier, so that each type of module, each instance of a

type of module, and each module on each board in each chassis can be addressed through the header.

EX1001, claim 1; *see also* Pet., 98 (claim appendix).

Claim 7:

[7pre] A method for data flow processing in a platform, comprising:

[7a] configuring a plurality of swappable pods or cards in one or more chassis, coupled through a messaging interface network, to implement a data flow processing architecture;

[7b] configuring user-definable hardware modules or user-definable software modules in each of one or more of the plurality of swappable pods or cards;

[7c] communicating a data flow in accordance with the implemented data flow processing architecture among one or more hardware modules or one or more software modules in each of the plurality of swappable pods or cards, including the user-definable hardware modules or user-definable software modules; and

[7d] selecting a memory superposition in at least one of the plurality of swappable pods or cards having a plurality of types of memory with selectable arrangement of the plurality of types of memory as multilevel cache, interleaved

memory, swapped memory over a specified address range, and memory allocated to specified address ranges according to parameterized task needs.

EX1001, claim 7; *see also* Pet., 99-100 (claim appendix).

Claim 13:

13[pre] A tangible, non-transitory, computer-readable media having instructions thereupon which, when executed by a processor, cause the processor to perform a method comprising:

[13a] configuring a plurality of swappable pods or cards in one or more chassis, coupled through a messaging interface network, to implement a data flow processing architecture;

[13b] configuring user-definable hardware modules or user-definable software modules in each of one or more of the plurality of swappable pods or cards;

[13c] communicating a data flow in accordance with the implemented data flow processing architecture among one or more hardware modules or one or more software modules in each of the plurality of swappable pods or cards, including the user-definable hardware modules or user definable software modules; and

[13d] communicating the data flow through the messaging interface network, comprising a network coupled to the plurality of swappable pods or

cards and supporting messaging-based communication using packets each having a header with a chassis identifier, a board identifier, a module identifier, an instance identifier, and a type identifier, so that each type of module, each instance of a type of module, and each module on each board in each chassis can be addressed through the header.

EX1001, claim 13; *see also* Pet., 101-02 (claim appendix).

C. The Parallel Litigation

Patent Owners, CV/XE, are presently asserting the '753 patent in the following district court action: *Concurrent Ventures, LLC and XtreamEdge, Inc. v. Advanced Micro Devices, Inc. and Pensando Systems, Inc.*, No. 1-24-cv-00335 (W.D. Tex. 2024).

D. The Petition's Relied-Upon Prior Art References

1. U.S. Patent Application Publication No. 2013/0346667 A1 ("Stroud") (EX1004)

Stroud, by its own terms, is directed to "systems and methods for testing communications networks, services, and devices, e.g., testing the traffic-handling performance and/or security of the network, network accessible devices, cloud services, and data center services." EX1004, ¶0001. Stroud discusses an increased cyber security threat environment and the importance of network security testing

(*id.*, ¶¶2-3) and notes the importance of “content-aware and software-driven packet inspection.” *Id.*, ¶5.

To address these issues, Stroud proposes a “network testing system 16” that “may be configured to test the performance (e.g., traffic-handling performance) of devices 14, the security of a test system 18 (e.g., from security attacks), or both the performance and security of a test system 18.” *Id.*, ¶81. Stroud’s proposed network testing system “*may* include *a chassis 50* including any suitable number of slots 52, each configured to receive a modular card, or blade, 54.” *Id.*, ¶98.¹ There is no disclosure in Stroud of multiple chassis or suggestion that multiple chassis would be useful or desirable. Nor does Stroud discuss or contemplate large-scale data storage or suggest that its teachings would be relevant to data center design.

Communication between certain internal components in Stroud’s system occurs via “backplane 56.” *Id.*, ¶101. This communication can occur via an internal Ethernet that is not connected to external networks and thus does not require that each component have a “globally unique” MAC address. *Id.*, ¶366. Stroud discloses that, “in some embodiments, each network processor 105 and CLD in system 16 automatically derives a 6-byte MAC address for itself” utilizing a specific format. *Id.*, ¶366. As discussed below, this six-field format for internal Ethernet

¹ All emphasis supplied unless otherwise noted.

communications does not include the “module identifier” required by the claims. Nor does it include a “chassis identifier”—since Stroud does not disclose or suggest multiple chassis.

2. U.S. Patent No. 9,148,389 (“DaSilva”) (EX1005)

The Petition relies on DaSilva for its teachings regarding a “chassis ID.” Pet., 19 (citing EX1005, Abstract). Notably, however, DaSilva’s title is “System and method for a virtual chassis system,” and its teachings are exclusively about the use of *virtual* chassis—there is no disclosure of the use of any physical chassis. Accordingly, as the Petition acknowledges, its teachings regarding the use of a chassis ID relate to a “virtual chassis system.” Pet. 52.² There is no teaching in DaSilva regarding the use of a chassis ID with respect to physical chassis.

3. “Memory Systems and Pipelined Processors” (“Cragon”) (EX1006)

Cragon is a 1996 computer textbook that provides an overview of a variety of general concepts and considerations relating to memory systems as of that date. The Petition relies on Cragon to supply the “selectable arrangement” of “types of

² The Petition goes on to state that DaSilva’s virtual chassis system “allowed multiple physical chassis to be grouped together.” Pet. 52. The language of DaSilva cited in support of this proposition, however, never mentions physical chassis and instead merely discusses how in DaSilva’s “virtual chassis system 100,” a “plurality of network nodes 110 operate as a single virtual network node with unified management capabilities.” EX1005, 3:64-4:7, 4:23-38; Pet. 52 (citing same).

memory” required by claim element 7[d], as well as the specific types of memory enumerated in the claim. Pet. 73-78. In fact, however, Cragon merely provides a general overview of various memory configurations, and includes no disclosure of the specific “selectable arrangement” required by the claims. Further, Cragon does not disclose, among other limitations, the claimed “memory allocated to specified address ranges according to parameterized task needs.” To the contrary, the portions of Cragon that Petitioners rely upon merely disclose a high-level discussion of general design considerations and shortcomings in then-contemporary memory systems—there is no disclosure of the allocation of memory to specific address ranges according to parameterized task needs. EX1006, 000536-548.

**4. U.S. Patent Application Publication No. 2002/0087821
 (“Saulsbury”) (EX1007)**

Petitioner—apparently recognizing the shortfalls of its Cragon-based theory for this limitation—relies on Saulsbury in Ground 3 to supply the “selectable arrangement” of “types of memory” required by claim element 7[d]. Pet. 84-85. As discussed below, however, Saulsbury does not teach a “selectable arrangement” of the particular types of memory specified by the claims, and thus does not resolve the defects in the Stroud/Cragon combination.

E. The IPR Petition’s Alleged Unpatentability Grounds

Grounds	Claims	Statutory Basis	Prior Art
1	1–3, 13, 14	§103	Stroud in view of DaSilva
2	7, 9-10	§103	Stroud in view of Cragon
3	7, 9-10	§103	Stroud in view of Cragon and Saulsbury
4	4, 8, 15	§103	Stroud in View of DaSilva, Cragon, and Saulsbury

F. Related IPR Matters

Petitioners have also filed three other petitions for *inter partes* reviews on three other patents asserted in the district court action: IPR2025-00223, IPR2025-00478, and IPR2025-00479.

III. CLAIM CONSTRUCTION

Petitioners identify constructions that “were proposed in district court” for four claim terms, but go on to state that “[t]he prior art teaches these terms irrespective of whether these constructions are adopted.” Pet., 14-15. The defects in the Petition’s unpatentability theories explained in this POPR do not hinge on any express constructions and hold true regardless of whether Petitioners’ proposed constructions are adopted. Accordingly, the Board need not engage in express claim construction in determining whether Petitioners have shown a reasonable likelihood

of prevailing as to a challenged claim. *Promptu Sys. Corp. v. Comcast Corp.*, 92 F.4th 1372, 1380 (Fed. Cir. 2024) (“[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.” (*quoting Vivid Technologies, Inc. v. American Science & Engineering, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

IV. PETITIONERS HAVE NOT SHOWN A REASONABLE LIKELIHOOD OF PREVAILING ON ANY CHALLENGED CLAIMS

A. Ground 1 - Stroud in view of DaSilva

- 1. Ground 1 fails because Stroud does not disclose the claimed “packets...having a header with a chassis identifier” and Petitioners’ proposed combination with DaSilva relies upon a fundamental mischaracterization of the references.**

Petitioners’ Ground 1 recognizes that Stroud does not disclose the “packet” that includes “a header with a chassis identifier” required by the claims and instead relies upon DaSilva to supply this missing limitation. Pet. 48-49. Petitioners’ justification for this proposed combination, however, fails at the threshold because it hinges on fundamental mischaracterizations of the prior art.

First, Petitioners distort Stroud’s teachings in asserting that “Stroud teaches” expansion to multiple chassis because it “suggest[s] that various implementations can be ‘distributed across multiple [chassis] devices of 16.’” Pet. 48-49 (brackets in original; citing EX1004, ¶343, Fig. 2E). In fact, Stroud never mentions expansion to

multiple chassis in the cited passage or anywhere else. EX1004, ¶343, Fig. 2E. Paragraph 343 of Stroud merely states that “[t]he hardware devices, software, CLD configuration information, and/or firmware of each respective sub-system may be embodied in a single device of system 16, or distributed across multiple devices of 16, as appropriate.” This merely indicates that system 16 can be embodied in multiple *devices*—*e.g.*, blades or CLDs—not that those devices can be housed in multiple chassis.

To the contrary, every discussion of “chassis” in Stroud refers to a single chassis, and there is no discussion or suggestion of multiple chassis. *See, e.g.*, EX1004, ¶¶ 98, 176, 365, 376 (“As discussed above, system 16 may be housed in a chassis 50 that interconnects multiple cards 54 via a backplane 56.”); 377, 381, 397, 667, 669, 714-15, Fig. 3. This consistent reference to a single chassis (which Stroud makes clear is optional) stands in sharp contrast to Stroud’s express statements as to other system features (such as boards or cards) that one or more can be used. *See* EX1004 ¶714 (“As discussed above, network testing system 16 may comprise *one or more boards or cards* 54 arranged in slots 52 defined by a chassis 50.”). In short, when Stroud contemplated that the claimed system could include more than one of a particular component, it said so.

Further, Petitioners’ claim that “Stroud contemplates ‘creat[ing] larger systems,’” Pet. 50 (brackets in original), omits key context. The full sentence from

which Petitioners selectively quote states as follows: “[a]s discussed above, the components of example architecture 100A may be provided on a single blade 54, and multiple blades 54 may be connected together via backplane 54 to create larger systems.” EX1004, ¶115. In other words, Stroud already disclosed how to create “larger systems” within the confines of the described single-chassis invention—by connecting multiple blades together. There is no suggestion here or anywhere else in Stroud that more than one chassis is needed or desirable.

Instead, Stroud’s disclosure, taken as a whole, teaches away from such an expansion. Stroud repeatedly emphasizes the importance of reducing “complexity” and associated manufacturing operational costs. *See, e.g.*, EX1004, ¶¶664 (explaining how a “conventional [board] access technique” is undesirable because it would require “separate cables for each processor” and thus “may cause increased complexity in the manufacturing setup and/or require operator intervention during the test, each of which may lengthen the test time and incur additional per board costs”); 674 (criticizing architecture that would “add[] further design complexity”); 678 (similar). Adding additional chassis would add complexity to Stroud’s system in multiple ways.

First, Stroud emphasizes “the cards 54 in chassis 50 are *physically connected to each other* via Ethernet over the backplane 56.” EX1004, ¶377. Adding additional chassis would thus not only add cost and complexity by virtue of the new chassis

themselves, it would also require the addition of an entirely new set of physical connections via an entirely new backplane. Second, adding a new “chassis identifier” to every new MAC address would increase the processing complexity of every packet transmission and processing action in Stroud’s system—the opposite of the simplification and efficiency Stroud is attempting to achieve.

Petitioners defend their modification of Stroud on the ground that “[i]t was common to use multiple chassis in data centers.” Pet. 49. But this betrays a fundamental misunderstanding of Stroud’s disclosed system. Stroud is not directed to a data center. Nor is it directed to any system for mass data storage. Instead, it is directed to a discrete, limited system for *testing* the performance of other larger networks. *See, e.g.*, EX1004 ¶80. Nothing in Stroud suggests a need for capacity greater than what could be achieved through the use of multiple cards in a single chassis, and Stroud teaches that the additional complexity such an expansion would necessitate would be contrary to the goals of its system. At base, Petitioners’ assertion that multiple chassis would be obvious because they were known in the art—without any evidence in their alleged prior art—is no more than impermissible hindsight. *See Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 886 (Fed. Cir. 2024) (“It does not suffice to meet the motivation to combine requirement to recognize that [the claimed subject matter was] known in the art.”).

Petitioners’ proposed combination with DaSilva also hinges on a mischaracterization of DaSilva. Petitioners claim that DaSilva “provides teachings for multi-chassis architecture” (Pet. 49) and that it “teaches packets being routed to a particular chassis based on its unique chassis ID.” Pet. 48. Consequently, according to Petitioner, “[a] POSITA looking to add capacity to Stroud would naturally have looked to DaSilva.” Pet. 49.

The clear implication of Petitioners’ argument is that DaSilva teaches multiple physical chassis, and thus it would be a logical expansion of Stroud’s single-chassis system. Putting aside that Stroud teaches away from additional chassis as discussed above, this argument fails because DaSilva is not directed to physical chassis at all. Instead, as noted above, DaSilva is directed to a “a *virtual* chassis system 100 including a plurality of network nodes 110 operably coupled by dedicated link aggregate groups for communicating control and addressing information called virtual fabric links (VFLs) 120.” EX1005, 3:47-51. As DaSilva further explains, “[w]ithin the virtual chassis system 100, a network node 110 is assigned a globally unique identifier called a chassis identifier or chassis ID.” *Id.*, 4:52-54. The “chassis ID” thus simply serves to identify particular “network nodes” within a particular “network topology”—it does not correspond to a physical chassis at all. *Id.*, 5:25-6:35; Fig. 1a.

This “virtual chassis” is an entirely different concept from the chassis disclosed in Stroud. The chassis discussed in Stroud is indisputably a tangible, physical housing for Stroud’s cards and other processing components. For example, Stroud explains how its cards may have “suitable handles, latches, locks, etc.” so they can be inserted into and removed from the chassis. *See, e.g.*, EX1004, ¶714 (“Each card 54 may also include a power button and any suitable handles, latches, locks, etc., for ***inserting, removing, and/or locking card 54 in chassis 50.***”). Further, Stroud explains how its chassis can have “openings” to facilitate heat transfer. *Id.*, ¶715 (discussing how “CLDs 102, processors 105 and 106, and management switch 110 may generate significant amounts of heat that need to be transferred away from system 16, e.g., ***out through openings in chassis 50***”). DaSilva’s “virtual chassis,” in contrast, is merely an arbitrary label applied to a particular network node—it does not correspond in any way to a physical chassis. Accordingly, Petitioners’ assertion that “[t]he references teach similar architectures for similar purposes” (Pet. 49) is flat wrong.

Petitioners’ cursory, conclusory attempt to paper over this fundamental difference between Stroud and DaSilva only underscores the legal insufficiency of its motivation to combine. Reproduced below is the totality of Petitioner’s attempt to reconcile DaSilva’s virtual chassis system with Stroud’s physical one:

Additionally, while the combination does not necessarily rely on virtualization, both references teach it; therefore the inclusion of virtualization—though not needed for Ground 1 or a chassis ID—would not have precluded the combination either. Stroud teaches implementing virtual infrastructure (Ex-1004, ¶84) and using virtual machines (Ex-1004, ¶89). DaSilva teaches a “virtual chassis system” that allowed multiple physical chassis to be grouped together. Ex-1005, 3:64-4:7, 4:23-38. This was compatible because Stroud already contemplated implementing the chassis architecture in a virtual environment. Ex-1003, ¶135.

Pet. 51-52. This stunted discussion of virtualization is rife with defects and inaccuracies.

As an initial matter, Petitioners’ first sentence creates ambiguity as to whether Petitioners are relying on virtualization at all, and highlights the fundamental problem that DaSilva’s exclusive disclosure of virtual chassis poses for the combination. Next, Petitioner’s assertion that Stroud “teaches implementing virtual infrastructure” and “using virtual machines” is deeply misleading. Petitioners cite Stroud’s paragraph 84, but that paragraph only discusses using Stroud’s network testing system as “virtual infrastructure” with respect to the *external network* being tested to, for example, “simulate traffic behavior of network devices.” EX1004, ¶84. There is no disclosure at all of using virtualization *within the internal Ethernet for the network testing system itself*—yet the Petition relies upon Stroud’s internal

Ethernet communications to supply all of the other packet field limitations. *See* Pet. at 41-46 (relying on Stroud’s 6-byte MAC address to supply all of the “identifier” limitations and citing EX1004, ¶¶366-372); EX1004, ¶¶366 (teaching that Stroud’s “6-byte MAC address” is for the “internal Ethernet network of system 16”). Petitioners’ only other cited support for virtualization in Stroud is paragraph 89, but the only disclosure of virtual architecture in that paragraph is again within the *external* data center being tested. EX1004, ¶89. There is simply no teaching whatsoever in Stroud for the use of virtualization with respect to the *internal* Ethernet network of Stroud’s network testing device—the very feature that Petitioners rely upon to supply the packet header “identifier” limitations of claim elements 1[e] and 13[e].

Petitioner’s assertion that “DaSilva teaches a ‘virtual chassis system’ that allowed multiple physical chassis to be grouped together” (Pet. 52) is even more misleading. The portions of DaSilva that Petitioners cite in support of this assertion do not disclose “physical chassis” at all. EX1005, 3:64-4:7, 4:23-38; Pet. 52 (citing same). Instead, the cited passages simply discuss how, in DaSilva’s virtual system, “the plurality of network nodes 110” can “operate as a single virtual network node with unified management capabilities,” such that “the network nodes 110 operate transparently to the external nodes 112 and are treated as a single logical device by the external nodes 112.” EX1005, 3:64-4:7. This does not remotely support the

proposition for which Petitioners' cite it. That Petitioners resorted to inventing a discussion of physical chassis when DaSilva includes nothing of the sort shows that Petitioners understand the weakness of a theory that hinges on applying teachings from a *virtual* chassis system to modify a physical one.

Finally, this is not a case where the mere existence of expert testimony nominally supporting Petitioners' position should change the analysis. Petitioner's expert declaration merely parrots the Petition in many key respects—including on the crucial issue of Stroud and DaSilva's teachings regarding virtualization. *Compare* Pet., 51-52 (“Additionally, while the combination does not necessarily rely on virtualization, both references teach it; therefore the inclusion of virtualization—though not needed for Ground 1 or a chassis ID—would not have precluded the combination either.”) *with* EX1003, ¶135 (“Additionally, while the combination does not necessarily rely on virtualization, both references teach it; therefore the inclusion of virtualization—though not needed for Ground 1—would not have precluded the combination either.”); *compare also* Pet. 31 *with* EX1003, ¶94. Such testimony is entitled to little weight. *See, e.g., Xerox Corp. v. Bytemark, Inc.*, No. IPR2022-00624, 2022 WL 3648989, at *6 (P.T.A.B. Aug. 24, 2022).

For all of the foregoing reasons, the Board should find that the Petition does not present a credible motivation to combine Stroud and DaSilva and thus does not create a reasonable likelihood of prevailing as to Ground 1.

2. Ground 1 fails because Stroud does not disclose the claimed “packets...having a header with a...module identifier.”

Ground 1 fails for another independent reason—Petitioners have not shown that Stroud discloses the “module identifier” required by claim elements 1[e] and 13[e]. Petitioners rely on the “6th Byte” field of Stroud’s six-byte Ethernet MAC address format to address this limitation. *See* Pet. 42-43 (citing EX1004 ¶372). In so doing, however, Petitioners once again overstate Stroud’s disclosure.

Reproduced below is the entirety of Stroud’s paragraph 372:

[0372] 6th Byte: indicates processor interface (each interface to the management switch has its own MAC address).

EX1004 ¶372. And here is how the Petition characterizes that minimal disclosure, relying solely on paragraph 372: “[a]s Stroud explains, ‘each interface to the management switch has its own MAC address’ **because the value for the field in the 6th byte of the MAC address is unique to the module within each card.**” Pet. 43 (citing EX1004 ¶372). As this comparison makes clear, Petitioners simply grafted their own self-serving statement as to what they apparently wish Stroud said (the bolded language above) onto a quote from paragraph 372—creating a misleading impression as to paragraph 372’s contents.

In reality, paragraph 372 says nothing about modules, much less that they have a unique MAC address (or otherwise disclose the “module identifier”). Petitioners effectively acknowledge as much in a footnote, conceding that the cited portion of Stroud mentions only a “‘processor’ interface.” Pet. 43, n.6. Petitioners next contend that “Stroud’s teachings are not limited to just the network processors because controllers, NPs, and CLDs all have an interface to the management switch, which uses the unique interface identifier—and therefore unique MAC address—to route packets to them.” *Id.* (internal citations omitted). But even if that is true, Petitioners still have not shown how the 6th byte is a “**module** identifier,” which is what the claim requires.

Implicitly, Petitioners appear to be equating each processor, NP, and CLD with a distinct module, but that is directly contrary to Stroud’s teachings, which emphasize that modules may comprise multiple CLDs and that a single CLD may contribute to multiple modules. *See, e.g.,* EX1004 ¶405 (“However, it should be clear that each of these modules may be implemented...across both CLD 102A and CLD 102B (e.g., a particular module may include certain logic in CLD 102A for providing certain functionality associated with that module, and certain other logic in CLD 102B for providing certain other functionality associated with that module.”). Thus even if Stroud’s “6th Byte” does identify specific “controllers, NPs, and CLDs” as Petitioners claim, ***this would still be insufficient to identify particular***

modules in Stroud, since Stroud teaches that modules can include multiple CLDs (and other components) and CLDs and other processors can contribute functionality to multiple modules.

In sum, nothing in Stroud indicates that the 6th byte in its internal Ethernet MAC format identifies a module. Petitioner’s arguments otherwise hinge on adding language to the reference that is not there, and on equating modules with hardware components, even though Stroud expressly teaches that they are not coextensive. The Board should find that Petitioners have failed to establish a reasonable likelihood that Stroud discloses this limitation and—since Petitioners have no alternate theory for supplying this limitation—that this is an independent basis for rejecting Ground 1.

B. Ground 2 – Stroud in view of Cragon

1. Ground 2 fails because Cragon does not teach Claim 7’s “selectable arrangement” of “types of memory”.

As noted above, the Petition relies on Cragon to supply the “selectable arrangement” of “types of memory” required by claim element 7[d], in addition to the specific types of memory enumerated in the claim. Pet. 73-78. The cited portions of Cragon, however, disclose nothing of the sort.

The Petition cites to pages 536-548 of Cragon as allegedly disclosing a “selectable arrangement of the plurality of types of memory” required by the claims.

Pet. 73. But the cited portions of Cragon provide nothing approaching the claimed selectable arrangement.

The cited portion of Cragon begins by stating that “[t]here is very little solid information published on the question of the disk bandwidth and storage requirements based upon workloads.” EX1006, 000536. This affirmatively undermines Petitioners’ contention that the claimed selectable arrangement is disclosed by Cragon or otherwise known in the art. Cragon then proceeds to provide a high-level, conversational overview of “[f]ive parameters [that] are commonly used to characterize a disk system.” *Id.* The identified parameters are reproduced below, as presented in Cragon:

Five parameters are commonly used to characterize a disk system.

1. Capacity. Bytes of storage (formatted).
2. Bandwidth. Bytes transferred/unit of time.
3. Service rate. Number of service requests satisfied/unit of time.
4. Response time. Time between the start and completion of an event.
5. Cost. \$/Mbyte.

Id.

At no point in the pages that follow does Cragon even remotely suggest a selectable arrangement of memory types based on these parameters as Petitioners

contend (Pet. 74). Indeed, it is unclear how generalized design considerations like “cost” can even be converted into a selectable arrangement of memory types; the Petition certainly provides no such explanation.

Instead, Cragon provides a generalized discussion of how these abstract parameters can play a role in disk system design. EX1006, 000536-548. Nothing in this highly generalized discussion of various design considerations is a disclosure of the “selectable arrangement” required by the claims. Petitioners apparently recognize as much, as evidenced by their inclusion of a backup theory for this limitation in Ground 3. As discussed below, however, Ground 3 fails to cure the defects in Ground 2 and thus fails as well.

2. Ground 2 also fails because Cragon does not disclose the claimed “memory allocated to specified address ranges according to parameterized task needs.”

Relying on the same portions of Cragon that Petitioners (incorrectly) claim disclose the “selectable arrangement” limitation, Petitioners also contend that “Cragon teaches allocating memory to a task according to parameterized task needs.” Pet. 78 (citing EX1006, 000536). Once again, this generalized high-level disclosure in Cragon fails to disclose the claimed feature.

Petitioners cite Cragon’s teachings regarding “five commonly-used parameters” and alleges that “[f]or each parameter, Cragon provides examples of different tasks and their differing requirements.” Pet. 78. As discussed above, that

characterization grossly overstates Cragon’s high-level disclosure. Indeed, it is not clear what it would mean to provide a “task” associated with a “cost” parameter and Petitioners never attempt such an explanation. Further, even if Petitioners statement were true (it is not) the claims are not directed to “examples of different tasks,” they require “memory allocated to specified address ranges according to parameterized task needs.” Nothing in the cited pages (which Petitioners cite broadly in large chunks, without specific examples) discloses any such allocation to a specific range in accordance with a parameterized task need.

C. Ground 3 – Stroud in view of Cragon and Saulsbury

As noted above, in apparent recognition of the weaknesses of the Stroud/Cragon combination, Petitioners adds a backup ground that relies on Saulsbury to supply the “selectable arrangement” limitation of claim 7. This ground fails as well.

Petitioners rely on Saulsbury solely for its disclosure of “*switch[ing] the memory mode* between physical memory and cache memory, depending on the particular application of the processor and memory chip.” Pet. 85 (emphasis and brackets in original; citing EX1007 ¶¶3, 65, Fig. 1). But this mere disclosure of switching between physical and cache memory is not a disclosure of the selectable arrangement of a plurality of memory types required by the claims. Further, Saulsbury does nothing to cure Cragon’s failure to disclose the claimed “memory

allocated to specified address ranges according to parameterized task needs” discussed above. Accordingly, Petitioners have not shown a reasonable likelihood of prevailing even as to the backup theory in Ground 3.

D. Ground 4 - Stroud in View of DaSilva, Cragon, and Saulsbury

The Petition explains that “Ground 4 combines the teachings from Ground 1 (which addressed the packet header of claim 1) with Ground 3 (which addressed the memory limitations of claim 7).” Pet. 93. Petitioners further state that Ground 4 relies upon the “same motivation” to combine as those grounds. Pet. 94. Accordingly, Petitioners have not shown a reasonable likelihood of prevailing as to Ground 4 for all of the reasons set forth above with respect to Grounds 1 and 3.

V. CONCLUSION

For the foregoing reasons, to the extent the Director does not discretionarily deny the Petition and the Board reaches the merits, the Board should deny institution of the requested IPR.

Dated: July 7, 2025

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*Counsel for Patent Owners
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CERTIFICATE OF COMPLIANCE

The undersigned hereby certifies that CV/XE's Patent Owners' Preliminary Response to the Petition for IPR consists of 5,218 words, excluding the table of contents, table of authorities, certificate of service, this certificate of compliance, or table of exhibits. This Patent Owners' Preliminary Response to the Petition for IPR complies with the type-volume limitation of 14,000 words as mandated by the Memo. In preparing this certificate, counsel has relied on the word count of the word processing system used to prepare this paper (Microsoft Word).

Dated: July 7, 2025

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that pursuant to 37 C.F.R. §42.6(e)(1), a copy of the foregoing **CV/XE's Patent Owners' Preliminary Response to the Petition for IPR** was served on July 7, 2025 by filing this document through the Patent Trial and Appeal Board's P-TACTS System as well as delivering a copy via electronic mail upon the following attorneys of record for Petitioners:

Dated: July 7, 2025

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