

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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ADVANCED MICRO DEVICES, INC. and  
PENSANDO SYSTEMS, INC.,  
Petitioner,

v.

XTREAMEDGE, INC.,  
Patent Owner.

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IPR2025-00486  
Patent 10,873,753 B1

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Before KARL D. EASTHOM, JUSTIN T. ARBES, and  
IFTIKHAR AHMED, *Administrative Patent Judges*.

EASTHOM, *Administrative Patent Judge*.

DECISION  
Granting Institution of *Inter Partes* Review  
35 U.S.C. § 314

## I. INTRODUCTION

Advanced Micro Devices, Inc. and Pensando Systems, Inc., Petitioner, filed a Petition (Paper 2, “Pet.”) requesting an *inter partes* review of claims 1–4, 7–10, and 13–15 (the “challenged claims”) of U.S. Patent No. 10,873,753 B1 (Ex. 1001, the “753 patent”). *See* Pet. 16. XstreamEdge, Inc., Patent Owner, filed a Preliminary Response. Paper 7 (“Prelim. Resp.”).<sup>1</sup>

An *inter partes* review may not be instituted unless the information presented in the petition and preliminary response shows that “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a).

For the reasons explained below, we determine that Petitioner establishes a reasonable likelihood that it would prevail with respect to at least one challenged claim. Accordingly, we institute an *inter partes* review as to the challenged claims and the grounds raised in the Petition.

## II. BACKGROUND

### A. *Real Parties in Interest*

Each party identifies itself as the real party in interest. Pet. 96; Paper 3, 2. Patent Owner also notes that “Concurrent Ventures, LLC is the exclusive licensee to U.S. Patent No. 10,873,753 and has all substantial rights to U.S. Patent No. 10,873,753.” Paper 3, 2.

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<sup>1</sup> The parties also filed briefing directed to discretionary denial issues pursuant to the Board’s bi-furcated process, and the Director referred the institution decision to the Board. *See* Papers 6, 8–10.

*B. Related Matters*

The parties identify *Concurrent Ventures, LLC v. Advanced Micro Devices, Inc.*, No. 1-24-cv-00335 (W.D. Tex.) as a related matter. Pet. 95–96; Paper 3, 2; Paper 6, 4. Patent Owner identifies IPR2025-00223, IPR2025-00478, and IPR2025-00479 as involving “three other patents asserted in the district court action.” Prelim. Resp. 10.

*C. The '753 Patent*

The '753 patent relates to a “platform for data flow processing.” Ex. 1001, code (57). The platform includes “one or more swappable pods or cards in one or more chassis, coupled through a module messaging interface network.” *Id.* Each swappable pod or card includes “one or more hardware modules or one or more software modules and one or more of the plurality of swappable pods or cards having a portion for user-definable hardware modules or user definable software modules.” *Id.* The swappable pods or cards are “user-configurable to implement data flow processing architectures.” *Id.*

*D. Illustrative Claim*

Independent claim 1 is illustrative of the challenged claims, and follows:

[1pre]. A platform for data flow processing, comprising:

[1a] one or more swappable pods or cards in one or more chassis, coupled through a messaging interface network;

[1b] each of the one or more swappable pods or cards having one or more hardware modules or one or more software modules;

[1c] one or more of the plurality of swappable pods or cards having a portion for user-definable hardware modules or user-definable software modules;

[1d] the plurality of swappable pods or cards being user-configurable to implement data flow processing architectures; and

[1e] a network coupled to the one or more swappable pods or cards and supporting messaging-based communication using packets each having a header with a chassis identifier, a board identifier, a module identifier, an instance identifier, and a type identifier, so that each type of module, each instance of a type of module, and each module on each board in each chassis can be addressed through the header.

Pet. 98 (alteration in original).

*E. Asserted Grounds of Unpatentability*

Petitioner contends that the challenged claims are unpatentable as follows:<sup>2</sup>

| <b>Claim(s)<br/>Challenged</b> | <b>35 U.S.C.<br/>§</b> | <b>Reference(s)/Basis</b>                 |
|--------------------------------|------------------------|-------------------------------------------|
| 1–4, 13, 14                    | 103                    | Stroud, <sup>3</sup> DaSilva <sup>4</sup> |
| 7, 9, 10                       | 103                    | Stroud, Cragon <sup>5</sup>               |
| 7, 9, 10                       | 103                    | Stroud, Cragon, Saulsbury <sup>6</sup>    |
| 4, 8, 15                       | 103                    | Stroud, DaSilva, Cragon, Saulsbury        |

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<sup>2</sup> The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102, 103 effective March 16, 2013, which is before the ’753 patent’s effective filing date. *See* Ex. 1001, code (22) (filing date July 15, 2018); Pet. 13 (referring to July 15, 2018). Therefore, the AIA version of § 103 applies.

<sup>3</sup> Stroud et al., US 2013/0346667 A1, published Dec. 26, 2013. Ex. 1004.

<sup>4</sup> DaSilva et al., US 9,148,389 B2, issued Sept. 29, 2015. Ex. 1005.

<sup>5</sup> Harvey G. Cragon, MEMORY SYSTEMS AND PIPELINED PROCESSORS (1996). Ex. 1006.

<sup>6</sup> Saulsbury et al., US 2002/0087821 A1, published July 4, 2002. Ex. 1007.

Pet. 16. Petitioner supports its Petition with the Declaration of Donald Alpert, Ph.D. Ex. 1003.

### III. ANALYSIS OF PETITIONER'S CHALLENGES

#### A. *The Obviousness Standard*

Section 103(a) forbids issuance of a patent when “the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.”

*KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007).<sup>7</sup> The obviousness question involves resolving underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and when presented (not here), (4) objective evidence of non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

#### B. *Level of Ordinary Skill in the Art*

Determining whether an invention would have been obvious under 35 U.S.C. § 103 requires resolving the level of ordinary skill in the pertinent art at the time of the effective filing date of the claimed invention. *Graham*, 383 U.S. at 17. The person of ordinary skill in the art is a hypothetical person who knows the relevant art. *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995). Factors in determining the level of ordinary skill in the art include the types of problems encountered in the art, the sophistication of the

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<sup>7</sup> Section 103(a) is materially similar to the AIA version of Section 103 for purposes of this trial.

technology, and educational level of active workers in the field. *Id.* One or more factors may predominate. *Id.*

Petitioner contends that a person of ordinary skill in the art (POSITA), would have been a person with a bachelor's degree in electrical engineering, computer engineering, or similar major with at least two years of experience in the field [of data processing and streaming architectures including user-defined hardware and software modules] or a master's degree in electrical engineering, computer engineering, or similar major with specialization in the field. A person with less education but more relevant practical experience may also meet this standard.

Pet. 13 (citing Ex. 1001, 1:6–21, 2:47–3:20, codes (54), (57); Ex. 1003 ¶¶ 35–37). Patent Owner does not provide a level of ordinary skill in the art. *See generally* Prelim. Resp.

Based on a review of the record, we adopt Petitioner's proposed level of ordinary skill in the art because it is consistent with the evidence of record, including the asserted prior art and '753 patent specification.

### C. *Claim Construction*

In *inter partes* reviews, the Board interprets claim language using the district-court-type standard, as described in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2024). Under this standard, claim terms have their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history. *See Phillips*, 415 F.3d at 1313–14.

Petitioner proposes constructions for four terms (as recited in claims 4, 7, and 15):

1. “memory superposition” as meaning “two or more types of memory that can be made available for a data flow or other data processing operation.” Pet. 15 (citing Ex. 1001, 7:1–9 (“For memory superposition 140, two or more types of memory, such as SRAM (static random access memory) 144, DRAM (dynamic random access memory) 146, FRAM (ferroelectric random-access memory) 148, RLDRAM (reduced latency dynamic random random-access memory) 150, flash 152 (electrically erasable programmable read-only memory or EPROM), 3D Xpoint, etc., are made available for a data flow or other data processing operation.”)); Ex. 1003 ¶ 41; Ex. 1036 (Patent Owner’s District Court preliminary proposal), 3).

2. “interleaved memory” as meaning “an arrangement of different types of memory that are alternately [capable of being] accessed to achieve an average access bandwidth.” Pet. 15. (citing Ex. 1001, 7:1–9, 8:35–40; Ex. 1003 ¶¶ 43–45).

3. “swapped memory over a specified address range” as meaning “memory with a specified address range where information is [capable of being] moved between the memory and non-volatile storage.” Pet. 15–16 (citing Ex. 1003 ¶¶ 49–50; Ex. 1038, 3; Ex. 1039, 3).

4. “memory allocated to specified address ranges according to parameterized task needs” as meaning “different types of memory allocated to specified address ranges according to parameters for task needs.” Pet. 16 (citing Ex. 1001, 7:1–9, 7:21–8:31; Ex. 1003 ¶¶ 52–56).

Patent Owner contends that “the Board need not engage in express claim construction” because “defects in the Petition’s unpatentability

theories explained in this [Preliminary Response] do not hinge on any express constructions.” Prelim. Resp. 10.

The preliminary record supports Petitioner’s proposals (as slightly modified by the panel as indicated via the bracketed information) for purposes of institution.

5. Claim 1 recites a “chassis identifier” and “one or more chassis.” Therefore, claim 1 does not require multiple chassis. The parties do not address whether a “chassis identifier” represents nonfunctional descriptive material when there is “one . . . chassis.” That is, claim 1 requires that “each module on each board in each chassis can be addressed through the header,” but it appears on this preliminary record that “each module . . . can be addressed through the header” regardless of the information conveyed by the “chassis identifier” when there is only “one . . . chassis.” The Board welcomes input on this claim construction issue during trial.

No other express construction of any claim term is necessary to determine whether to institute *inter partes* review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

*D. Ground 1, Alleged Obviousness of Claims 1–3, 13, and 14 over Stroud and DaSilva*

Petitioner contends that claims 1–3, 13, and 14 would have been obvious over the combined teachings of Stroud and DaSilva. Pet. 17–53.

1. *Stroud*

Stroud’s “[n]etwork testing system 16 may include a chassis 50 including any suitable number of slots 52, each configured to receive a modular card, or blade, 54.” Ex. 1004 ¶ 98; *accord id.* ¶ 176.

Stroud’s Figure 3 follows:

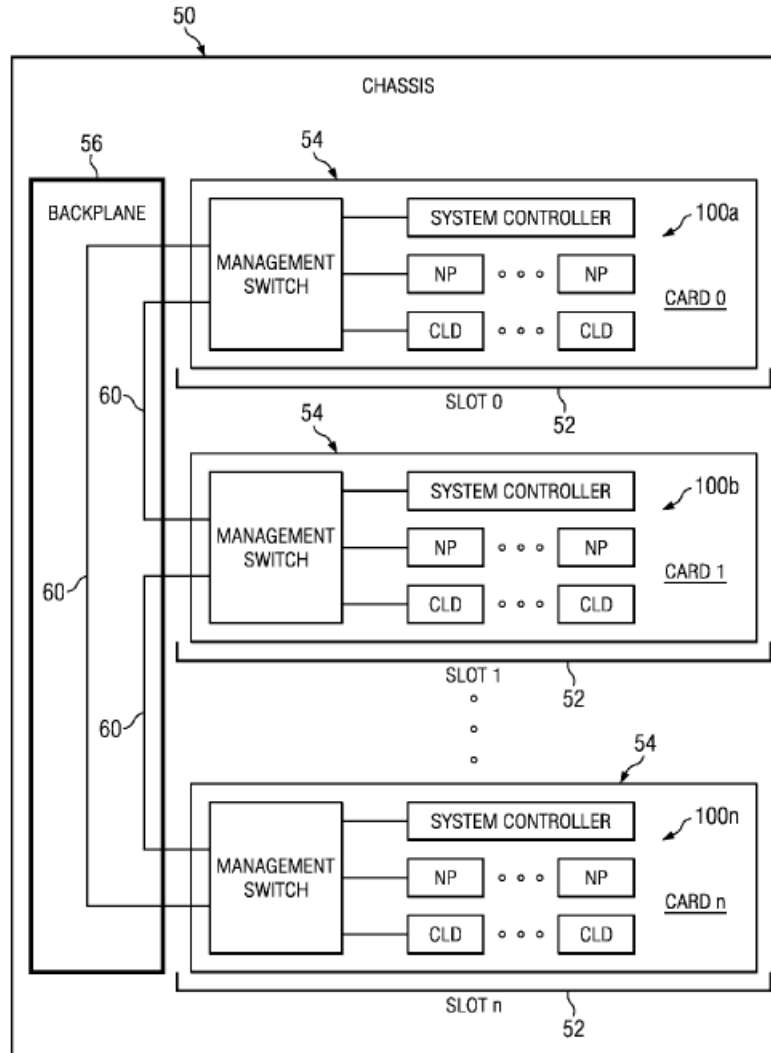


FIG. 3

Stroud’s Figure 3 above illustrates network testing system 16 comprising chassis 50 slots 52 holding cards/blades 54 with management switches connecting devices on the cards/blades together via backplane 56. Ex. 1004 ¶ 101. “Each card 54 may be plugged into a backplane 56, which may

include physical connections 60 for communicatively connecting cards 54 to each other. . . .” *Id.* ¶ 99. Each card 54 “may include any architecture 100 of hardware, software, and/or firmware components for providing the functionality of network testing system 16.” *Id.* ¶ 100. Each card’s system architecture “may include a system controller, one or more network processors, and one or more [configurable logic devices (CLDs)] connected to a management switch 110 (and any other suitable components, e.g., memory devices, communication interfaces, etc.).” *Id.* ¶ 101.

## 2. *DaSilva*

DaSilva describes virtual chassis system 100 with network nodes 110, with each node having “one or more different types of node architectures, such as single module, stackable, or multi-slot chassis-based architectures.” Ex. 1005, 7:52–55. DaSilva’s “network nodes 110 [are] in a virtual chassis system 100” as they are capable of “coupl[ing] in any of a plurality of types of network topologies without affecting operation of the virtual chassis system 100.” *Id.* at 5:26–29 (emphasis added).

## 3. *Analysis of Claim 1*

### a) *Preamble and Limitations 1a–1d*

For independent claim 1’s preamble, “[a] platform for data flow processing, comprising,” Petitioner relies on Stroud’s network testing system 16 (Ex. 1004 ¶¶ 85–87), which processes and tests data flows from devices 14 in network 12 (*id.* ¶ 80). Pet. 21 (citing Ex. 1004 ¶¶ 80–81, 84–87, 89–93, 298, Fig. 1). Petitioner contends that the testing platform processes packet data flowing in the network. *Id.* (citing Ex. 1004 ¶¶ 84, 86, 89–93, 298; Ex. 1003 ¶¶ 72–73).

For limitation 1a, “one or more swappable pods or cards in one or more chassis, coupled through a messaging interface network,” Petitioner relies on Stroud’s chassis 50, which receives multiple modular cards or blades. Pet. 22 (citing Ex. 1004 ¶¶ 98 (“Network testing system 16 may include a chassis 50 including any suitable number of slots 52, each configured to receive a modular card, or blade, 54”), 376 (“[S]ystem 16 may be housed in a chassis 50 that interconnects multiple cards 54 via a backplane 56.”). Petitioner also cites Stroud’s “hot-swapped” cards 54 (Ex. 1004 ¶ 382), swappable in chassis slots (*id.* ¶ 98), where testing system 16 is “configured to support any suitable number of cards” (*id.* ¶ 176). *See* Pet. 24 (citing Ex. 1004 ¶¶ 98, 176, 378, 382, 714; Ex. 1003 ¶ 78).

Petitioner explains that “[t]he cards/blades comprise one or more circuit boards,” and “[e]ach blade is a module that comprises a large card.” Pet. 23 (citing Ex. 1004 ¶¶ 98, 115, 176, 382, Figs. 54–57B). Petitioner also explains that “the cards are connected to each other through an Ethernet network that goes through physical backplane interfaces.” *Id.* at 24 (citing Ex. 1004 ¶¶ 101 (“Cards 54 may be communicatively coupled to each other via the backplane 56 and management switches 110 of the respective cards 54, as shown in Fig. 3.”), 99, 113–115, 176, 353–354, 376–378, 382, 393). Petitioner further explains that each card contains “management switch” 110 connected to an interface on the backplane so that the chassis cards are “communicatively coupled to each other via the backplane 56” (Ex. 1004 ¶ 101). Pet. 25 (citing Ex. 1004 ¶¶ 101, 113, 114, 314–319, Figs. 4–5; Ex. 1043, 2:10–35; Ex. 1044, 1–3, 8; Ex. 1003 ¶ 81).

For limitation 1b, “each of the one or more swappable pods or cards having one or more hardware modules or one or more software modules,”

Petitioner relies on Stroud’s “controller 106, two network processors 105 and multiple CLDs 102 coupled to a management switch 110,” which are on each swappable card or pod. Pet. 26 (citing Ex. 1004 ¶¶ 103–113, 114, 456–459, Figs. 3–5, 14A–14B). Petitioner explains that Stroud’s configurable logic devices (CLDs) are programmable logic hardware modules such as “programmable logic devices (PLDs)” and “FPGAs” (field programmable gate arrays). *Id.* at 28 (quoting Ex. 1004 ¶ 107; citing Ex. 1004 ¶¶ 110–112, 311–313).

Petitioner further explains that Stroud’s “application software . . . executed on network processor” NP 105 on each card is a software module. *Id.* at 29 (quoting Ex. 1004 ¶ 309; citing Ex. 1004 ¶¶ 105, 219, 224, 464; Ex. 1003 ¶¶ 88–89). Petitioner also relies on “management processor 134 of controller 106 configured to execute controller software 132” and other software run by management processor 134. *Id.* (quoting Ex. 1004 ¶ 188; citing Ex. 1004 ¶¶ 208, 227, 262 (describing “management processor 134 on controller 106 configured to execute the controller software 132, collect and store statistics, and/or generate malicious application traffic”), 263 (describing “the management processor 134 of controller 106 can generate malicious traffic packet-by-packet and forward these to the network processor 105 as if they were generated locally”), 266 (describing “management processor 134 of controller 106, in addition to providing a place for much of the control software for various subsystems to execute, may also host a statistics database 160 and reporting engine 162”).

For limitation 1c, “one or more of the plurality of swappable pods or cards having a portion for user-definable hardware modules or user-definable software modules,” Petitioner relies on the “portion of Stroud’s

card that contains CLDs, NPs, and/or a controller.” Pet. 32 (citing Ex. 1004 ¶ 717, Figs. 3–4; Ex. 1003 ¶ 95).

For limitation 1d, “the plurality of swappable pods or cards being user-configurable to implement data flow processing architectures,” Petitioner relies on its showing above with respect to the cards including user-configurable CLDs (configurable logic devices), which include FPGAs (field programmable gate arrays), and software stored in a hard disk attached to the card. Pet. 36–37 (citing Ex. 1004 ¶¶ 105, 144, 149–153, 158, 170–173, 188, 208, 219, 220, 223, 234, 227–229, 234, 262, 263, 266, 309, 464, Figs. 3–5, 14A–14B). Petitioner contends that “the user configures the overall function of the card and the way in which the hardware and software modules work together to perform the user’s application.” *Id.* at 37 (citing Ex. 1004 ¶ 84 (“e.g., database server, Web server”), ¶¶ 89–93; Ex. 1003 ¶¶ 104, 105). Petitioner explains that

Stroud configures its cards to implement several data flow processing architectures that process packetized data flows by, for example, capturing packets, generating and measuring packets, simulating and measuring network traffic at the application level, analyzing security in network data flows, simulating security exploits in packet traffic, and processing data flows to collect and report statistics of the data flow.

*Id.* at 38 (citing Ex. 1004 ¶ 177; Ex. 1003 ¶ 107).

Patent Owner does not address Petitioner’s showing for the preamble and limitations 1a–1d. *See generally* Prelim. Resp. On this preliminary record, Petitioner’s showing, as summarized above, is sufficient for purposes of institution.

*b) Limitation 1e*

For limitation 1.e,

a network coupled to the one or more swappable pods or cards and supporting messaging-based communication using packets each having a header with a chassis identifier, a board identifier, a module identifier, an instance identifier, and a type identifier, so that each type of module, each instance of a type of module, and each module on each board in each chassis can be addressed through the header,

Petitioner relies on the combined teachings of Stroud and DaSilva. Pet. 39–52.

*(i) Board, Instant, Type Identifiers*

Petitioner contends that Stroud’s packet headers include the following claimed header fields recited in limitation 1e: “a board identifier, a module identifier, an instance identifier, and a type identifier.” Pet. 41–46.

For the recited “board identifier,” Petitioner relies on Stroud’s board slot ID within a destination MAC address of a packet header. Pet. 41 (citing Ex. 1004 ¶¶ 347 (“Sub-fields within the destination MAC address (6 bytes total in length) identify the CLD type, an CLD index and a board slot ID.”), 370 (“4th Byte: indicates slot number”)). Petitioner contends that “[t]his distinct sub-field identifies a particular board, which resides in a particular slot in a chassis.” *Id.* (citing Ex. 1004 ¶¶ 98, 344).

For the recited “instance identifier,” Petitioner relies on Stroud’s header sub-field for a “processor or CLD number” that is used “to *distinguish between multiple instances* of the same type of processor or CLD on the same card.” Pet. 45 (quoting Ex. 1004 ¶ 371) (emphasis in original).

For the recited “type identifier,” Petitioner relies on Stroud’s header sub-field for “chip type: e.g., processor, CLD, or other type of device.” Pet.

46 (quoting Ex. 1004 ¶ 368; citing Ex. 1003 ¶ 121). Petitioner explains that “[w]hen there are multiple instances of the same type of NP/CLD on a card, the processor or CLD number identifies the unique instance of the CLD or processor on that card.” *Id.* at 45–46 (citing Ex. 1003 ¶ 120).

Patent Owner does not address Petitioner’s showing for the above-noted header sub-field identifiers in limitation 1e. *See generally* Prelim. Resp. On this preliminary record, Petitioner’s showing as to these aspects of limitation 1e, as summarized above, is sufficient for purposes of institution.

*(ii) Module Identifier*

For limitation 1e’s “header with . . . a module identifier, so that each type of module, each instance of a type of module, and each module on each board in each chassis can be addressed through the header,” Petitioner relies on Stroud’s “sub-field for an ‘interface’ identifier that identifies modules by their interface to the management switch.” Pet 42–43 (citing Ex. 1004 ¶ 372). As indicated above in the discussion of limitations 1b and 1c, Petitioner contends that “Stroud’s card includes a number of controller, NP, and CLD modules; each is connected to the management switch.” *Id.* at 43 (citing Ex. 1004 ¶¶ 101, 103, 113, 174, 176, 189, 314, Figs. 3–5).

Petitioner relies on Stroud’s description that “‘each interface to the management switch has its own MAC address’ because the value for the field in the 6th byte of the MAC address is unique to the module within each card.” Pet. 43 (quoting Ex. 1004 ¶ 372). Therefore, Petitioner asserts that “the interface identifier in the 6th byte [of the header] identifies each module on a card (e.g., each controller, NP, or CLD[]) by its interface to the management switch.” *Id.* (citing Ex. 1004 ¶¶ 100, 372). Petitioner explains further as follows:

Stroud's interface identifier is assigned to the controller, NP, and CLD modules. Each interface has its own unique identifier. Ex-1004, ¶372. While Stroud refers to the "processor" interface (*id.*), Stroud's teachings are not limited to just the network processors because controllers, NPs, and CLDs all have an interface to the management switch (*id.*, Figs. 4–5, 7A–8A), which uses the unique interface identifier—and therefore unique MAC address—to route packets to them.

Pet. 43 n.6 (citing Ex. 1004 ¶¶ 354, 356).

Patent Owner disputes that Stroud's switch interface address is unique to a module within each card. Prelim. Resp. 20–21 (citing Ex. 1004 ¶ 372). Patent Owner contends that Stroud's "paragraph 372 says nothing about modules, much less that they have a unique MAC address (or otherwise disclose the 'module identifier')." *Id.* at 21. Patent Owner contends that "even if [i]t is true" that Stroud's "controllers, NPs, and CLDs all have an interface to the management switch, which uses the unique interface identifier—and therefore unique MAC address—to route packets to them," "[i]t is directly contrary to Stroud's teachings" to "equat[e] each processor, NP, and CLD with a distinct module." *Id.* (citing Ex. 1004 ¶ 405 ("[I]t should be clear that each of these modules may be implemented . . . across both CLD 102A and CLD 102B (e.g., a particular module may include certain logic in CLD 102A for providing certain functionality associated with that module, and certain other logic in CLD 102B for providing certain other functionality associated with that module.")). Patent Owner contends that Stroud's 6<sup>th</sup> Byte is "insufficient to identify particular modules in Stroud, since Stroud teaches that modules can include multiple CLDs (and other components) and CLDs and other processors can contribute functionality to multiple modules." *Id.* at 21–22 (emphasis omitted).

These arguments are unavailing to undermine Petitioner’s showing. Even if Stroud discloses that one “may” combine different CLDs to include different functionality in some embodiments, this does not address, much less undermine, Petitioner’s reliance on the identified CLD and processor (e.g., NP) modules as distinct devices with a distinct connection to Ethernet switch 110 interface with a corresponding address for each connected device. *See* Pet. 43 n.6 (citing Ex. 1004 ¶¶ 354, 356); Ex. 1004 ¶¶ 353–356, Fig. 5. Claim 1 is broad enough to encompass one or more hardware modules without one or more software modules. Petitioner sufficiently reads the claimed hardware modules onto CLDs, with at least one connected directly to Stroud’s network switch. *See* Pet. 27–28 (annotating Ex. 1004, Fig. 3). Petitioner also sufficiently reads the alternatively claimed software modules onto NPs running software, with NPs connected directly to Stroud’s network switch. *See id.* at 27–32 (annotating Ex. 1004, Figs. 3–5).

*(iii) Chassis Identifier*

For limitation 1e’s packet header subfield “chassis identifier,” Petitioner generally relies on Stroud’s “chassis with multiple cards that communicate using Ethernet with packet header identifiers,” and DaSilva’s “improvement for networks with multiple chassis, where packet headers include a ‘chassis ID’ to indicate a particular chassis.” Pet. 17 (citing Ex. 1003 ¶¶ 58–59; Ex. 1004 ¶¶ 367–372; Ex. 1005, 4:23–5:24).

As discussed in more particular below, Petitioner generally contends that in view of Stroud’s disclosure of larger networks and packet headers, DaSilva’s multiple-chassis and packet headers, and known multi-chassis data processing networks, it would have been obvious to add multiple chassis in Stroud’s test system with corresponding chassis IDs in Stroud’s

packet header in order to expand Stroud’s testing network capacity via communication with the multiple chassis. *See* Pet. 48–53. That is, Petitioner contends it would have been obvious to include DaSilva’s packet header sub-field “chassis ID” in Stroud’s packet header as a distinct sub-field in order to expand Stroud’s data processing capacity and distinguish between multiple chassis for packet communication therewith. *Id.* at 47–48.

Petitioner explains that Stroud’s network cards use Ethernet packets to communicate via a management switch on each card to the network. Pet. 39 (citing Ex. 1004 ¶¶ 119, 121, 174, 181, 236, 242, 345–347). Petitioner relies on Stroud’s Ethernet packet headers with different fields for routing packets. *See id.* at 40 (citing Ex. 1004 ¶¶ 349 (“The first portion of the packet is the IEEE standard header for Ethernet packets, including the destination MAC address, the source MAC address, and the Ethernet packet type field.”), 124 (describing “the packet’s layer 2/3/4 headers”)).

Petitioner also notes that Stroud’s “management switch 110 may essentially act as a router” (Ex. 1004 ¶ 314) to communicate with internal and external destinations of each card. *Id.* (citing Ex. 1004 ¶¶ 113–115, 365, 413–426, Figs. 3, 12, 31; Ex. 1003 ¶¶ 110–111).

Petitioner provides DaSilva’s Figure 6, which follows (Pet. 47):

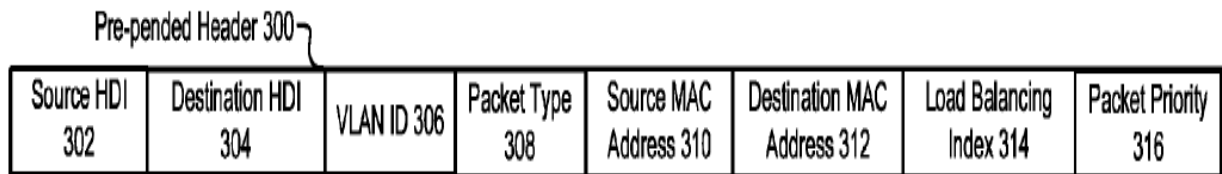
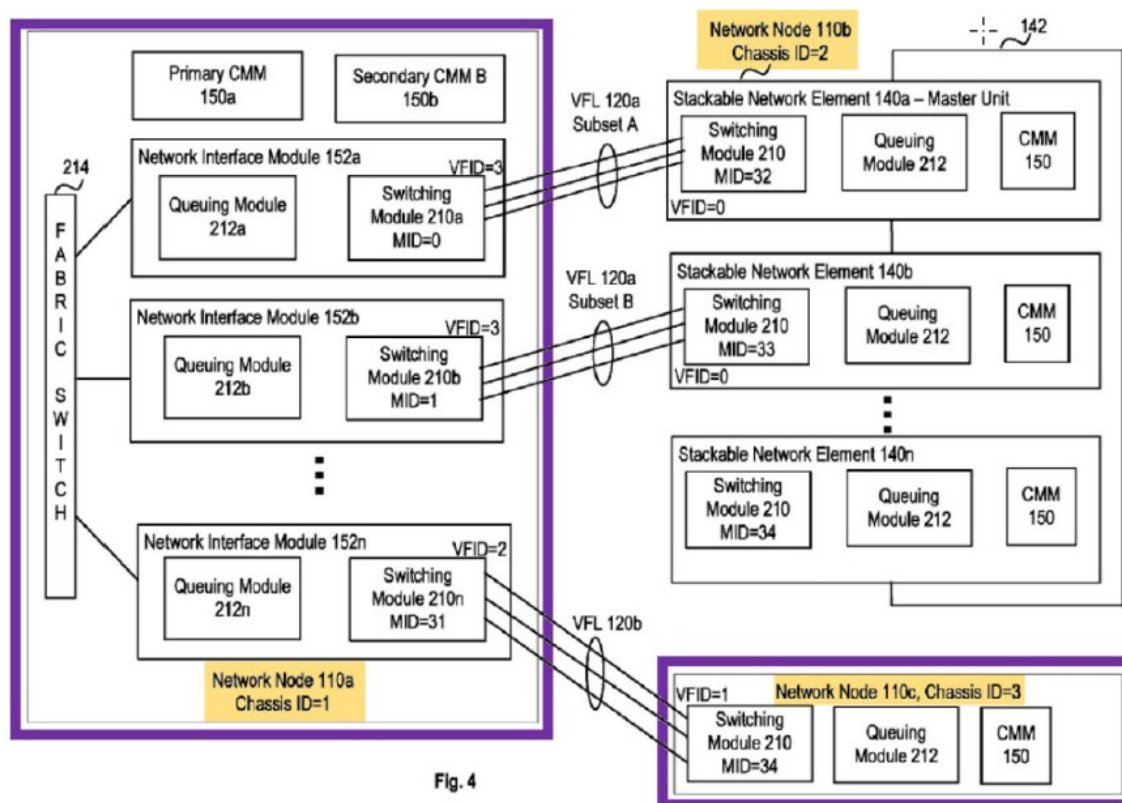


Fig. 6

DaSilva’s Figure 6 above illustrates Destination HDI (hardware device information) as part 304 of a packet header. Petitioner contends that DaSilva teaches that a “chassis ID” is part of the Destination HDI. *See* Pet.

47 (citing Ex. 1005, 9:58–10:14 (describing “add[ing] a pre-pended header (or otherwise modify[ing]) the packet header to include hardware device information (HDI) associated with the source and/or destination address of the packet” wherein “[t]he hardware device information includes . . . chassis ID”), 5:13–18 (“network nodes 110 exchange packets with pre-pended headers . . . such as source chassis ID”), Fig. 6 (Destination HDI).

Petitioner also provides an annotated version of DaSilva’s Figure 4, which follows (Pet. 47):



DaSilva’s Figure 4 above shows three network nodes 110a, b, and c identified by Chassis ID=1, Chassis ID=2, and Chassis ID=3, respectively (and highlighted in yellow by Petitioner). These nodes are “in a virtual chassis system 100 with different types of node architectures.” Ex. 1005, 7:56–58. “[N]etwork node 110a has a multi-slot *chassis-based* architecture

with a plurality of network interface modules 152a–n.” *Id.* at 7:58–60 (emphasis added). “The network interface modules 152n include a queuing module 212 and switching module 210 and are connected by a fabric switch 214 integrated *into the back-plane of the chassis.*” *Id.* at 7:64–67 (emphasis added). “Network node 110c has a single module node architecture, such as a single stackable element 140 or alternatively, *a multi-slot chassis-based architecture with a single network interface module 152.*” *Id.* at 8:23–26 (emphasis added).

Petitioner explains that “DaSilva teaches packets being routed to a particular chassis based on its unique chassis ID.” Pet. 48 (citing Ex. 1005, 4:53–54, 9:1–5 (stating the “chassis ID for each network node 110 is unique”), 11:55–12:14; Ex. 1003 ¶¶ 125–126).

Turning back to Stroud, Petitioner contends that “Stroud expands capacity by adding ‘modular card[s], or blade[s]’ to a chassis.” Pet. 48 (citing Ex. 1004 ¶¶ 98, 176). Petitioner also contends that Stroud teaches expansion by stating that various implementations are “distributed across multiple [chassis] devices of 16.” *Id.* at 49 (quoting Ex. 1004 ¶ 343 (alteration in original); citing Ex. 1004, Fig. 2E). Petitioner also contends that “Stroud contemplates ‘creat[ing] larger systems.’” *Id.* at 50 (quoting Ex. 1004 ¶ 115) (alteration in original). Petitioner reasons that “[w]hen all slots are full, it would have been obvious to add more chassis as the most straightforward option of a finite number of ways to expand capacity further.” *Id.* at 48. Petitioner also relies on known prior art systems that commonly “use multiple chassis in data centers.” *Id.* at 49 (citing Ex. 1040 ¶ 2; Ex. 1014, 14–18, 23).

Based on the above-summarized teachings in Stroud and DaSilva, Petitioner argues that a “POSITA looking to scale Stroud’s architecture to serve a larger network load would increase the number of chassis” based on Stroud’s expansion teachings and DaSilva’s teachings for multi-chassis architectures. *See* Pet. 49 (citing Ex. 1003 ¶¶ 127–129).

Petitioner also contends that

[t]he references teach similar architectures for similar purposes. Stroud features a multi-card chassis for network testing (Ex-1004, ¶81), where each card has a management switch connected to a backplane (*id.*, ¶101, ¶99). Similarly, DaSilva features a multi-card chassis for routing traffic over network topologies, where each card has a switching module connected to a backplane. Ex-1005, 7:58-67. The references share similar goals—providing reliable and flexible networking and data processing infrastructure. Ex-1004, ¶2; Ex-1005, 1:55-59; Ex-1003, ¶133.

Pet. 49.

Petitioner summarizes that “[t]he combination was simple . . . merely adding chassis and a chassis ID. This required minimal modification—a prepended header or additional sub-field—with minor changes following the direct teachings of DaSilva and Stroud.” Pet. 52 (citing Ex. 1005, 9:58–10:14; Ex. 1004 ¶¶ 366–372).

Patent Owner argues that Petitioner’s showing is deficient with respect to limitation 1e’s “chassis identifier.” Prelim. Resp. 11–19. Patent Owner argues that “every discussion of ‘chassis’ in Stroud refers to a single chassis, and there is no discussion or suggestion of multiple chassis.” *Id.* at 12 (citing Ex. 1004 ¶¶ 98, 176, 365, 376 (“[S]ystem 16 may be housed in a chassis 50 that interconnects multiple cards 54 via a backplane 56.” (emphasis in original))).

Patent Owner also argues that “DaSilva is directed to a ‘a *virtual* chassis system 100 including a plurality of network nodes 110 operably coupled by dedicated link aggregate groups for communicating control and addressing information called virtual fabric links (VFLs) 120.’” Prelim. Resp. 15 (quoting Ex. 1005, 3:47–51)(emphasis in original). Patent Owner also argues that DaSilva teaches “[w]ithin the virtual chassis system 100, a network node 110 is assigned a globally unique identifier called a chassis identifier or chassis ID.” *Id.* (quoting Ex. 1005, 4:52–54). Therefore, Patent Owner contends that “[t]he ‘chassis ID’ . . . simply serves to identify particular ‘network nodes’ within a particular ‘network topology’—it does not correspond to a physical chassis at all.” *Id.* (citing Ex. 1005, 5:25–6:35; Fig. 1a).

Patent Owner’s arguments attack the references individually without undermining Petitioner’s showing. As described above, Petitioner relies on the combined teachings of Stroud and DaSilva, where Stroud generally discloses expansion to create larger capacity packet data testing systems, with system 16 described in one embodiment as including a chassis 50, and DaSilva teaches using multiple chassis ID headers to route packets between nodes. *See* 1004 ¶¶ 98, 115, 176, 343; Ex. 1005, Fig. 4, code (57). In addition, although Stroud discloses single chassis embodiments as Patent Owner argues, nothing in Stroud limits its system to a single chassis. Rather, in paragraph 176 cited by Petitioner (Pet. 23, 24, 48), Stroud discloses that “[n]etwork testing system 16 may be configured to support *any suitable number of cards or blades* 54,” and then states that “[i]n one embodiment, system 16 is configured to support between 1 and 14 cards 54 in a single chassis 50.” Ex. 1004 ¶ 176 (emphasis added). Based on the

current record, this disclosure implies or at least suggests that in Stroud, a larger network testing system 16 supporting 15 or more cards requires at least two chassis. *See id.*

In addition, DaSilva's Figure 4, which Petitioner relies upon and annotates as indicated above, discloses multiple nodes 110a and 110c that DaSilva describes as including "multi-slot *chassis-based* architecture[s]," with modules generally "integrated into the back-plane of the chassis." *See* Ex. 1005, 7:64–67 (emphasis added), 8:23–26; Pet. 47 (annotating Ex. 1005, Fig. 4; citing Ex. 1003 ¶¶ 123 ("Similar to Stroud's chassis, each chassis includes cards with modules connected through a backplane interface network.")), 135 ("DaSilva teaches a 'virtual chassis system' that allowed multiple physical chassis to be grouped together." (citing Ex. 1005, 3:64–4:7, 4:23–38)). On this preliminary record, DaSilva describes the hardware architecture as "virtual" in the sense that it is easy to alter nodes into different topologies—not because there are no physical chassis. *See* Ex. 1005, 2:14–19 (describing prior art problems with networks such that "once implemented, it is sometimes difficult to upgrade or transition from one type of network topology to another type of network topology"), 5:26–29 ("[T]he network nodes 110 in a virtual chassis system 100 may be coupled in any of a plurality of types of network topologies without affecting operation of the virtual chassis system 100.").

Patent Owner also argues that Stroud teaches away from adding additional chassis. Prelim. Resp. 13. Patent Owner contends that adding additional chassis would add cost and complexity based on the manufacturing costs, including for the new chassis, connections, and

backplane, and also based on processing the chassis ID for each packet. *Id.* at 13–14.

The record does not support a teaching away of multiple chassis in Stroud. As noted above, Patent Owner contends that “there is no discussion or suggestion of multiple chassis” in Stroud. Prelim. Resp. 12. Therefore, on this preliminary record, Stroud does not disparage the use of, or teach away from, multiple chassis. As discussed above, based on the current record, Stroud implies or suggests two or more chassis for large testing systems that require more than 15 cards. *See* Ex. 1004 ¶ 176. That Stroud describes a way to expand capacity by using more boards or cards in a single chassis is simply teaching another way to expand capacity—it is not a teaching away from expanding capacity via multiple chassis.

Single chassis systems that use more cards to expand capacity create added cost and complexity based on the increase in cards and networking for those cards. Therefore, contrary to Patent Owner’s arguments, Stroud does not teach away from adding cost and complexity but rather at most signifies there is a trade-off with capacity expansion. In addition, based on the current record, an artisan of ordinary skill using common sense would have recognized that a large chassis will not always fit into a small room or space, so that an artisan of ordinary skill would have contemplated multiple chassis distributed across multiple rooms or spaces based on the teachings of Stroud and DaSilva.

Patent Owner also argues that Petitioner’s evidence showing the well-known use of “multiple chassis in data centers” is not applicable to Stroud, because Stroud does not disclose a data center. Prelim. Resp. 14 (quoting Pet. 49). Patent Owner further contends that because the alleged prior art

use is not in the relevant art, Petitioner’s use thereof is “impermissible hindsight.” *Id.* (citing *Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 886 (Fed. Cir. 2024) (“It does not suffice to meet the motivation to combinerequirement to recognize that [the claimed subject matter was] known in the art.”)).

These arguments do not undermine Petitioner’s showing. Even withoutthe use of known prior art as including “multiple chassis in data centers” (Pet. 49), Petitioner’s specific showing is sufficient for the reasons outlined above. Also, contrary to Patent Owner’s argument that multi-chassis data centers are not relevant to Stroud, Petitioner shows that “Stroud features a multi-card chassis for network testing” and similar to DaSilva, “provid[es] reliable and flexible networking and *data processing infrastructure.*” Pet. 49 (citing Ex. 1004 ¶ 81) (emphasis added). Therefore, Petitioner shows that known prior art data centers, which process data using multi-chassis data processing infrastructure, are analogous to Stroud’s chassis-based test and data processing system.

In addition, in distinction to *Virtek Vision*, Petitioner provides sufficient motivating reasons for using multiple chassis commonly used in networking systems on this preliminary record. *Cf. Virtek Vision*, 97 F.4th at 886 (“There was no evidence that there are a finite number of identified, predictable solutions. There is no evidence of a design need or market pressure.”); *Western Union Co. v. MoneyGram Payment Sys., Inc.*, 626 F.3d 1361, 1369–71 (Fed. Cir. 2010) (“find[ing] the use of an electronic transaction device where the prior art employed a fax machine to be an unpatentable improvement at a time when such a transition was commonplace in the art”). As discussed above, Petitioner argues multiple

chassis would have provided more capacity to Stroud's data processing network and increasing the number of chassis was one of a number of finite ways to provide capacity expansion. Pet. 48 ("When all slots are full, it would have been obvious to add more chassis as the most straightforward option of a finite number of ways to expand capacity further."). Patent Owner does not address Petitioner's rationale of expanding network capacity via multiple chassis when all the slots in a single chassis are full. *See* Prelim. Resp. 11–17.

*(iv) Summary for limitation 1e*

On this preliminary record, Petitioner's showing for limitation 1e, as summarized above and in light of Patent Owner's arguments otherwise, is sufficient for purposes of institution.

*c) Summary for Claim 1*

Based on our analysis set forth above and the current record, we determine that the information presented in the Petition, in light of the Preliminary Response, demonstrates a reasonable likelihood that Petitioner will prevail in establishing that claim 1 is unpatentable under 35 U.S.C. § 103 over the combination of Stroud and DaSilva.

*4. Analysis of Claims 2, 3, 13, and 14*

Independent claim 13 is similar to independent claim 1, where claim 1 recites a platform and claim 13 recites a computer-readable media. Limitation 13c of claim 13 is also similar to limitation 7c in independent claim 7, and Petitioner relies solely on Stroud, as discussed below in the analysis of independent claim 7. Claims 2 and 3 depend from claim 1, and claim 14 depends from claim 13.

On this preliminary record, the Petition sufficiently shows for institution purposes that Stroud and DaSilva teach the limitations of claims 2, 3, 13, and 14. *See* Pet. 53–68. Patent Owner does not address Petitioner’s showing for these claims. *See generally* Prelim. Resp.

Accordingly, we determine on this record that the information presented in the Petition, in light of the Preliminary Response, demonstrates a reasonable likelihood that Petitioner will prevail in establishing that claim 2, 3, 13, and 14 are unpatentable under 35 U.S.C. § 103 over the combination of Stroud and DaSilva.

*E. Ground 2, Alleged Obviousness of Claims 7, 9, and 10 over Stroud and Cragon*

Petitioner contends that claims 7, 9, and 10 would have been obvious over the combined teachings of Stroud and Cragon. Pet. 31–38.

*1. Cragon*

Cragon is a textbook that describes common memory systems and groups of memory types, with “rules for implementation.” Ex. 1006, 3 (“Computer designers strive to provide the best performance consistent with cost objectives.”). One example is a hierarchy of memory units, for example processor internal registers, the main memory, and bulk storage on magnetic wire recorders. Ex. 1006, 48. “Hierarchical memory systems permit the designer to trade latency or access time against cost.” *Id.* “Main memory is the largest random access memory in the system.” *Id.* at 49. Another example involves four types of cache, including an instruction cache, a data cache, a unified cache, and a split cache. *Id.* at 71. Other examples include a multi-level cache (*id.* at 69, 219–220) and interleaved memory (*id.* at 496–497).

2. *Claim 7*

[7pre]. A method for data flow processing in a platform, comprising:

[7a] configuring a plurality of swappable pods or cards in one or more chassis, coupled through a messaging interface network, to implement a data flow processing architecture;

[7b] configuring user-definable hardware modules or user-definable software modules in each of one or more of the plurality of swappable pods or cards;

[7c] communicating a data flow in accordance with the implemented data flow processing architecture among one or more hardware modules or one or more software modules in each of the plurality of swappable pods or cards, including the user-definable hardware modules or user-definable software modules; and

[7d] selecting a memory superposition in at least one of the plurality of swappable pods or cards having a plurality of types of memory with selectable arrangement of the plurality of types of memory as multilevel cache, interleaved memory, swapped memory over a specified address range, and memory allocated to specified address ranges according to parameterized task needs.

3. *Analysis of Claim 7*

a) *Preamble and Limitations 7a–7c*

Petitioner relies on Stroud and its showing for claim 1 to address claim 7’s preamble and limitations 7a and 7b. Pet. 69–70.

Relying on its showing for limitation 13c, Petitioner contends that Stroud discloses limitation 7c. Pet. 70 (citing Ex. 1003 ¶¶ 210–211). In particular, Petitioner relies on Stroud’s network testing application for generating synthetic data flows, citing several examples, including HTTP Authenticated and HTTP Flash Video. *Id.* at 62 (citing Ex. 1003 ¶ 175; Ex. 1004 ¶¶ 80–93, 98). Petitioner generally explains that the purpose of

Stroud's network testing network testing system is communicating data flow in accordance with the data flow processing architecture by "simulat[ing] . . . network traffic by generating and then sending a data flow (e.g., HTTP, video, and other network data flows) using the parallel architecture of the platform." *Id.* Petitioner provides several other examples of simulating network components and data flow for testing. *See id.* at 62–67.

Patent Owner does not address Petitioner's showing for the preamble and limitations 7a–7c. *See generally* Prelim. Resp. On this preliminary record, Petitioner's showing, as summarized above, is sufficient for purposes of institution.

*b) Limitation 7d*

Limitation 1.d recites

selecting a memory superposition in at least one of the plurality of swappable pods or cards having a plurality of types of memory with selectable arrangement of the plurality of types of memory as multilevel cache, interleaved memory, swapped memory over a specified address range, and memory allocated to specified address ranges according to parameterized task needs.

*i. "memory superposition"*

Petitioner contends that each of Stroud's cards include multiple types of memory. Pet. 70–71 (citing Ex. 1004 ¶¶ 127, 169; Ex. 1003 ¶ 214). Petitioner relies on Cragon for its "textbook [approaches for using] different types of memory in computers" to provide "a flexible and selectable arrangement" in Stroud's system depending on the needs of particular workloads. *Id.* at 68, 73–74 (citing Ex. 1006, 413–414, 536–548; Ex. 1003 ¶ 217).

In particular, Petitioner contends that Stroud teaches two or more types of memory on its swappable pods or cards, where Stroud discloses that

memory 103A may include “DRAM, SRAM, [] Flash memory, hard drive, or any other memory” (Ex. 1004 ¶ 127), and memory “103B may comprise any suitable memory device” such as “QDR (quad data rate) SRAM” (*id.* ¶ 169). Pet. 71–72 (annotating Ex. 1005, Fig. 5; citing Ex. 1003 ¶ 215); *see also id.* at 72–73 (stating “Stroud’s figures teach various card configurations with a plurality of memory types”) (citing Ex. 1004 ¶ 717, Figs. 6A–9A, 14A–14B, 59A–59B; Ex. 1003 ¶ 125).

Based on Stroud’s multiple memories, Petitioner contends that Stroud teaches “a memory superposition” as limitation 7d recites under Petitioner’s claim construction (adopted above). *Supra* Section III.C (Claim Construction); Ex. 1001, 6:65–7:11 (listing various types of memory including DRAM and SRAM). That is, Petitioner alleges that Stroud teaches “two or more types of memory on its cards . . . that are made available for data-flow processing.” *See* Pet. 70–71 (citing Ex. 1003 ¶ 213).

*ii. “a selectable arrangement of the plurality of types of memory”*

Petitioner contends that Cragon teaches “a selectable arrangement of the plurality of types of memory” as limitation 7d recites, where Cragon teaches that “multilevel cache, interleaved memory, swapped memory over a specified address range, and memory allocated to specified address ranges according to parameterized task needs” were common alternative memory arrangements providing flexibility to an artisan of ordinary skill. *See* Pet. 73–74 (citing Ex. 1006, 413–414 (discussing bounds registers, memory keys, translation table keys, and distinct address spaces)), 536–548 (discussing disks, disk arrays, low cost RAM, buffers, and disk caches), 74–78 (showing that Cragon discloses the four recited memory arrangements); Ex. 1003 ¶ 217). Petitioner contends that because “Stroud aims to provide a

flexible platform with user-definable modules configured to perform a wide variety of applications,” it would have been obvious in view of Cragon “to select between common memory arrangements to suit the particular application” in order to optimize memory performance using known methods and to yield predictable results depending on the needs of particular workloads. *See id.* at 73–74 (citing Ex. 1004 ¶¶ 106–113, 117–120, 311–313, 343, 373, 689–700, Figs. 51–52; Ex. 1006, 413–414, 536–548; Ex. 1003 ¶¶ 219–233), 79–80 (listing reasons for the combination).

According further to Petitioner, it would have been obvious to employ Cragon’s common memory arrangements for their known benefits (as listed below) in order to provide selectable options to fit a particular application in Stroud’s user-definable, scalable, and flexible system, where Stroud teaches “any suitable type of memory device” (Ex. 1004 ¶ 127). Pet. 78–79 (citing Ex. 1004 ¶¶ 127–128, 144, 382, 399, 493). Petitioner also notes that “[f]inding ways to improve system memory is . . . a motivation of computing system engineers.” *Id.* (quoting Ex. 1028 ¶ 2; citing Ex. 1003 ¶¶ 236–237).

As indicated in the previous paragraph and below, Petitioner also separately provides beneficial reasons to select each of the four types of memory arrangements in Stroud’s system, depending on design goals (workload requirements), as summarized below.

*iii. “multi-level cache”*

Petitioner relies on Cragon’s and Stroud’s combined teachings to address limitation 7d’s “multilevel cache.” Petitioner notes that Cragon discloses a two-level cache, with the first a small, fast memory close to the processor and implemented in SRAM (which Stroud teaches), and the second a larger and slower memory (Stroud discloses a hard drive, DRAM,

or other suitable memory as noted above), such that it would have been obvious to implement a multi-level cache system on one or more of Stroud's cards, according to work load or system needs. *See* Pet. 74–75 (citing Ex. 1004 ¶¶ 127, 169; Ex. 1006, 67, 73, 219 (discussing multi-level caches including disk cache, and discussing improving transport time and bus loading with two-level cache between processor and main memory), Fig. 2.27 (“Two-level cache”); Ex. 1003 ¶¶ 219–221). Petitioner also contends that “[m]ultilevel cache was known in the art for accelerating access to recently-used data and was widely used for decades.” *Id.* at 74 (citing Ex. 1006, 67, 73).

*iv. “interleaved memory”*

Petitioner relies on Cragon's and Stroud's combined teachings to address limitation 7d's “interleaved memory.” Petitioner notes that Cragon teaches that “[h]igh-order interleaving . . . permits the easy *intermixing* of different memory technology such as a combination of RAM and ROM.” Pet. 75 (quoting Ex. 1006, 497 (emphasis in original)). Petitioner contends that Cragon teaches that interleaved memory is a form of parallelism by distributing read and write accesses over multiple memory modules, and that applying Cragon's interleaving teachings to Stroud allows for alternately accessing different types of memory arranged on-chip or off-chip and further allows for blending memory speed and size combined with easy memory expansion. *Id.* at 75–76 (citing Ex. 1006, 491, 495; Ex. 1003 ¶¶ 222–224). Petitioner also submits that “when applying Cragon's high-order interleaving to Stroud's various on-chip and on-card memory, the resulting accesses achieve an average access bandwidth of those memories.” *Id.* at 76 (citing Ex. 1006, 491–497; Ex. 1003 ¶¶ 223–224).

Petitioner also contends that “Cragon teaches allocating memory to a task according to parameterized task needs, e.g., disk storage for interleaving or swapping, to meet ‘requirements based upon workloads.’” Pet. 78 (quoting Ex. 1006, 536) (emphasis omitted). Although Cragon states that “[t]here is very little solid information published” about “disk bandwidth and storage requirements based upon workloads,” Petitioner contends that “Cragon teaches five commonly-used parameters for task needs: ‘[c]apacity,’ ‘[b]andwidth,’ ‘[s]ervice rate,’ ‘[r]esponse time,’ and ‘cost.’” *Id.* (quoting Ex. 1006, 536); Ex. 1006, 536 (“1. Capacity. Bytes of storage (formatted). 2. Bandwidth. Bytes transferred/unit of time. 3. Service rate. Number of service requests satisfied/unit of time. 4. Response time. Time between the start and completion of an event. 5. Cost. \$/Mbyte.”); *see also* Ex. 1003 ¶ 232.

Petitioner also contends that Cragon provides examples of different tasks and their requirements, such as access times versus different types of memory used for specific tasks. *See* Pet. 78 (citing Ex. 1006, 41–63, 536–548; Ex. 1003 ¶ 232). At the cited paragraph, Dr. Alpert states that the above-listed five parameters, and others, “were equally important for other types of memory and used to organize the memory hierarchy.” Ex. 1003 ¶ 232 (listing parameters including latency, service rate, amount of work completed in a specific time, scheduling, and the varying performance between main memory and bulk storage as well-known parameters (citing Ex. 1006, 48–63)).

v. “*swapped memory over a specified address range*”

Petitioner relies on Cragon’s and Stroud’s combined teachings to address limitation 7d’s “[s]wapped memory over a specified address range.”

Pet. 76–77 (citing Ex. 1003 ¶¶ 227–229 (“Swap files and virtual memory were commonly used to expand the amount of memory that a processor could utilize.”). Petitioner contends that Cragon teaches swapping memory over specified memory ranges by moving data for certain address ranges from DRAM (main memory) to non-volatile memory (e.g., disk) when not in use. *Id.* at 76 (citing Ex. 1006, 51, 255–257, 264–265). Petitioner further states that Cragon teaches “paged allocation,” which splits the address space into pages and “mov[es] pages back and forth between real and auxiliary memory.” *Id.* (citing Ex. 1006, 262, 265, 352 (“page swap”); Ex. 1003 ¶ 227).

According to Petitioner, “the combination teaches a plurality of memory types (on-chip or on-card) as swapped memory over a specified address range, e.g., DRAM as main memory and disk as non-volatile storage for the swap file.” Pet. 77 (citing Ex. 1004 ¶¶ 127, 169, 195–196, 269, 308, Figs. 5–10, 14A–B, 20, 23, 30, 49; Ex. 1006, 262, 265, 352 (“page swap”)). In other words, “each page is swapped in and out for a specific address range at fixed size intervals.” *Id.* at 76. Dr. Alpert opines that in view of Stroud and Cragon, it would have been obvious to use Stroud’s DRAM or SRAM as the main physical memory and disk as non-volatile storage for the swap file to expand the amount of available memory to a processor. *See* Ex. 1003 ¶¶ 228–229 (citing Ex. 1004 ¶¶ 195–196, 269, 308, Figs. 5–10, 14A–B, 20, 23, 30, 49); Pet. 76–77 (citing Ex. 1003 ¶¶ 227–229).

vi. “*memory allocated to specified address ranges according to parameterized task needs*”

Petitioner also relies Cragon’s and Stroud’s combined teachings to address limitation 7d’s “[m]emory allocated to specified address ranges according to parameterized task needs.” Pet. 77–78. Petitioner contends

that “Stroud teaches assigning specified address ranges to memory types based on their intended use (e.g., configuration memory, internal working memory, external memory).” *Id.* at 77 (citing Ex. 1004 ¶ 352). Petitioner contends that Cragon teaches memory allocated to specified address ranges for each task, to avoid “interfer[ing] with another task.” *Id.* (citing Ex. 1006, 413). According to Petitioner, Cragon provides details such as use of “‘bounds registers’ that set the ‘upper address limit’ and the ‘lower address limit’ of contiguous memory allocated to a task.” *Id.* (quoting Ex. 1006, 413–414). Petitioner provides an example of Cragon’s paged memory systems using tasked-based allocations of memory as described above. *Id.* at 77–78 (citing Ex. 1006, 414–417; Ex. 1003 ¶¶ 230–233).

Petitioner also asserts that Stroud teaches allocating different memory to address ranges so that it would have been natural to look to Cragon to teach implementation details such as translation tables and bound registers to specify address ranges for each task. Pet. 80 (citing Ex. 1004 ¶ 352; Ex. 1006, 66; Ex. 1003 ¶ 236–237).

*vii. Patent Owner’s Arguments*

Patent Owner argues that Cragon does not “provide . . . the claimed selectable arrangement” as recited in limitation 7d. Prelim. Resp. 23. Patent Owner argues that “Cragon provides a generalized discussion of how . . . abstract parameters can play a role in disk system design,” but “[n]othing in [Cragon’s] highly generalized discussion of various design considerations is a disclosure of the ‘selectable arrangement’ required by the claims.” *Id.* at 24 (citing Ex. 1006, 536–48). Patent Owner also argues that Petitioner’s citations to Cragon at pages 536–48 only relate to “a generalized discussion of how these abstract parameters can play a role in disk system design.” *Id.*

Patent Owner notes that Cragon discusses parameters, generalized design considerations, costs, bandwidth, and storage requirements, and alleges, without specificity, that this generalized discussion undermines the Petition. *See id.* at 22–24. Patent Owner also argues that it is not clear how cost, “a generalized design consideration,” can even be converted into a selectable arrangement of memory types. *Id.* at 23–24.

Patent Owner also argues that claim 7 requires “memory allocated to specified address ranges according to parameterized task needs” and Cragon fails to disclose this limitation. Prelim. Resp. 25. Patent Owner contends “it is not clear what it would mean to provide a ‘task’ associated with a ‘cost’ parameter.” *Id.* Patent Owner also contends that the claims are not directed to “examples of different tasks”; they require “memory allocated to specified address ranges according to parameterized task needs.” *Id.*

*vii. Analysis of the Parties’ Positions*

Patent Owner’s arguments do not undermine Petitioner’s specific showing as outlined above. Petitioner does not rely exclusively on pages 536–48 of Cragon to address the selectable arrangement limitation. Rather, as summarized above, Petitioner also relies on the combined teachings of Stroud and Cragon by citing various paragraphs and pages to teach or suggest selecting multilevel cache, interleaved memory, swapped memory, and memory allocated to specified address ranges, to address the selectable arrangement limitation. *See* Pet. 74 (“Ground 2 teaches the selectable arrangement including the arrangements listed in [7d], addressed in sequence below.” (citing Ex. 1003 ¶¶ 219–233)), 74–81 (discussing multilevel cache, interleaved memory, swapped memory, and memory allocated to specified address ranges based on the combined teachings of

Stroud and Cragon to show the recited selectable arrangement). Patent Owner's focus on one cited portion of Cragon as allegedly limited to disk memory does not address the Petition's full showing. As noted above, Dr. Alpert testifies that the five parameters, and others, "were equally important for other types of memory and used to organize the memory hierarchy." Ex. 1003 ¶ 232.

As part of this showing and as also summarized above, based on the current record, Petitioner provides sufficient rationale with factual underpinnings to show how the combined teachings of Stroud and Cragon suggest a selectable arrangement based in part on known benefits of each of the four recited memory arrangements in limitation 1d, including memory allocated to specified address ranges according to parameterized task needs. *See* Pet. 67–81. For example, Petitioner shows that an artisan of ordinary skill would have provided the selectable memory arrangement of "memory allocated to specific address ranges based on parameterized task needs," to avoid "interfer[ing] with another task." *See id.* at 77 (quoting Ex. 1006, 413) (alteration in original).

Patent Owner's argument that "the claims are not directed to 'examples of different tasks,'" because "they require 'memory allocated to specified address ranges according to parameterized task needs,'" essentially amounts to repeating a portion of limitation 7d without explaining why the Petition is deficient. *See* Prelim. Resp. 25 (citing Pet. 78). The Petition, based on Cragon's teachings and the testimony of Dr. Alpert, sufficiently shows that different tasks have different "parameterized task needs" such as, *inter alia*, cost per capacity, bandwidth, response time, access time, service

rate, storage capacity, etc. *See* Pet. 77–78 (citing Ex. 1006, 41–63, 536–548; Ex. 1002 ¶ 232).

Petitioner also provides an example of implementing disk storage for interleaving or swapping (which require specified address ranges) as meeting parameterized task needs, listing specific access times for implementing interleaving or swapping via use of cache, main memory, and disk. *See id.* at 78 (citing Ex. 1006, 41–63, 536–548; Ex. 1002 ¶ 232). At the cited paragraph, Dr. Albert provides another example, *inter alia*, of running background processes (parameterized task needs), which have lower bandwidth, service rate, and response time requirements than processes such as displaying video data (another parameterized task need), and he testifies that system designers were well aware of the various parameters for these and the other workload requirements. *See* Ex. 1003 ¶ 232.

In general, Petitioner sufficiently shows for institution purposes that Stroud teaches allocating memory to specific address ranges and flexible memory options, and Cragon teaches that the four recited memory arrangements were well-known selectable configurations to system designers with known benefits and trade-offs. *See* Pet. 67–81. As summarized above, Petitioner shows various sufficient reasons on this record for the combination: to expand memory capacity, to blend speed and capacity, to provide quick memory access, to mix different available memory types, to obtain average bandwidths across memory modules, and generally to accommodate known memory design or workload goals like bandwidth, response time, cost per storage capacity, storage capacity, etc. *See id.*; Ex. 1003 ¶¶ 221–223, 228–229, 232 (discussing and summarizing workload requirements based on processing types, memory types,

bandwidth, storage requirements, service rate, and latency (citing Ex. 1006, 48–63, 536–541, 548)). Patent Owner does not challenge this rationale. *See generally* Prelim. Resp.

On this preliminary record, Petitioner’s showing for limitation 7d, as summarized above and in light of Patent Owner’s arguments otherwise, is sufficient for purposes of institution.

4. *Summary for Claim 7*

Based on our analysis set forth above, including our analysis of Patent Owner’s arguments and the current record, we determine that the information presented in the Petition demonstrates a reasonable likelihood that Petitioner will prevail in establishing that claim 7 is unpatentable under 35 U.S.C. § 103 over the combination of Stroud and Cragon.

5. *Analysis of Claims 9 and 10*

Petitioner’s showing for claims 9 and 10, which depend from claim 7, is sufficient for purposes of institution. *See* Pet. 81–82. Patent Owner does not address claims 9 and 10 separately. *See generally* Prelim. Resp.

Accordingly, we determine on this record that the information presented in the Petition, in light of the Preliminary Response, demonstrates a reasonable likelihood that Petitioner will prevail in establishing that claims 9 and 10 are unpatentable under 35 U.S.C. § 103 over the combination of Stroud and Cragon.

F. *Alleged Obviousness of Claims 7, 9, and 10 over Stroud, Cragon, and Saulsbury*

Petitioner contends that claims 7, 9, and 10 would have been obvious over the combined teachings of Stroud, Cragon, and Saulsbury. Pet. 81–93.

1. *Saulsbury (Ex. 1007)*

Saulsbury teaches using multiple memory types in a “scalable computer processing architecture.” Ex. 1007 ¶ 8. Saulsbury states “the present invention may comprise, in a computer system, a scalable computer processing architecture including one or more processor chips each having . . . at least one bank of memory.” *Id.* “The at least one bank of memory on each of the processor chips include a mode control input for controlling the mode of the at least one bank of memory between physical memory and cache memory.” *Id.*

2. *Analysis of Claims 7, 9, and 10*

Petitioner’s showing for here is similar to its showing based on Stroud and Cragon discussed above. *See* Pet. 81–93.

Petitioner adds Saulsbury to Stroud and Cragon, *inter alia*, for its teaching of “*switch[ing] the memory mode* between physical memory and cache memory, depending on the particular application of the processor and memory chip.” Pet. 84–85 (quoting Ex. 1007 ¶ 3; citing Ex. 1007 ¶ 65, Fig. 1). Petitioner argues that because “Stroud . . . provide[s] a flexible platform, . . . it was obvious to apply Saulsbury’s teachings to select between textbook memory arrangements as taught by Cragon for the memories on each card.” *Id.* at 85 (citing Ex. 1003 ¶ 260). Similar to its showing above with respect to Stroud and Cragon, Petitioner relies on the combined teachings of Stroud, Cragon, and Saulsbury, and addresses how they teach limitation 7e’s multilevel cache, interleaved memory, swapped memory over a specified address range, and “memory allocated to specified address ranges according to parameterized task needs.” Pet. 86–88.

Petitioner also contends that

Saulsbury teaches two techniques that further Stroud's stated goals of scalability and flexibility: (1) the addition of on-chip DRAM to a CPU and (2) techniques for selecting the arrangement of a memory hierarchy. As Saulsbury explains, its teachings are directed to "scalable computer processing architecture[s]" (Ex-1007, ¶8, ¶16) and provide flexible memory arrangements "depending on the particular application." *Id.*, ¶3. Pet. 89.

Patent Owner generally relies on its arguments for Stroud and Cragon, and contends that Saulsbury merely teaches "switching between physical and cache memory," which "is not a disclosure of the selectable arrangement of a plurality of memory types required by the claims." Prelim. Resp. 25. Patent Owner also argues that "Saulsbury does nothing to cure Cragon's failure to disclose the claimed "memory allocated to specified address ranges according to parameterized task needs.'" *Id.* at 25–26.

These arguments do not address the full thrust of Petitioner's reliance on the combined teachings of Stroud, Cragon, and Saulsbury. *See* Pet. 81–93. On this preliminary record, including Petitioner's showing with respect to Stroud and Cragon as summarized above, the Petition sufficiently shows for institution purposes that Stroud, Cragon, and Saulsbury teach the limitations of claims 7, 9, and 10. *See* Pet. 81–93.

Based on our analysis set forth above, we determine on this record that the information presented in the Petition, in light of the Preliminary Response, demonstrates a reasonable likelihood that Petitioner will prevail in establishing that claim 7, 9, and 10 are unpatentable under 35 U.S.C. § 103 over the combination of Stroud, Cragon, and Saulsbury.

*G. Alleged Obviousness of Claims 4, 8, and 15 over Stroud, DaSilva, Cragon, and Saulsbury*

Petitioner contends that claims 4, 8, and 15 would have been obvious over the combined teachings of Stroud, DaSilva, Cragon, and Saulsbury. Pet. 93–94.

Claim 4 depends from claim 1 and adds limitations similar to those addressed for claim 7. Claim 8 depends from claim 7 and adds limitations similar to those addressed for limitation 1e. Claim 15 depends from claim 13 and adds limitations similar to those addressed for claim 7. As indicated above, claim 13 is similar to claim 1.

Petitioner relies on its showing for claims 1, 7, and 13. *See* Pet. 93–94. Patent Owner relies on its arguments for claims 1 and 7. Prelim. Resp. 26.

Based on our analysis set forth above and the current record, we determine that the information presented in the Petition, in light of the Preliminary Response, demonstrates a reasonable likelihood that Petitioner will prevail in establishing that claims 4, 8, and 15 are unpatentable under 35 U.S.C. § 103 over the combination of Stroud, DaSilva, Cragon, and Saulsbury.

#### IV. CONCLUSION

After considering the evidence and arguments presented in the Petition and the Preliminary Response, we determine that Petitioner demonstrates a reasonable likelihood of prevailing on its assertion that at least one claim of the '753 patent is unpatentable. Accordingly, we institute an *inter partes* review of the challenged claims on all of the grounds presented in the Petition. *See* 37 C.F.R. § 42.108(a); *SAS Inst., Inc. v. Iancu*,

138 S. Ct. 1348, 1359–60 (2018); *AC Techs. S.A. v. Amazon.com, Inc.*, 912 F.3d 1358, 1364 (Fed. Cir. 2019) (“[I]f the Board institutes an IPR, it must . . . address all grounds of unpatentability raised by the petitioner.”). At this stage of the proceeding, we have not made a final determination as to the patentability of these challenged claims.

## V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that pursuant to 35 U.S.C. § 314, *inter partes* review is instituted as to claims 1–4, 7–10, and 13–15 of the ’753 patent with respect to all grounds of unpatentability presented in the Petition; and

FURTHER ORDERED that *inter partes* review is commenced on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

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