UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,803,214 B2
APPLICATION NO. : 12/825211
DATED : August 12, 2014
INVENTOR(S) : Tang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page:

The first or sole Notice should read --

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 473 days.

Signed and Sealed this
Thirtieth Day of May, 2017



Michelle K. Lee
Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

73115 7590 06/04/2015

SCHWEGMAN LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER
JEAN BAPTISTE, WILNER

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
06/04/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@slwip.com
SLW@blackhillsip.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

In re Patent No. 8,803,214	:
Tang et al	: REDETERMINATION OF
Issue Date: August 12, 2014	: PATENT TERM ADJUSTMENT
Application No. 12/825,211	:
Filed: June 28, 2010	:
Attorney Docket No. 303.B12US1	:
Title: THREE DIMENSIONAL MEMORY	:
AND METHODS OF FORMING THE SAME	:

This is a decision on the petition filed on October 7, 2014, which is being treated as a petition under 37 CFR 1.705(b) requesting that the patent term adjustment indicated on the above-identified patent be corrected to indicate that the term of the above-identified patent is extended or adjusted from 312 to 446 days. The Office has re-determined the PTA to be 473 days.

This redetermination of patent term adjustment is not the Director's decision on the applicant's request for reconsideration within the meaning of 35 U.S.C. 154(b)(4) that triggers a 180-day period for applicant disagreeing with the Office redetermination to commence a civil action in the District Court for the Eastern District of Virginia.

The Office acknowledges submission of the $200.00 fee set forth in 37 CFR 1.18(e). No additional fees are required. The fee set forth in 37 CFR 1.18(e) is required and will not be refunded.

The term of the above-identified patent is extended or adjusted by 473 days.

Relevant Procedural History

On August 12, 2014, this patent issued with a patent term adjustment determination of 312 days. On October 7, 2014, patentee filed this request for redetermination of patent term adjustment, requesting that patentee be granted a patent term adjustment of 446 days.

Redetermination

Patentee agrees with the Office's calculation of A delay of 266 days, C delay of 0 day, overlap of 0 days and 43 days of applicant delay. Patentees dispute the period of B delay.

The Office disagrees with the calculation of 43 days of applicant delay. A review of the record shows that a reduction of 29 days was taken for the submission of the RCE on September 26, 2013 after a reply in the form of the issue fee was submitted. However, a reduction for the submission of an RCE is not warranted based on the filing date of the RCE pursuant to 37 CFR 1.704 (c)(12). As such the 29 day reduction will be removed.

Further review of the record shows that a reduction of 2 days for the submission of the petition to withdraw the application from issuance is required.

37 CFR 1.704 (c)(10) provides:

(10) Submission of an amendment under § 1.312 or other paper, other than a request for continued examination in compliance with §1.114, after a notice of allowance has been given or mailed, in which case the period of adjustment set forth in § 1.703 shall be reduced by the lesser of:

i) The number of days, if any, beginning on the date the amendment under § 1.312 or other paper was filed and ending on the mailing date of the Office action or notice in response to the amendment under § 1.312 or such other paper;

or

ii) Four months;

In this instance the petition to withdraw the application from issuance was submitted after the mailing of the Notice of Allowance and after payment of the issue fee. The 2 day reduction is calculated beginning on the date the petition to withdraw from issuance was filed September 26, 2013 and ending on the mailing of the petition decision on September 27, 2013.

As such, applicant delay totals 16 (2 + 14) day.

The Office accorded 89 days of B delay based upon the Office's former interpretation of rule 37 CFR 1.703(b)(1) which excluded

from the amount of "B" delay the period beginning on the date of filing of the continued examination and ending on the date of the issuance of the patent. The Federal Circuit reviewed the statutory interpretation of 35 U.S.C. § 154(b)(1)(B)(i) and issued a decision regarding the effects of a Request for Continued Examination ("RCE") on "B" delay in the Novartis AG v. Lee, 740 F.3d 593 (Fed. Cir. 2014. In *Novartis*, the Federal Circuit agreed with the Office that "no ["B" delay] adjustment time is available for any time in continued examination, even if the continued examination was initiated more than three calendar years after the application's filing." *Novartis*, 740 F.3d at 601. However, the *Novartis* court found that if the Office issues a notice of allowance after an RCE is filed, the period after the notice of allowance should not be excluded from the "B" delay period but should be counted as "B" delay. Id. at 602.

Pursuant to the Novartis decision, the UPSTO has determined that patentee is entitled to 223 days of "B" delay. In this case, the application was filed on June 28, 2010 and the patent issued on August 12, 2014. Thus, the application was pending for 1507 days. During this period, applicant filed one RCE, on September 26, 2013. The Office mailed two Notices of Allowance the first on May 28, 2013 and the second Notice of Allowance was mailed on March 31, 2014. Under 35 USC 154(b)(1)(B)(i), the time period consumed by continued examination ("RCE period") began on September 26, 2013 and ended on March 31, 2014, i.e., 187 days. Subtracting the RCE period from the total number of days the application was pending results in 1320 (1507 - 187) days. Thus, for purposes of "B" delay, the application was pending for (1320 - 1097) [i.e., 3 years (including a leap year) from the actual filing date] = 223 days beyond the three-year anniversary of the filing date.

The Office finds that there are 0 days of overlapping days of Office delay. In Wyeth v. Kappos, 591 F.3d 1364 (Fed. Cir. 2010), the United States Court of Appeals for the Federal Circuit determined that overlap occurs when the calendar days overlap between the "A" and "B" delays.

Overall PTA Calculation

Formula:

"A" delay + "B" delay + "C" delay - Overlap - applicant delay = X

USPTO's Calculation:

266 + 223 + 0 - 0 - 16 = 473

Patentee's Calculation

446

Conclusion

Patentee is entitled to PTA of four hundred seventy-three (473) days. Using the formula "A" delay + "B" delay + "C" delay - overlap - applicant delay = X, the amount of PTA is calculated as following: 266 + 223 + 0 - 0 - 16 = 473 days.

Patentee has two (2) months from the date of the Office's redetermination of patent term adjustment to request reconsideration of the patent term adjustment if patentee continues to disagree with this determination (no petition fee). This two month period is extendible under 37 CFR 1.136(a). The new/renewed request for reconsideration may be filed w/out any additional fee. However, patentee who responds more than two months after the mail date of the redetermination is required to pay the extension of time fee. After the period of time to respond has expired, the Office will sua sponte issue a certificate of correction adjusting the PTA to four hundred seventy-three (473) days.

Telephone inquiries specific to this matter should be directed to the undersigned at (571) 272-3215.

/Charlema Grant/

Charlema Grant
Attorney Advisor
Office of Petitions

Enclosure: Copy of DRAFT Certificate of Correction and Copy of REVISED PALM Screen

DRAFT COPY

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT : 8,803,214 B2

DATED : August 12, 2014

INVENTOR(S) : Tang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page,

[*] Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 USC 154(b) by 312 days

Delete the phrase "by 312 days" and insert – by 473 days --

Office of Petitions: Routing Sheet



Application No. 12825211

This application is being forwarded to your office for further processing. A decision has been rendered on a petition filed in this application, as indicated below. For details of this decision, please see the document PET.OP.DEC filed on the same date as this document.

☐ **GRANTED**

☒ **DISMISSED**

☐ **DENIED**

Patent Term Adjustments

Patent Term Adjustment (PTA) for Application Number: 12/825,211

Filing or 371(c) Date:	06-28-2010	Overlapping Days Between { A and B} or { A and C} :	0
Issue Date of Patent:	08-12-2014	Non-Overlapping USPTO Delays:	355
A Delays:	266	PTO Manual Adjustments:	161
B Delays:	89	Applicant Delays:	43
C Delays:	0	Total PTA Adjustments:	473

Patent Term Adjustment History Explanation Of Calculations

Number	Date	Contents Description	PTO(Days)	APPL(Days)	Start
108	05-29-2015	Adjustment of PTA Calculation by PTO	134		0
108	05-29-2015	Adjustment of PTA Calculation by PTO	134		0
107	05-29-2015	Adjustment of PTA Calculation by PTO		2	0
107	05-29-2015	Adjustment of PTA Calculation by PTO		2	0
106	05-29-2015	Adjustment of PTA Calculation by PTO	29		0
106	05-29-2015	Adjustment of PTA Calculation by PTO	29		0
100.5	09-25-2013	PTA 36 Months	89		0.5
100	08-12-2014	Patent Issue Date Used in PTA Calculation			0
99	07-02-2014	Export to Final Data Capture			0
98	07-01-2014	Dispatch to FDC			0
97	06-30-2014	Issue Fee Payment Verified			0
96	06-30-2014	Issue Fee Payment Received			0
95	08-27-2013	Reverse Issue Fee			0
94	04-02-2014	Export to Initial Data Capture			0
93	03-31-2014	Electronic Review			0
92	03-31-2014	Email Notification			0
91	03-31-2014	Mail Notice of Allowance	64		75
90	03-26-2014	Office Action Review			0
89	03-26-2014	Office Action Review			0
88	03-26-2014	Issue Revision Completed			0
87	03-26-2014	Document Verification			0
	03-26-				

86	2014	Notice of Allowance Data Verification Completed		0
85	03-21-2014	Reasons for Allowance		0
84	03-21-2014	Allowability Notice		0
80	03-10-2014	Information Disclosure Statement considered		0
79	10-10-2013	Information Disclosure Statement (IDS) Filed		0
78	10-10-2013	Information Disclosure Statement (IDS) Filed	14	75
77	10-07-2013	Date Forwarded to Examiner		0
76	09-26-2013	Amendment Submitted/Entered with Filing of CPA/RCE		0
75	09-26-2013	Request for Continued Examination (RCE)	29	56
74	10-07-2013	Disposal for a RCE / CPA / R129		0
73	09-27-2013	Mail-Record Petition Decision of Granted to Withdraw from Issue - with assigned Patent NO.		0
72	09-27-2013	Record Petition Decision of Granted to Withdraw from Issue - with assigned Patent NO.		0
71	09-27-2013	Withdrawal Patent Case from Issue		0
70	09-26-2013	Petition Entered		0
69	09-26-2013	Workflow - Request for RCE - Begin		0
68	09-12-2013	Email Notification		0
67	09-11-2013	Issue Notification Mailed		0
65	08-30-2013	Export to Final Data Capture		0
64	08-29-2013	Dispatch to FDC		0
63	08-29-2013	Application Is Considered Ready for Issue		0
62	08-27-2013	Issue Fee Payment Verified		0
61	08-27-2013	Issue Fee Payment Received		0
60	06-24-2013	Finished Initial Data Capture		0
59	05-27-2013	Export to Initial Data Capture		0
58	05-28-2013	Electronic Review		0
57	05-28-2013	Email Notification		0
56	05-28-2013	Mail Notice of Allowance		0
55	05-22-2013	Office Action Review		0

54	05-22-2013	Office Action Review		0
53	05-22-2013	Office Action Review		0
52	05-22-2013	Office Action Review		0
51	05-22-2013	Issue Revision Completed		0
50	05-22-2013	Document Verification		0
49	05-22-2013	Notice of Allowance Data Verification Completed		0
48	05-07-2013	Interview Summary - Examiner Initiated		0
47	05-20-2013	Reasons for Allowance		0
46	05-20-2013	Examiner's Amendment Communication		0
45	05-20-2013	Allowability Notice		0
42	05-01-2013	Date Forwarded to Examiner		0
41	04-30-2013	Response after Final Action		0
40	02-01-2013	Electronic Review		0
39	02-01-2013	Email Notification		0
38	02-01-2013	Mail Final Rejection (PTOL - 326)	25	34
37	01-28-2013	Office Action Review		0
36	01-28-2013	Final Rejection		0
35	09-14-2012	Date Forwarded to Examiner		0
34	09-07-2012	Response after Non-Final Action		0
33	09-07-2012	New or Additional Drawing Filed		0
32	06-07-2012	Electronic Review		0
31	06-07-2012	Email Notification		0
30	06-07-2012	Mail Non-Final Rejection		0
29	06-04-2012	Office Action Review		0
28	06-03-2012	Non-Final Rejection		0
27	06-30-2011	Information Disclosure Statement considered		0
26	03-25-2012	Date Forwarded to Examiner		0
25	03-22-2012	Response to Election / Restriction Filed		0

24	02-21-2012	Electronic Review		0
23	02-21-2012	Email Notification		0
22	02-21-2012	Mail Restriction Requirement	177	0.5
21	02-13-2012	Office Action Review		0
20	02-12-2012	Restriction/Election Requirement		0
19	12-31-2011	Email Notification		0
18	12-30-2011	PG-Pub Issue Notification		0
17	12-07-2011	Case Docketed to Examiner in GAU		0
16	06-30-2011	Information Disclosure Statement (IDS) Filed		0
15	06-30-2011	Information Disclosure Statement (IDS) Filed		0
14	03-21-2011	New or Additional Drawing Filed		0
13	03-21-2011	Preliminary Amendment		0
12	09-08-2010	Case Docketed to Examiner in GAU		0
11	08-02-2010	Application Dispatched from OIPE		0
10	07-08-2010	Application Is Now Complete		0
9	07-08-2010	Email Notification		0
8	07-08-2010	Email Notification		0
7	07-08-2010	Change in Power of Attorney (May Include Associate POA)		0
6	07-07-2010	Sent to Classification Contractor		0
5	07-08-2010	Filing Receipt		0
4	06-28-2010	Applicants have given acceptable permission for participating foreign		0
3	06-29-2010	Cleared by OIPE CSR		0
2	06-28-2010	IFW Scan & PACR Auto Security Review		0
1	06-28-2010	Initial Exam Team nn		0
0.5	06-28-2010	Filing date		0

Close Window

Office of Petitions: Decision Count Sheet

Mailing Month

Application No. 12825211



For US serial numbers: enter number only, no slashes or commas. Ex: 10123456
For PCT: enter "51+single digit of year of filing+last 5 numbers", Ex. for PCT/US05/12345, enter 51512345

Deciding Official: GRANT, CHARLEMA

Count (1) - Palm Credit 12/825,211

Decision: DISMISSED

FINANCE WORK NEEDED
☐ Select Check Box for YES



Decision Type: 547-PTA Reclaculation- Novartis Decision 2014



Notes:

Count (2)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Count (3)

Decision: n/a

FINANCE WORK NEEDED
☐ Select Check Box for YES

Decision Type: NONE

Notes:

Initials of Approving Official (if required)

If more than 3 decisions, attach 2nd count sheet & mark this box ☐

Printed on: *5/28/2015*

Office of Petitions Internal Document - Ver. 5.0

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 8,803,214 B2
APPLICATION NO. : 12/825211
DATED : August 12, 2014
INVENTOR(S) : Sanh D. Tang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, in column 2, "Primary Examiner", line 1, delete "Olik Chaudhur" and insert -- Olik Chaudhuri --, therefor.

Signed and Sealed this
Fourth Day of November, 2014

Michelle K. Lee

Michelle K. Lee
Deputy Director of the United States Patent and Trademark Office

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sanh D. Tang et al.	Examiner: Wilner Jean Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket: 303.B12US1	
Customer No.:	73115	Confirmation No.: 1275	
Patent No.:	8,803,214	Issue Date: August 12, 2014	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

APPLICATION FOR PATENT TERM ADJUSTMENT UNDER 37 C.F.R § 1.705(b)

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patentee hereby applies for an adjustment of the patent term due to examination delay as shown on the patent granted on August 12, 2014. The required fee of $200.00 under 37 C.F.R. § 1.18(e) and a statement of facts in support of this application is attached.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 10-7-14 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sanh D. Tang et al.	Examiner: Wilner Jean Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket: 303.B12US1	
Customer No.:	73115	Confirmation No.: 1275	
Patent No.:	8,803,214	Issue Date: August 12, 2014	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

STATEMENT OF FACTS UNDER 37 C.F.R. § 1.705(b)(2) IN SUPPORT OF APPLICATION FOR PATENT TERM ADJUSTMENT

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The following is a statement of facts in support of the application for patent term adjustment.

Patentee has calculated the correct patent term adjustment as **446 days**. Patentee agrees with the calculations of the U.S. Patent Office as indicated in PAIR except for the error(s) in calculating the patent term adjustment as specified below:

The USPTO calculated the B-Term ("PTA 36 Months") as ending with the filing of a Request for Continued Examination on September 26, 2013. However, as determined by the Court in Novartis AG v. Lee (Fed. Cir. 2014), the patent term adjustment should be calculated by subtracting continued examination time (and other time identified in (i), (ii), and (iii) of (b)(1)(B) of the Patent Act) from the period of time between filing and issuance, to the extent the result exceeds three years. Furthermore, the Court concluded that continued examination time does not include time from allowance to issuance. The USPTO incorrectly included the time from allowance to issuance in its patent term adjustment calculation for this matter. As a result, an additional 134 days not credited to Patentee should be added to the patent term for the above-identified patent.

The above-identified patent **IS NOT** subject to a terminal disclaimer. The application that issued as the above-identified patent **WAS NOT** subject to circumstances constituting a failure to engage in reasonable efforts to conclude processing or examination of such application as set forth in 37 C.F.R. § 1.704.

Patentee has detailed above any circumstances during the prosecution of the present application that may constitute a failure to engage in reasonable efforts to conclude processing or examination of the application as set forth in 37 C.F.R. § 1.704.

As set forth above, Patentee's patent term adjustment should be **446 days**, and Patentee respectfully requests notification to that effect. The Commissioner is invited to contact the undersigned at (612) 373-6969 with any questions concerning this submission.

Respectfully submitted,

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 10-7-14 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

Electronic Patent Application Fee Transmittal

Application Number:	12825211
Filing Date:	28-Jun-2010
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Filer:	Mark Victor Muller/Julie Nelson
Attorney Docket Number:	303.B12US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Application for patent term adjustment	1455	1	200	200
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**200**

Electronic Acknowledgement Receipt

EFS ID:	20351809
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Mark Victor Muller/Julie Nelson
Filer Authorized By:	Mark Victor Muller
Attorney Docket Number:	303.B12US1
Receipt Date:	07-OCT-2014
Filing Date:	28-JUN-2010
Time Stamp:	15:57:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$200
RAM confirmation Number	2589
Deposit Account	190743
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303B12US1.pdf	85581 ab572f7b6809666293e8a12ffd439ccf7acf6f57	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal Letter	1	1
	Patent Term Adjustment Petition	2	4

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30195 4bff7729962f2d749328715f252cc0ace2361546	no	2

Warnings:

Information:

Total Files Size (in bytes):	115776

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.
Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.: 303.B12US1
Filed: June 28, 2010
Examiner: Wilner Jean Baptiste
Customer No.: 73115
Patent No.: 8,803,214

Serial No.: 12/825,211
Due Date: October 12, 2014
Group Art Unit: 2823
Confirmation No.: 1275
Issue Date: August 12, 2014

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X Application for Patent Term Adjustment Under 37 C.F.R § 1.705(b) (1 pg)

X Statement of Facts Under 37 C.F.R. § 1.705(b)(2) in Support of the Application for Patent Term Adjustment (2 pgs.)

X Authorization to charge Deposit Account No. 19-0743 in the amount of $200.00 as required under 37 C.F.R. § 1.18(e).

Please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

IN UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.: 8,803,214 Docket No: 303.B12US1

Issue Date: August 12, 2014 Patentee: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

OPAS
SEP 0 3 2014
PATENT & TRADEMARK OFFICE

REQUEST FOR CERTIFICATE OF CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450
ATTN: Certificate of Correction Branch

It is requested that a Certificate of Correction be issued correcting printing errors appearing in the above-identified United States patent. Two copies of the text of the Certificate in the suggested form are enclosed.

As the error is that of the Patent Office, it is believed that no fee is due.

Issuance of the Certificate of Correction would neither expand nor contract the scope of the claims as properly allowed, and re-examination is not required.

Respectfully submitted,

Customer Number: 26809

Date: August 27, 2014 By: _____

Russ Slifer
Reg. No. 39,838

CERTIFICATE UNDER 37 CFR § 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450, on this 27 day of August 2014

Janessa Lopez /Janessa Lopez/

Name Signature

PTO/SB/44 (02-01)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 8,803,214

DATED : August 12, 2014

INVENTOR(S) : Sanh D. Tang et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the first page, in column 2, in "Primary Examiner", line 1, delete "Olik Chaudhur" and insert - - Olik Chaudhuri - -, therefor.

PTO/SB/44 (02-01)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 8,803,214

DATED : August 12, 2014

INVENTOR(S) : Sanh D. Tang et al.

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the first page, in column 2, in "Primary Examiner", line 1, delete "Olik Chaudhur" and insert - - Olik Chaudhuri - -, therefor.

OPAP
SEP 0 3 2014
PATENT & TRADEMARK OFFICE

12/825211

COPY

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Examiner: Wilner Jean Baptiste

Patent No.: 8,803,214

Group Art Unit: 2823

Issue Date: August 12, 2014

Docket No: 303.B12US1

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Commissioner for Patents
Office of Patent Publication
ATTN: Certificate of Correction Branch

We are transmitting herewith the attached:

X Request for Certificate of Correction.
X Certificate of Correction Form - PTO-1050 (in duplicate)
X A return postcard.

Please charge any additional fees or credit overpayment to Deposit Account No. 13-3092.

Customer Number: 26809

Respectfully submitted,

Date: August 27, 2014 By: _____
Russ Slifer
Reg. No. 39,838

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents and Trademarks, P.O. Box 1450, Alexandria VA 22313-1450, on this 27 day of August 2014.

Janessa Lopez
Name

/Janessa Lopez/
Signature

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	08/12/2014	8803214	303.B12US1	1275

73115 7590 07/23/2014

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 312 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Sanh D. Tang, Boise, ID;
John K. Zahurak, Eagle, ID;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IPR2015-00369
YMTC EXHIBIT 1002
Page 27 of 382

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

73115 7590 03/31/2014
SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Lisa M. Lee	(Depositor's name)
/Lisa Lee/	(Signature)
June 30, 2014	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$0	$0	$1780	$0	06/30/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
JEAN BAPTISTE, WILNER	2823	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Schwegman, Lundberg
2 & Woessner, P.A.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Micron Technology, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Boise, Idaho

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 19-0743 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Viet Tong/ Date 6-30-14

Typed or printed name Viet V. Tong Registration No. 45,416

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sanh D. Tang et al.	Examiner: Wilner Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.: 73115		Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

REQUEST TO APPLY PREVIOUSLY PAID ISSUE FEE

Mail Stop Issue Fee
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

An issue fee for the above-identified application was previously paid on August 27, 2013. A petition under 37 CFR 1.313(c)(2) to withdraw the above-identified application from issue after payment of the issue fee was subsequently filed on September 26, 2013. Applicant received a decision, dated September 27, 2013, granting the petition to withdraw.

Applicant respectfully requests that the above-identified previously-paid issue fee be applied toward the fee required by the new Notice of Allowance dated March 31, 2014.

This request is being submitted together with the new Issue Fee Transmittal Form PTOL-85. Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743. Please direct any inquiries to the undersigned attorney at (612) 373-6969.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 6-30-14 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

VVT:CMG:lml

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Sanh D. Tang et al.	Examiner:	Wilner Baptiste
Serial No.:	12/825,211	Group Art Unit:	2823
Filed:	June 28, 2010	Docket No.:	303.B12US1
Customer No.:	73115	Confirmation No.:	1275
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

COMMUNICATION RE: FEE ADDRESS

Mail Stop Issue Fee
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

In response to the Notice of Allowance and Issue Fee Due, please record the Fee Address under the provisions of 37 CFR 1.363 as the following:

Customer Number 26809

which is associated with Micron Technology, Inc..

Please direct any inquiries to the undersigned attorney at (612) 373-6969.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 6-30-14 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

VVT:CMG:lm1

Electronic Acknowledgement Receipt

EFS ID:	19453799
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Mark Victor Muller/Lisa Lee
Filer Authorized By:	Mark Victor Muller
Attorney Docket Number:	303.B12US1
Receipt Date:	30-JUN-2014
Filing Date:	28-JUN-2010
Time Stamp:	15:35:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303B12US1IssueFee.pdf	307415 a6f0415400165f0aa7d791d9cf033e269f5804aa	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Issue Fee Payment (PTO-85B)	2	2
	Miscellaneous Incoming Letter	3	3
	Change of Address	4	4

Warnings:	
Information:	
Total Files Size (in bytes):	307415

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Sanh D. Tang et al.
Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010	Due Date:	June 30, 2014
Examiner:	Wilner Baptiste	Group Art Unit:	2823
Customer No.:	73115	Confirmation No.:	1275

Notice of Allowance Date: March 31, 2014

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following:

X Issue Fee Transmittal (Form PTOL-85).
X Request to Apply Previously Paid Issue Fee (1 pg.)
X Communication Re: Fee Address (1 page).

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A. By /Viet Tong/
Customer No.: 73115 Viet V. Tong
VVT:CMG:lm1 Reg. No. 45,416

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

73115 7590 03/31/2014
SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

07/01/2014 EEKUBAY2 00000020 190743 12825211

01 FC:1501 960.00 DA
02 FC:1508 820.00 DA

OPAP AKUMA-2 JUN 3 0 2014 PATENT & TRADEMARK OFFICE

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Lisa M. Lee	(Depositor's name)
	(Signature)
June 30, 2014	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$0	$0	$1780	$0	06/30/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
JEAN BAPTISTE, WILNER	2823	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Schwegman, Lundberg
2 & Woessner, P.A.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Micron Technology, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Boise, Idaho

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 19-0743 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ Applicant certifying micro entity status. See 37 CFR 1.29
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
☐ Applicant asserting small entity status. See 37 CFR 1.27
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
☐ Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Viet Tong/ Date 6-30-14

Typed or printed name Viet V. Tong Registration No. 45,416

YMTC EXHIBIT 1002
Page 34 of 382

07/01/2014 EEKUBAY2 00000020 190743 12825211
01 FC:1501 1780.00 CR

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

73115 7590 03/31/2014

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
JEAN BAPTISTE, WILNER	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$0	$0	$1780	$0	06/30/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

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P.O. BOX 2938
MINNEAPOLIS, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$0	$0	$1780	$0	06/30/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
JEAN BAPTISTE, WILNER	2823	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

73115 7590 03/31/2014

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
JEAN BAPTISTE, WILNER	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 266 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 266 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/825,211	Applicant(s) TANG ET AL.	
	Examiner WILNER JEAN BAPTISTE	Art Unit 2823	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/26/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-21*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 10/10/2013
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/WILNER JEAN BAPTISTE/ Examiner, Art Unit 2823	/OLIK CHAUDHURI/ Supervisory Patent Examiner, Art Unit 2823

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under Ex Parte Quayle, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 09/26/2013 has been entered.

Information Disclosure Statement

3. The information disclosure statements (IDS) were submitted on the following: 10/10/2013. The submissions are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

Allowable Subject Matter

4. Claims 1-21 are allowed.

5. **Reasons for Allowance**

The following is an examiner's statement of reasons for allowance:

The instant application is allowed for the same reasons that set forth in paragraph five (3) of the office action that was mailed on 05/28/2013.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILNER JEAN BAPTISTE whose telephone number is (571)270-7394. The examiner can normally be reached on M-F FROM 7:30 AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, OLIK CHAUDHURI can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/OLIK CHAUDHURI/
Supervisory Patent Examiner, Art Unit 2823

/WILNER JEAN BAPTISTE/
Examiner, Art Unit 2823

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	Art Unit
	WILNER JEAN BAPTISTE	2823

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner
H01L27/0688 H01L27/101 H01L27/11551 H01L27/11556 H01L27/11578 H01L27/2436	3/30/2014	wj
H01L29/66825 H01L29/66833 H01L29/7889 H01L29/7926	3/10/2014	wj
H01L45/04 H01L45/1226	3/10/2014	wj

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
257	314,E21.602,E29.255,E21.001	5/31/2012	wj
438	128, 309	5/31/2012	wj
365	189.11	12/20/2012	wj

SEARCH NOTES

Search Notes	Date	Examiner
East	5/31/2012	wj
East updated	12/20/2012	wj
East updated	5/8/2013	wj
East updated	3/10/2014	wj
CPC.class.	3/10/2014	wj
Google-Patents	3/10/2014	wj

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	314,E21.602,E29.255,E21.001	6/2/2013	wj

/W.J./ Examiner.Art Unit 2823	

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
365	185.07,185.11, 185.17	5/8/2013	wj
H01L27	0688,101,11551,11556,11578,2436	3/10/2014	wj
H01L29	66825,66833 ,7889,7926	3/10/2014	wj
H01L45	04 ,1226	3/10/2014	wj

/W.J./ Examiner.Art Unit 2823	

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1275

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/825,211	06/28/2010	257	2823	303.B12US1

APPLICANTS

INVENTORS

Sanh D. Tang, Boise, ID;
John K. Zahurak, Eagle, ID;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
07/01/2010

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /WILNER JEAN BAPTISTE/ Examiner's Signature	☐ Met after Allowance wj Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		ID	38	~~34~~ 21	5

ADDRESS

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402
UNITED STATES

TITLE

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

FILING FEE RECEIVED		
2558	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S50	14459	(Non-volatile near3 memory near3 devices) and (flash near3 memory near3 devices)	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:50
S51	37530	computers and (electronic near2 devices) and (store near2 information)	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:50
S52	10425	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:50
S53	550	S50 and S51	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:51
S54	8	S52 and S53	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:51
S67	7368	(H01L27/0688 H01L27/101 H01L27/11551 H01L27/11556 H01L27/11578 H01L27/2436).cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:02
S68	158	(H01L27/249).cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:02
S69	5723	(H01L29/66825 H01L29/66833 H01L29/7889 H01L29/7926).cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:03
S70	3020	(H01L45/04 H01L45/1226).cpc.	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:03
S71	14295	S67 S68 S69 S70	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:03
S72	322921	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:03
S73	12382	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same	US-PGPUB; USPAT;	OR	ON	2014/03/10 15:04

		device))	UPAD			
S74	3769	S72 and S73	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:05
S75	510	S71 and S74	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:05
S76	7218	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:05
S77	3	S75 and S76	US-PGPUB; USPAT; UPAD	OR	ON	2014/03/10 15:07

3/ 10/ 2014 3:40:14 PM
C:\ Users\ wjeanbaptiste\ Documents\ EAST\ Workspaces\ 12-825211 (three dimensional memory and method of forming).wsp

Modified form PTO/SB/08A(04-07) OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (Use as many sheets as necessary)	*Complete if Known*	
	Application Number	12/825,211
	Filing Date	June 28, 2010
	First Named Inventor	Sanh D. Tang
	Group Art Unit	2823
	Examiner Name	Wilner Baptiste
Sheet 1 of 1	Attorney Docket No: 303.B12US1	

US PATENT DOCUMENTS			
Examiner Initial *	**USP Document Number**	**Publication Date**	**Name of Patentee or Applicant of cited Document**

FOREIGN PATENT DOCUMENTS				
Examiner Initial *	**Foreign Document Number**	**Publication Date**	**Name of Patentee or Applicant of cited Document**	**T 1**

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS		
Examiner Initial *	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T 1**
	TANAKA, H., et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory", IEEE Symposium on VLSI Technology, (2007), 14-15	

EXAMINER	/Wilner Jean Baptiste/	DATE CONSIDERED	03/10/2014

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /W.J./

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

CPC		
Symbol	**Type**	**Version**

CPC Combination Sets				
Symbol	**Type**	**Set**	**Ranking**	**Version**

/WILNER JEAN BAPTISTE/ Examiner.Art Unit 2823 (Assistant Examiner)	3/10/2014 (Date)	**Total Claims Allowed:** 21	
/OLIK CHAUDHURI/ Supervisory Patent Examiner.Art Unit 2823 (Primary Examiner)	03/21/2014 (Date)	O.G. Print Claim(s) 9	O.G. Print Figure 4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	204

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
257	316				
365	185.26				

INTERNATIONAL CLASSIFICATION														
CLAIMED					**NON-CLAIMED**									
H	0	1	L	27 / 06 (2006.01.01)					
H	0	1	L	27 / 10 (2006.01.01)					
H	0	1	L	27 / 115 (2006.01.01)					
H	0	1	L	29 / 66 (2006.01.01)					

/WILNER JEAN BAPTISTE/ Examiner.Art Unit 2823	3/10/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	21	
/OLIK CHAUDHURI/ Supervisory Patent Examiner.Art Unit 2823	03/21/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	9	4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17	---	33										
2	2	18	18	---	34										
3	3	19	19												
8	4	21	20												
4	5	20	21												
5	6	---	22												
6	7	---	23												
7	8	---	24												
9	9	---	25												
10	10	---	26												
11	11	---	27												
12	12	---	28												
13	13	---	29												
14	14	---	30												
15	15	---	31												
16	16	---	32												

/WILNER JEAN BAPTISTE/ Examiner.Art Unit 2823	3/10/2014	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	21	
/OLIK CHAUDHURI/ Supervisory Patent Examiner.Art Unit 2823	03/21/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	9	4

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	12/825211.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 16:07
S2	15024	(257/314,E21.602,E29.255,E21.001).ccls. (438/128,309).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:00
S3	233430	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:09
S4	9410	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:10
S5	2242	S3 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:10
S6	59	S2 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:11
S7	7282	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:53

YMTC EXHIBIT 1002

		hole))				
S8	11	S5 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:54
S9	38	S4 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:59
S10	4266	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices)) and ((vias or holes or grooves) with dielectrics)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 18:07
S11	138	S7 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 18:07
S12	233430	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S13	9410	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S14	2242	S12 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S15	4266	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices)) and ((vias or holes or grooves) with dielectrics)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S16	183	S14 and S15	US-PGPUB; USPAT;	OR	ON	2012/05/30 20:20

YMTC EXHIBIT 1002

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S17	183	S13 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:21
S18	138	S15 and ((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:22
S19	7282	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:38
S20	2541	438/128.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:39
S21	13	S19 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:40
S22	854	438/309.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:42
S23	317	Tang-Sanh-D.in. or Zahurak-John-K.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:43
S24	1	S19 and S23	US-PGPUB;	OR	ON	2012/05/30

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Page 54 of 382

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			20:44
S25	13	S19 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:44
S26	2	12/047414.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 11:09
S27	3	("20040206996" | "20050133851" | "20080179659").PN. OR ("7906818").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/05/31 11:13
S28	7289	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:51
S29	735	S28 and ((double adj gate) or (double near2 gate) or (double same gate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:53
S30	31	S29 and ((257/314,E21.602,E29.255,E21.001).ccls. or (438/128,309).ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:54
S31	1	08/985182.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 15:12
S32	0	13/049629.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/03 23:48

S33	0	13/049699.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:18
S34	0	13/311276.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:45
S35	11325	((metallization same (integrated adj circuit)) or (metallization near3 (integrated adj circuit))) and "257"/$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:56
S36	6768	S35 and copper	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:56
S37	68	S36 and (nanoparticles or nano-paticles or (nano adj particles))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:58
S38	2201	365/189.11.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:30
S39	13021	(non-volatile memory cell) and (first near3 memory near3 element)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:33
S40	75	(first near3 memory near3 element) and (ring near2 shape)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:34
S41	45	S38 and S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2012/12/19 23:35

			DERWENT; IBM_TDB			
S42	10734	(THREE near3 DIMENSIONAL near3 MEMORY) or (3-D near2 MEMORY)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:38
S43	528	S39 and S42	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:39
S44	6	S40 and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:39
S45	14315	(Non-volatile near3 memory near3 devices) and (flash near3 memory near3 devices)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:07
S46	37052	computers and (electronic near2 devices) and (store near2 information)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:08
S47	528	S45 and S46	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:09
S48	11288	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:14
S49	8	S47 and S48	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:14
S55	2	"20110316063"	US-PGPUB; USPAT; USOCR;	OR	ON	2014/03/10 14:47

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Page 57 of 382

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S56	15334	(H01L27/0688 H01L27/101 H01L27/11551 H01L27/11556 H01L27/11578 H01L27/2436).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:50
S57	350	(H01L27/249).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:50
S58	10626	(H01L29/66825 H01L29/66833 H01L29/7889 H01L29/7926).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:51
S59	6565	(H01L45/04 H01L45/1226).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:52
S60	28939	S56 S57 S58 S59	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:52
S61	328144	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:53
S62	13969	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:53
S63	3783	S61 and S62	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:54
S64	1047	S60 and S62	US-PGPUB;	OR	ON	2014/03/10

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			14:54
S65	8938	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:54
S66	12	S64 and S65	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2014/03/10 14:57

3/10/2014 3:39:32 PM
C:\Users\wjeanbaptiste\Documents\EAST\Workspaces\12-825211 (three dimensional memory and method of forming).wsp

Modified form PTO/SB/08A(04-07) OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (Use as many sheets as necessary)	*Complete if Known*	
	Application Number	12/825,211
	Filing Date	June 28, 2010
	First Named Inventor	Sanh D. Tang
	Group Art Unit	2823
	Examiner Name	Wilner Baptiste
Sheet 1 of 1	Attorney Docket No: 303.B12US1	

US PATENT DOCUMENTS			
Examiner Initial *	**USP Document Number**	**Publication Date**	**Name of Patentee or Applicant of cited Document**

FOREIGN PATENT DOCUMENTS				
Examiner Initial *	**Foreign Document Number**	**Publication Date**	**Name of Patentee or Applicant of cited Document**	**T 1**

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS		
Examiner Initial *	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T 1**
	TANAKA, H., et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory", IEEE Symposium on VLSI Technology, (2007), 14-15	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt

EFS ID:	17098908
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Marc S. Hanish/Patrick McNally
Filer Authorized By:	Marc S. Hanish
Attorney Docket Number:	303.B12US1
Receipt Date:	10-OCT-2013
Filing Date:	28-JUN-2010
Time Stamp:	17:49:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		12825211_SIDS_10-10-13.pdf	200925 bee5084fcd07a48e3a240d0ca9410ac74dffdd76	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Transmittal Letter	2	3
	Information Disclosure Statement (IDS) Form (SB08)	4	4

Warnings:					
Information:					
2	Non Patent Literature	0001_tanaka_p14_2007.pdf	673448 f9c7eef4e8a9205628b932d7ee7c4880de9b3d3f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	874373		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010	Due Date:	N/A
Examiner:	Wilner Baptiste	Group Art Unit:	2823
Customer No.:	73115	Confirmation No.:	1275

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.) Copies of Cited References (1).

If not provided for in a separate paper filed herewith, please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sanh D. Tang et al.	Examiner:	Wilner Baptiste
Serial No.:	12/825,211	Group Art Unit:	2823
Filed:	June 28, 2010	Docket:	303.B12US1
Customer No.:	73115	Confirmation No.:	1275
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq*., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached PTO 1449 Form be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the PTO 1449 Form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. § 1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed after filing of the application or after the filing of the most recent RCE, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. § 1.98(a)(2), copies of cited U.S. Patents and Published Applications, and Non-Published Applications identifiable by USPTO Serial Number, are no longer required to be provided to the Office. Applicants acknowledge the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R § 1.98(a)(2).

The Examiner is invited to contact the undersigned at the telephone number indicated if there are any questions regarding this communication.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 10-10-13 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

VVT:pjm

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

PATENT WITHDRAWAL NOTICE

DATE WITHDRAWN	WITHDRAWAL NUMBER
10/1/2013	23326

The following application has been **WITHDRAWN** from the

10/1/2013 issue.

SERIAL NO.	PATENT NUMBER
12825211	8546864
DRAWINGS	**CLASS**
0	/

TITLE

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

NAME AND ADDRESS

SANH D. TANG, ET AL
BOISE, ID

REASON FOR WITHDRAWAL

Applicant's petition to withdraw - Granted.

APPROVED

/Kimberly Terrell/, Manager

Patent Publication Branch
Office of Data Management

FORM PTO-302 -- (REV. 05-2009)

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov



SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS MN 55402

In re Application of	:	
Sanh D. Tang et al	:	
Application No. 12/825,211	:	DECISION ON PETITION
Filed: June 28, 2010	:	UNDER 37 CFR 1.313(c)
Attorney Docket No. 303.B12US1	:	

This is a decision on the petition under 37 CFR 1.313(c), filed September 26, 2013, to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED**.

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). *See* 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid on August 27, 2013, cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.[1]

Telephone inquiries should be directed to the undersigned at (571) 272-3208.

This application is being referred to Technology Center AU 2823 for processing of the request for continued examination under 37 CFR 1.114 and for consideration of the concurrently filed amendment.

/Karen Creasy/
Karen Creasy
Paralegal Specialist
Office of Petitions

[1] *The request to apply the issue fee to the new Notice may be satisfied by completing and returning the new Part B – Fee(s) Transmittal Form (along with any balance due at the time of submission). Petitioner is advised that the Issue Fee Transmittal Form must be completed and timely submitted to avoid abandonment of the application.*

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Date : September 27, 2013

TO : Director, Office of Patent Publication

FROM : Office of Petitions

SUBJECT : Withdrawal from Issue of **Application No. 12/825,211**

Applicant(s) : Sanh D. Tang et al
Application No. : 12/825,211
Filed : June 28, 2010

The above-identified application has been assigned Patent No. 8,546,864 and an issue date of October 1, 2013.

It is hereby directed that this application be withdrawn from issue at the request of the applicant. Do not refund the issue fee.

The following erratum should be published in the Official Gazette if the above-identified application is published in the OG of October 1, 2013:

"All reference to Patent No. 8,546,864 to Sanh D. Tang et al of Idaho for THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME appearing in the Official Gazette of October 1, 2013 should be deleted since no patent was granted."

/Karen Creasy/
Karen Creasy
Paralegal Specialist
Office of Petitions

cc: Paul Harrison
Mary Louise McAskill
Niomi Farmer
Mary E. Johnson (Cookie)
Brad Harris
Kim Terrell
Lamont Fletcher

REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL		
	Application Number	12/825,211
	Filing Date	June 28, 2010
	First Named Inventor	Sanh D. Tang
	Confirmation Number	1275
	Group Art Unit	2823
	Examiner Name	Wilner Baptiste
	Attorney Docket Number	303.B12US1
	Customer No.	73115

This is a Request for Continued Examination (RCE) under 37 C.F.R § 1.114 of the above-identified application entitled
THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

1. Submission required under 37 C.F.R. § 1.114:
   - X Preliminary Amendment (8 pages) is enclosed.
   - X Petition to Withdraw from Issue (1 pg)

2. Fees
   - X Authorization to charge deposit account 19-0743 in the amount of $1200.00 to pay the RCE filing fee required under 37 C.F.R. § 1.17(e).
   - X Authorization to charge deposit account 19-0743 in the amount of $140.00 to pay the petition fee required under 37 C.F.R. § 1.17(h).

The Commissioner is hereby authorized to charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sanh D. Tang et al.	Examiner: Wilner Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.: 73115		Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

Petition to Withdraw From Issue Under 37 C.F.R. 1.313(c)

Mail Stop 313(c)
Commissioner for Patents
Office of Petitions
Madison West Building, 7th Floor
600 Dulany Street
Alexandria, VA 22313

The above-referenced patent application was allowed on May 28, 2013, and the Issue Fee was paid on August 27, 2013. Applicant respectfully requests that the above-identified patent application be withdrawn from Issue so the attached amendments can be entered. Additionally, Applicant has enclosed a Request for Continued Examination transmittal and the requisite fee, which Applicant wishes to enter even date herewith.

Authorization is hereby given to charge the petition fee of $140.00 as set forth in § 1.17(h) which is required pursuant to 37 C.F.R. § 1.313(a), to Deposit Account 19-0743. Please charge any additional fees or credit overpayment to Deposit Account 19-0743.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully Submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402--0938
(612) 373-6969

Date September 26, 2013 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sanh D. Tang et al.	Examiner: Wilner Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.: 73115		Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

PRELIMINARY AMENDMENT

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Prior to taking up this application for examination, please enter the following amendments:

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a substrate of a memory device;

a plurality of first memory cells located in a first device level of the memory device over the substrate;

a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate; and

data lines configured to be selectively coupled to a common source and the memory cells through [[a]] conductive material.

2. (Currently Amended) The apparatus of claim 1, wherein ~~each of~~ the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. (Original) The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory

cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. (Currently Amended) An apparatus comprising:

a plurality of first memory cells located in a first device level of a memory device;

a plurality of second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate, wherein ~~each of~~ the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction;

a common source; and

data lines configured to be selectively coupled to the common source and the <u>first and second</u> memory cells through [[a]] conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. (Original) The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

6. (Original) The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

7. (Currently Amended) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

8. (Currently Amended) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

9. (Currently Amended) An apparatus comprising:

a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device;

a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level;

a conductive material extending through the first and second memory elements; and

a data ~~lines~~ line configured to be selectively coupled to a common source and the first and second memory cells through [[a]] the conductive material.

10. (Currently Amended) The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in the first device level of the memory device ~~in which the first and second memory cells are located~~; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in the second device level of the memory device.

11. (Currently Amended) The apparatus of claim 10, wherein each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. (Currently Amended) The apparatus of claim 11, wherein each of the first and second memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. (Currently Amended) The apparatus of claim 9, ~~further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells,~~ wherein the data line is located between the substrate and the first memory cell.

14. (Currently Amended) The apparatus of claim 9, ~~further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells,~~ wherein the first and second memory cells are located between the substrate and the data line.

15. (Previously Presented) An apparatus comprising:

a substrate of a memory device;

a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

16. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

17. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.

18. (Original) The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.

19. (Original) The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

20. (Previously Presented) An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element;

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric;

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

21. (Currently Amended) The apparatus of claim 15, further comprising:

~~a substrate; and~~

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

CONCLUSION

It is respectfully submitted that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the undersigned at (612) 373-6969 to facilitate prosecution of this Application.

If necessary, please charge any additional fees or deficiencies, or credit any overpayments to Deposit Account No. 19-0743.

Respectfully Submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402--0938
(612) 373-6969

Date September 26, 2013 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

Electronic Patent Application Fee Transmittal

Application Number:	12825211
Filing Date:	28-Jun-2010
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Filer:	Suneel Arora/Amy Moriarty
Attorney Docket Number:	303.B12US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Petition fee- 37 CFR 1.17(h) (Group III)	1464	1	140	140
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
		Total in USD ($)		**1340**

Electronic Acknowledgement Receipt

EFS ID:	16966568
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Suneel Arora/Amy Moriarty
Filer Authorized By:	Suneel Arora
Attorney Docket Number:	303.B12US1
Receipt Date:	26-SEP-2013
Filing Date:	28-JUN-2010
Time Stamp:	15:19:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1340
RAM confirmation Number	2159
Deposit Account	190743
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303b12us1SIGNEDrce.pdf	142734 dd8216776a9d8fcc3ce6cab62e1b259995c9bbb2	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Request for Continued Examination (RCE)	1	1
	Petition to Withdraw from Issue	2	2
	Preliminary Amendment	3	3
	Claims	4	9
	Applicant Arguments/Remarks Made in an Amendment	10	10

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	32109 baa8d36ce554422e13658977d45f5ce55552cad0	no	2

Warnings:

Information:

Total Files Size (in bytes):	174843

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/825,211	Filing Date 06/28/2010	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **09/26/2013**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 21	Minus	** 34	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LAJUAN HICKSON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	10/01/2013	8546864	303.B12US1	1275

73115 7590 09/11/2013

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 297 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Sanh D. Tang, Boise, ID;
John K. Zahurak, Eagle, ID;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

73115 7590 05/28/2013
SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Lisa M. Lee	(Depositor's name)
	(Signature)
August 27, 2013	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	08/28/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
JEAN BAPTISTE, WILNER	2823	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Schwegman, Lundberg
2 & Woessner, P.A.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE	(B) RESIDENCE: (CITY and STATE OR COUNTRY)
Micron Technology, Inc.	Boise, Idaho

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 19-0743 (enclose an extra copy of this form).

YMTC EXHIBIT 1002
Page 86 of 382

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

❑ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

❑ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Viet Tong/ Date 8-27-13

Typed or printed name Viet V. Tong Registration No. 45,416

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sanh D. Tang et al.	Examiner: Wilner Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.:	73115	Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

COMMUNICATION RE: FEE ADDRESS

Mail Stop Issue Fee
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

In response to the Notice of Allowance and Issue Fee Due, please record the Fee Address under the provisions of 37 CFR 1.363 as the following:

Customer Number 26809

which is associated with Micron Technology, Inc..

Please direct any inquiries to the undersigned attorney at (612) 373-6969.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 8-27-13 By /Viet Tong/
Viet V. Tong
Reg. No. 45,416

VVT:CMG:lm1

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 27th day of August, 2013.

Lisa M. Lee
Name

/Lisa Lee/
Signature

Electronic Patent Application Fee Transmittal

Application Number:	12825211
Filing Date:	28-Jun-2010
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Filer:	Ann Marie McCrackin/Lisa Lee
Attorney Docket Number:	303.B12US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2080**

Electronic Acknowledgement Receipt

EFS ID:	16696680
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Ann Marie McCrackin/Lisa Lee
Filer Authorized By:	Ann Marie McCrackin
Attorney Docket Number:	303.B12US1
Receipt Date:	27-AUG-2013
Filing Date:	28-JUN-2010
Time Stamp:	14:12:50
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2080
RAM confirmation Number	496
Deposit Account	190743
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303B12US1.pdf	423119 a8f106baf781740bb5496dc38935a0fdce7dc85b	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Transmittal Letter	1	1
	Issue Fee Payment (PTO-85B)	2	3
	Change of Address	4	4

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	31980 81264a1fd36d703e1fed27aa8a25e096ab956e34	no	2

Warnings:

Information:

Total Files Size (in bytes):	455099

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010	Due Date:	August 28, 2013
Examiner:	Wilner Baptiste	Group Art Unit:	2823
Customer No.:	73115	Confirmation No.:	1275

Notice of Allowance Date: May 28, 2013

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following:

X Authorization to charge Deposit 19-0743 in the amount of $1780 to cover the Large Entity Issue Fee Payment.
X Authorization to charge Deposit 19-0743 in the amount of $300.00 to cover the Publication Fee Payment.
X Issue Fee Transmittal (Form PTOL-85).
X Communication Re: Fee Address (1 page).

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A. By /Viet Tong/
Customer No.: 73115 Viet V. Tong
VVT:CMG:lm1 Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 27th day of August, 2013.

Lisa M. Lee
Name

/Lisa Lee/
Signature

Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	12/825,211	TANG ET AL.	
	Examiner	Art Unit	
	WILNER JEAN BAPTISTE	2823	

All participants (applicant, applicant's representative, PTO personnel):

(1) *WILNER JEAN BAPTISTE*. (3)_____.

(2) *Viet, Tong*. (4)_____.

Date of Interview: *07 May 2013*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1,2 and 9*.

Identification of prior art discussed: *Pekny US 2009/0230454 A1* .

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

The issues were about a proposed amendment to claims 1, 2 and 9.Viet,Tong, representative for applicants, has authorized the changes in the claim as shown in the Examiner's Amendment. It is not necessary for applicants to provide a separate record of the substance of the interview, since the interview resulted in the allowance of the application.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/WILNER JEAN BAPTISTE/ Examiner, Art Unit 2823	

YMTC EXHIBIT 1002
Page 94 of 382

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

73115 7590 05/28/2013

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER
JEAN BAPTISTE, WILNER

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/28/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	08/28/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

YMTC EXHIBIT 1002
Page 95 of 382

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

73115 7590 05/28/2013
SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

TITLE OF INVENTION: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1780	$300	$0	$2080	08/28/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
JEAN BAPTISTE, WILNER	2823	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

YMTC EXHIBIT 1002
Page 96 of 382

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29	NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
❑ Applicant asserting small entity status. See 37 CFR 1.27	NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
❑ Applicant changing to regular undiscounted fee status.	NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

73115 7590 05/28/2013

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
JEAN BAPTISTE, WILNER	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/28/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 202 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 202 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

YMTC EXHIBIT 1002
Page 98 of 382

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/825,211	Applicant(s) TANG ET AL.	
	Examiner WILNER JEAN BAPTISTE	Art Unit 2823	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *4/30/2013*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-21*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

   Interim copies:

   a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☒ Interview Summary (PTO-413), Paper No./Mail Date *05/07/2013* .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/WILNER JEAN BAPTISTE/
Examiner, Art Unit 2823

YMTC EXHIBIT 1002

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Viet, Tong, on 05/07/2013.

Amend the claims as follows:

- Claim 1, **line 10**, delete "and"; **line 13**, before the period insert --- and data lines configured to be selectively coupled to a common source and the memory cells through a conductive material---.

- Claim 2, **line 3**, after "second direction" delete "further comprising: a common source; and data lines configured to be selectively coupled to the common source and the memory cells through a conductive material".

- Claim 9, **line 8**, delete "and", **line 9**, before the period insert --- and data lines configured to be selectively coupled to a common source and the memory cells through a conductive material---.

Allowable Subject Matter

2. Claims 1-21 are allowed over the prior art of the record.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance:

The prior art of record neither anticipates nor renders obvious the claimed subject matter of the instant application as a whole either taken alone or in combination, in particular, prior art of record does not teach the following:

- a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate; and data lines configured to be selectively coupled to a common source and the memory cells through a conductive material, as recited in claims 1, 4, 9 and 20.

- a second dielectric formed on a side of the first memory element and on a side of the second memory element; and a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric, as recited in claim 15.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILNER JEAN BAPTISTE whose telephone number is (571)270-7394. The examiner can normally be reached on M-F FROM 7:30 AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, OLIK CHAUDHURI can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WILNER JEAN BAPTISTE/

Examiner, Art Unit 2823

05/07/2013

/WALTER H SWANSON/
Primary Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 12/825,211	Applicant(s)/Patent Under Reexamination TANG ET AL.	
	Examiner WILNER JEAN BAPTISTE	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0014858	01-2009	Boon et al.	257/686
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

OK TO ENTER: /W.J./ 05/08/2013

EXPEDITED PROCEDURE-EXAMINING GROUP 2823

S/N 12/825,211 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sanh D. Tang et al.	Examiner: Wilner Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.: 73115		Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

AMENDMENT & RESPONSE UNDER 37 C.F.R. 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Final Office Action dated February 1, 2013, please amend the application as follows, and consider the appended remarks.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1275

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/825,211	06/28/2010 RULE	257	2823	303.B12US1

APPLICANTS

Sanh D. Tang, Boise, ID;
John K. Zahurak, Eagle, ID;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
07/01/2010

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /WILNER JEAN BAPTISTE/ Examiner's Signature	☐ Met after Allowance wj Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		ID	38	~~34~~ 21	5

ADDRESS

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402
UNITED STATES

TITLE

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
2258	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

CPC				
Symbol			**Type**	**Version**
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CPC Combination Sets						
Symbol			**Type**	**Set**	**Ranking**	**Version**
		/				
		/				

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	314

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
257	E21.602	E29.255				
365	185.17	185.05				

INTERNATIONAL CLASSIFICATION

CLAIMED					NON-CLAIMED				
H	0	1	L	29 / 76 (2006.0)					
G	1	1	C	11 / 34 (2006.0)					
G	1	1	C	16 / 04 (2006.01.01)					

/WILNER JEAN BAPTISTE/ Examiner.Art Unit 2823 (Assistant Examiner)	05/08/2013 (Date)	**Total Claims Allowed:** 21
(Primary Examiner)	(Date)	O.G. Print Claim(s): 9 / O.G. Print Figure: 4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

/WILNER JEAN BAPTISTE/ Examiner.Art Unit 2823	05/08/2013	**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	21	
		O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	9	4

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17	---	33										
2	2	18	18	---	34										
3	3	19	19												
8	4	21	20												
4	5	20	21												
5	6	---	22												
6	7	---	23												
7	8	---	24												
9	9	---	25												
10	10	---	26												
11	11	---	27												
12	12	---	28												
13	13	---	29												
14	14	---	30												
15	15	---	31												
16	16	---	32												

/WILNER JEAN BAPTISTE/ Examiner.Art Unit 2823	05/08/2013	**Total Claims Allowed:**
(Assistant Examiner)	(Date)	21
		O.G. Print Claim(s) / O.G. Print Figure
(Primary Examiner)	(Date)	9 / 4

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	Art Unit
	WILNER JEAN BAPTISTE	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2012	12/20/2012	05/08/2013						
1	1	✓	=	=						
2	2	✓	=	=						
3	3	✓	=	=						
8	4	✓	=	=						
4	5	✓	=	=						
5	6	✓	=	=						
6	7	✓	=	=						
7	8	✓	=	=						
9	9	✓	✓	=						
10	10	✓	✓	=						
11	11	✓	✓	=						
12	12	✓	✓	=						
13	13	✓	✓	=						
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15	15	✓	=	=						
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---	31	N	-	-						
---	32	N	-	-						
---	33	N	-	-						
---	34	N	-	-						

YMTC EXHIBIT 1002
Page 111 of 382

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L11	14459	(Non-volatile near3 memory near3 devices) and (flash near3 memory near3 devices)	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:50
L12	37530	computers and (electronic near2 devices) and (store near2 information)	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:50
L13	10425	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:50
L14	550	11 and 12	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:51
L15	8	13 and 14	US-PGPUB; USPAT; UPAD	OR	ON	2013/05/08 10:51

5/8/2013 11:17:42 AM
C:\Users\wjeanbaptiste\Documents\EAST\Workspaces\12-825211 (three dimensional memory and method of forming).wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	14315	(Non-volatile near3 memory near3 devices) and (flash near3 memory near3 devices)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:07
L7	37052	computers and (electronic near2 devices) and (store near2 information)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:08
L8	528	6 and 7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:09
L9	11288	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:14
L10	8	8 and 9	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/05/08 10:14
S1	1	12/825211.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 16:07
S2	15024	(257/314,E21.602,E29.255,E21.001).ccls. (438/128,309).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:00
S3	233430	((Non-volatile adj memory adj devices) or	US-PGPUB;	OR	ON	2012/05/30

YMTC EXHIBIT 1002

		(Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			17:09
S4	9410	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:10
S5	2242	S3 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:10
S6	59	S2 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:11
S7	7282	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:53
S8	11	S5 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:54
S9	38	S4 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:59
S10	4266	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices)) and ((vias or holes or grooves) with dielectrics)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 18:07
S11	138	S7 and S10	US-PGPUB; USPAT;	OR	ON	2012/05/30 18:07

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Page 114 of 382

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S12	233430	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S13	9410	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S14	2242	S12 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S15	4266	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices)) and ((vias or holes or grooves) with dielectrics)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S16	183	S14 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S17	183	S13 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:21
S18	138	S15 and ((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:22
S19	7282	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first	US-PGPUB; USPAT; USOCR;	OR	ON	2012/05/30 20:38

		same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S20	2541	438/128.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:39
S21	13	S19 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:40
S22	854	438/309.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:42
S23	317	Tang-Sanh-D.in. or Zahurak-John-K.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:43
S24	1	S19 and S23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:44
S25	13	S19 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:44
S26	2	12/047414.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 11:09
S27	3	("20040206996" | "20050133851" | "20080179659").PN. OR ("7906818").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/05/31 11:13
S28	7289	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3	US-PGPUB; USPAT;	OR	ON	2012/05/31 14:31

		gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S29	735	S28 and ((double adj gate) or (double near2 gate) or (double same gate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:53
S30	31	S29 and ((257/314,E21.602,E29.255,E21.001).ccls. or (438/128,309).ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:54
S31	1	08/985182.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 15:12
S32	0	13/049629.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/03 23:48
S33	0	13/049699.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:18
S34	0	13/311276.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:45
S35	11325	((metallization same (integrated adj circuit)) or (metallization near3 (integrated adj circuit))) and "257"/$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:56
S36	6768	S35 and copper	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2012/06/04 00:56

			EPO; JPO; DERWENT; IBM_TDB			
S37	68	S36 and (nanoparticles or nano-paticles or (nano adj particles))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/06/04 00:58
S38	2201	365/189.11.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:30
S39	13021	(non-volatile memory cell) and (first near3 memory near3 element)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:33
S40	75	(first near3 memory near3 element) and (ring near2 shape)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:34
S41	45	S38 and S39	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:35
S42	10734	(THREE near3 DIMENSIONAL near3 MEMORY) or (3-D near2 MEMORY)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:38
S43	528	S39 and S42	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:39
S44	6	S40 and S43	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/12/19 23:39

C:\ Users\ wjeanbaptiste\ Documents\ EAST\ Workspaces\ 12-825211 (three dimensional memory and method of forming).wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	Art Unit
	WILNER JEAN BAPTISTE	2823

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	314,E21.602,E29.255,E21.001	5/31/2012	wj
438	128, 309	5/31/2012	wj
365	189.11	12/20/2012	wj

SEARCH NOTES		
Search Notes	Date	Examiner
East	5/31/2012	wj
East updated	12/20/2012	wj
East updated	5/8/2013	wj

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	314,E21.602,E29.255,E21.001	6/2/2013	wj
365	185.07,185.11, 185.17	5/8/2013	wj

/W.J./ Examiner.Art Unit 2823	

YMTC EXHIBIT 1002
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EXPEDITED PROCEDURE-EXAMINING GROUP 2823

S/N 12/825,211 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sanh D. Tang et al.	Examiner: Wilner Baptiste	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.: 73115		Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

AMENDMENT & RESPONSE UNDER 37 C.F.R. 1.116

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Final Office Action dated February 1, 2013, please amend the application as follows, and consider the appended remarks.

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a substrate of a memory device;

a plurality of first memory cells located in a first device level of the memory device over the substrate;

a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the ~~first~~ second device level;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate.

2. (Original) The apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. (Original) The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory

cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. (Previously Presented) An apparatus comprising:

a plurality of first memory cells located in a first device level of a memory device;

a plurality of second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction;

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. (Original) The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

6. (Original) The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

7. (Original) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

8. (Original) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

9. (Currently Amended) An apparatus comprising:

a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device;

a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level; and

a conductive material extending through the first and second memory elements.

10. (Currently Amended) The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in [[a]] the first device level of [[a]] the memory device in which the first and second memory cells are located; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in [[a]] second device level of the memory device.

11. (Original) The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. (Original) The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. (Original) The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell.

14. (Original) The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

15. (Currently Amended) An apparatus comprising:

a substrate of a memory device;

a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the ~~first~~ second device level;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

16. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

17. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.

18. (Original) The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.

19. (Original) The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

20. (Previously Presented) An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element;

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

21. (Original) The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

22.-34. (Canceled)

REMARKS

This communication responds to the Final Office Action dated February 1, 2013.

Claims 1, 9, 10, and 15 are amended. Claims 22-34 were previously canceled. No claims are added. Thus, claims 1-21 are now pending in this application.

It is noted that unless otherwise stated herein, amendments to the claims have been made to clarify meaning, correct typographical errors, provide proper antecedent basis, and/or provide consistent terminology, and not for reasons related to patentability.

Allowed claims 1 and 15 are amended only to correct an obvious typographical error. The amendment does not alter the scope of claims 1 and 15.

The Rejection of Claims Under § 103

Claims 9-14 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pekny US 2009/0230454 A1 as previously applied. This rejection is respectfully traversed in view of the following.

Independent claim 9 is amended to include elements similar to those of allowed claim 1, such as "the first memory element located in a first device level of a memory device" and "the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level". Accordingly, reconsideration, withdrawal of the rejection, and allowance of claim 20 and its dependent claim 10-14 is respectfully requested.

Allowable Subject Matter

Claims 1-8 and 15-21 were allowed.

The undersigned thanks the Examiner for the allowance of claims 1-8 and 15-21.

CONCLUSION

It is respectfully submitted that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the undersigned at (612) 373-6969 to facilitate prosecution of this Application.

If necessary, please charge any additional fees or deficiencies, or credit any overpayments to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402--0938
(612) 373-6969

Date April 30, 2013 By /Viet Tong/
Viet V. Tong
Reg. No. 45,416

Electronic Acknowledgement Receipt

EFS ID:	15653347
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Suneel Arora/Amy Moriarty
Filer Authorized By:	Suneel Arora
Attorney Docket Number:	303.B12US1
Receipt Date:	30-APR-2013
Filing Date:	28-JUN-2010
Time Stamp:	16:08:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303b12us1SIGNEDfoa.pdf	75279 50acc23efc67d9a48e028bbddce93c12748a485d	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment After Final	2	2
	Claims	3	8
	Applicant Arguments/Remarks Made in an Amendment	9	10
Warnings:			
Information:			
	Total Files Size (in bytes):	75279	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010	Due Date:	May 1, 2013
Examiner:	Wilner Baptiste	Group Art Unit:	2823
Customer No.:	73115	Confirmation No.:	1275

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X Amendment and Response under 37 C.F.R. § 1.116 (9 pgs.)

If not provided for in a separate paper filed herewith, please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/825,211	Filing Date 06/28/2010	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)		
	04/30/2013	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 21	Minus	** 34	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DOROTHY BELL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/825,211	Filing Date 06/28/2010	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **03/20/2013**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/VICTORIA BROWN/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

73115 7590 02/01/2013

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
JEAN BAPTISTE, WILNER	
ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
02/01/2013	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@slwip.com
SLW@blackhillsip.com

Office Action Summary	Application No.	Applicant(s)	
	12/825,211	TANG ET AL.	
	Examiner	Art Unit	
	WILNER JEAN BAPTISTE	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2012*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-21* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *1-8 and 15-21* is/are allowed.

7)☒ Claim(s) *9-14* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *21 March 2011* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

YMTC EXHIBIT 1002
Page 136 of 382

DETAILED ACTION

Claim Objections

1. The claim objection set forth in the prior Office action has been withdrawn in response to Applicant's amendments to claim 1.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained through the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The examination guidelines for determining obviousness under 35 U.S.C. 103 are described in MPEP 2141-2145.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pekny US 2009/0230454 A1 as previously applied.

4. **Claim 9 presents:** "An apparatus comprising: a first non-volatile memory cell including a first memory element, the first memory element having a ring shape; a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and a conductive material extending through the first and second memory elements."

Pekny illustrates:

Figs. 3-4, [0034-40], an apparatus comprising:

- a first non-volatile memory including a first memory element cell **450.sub.1, 2**, **fig. 4**;
- a second non-volatile memory cell including a second memory element **450.sub.2,2**, **fig. 4**; and
- a conductive material **230** (**conductive pillar**) extending through the first and second memory elements, **fig. 2B**.

Although **Pekny** discloses a non-volatile memory with a first memory element cell, a second memory element cell, but, **Pekny** does not specifically structure the first memory element cell and the second memory element cell having "**a ring shape**". However, it is noted that **Pekny in fig. 4**, demonstrates that the holes **226** have a circular cross section which is associated to the shape of the memory element. It would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust the hole until the desired shape is obtained, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

5. **Claim 10 presents:** "The apparatus of claim 9, further comprising: a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device."

Pekny illustrates the apparatus, further comprising:

- a first additional conductive material (**word line 424.sub.1,2**, **as a control gate for the memory cell 450**) configured to operate as a control gate to access the first memory cell, wherein the first memory element (**450.sub.1, 2, fig. 4**); and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells (**450.sub.2,2**) are located **figs. 3-4, [0034-40]**; and
- a second additional conductive material **424.sub.2,2** configured to operate as a control gate to access the second memory cell **450.sub.2,2**, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device **figs. 3-4, [0034-40]**.

6. **In re-claim 11, Pekny** illustrates the apparatus of claim 10, wherein each of the memory cells further includes a first dielectric **202** between the respective memory element and the conductive material **figs. 2A-2C**, **[0021-22]**.

7. **In re-claim 12, Pekny illustrates** the apparatus of claim 11, wherein each of the memory cells further includes a second dielectric **206** between the respective memory element and the respective additional conductive material **[0023]**.

8. **In re-claims 13 and 14, Pekny** discloses the apparatus of claim 9, but further, **Pekny** illustrates merely “a data line over a substrate to carry signals representing

values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell", however, **Pekny** states that "During a read operation, data is passed from the cache register 118 to the I/O control circuitry 112 for output to the external processor 130; then new data is passed from the data register 120 to the cache register 118" (**See paragraph 16**). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the control logic 116 to temporarily store data while the memory array 104 is busy writing or reading, respectively, other data.

Allowable Subject Matter

9. Claims 1-8 and 15-21 are allowed. The following is an examiner's statement of reasons for allowance: the prior art does not teach or suggest a method having all of the limitations of claims 1, 4, 15 and 20, including:

- a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the first device level, as recited in claim 1;
- a common source; and data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions , wherein the common source is formed over a substrate of the

memory device, such that the first and second memory cells are between the common source and the substrate, as recited in claim 4;

- a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the first device level, as recited in claims 15 and 20.

Response to Arguments

10. Applicants' arguments with respect to claims 1-21 have been considered by amendment filed on 09/07/2012.

11. Applicant argues that “Independent claim 9 recites, among other elements: a first non-volatile memory cell including a first memory element, "the first memory element having a ring shape"; and a second non-volatile memory cell including a second memory element, "the second memory element having a ring shape". It is respectfully submitted that these elements are not found in Pekny.”

In response, Pekny clearly discloses in 3-4, [0034-40], all the features of the invention, for example Pekny discloses “a first non-volatile memory including a first memory element cell 450.sub.1, 2, fig. 4; a second non-volatile memory cell including a

second memory element 450.sub.2, 2, fig. 4; and a conductive material 230 (conductive pillar) extending through the first and second memory elements, fig. 2B.

Although Pekny discloses a non-volatile memory with a first memory element cell, a second memory element cell, but, Pekny does not specifically structure the first memory element cell and the second memory element cell having “a ring shape”. However, it is noted that Pekny in fig. 4, demonstrates that the holes 226 have a circular cross section which is associated to the shape of the memory element. It would have been obvious to one having ordinary skill in the art at the time the invention was made to adjust the hole until the desired shape is obtained, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

However, the Pekny et al. reference was previously-cited in the first action, for the reasons discussed in detail above.

12. **Conclusion**

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILNER JEAN BAPTISTE whose telephone number is (571)270-7394. The examiner can normally be reached on M-F FROM 7:30 AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, OLIK CHAUDHURI can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WILNER JEAN BAPTISTE/
Examiner, Art Unit 2823

/Matthew Smith/
Supervisory Patent Examiner, Art Unit 2800

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

SEARCHED

Class	Subclass	Date	Examiner
257	314,E21.602,E29.255,E21.001	5/31/2012	wj
438	128, 309	5/31/2012	wj
365	189.11	12/20/2012	wj

SEARCH NOTES

Search Notes	Date	Examiner
East	5/31/2012	wj
East updated	12/20/2012	wj

INTERFERENCE SEARCH

Class	Subclass	Date	Examiner

/W.J./ Examiner.Art Unit 2823	

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	**Art Unit**
	WILNER JEAN BAPTISTE	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2012	12/20/2012							
	1	✓	=							
	2	✓	=							
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	33	N	-							
	34	N	-							

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sanh D. Tang et al.	Examiner: Unknown	
Serial No.:	12/825,211	Group Art Unit: 2823	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.:	73115	Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.111

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Office Action dated June 7, 2012, please amend the application as follows, and consider the appended remarks.

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus comprising:

a substrate of a memory device;

a plurality of first memory cells located in a first device level of [[a]] the memory device over the substrate;

a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the first device level;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate.

2. (Original) The apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. (Original) The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory

cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. (Currently Amended) An apparatus comprising:

a plurality of first memory cells located in a first device level of a memory device;

a plurality of second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction;

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions ~~The apparatus of claim 2~~, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. (Original) The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

6. (Original) The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

7. (Original) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

8. (Original) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

9. (Currently Amended) An apparatus comprising:

a first non-volatile memory cell including a first memory element, the first memory element having a ring shape;

a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and

a conductive material extending through the first and second memory elements.

10. (Original) The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device.

11. (Original) The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. (Original) The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. (Original) The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell.

14. (Original) The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

15. (Currently Amended) An apparatus comprising:

a substrate of a memory device;

a first conductive material located in a first device level of [[a]] the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the first device level;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically

isolated from the first and second memory elements by at least a respective portion of the second dielectric.

16. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

17. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.

18. (Original) The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.

19. (Original) The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

20. (Currently Amended) An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element;

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically

isolated from the first and second memory elements by at least a respective portion of the second dielectric ~~The apparatus of claim 15, further comprising:~~

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

21. (Original) The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

22.-34. (Canceled)

REMARKS

This reply responds to the Office Action dated June 7, 2012.

Claims 1, 4, 15, and 20 are amended. Claims 22-34 are canceled. No claims are added. Thus, claims 1-21 are now pending in this application.

It is noted that unless otherwise stated herein, amendments to the claims have been made to clarify meaning, correct typographical errors, provide proper antecedent basis, and/or provide consistent terminology, and not for reasons related to patentability.

Support for the amendments made to the claims can be found in the application, such as in paragraph 0026. No new matter has been added. Reconsideration of the claims in view of the amendments above and the remarks that follow is respectfully requested.

Claim Objections

The Office Action raises an objection to claim 1 based on reasons of alleged informalities in claim 1. For clarity, claim 1 is amended to include "a plurality of". Accordingly, reconsideration and withdrawal of the objection is respectfully requested.

Affirmation of Election

The undersigned acknowledges the election without traverse of claims 1-21 in the reply filed on 03/22/2012. Claims 22-34 are now canceled without prejudice or disclaimer.

The Rejection of Claims Under § 103

Claims 1-6, 9-21 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pekny US 2009/0230454 A1. This rejection is respectfully traversed in view of the following, which demonstrates why a *prima facie* case of obviousness has not been properly established.

Amended independent claim 1 recites, among other elements, a plurality of first memory cells located in a first device level of the memory device over the substrate; and a plurality of second memory cells located in "a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the first device level". It is respectfully submitted that this element is not found in Pekny.

The Office Action, on page 4, indicates that cells $450_{1,2}$ and $450_{2,2}$ in FIG. 4 of Pekny correspond to the first memory cells and the second memory cells, respectively, of claim 1. The undersigned respectfully disagrees. For example, paragraph 0021 of Pekny describes a substrate 200 (e.g., FIG. 2B). As shown in FIG. 2B of Pekny, cells $450_{1,2}$ and $450_{2,2}$ are located in the *same level* over substrate 200. In contrast, amended claim 1 recites that the first memory cells are located in a first device level over the substrate, and second memory cells are located in a second device level of the memory device over the first device level and over the substrate, wherein "the first device level is different from the first device level".

Claim 1 also recites "a first control gate formed in the first device level" and "a second control gate formed in the second device level". The undersigned also cannot find these elements in Pekny. As discussed above, amended claim 1 recites that the first device level is different from the first device level. Thus, the first and second control gates of claim 1 are formed on "different" device levels over the substrate. The Office Action, on page 4, indicates that word lines $424_{2,1}$ and $424_{2,2}$ in FIG. 4 of Pekny correspond to the first and second control gates, respectively, of claim 1. The undersigned respectfully disagrees. For example, as shown in FIG. 2B of Pekny, word lines $424_{2,1}$ and $424_{2,2}$ are formed on *the same* level over substrate 200. In contrast, recites "a first control gate formed in the first device level" and "a second control gate formed in the second device level".

For at least the above reasons, Pekny lacks at least one element of amended claim 1 and its dependent claims 2, 3, 5, and 6. Thus, claims 1-3, 5, and 6 are not obvious over Pekny. Accordingly, reconsideration, withdrawal of the rejection, and allowance of claims 1-3, 5, and 6 is respectfully requested.

Dependent claim 4 is amended only to rewrite it in independent form to incorporate elements of base claim 1 and intervening claim 2. The rewriting of claim 4 does not alter its scope. Claim 4 recites, among other elements, that "the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate". It is respectfully submitted that this element is not found in Pekny.

The Office Action, on page 6, indicates that paragraphs 0041-42 of Pekny teach this element. The undersigned respectfully disagrees. For example, paragraphs 0041-42 of Pekny describe some elements of the device of Pekny including cells $450_{1,2}$ and $450_{2,2}$. Paragraph 0021 of Pekny describes a substrate 200 (e.g., FIG. 2B). As discussed above regarding claim 1, the Office Action, on page 4, in indicates that cells $450_{1,2}$ and $450_{2,2}$ in FIG. 4 of Pekny correspond to the first memory cells and the second memory cells, respectively, of claim 1. The undersigned cannot find in paragraphs 0041-42 or anywhere within the bounds of Pekny a teaching or suggestion of a common source formed over substrate 200, such that cells $450_{1,2}$ and $450_{2,2}$ of Pekny are *between* such a common source and substrate 200. In contrast, claim 4 recites that "the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate". Accordingly, reconsideration, withdrawal of the rejection, and allowance of claim 4 is respectfully requested.

Independent claim 9 recites, among other elements: a first non-volatile memory cell including a first memory element, "the first memory element having a ring shape"; and a second non-volatile memory cell including a second memory element, "the second memory element having a ring shape". It is respectfully submitted that these elements are not found in Pekny.

The Office Action, on page 7, indicates that cells $450_{1,2}$ and $450_{2,2}$ in FIG. 4 of Pekny correspond to the first memory cells and the second memory cells, respectively, of claim 9. The undersigned respectfully disagrees. For example, as shown in FIG. 4 of Pekny, cell $450_{1,2}$ does not have ring shape. Rather, cell $450_{1,2}$ has a semi-circular shape. Similarly, as shown in FIG. 4 of Pekny, cell $450_{2,2}$ does not have ring shape. Rather, cell $450_{2,2}$ has a semi-circular shape. In contrast, claim 9 recites: a first non-volatile memory cell including a first memory element, "the first memory element having a ring shape"; and a second non-volatile memory cell including a second memory element, "the second memory element having a ring shape". Thus, Pekny lacks at least one element of claim 9 and its dependent claims 10-14.

Further, the undersigned cannot find the elements of claim 13 in Pekny, such as a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein "the data line is located between the substrate and the first memory cell".

For at least the above reasons, reconsideration, withdrawal of the rejection, and allowance of claims 9-14 is respectfully requested.

Amended independent claim 15 recites, among other elements: a first conductive material located in a first device level of the memory device over the substrate, and a second conductive material located in a second device level of the memory device over the first device level and over the substrate, wherein "the first device level is different from the first device level". It is respectfully submitted that this element is not found in Pekny.

The Office Action, on pages 8-9, indicates that word lines $424_{2,1}$ and $424_{2,2}$ in FIG. 4 of Pekny correspond to the first and second conductive materials, respectively, of claim 15. The undersigned respectfully disagrees. For example, as shown in FIG. 2B of Pekny, word lines $424_{2,1}$ and $424_{2,2}$ are formed on *the same* level over a substrate 200. In contrast, recites a first conductive material located in a first device level of the memory device over the substrate, and a second conductive material located in a second device level of the memory device over the first device level and over the substrate, wherein "the first device level is different from the first device level".

For at least the above reasons, Pekny lacks at least one element of amended claim 15 and its dependent claims 16-19 and 21. Thus, claims 15-19 and 21 are not obvious over Pekny. Accordingly, reconsideration, withdrawal of the rejection, and allowance of claims 15-19 and 21 is respectfully requested.

Dependent claim 20 is amended only to rewrite it in independent form to incorporate elements of base claim 15. The rewriting of claim 20 does not alter its scope. Claim 20 recites, among other elements, that "the data line is located between the second conductive material and the substrate". It is respectfully submitted that this element is not found in Pekny.

The Office Action, on page 10, indicates that paragraphs 0041-42 of Pekny teach this element. The undersigned respectfully disagrees. For example, paragraphs 0041-42 of Pekny describes some elements of the device of Pekny including a bit line 290 (FIG. 2C). As discussed above regarding claim 15, the Office Action, on page 9, in indicates that word line $424_{2,2}$ (FIG. 2C and FIG. 4) of Pekny corresponds to the claimed second conductive material. As shown in

FIG. 2C of Pekny, bit line 290 is *not* located between word line $424_{2,2}$ and substrate 200. In contrast, claim 20 recites that "the data line is located between the second conductive material and the substrate". Accordingly, reconsideration, withdrawal of the rejection, and allowance of claim 20 is respectfully requested.

Claims 7 and 8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Pekny, and in view of Matsui et al. US 2007/0057310 A1. This rejection is respectfully traversed in view of the following, which demonstrates why a *prima facie* case of obviousness has not been properly established.

Dependent claims 7 and 8 depend from independent claim 1. Matsui does not teach the element of amended claim 1 that is missing from Pekny. Thus, for at least the reasons presented above regarding claim 1, dependent claims 7 and 8 are also patentable over Pekny and Matsui. Accordingly, reconsideration, withdrawal of the rejection, and allowance of claims 7 and 8 is respectfully requested.

CONCLUSION

It is respectfully submitted that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone the undersigned at (612) 373-6969 to facilitate prosecution of this Application.

If necessary, please charge any additional fees or deficiencies, or credit any overpayments to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402--0938
(612) 373-6969

Date September 7, 2012 By /Viet Tong/
Viet V. Tong
Reg. No. 45,416

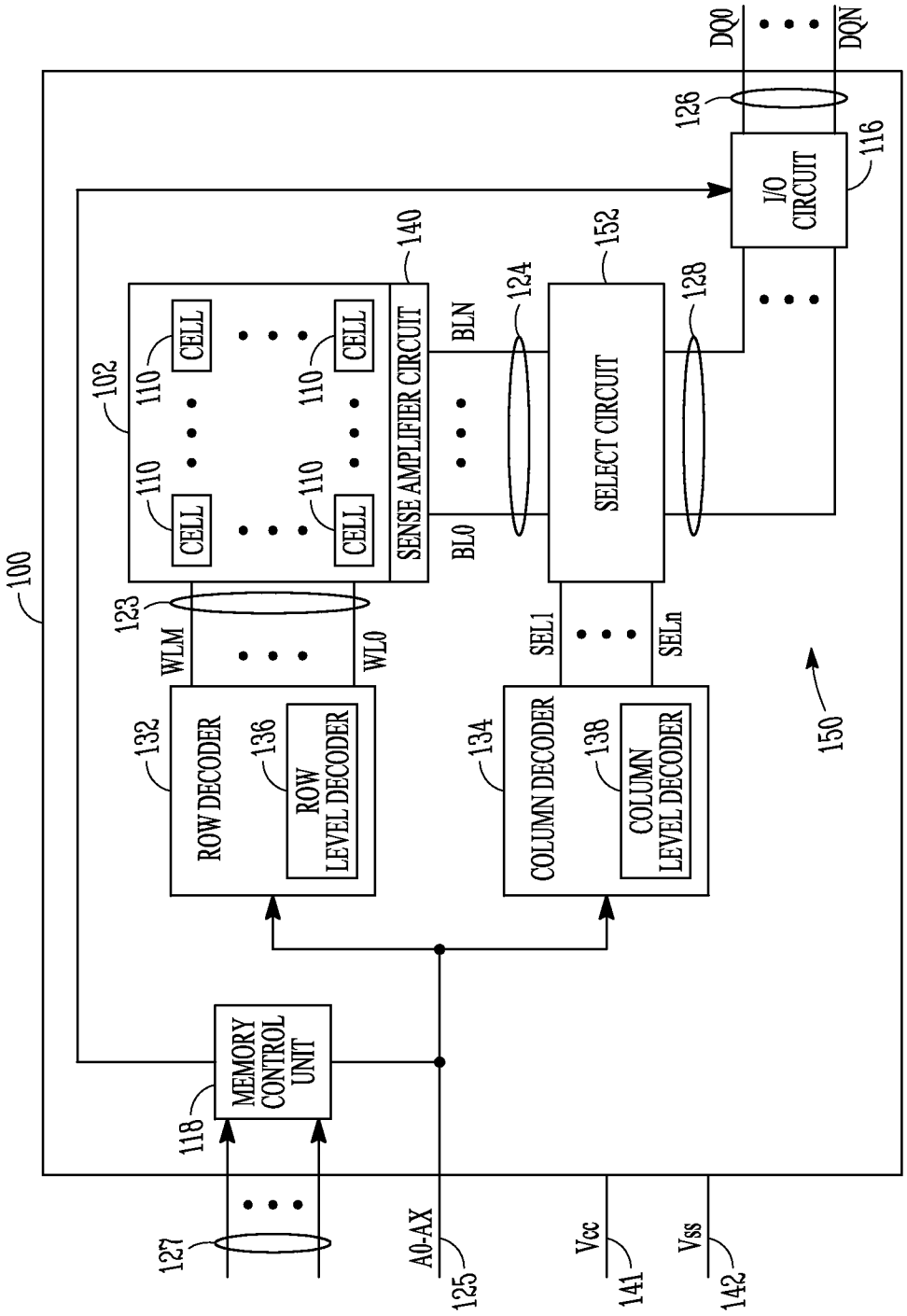

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COLUMN DECODER
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FIG. 1

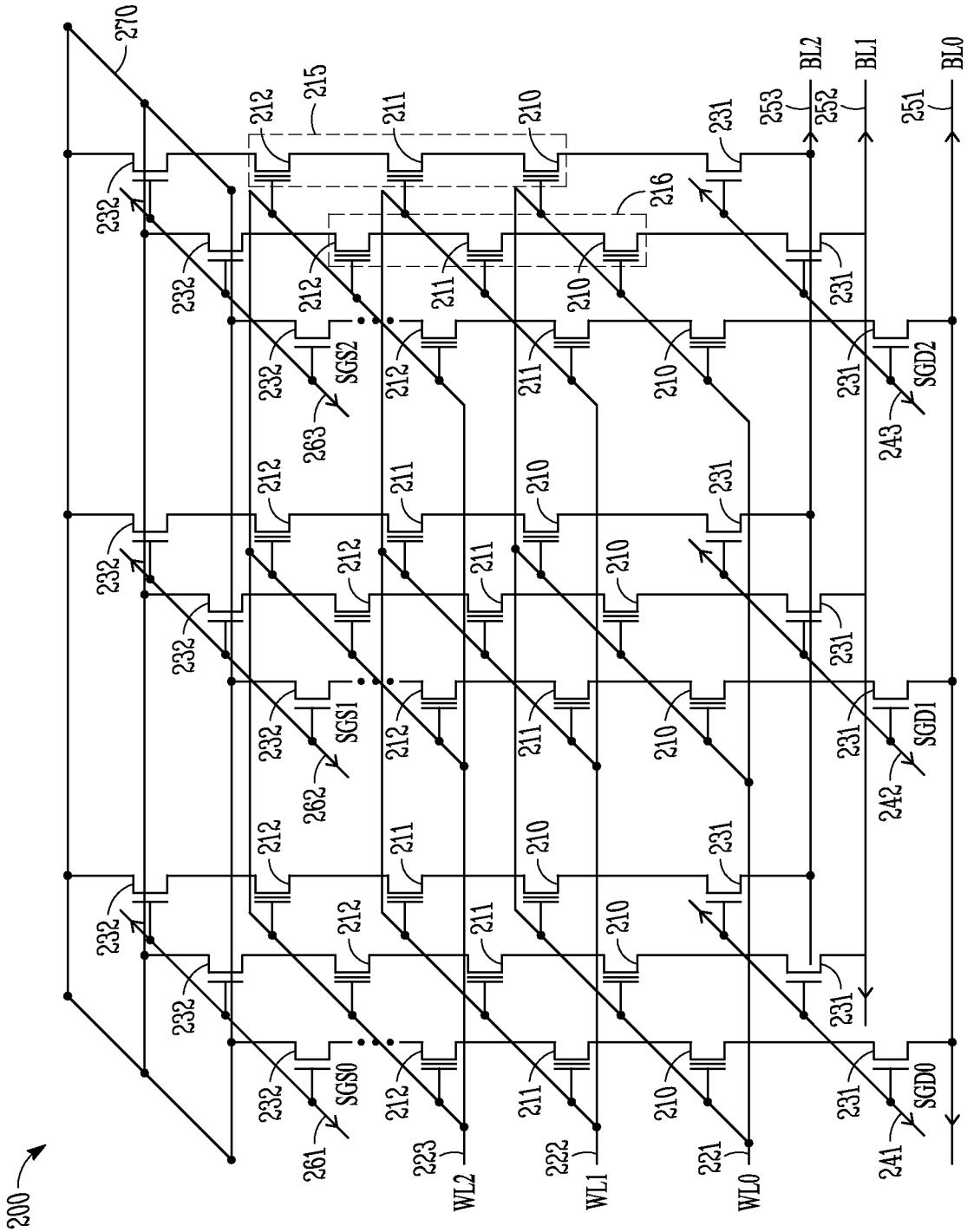

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FIG. 2

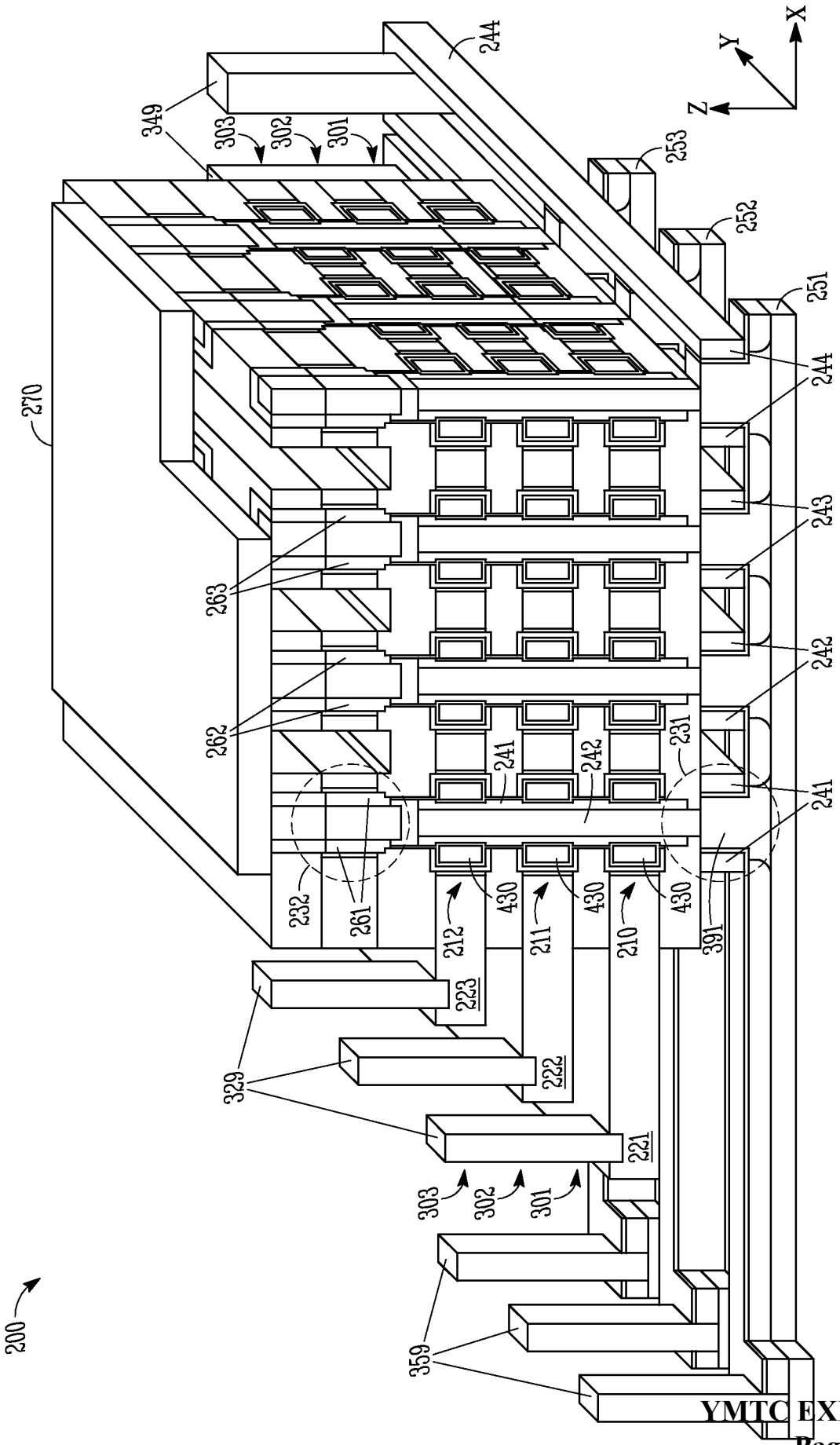

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262
241
242
231
232
261
212
211
210
430
391
223
222
221
329
359
200

FIG. 3

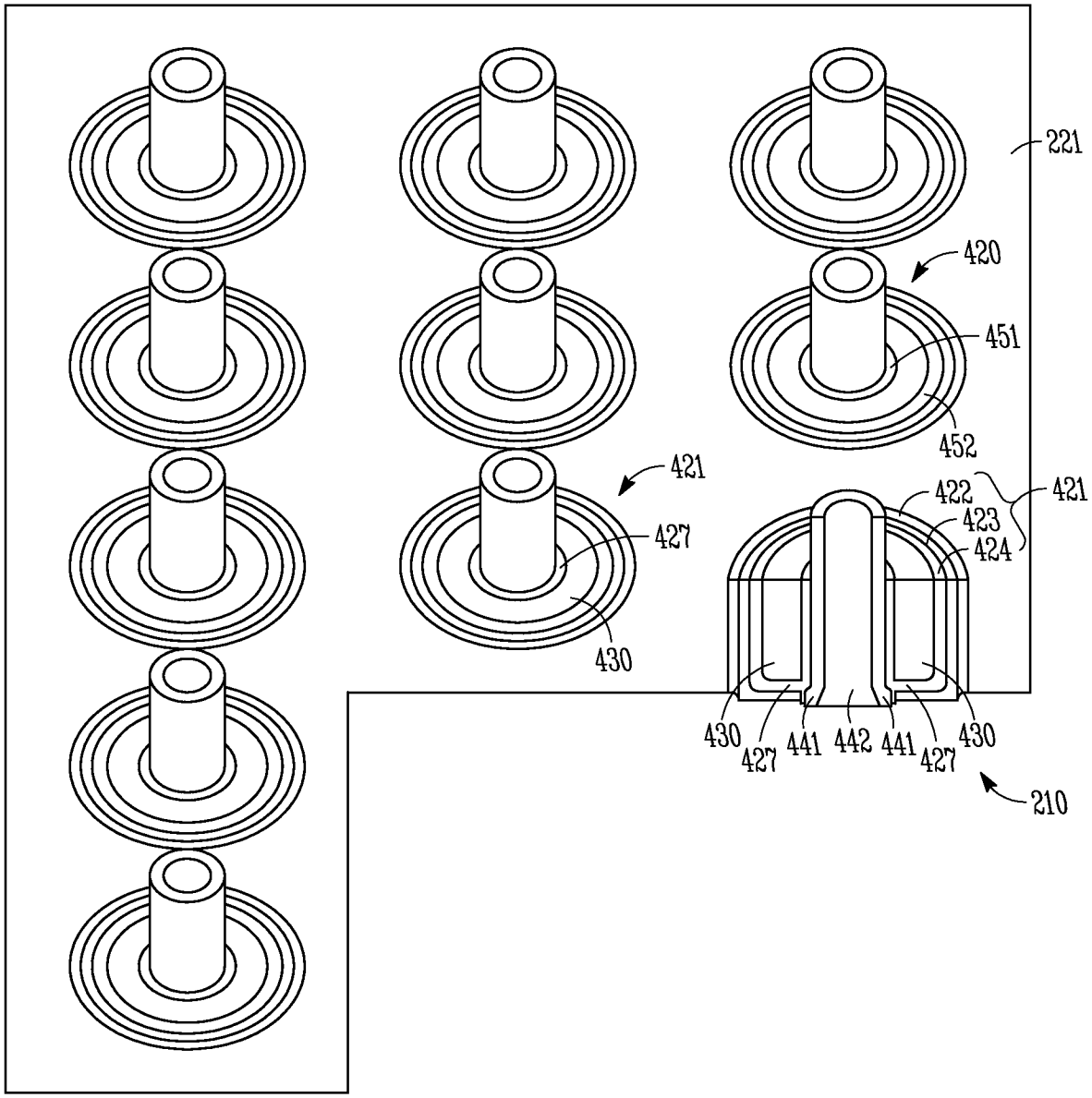

221
420
451
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423
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421
427
430
430
427
441
442
441
427
430
210

FIG. 4

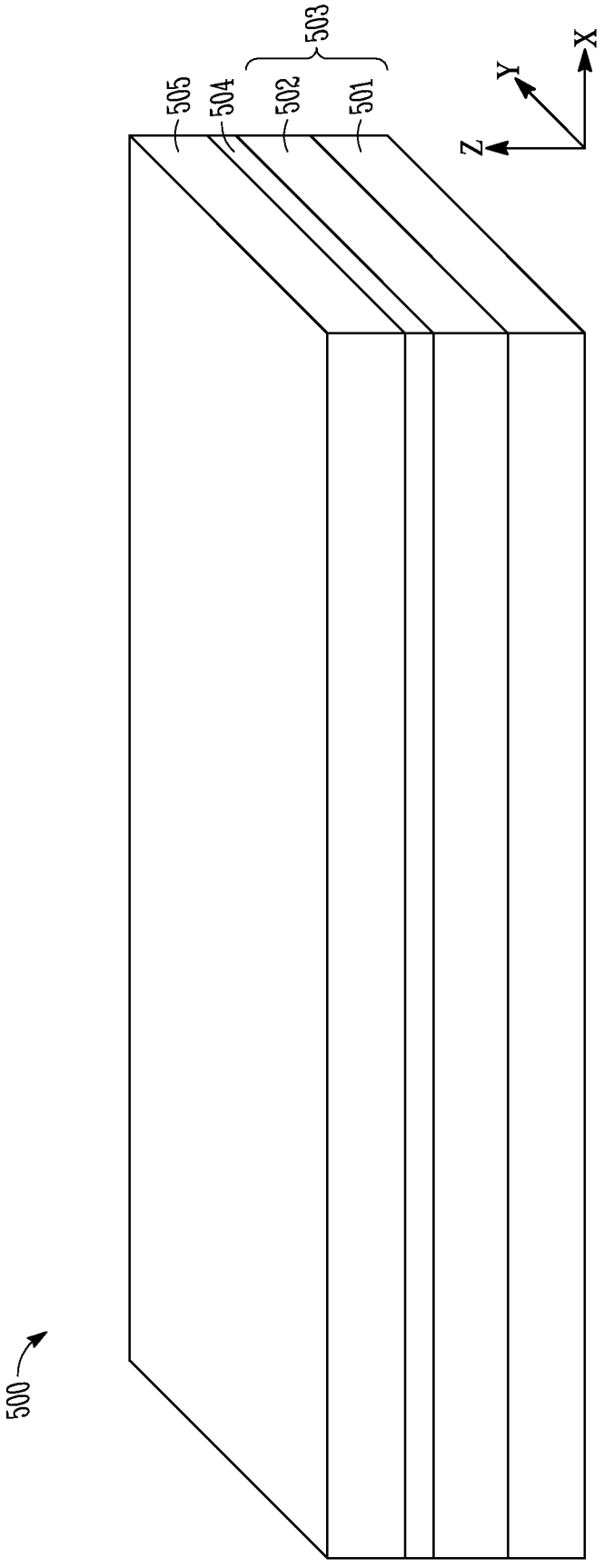


FIG. 5

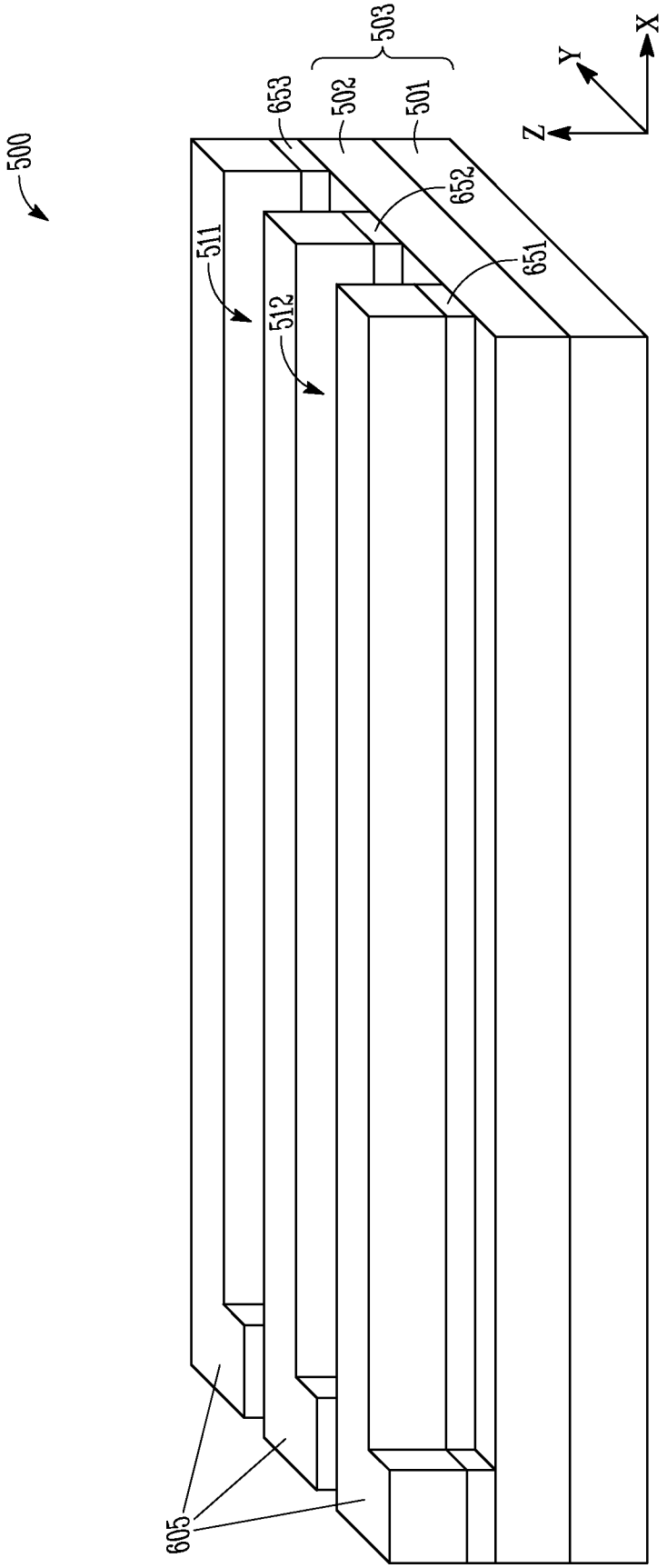


FIG. 6

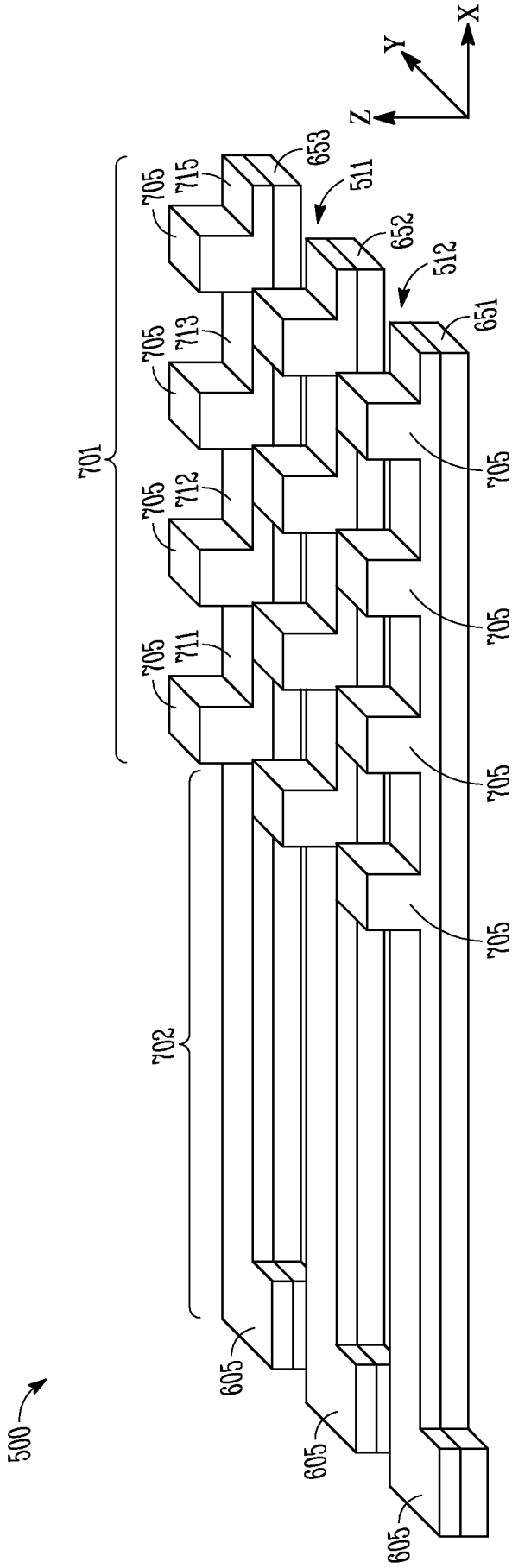


FIG. 7

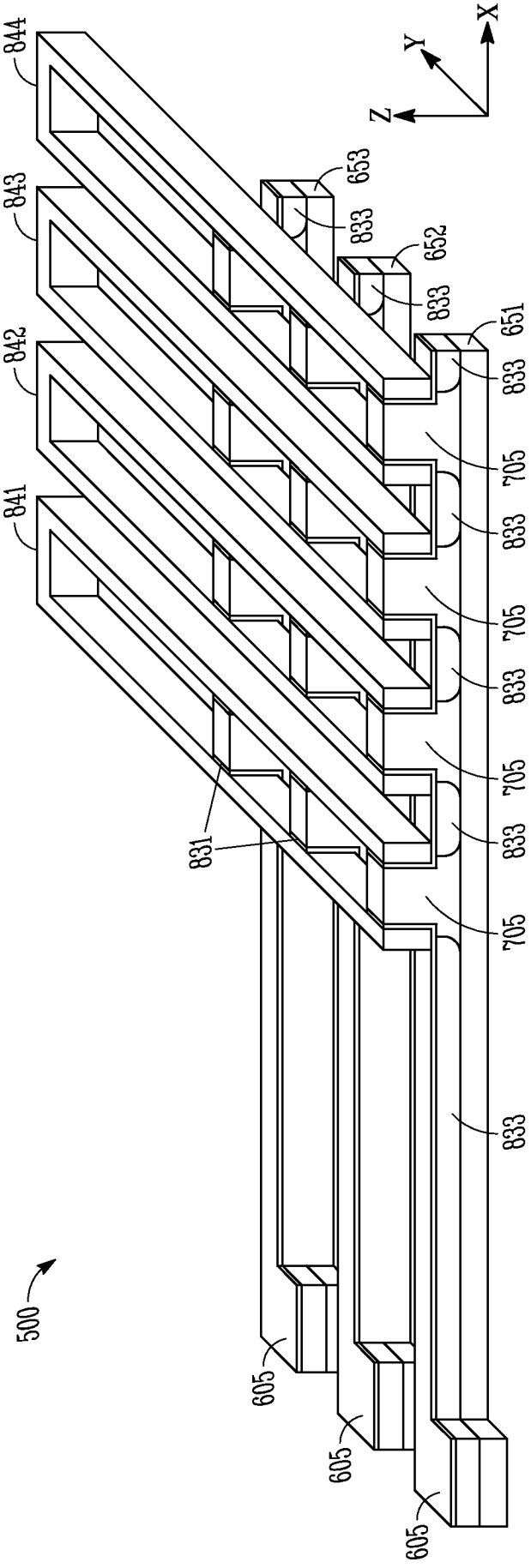


FIG. 8

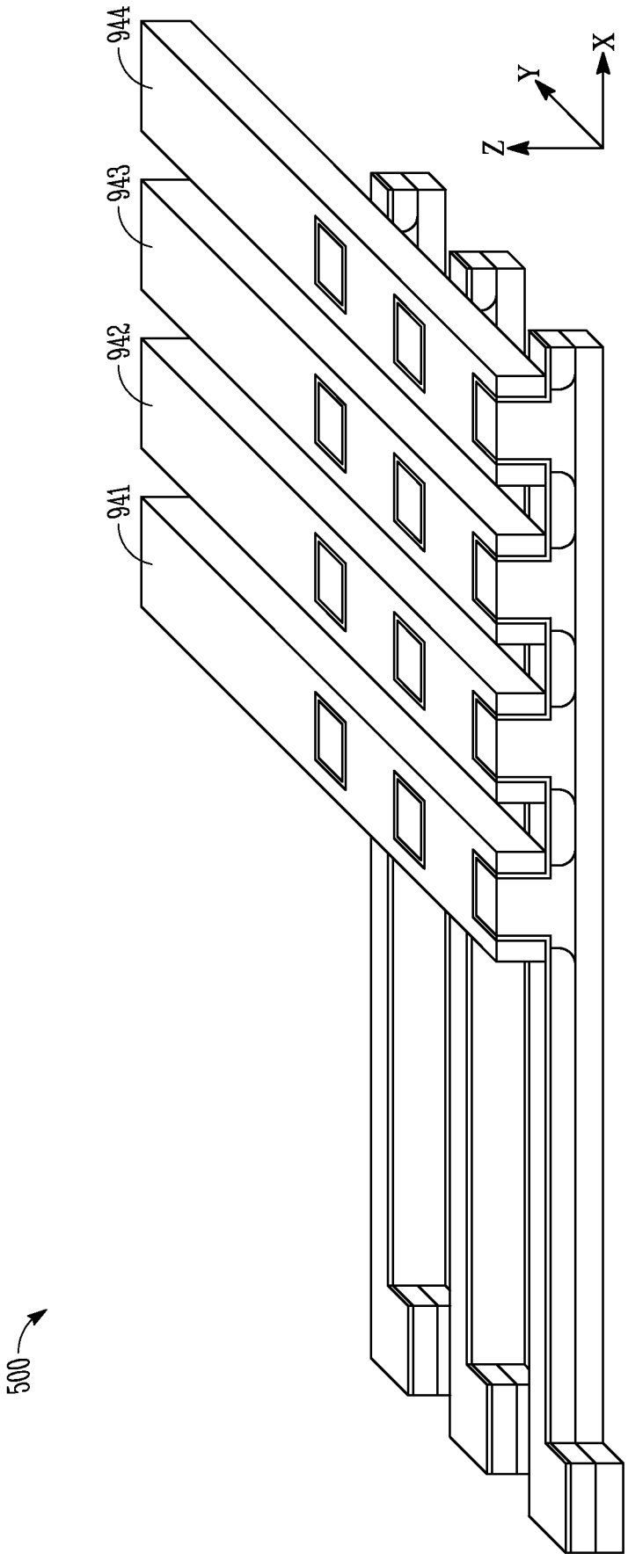


FIG. 9

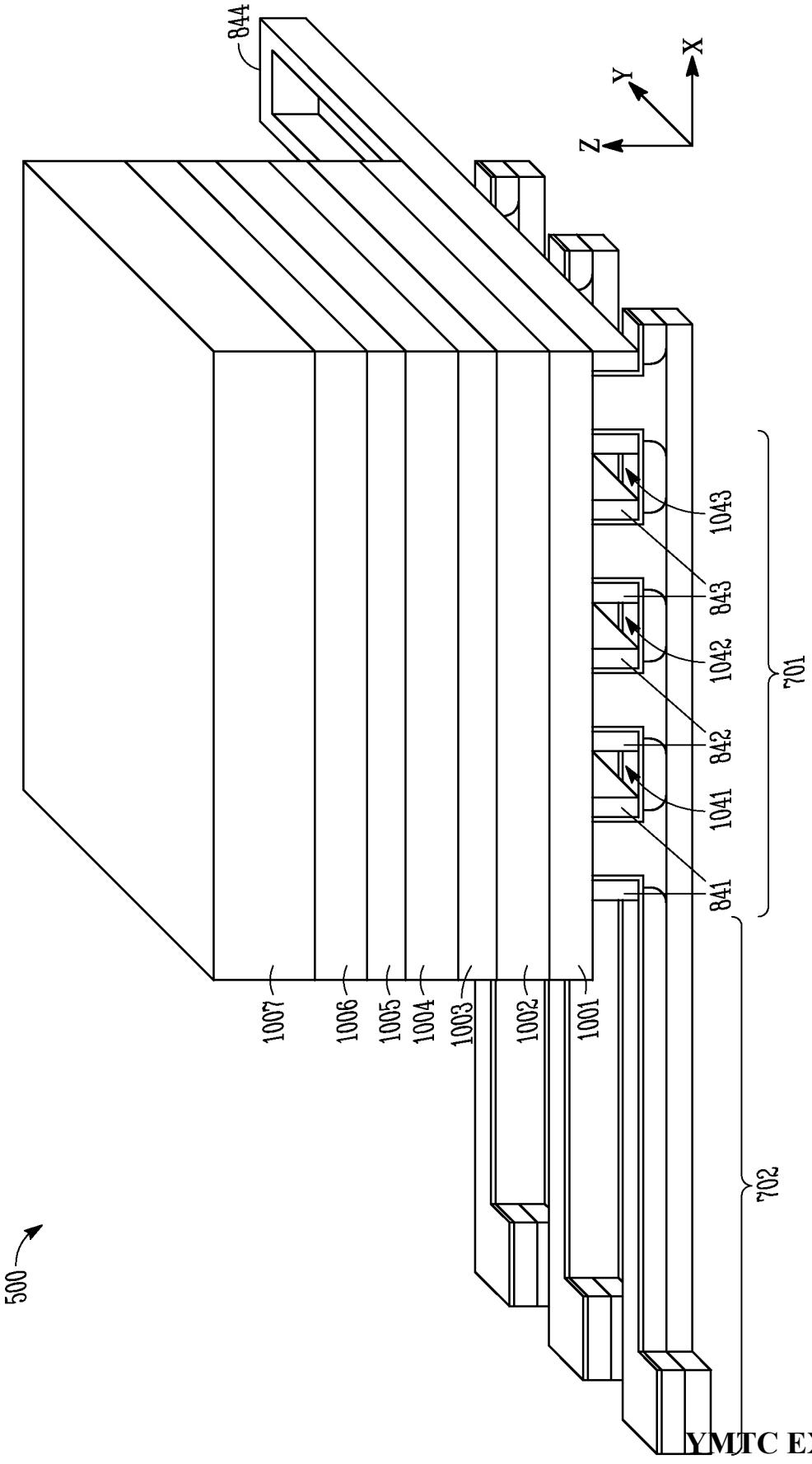

844
Y
X
Z
1043
843
1042
842
1041
841
701
1007
1006
1005
1004
1003
1002
1001
702
500

FIG. 10

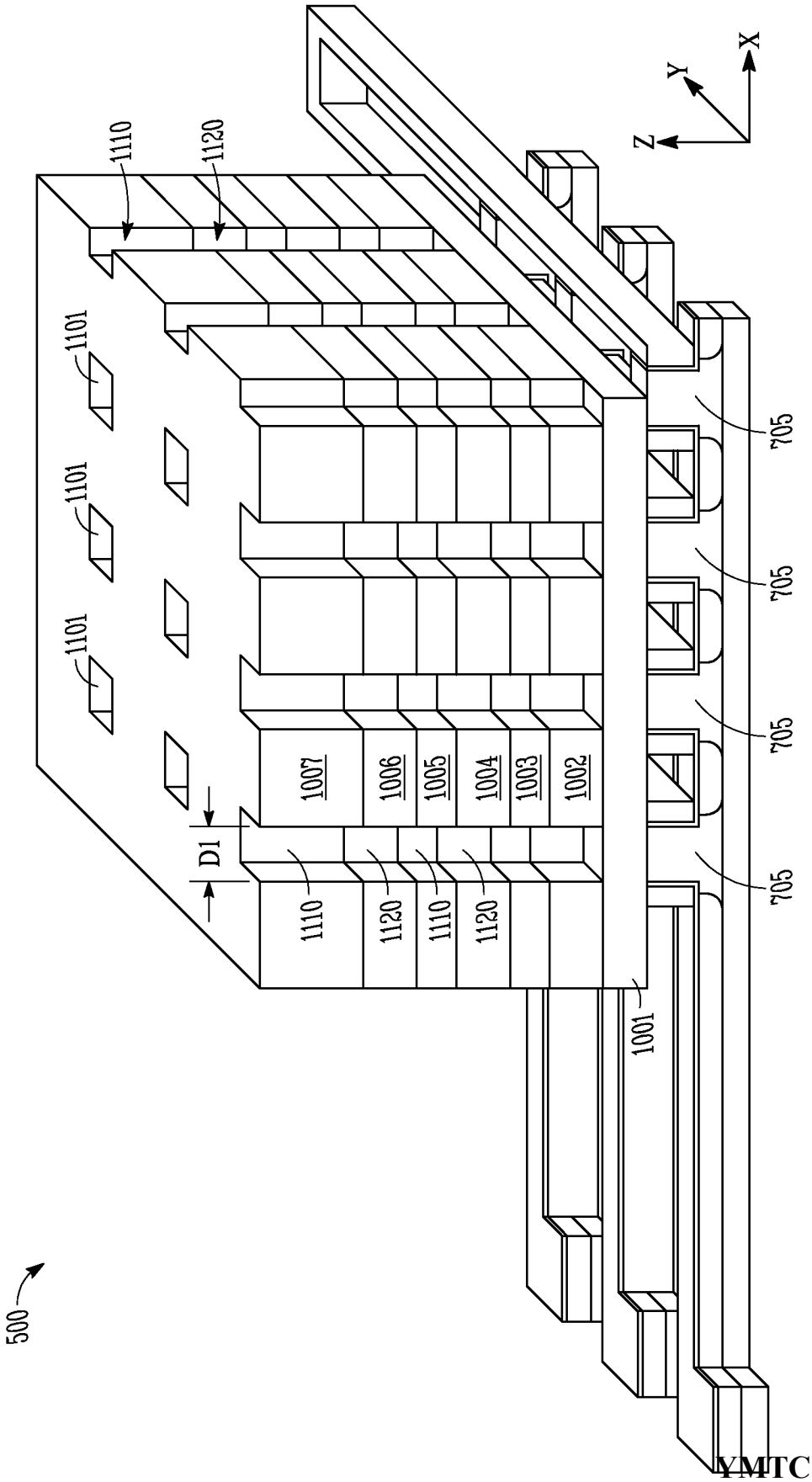

X
Y
Z
1110
1120
1101
1101
1101
705
705
705
705
1007
1006
1005
1004
1003
1002
D1
1110
1120
1110
1120
1001
500

FIG. 11

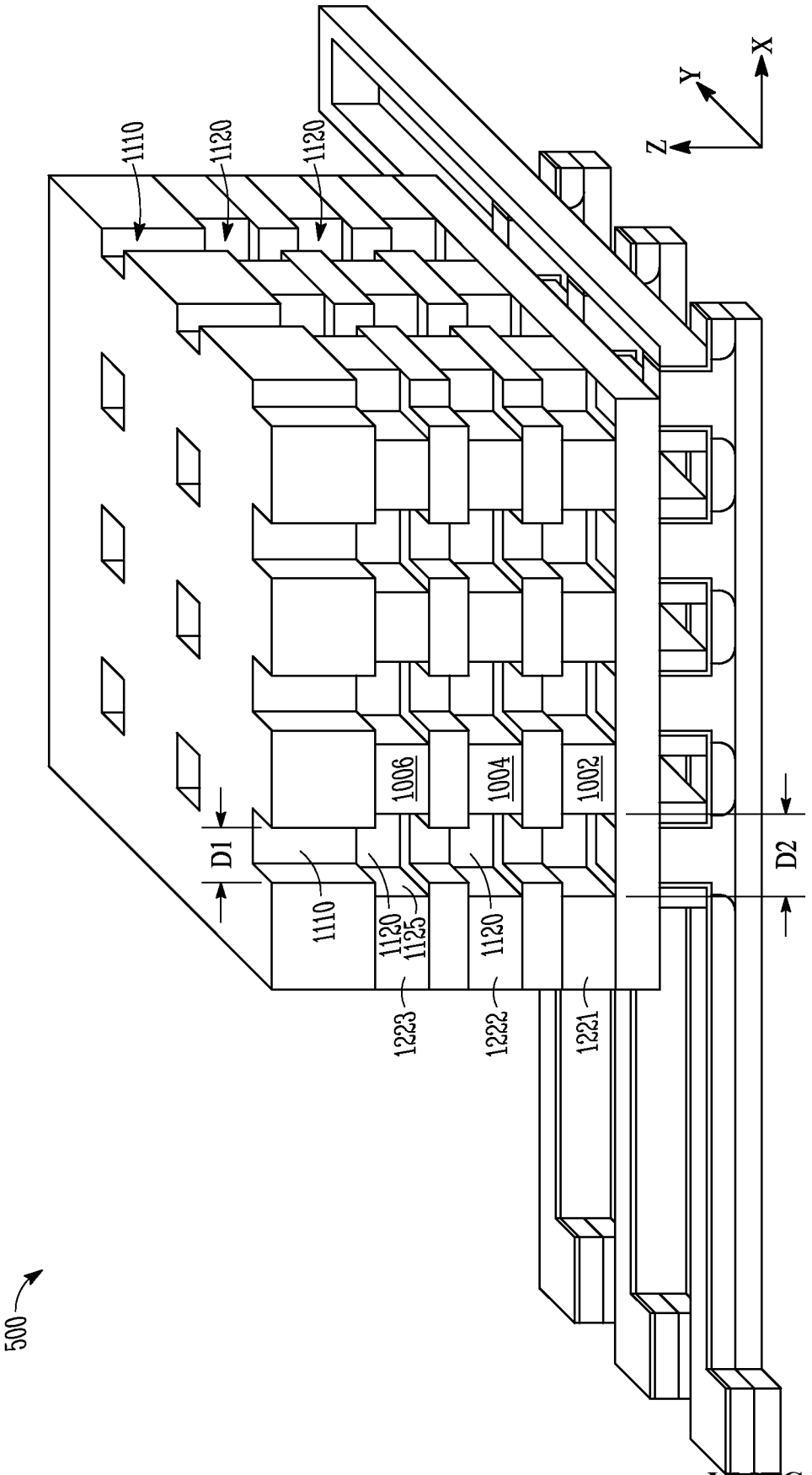

X
Y
Z
1110
1120
1120
1006
1004
1002
D1
D2
1110
1120
1125
1120
1223
1222
1221
500

FIG. 12

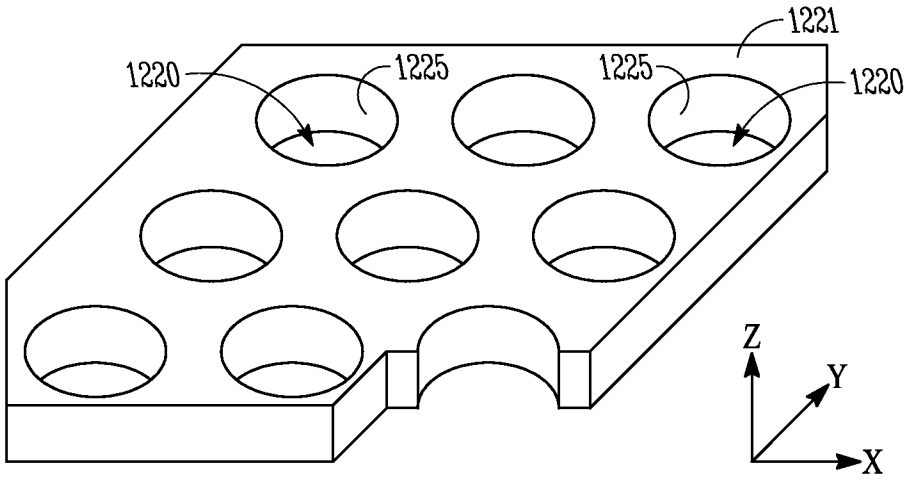


FIG. 13

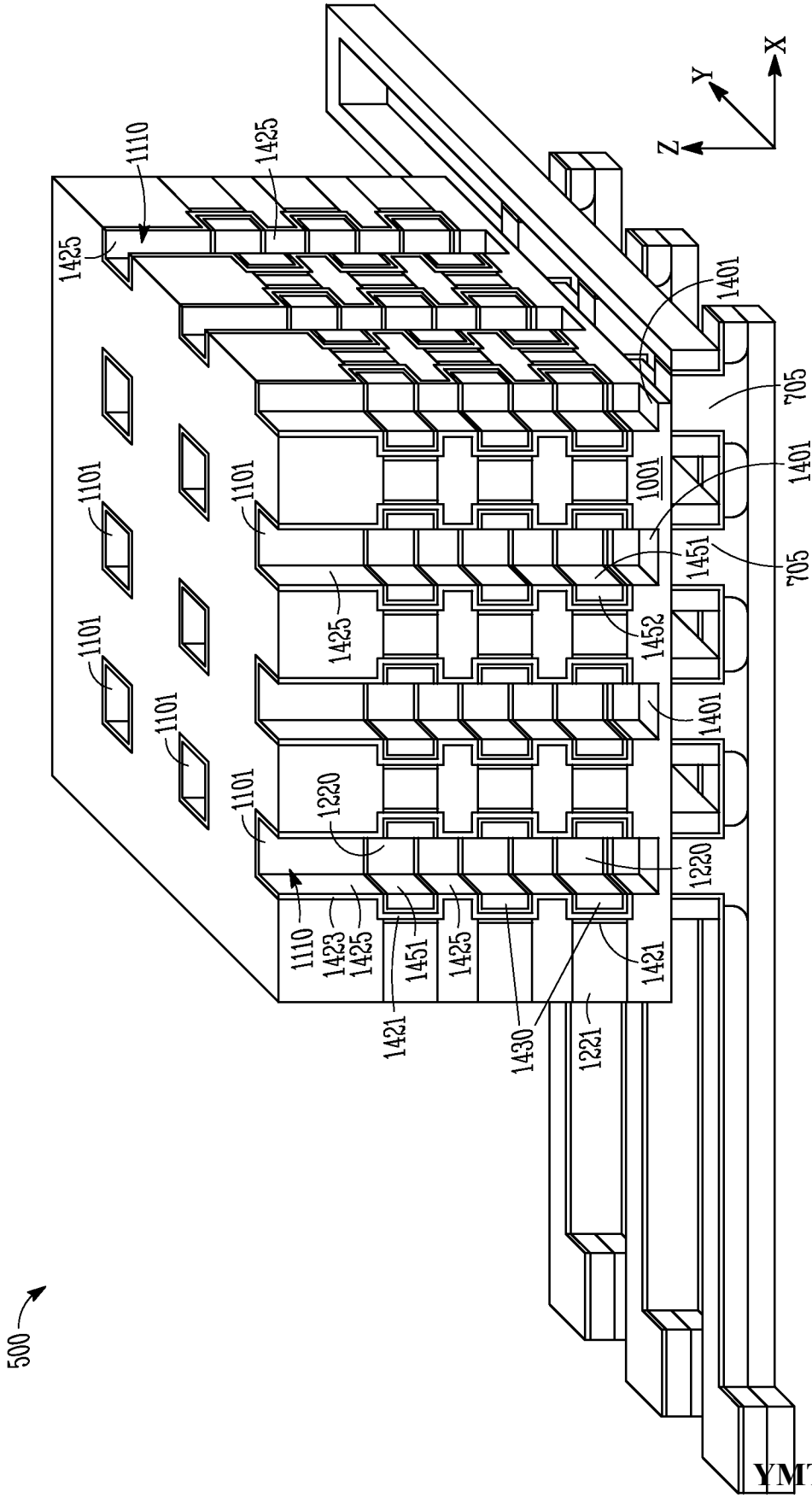

X
Y
Z
1110
1425
1425
1401
705
1001
1401
1451
705
1101
1101
1425
1452
1101
1401
1101
1101
1220
1220
1110
1423
1425
1451
1425
1421
1421
1430
1221
500

FIG. 14

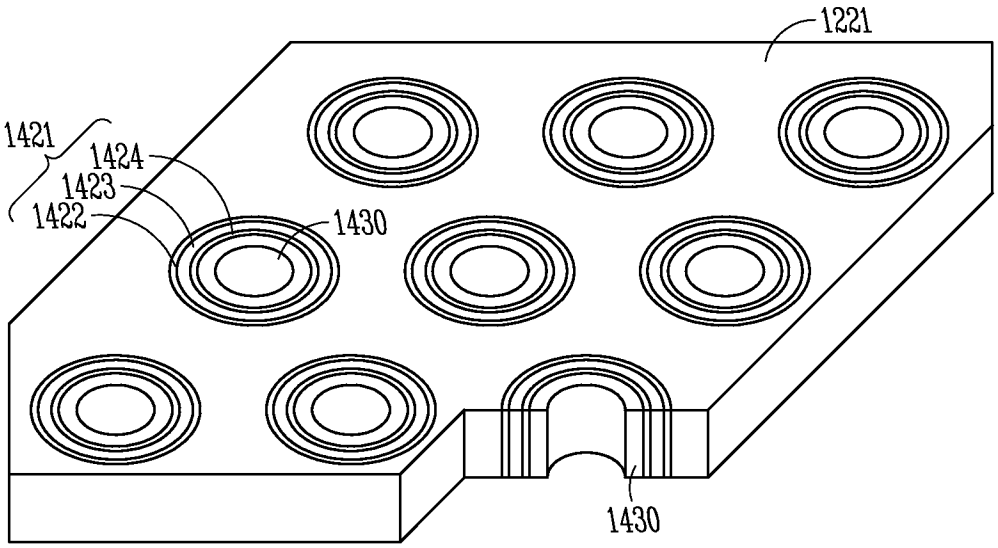


FIG. 15

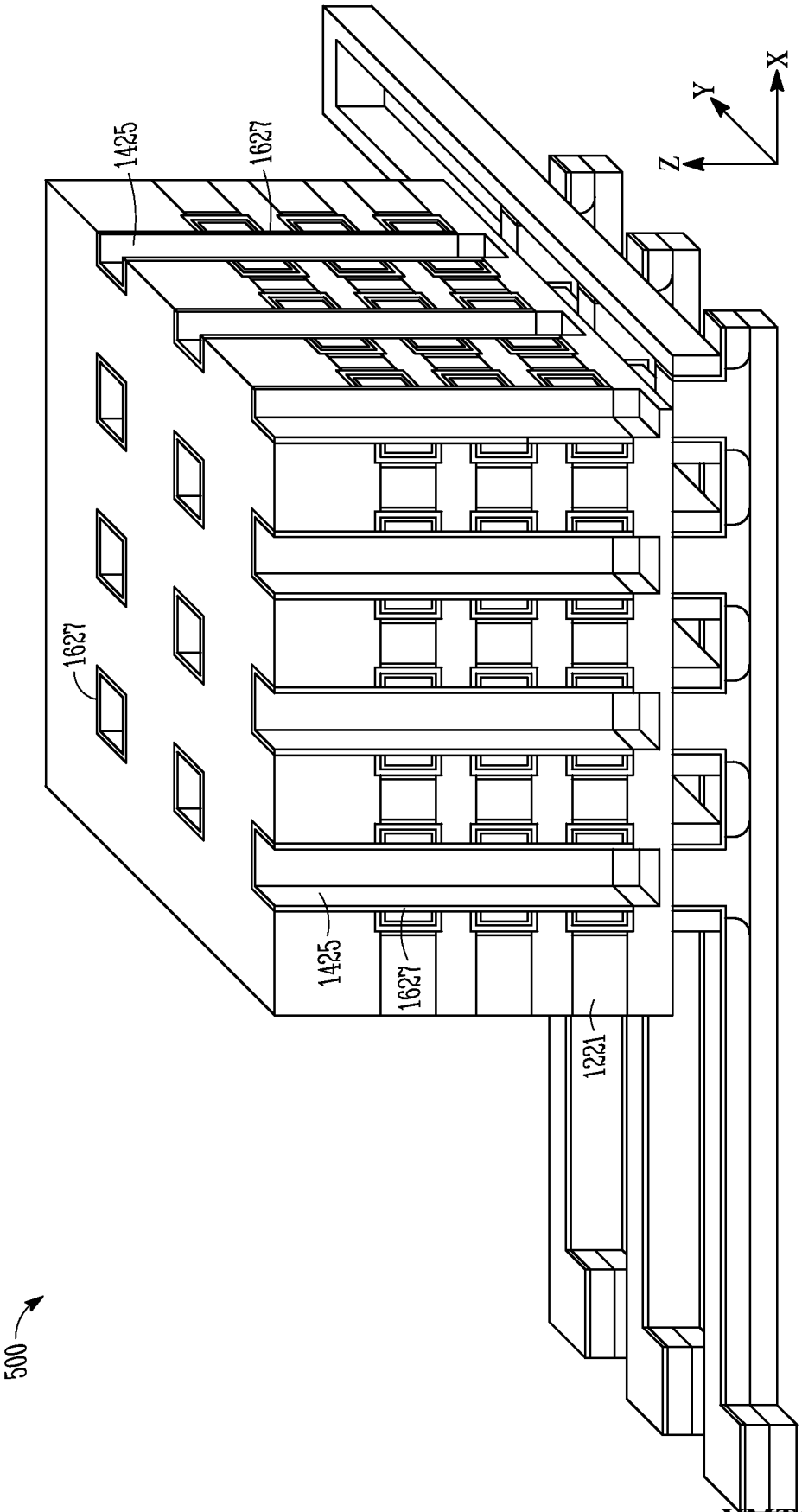


FIG. 16

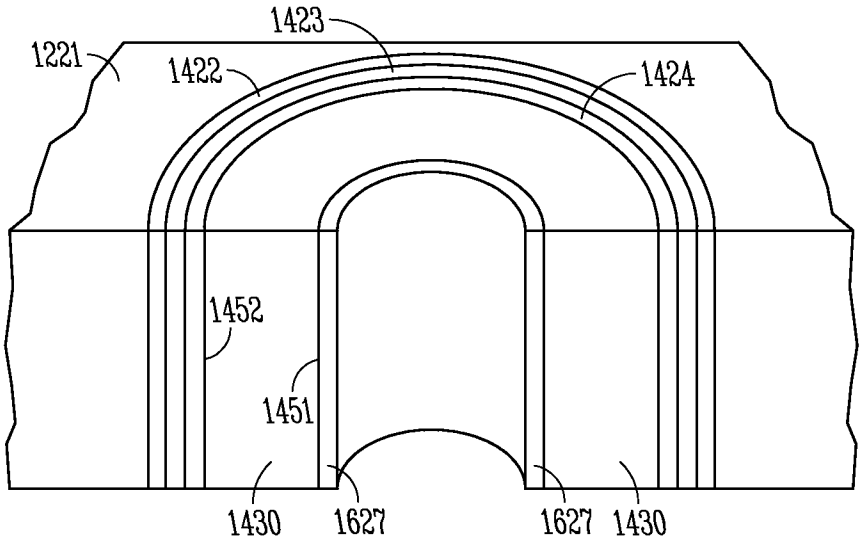


FIG. 17

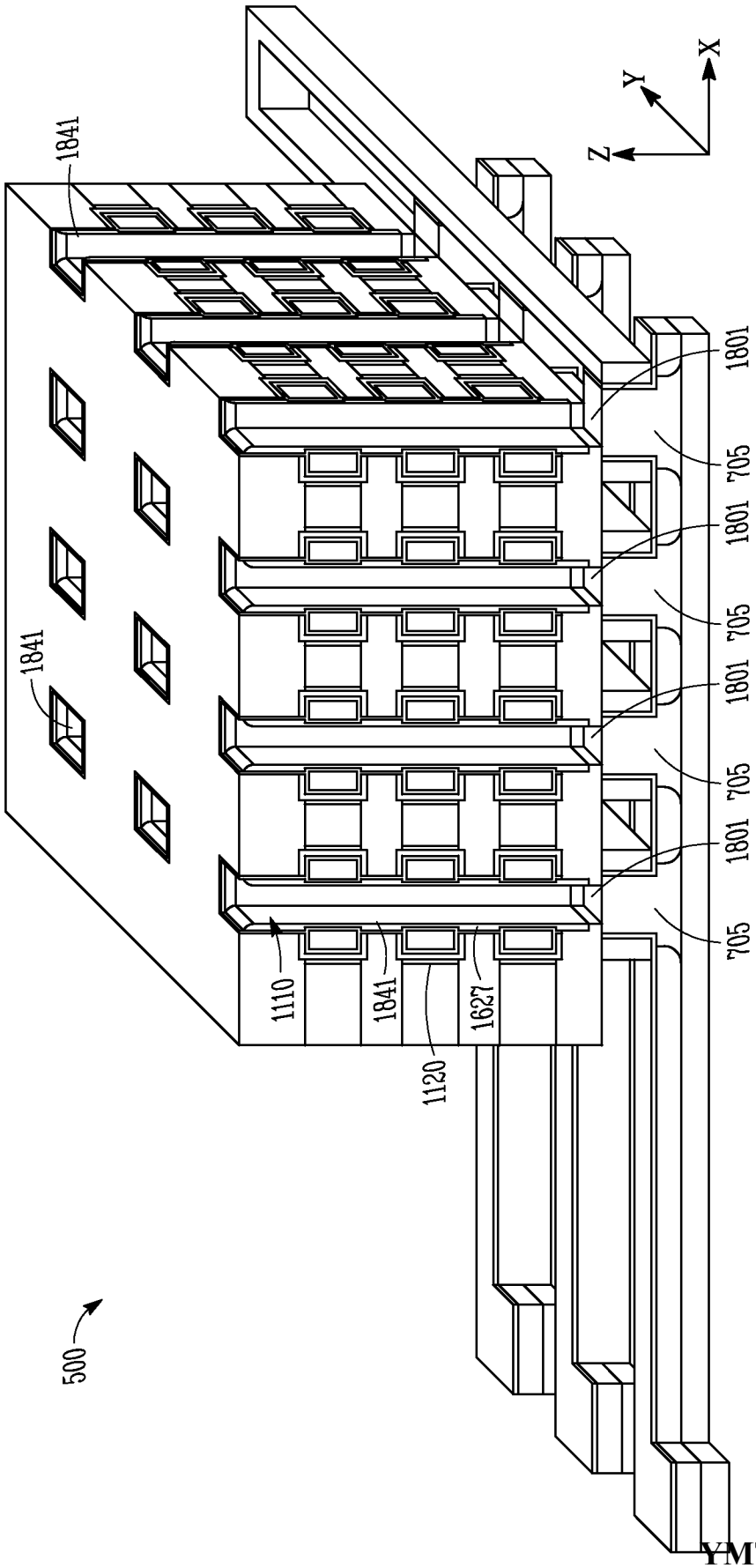

Y
X
Z
1841
1801
705
1801
705
1801
705
1801
705
1841
1110
1841
1627
1120
500

FIG. 18

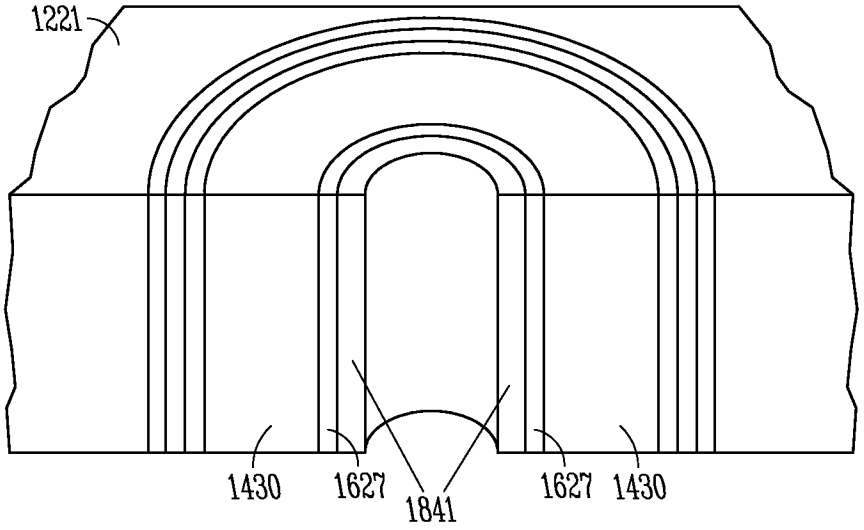


FIG. 19

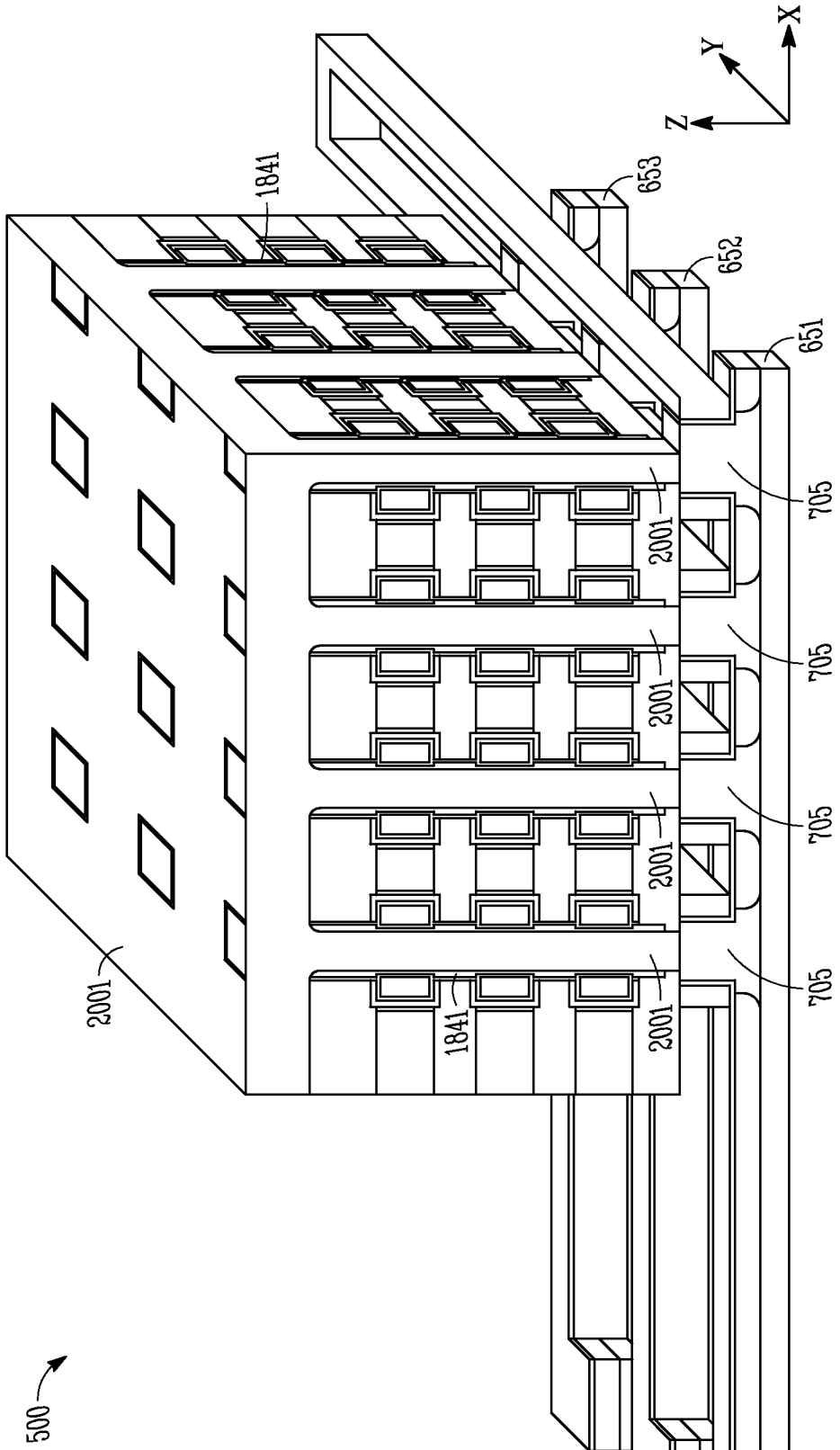


FIG. 20

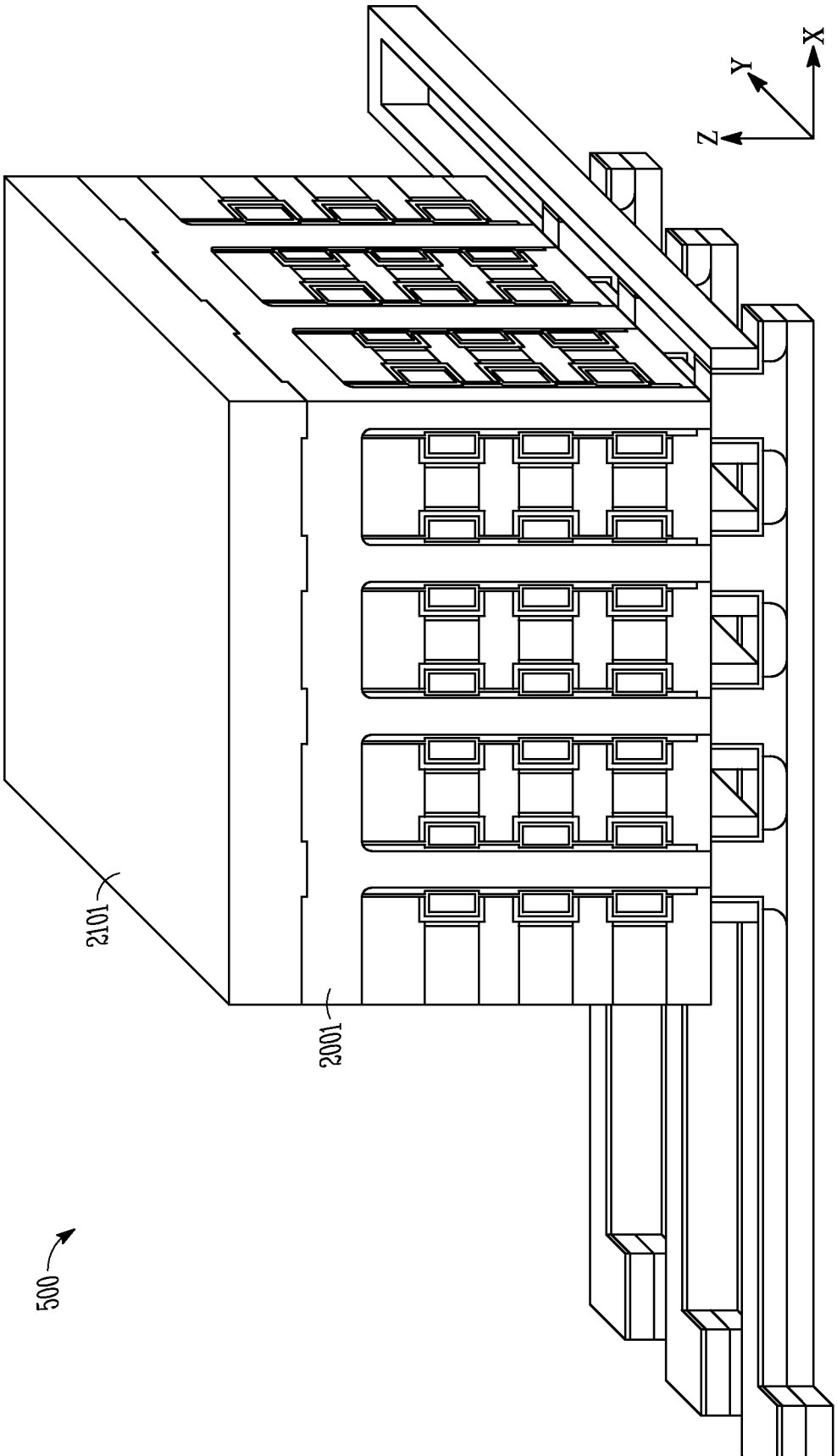


FIG. 21

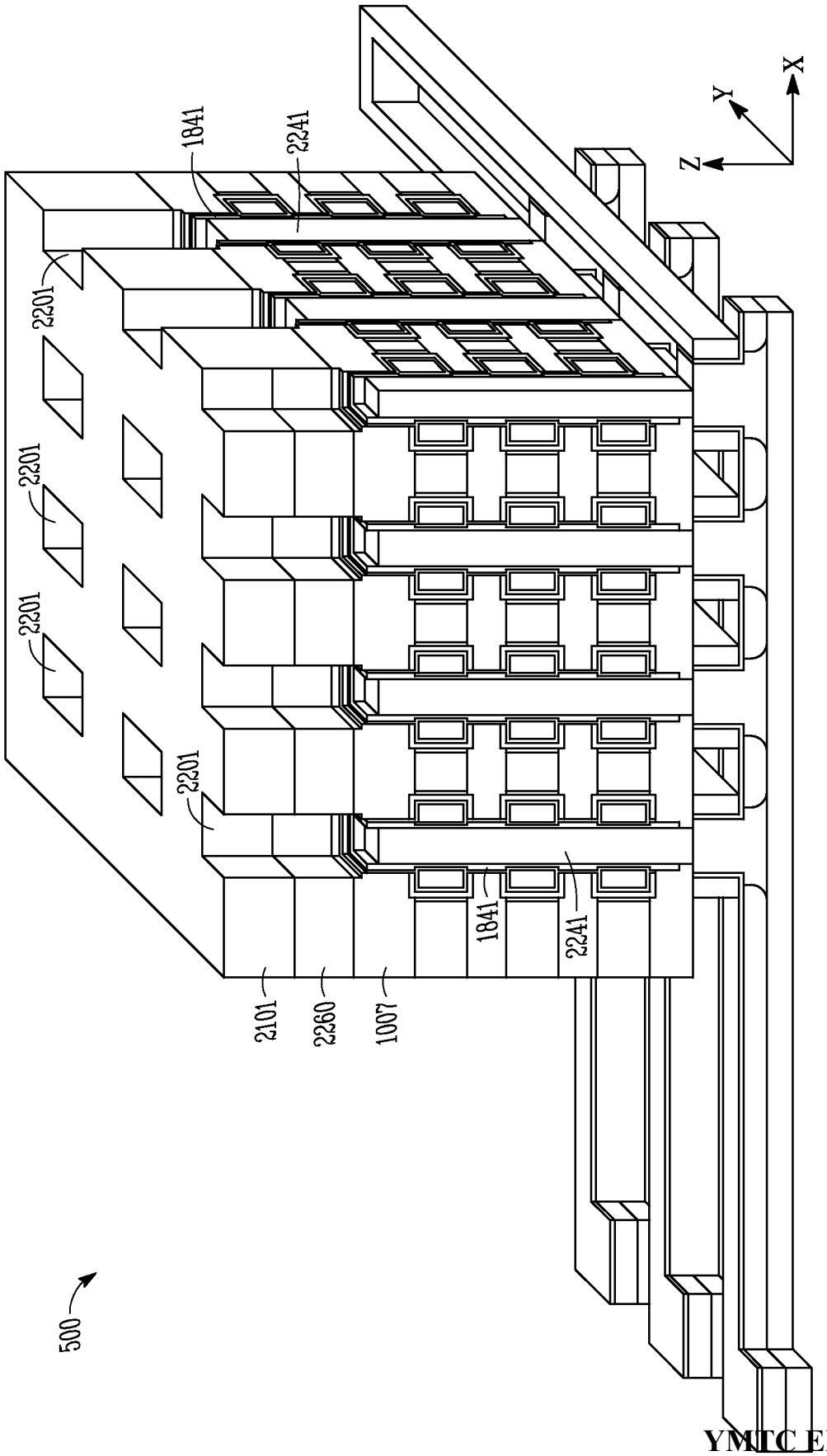

1841
2241
2201
2201
2201
2201
1841
2241
2101
2360
1007
500
Y
X
Z

FIG. 22

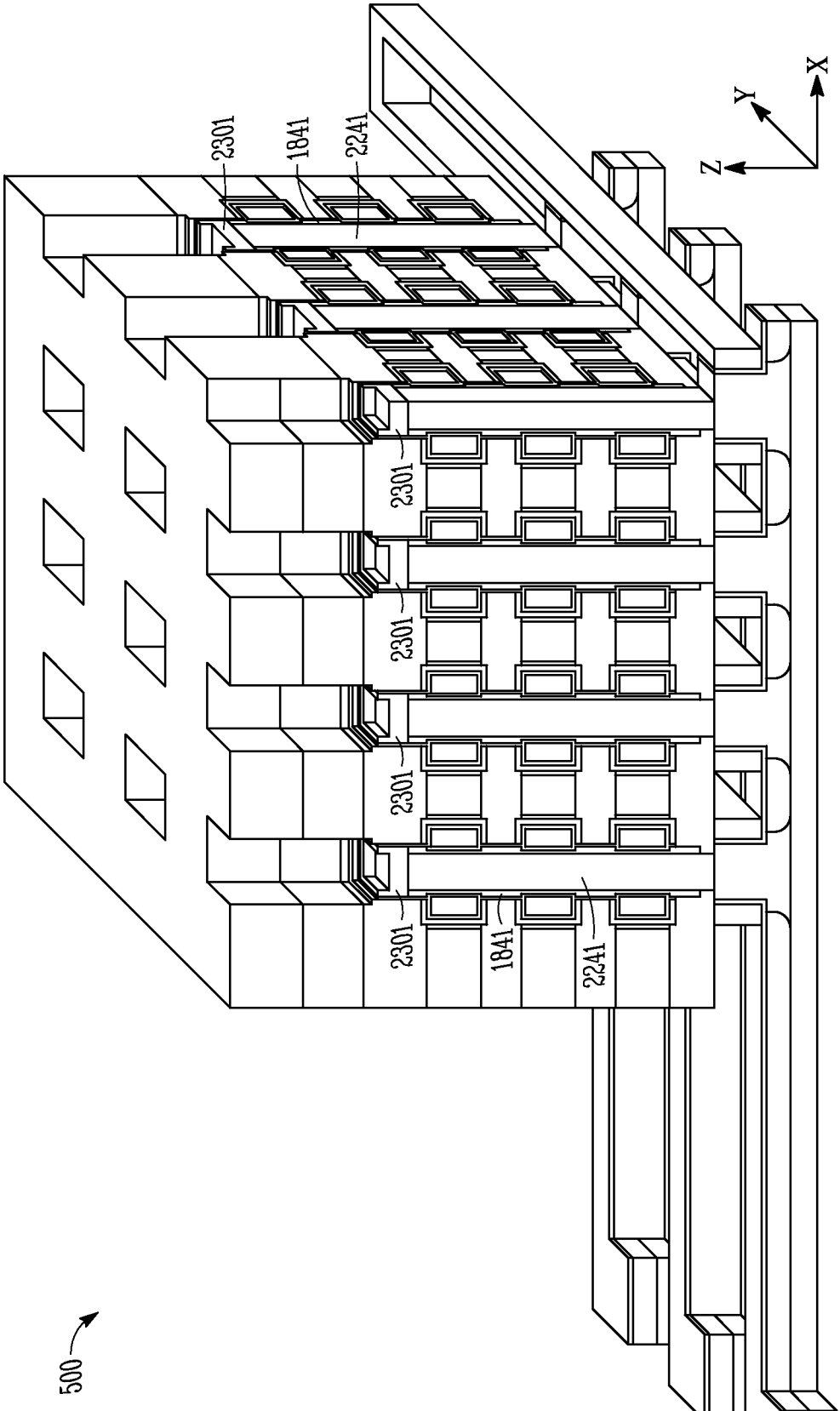


FIG. 23

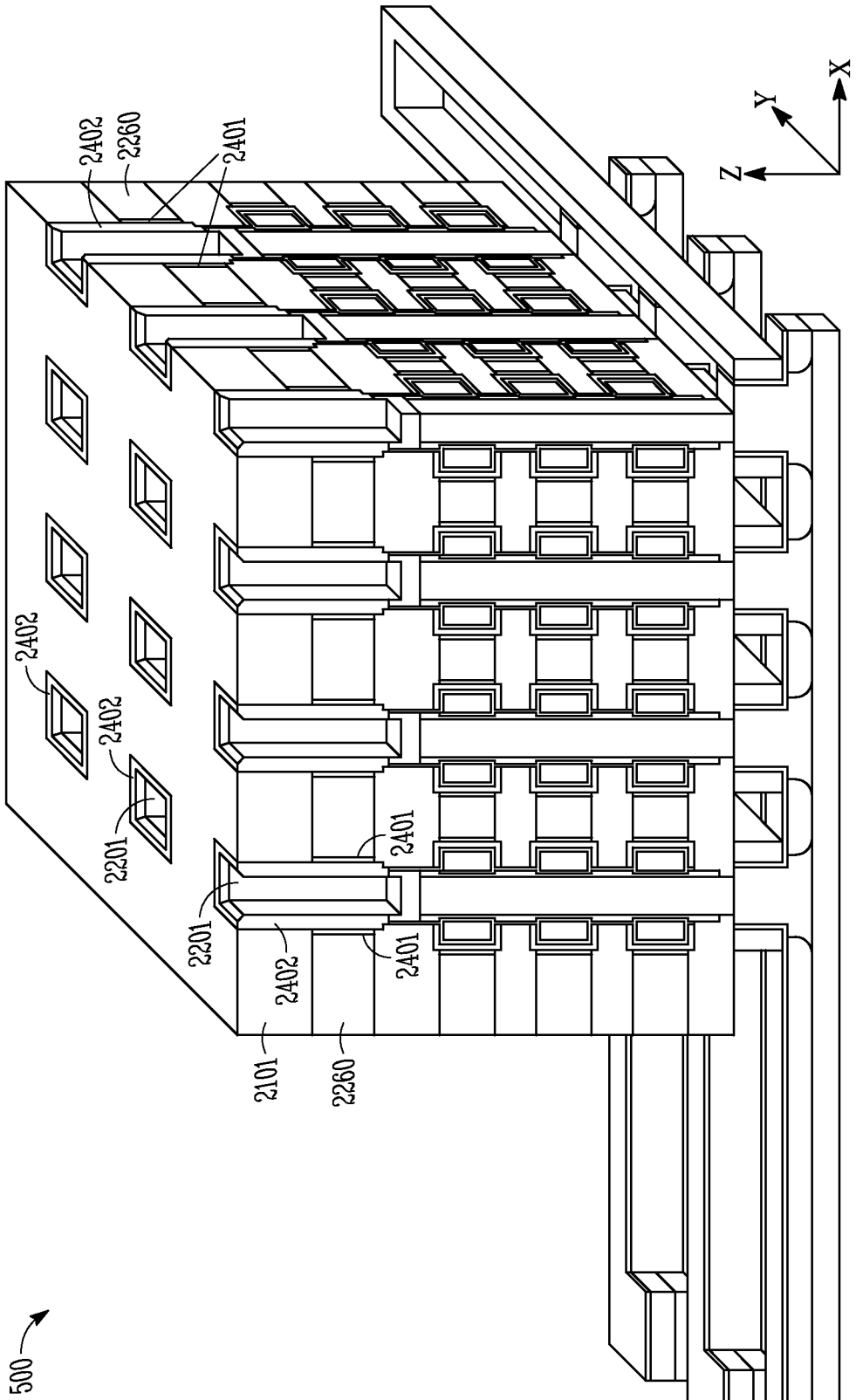

X
Y
Z
2402
2260
2401
2402
2402
2201
2401
2201
2402
2401
2101
2260
500

FIG. 24

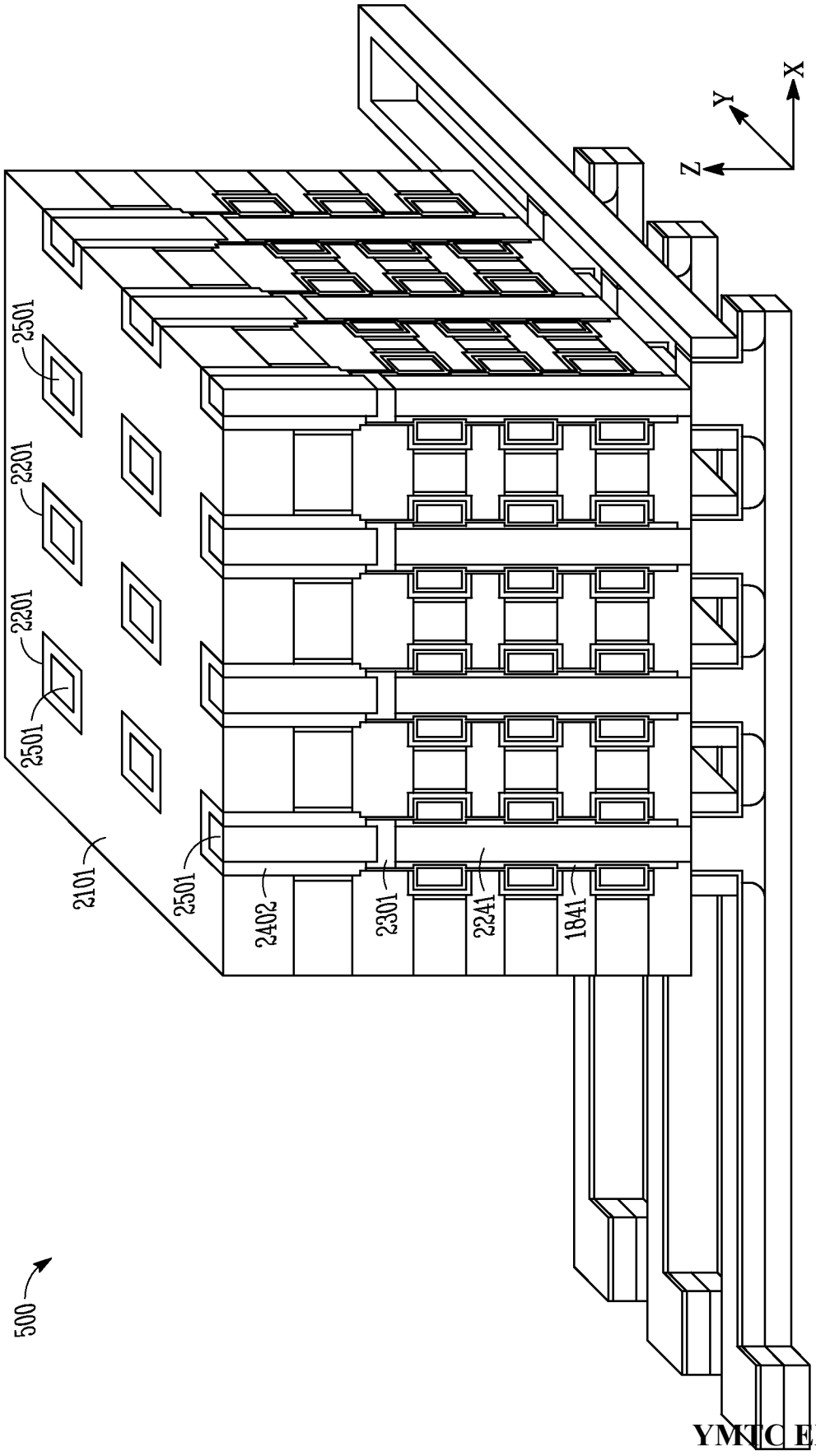


FIG. 25

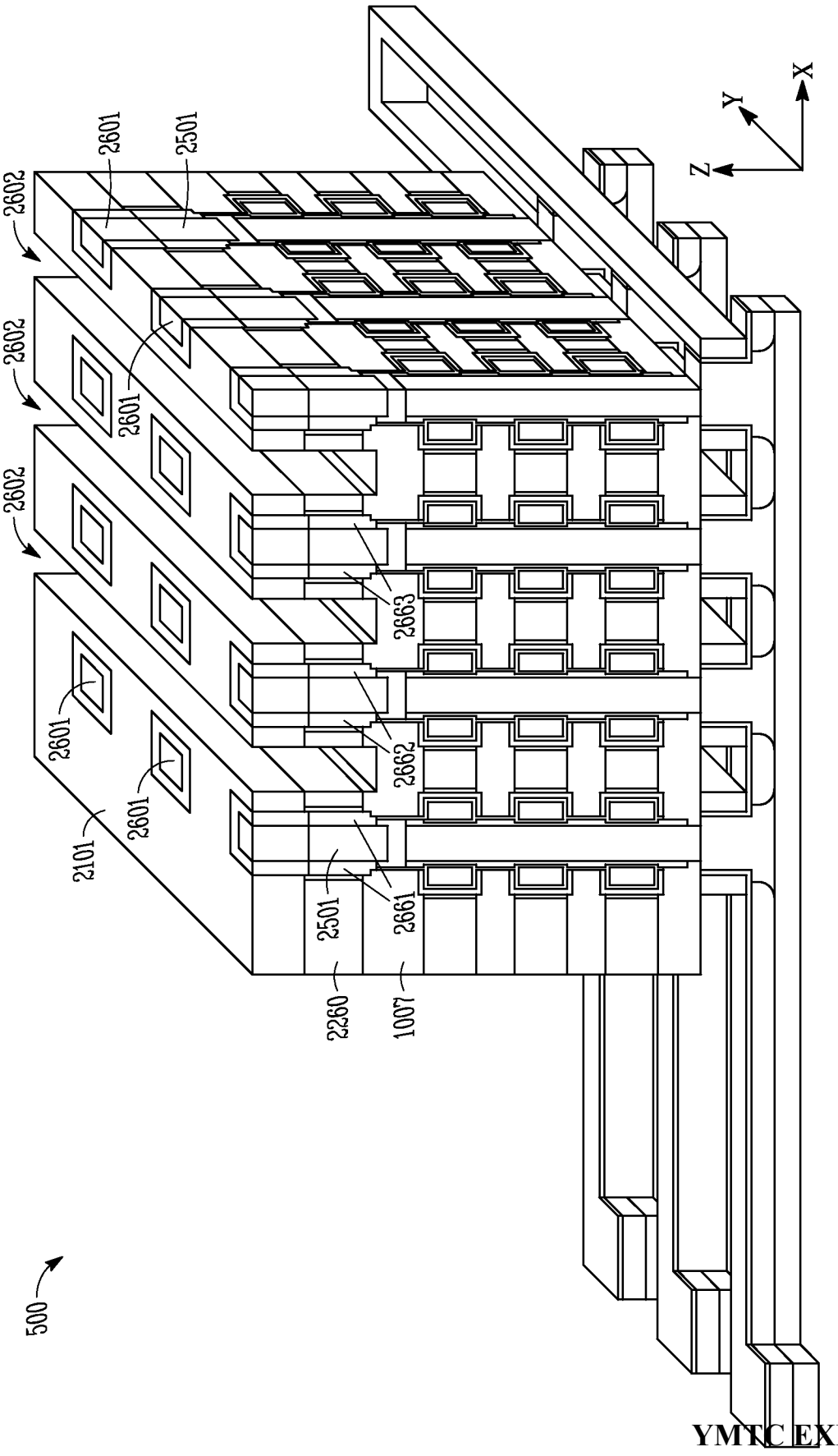

X
Y
Z
2602
2601
2501
2602
2601
2602
2663
2601
2662
2601
2101
2501
2661
2260
1007
500

FIG. 26

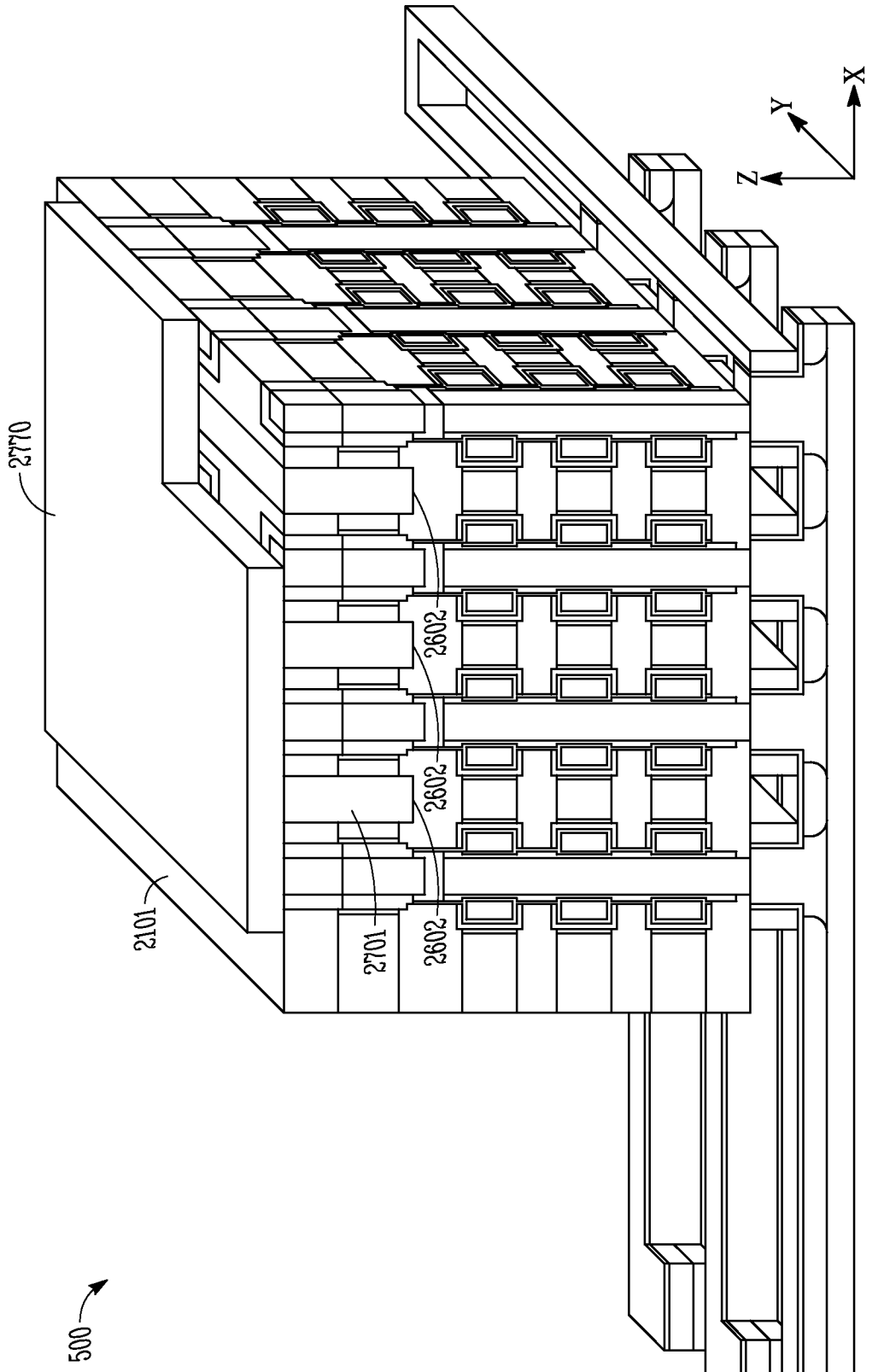


FIG. 27

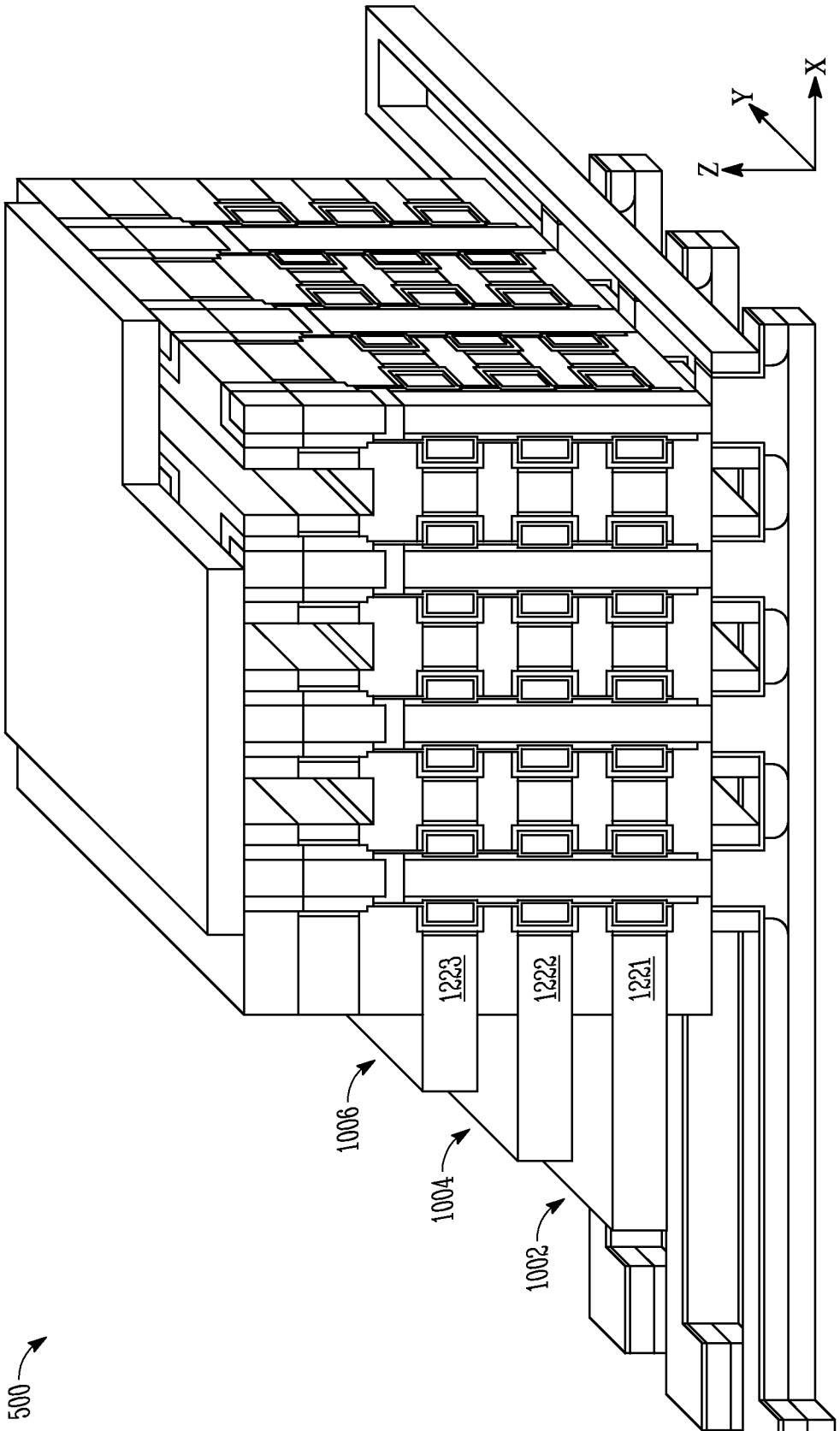


FIG. 28

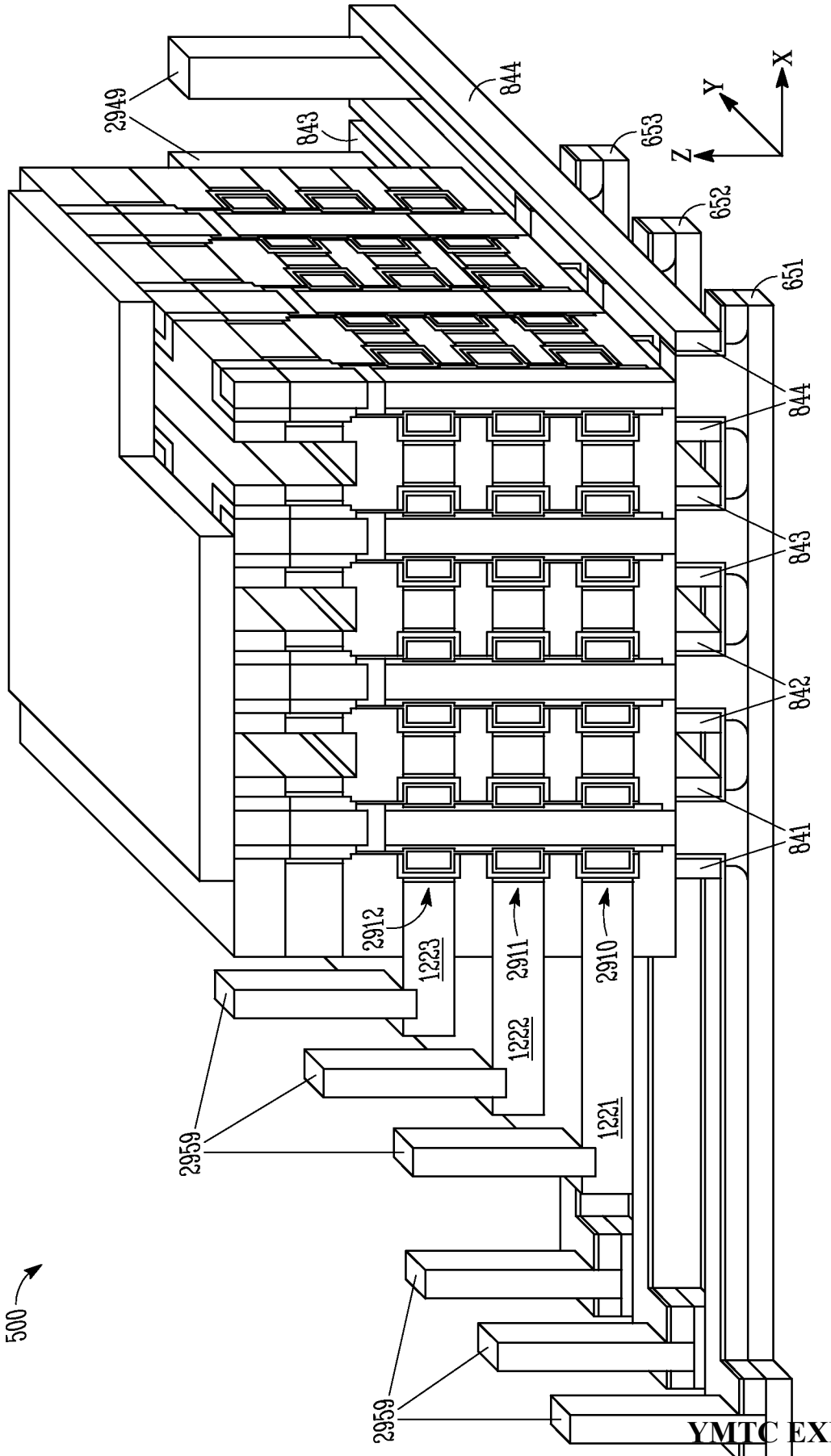

2949
844
843
653
652
651
Y
X
Z
844
843
842
841
2912
2911
2910
1223
1222
1221
2959
2959
500

FIG. 29

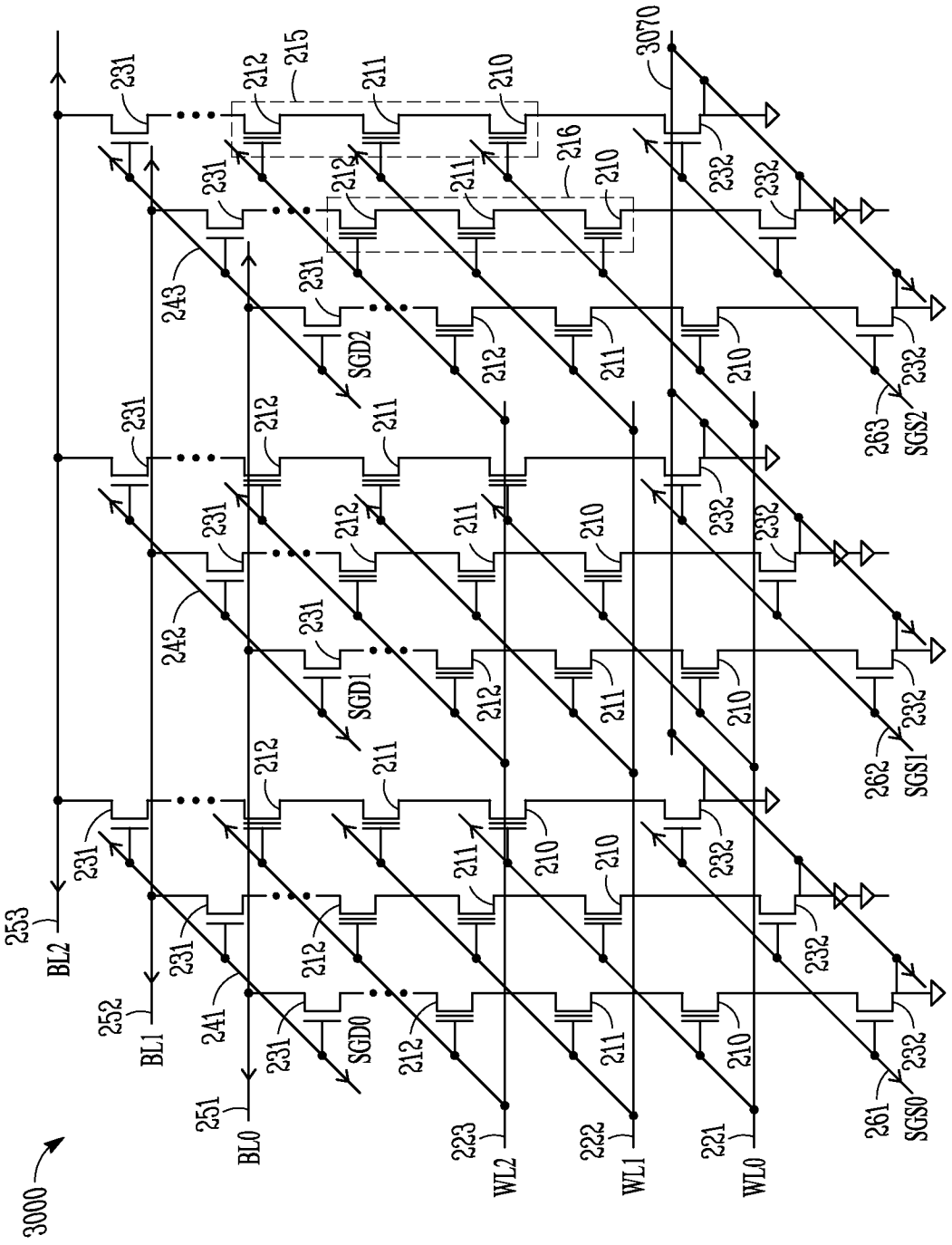

3000
3070
231
212
215
211
210
216
232
243
242
241
SGD2
SGD1
SGD0
263
SGS2
262
SGS1
261
SGS0
253
BL2
252
BL1
251
BL0
223
WL2
222
WL1
221
WL0

FIG. 30

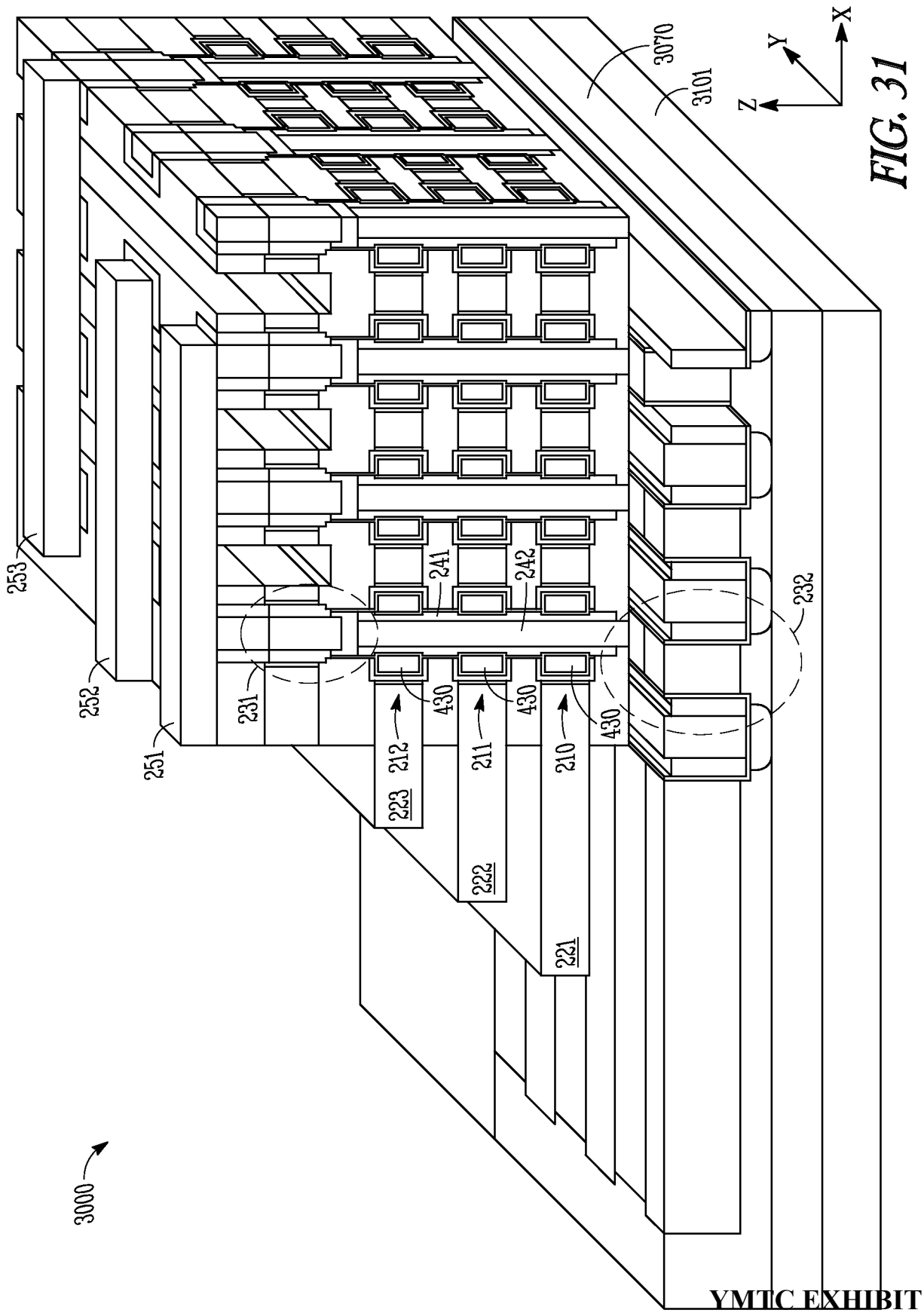

3070
3101
X
Y
Z
253
252
251
231
241
242
232
430
212
211
210
223
222
221
3000

FIG. 31

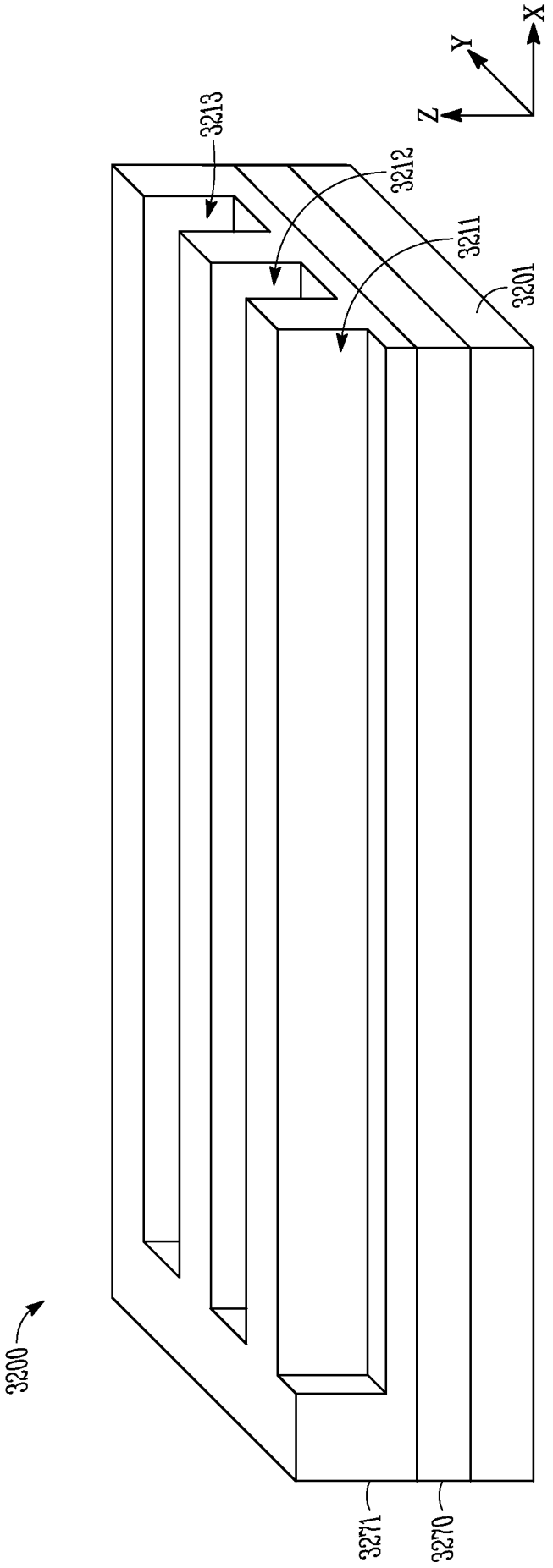


FIG. 32

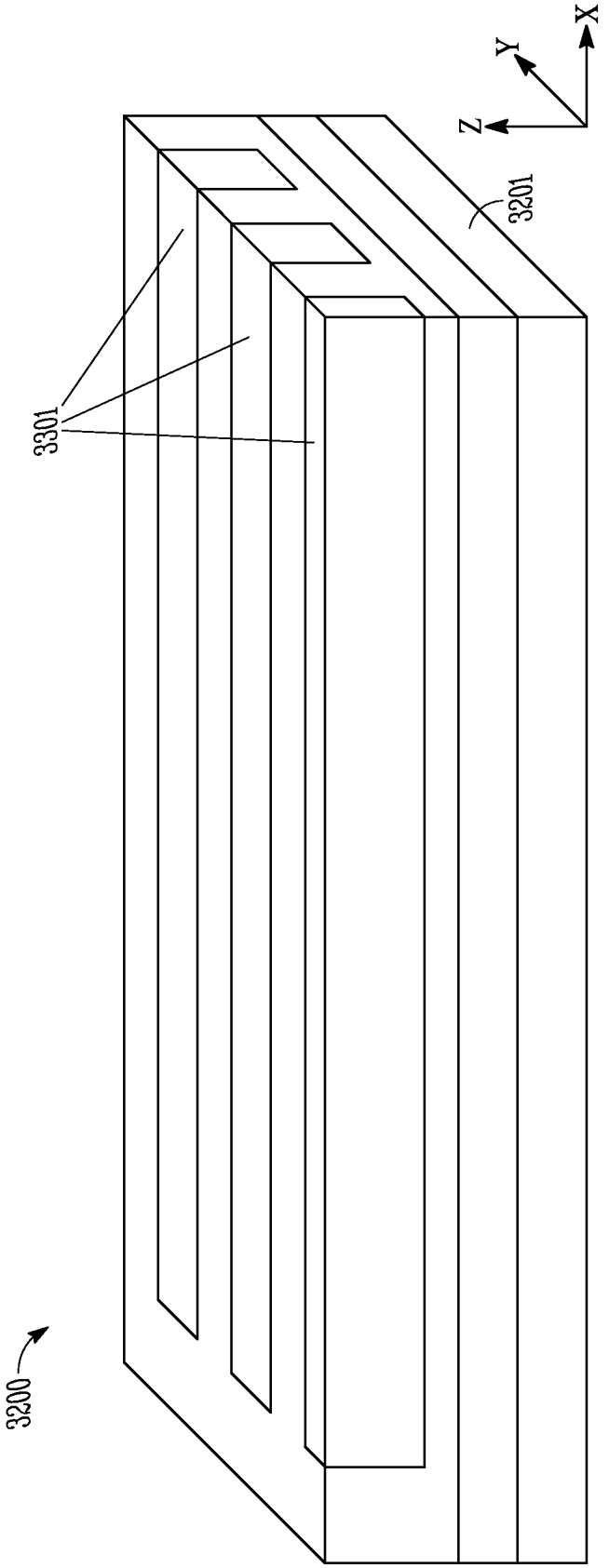


FIG. 33

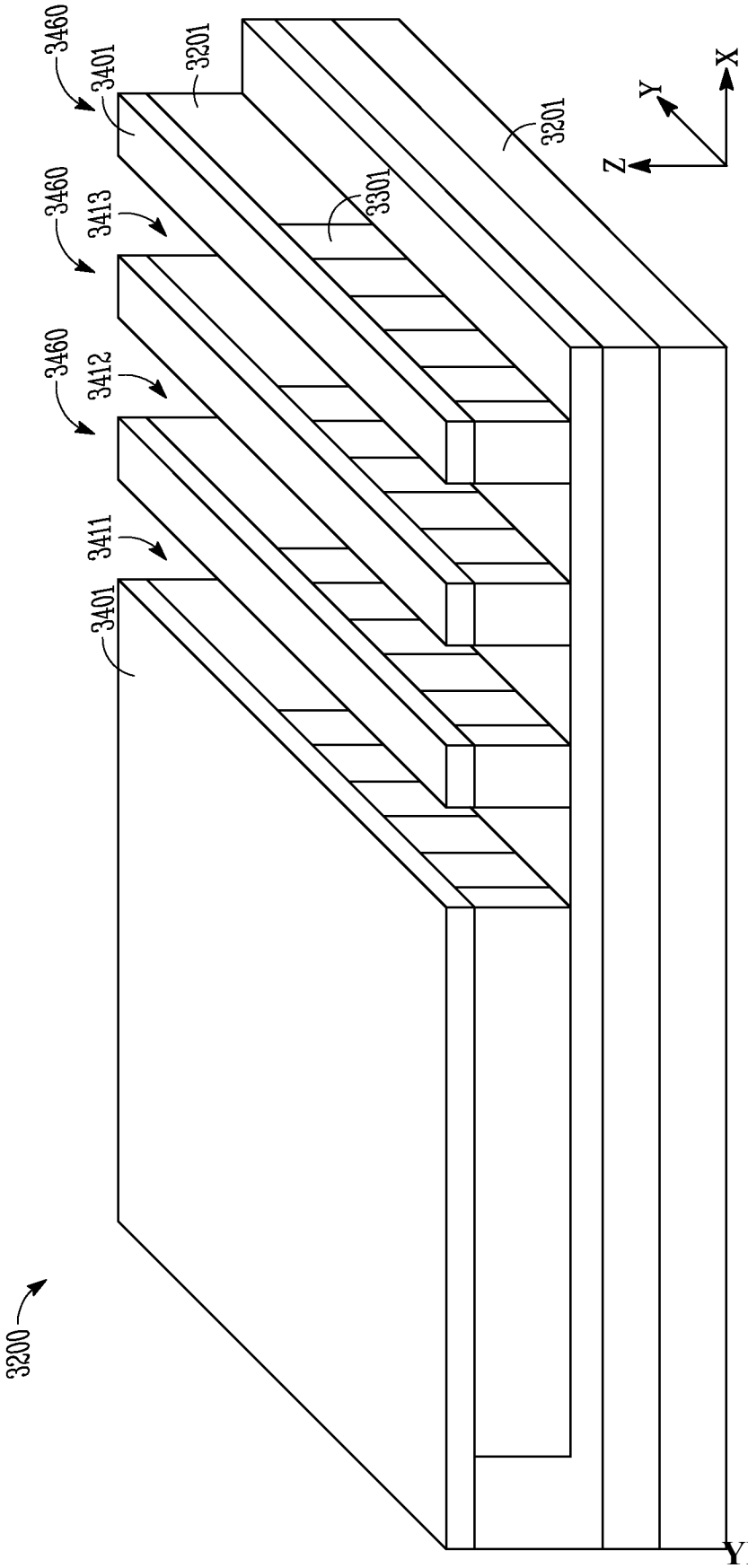

3460
3401
3201
3201
Y
X
Z
3460
3413
3301
3460
3412
3411
3401
3200

FIG. 34

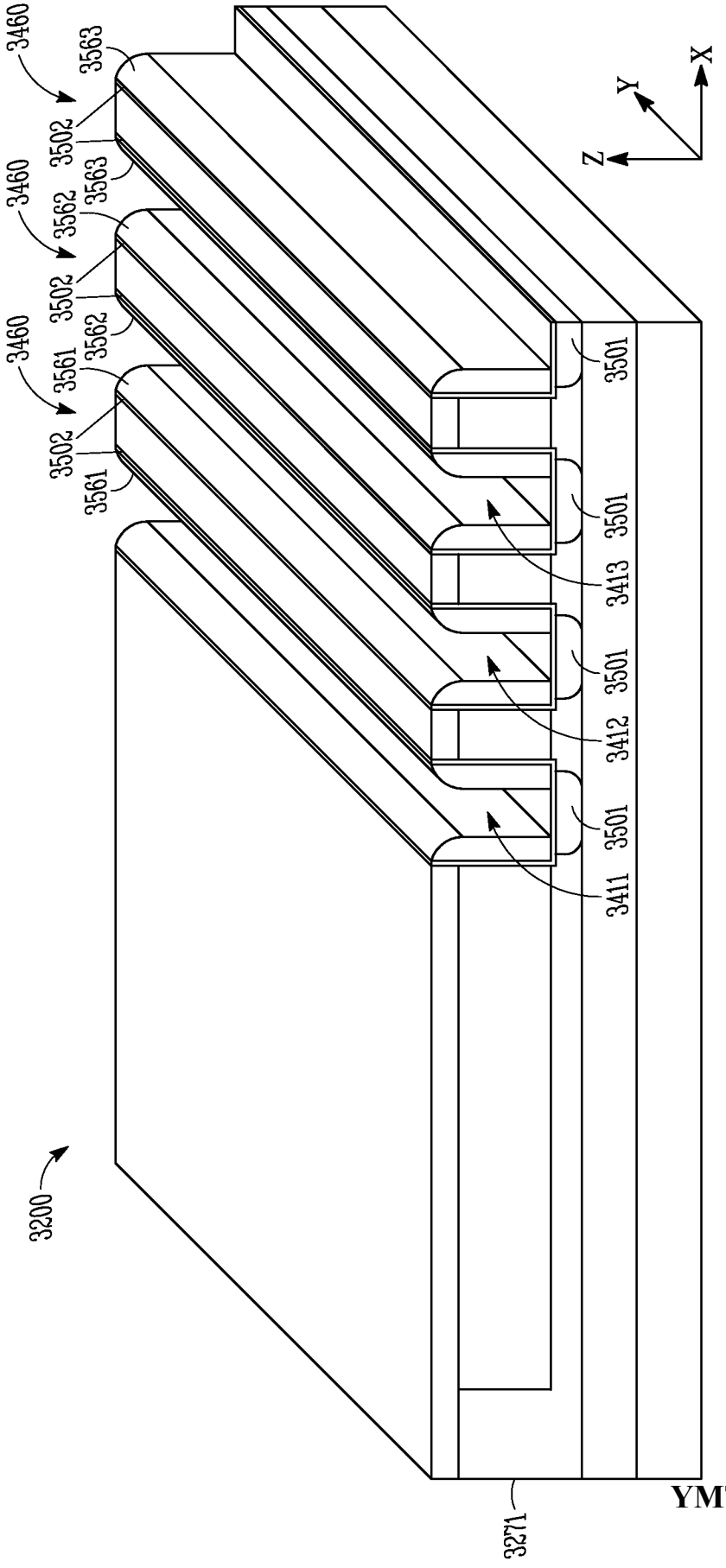

3460
3563
3502
3460
3563
3562
3502
3460
3562
3561
3502
3561
3501
3501
3413
3501
3412
3501
3411
3200
3271
Y
X
Z

FIG. 35

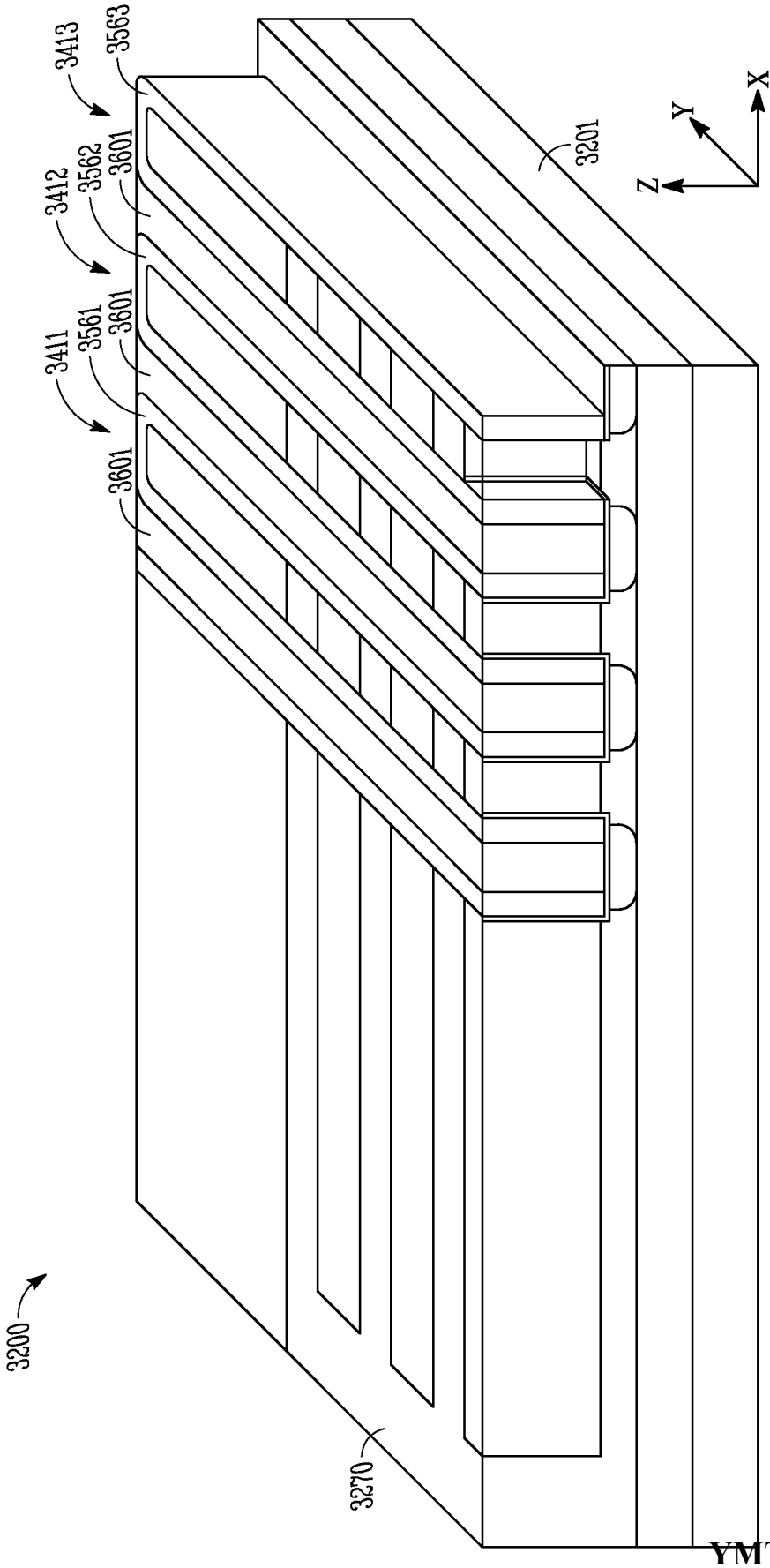

3413
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3412
3562
3601
3411
3561
3601
3601
3201
Y
X
Z
3200
3270

FIG. 36

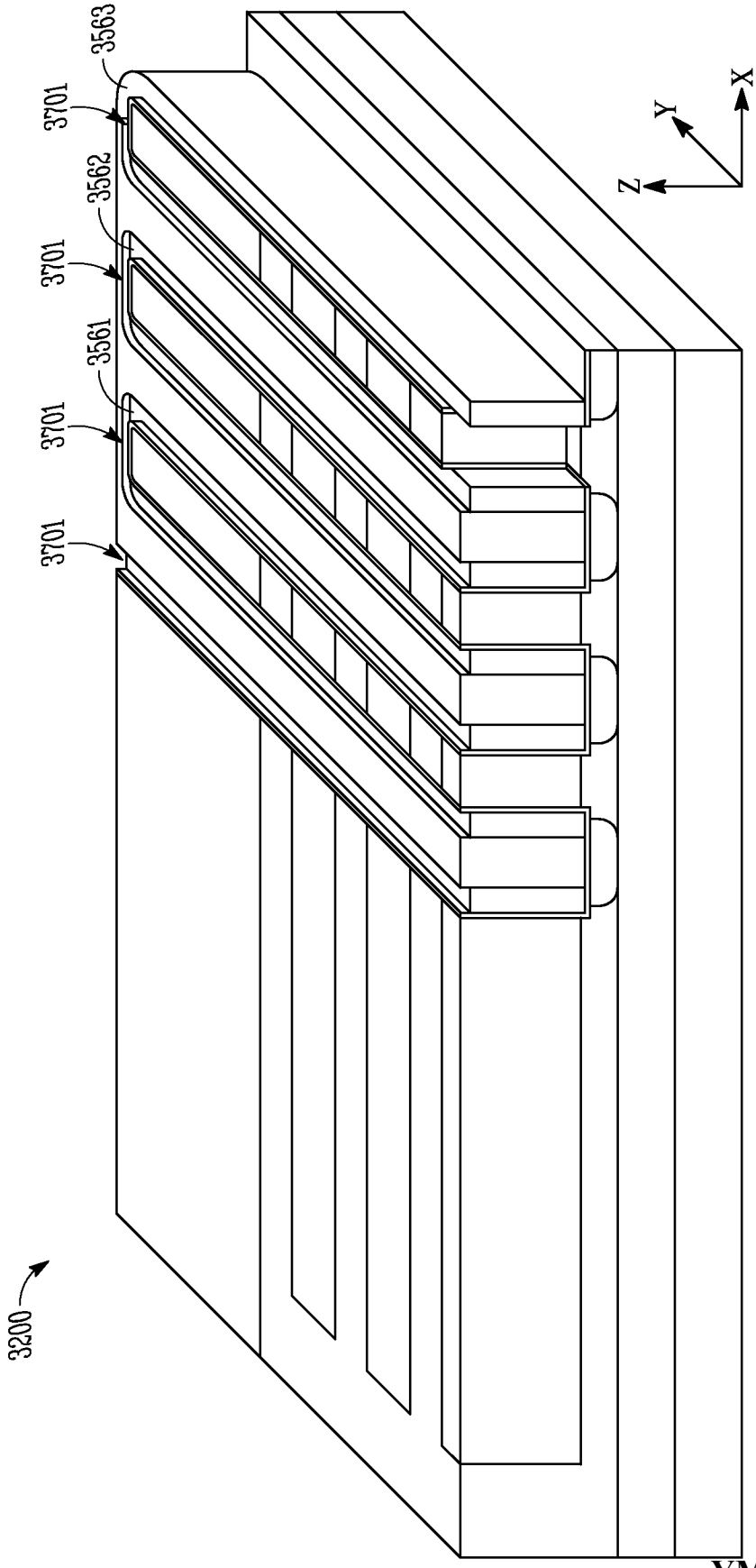


FIG. 37

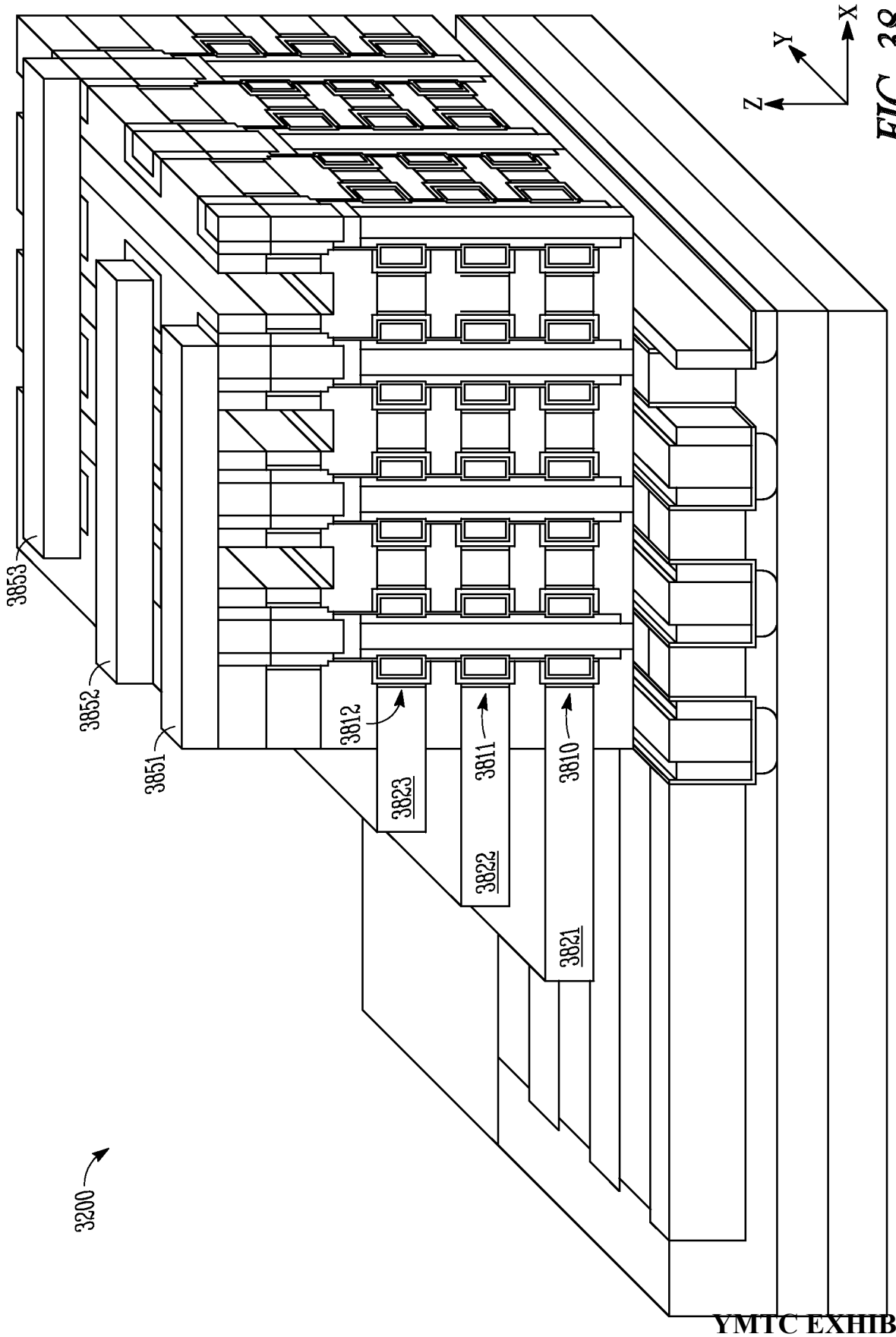


FIG. 38

Electronic Acknowledgement Receipt

EFS ID:	13690808
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Kevin R. Greenleaf/Amy Moriarty
Filer Authorized By:	Kevin R. Greenleaf
Attorney Docket Number:	303.B12US1
Receipt Date:	07-SEP-2012
Filing Date:	28-JUN-2010
Time Stamp:	18:26:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303b12us1SIGNEDoaresp.pdf	1339867 be3c45b00043968426dd6379414f47794a361790	yes	52

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Amendment/Req. Reconsideration-After Non-Final Reject	2	2
	Claims	3	8
	Applicant Arguments/Remarks Made in an Amendment	9	14
	Drawings-only black and white line drawings	15	52
Warnings:			
Information:			
	Total Files Size (in bytes):	1339867	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010	Due Date:	September 7, 2012
Examiner:	Unknown	Group Art Unit:	2823
Customer No.:	73115	Confirmation No.:	1275

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X Amendment and Response under 37 C.F.R. § 1.111 (13 pgs.)
X Formal Drawings (38 pgs.)

If not provided for in a separate paper filed herewith, please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/825,211	06/28/2010	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 09/07/2012	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 21	Minus	** 34	= 0	X $ =		OR	X $60=	0
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/DEBORAH PORTER/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

73115 7590 06/07/2012

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
JEAN BAPTISTE, WILNER	
ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
06/07/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@slwip.com
SLW@blackhillsip.com

Office Action Summary	Application No.	Applicant(s)	
	12/825,211	TANG ET AL.	
	Examiner	Art Unit	
	WILNER JEAN BAPTISTE	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2012*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-34* is/are pending in the application.

5a) Of the above claim(s) *22-34* is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-21* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *21 January 2012* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/30/2011*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

YMTC EXHIBIT 1002

DETAILED ACTION

Oath/Declaration

1. The Oath/Declaration filed on 06/28/2010, is acceptable.

Information Disclosure Statement

2. The information disclosure statements (IDS) were submitted on the following: 06/30/2011. The submissions are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

Election/Restrictions

3. Applicant's election without traverse of claims 1-21 in the reply filed on 03/22/2012 is acknowledged. This application contains claims 22-34 drawn to an invention nonelected with traverse in the reply filed on 03/22/2012. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Claim Objections

4. Claim 1 is objected to because of the following informalities: in line 2, “first memory cells” should be “a first memory cells”; in line 3, “second memory cells” should be “a second memory cells”. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained through the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The examination guidelines for determining obviousness under 35 U.S.C. 103 are described in MPEP 2141-2145.

The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-6, 9-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pekny US 2009/0230454 A1.

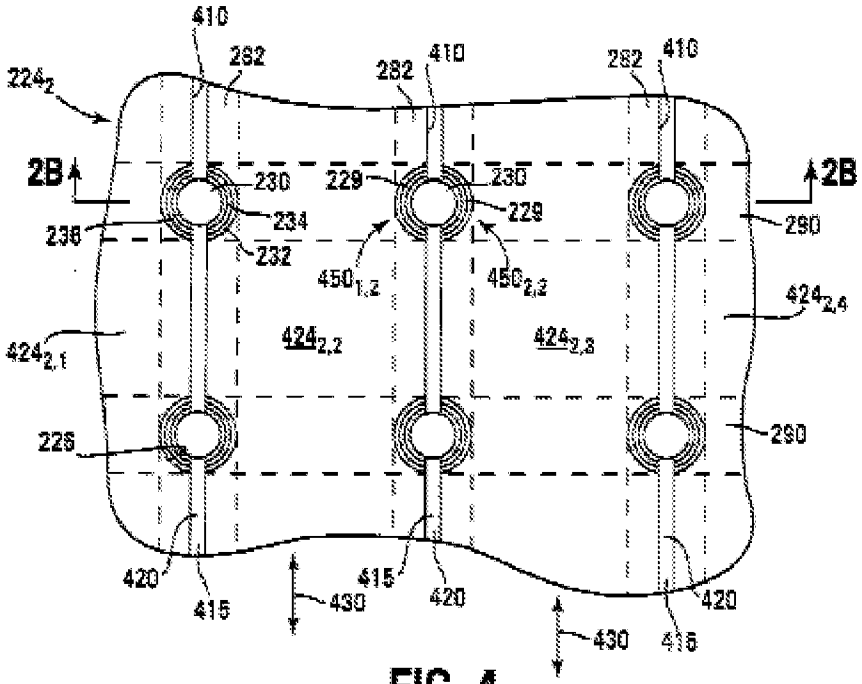


FIG. 4

7. In re-claim 1, **Pekny** illustrates **figs. 3-4**, [**0034-40**], an apparatus comprising:

- first memory cells $\mathbf{450_{1,2}}$ located in a first device level of a memory device;
- second memory cells $\mathbf{450_{2,2}}$ located in a second device level of the memory device;
- a first control gate $\mathbf{424_{2,1}}$ formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and
- a second control gate $\mathbf{424_{2,2}}$ formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the

second memory cells includes a memory element formed in a cavity **226** of the second control gate.

Pekny discloses a first memory cells, a second memory cells, a first control gate, a second control gate, but, Pekny does not specifically structure the second control gate to control access to the second memory cells as "each of the second memory cells includes a memory element formed in a cavity". **Pekny** discloses in the abstract "For example, a first memory cell can have a first control gate on the first side of the conductive pillar and a first charge trap interposed between the first side of the conductive pillar and the first control gate. A second memory cell can have a second control gate on the second side of the conductive pillar and a second charge trap interposed between the second side of the conductive pillar and the second control gate". It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a second control gate to control access to the second memory cells, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

8. In re-claim 2, **Pekny** illustrates the apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:

- a common source [**0042**]; and

- data lines **290** configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions [**0041-42**].

9. In re-claim 3, **Pekny** illustrates the apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation [**0041-42**].

10. In re-claim 4, **Pekny** illustrates the apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate [**0041-42**].

11. In re-claim 5, **Pekny** illustrates the apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells [**0009**].

12. In re-claim 6, **Pekny** illustrates the apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells [**0009**].

13. In re-claim 9, **Pekny** illustrates **figs. 3-4**, [**0034-40**], an apparatus comprising:

- a first non-volatile memory cell **$450_{1,2}$** including a first memory element, the first memory element having a ring shape;
- a second non-volatile memory cell **$450_{2,2}$** including a second memory element, the second memory element having a ring shape; and
- a conductive material extending through the first and second memory elements **fig. 4**.

14. In re-claim 10, **Pekny** illustrates the apparatus of claim 9, further comprising:

- a first additional conductive material **$424_{2,1}$** configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located **figs. 3-4**, [**0034-40**]; and
- a second additional conductive material **$424_{2,2}$** configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device **figs. 3-4**, [**0034-40**].

15. In re-claim 11, **Pekny** illustrates the apparatus of claim 10, wherein each of the memory cells further includes a first dielectric **202** between the respective memory element and the conductive material [**0021-22**].

16. In re-claim 12, **Pekny** illustrates the apparatus of claim 11, wherein each of the memory cells further includes a second dielectric **206** between the respective memory element and the respective additional conductive material [**0023**].

17. In re-claim 13, **Pekny** illustrates the apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell [**0041-42**].

18. In re-claim 14, **Pekny** illustrates the apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line [**0041-42**].

19. In re-claim 15, **Pekny** illustrates **figs. 3-4**, [**0034-40**], an apparatus comprising:

- a first conductive material $\mathbf{424_{2,1}}$ located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

- a second conductive material **$424_{2,2}$** located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;
- a first dielectric **202** formed on the first sidewall and the second sidewall [**0024**];
- a first memory element **$450_{1,2}$** located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;
- a second memory element **$450_{2,2}$** located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;
- a second dielectric **206** formed on a side of the first memory element and on a side of the second memory element [**0024**]; and
- a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric [**0025-26**].

Pekny discloses a first memory cells, a second memory cells, a first control gate, a second control gate, but, Pekny does not specifically structure the second control gate to control access to the second memory cells as “each of the second memory cells includes a memory element formed in a cavity”. **Pekny** discloses in the abstract “For example, a first memory cell can have a first control gate on the first side of the conductive pillar and a first charge trap interposed between the first side of the conductive pillar and the first control gate. A second memory cell can have a second

control gate on the second side of the conductive pillar and a second charge trap interposed between the second side of the conductive pillar and the second control gate". It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a second control gate to control access to the second memory cells, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

20. In re-claim 16, **Pekny** illustrates the apparatus of claim 15, wherein the first and second memory elements comprise polysilicon [**0027**].

21. In re-claim 17, **Pekny** illustrates the apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material [**0027**].

22. In re-claim 18, **Pekny** illustrates the apparatus of claim 17, wherein the dielectric material comprises silicon nitride [**0023**].

23. In re-claim 19, **Pekny** illustrates the apparatus of claim 15, further comprising dielectric material between the first and second conductive materials [**0025-26**].

24. In re-claim 20, **Pekny** illustrates the apparatus of claim 15, further comprising: a substrate [**0021**]; and a data line configured to be selectively coupled to the conductive

channel, wherein the data line is located between the second conductive material and the substrate [**0041-42**].

25. In re-claim 21, **Pekny** illustrates the apparatus of claim 15, further comprising: a substrate [**0021**]; and a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate [**0040-42**].

26. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pekny, and in view of Matsui et al. US 2007/0057310 A1.

27. In re-claim 7, **Pekny** illustrates the apparatus of claim 1, but silent regarding the transistors comprises a double-gate.

Matsui illustrates in [**0009**], further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the invention of Matsui to the invention of Pekny.

The motivation to do so is that the combination produces the predictable results of the delay caused by the resistance is increased so as to lower the performance of the element (Matsui, [0011]). See MPEP § 2144.07.

28. In re-claim 8, the combination of **Pekny** with **Matsui** illustrates the apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate (Matsui, [**0011**]).

29. **Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILNER JEAN BAPTISTE whose telephone number is (571)270-7394. The examiner can normally be reached on M-F FROM 7:30 AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, OLIK CHAUDHURI can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WILNER JEAN BAPTISTE/
Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 12/825,211	Applicant(s)/Patent Under Reexamination TANG ET AL.	
	Examiner WILNER JEAN BAPTISTE	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2009/0230454	09-2009	Pekny, Theodore T.	257/319
*	B	US-2007/0057310	03-2007	MATSUI et al.	257/314
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	12/825211.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 16:07
S2	15024	(257/314,E21.602,E29.255,E21.001).ccls. (438/128,309).ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:00
S3	233430	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:09
S4	9410	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:10
S5	2242	S3 and S4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:10
S6	59	S2 and S5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:11
S7	7282	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:53

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		hole))				
S8	11	S5 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:54
S9	38	S4 and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 17:59
S10	4266	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices)) and ((vias or holes or grooves) with dielectrics)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 18:07
S11	138	S7 and S10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 18:07
S12	233430	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S13	9410	((three-dimensional or 3D) same (3D adj memory adj device) or (3D near3 memory near3 device) or (3D same memory same device))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S14	2242	S12 and S13	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S15	4266	((Non-volatile adj memory adj devices) or (Non-volatile near4 memory near4 devices) or (Non-volatile same memory same devices) or (flash adj memory adj devices) or (flash near3 memory near3 devices) or (flash same memory same devices)) and ((vias or holes or grooves) with dielectrics)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:20
S16	183	S14 and S15	US-PGPUB; USPAT;	OR	ON	2012/05/30 20:20

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			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S17	183	S13 and S15	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:21
S18	138	S15 and ((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:22
S19	7282	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:38
S20	2541	438/128.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:39
S21	13	S19 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:40
S22	854	438/309.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:42
S23	317	Tang-Sanh-D.in. or Zahurak-John-K.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:43
S24	1	S19 and S23	US-PGPUB;	OR	ON	2012/05/30 20:45

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			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			20:44
S25	13	S19 and S20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/30 20:44
S26	2	12/047414.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 11:09
S27	3	("20040206996" | "20050133851" | "20080179659").PN. OR ("7906818").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2012/05/31 11:13
S28	7289	((first adj control adj gate) with (cavity or via or hole) or (first near3 control near3 gate) with (cavity or via or hole) or (first same control same gate) with (cavity or via or hole)) and ((second adj control adj gate) with (cavity or via or hole) or (second near3 control near3 gate) with (cavity or via or hole) or (second same control same gate) with (cavity or via or hole))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:51
S29	735	S28 and ((double adj gate) or (double near2 gate) or (double same gate))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:53
S30	31	S29 and ((257/314,E21.602,E29.255,E21.001).ccls. or (438/128,309).ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 14:54
S31	1	08/985182.app.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2012/05/31 15:12

5/31/2012 4:41:25 PM
C:\Users\wjeanbaptiste\Documents\EAST\Workspaces\12-825211 (three dimensional memory and method of forming).wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	Art Unit
	WILNER JEAN BAPTISTE	2823

SEARCHED			
Class	Subclass	Date	Examiner
257	314,E21.602,E29.255,E21.001	5/31/2012	wj
438	128, 309	5/31/2012	wj

SEARCH NOTES		
Search Notes	Date	Examiner
East	5/31/2012	wj

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

/W.J./ Examiner.Art Unit 2823	

PTO/SB/08A(04-07)
Modified form approved for use through 09/30/2007. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (Use as many sheets as necessary)	*Complete if Known*	
	Application Number	12/825,211
	Filing Date	June 28, 2010
	First Named Inventor	Sanh D. Tang
	Group Art Unit	2827
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: 303.B12US1	

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T 1

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS

Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 1
	KIM, JIYOUNG, et al., "Novel 3-D structure for ultra high density flash memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE)", 2008 Symposium on VLSI Technology, (June 17-19, 2008), 122-23	
	KOMORI, et al., "Disturbless flash memory due to high boost efficiency on BiCS structure and optimal memory film stack for ultra high density storage device", Electron Devices Meeting, 2008. IEDM 2008. IEEE International, (2008), 851-4	

EXAMINER	/Wilner Jean Baptiste/	DATE CONSIDERED	05/31/2012

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /W.J./

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12825211	TANG ET AL.
	Examiner	Art Unit
	WILNER JEAN BAPTISTE	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/31/2012								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
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	26	N								
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	29	N								
	30	N								
	31	N								
	32	N								
	33	N								
	34	N								

YMTC EXHIBIT 1002
Page 224 of 382

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sanh D. Tang et al.	Examiner:	Unknown
Serial No.:	12/825,211	Group Art Unit:	2823
Filed:	June 28, 2010	Docket:	303.B12US1
Customer No.:	73115	Confirmation No.:	1275
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

RESPONSE TO RESTRICTION REQUIREMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the Restriction Requirement mailed February 21, 2012, Applicants submit the following.

IN THE CLAIMS

1. (Original) An apparatus comprising:

first memory cells located in a first device level of a memory device;

second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate.

2. (Original) The apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. (Original) The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. (Original) The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. (Original) The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

6. (Original) The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

7. (Original) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

8. (Original) The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

9. (Original) An apparatus comprising:

a first non-volatile memory cell including a first memory element, the first memory element having a ring shape;

a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and

a conductive material extending through the first and second memory elements.

10. (Original) The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device.

11. (Original) The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. (Original) The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. (Original) The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell.

14. (Original) The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

15. (Original) An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second

sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

16. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

17. (Original) The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.

18. (Original) The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.

19. (Original) The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

20. (Original) The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

21. (Original) The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

22. (Withdrawn) A method comprising:

forming a first non-volatile memory cell including a first memory element having a ring shape;

forming a non-volatile second memory cell including a second memory element having a ring shape; and

forming a conductive material extending through the first and second memory elements.

23. (Withdrawn) The method of claim 22, wherein forming the first memory cell comprises forming a first cavity in a first conductive material, wherein the first memory element is formed in the first cavity, wherein forming the second memory cell comprises forming a second cavity in a second conductive material, and wherein the second memory element is formed in the second cavity.

24. (Withdrawn) The method of claim 23, wherein the first cavity is substantially aligned over the second cavity.

25. (Withdrawn) The method of claim 22, further comprising:

forming a data line over a substrate, wherein the data line is located between the substrate and the first and second memory cells.

26. (Withdrawn) The method of claim 22, further comprising:

forming a data line over a substrate, wherein the first and second memory cells are located between the substrate and the data line.

27. (Withdrawn) A method comprising:

forming conductive material layers and dielectric material layers such that the conductive material layers are electrically isolated from each other by the dielectric material layers;

forming cavities in each of the conductive material layers; and

forming a memory element in each of the cavities.

28. (Withdrawn) The method of claim 27, wherein each of the conductive material layers is between two of the dielectric material layers and at least one of the conductive material layers is between two of the conductive material layers.

29. (Withdrawn) The method of claim 27, wherein the memory element comprises polysilicon.

30. (Withdrawn) The method of claim 27, wherein the memory element comprises a dielectric material.

31. (Withdrawn) The method of claim 27, wherein forming the cavities includes:

forming initial cavities in the conductive material layers; and

enlarging a size of the initial cavities to form the cavities in each of the conductive material layers.

32. (Withdrawn) The method of claim 31, further comprising:

forming openings through the conductive material layers and the dielectric material layers to form the initial cavities.

33. (Withdrawn) The method of claim 32, wherein second cavities are formed in each of the dielectric material layers when the openings are formed, and a size of the second cavities remains substantially unchanged when the size of the initial cavities is enlarged.

34. (Withdrawn) The method of claim 33, wherein each of the second cavities and each of the initial cavities has a substantially same diameter.

REMARKS

This reply responds to the Restriction Requirement mailed on 21 February 2012.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-34 are pending in this application with claims 1-21 under examination. Consideration of the above-identified application is respectfully requested.

Election/Restriction Response

In response to the Restriction Requirement mailed 21 February 2012, Group I, which includes claims 1-21, is elected without traverse.

The right to reintroduce non-elected claims for reconsideration in this application upon the allowance of a linking claim or to reintroduce non-elected claims in one or more divisional applications at a later date is herein reserved.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney at (612) 373-6969 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 3-22-12 By /Viet Tong/

Viet V. Tong
Reg. No. 45,416

Electronic Acknowledgement Receipt

EFS ID:	12366580
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Suneel Arora/Amy Moriarty
Filer Authorized By:	Suneel Arora
Attorney Docket Number:	303.B12US1
Receipt Date:	22-MAR-2012
Filing Date:	28-JUN-2010
Time Stamp:	12:19:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303b12us1SIGNEDrr.pdf	71553 07925fbfbee9c7248fd51ed401407963449c adf2	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Response to Election / Restriction Filed	2	2
	Claims	3	9
	Applicant Arguments/Remarks Made in an Amendment	10	10
Warnings:			
Information:			
	Total Files Size (in bytes):	71553	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010	Due Date:	March 22, 2012
Examiner:	Unknown	Group Art Unit:	2823
Customer No.:	73115	Confirmation No.:	1275

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X Response to Restriction Requirement (9 pgs.)

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 22nd day of March, 2012.

Amy Moriarty — Name

/Amy Moriarty/ — Signature

PTO/SB/06 (07-06)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/825,211	Filing Date 06/28/2010	☐ To be Mailed

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
	03/22/2012	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	* 34	Minus	** 34	= 0	X $ =		OR	X $60=	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $250=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)					
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
AMENDMENT	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/MYRTLE LEIGH/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1	1275

73115 7590 02/21/2012

SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
JEAN BAPTISTE, WILNER	
ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
02/21/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

uspto@slwip.com
SLW@blackhillsip.com

Office Action Summary	Application No.	Applicant(s)	
	12/825,211	TANG ET AL.	
	Examiner	Art Unit	
	WILNER JEAN BAPTISTE	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *1* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2010*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-34* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☐ Claim(s) _____ is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☒ Claim(s) *1-34* are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

YMTC EXHIBIT 1002
Page 239 of 382

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-21, drawn to drawn to a memory semiconductor device, classified in class 257, subclass 314.

II. Claims 22-34 drawn to a method of forming a memory semiconductor device, classified in class 438, subclass 128.

The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case, the product as claimed can be made by another and materially different process. For example, the step of "forming a memory element in each of the cavity" is not required for the device structure.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

2. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WILNER JEAN BAPTISTE whose telephone number is (571)270-7394. The examiner can normally be reached on M-F FROM 7:30 AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, CHAUDHURI OLIK can be reached on 571-272-9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/WILNER JEAN BAPTISTE/

Examiner, Art Unit 2823

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1

CONFIRMATION NO. 1275

PUBLICATION NOTICE

73115
SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

OC000000051742597

Title:THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Publication No.US-2011-0316063-A1
Publication Date:12/29/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

YMTC EXHIBIT 1002
Page 243 of 382

PTO/SB/08A(04-07)
Modified form approved for use through 09/30/2007. OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** (Use as many sheets as necessary)	*Complete if Known*	
	Application Number	12/825,211
	Filing Date	June 28, 2010
	First Named Inventor	Sanh D. Tang
	Group Art Unit	2827
	Examiner Name	Unknown
Sheet 1 of 1	Attorney Docket No: 303.B12US1	

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

Examiner Initial *	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	T 1

OTHER DOCUMENTS – NON PATENT LITERATURE DOCUMENTS

Examiner Initial *	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 1
	KIM, JIYOUNG, et al., "Novel 3-D structure for ultra high density flash memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE)", 2008 Symposium on VLSI Technology, (June 17-19, 2008), 122-23	
	KOMORI, et al., "Disturbless flash memory due to high boost efficiency on BiCS structure and optimal memory film stack for ultra high density storage device", Electron Devices Meeting, 2008. IEDM 2008. IEEE International, (2008), 851-4	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt

EFS ID:	10435148
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Barbara Jean Clark/Judy Dent
Filer Authorized By:	Barbara Jean Clark
Attorney Docket Number:	303.B12US1
Receipt Date:	30-JUN-2011
Filing Date:	28-JUN-2010
Time Stamp:	22:23:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		signed_303-B12US1.pdf	1068689 4e7906369e5a7577dc2a2311347341042d770884	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Transmittal Letter	2	3
	Information Disclosure Statement (IDS) Form (SB08)	4	4

Warnings:					
Information:					
2	Non Patent Literature	0001_kim_12223.pdf	483788 cc4dd237e08fc126fcb6453d33a372dbe8b30d79	no	2
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Information:					
3	Non Patent Literature	0002_komoridisturbless.pdf	1437442 9a535b9e45273b8482aabe0df7beb7f6352ce876	no	4
Warnings:					
Information:					
		Total Files Size (in bytes):	2989919		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010	Due Date:	N/A
Examiner:	Unknown	Group Art Unit:	2827
Customer No.:	73115	Confirmation No.:	1275

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.) Copies of Cited References (2).

If not provided for in a separate paper filed herewith, please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: / Viet Tong /
Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 30th day of June, 2011.

Judy Dent
Name

/ Judy Dent /
Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sanh D. Tang et al.	Examiner: Unknown	
Serial No.:	12/825,211	Group Art Unit: 2827	
Filed:	June 28, 2010	Docket: 303.B12US1	
Customer No.: 73115		Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

INFORMATION DISCLOSURE STATEMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached PTO 1449 Form be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the PTO 1449 Form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. § 1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

Pursuant to 37 C.F.R. § 1.98(a)(2), copies of cited U.S. Patents and Published Applications, and Non-Published Applications identifiable by USPTO Serial Number, are no longer required to be provided to the Office. Applicants acknowledge the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R § 1.98(a)(2).

The Examiner is invited to contact the undersigned at the telephone number indicated if there are any questions regarding this communication.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6969

Date 6-30-11 By / Viet Tong /
Viet V. Tong
VVT:jld Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 30th day of June, 2011.

Judy Dent /Judy Dent/
Name Signature

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Sanh D. Tang et al.	Examiner: Unknown	
Serial No.:	12/825,211	Group Art Unit: 2827	
Filed:	June 28, 2010	Docket No.: 303.B12US1	
Customer No.:	73115	Confirmation No.: 1275	
Title:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME		

PRELIMINARY AMENDMENT

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Prior to taking up this application for examination, please enter the following amendments:

IN THE DRAWINGS

Corrected drawings are supplied herewith. Enclosed is a complete set of replacement sheets of drawings. FIG. 2 and FIG. 30 are amended.

REMARKS

FIG. 2 is amended to remove a vertical line in each of the symbols for transistors 231 coupled to line 253. FIG. 30 is amended to remove a vertical line coupling between the gate of transistor 232 and the gates of memory cells 210, 211, and 212 in string 216.

It is submitted that the amendments to FIG. 2 and FIG. 30 are made only to correct typographical errors. The amendments do not introduce new matter. Accordingly, consideration and approval of the replacement sheets of drawings is respectfully requested.

CONCLUSION

The Examiner is invited to telephone the undersigned at (612) 373-6969 to facilitate prosecution of this Application.

If necessary, please charge any additional fees or deficiencies, or credit any overpayments to Deposit Account No. 19-0743.

Respectfully Submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402--0938
(612) 373-6969

Date March 21, 2011 By /Viet Tong/
Viet V. Tong
Reg. No. 45,416

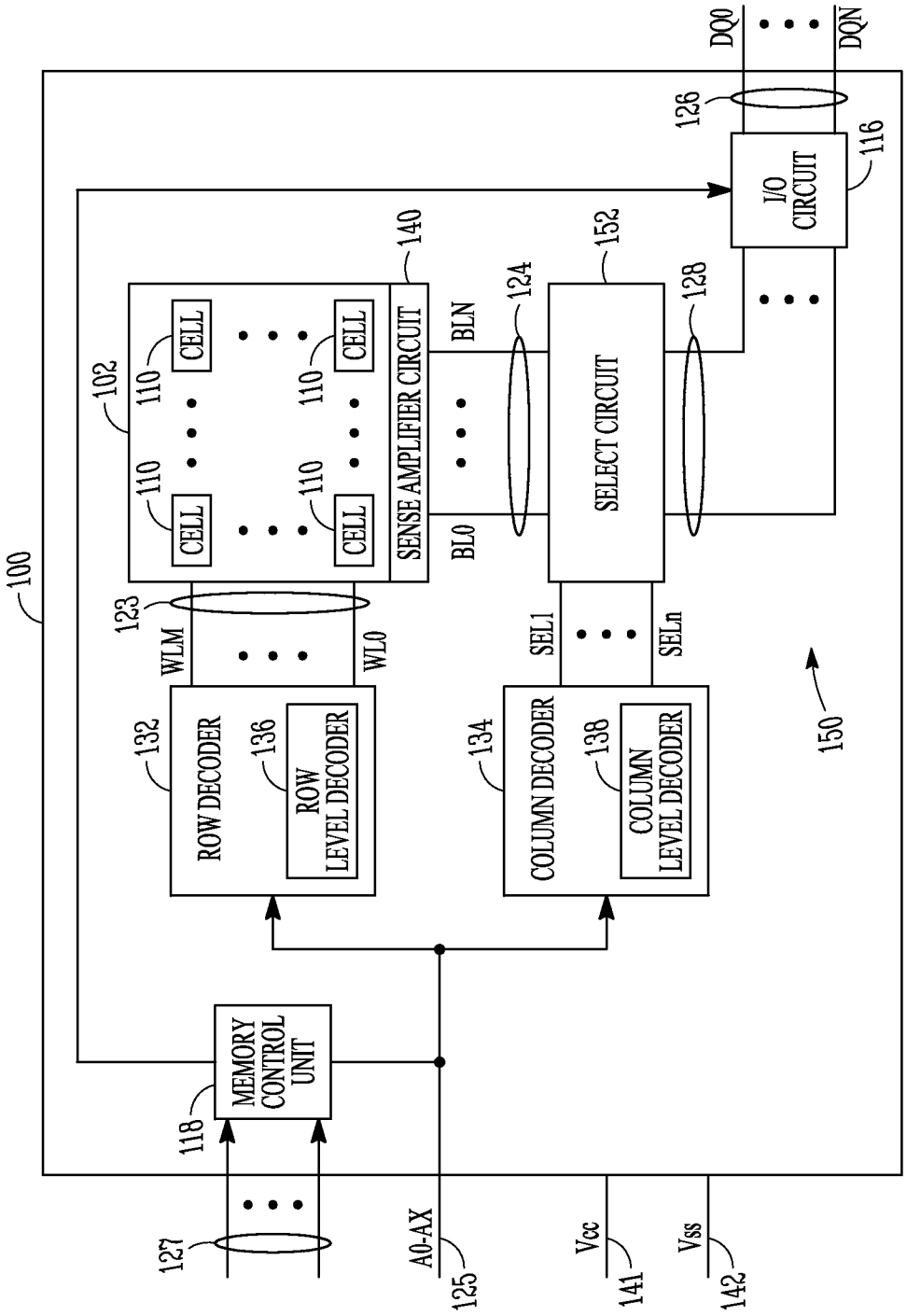

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102
110
CELL
123
WLM
WL0
BLN
BL0
140
SENSE AMPLIFIER CIRCUIT
124
152
SELECT CIRCUIT
128
126
DQ0
DQN
I/O CIRCUIT
116
SEL1
SELn
132
ROW DECODER
136
ROW LEVEL DECODER
134
COLUMN DECODER
138
COLUMN LEVEL DECODER
150
118
MEMORY CONTROL UNIT
127
A0-AX
125
Vcc
141
Vss
142

FIG. 1

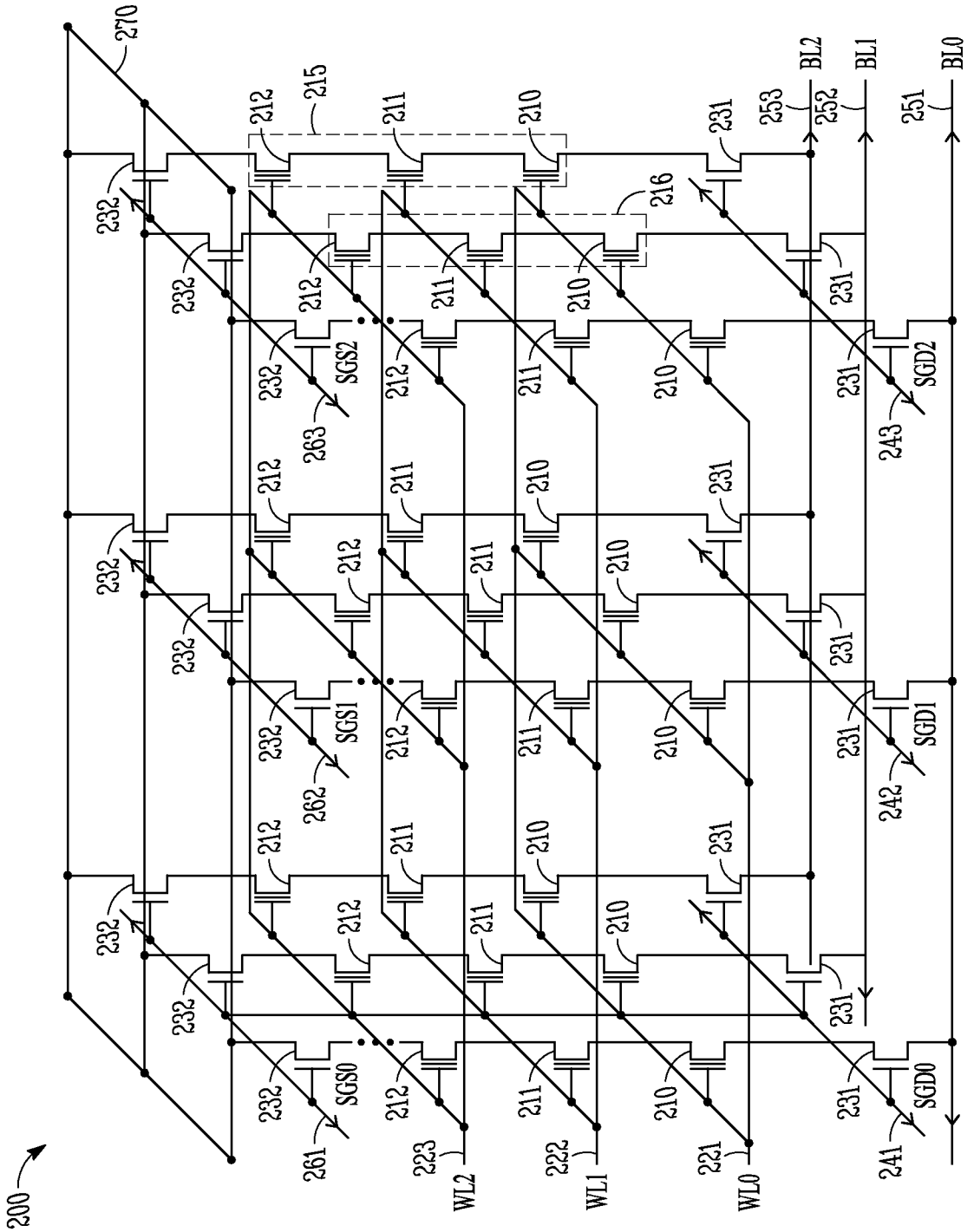

200
270
212
215
211
210
231
253
252
251
BL2
BL1
BL0
216
232
SGS2
SGS1
SGS0
SGD2
SGD1
SGD0
263
262
261
243
242
241
223
222
221
WL2
WL1
WL0

FIG. 2

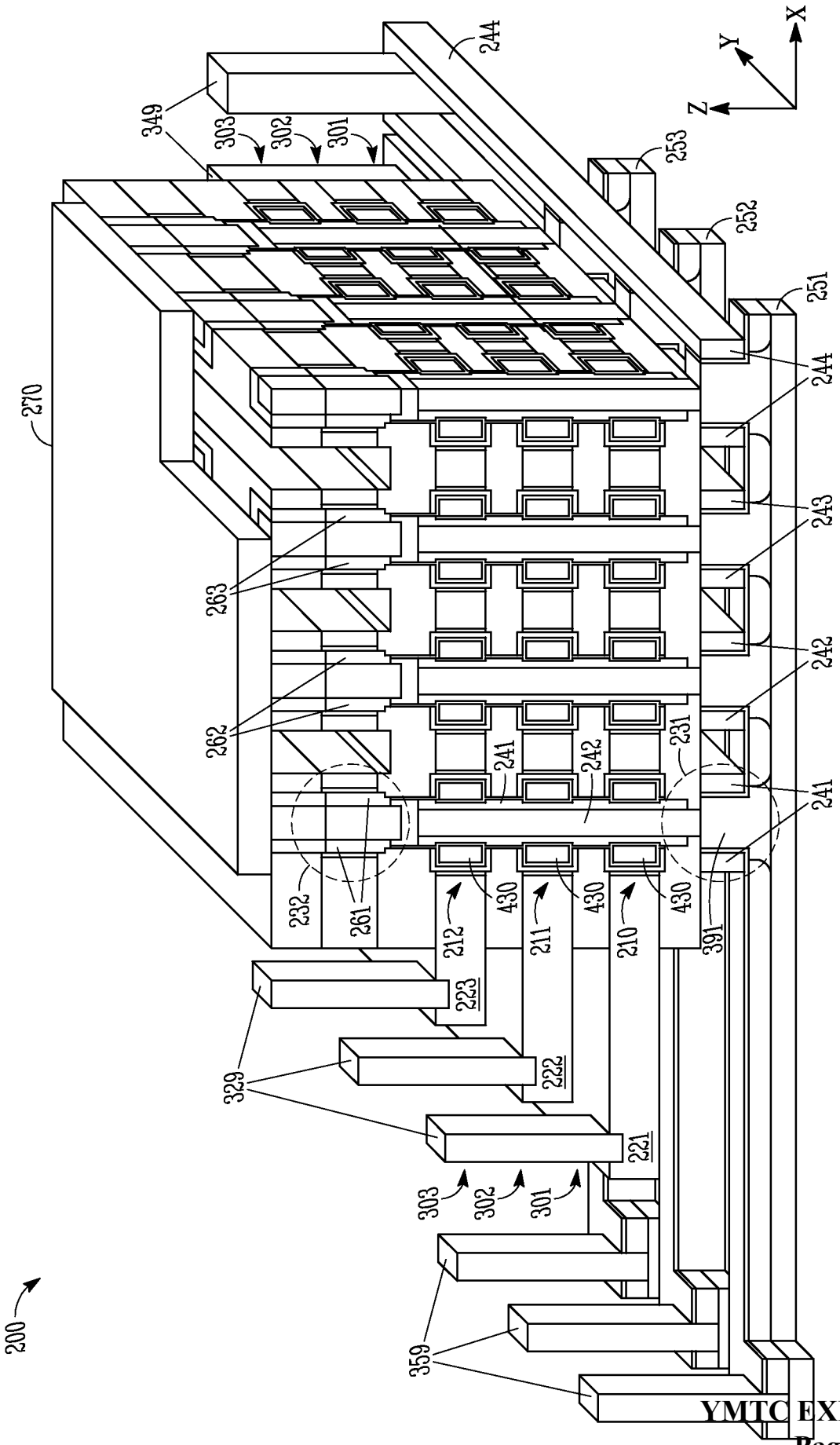

X
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244
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303
302
301
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329
359
200

FIG. 3

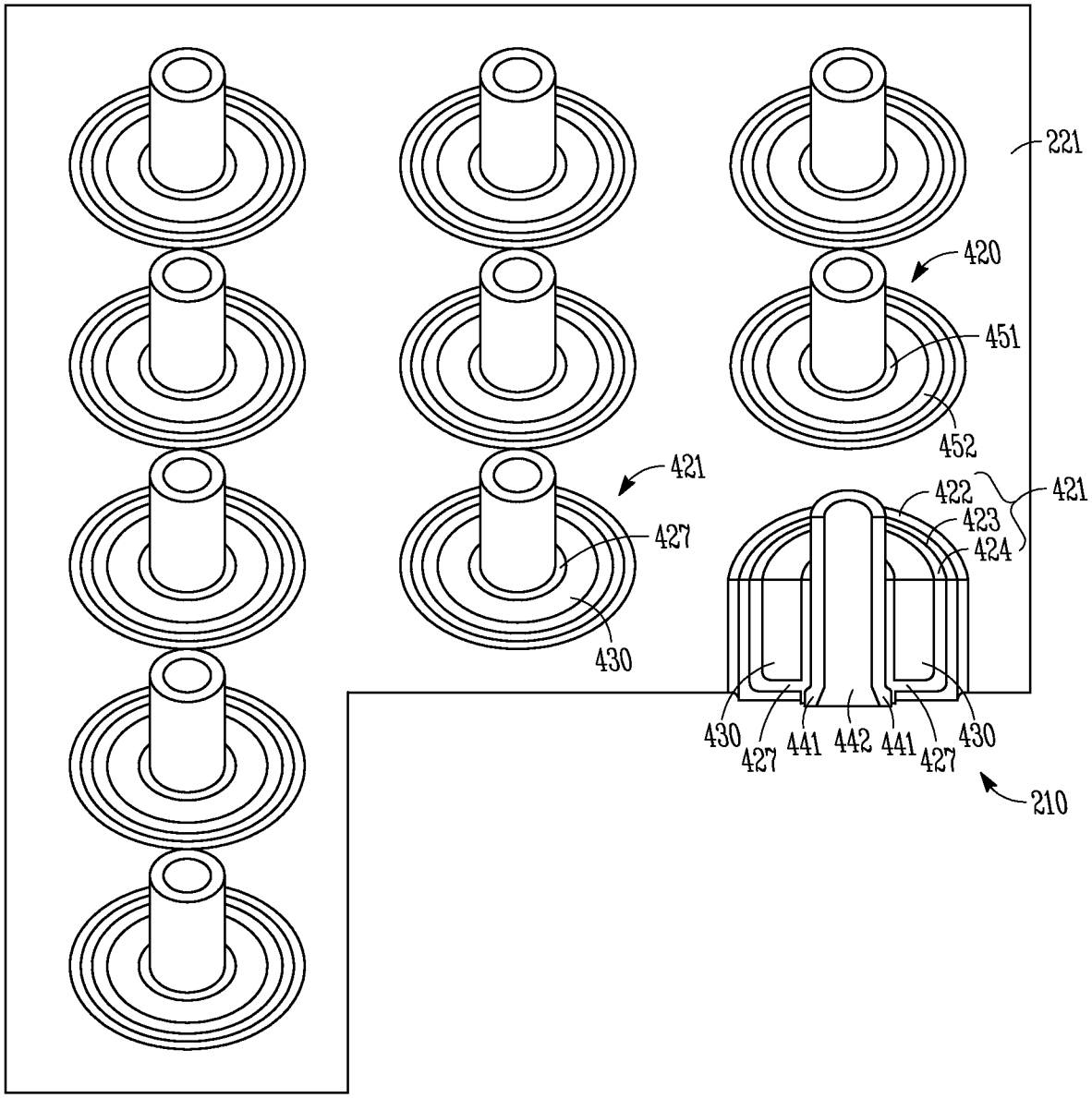

221
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210

FIG. 4

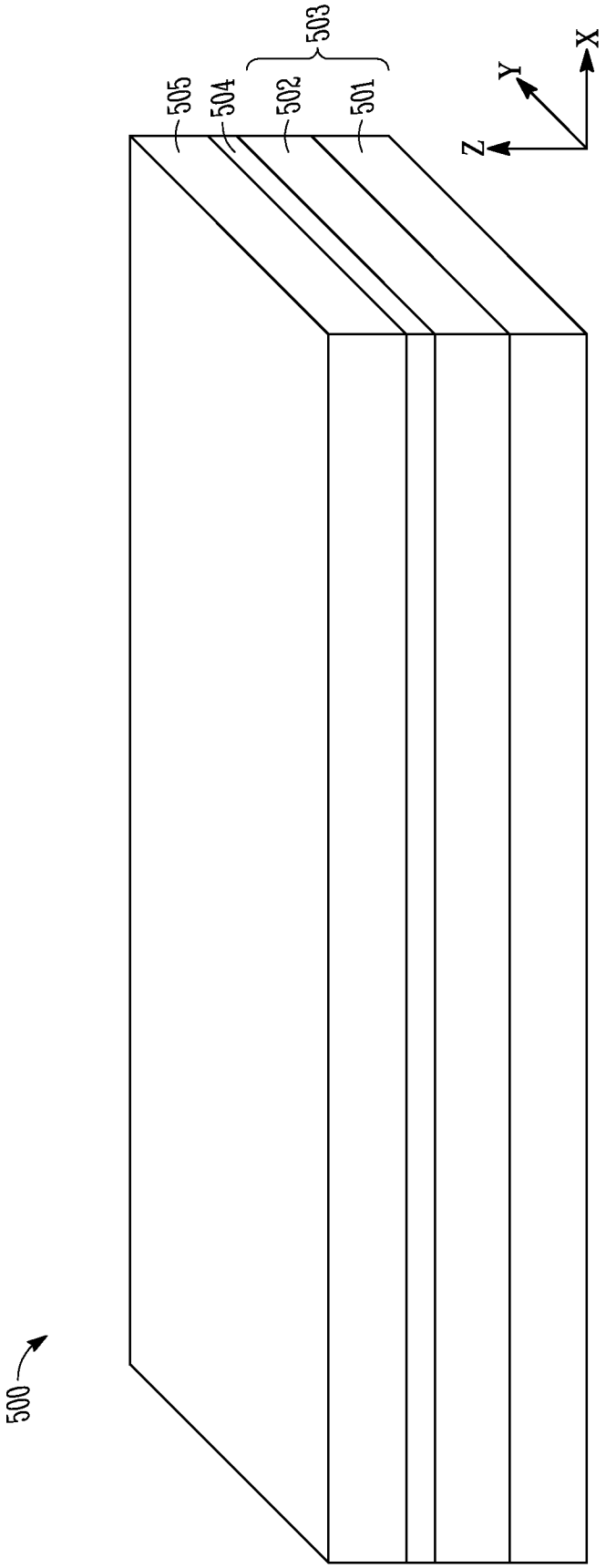


FIG. 5

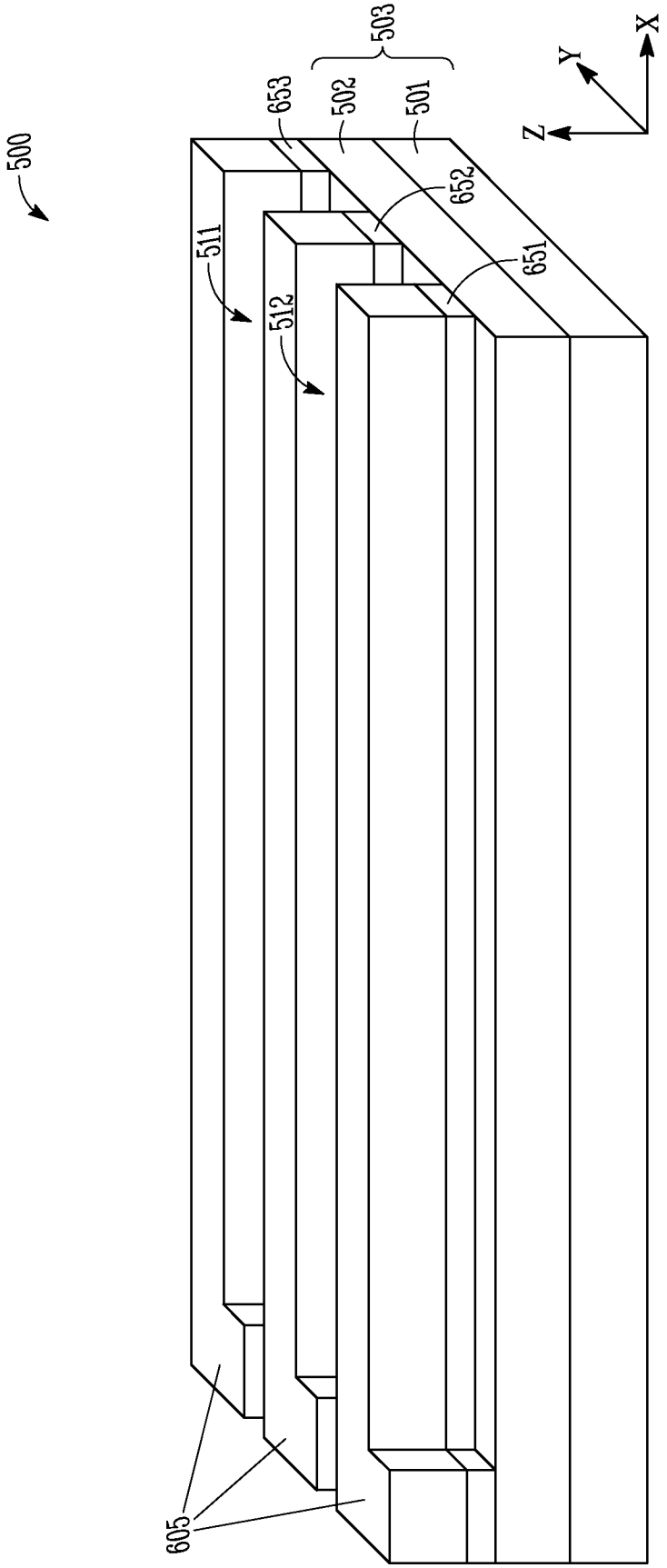


FIG. 6

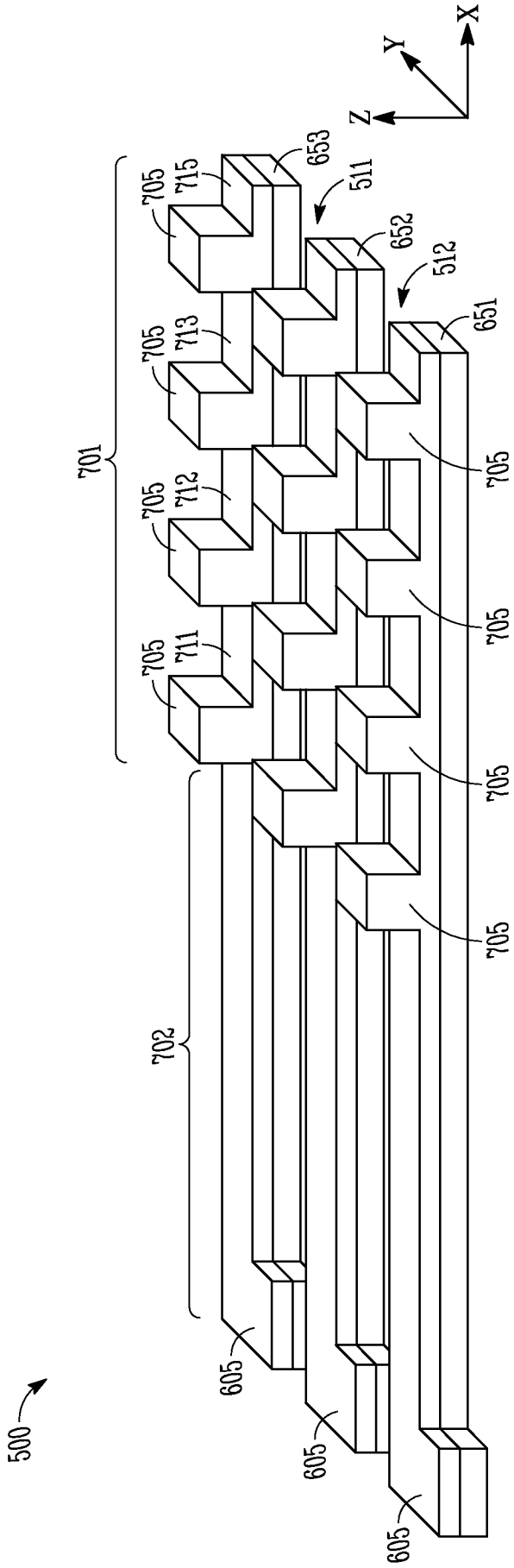


FIG. 7

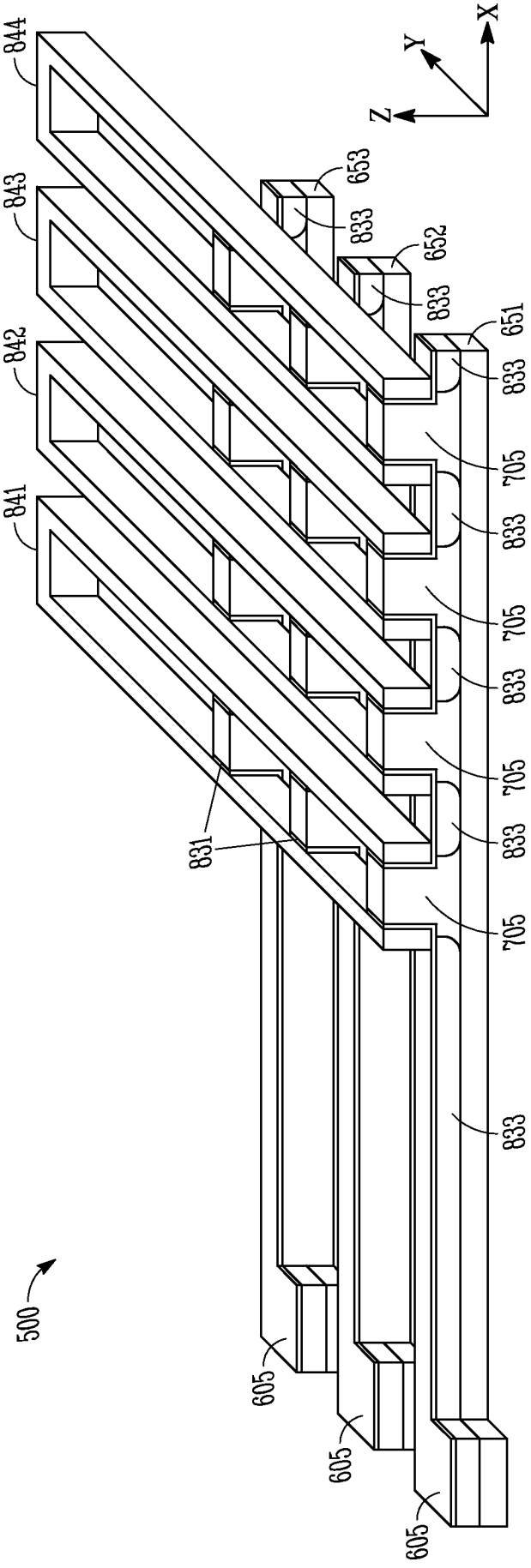


FIG. 8

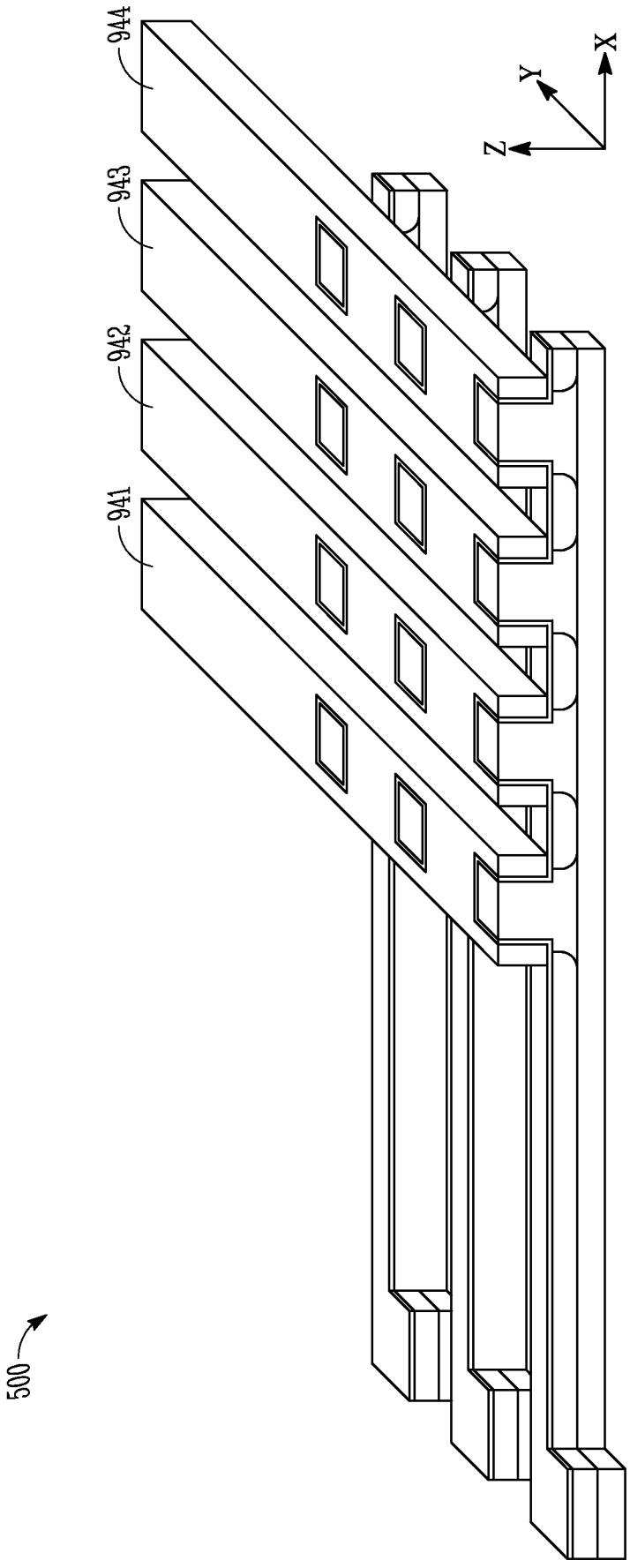


FIG. 9

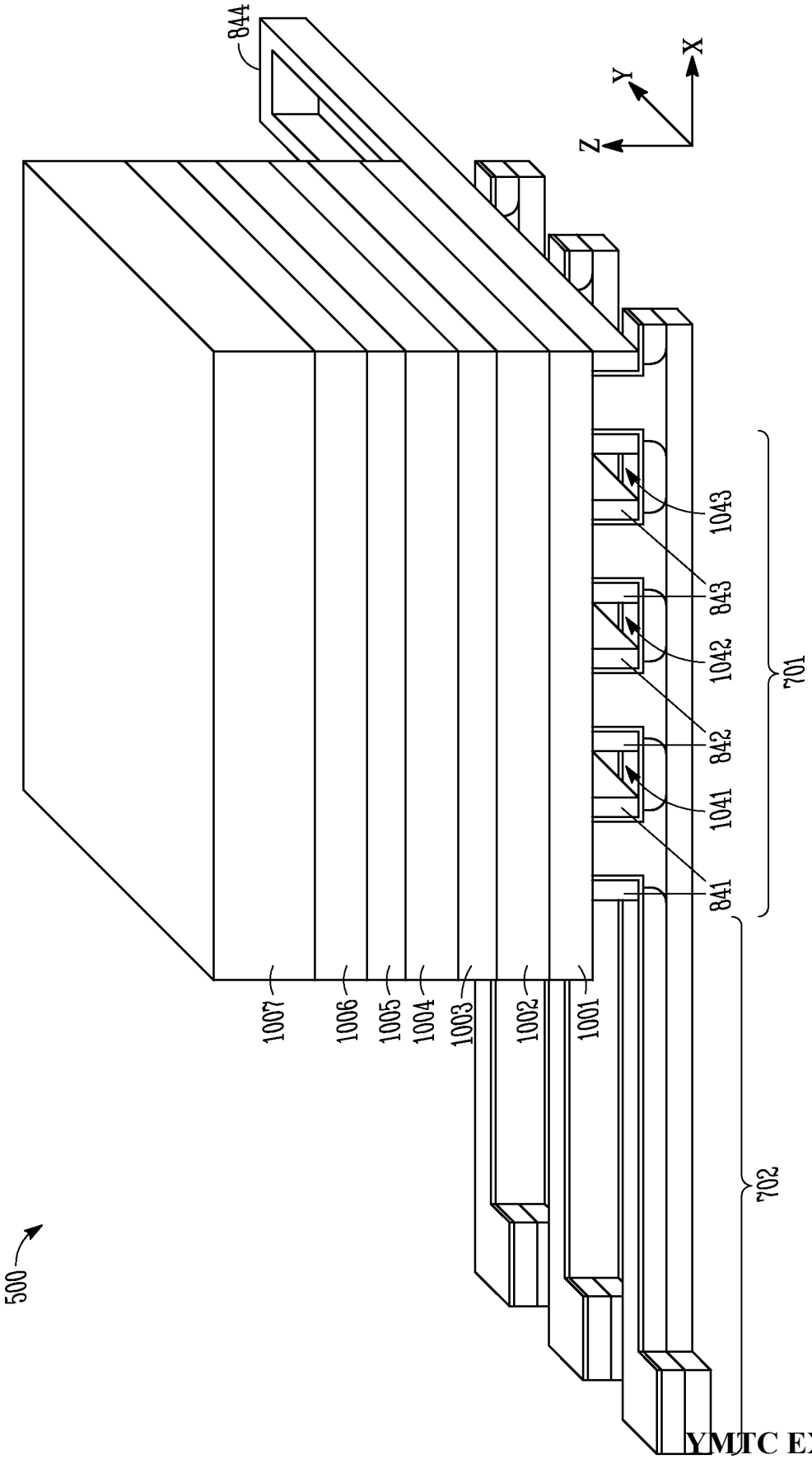

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Y
X
Z
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842
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701
1007
1006
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1004
1003
1002
1001
702
500

FIG. 10

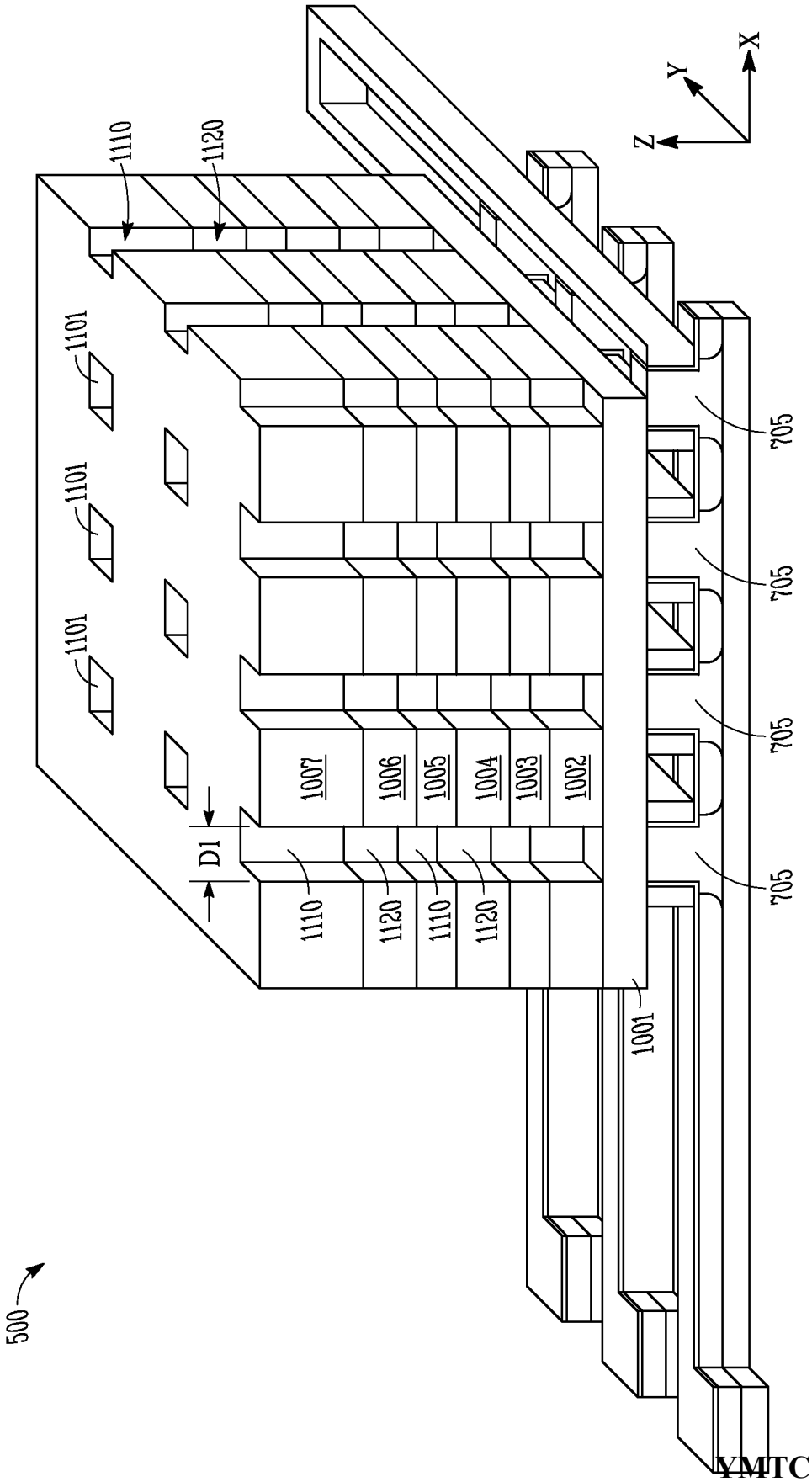

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Y
Z
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1101
1101
1101
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1007
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1003
1002
D1
1110
1120
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1120
1001
500

FIG. 11

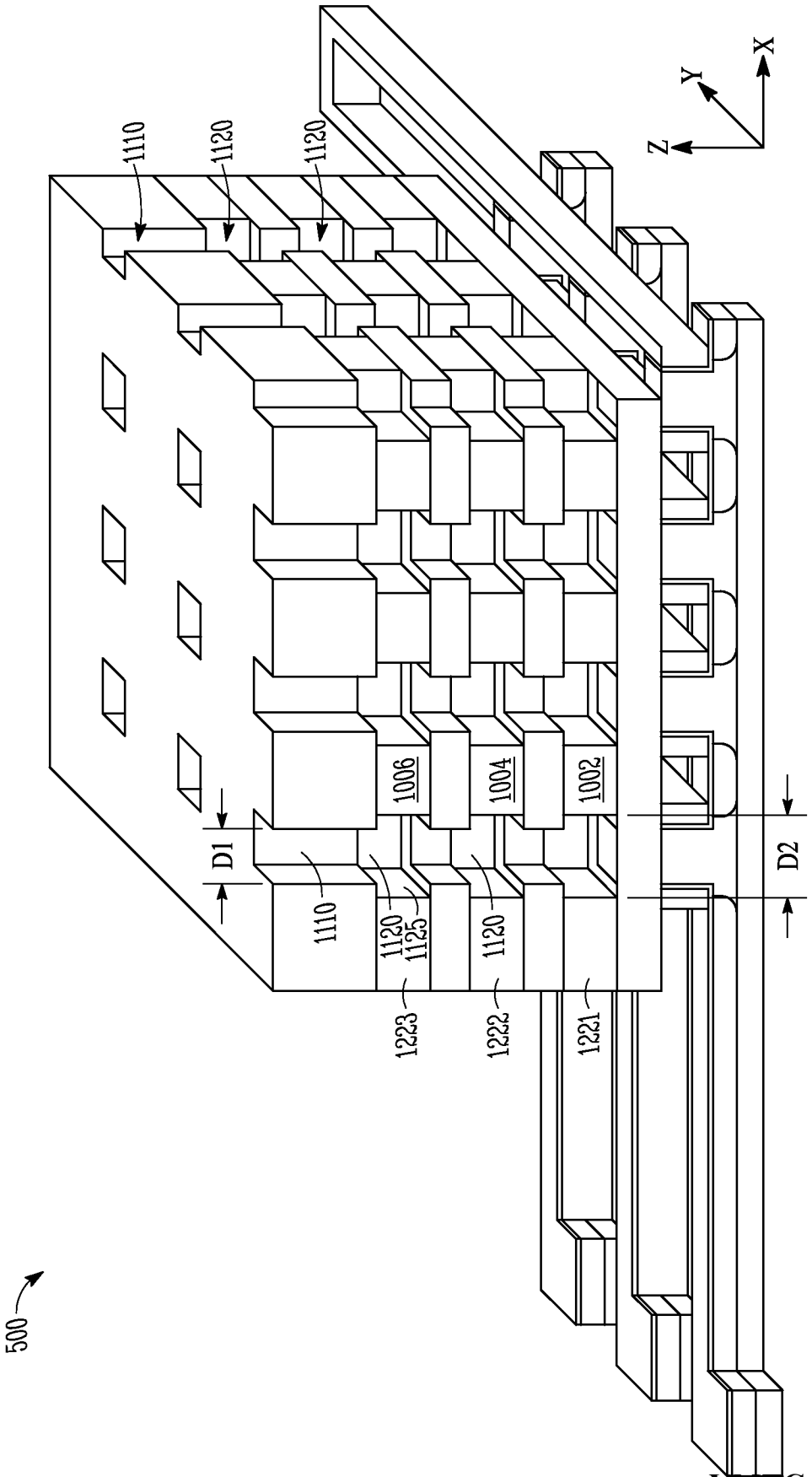

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1222
1221
500

FIG. 12

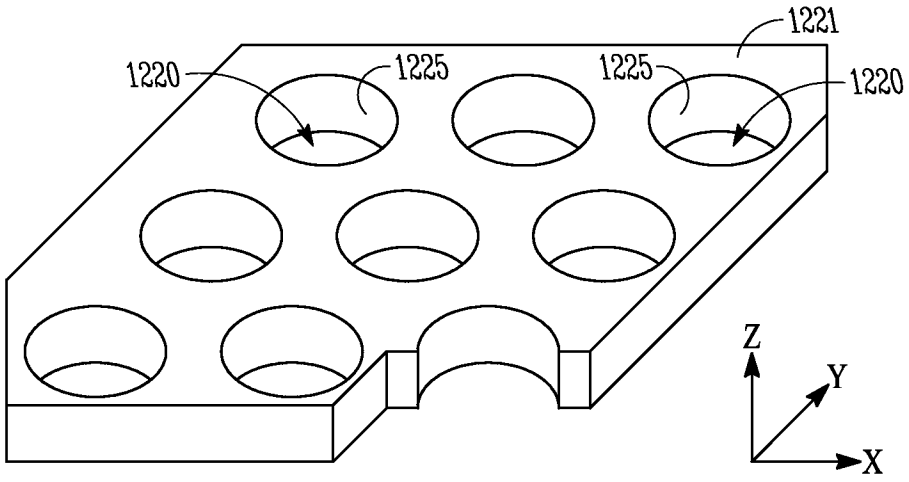


FIG. 13

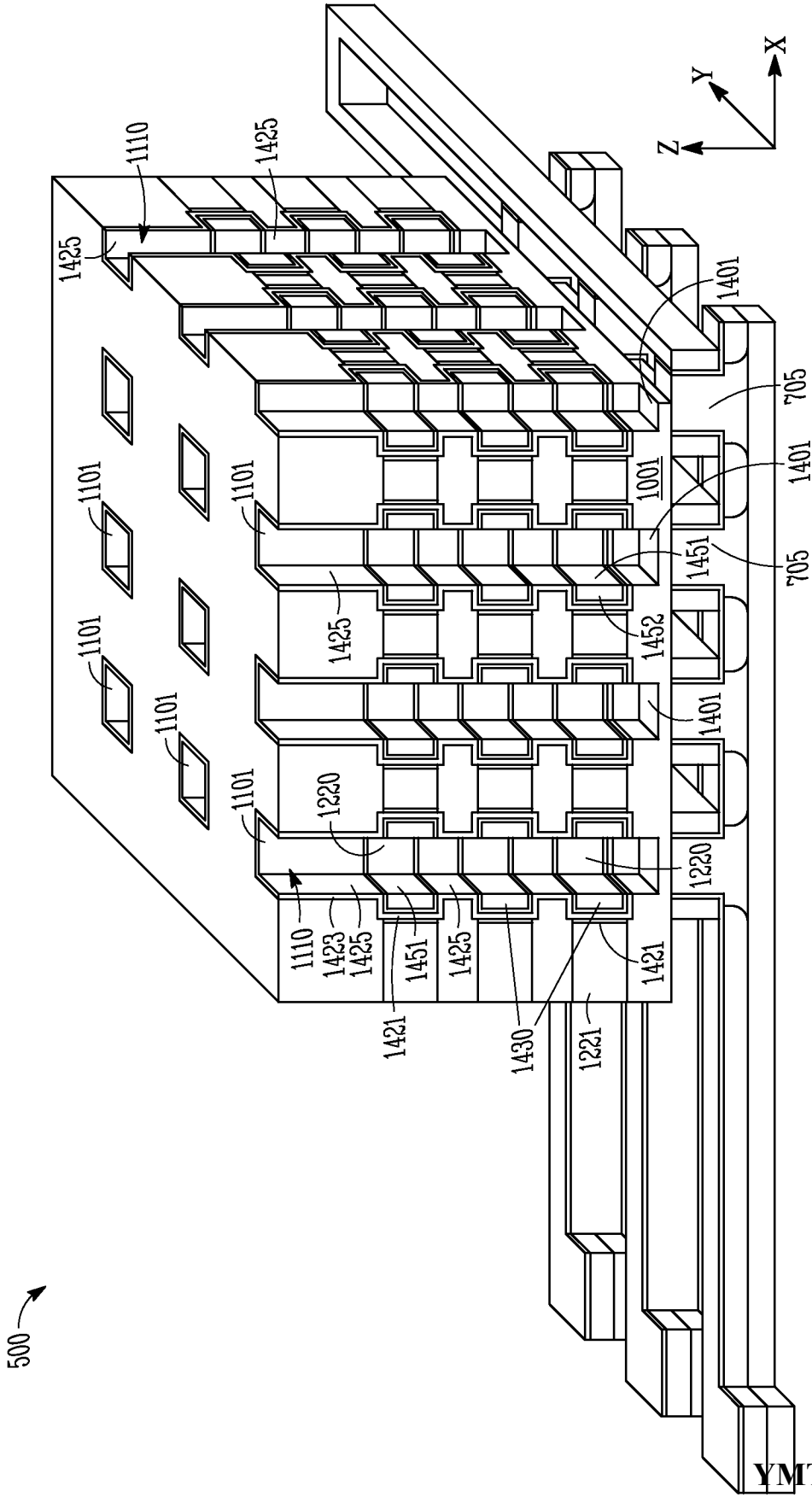

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FIG. 14

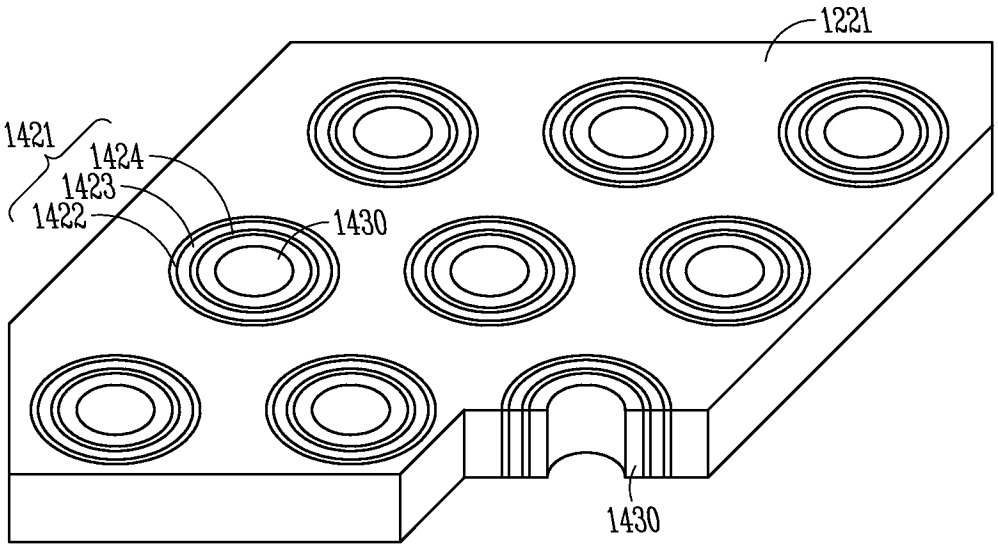


FIG. 15

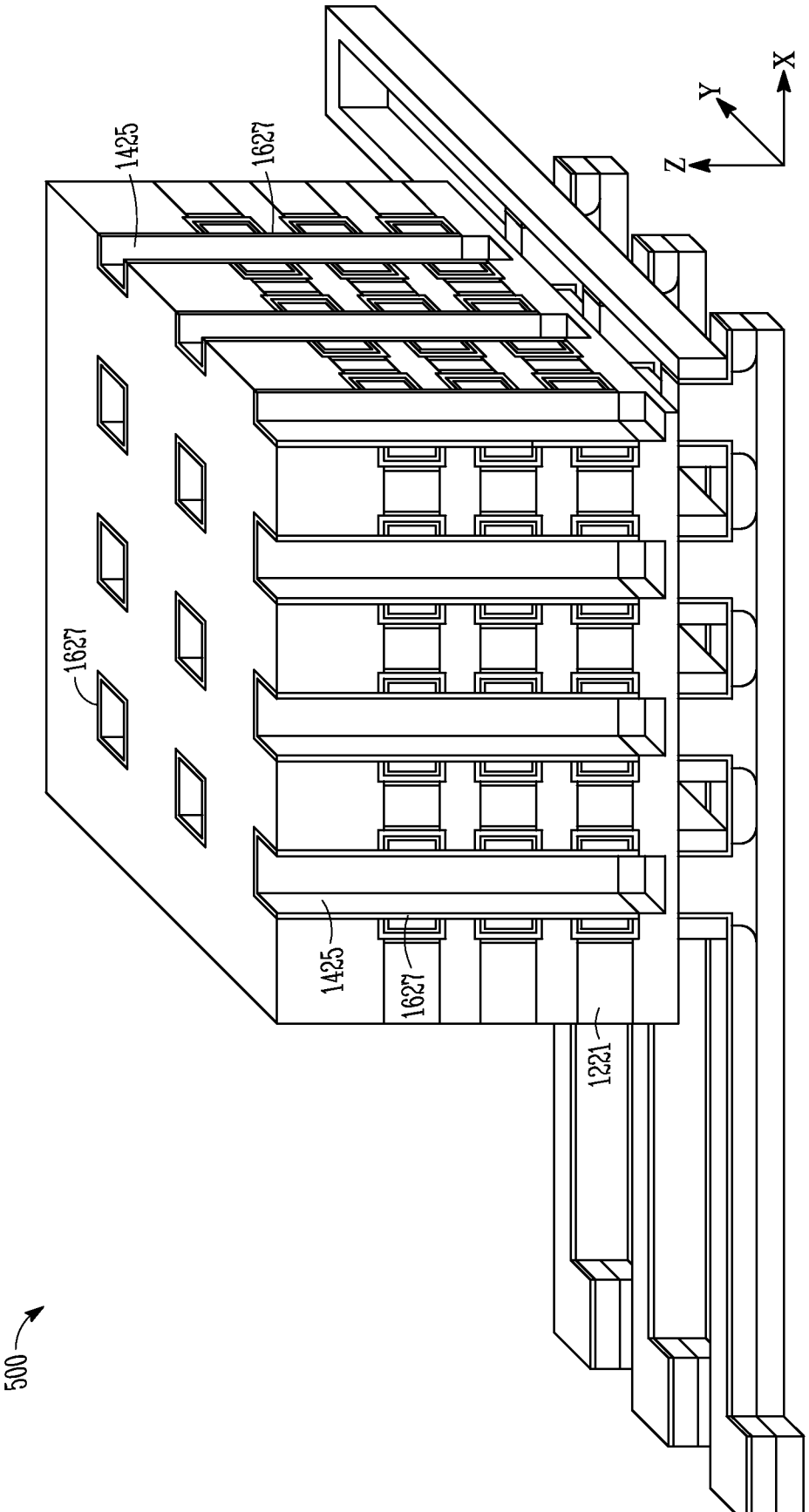


FIG. 16

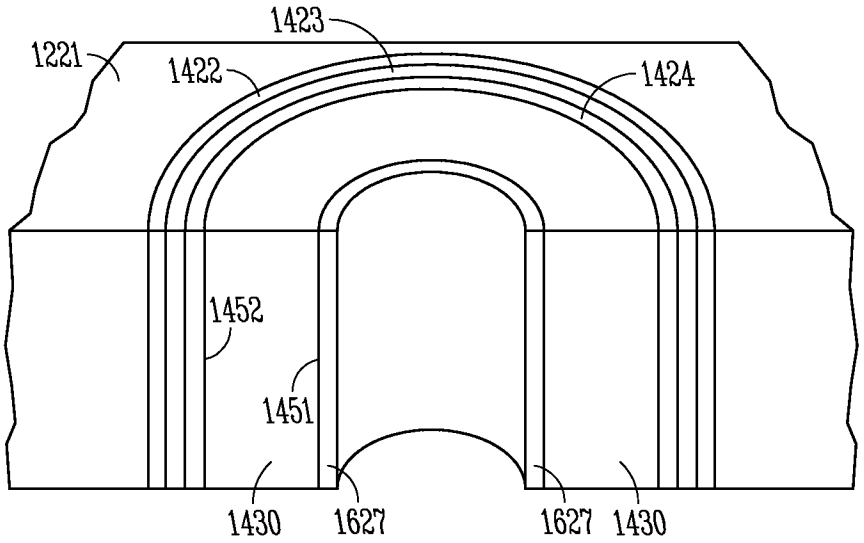


FIG. 17

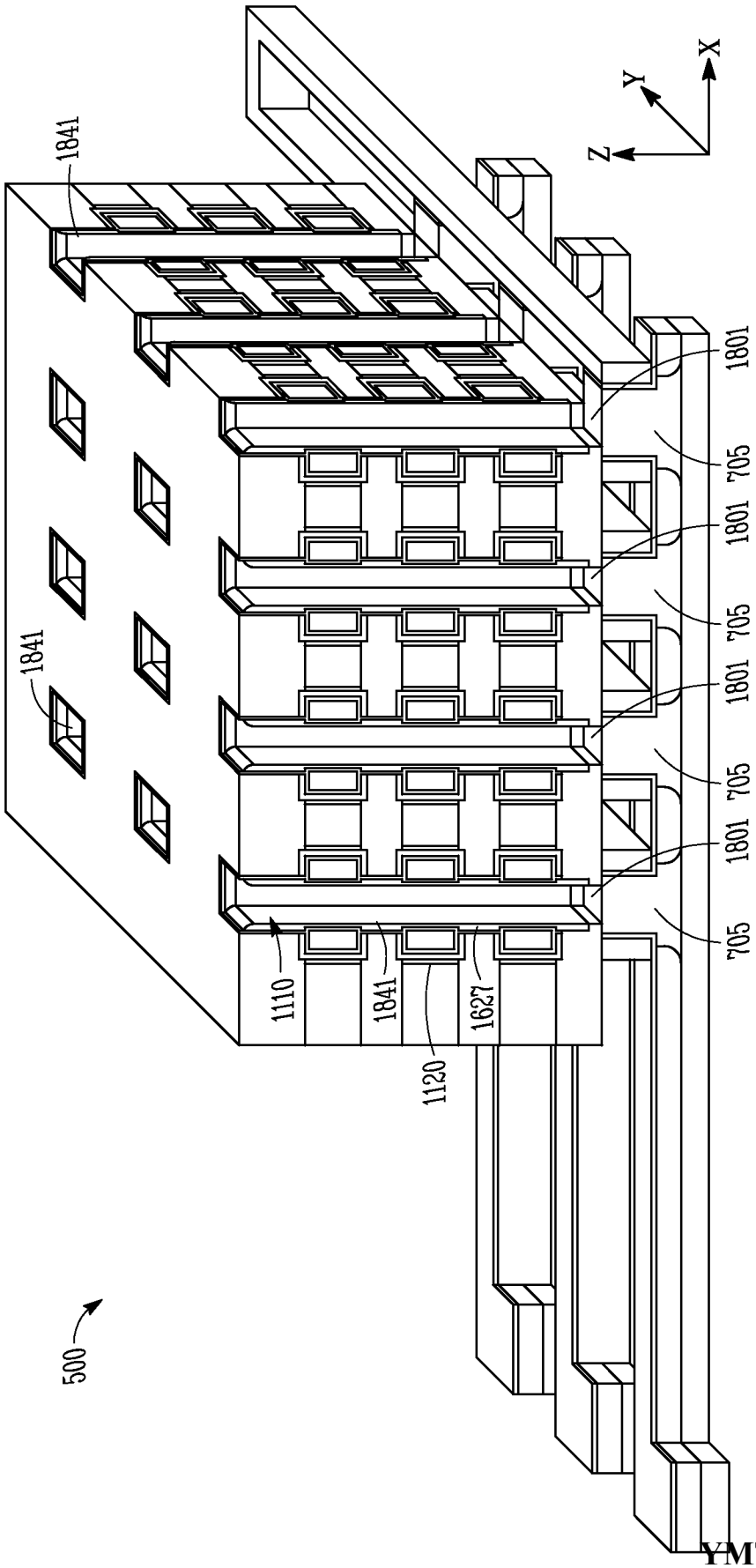

Y
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1120
500

FIG. 18

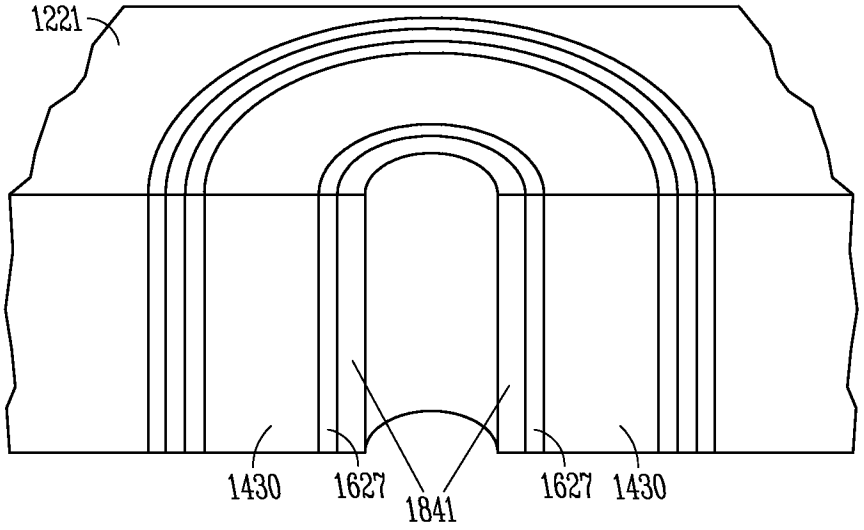


FIG. 19

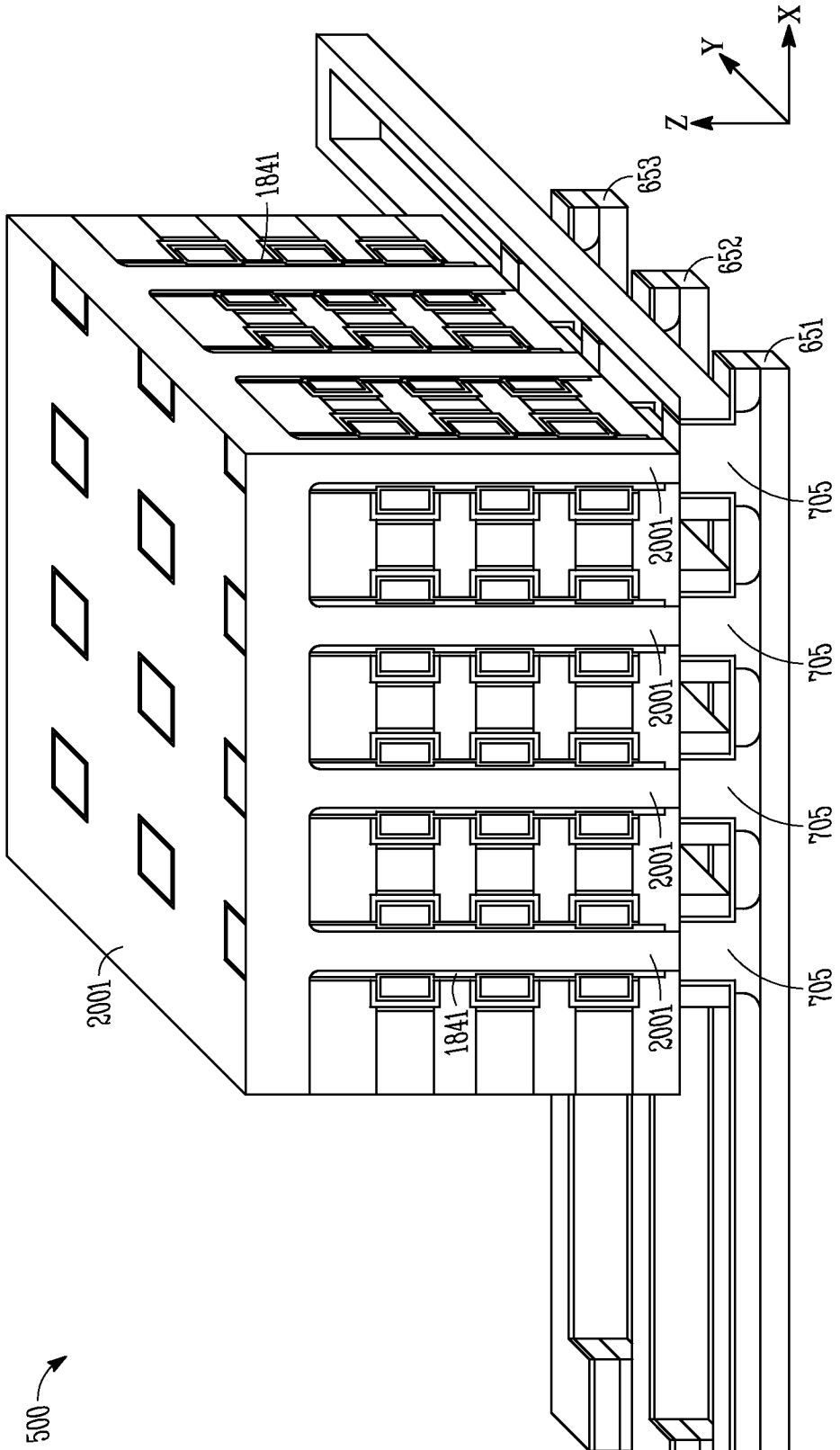


FIG. 20

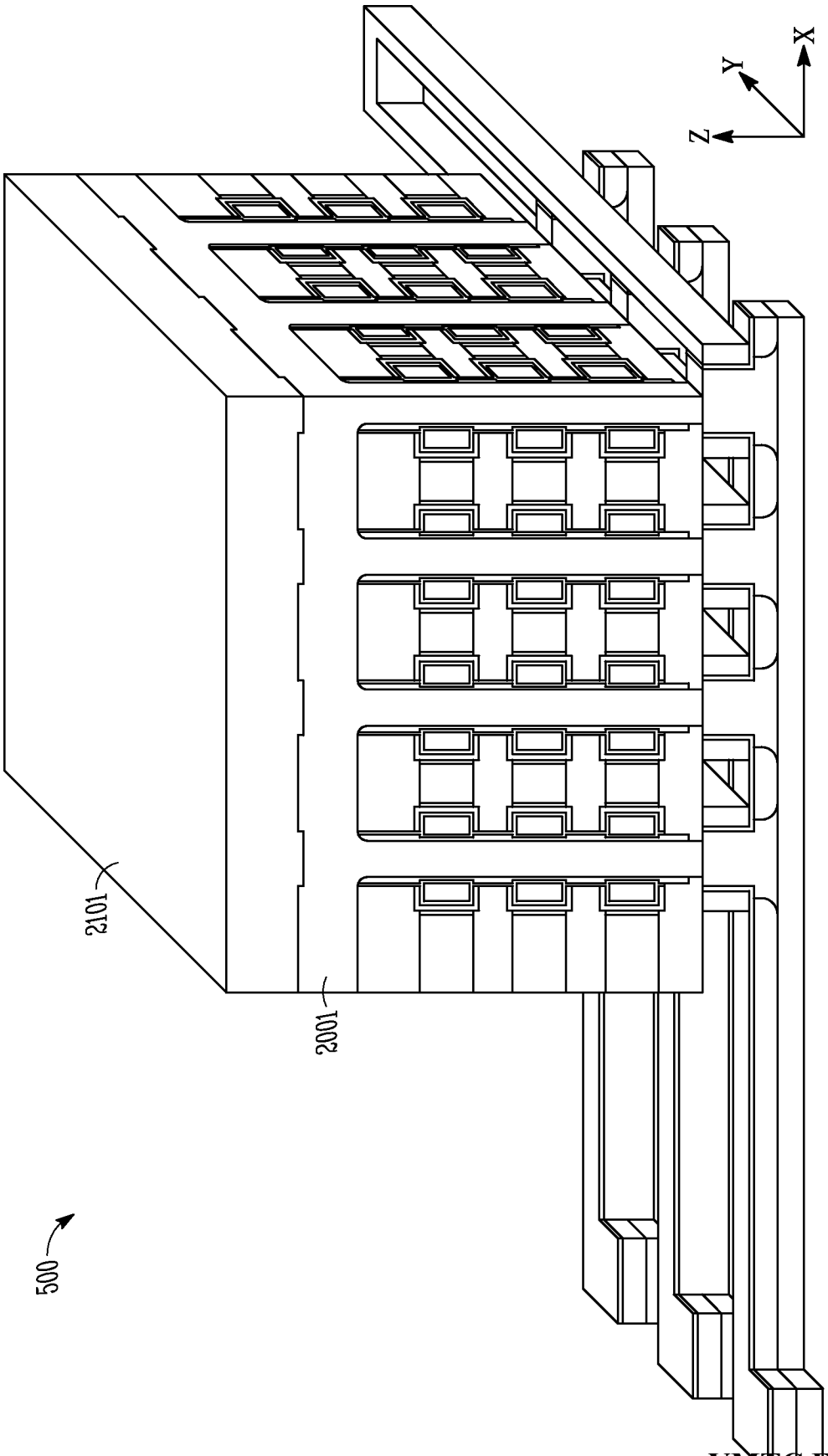


FIG. 21

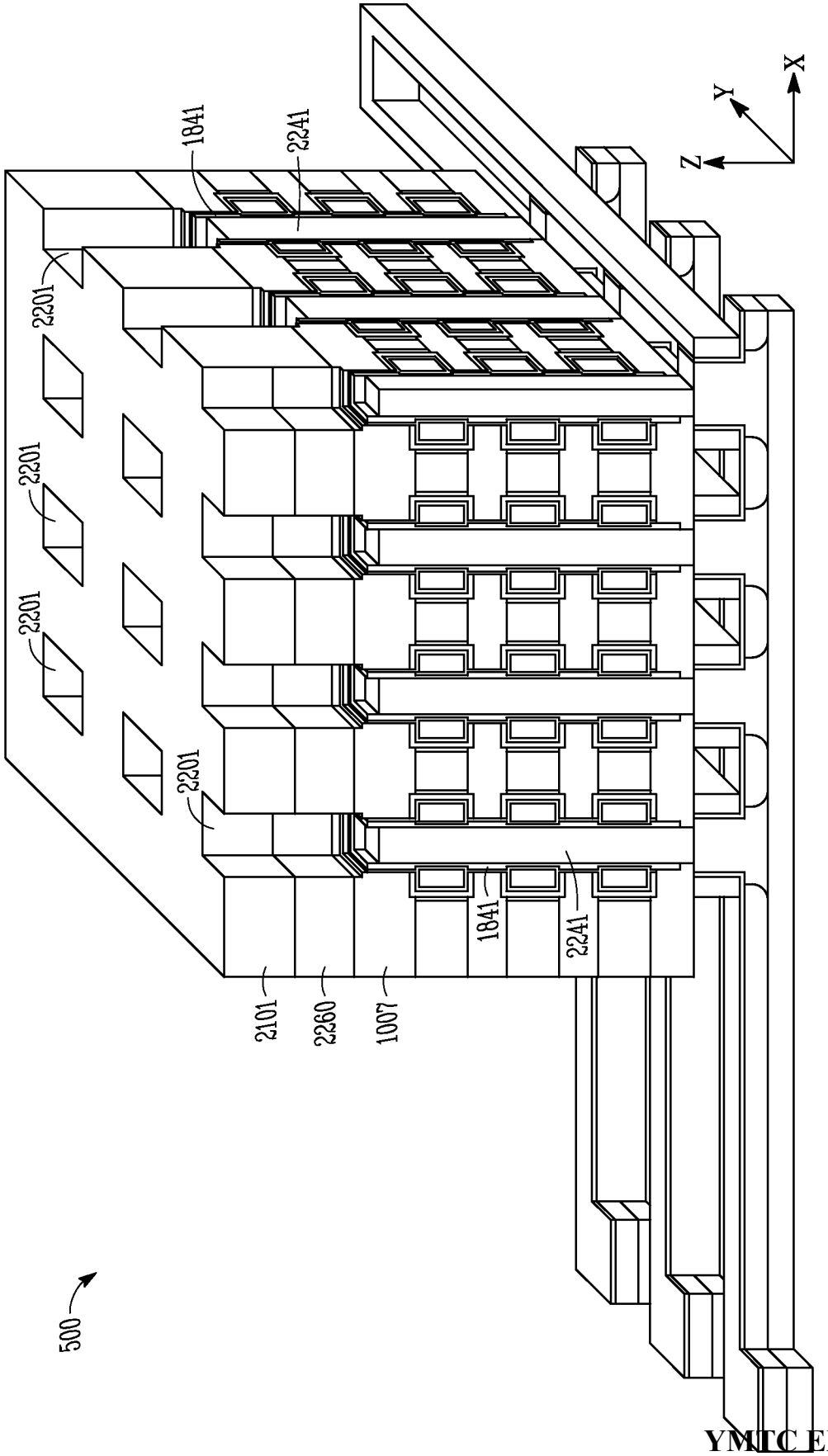

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1841
2241
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2360
1007
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X
Y
Z

FIG. 22

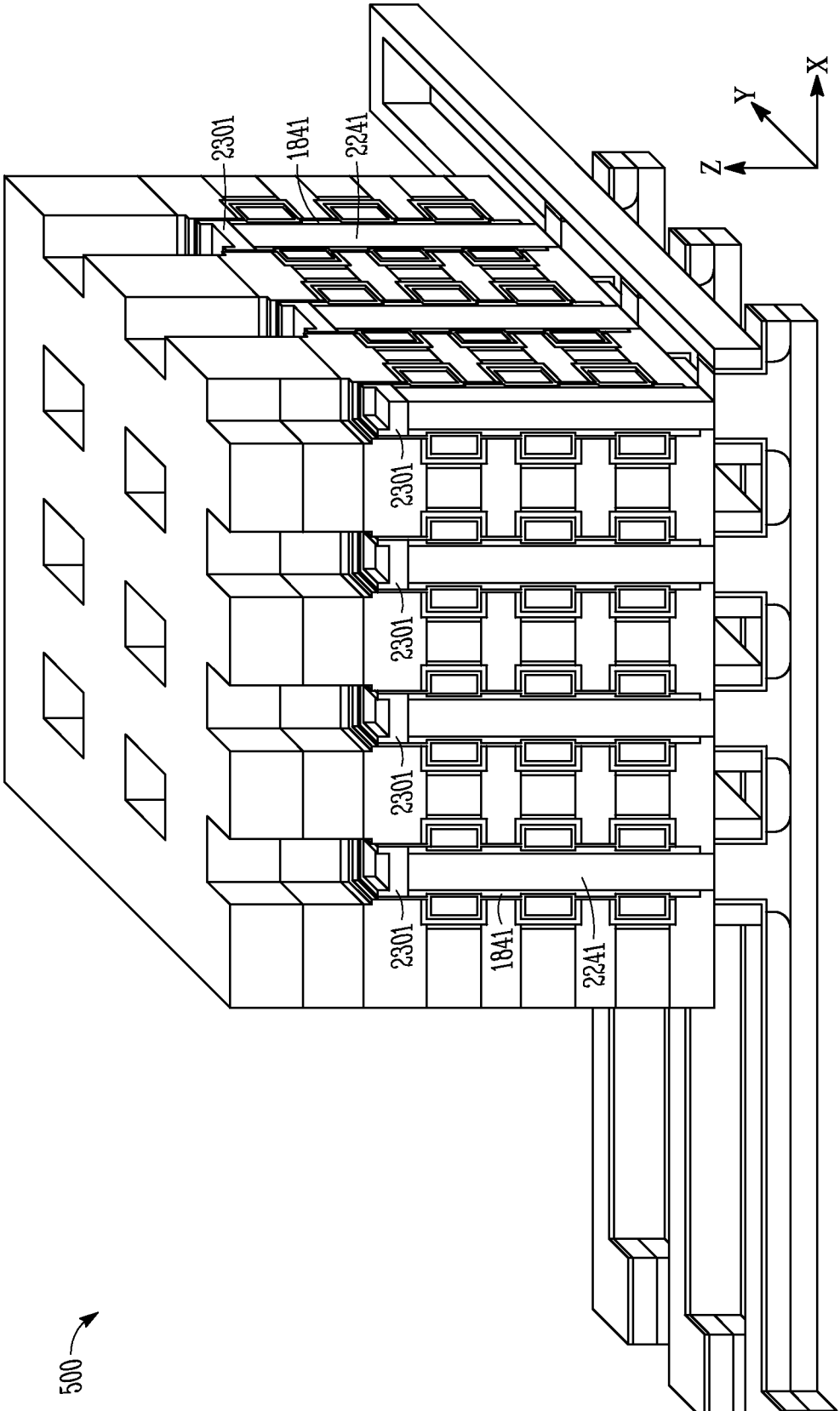


FIG. 23

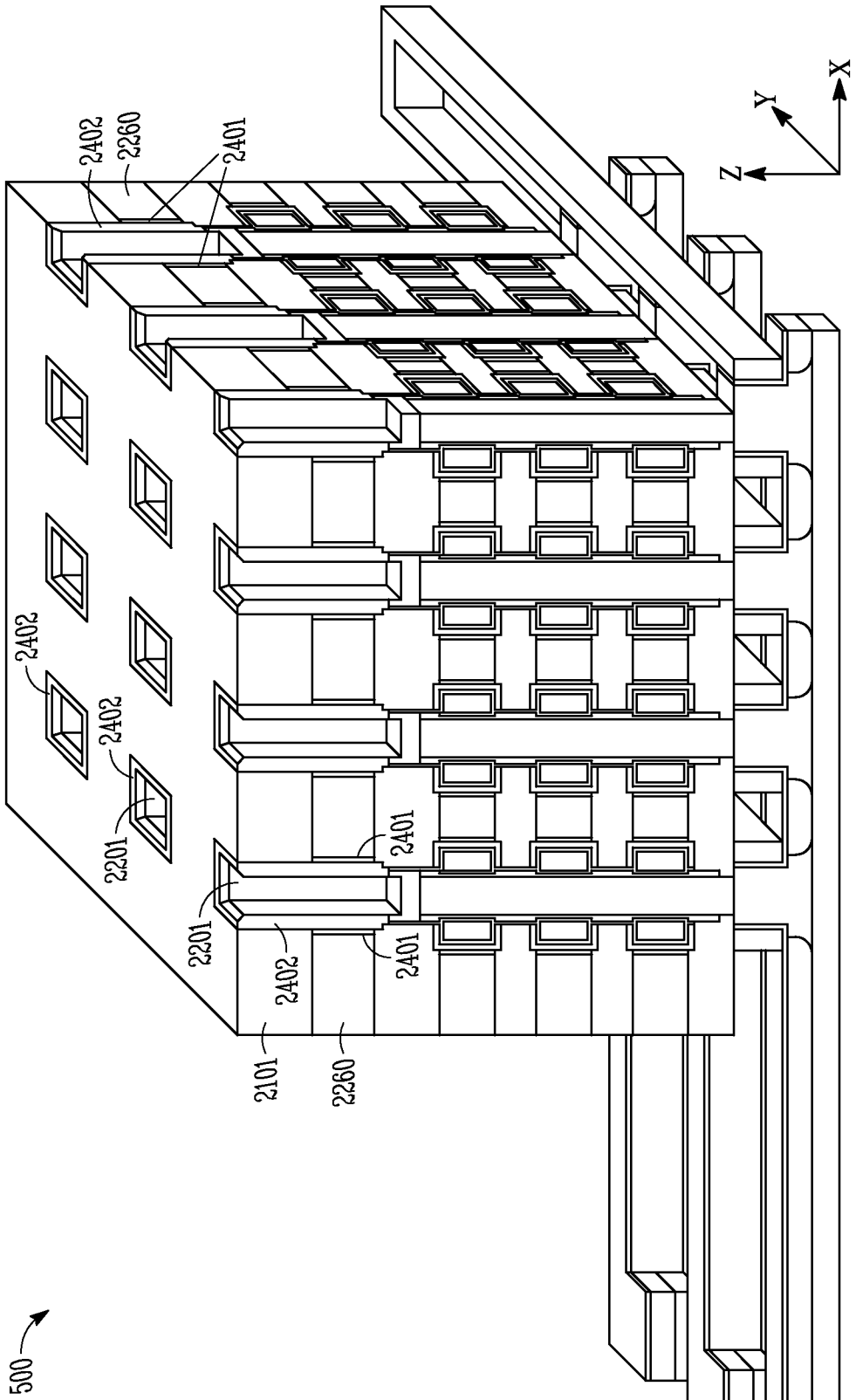

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Y
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2402
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2201
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2201
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2401
2101
2260
500

FIG. 24

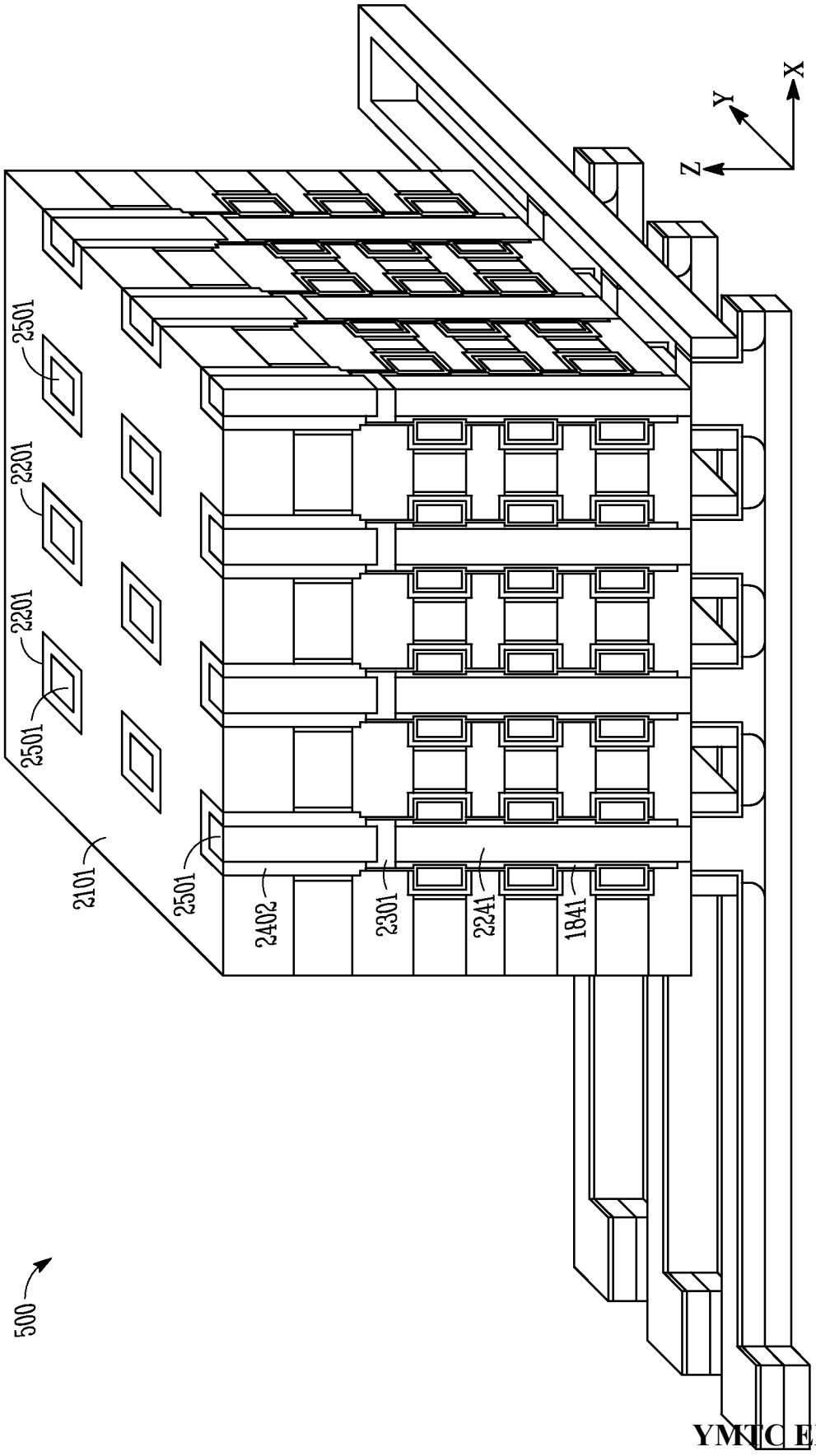


FIG. 25

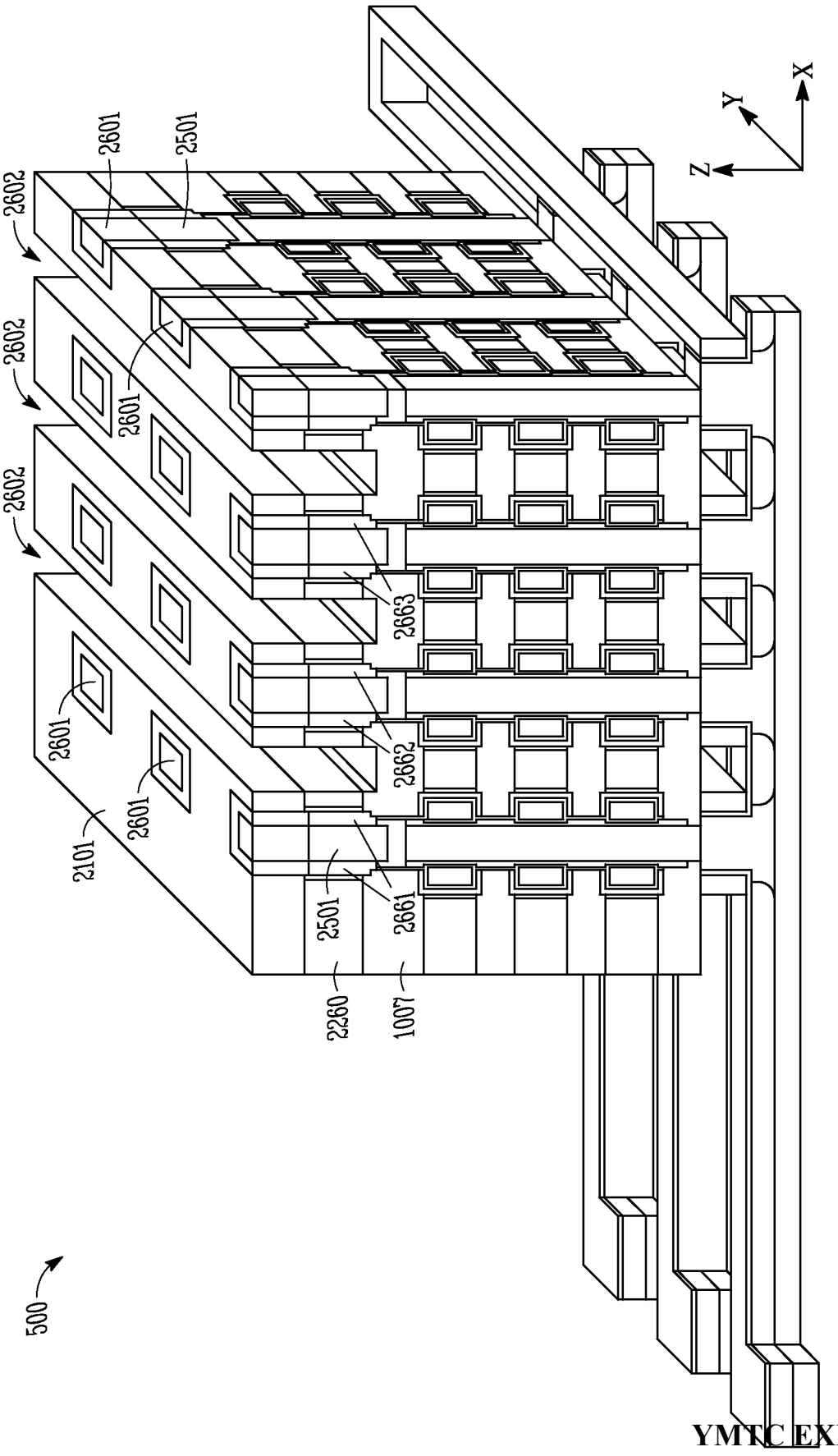

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Y
Z
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2501
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1007
500

FIG. 26

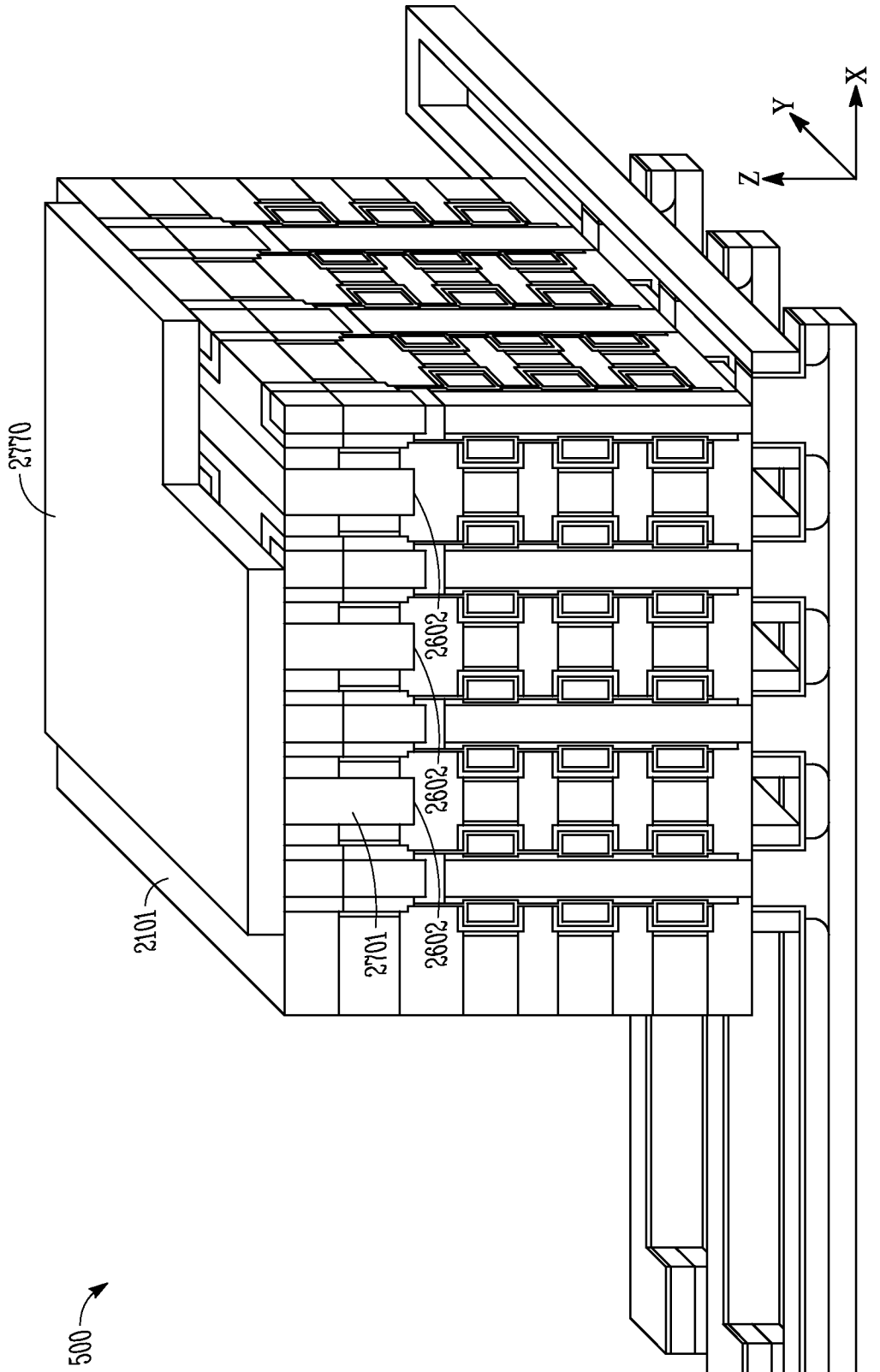


FIG. 27

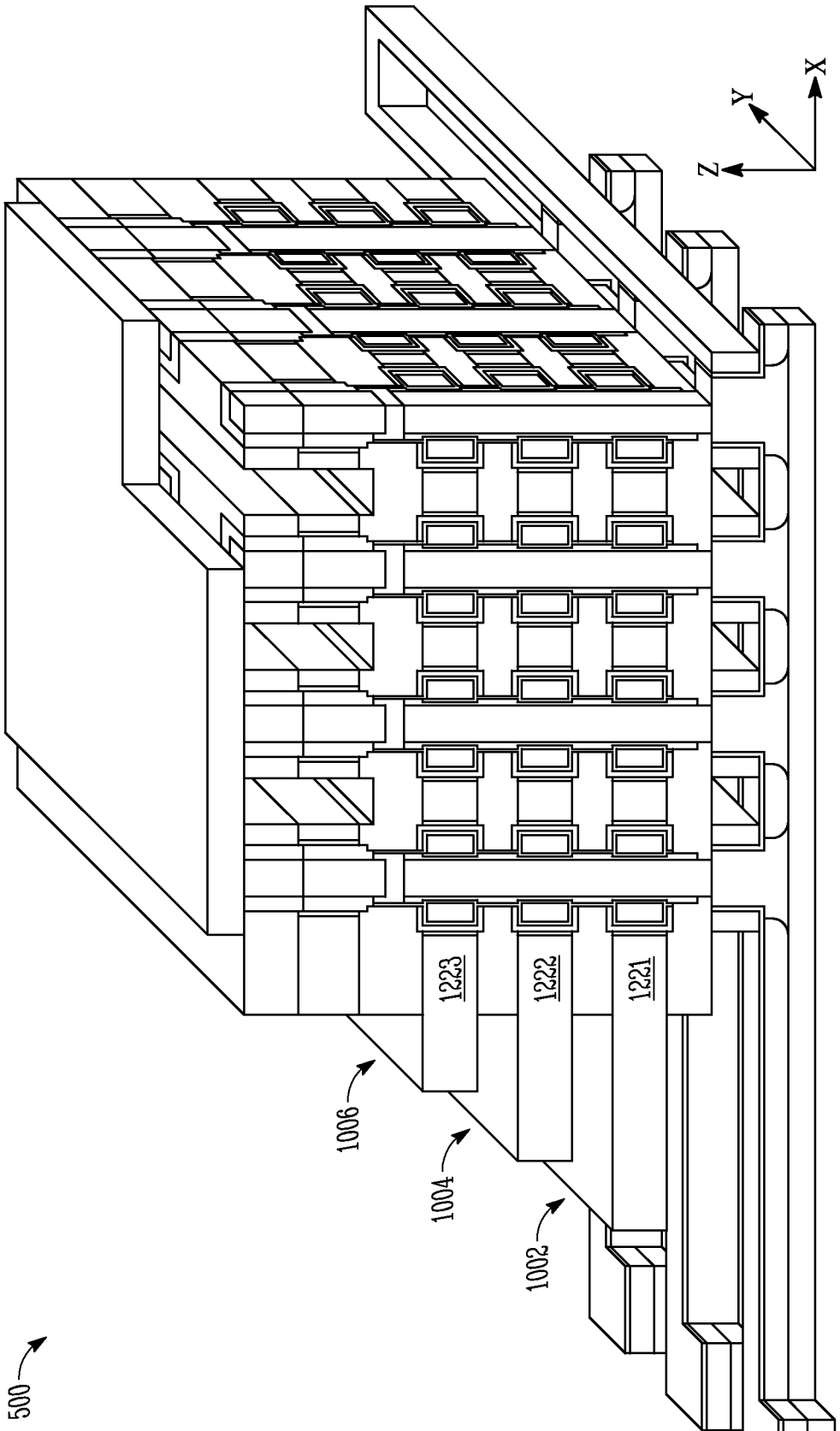


FIG. 28

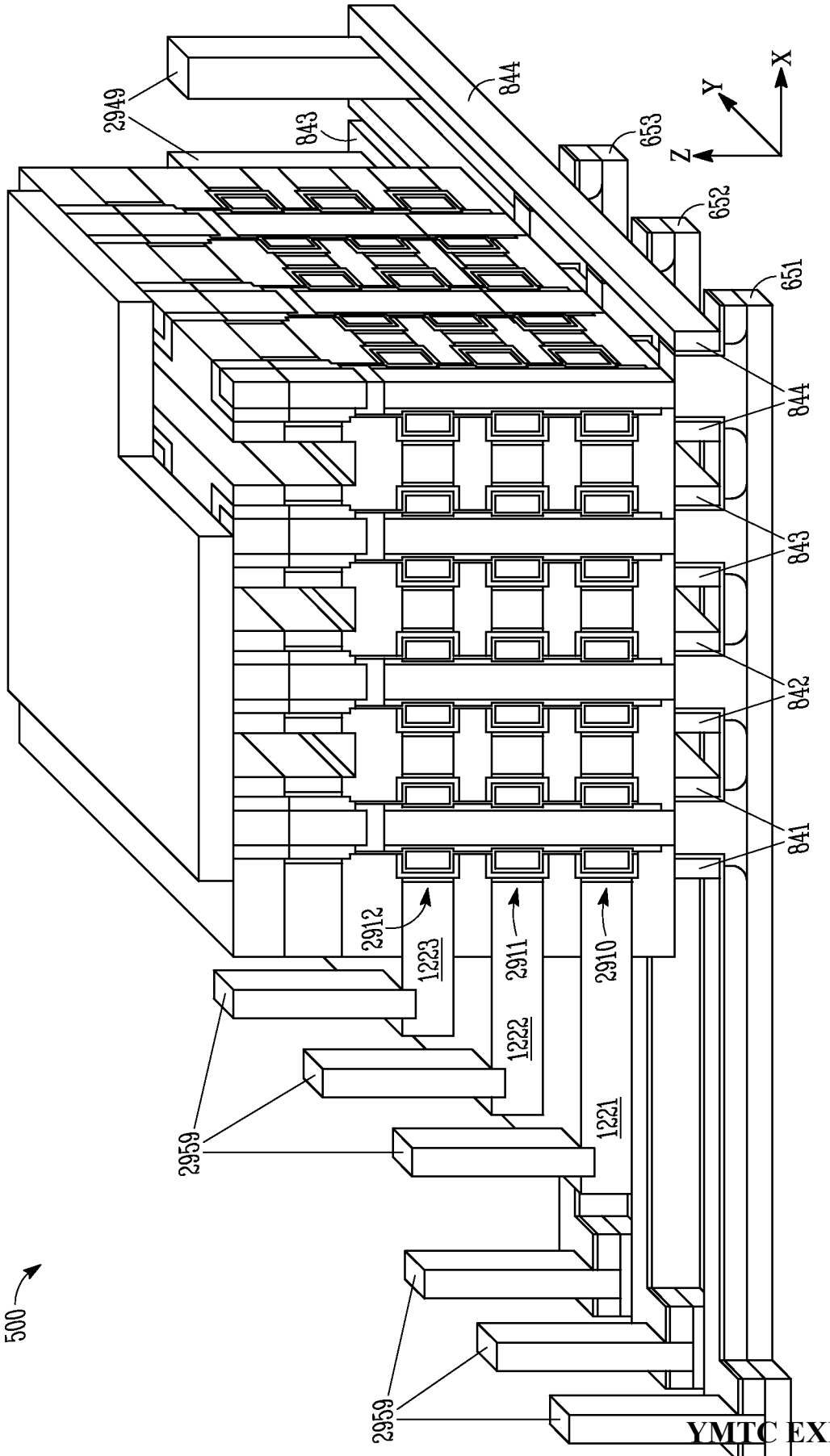

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653
652
651
Y
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841
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2910
1223
1222
1221
2959
2959
500

FIG. 29

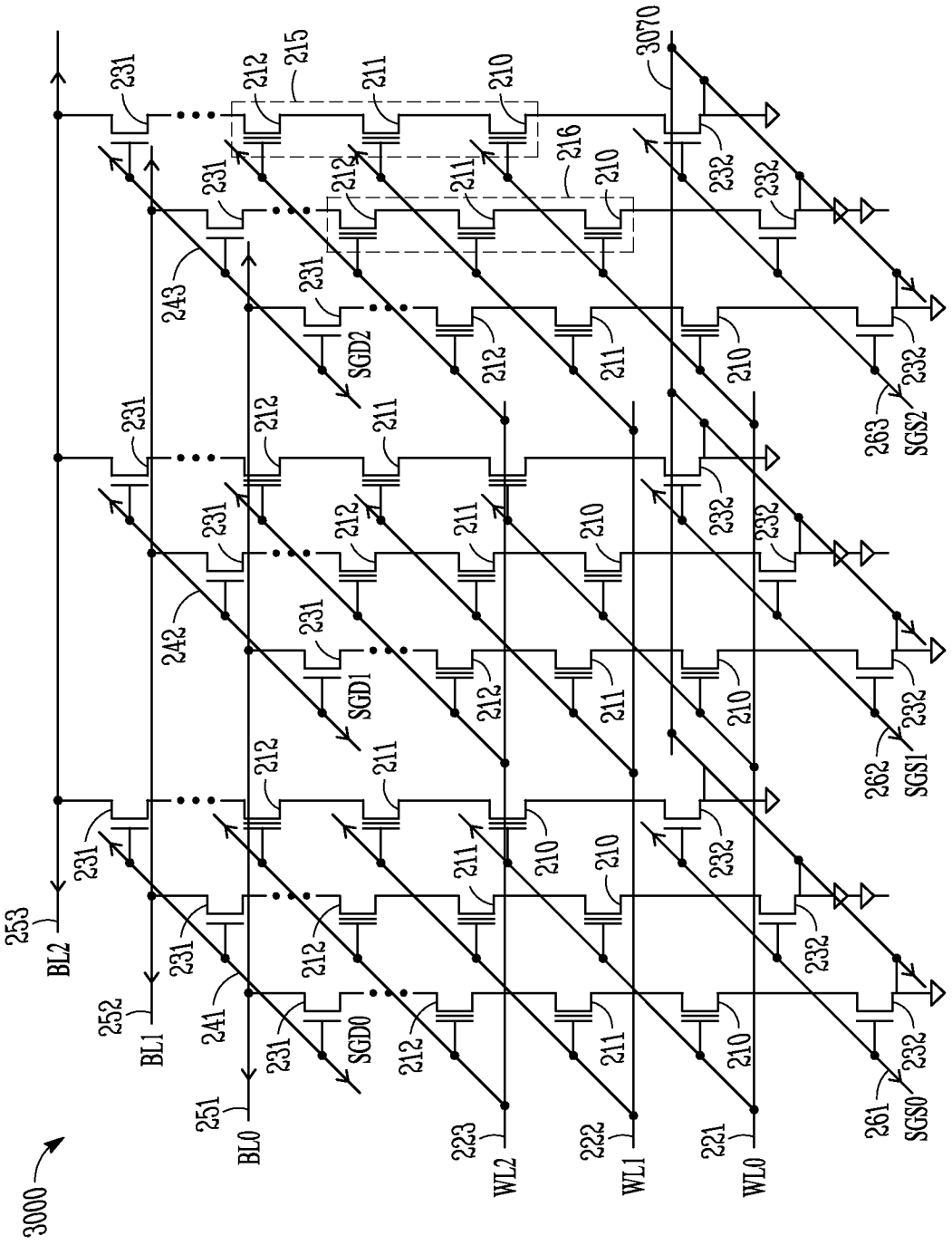

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243
242
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SGD2
SGD1
SGD0
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SGS2
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SGS0
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BL1
251
BL0
223
WL2
222
WL1
221
WL0

FIG. 30

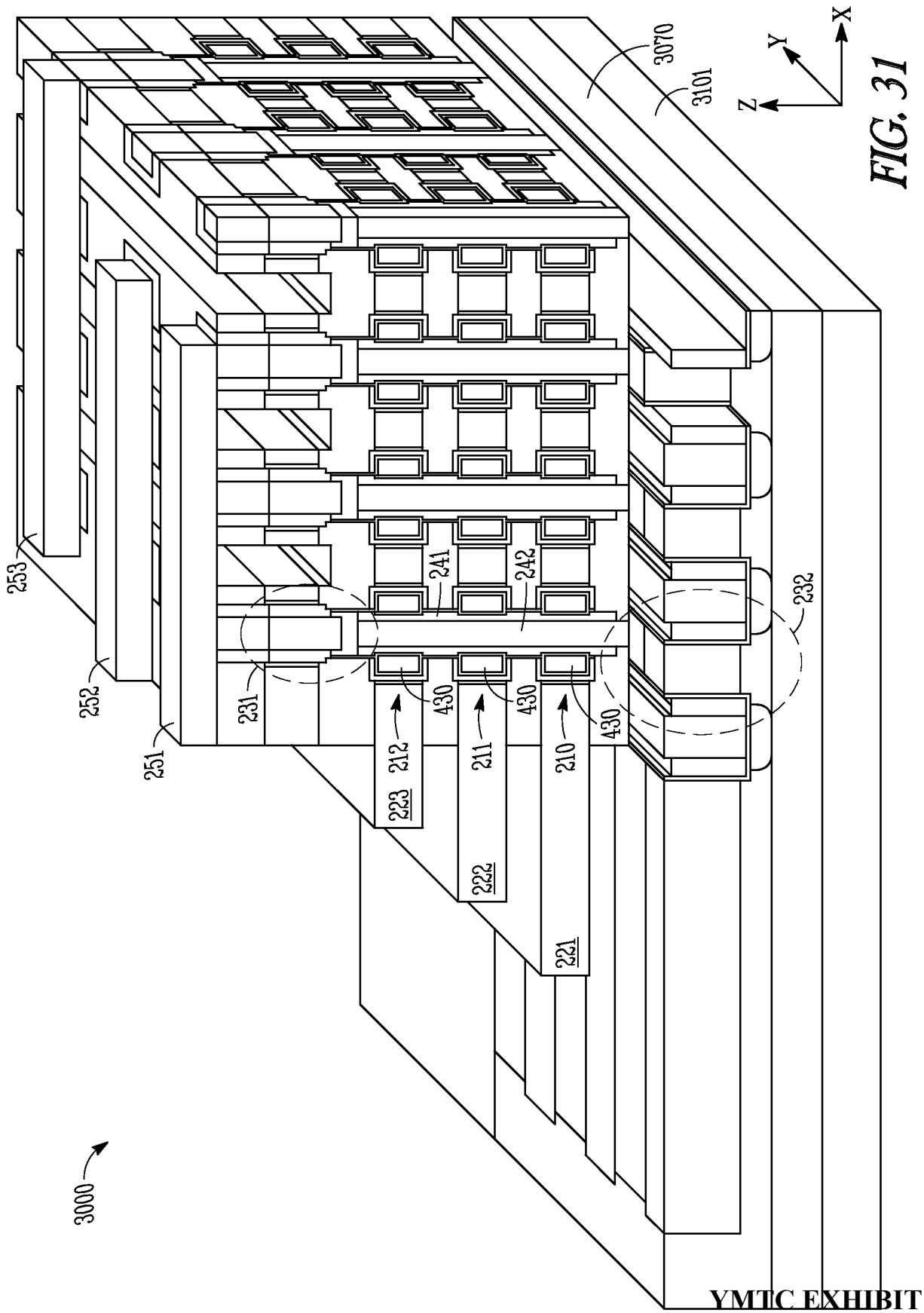

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FIG. 31

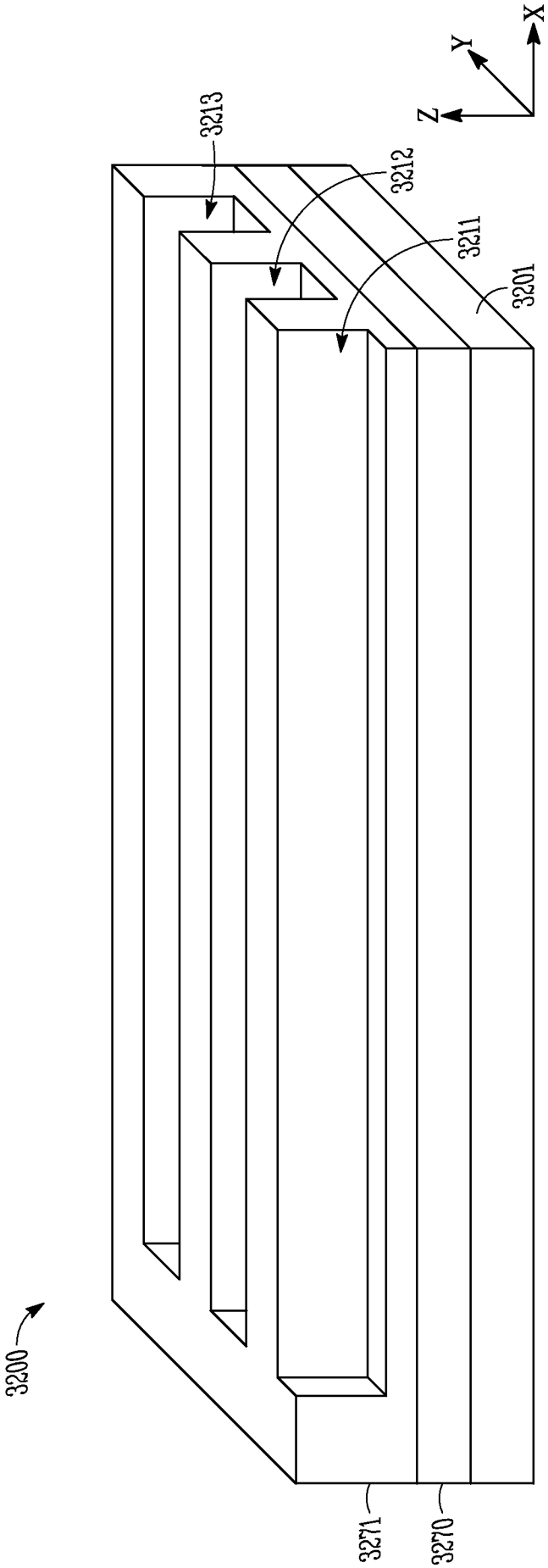


FIG. 32

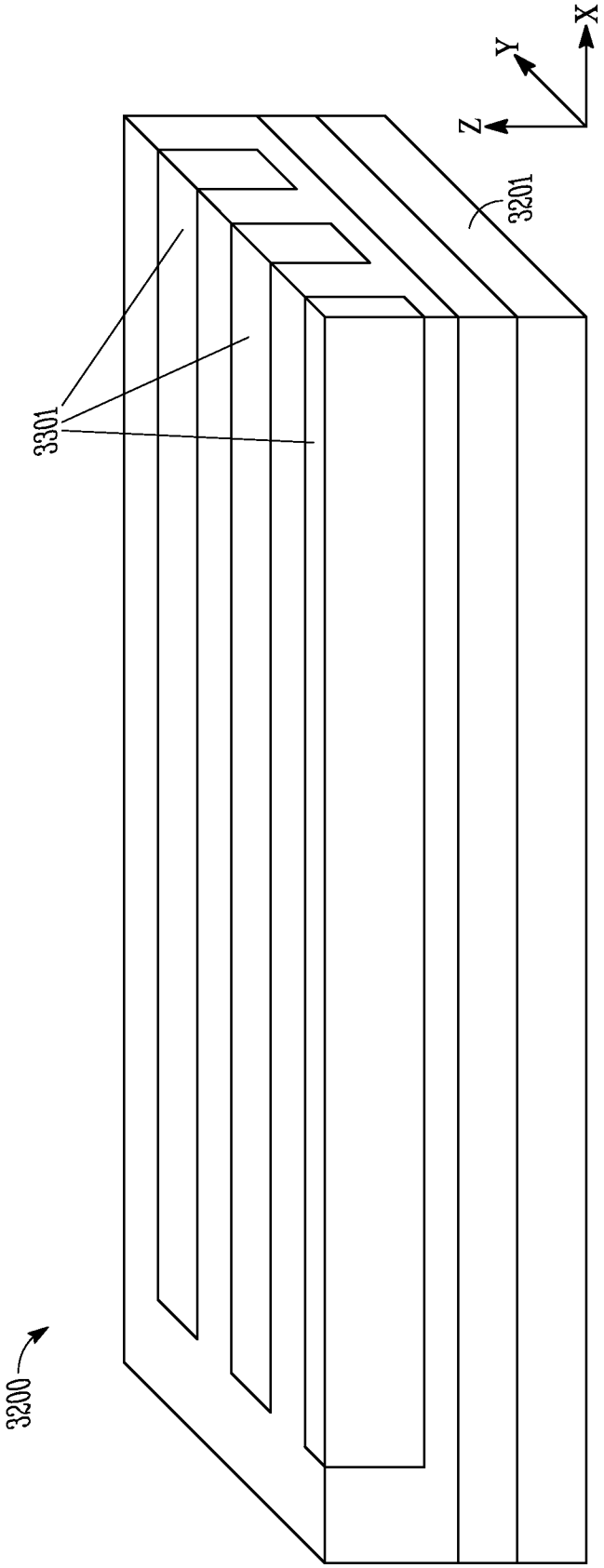


FIG. 33

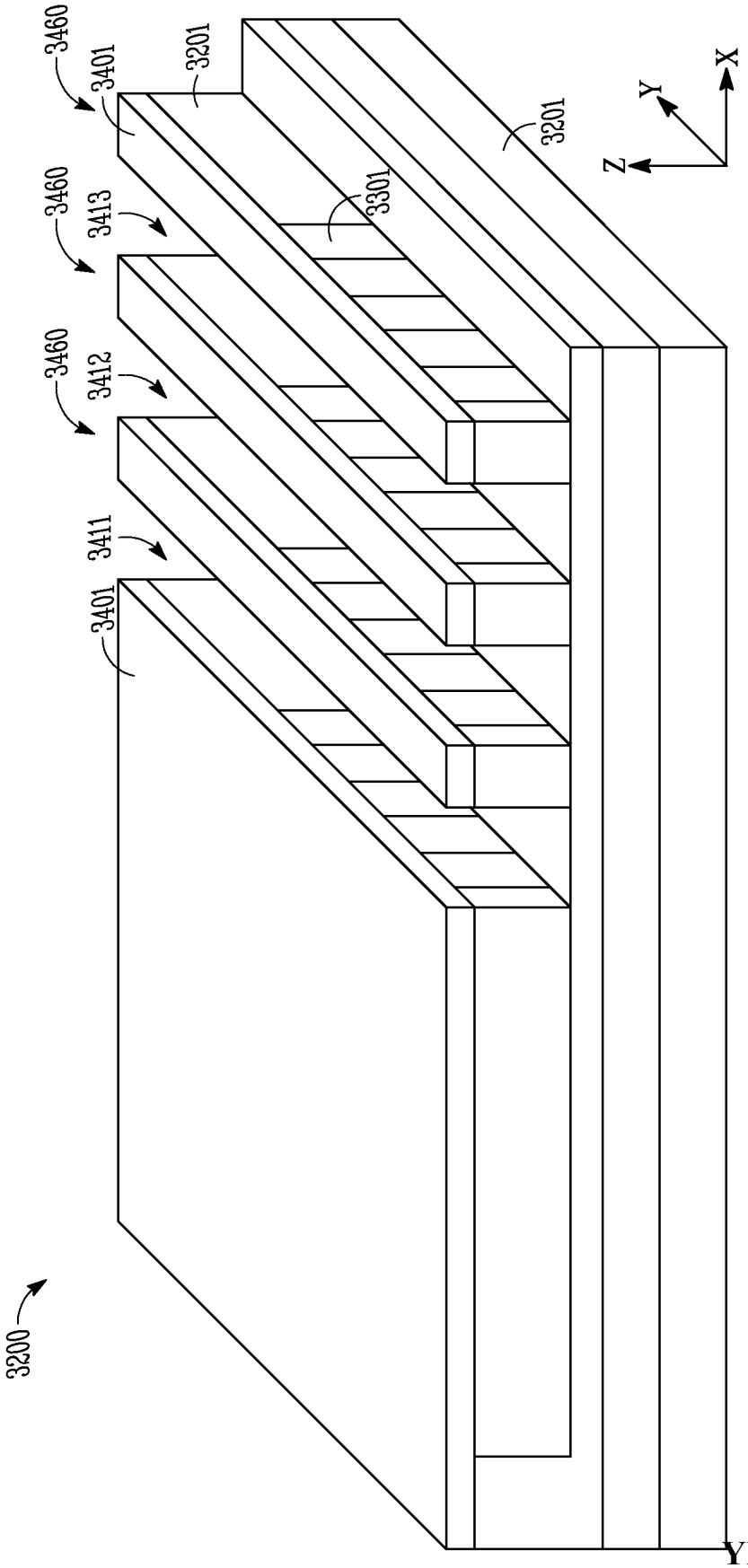

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3201
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X
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3413
3301
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3401
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FIG. 34

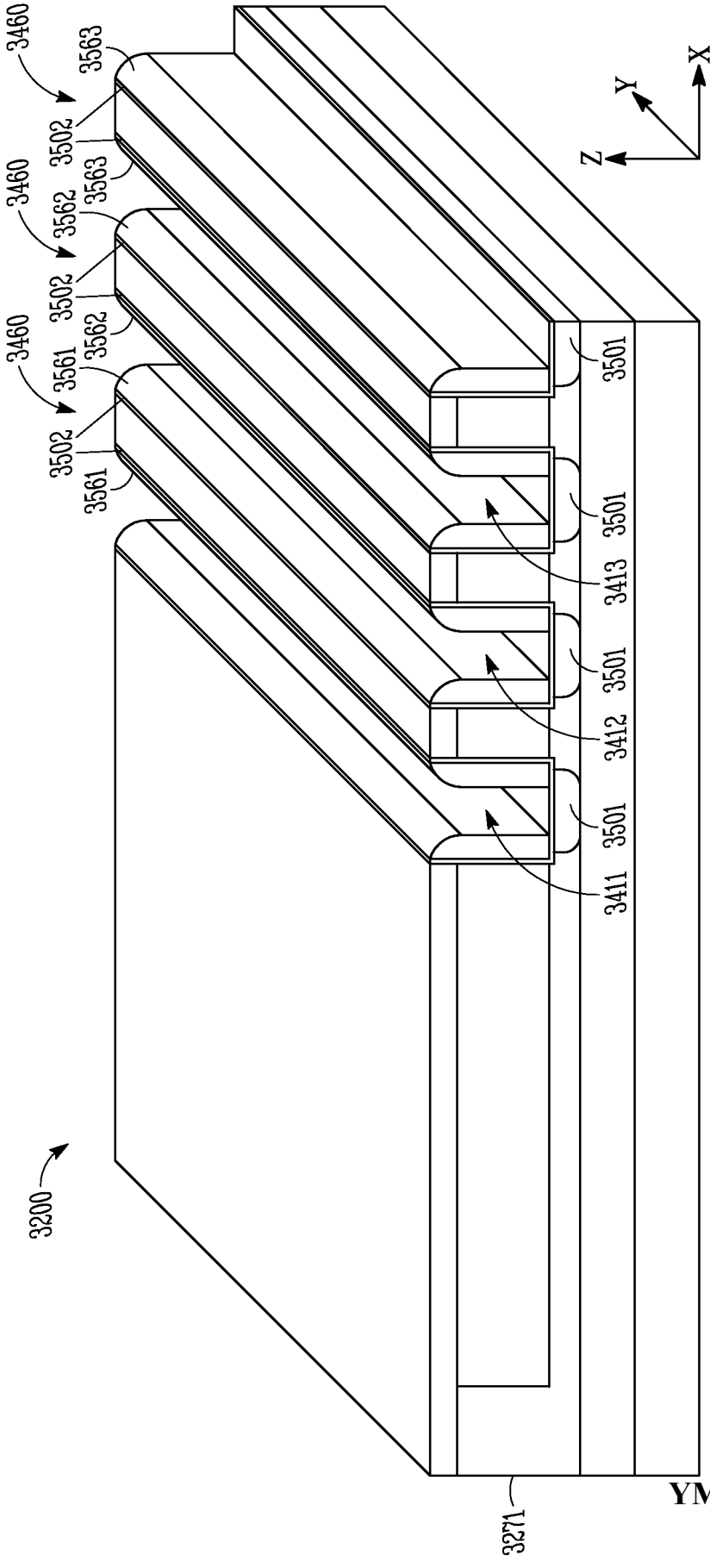

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3271
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FIG. 35

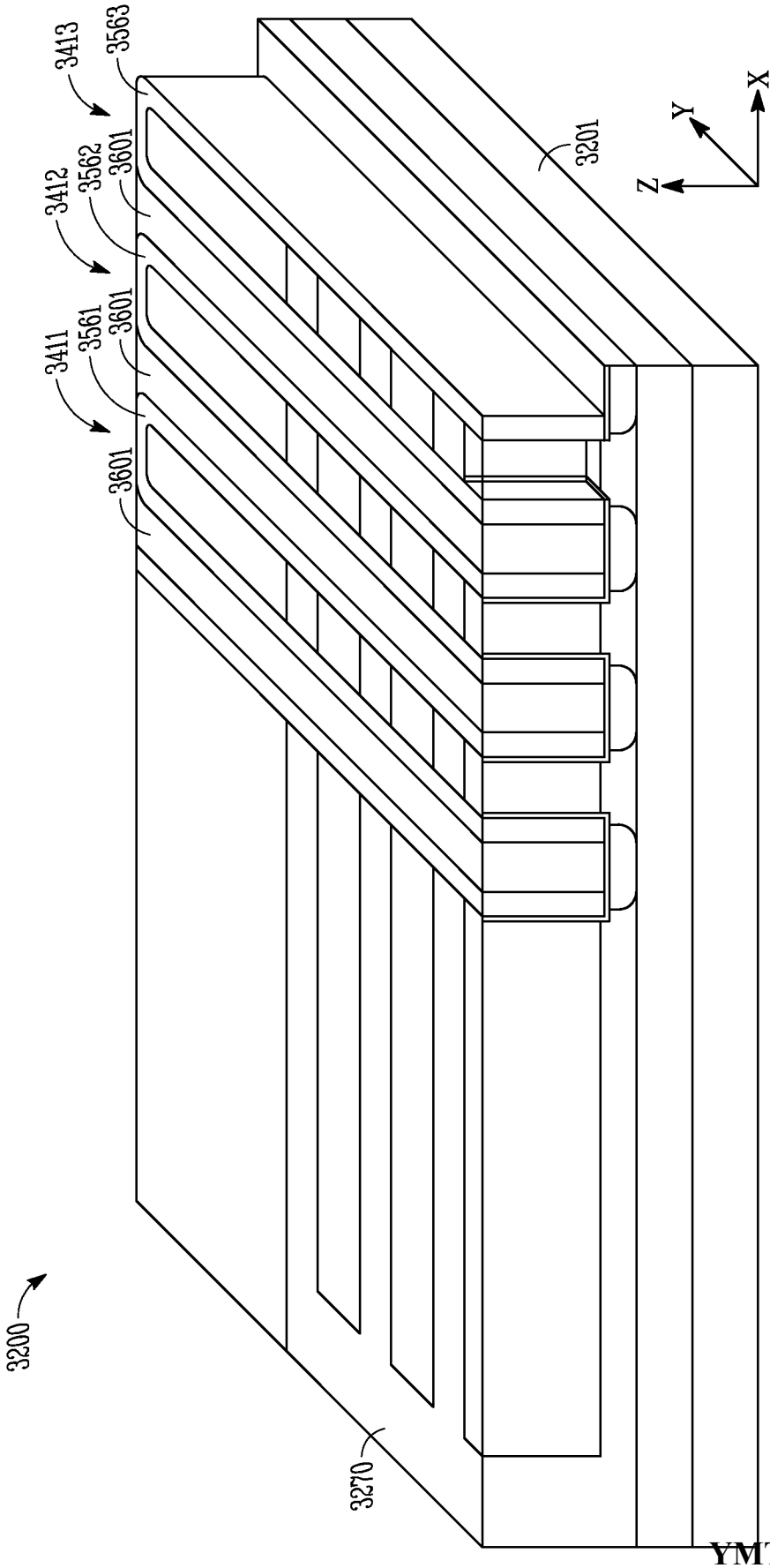

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FIG. 36

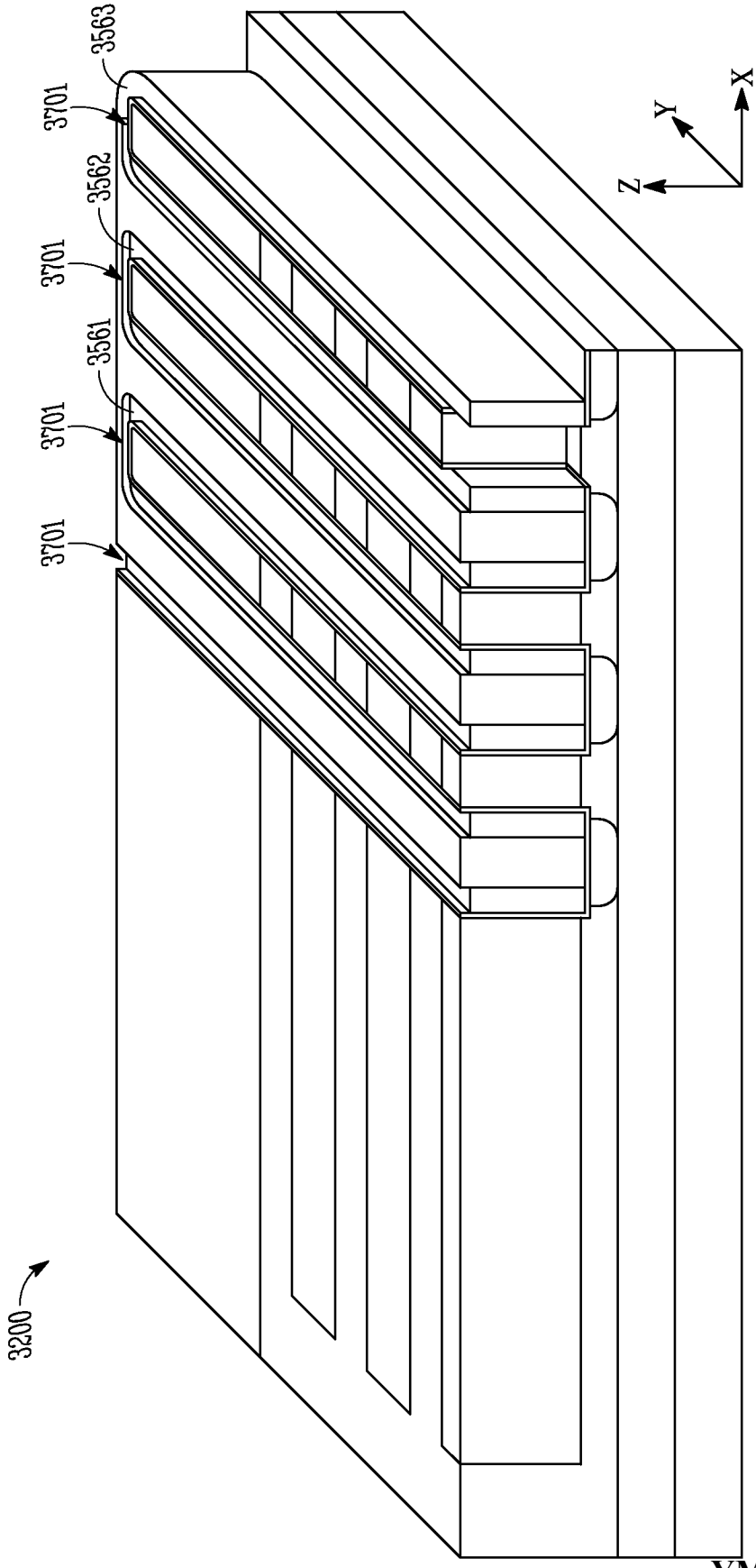


FIG. 37

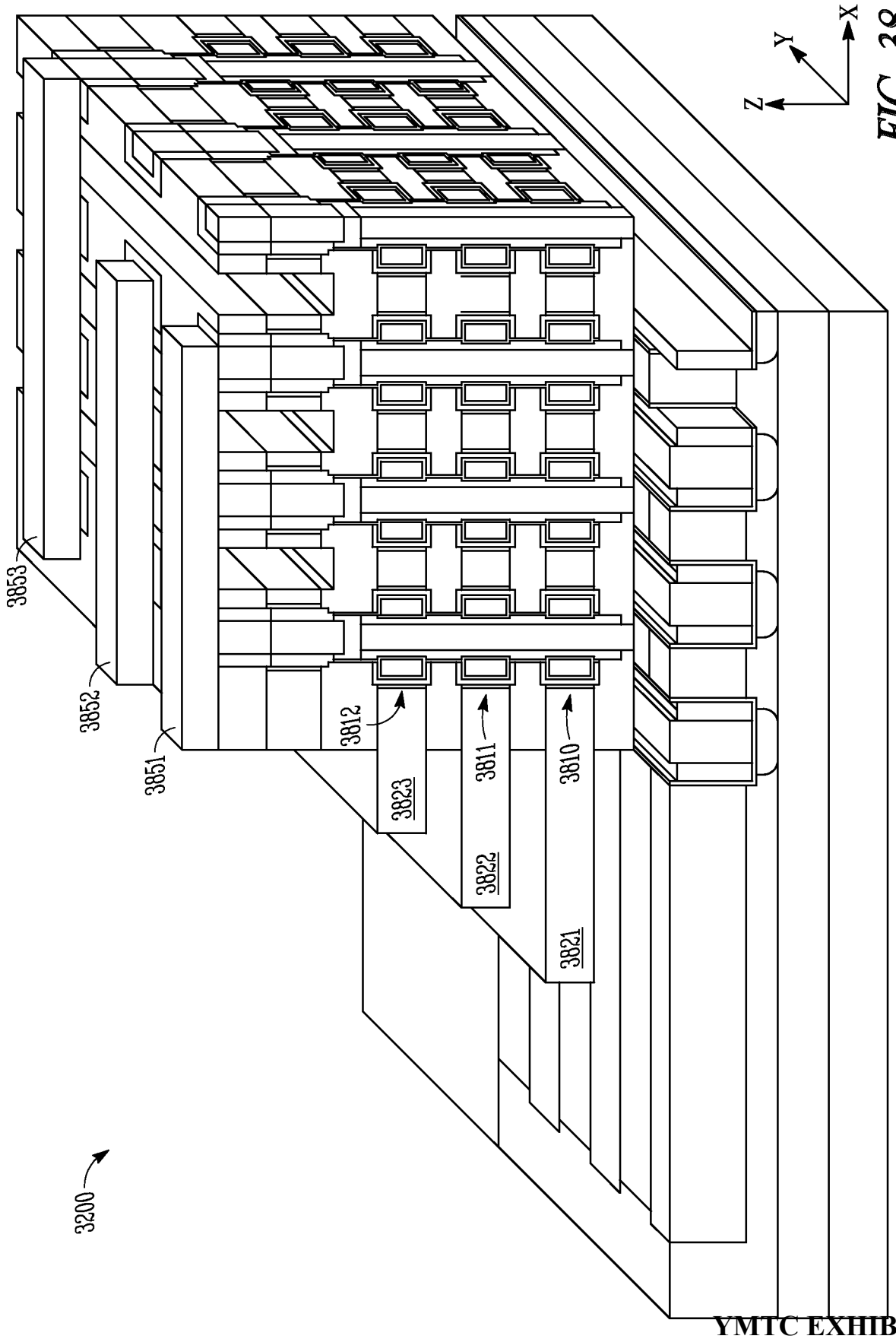


FIG. 38

Electronic Acknowledgement Receipt

EFS ID:	9702882
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	Suneel Arora/Amy Moriarty
Filer Authorized By:	Suneel Arora
Attorney Docket Number:	303.B12US1
Receipt Date:	21-MAR-2011
Filing Date:	28-JUN-2010
Time Stamp:	16:58:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303b12us1SIGNEDpamd.pdf	1364173 34659741b5830b170be65e19c3d4eee48b33d7ef	yes	42

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Preliminary Amendment	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	4
	Drawings-only black and white line drawings	5	42
Warnings:			
Information:			
	Total Files Size (in bytes):	1364173	

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National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sanh D. Tang et al.

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Docket No.:	303.B12US1	Serial No.:	12/825,211
Filed:	June 28, 2010		
Examiner:	Unknown	Group Art Unit:	2827
Customer No.:	73115	Confirmation No.:	1275

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

X Preliminary Amendment (3 pgs.)
X Formal Drawings (38 pgs.)

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer No.: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 21st day of March, 2011.

Amy Moriarty
Name

/Amy Moriarty/
Signature

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/825,211	06/28/2010	2827	2258	303.B12US1	34	5

CONFIRMATION NO. 1275

73115
SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

FILING RECEIPT

OC000000042402754

Date Mailed: 07/08/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Sanh D. Tang, Boise, ID;
John K. Zahurak, Eagle, ID;

Power of Attorney: The patent practitioners associated with Customer Number 73115

Domestic Priority data as claimed by applicant

Foreign Applications

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 07/01/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/825,211**

Projected Publication Date: 12/29/2011

Non-Publication Request: No

Early Publication Request: No

YMTC EXHIBIT 1002
Page 294 of 382

Title

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Preliminary Class

365

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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YMTC EXHIBIT 1002
Page 295 of 382

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/825,211	06/28/2010	Sanh D. Tang	303.B12US1

CONFIRMATION NO. 1275

POA ACCEPTANCE LETTER

73115
SCHWEGMAN, LUNDBERG & WOESSNER/MICRON
P.O. BOX 2938
MINNEAPOLIS, MN 55402

OC000000042402766

Date Mailed: 07/08/2010

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/28/2010.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tmelesse/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Sanh D. Tang et al.
Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
Attorney Docket No.: 303.B12US1
Customer No.: 73115

PATENT APPLICATION TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **Utility Patent Application under 37 CFR 1.53(b) comprising:**
- X Specification (30 pgs, including a 1 page coversheet, claims numbered 1 through 34 and a 1 page Abstract).
- X Formal Drawings (38 sheets).
- X Signed Declaration (3 pgs).
- X Signed Power of Attorney (1 pg) along with a copy of the signed Assignment document (4 pges)
- X Authorization to charge Deposit Account 19-0743 in the amount of $2258.00 to pay the filing fee.
- X Authorization to Permit Access (PTO/SB/39) (1 pg)

The filing fee has been calculated below as follows:

	No. Filed	No. Extra	Rate	Fee
TOTAL CLAIMS	34- 20	14	x $52.00 =	$728.00
INDEPENDENT CLAIMS	5 - 3	2	x $220.00 =	$440.00
☐MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
BASIC FEE				$330.00
SEARCH FEE				$540.00
EXAMINATION FEE				$220.00
	No. of pages (75% for e-filing)	Extra sets of 50 pages	Rate	
APPLICATION SIZE FEE	(51 - 100) / 50	0	$270.00	$0.00
TOTAL				$2258.00

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer Number: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

Date of Deposit: June 28, 2010
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Sanh D. Tang et al.
Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
Attorney Docket No.: 303.B12US1
Customer No.: 73115

PATENT APPLICATION TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items and information (as indicated with an "X"):

X **Utility Patent Application under 37 CFR 1.53(b) comprising:**
- X Specification (30 pgs, including a 1 page coversheet, claims numbered 1 through 34 and a 1 page Abstract).
- X Formal Drawings (38 sheets).
- X Signed Declaration (3 pgs).
- X Signed Power of Attorney (1 pg) along with a copy of the signed Assignment document (4 pges)
- X Authorization to charge Deposit Account 19-0743 in the amount of $2258.00 to pay the filing fee.
- X Authorization to Permit Access (PTO/SB/39) (1 pg)

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TOTAL CLAIMS	34- 20	14	x $52.00 =	$728.00
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☐MULTIPLE DEPENDENT CLAIMS PRESENTED				$0.00
BASIC FEE				$330.00
SEARCH FEE				$540.00
EXAMINATION FEE				$220.00
	No. of pages (75% for e-filing)	Extra sets of 50 pages	Rate	
APPLICATION SIZE FEE	(51 - 100) / 50	0	$270.00	$0.00
TOTAL				$2258.00

Please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
Customer Number: 73115

By: /Viet Tong/
Viet V. Tong
Reg. No. 45,416

Date of Deposit: June 28, 2010
This paper or fee is being filed on the date indicated above using the USPTO's electronic filing system EFS-Web, and is addressed to The Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO/SB/39 (12-08)
Approved for use through 01/31/2009. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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AUTHORIZATION TO PERMIT ACCESS TO APPLICATION BY PARTICIPATING OFFICES Send completed form to: Commissioner for Patents P.O. Box 1450, Alexandria, VA 22313-1450	First Named Inventor	Sanh D. Tang et al.
	Title	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
	Atty Docket Number	303.B12US1

The undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), and any other intellectual property offices in which a foreign application claiming priority to the above-identified application is filed access to the above-identified patent application. See 37 C.F.R. § 1.14(c) and (h).

In accordance with 37 C.F.R. § 1.14(h)(3), access will be provided to a copy of the application-as-filed with respect to: 1) the above-identified application, 2) any foreign application to which the above-identified application claims priority under 35 U.S.C. § 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 C.F.R. § 1.55 has been filed in the above-identified US application, and 3) any U.S. application from which benefit is sought in the above-identified application.

In accordance with 37 C.F.R. § 1.14(c), access may be provided to information concerning the date of filing the Authorization to Permit Access to Application by Participating Offices.

This written authorization should be submitted prior to the filing of a subsequent foreign application, in which priority is claimed to the above-identified patent application, with any intellectual property office (e.g., the EPO, JPO, or KIPO). However, if applicant does not wish the EPO, JPO, KIPO, or other intellectual property office in which a foreign application claiming priority to the above-identified application is filed to have access to the application, this written authorization should not be filed.

No fee will be charged under 37 C.F.R. § 1.19(b)(1) for providing a participating intellectual property office with an electronic copy of the above-identified application.

This form must be signed by an authorized party in accordance with 37 C.F.R. § 1.14(c).

/Viet Tong/	6-28-10
Signature	Date
Viet V. Tong, Reg No. 45,416	(612) 373-6969
Typed or printed name	Telephone Number

This collection of information is required by 37 CFR 1.14(h). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process an application). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Date of Deposit: June 28, 2010
This paper or fee is being filed on the date indicated above using the USPTO's electronic filing system EFS-Web, and is addressed to The Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

SCHWEGMAN ■ LUNDBERG ■ WOESSNER

United States Patent Application

DECLARATION

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME**,

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability of this application in accordance with 37 C.F.R. § 1.56 (attached hereto). I also acknowledge my duty to disclose all information known to be material to patentability which became available between a filing date of a prior application and the national or PCT international filing date in the event this is a Continuation-In-Part application in accordance with 37 C.F.R. § 1.63(e).

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or 365(b) of, and incorporate in the present patent application by reference, any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 119(e) of, and incorporate in the present patent application by reference, any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of, and incorporate in the present patent application by reference, any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

No such claim for priority is being made at this time.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of joint inventor number 1: **Sanh D. Tang**
Citizenship: **United States of America** Residence: **Boise, ID**
Post Office Address: ~~1273 North Jullian Avenue~~ ST.
~~Boise, ID 83704~~
11587 W. VERDE Dr
Boise ID 83709

Signature: Sanh D. Tang Date: 06-23-2010
Sanh D. Tang

Full Name of joint inventor number 2: **John K. Zahurak**
Citizenship: **United States of America** Residence: **Eagle, ID**
Post Office Address: 2633 W. Sugarberry Drive
Eagle, ID 83616

Signature: John K. Zahurak Date: 6/24/2010
John K. Zahurak

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Sanh D. Tang et al.	Examiner:	Unknown
Serial No.:	Unknown	Group Art Unit:	Unknown
Filed:	Herewith	Docket:	303.B12US1

Customer No.: 73115

Title: THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

POWER OF ATTORNEY BY ASSIGNEE, CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b), AND NOTIFICATION OF CORRESPONDENCE ADDRESS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Micron Technology, Inc., assignee of the entire right, title and interest in the above-identified application by assignment from the inventor(s), hereby appoints the attorneys and agents of the firm of SCHWEGMAN, LUNDBERG & WOESSNER, P.A., listed under:

Customer Number: 73115

as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The assignee certifies that the above-identified assignment has been reviewed and to the best of the assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to:

Schwegman, Lundberg & Woessner, P.A.
Customer No. 73115

Telephone: (612) 373-6900
Facsimile: (612) 339-3061

MICRON TECHNOLOGY, INC.

Dated: 6/25/10

By: _____

Name: Russell D. Slifer

Title: Chief Patent Counsel

ASSIGNMENT

WHEREAS, We, Sanh D. Tang, residing at 1273 North Jullian Avenue, Boise, ID 83704, and John K. Zahurak, residing at 2633 W. Sugarberry Drive, Eagle, ID 83616, made certain new and useful inventions and improvements which are described in an application for U.S. Letters Patent entitled THREE DIMENSIONAL MEMORY AND METHODS OF

FORMING THE SAME;

WHEREAS, We hereby authorize and request the attorneys, representing Micron Technology, Inc. on this application, at Schwegman, Lundberg & Woessner, P.A., located at 121 South Eighth Street, Suite 1600, Minneapolis, MN 55402, to insert here in parentheses (Ser. No. _____; Filing Date: _____) the filing date and application number of said application when known.

FOR GOOD AND VALUABLE CONSIDERATION, the receipt, sufficiency and adequacy of which are hereby acknowledged, the undersigned do hereby:

SELL, ASSIGN AND TRANSFER to Micron Technology, Inc. (the "Assignee"), a corporation of the State of Delaware, having a place of business at 8000 So. Federal Way, Boise, ID 83716-9632, the entire right, title and interest for the United States and all foreign countries in and to: any and all inventions and improvements which are disclosed in the identified application for U.S. Letters Patent, and which may be further identified below; such application and all divisional, continuing, substitute, renewal, reissue and all other applications for patent which have been or shall be filed in the United States (including all provisional and non-provisional applications), and in all foreign countries on any of such inventions and/or improvements (including any applications for utility models); all original and reissued patents which have been or shall be issued in the United States and all foreign countries on such inventions and/or improvements; and specifically including the right to file foreign applications under the provisions of any convention or treaty and to claim priority based on the identified application;

AUTHORIZE AND REQUEST that any attorney associated with U.S. PTO Customer No. 73115 may (directly or through his/her designee) delete, insert, or alter any information identifying this application, or any related application, below, after execution of this Assignment;

Additional Application Information

No Provisional claim for priority is being made at this time.

No U.S. Non-Provisional claim for priority is being made at this time.

No International or foreign claim for priority is being made at this time.

AUTHORIZE AND REQUEST the issuing authority to issue any and all United States and foreign patents granted on such improvements to the Assignee;

WARRANT AND COVENANT that no assignment, grant, mortgage, license or other agreement affecting the rights and/or property herein conveyed has been or will be made to others by the undersigned, and that the full right to convey the same as herein expressed is possessed by the undersigned;

COVENANT, that when requested and without compensation, but at the expense of the Assignee, in order to carry out in good faith the intent and purpose of this Assignment, the undersigned will (1) execute all provisional, non-provisional, divisional, continuing, substitute, renewal, reissue, and all other patent applications on any and all such improvements; (2) execute all rightful oaths, declarations, assignments, powers of attorney and other papers; (3) communicate to the Assignee all facts known to the undersigned relating to such improvements and the history thereof; (4) cooperate with the Assignee in any interference, reexamination, reissue, opposition, dispute, or litigation involving any of the applications or patents for such improvements; and (5) take such further actions as the Assignee shall reasonably consider necessary or desirable for vesting title to such improvements in the Assignee, or for securing, maintaining and enforcing proper patent protection for such improvements;

THIS AGREEMENT IS TO BE BINDING on the heirs, assigns, representatives and successors of the undersigned, and is to extend to the benefit of the successors, assigns and nominees of the Assignee.

AGREED as of the date of my signature below:

IN TESTIMONY WHEREOF, I have hereunto set my hand this 23 day of June, 2010.

Sanh D. Tang

STATE OF Idaho)
)ss
COUNTY OF Ada)

On this 23rd day of June, 2010 before me personally appeared Sanh D. Tang, to me known and known to me to be the person described in and who executed the foregoing instrument, and he/she duly acknowledged to me that he/she executed the same for the uses and purposes therein set forth.

KELLI C. BAUER NOTARY PUBLIC STATE OF IDAHO

Notary Public

exp: 2/28/2012

Docket No: 303.B12US1

IN TESTIMONY WHEREOF, I have hereunto set my hand this 24 day of June, 2010.

John K. Zahurak

STATE OF Idaho)
)ss
COUNTY OF Ada)

On this 24th day of June, 2010 before me personally appeared John K. Zahurak, to me known and known to me to be the person described in and who executed the foregoing instrument, and he/she duly acknowledged to me that he/she executed the same for the uses and purposes therein set forth.

[SEAL] KELLI C. BAUER NOTARY PUBLIC STATE OF IDAHO

Kelli C Bauer
Notary Public exp: 2/28/2012

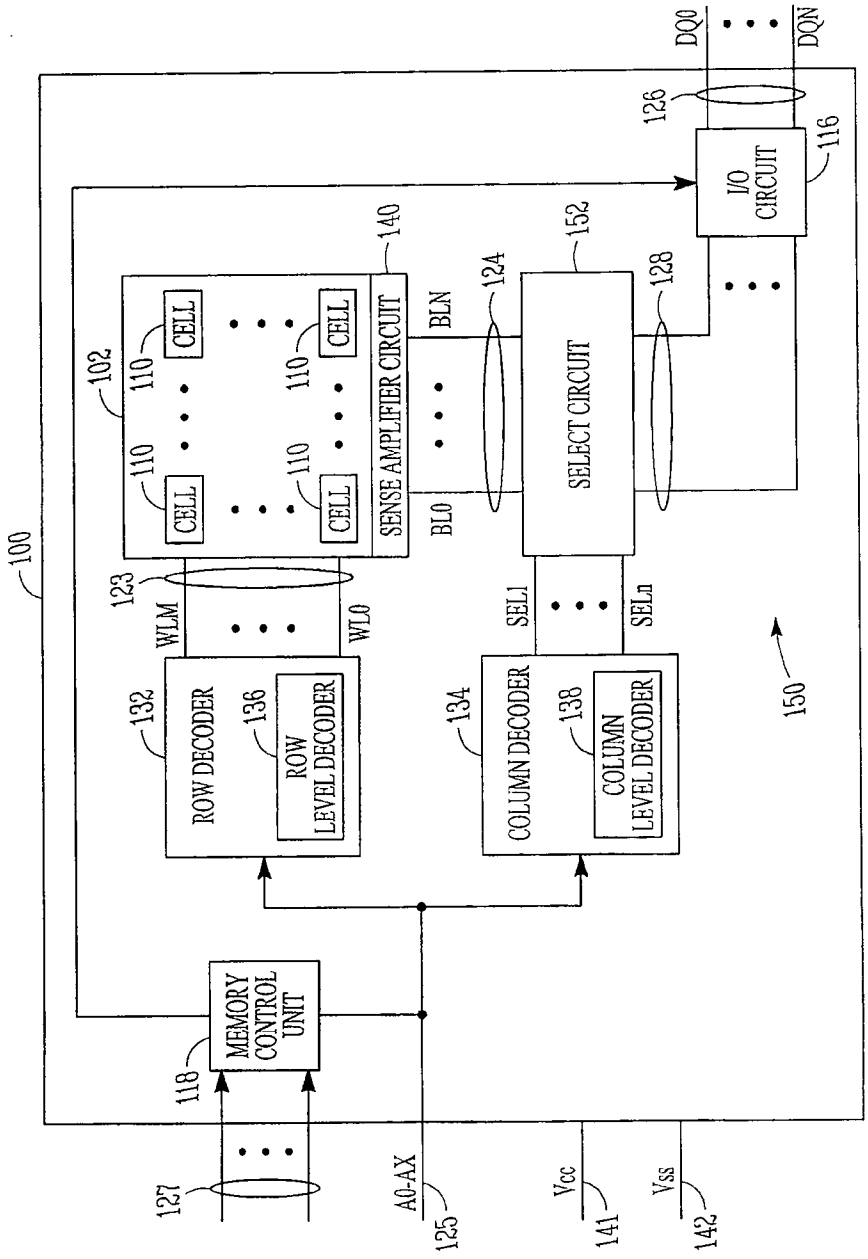

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WLM
WL0
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ROW DECODER
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ROW LEVEL DECODER
SEL1
SELn
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COLUMN DECODER
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FIG. 1

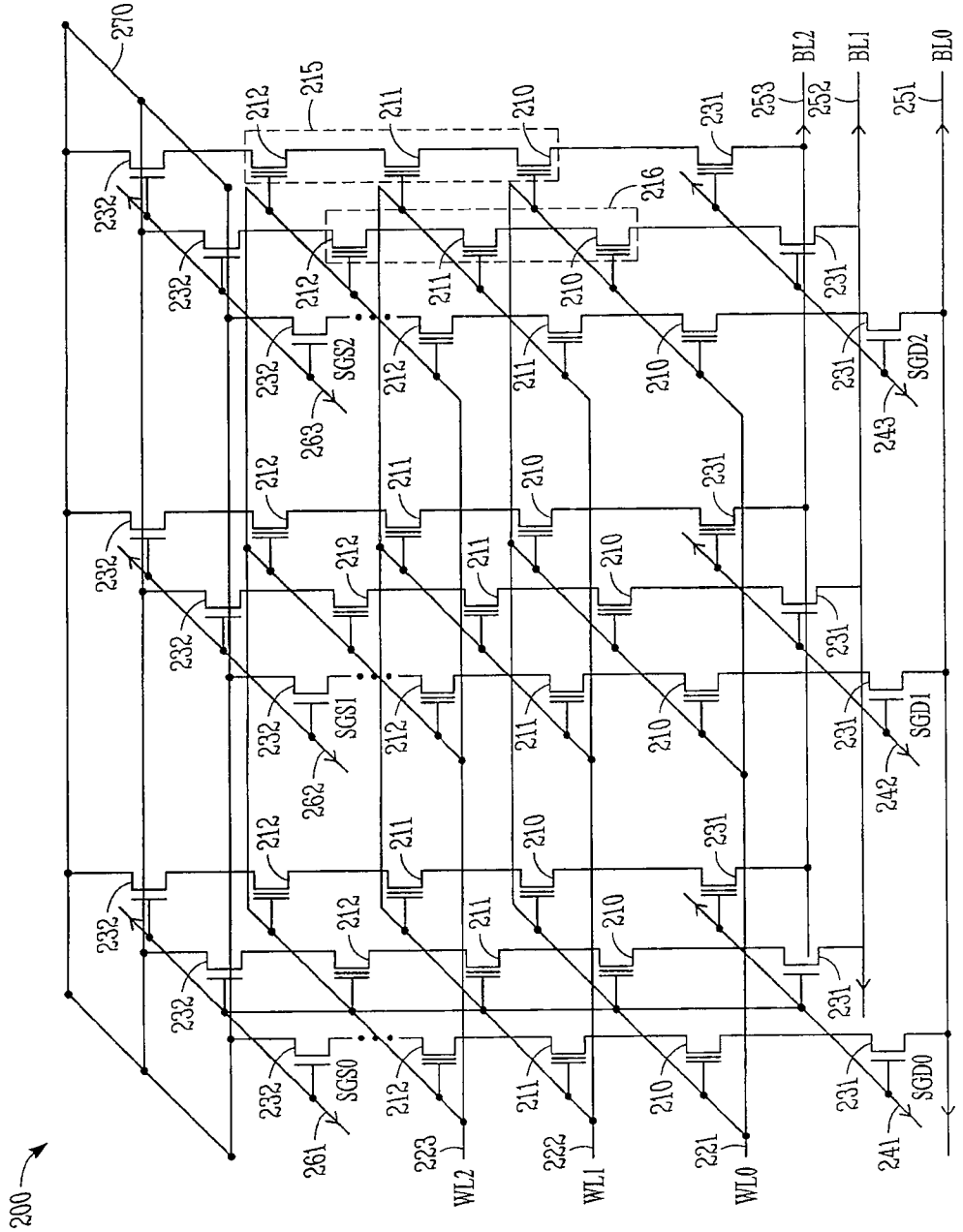

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FIG. 2

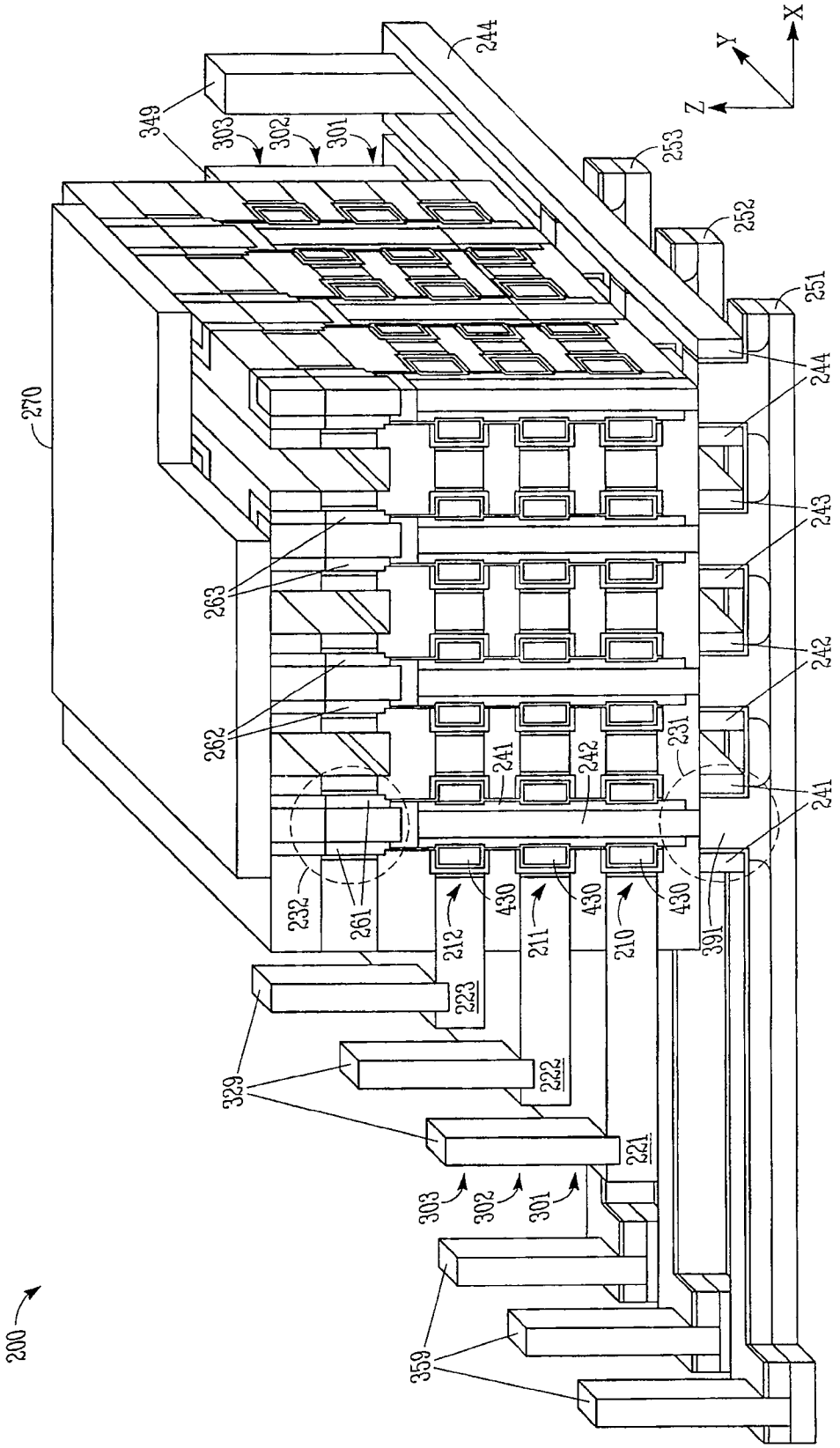

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FIG. 3

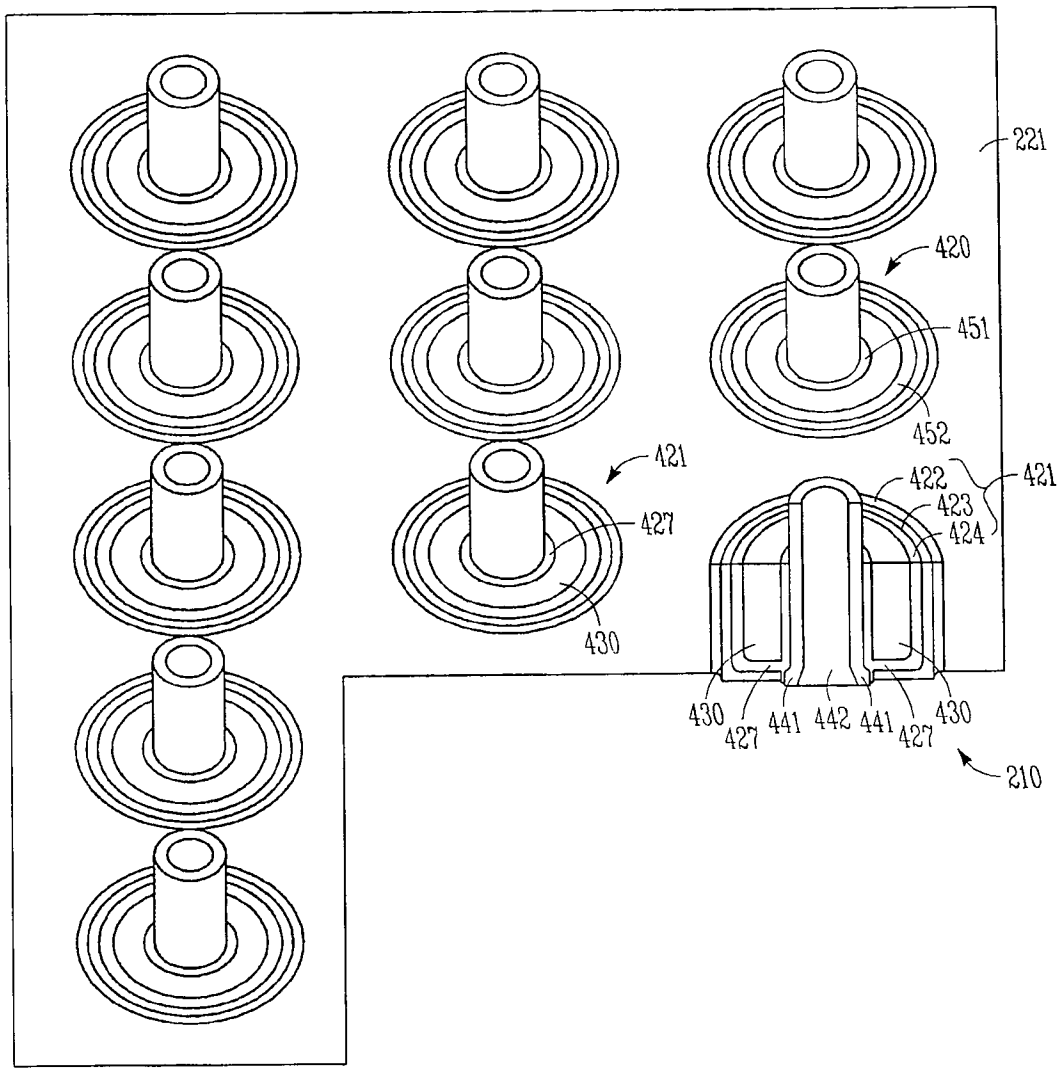

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FIG. 4

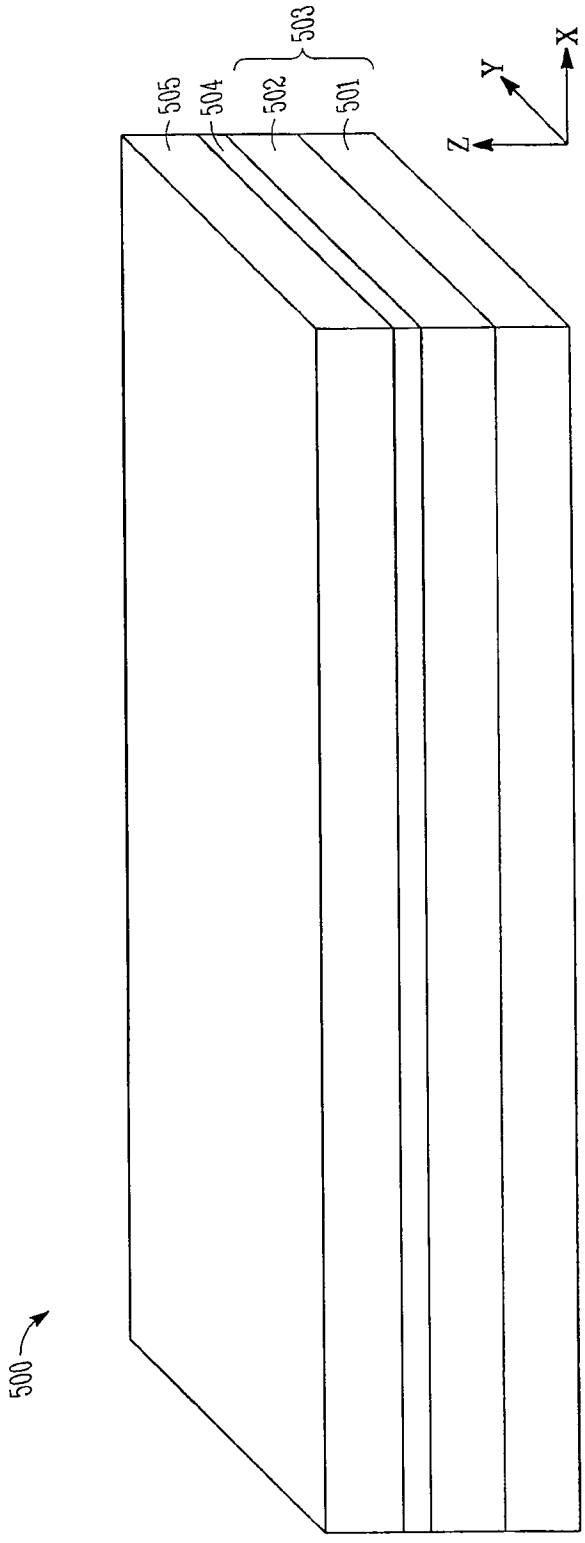


FIG. 5

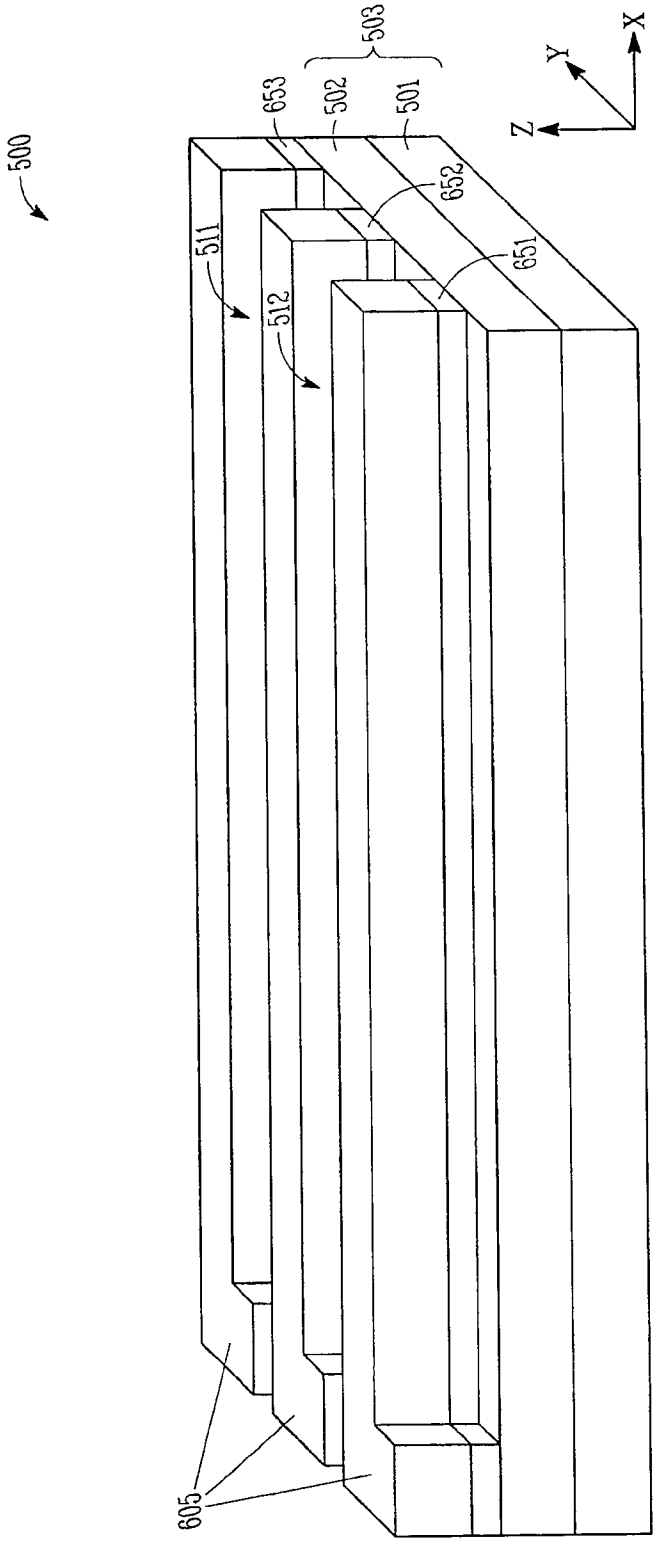


FIG. 6

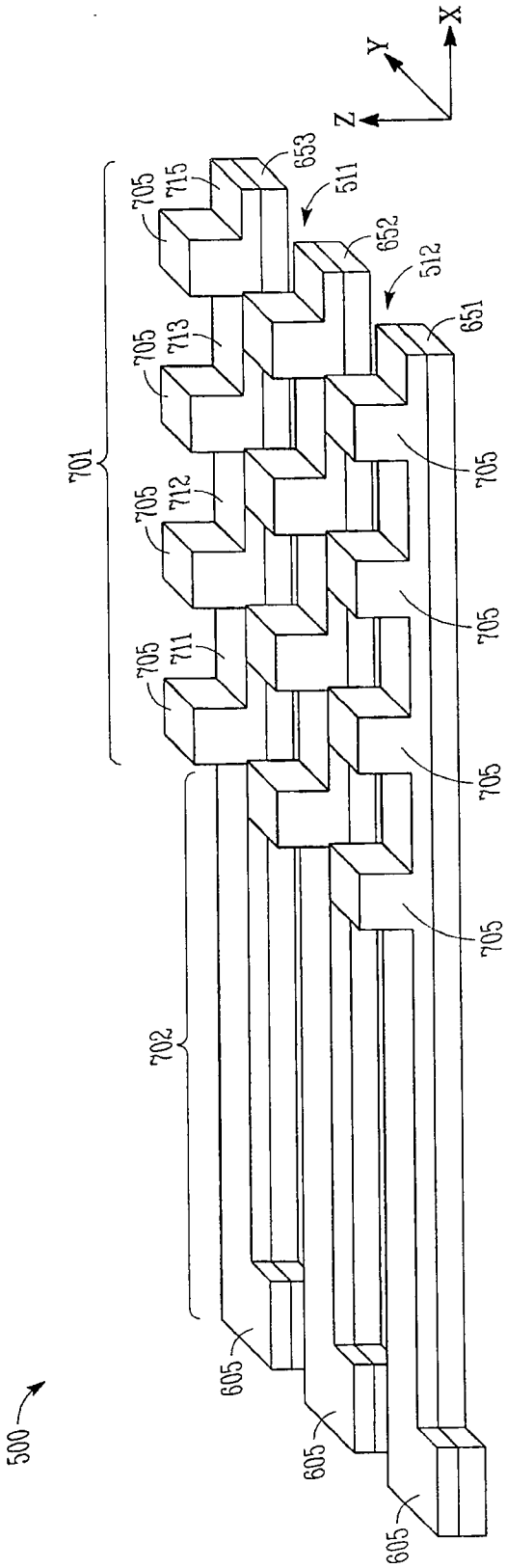


FIG. 7

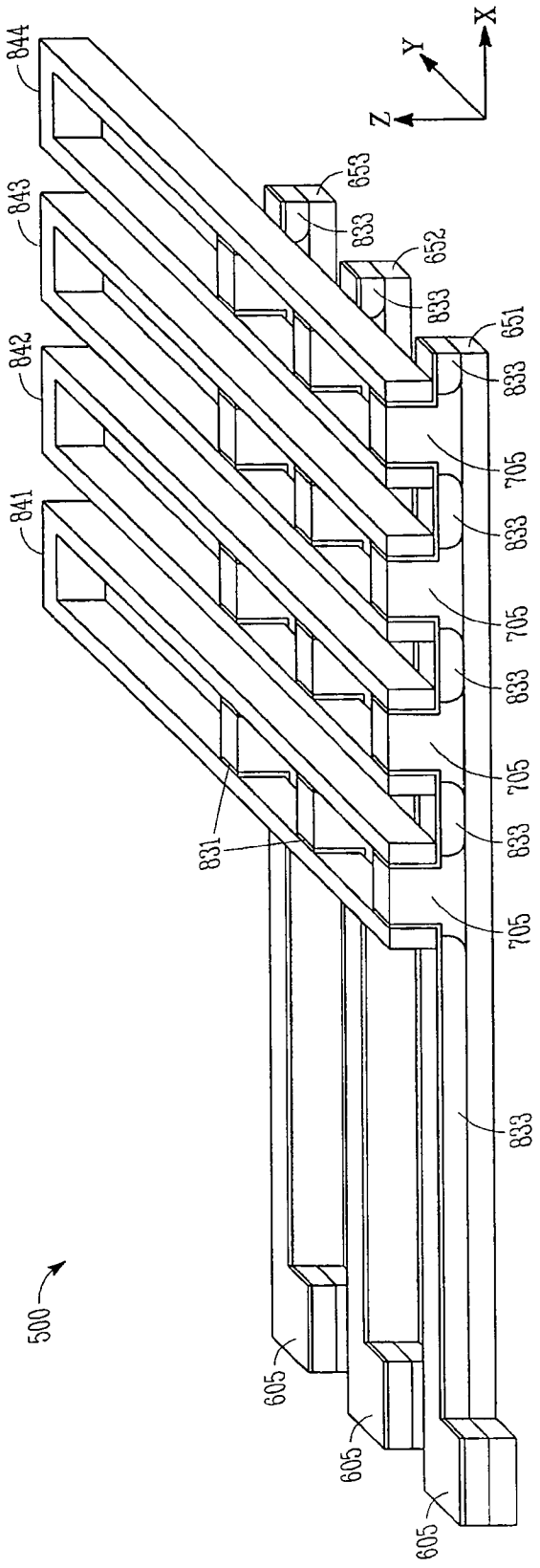


FIG. 8

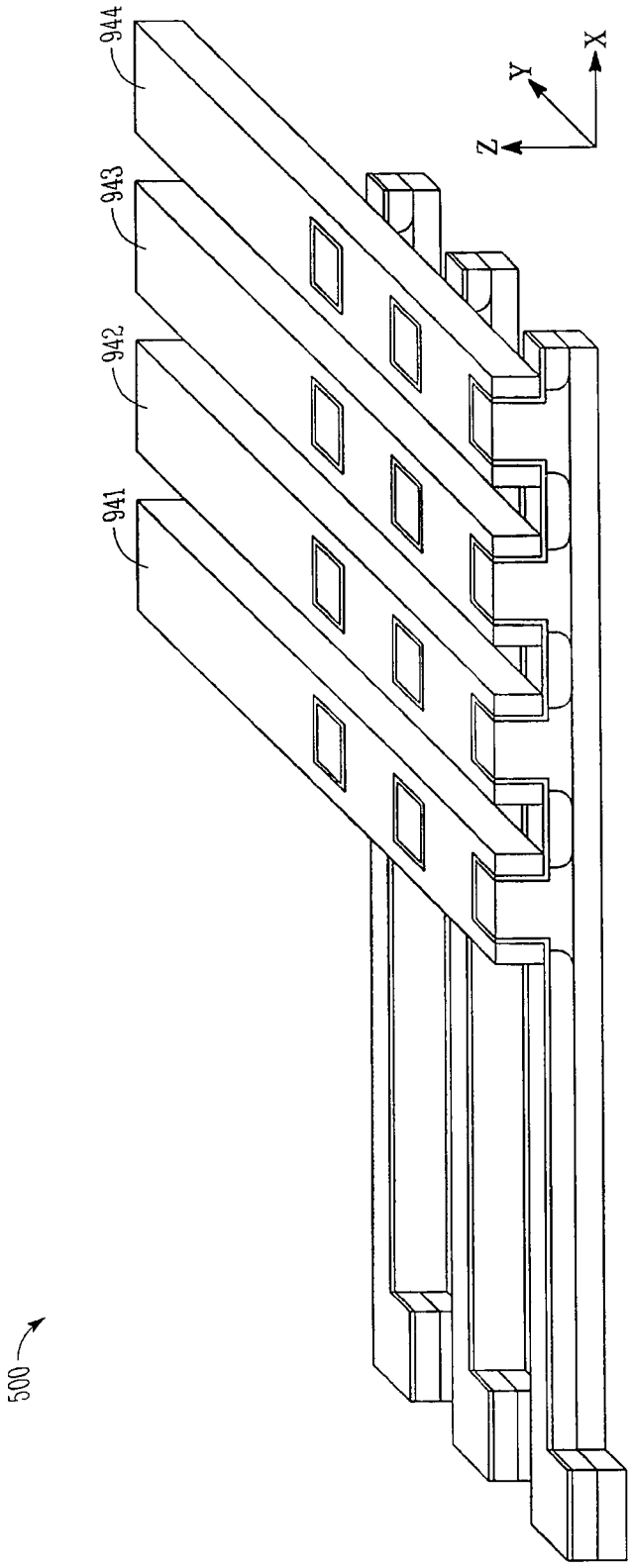


FIG. 9

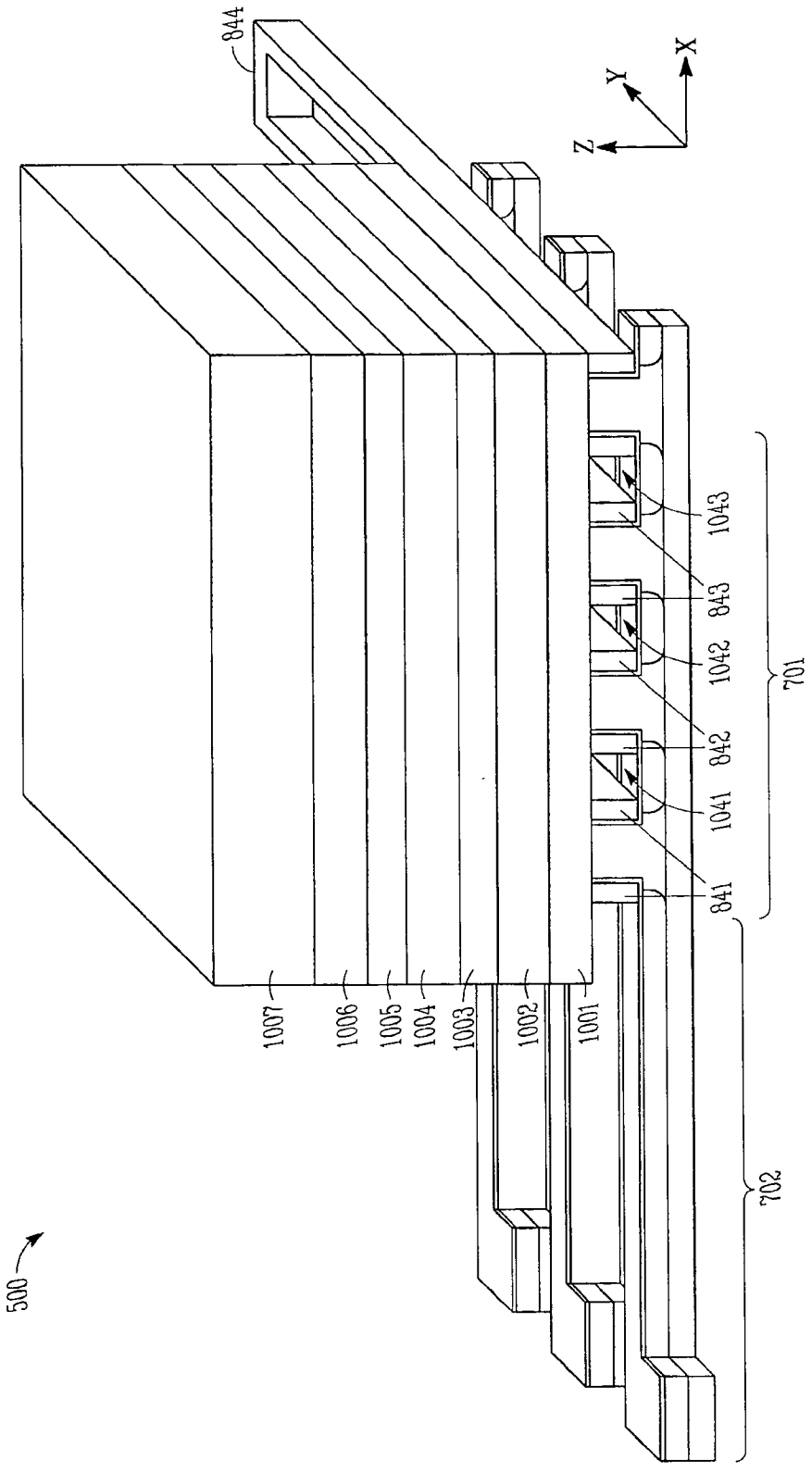

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FIG. 10

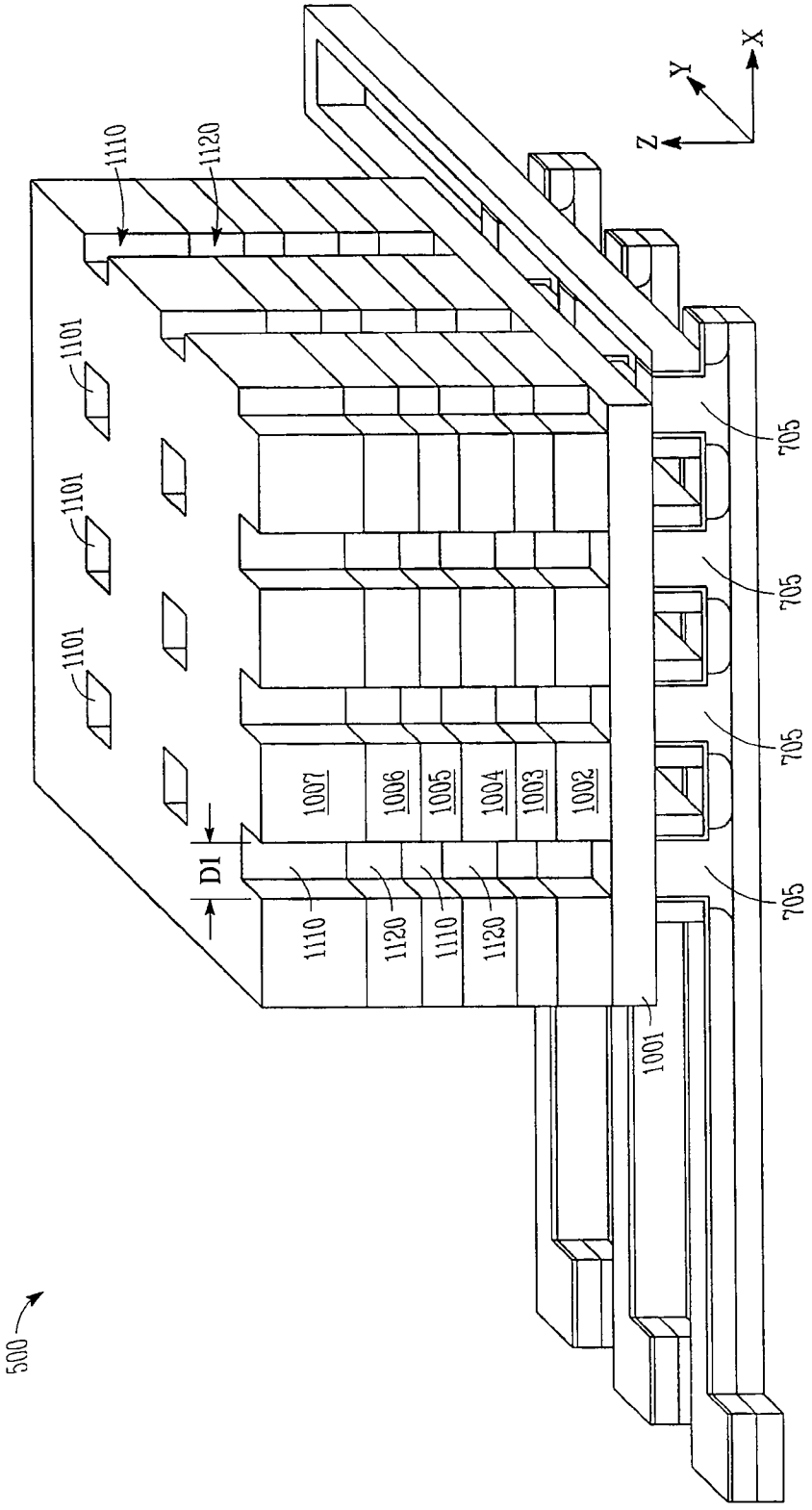

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X

FIG. 11

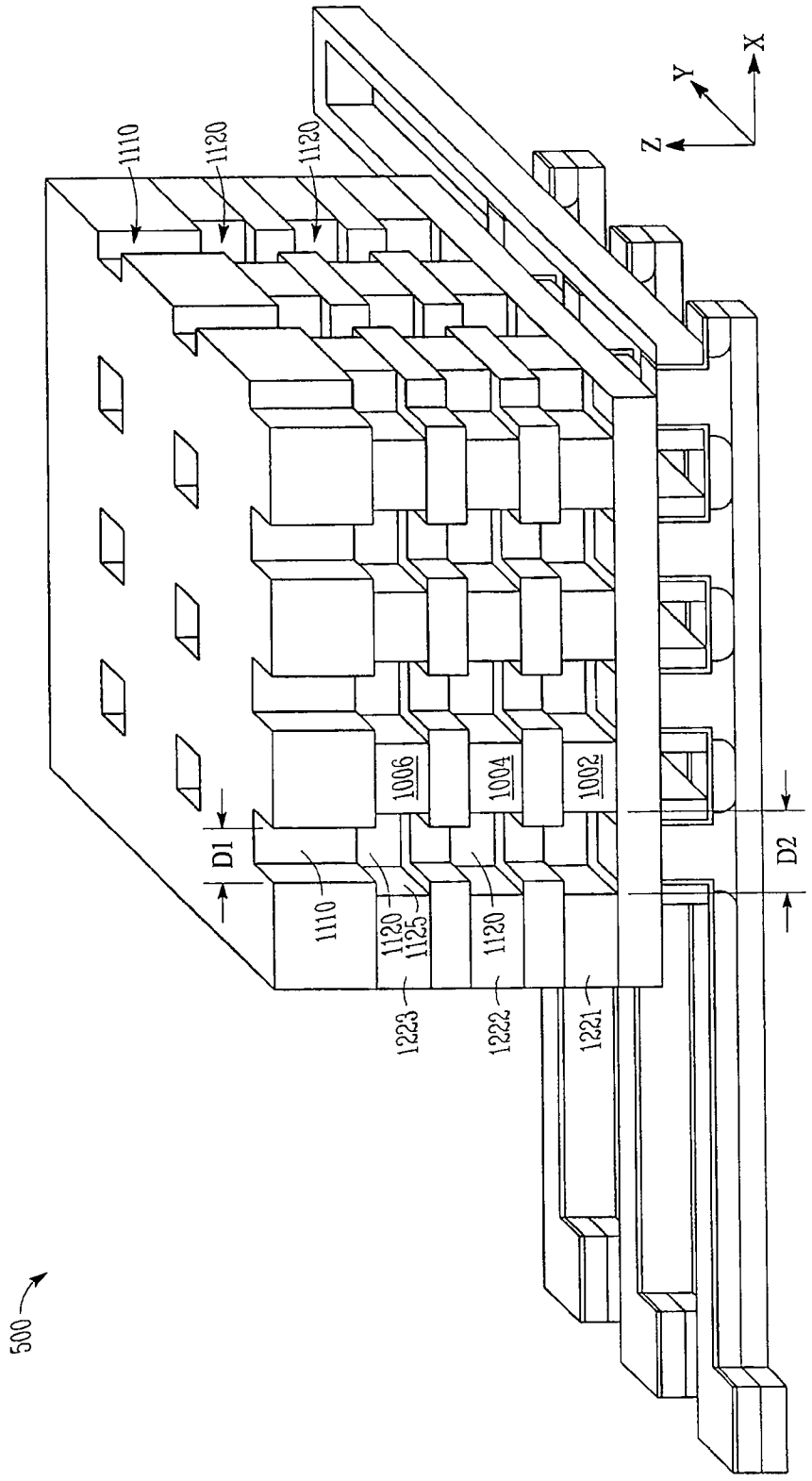

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FIG. 12

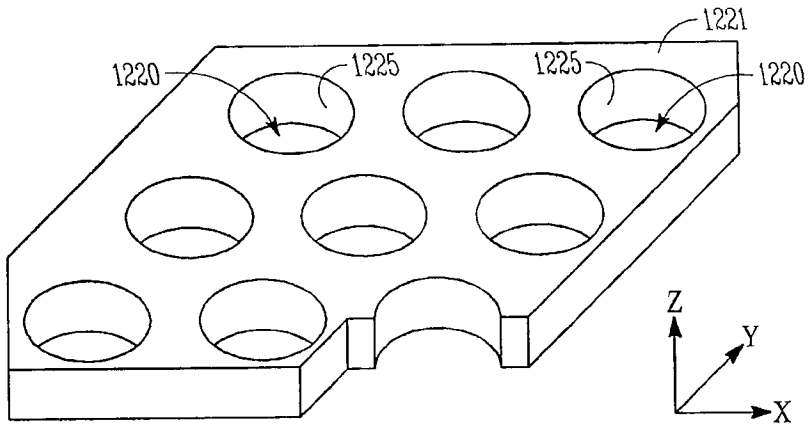


FIG. 13

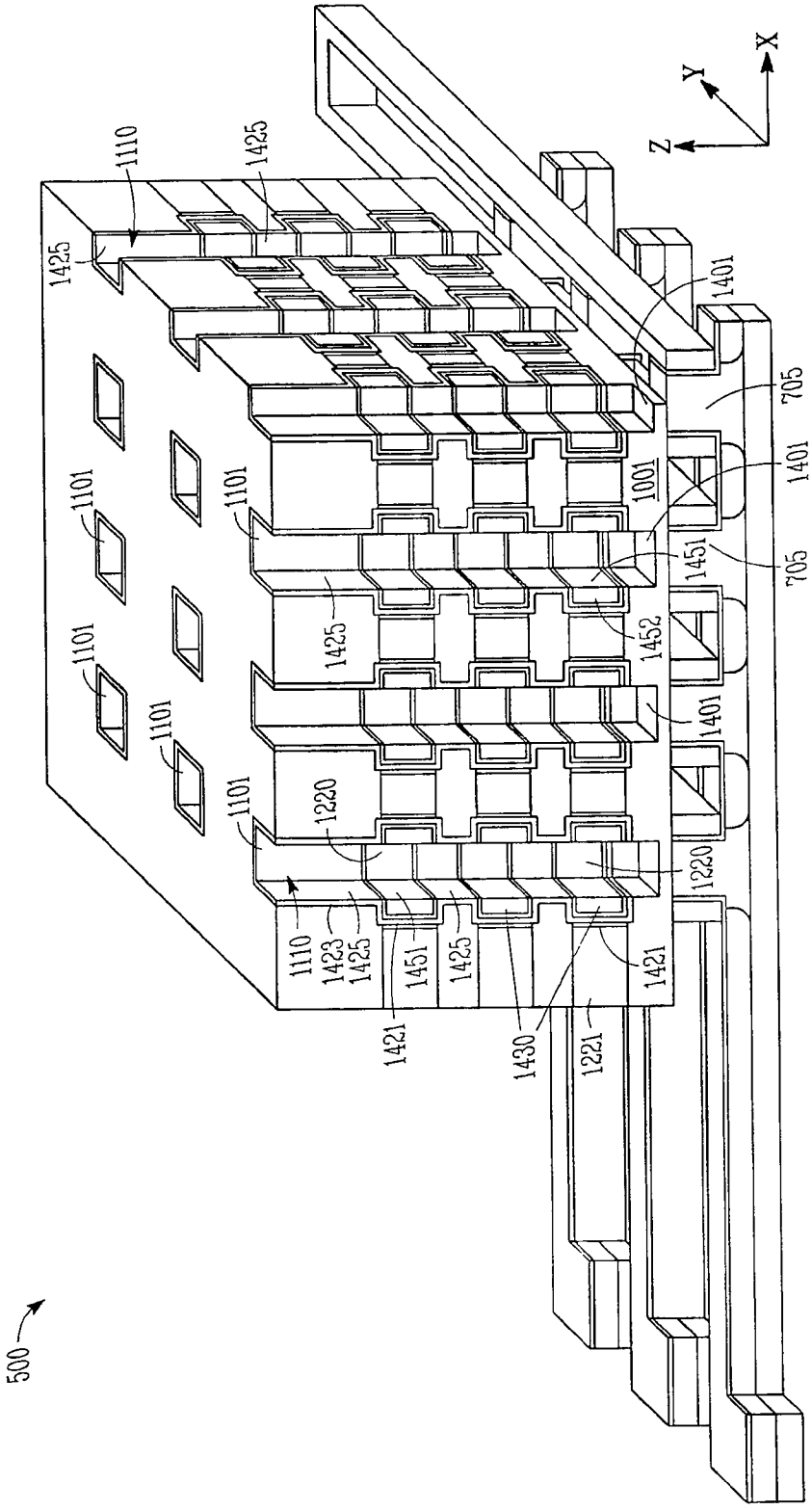

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FIG. 14

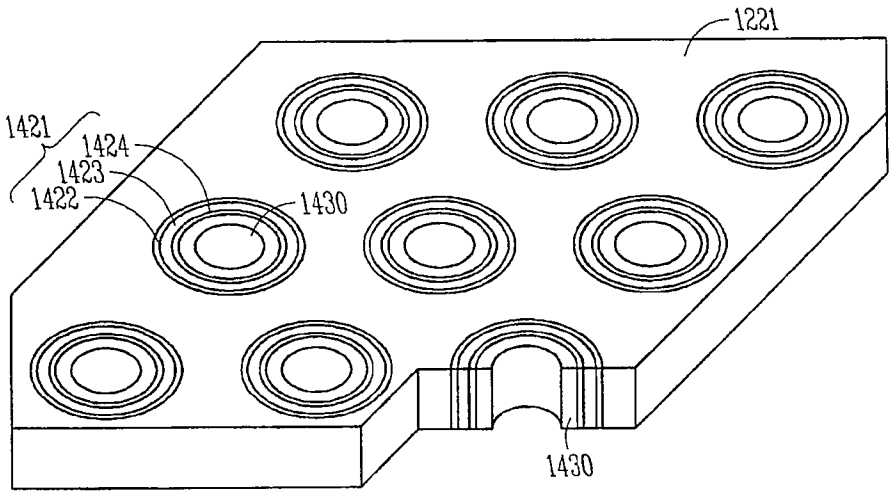


FIG. 15

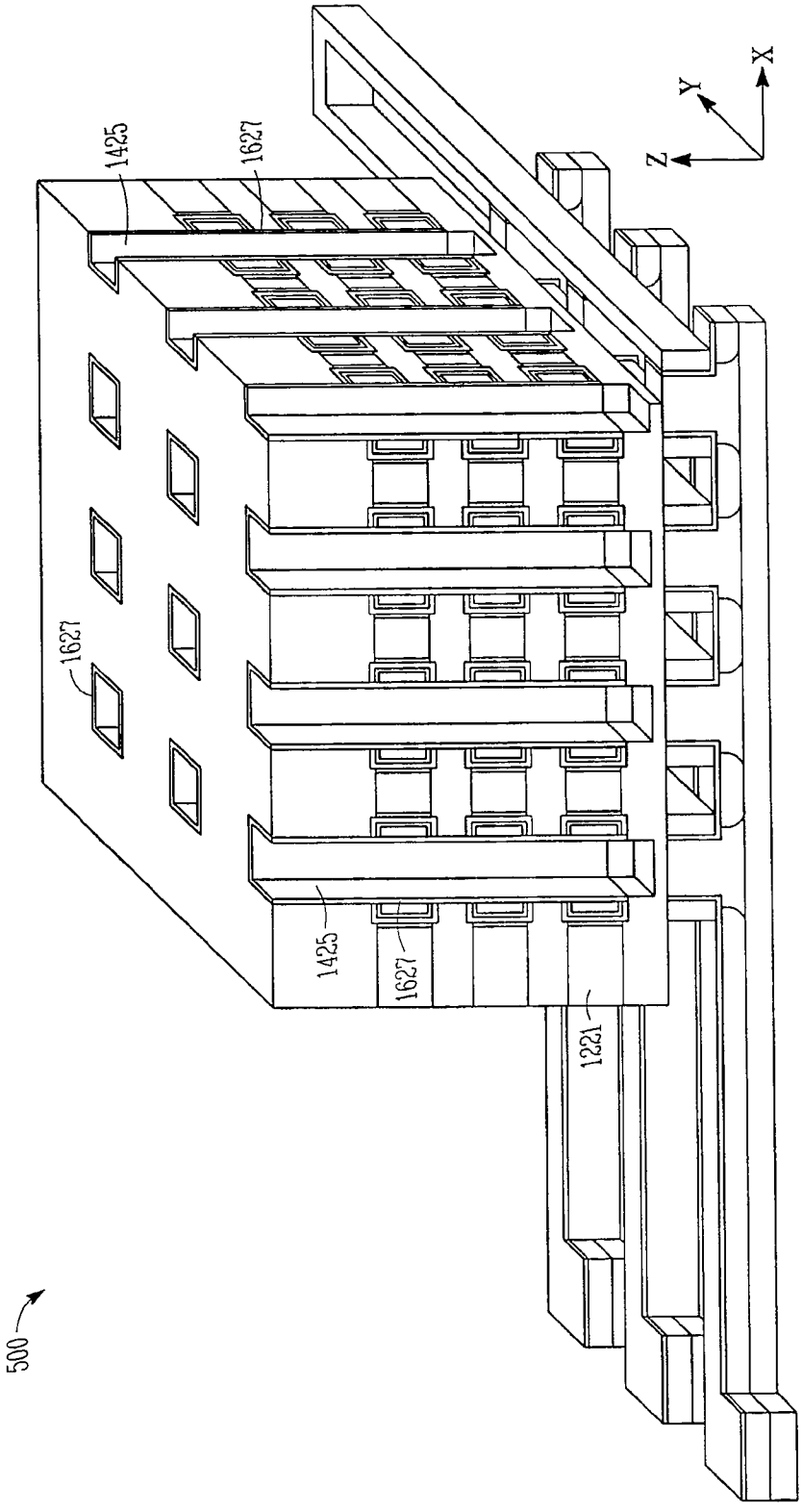


FIG. 16

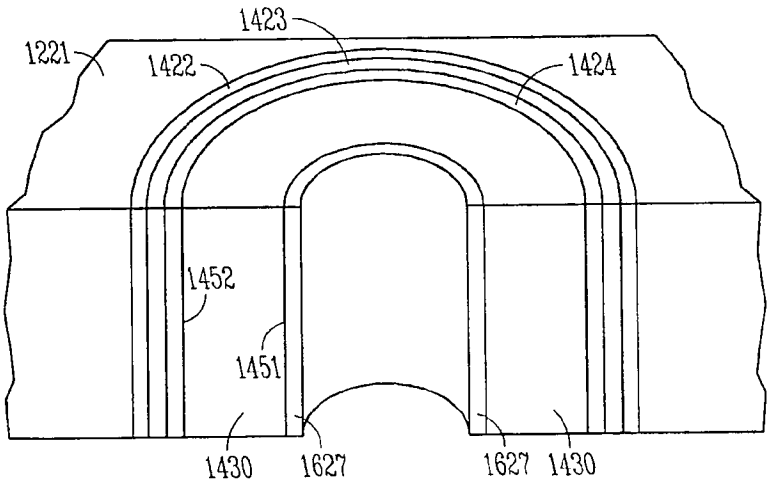


FIG. 17

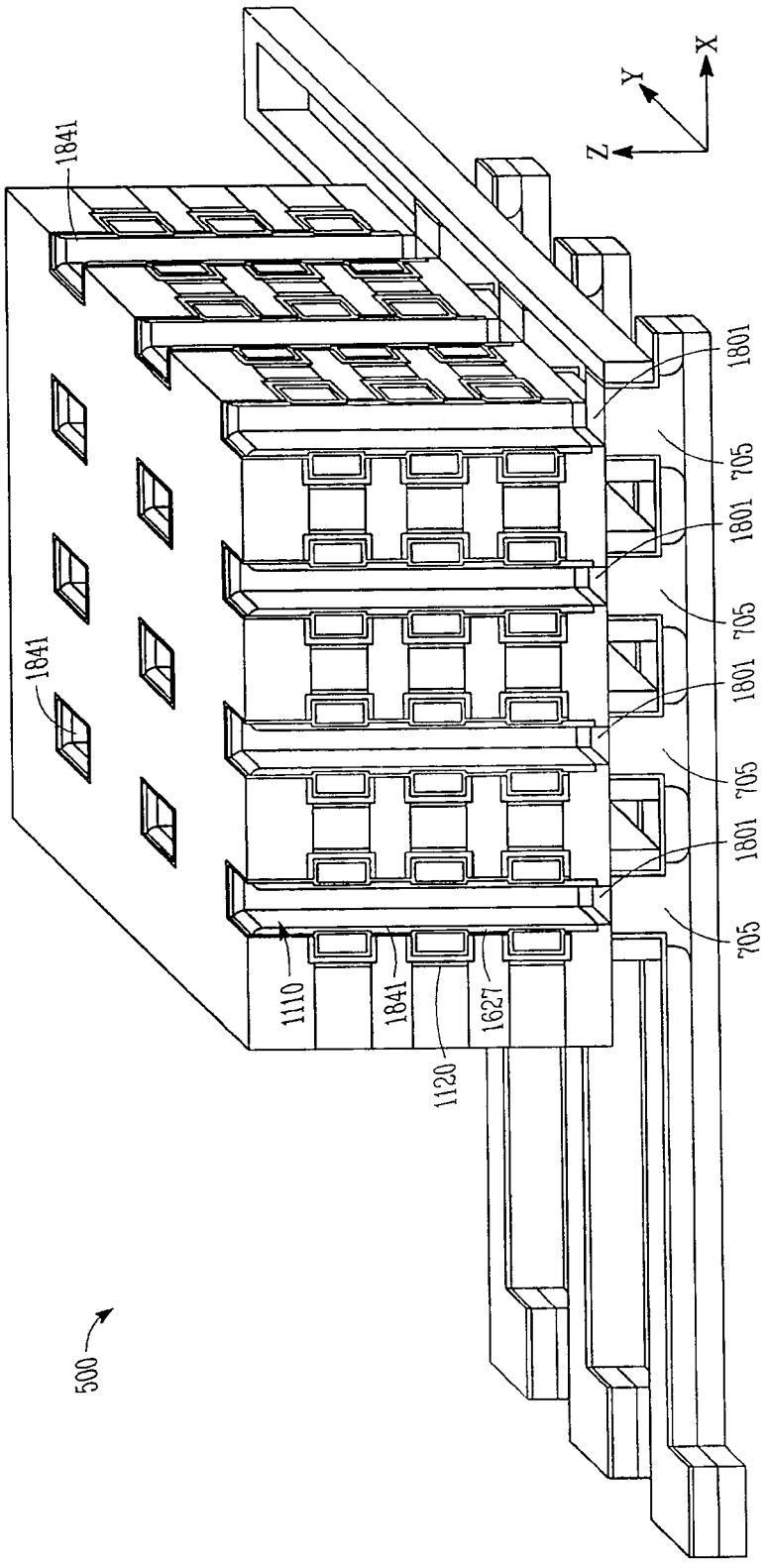

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FIG. 18

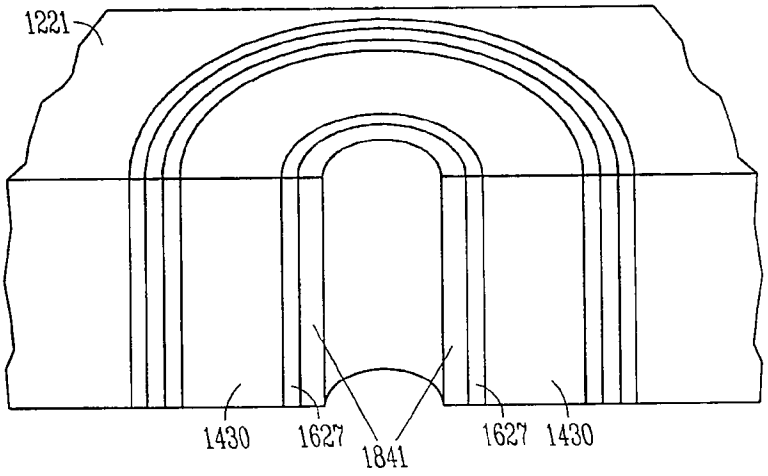


FIG. 19

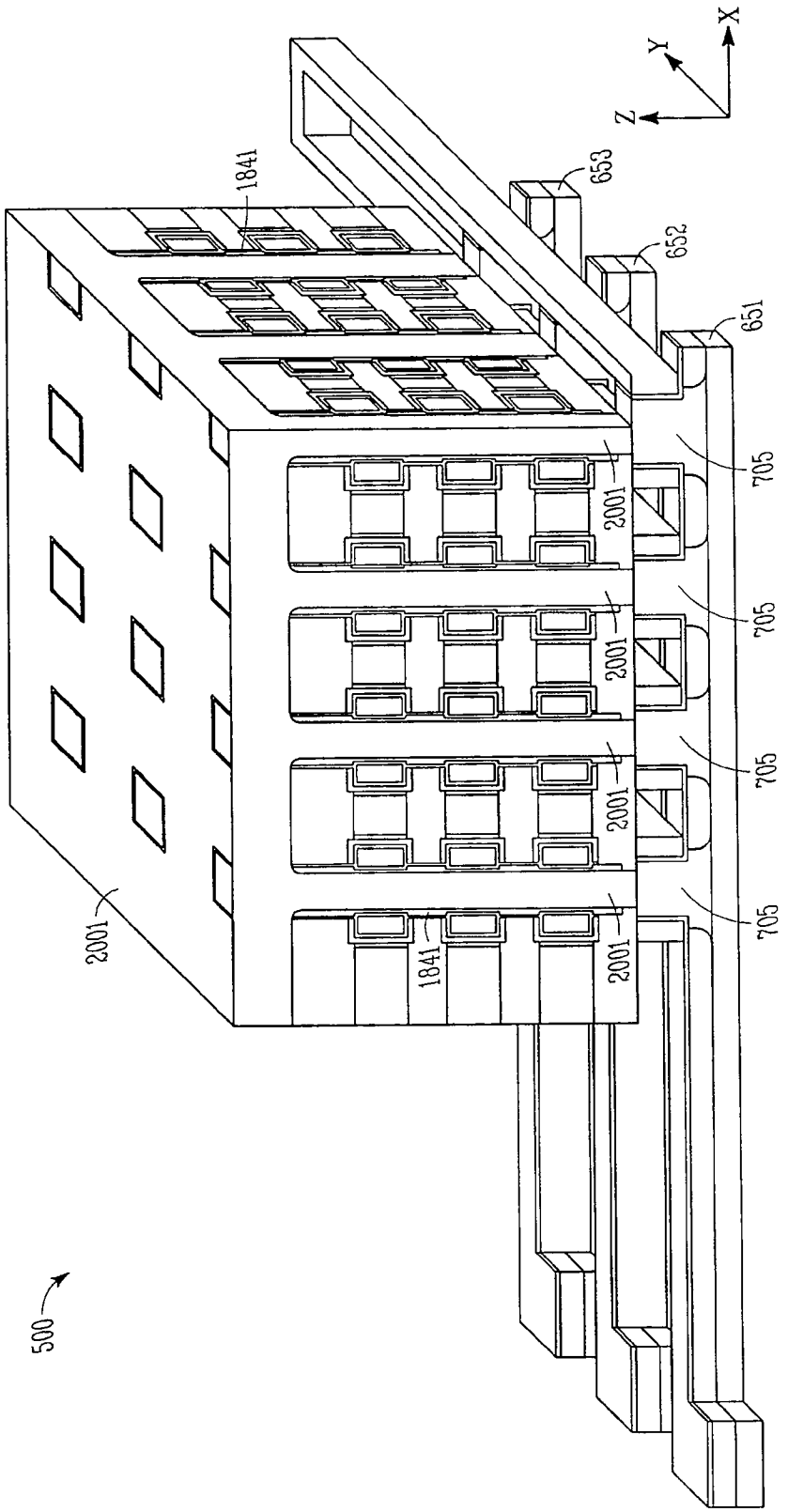


FIG. 20

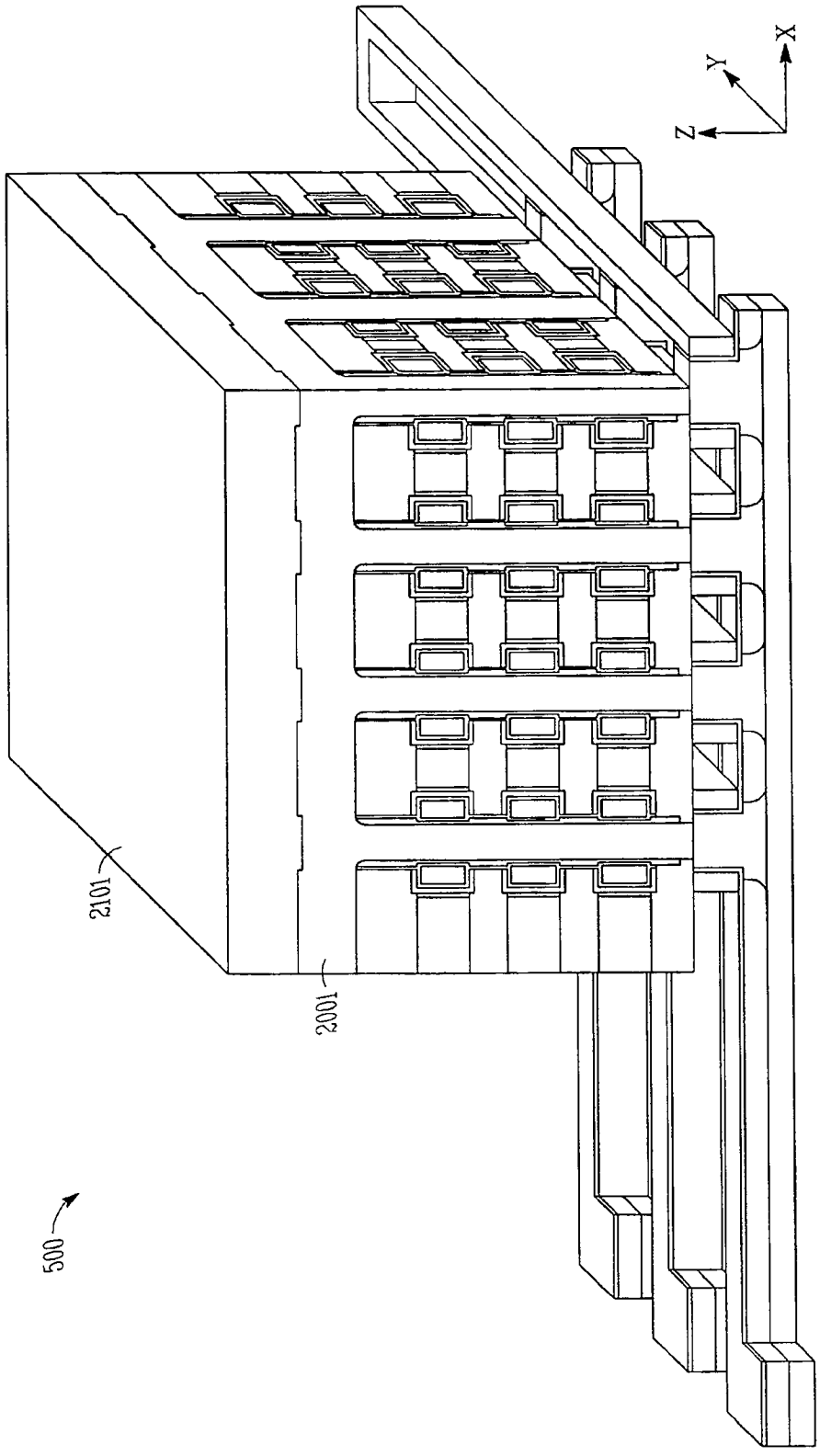


FIG. 21

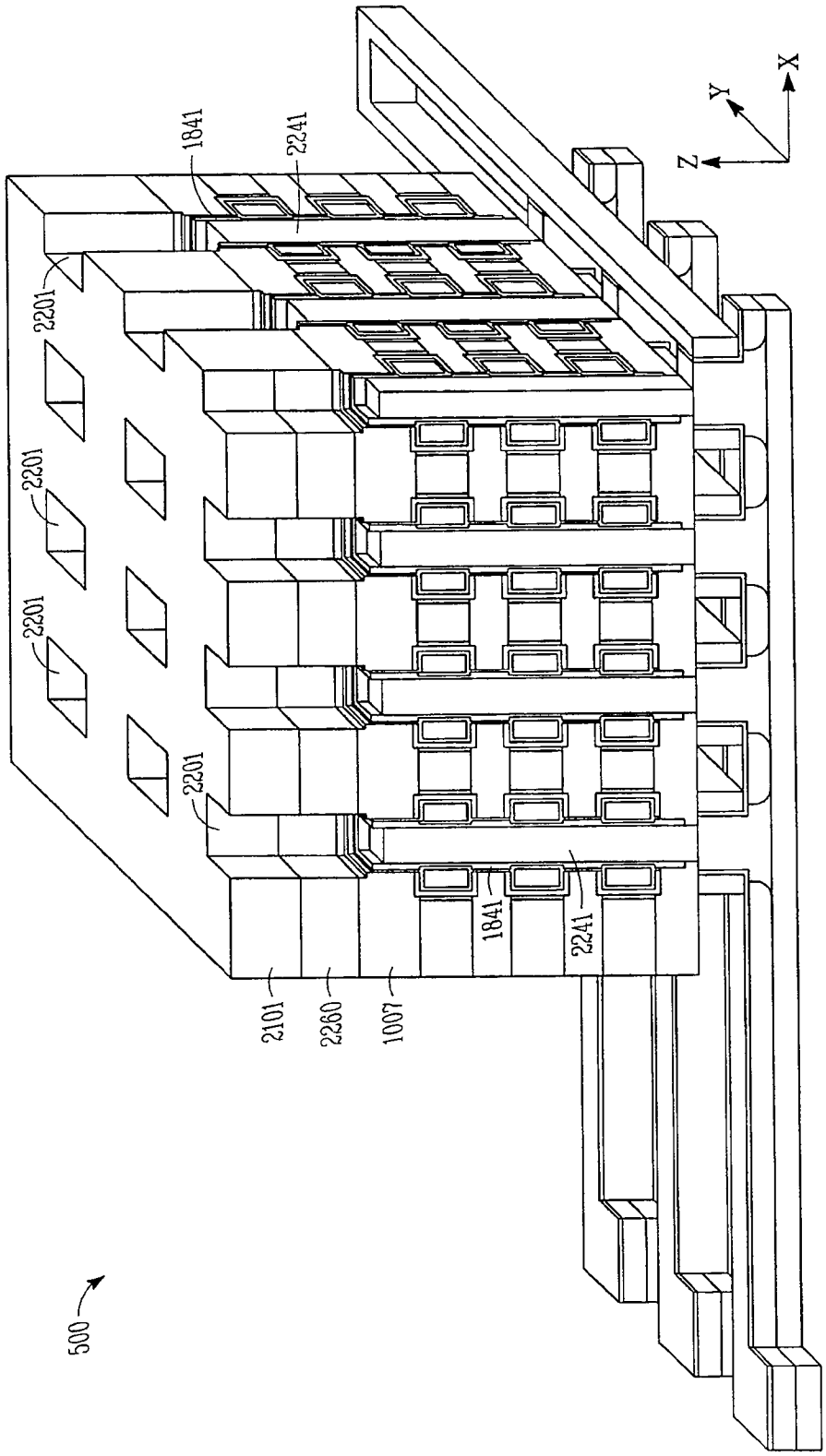

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FIG. 22

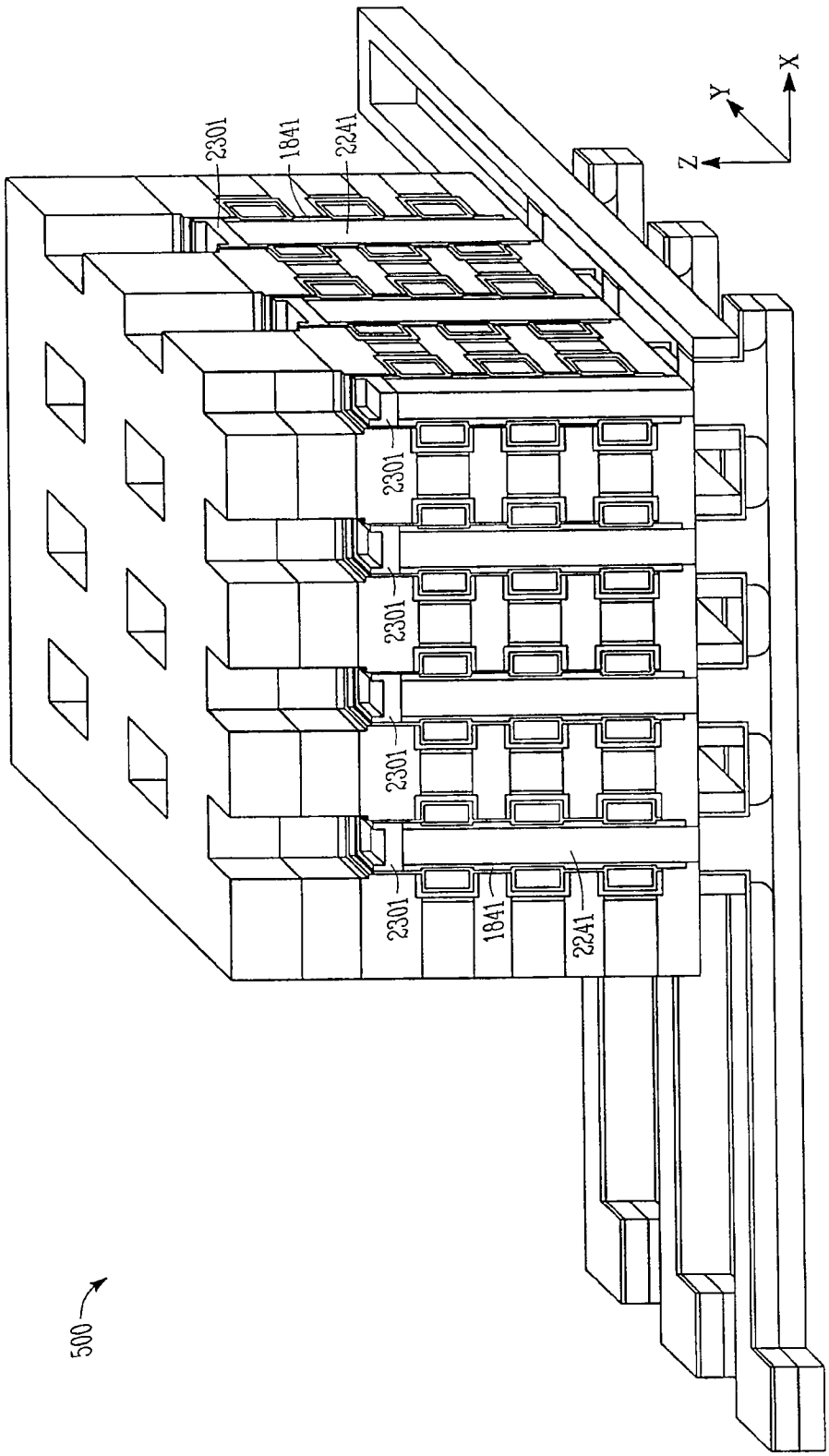


FIG. 23

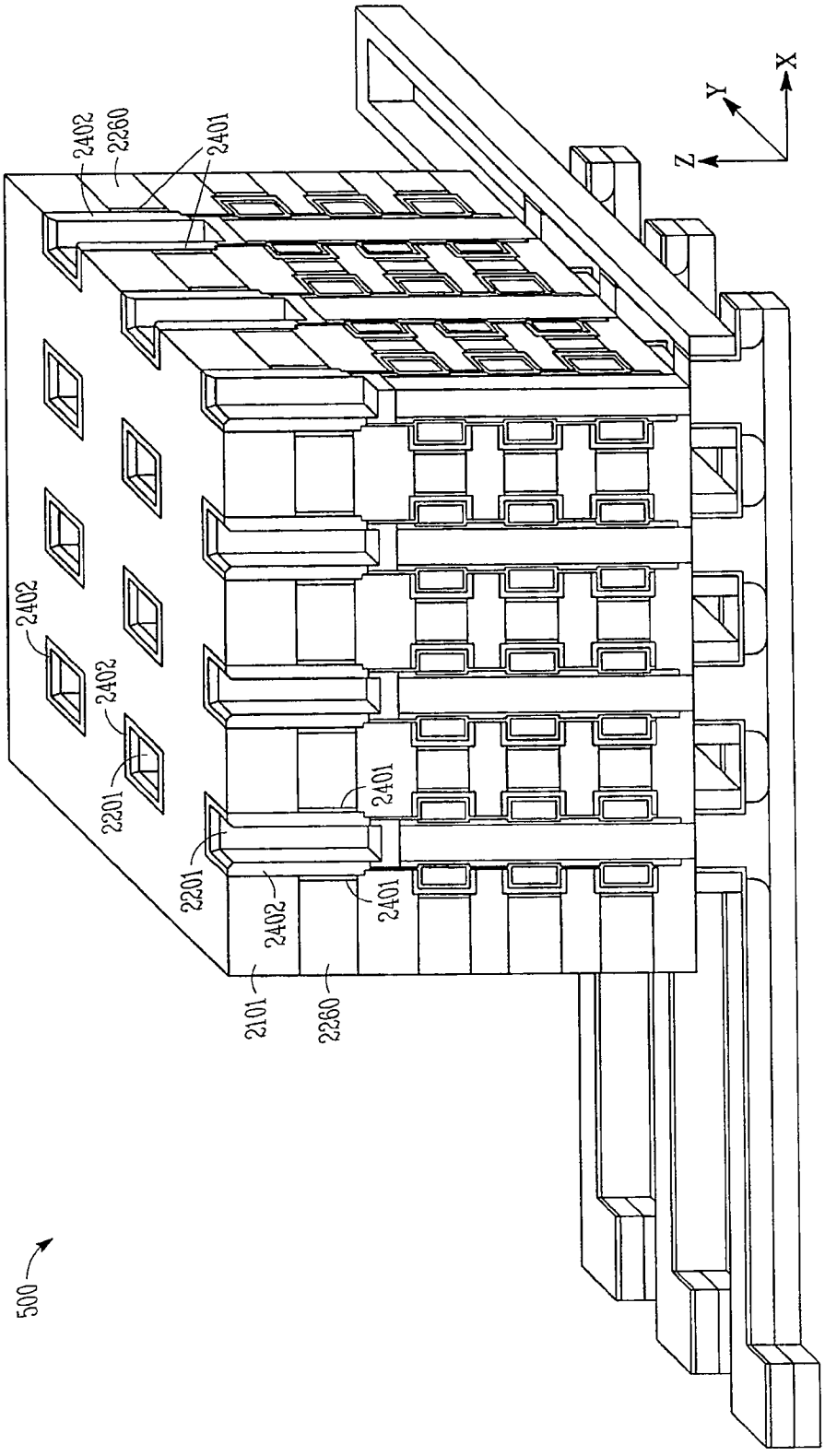

X
Y
Z
2402
2260
2401
2402
2402
2201
2401
2201
2402
2401
2101
2260
500

FIG. 24

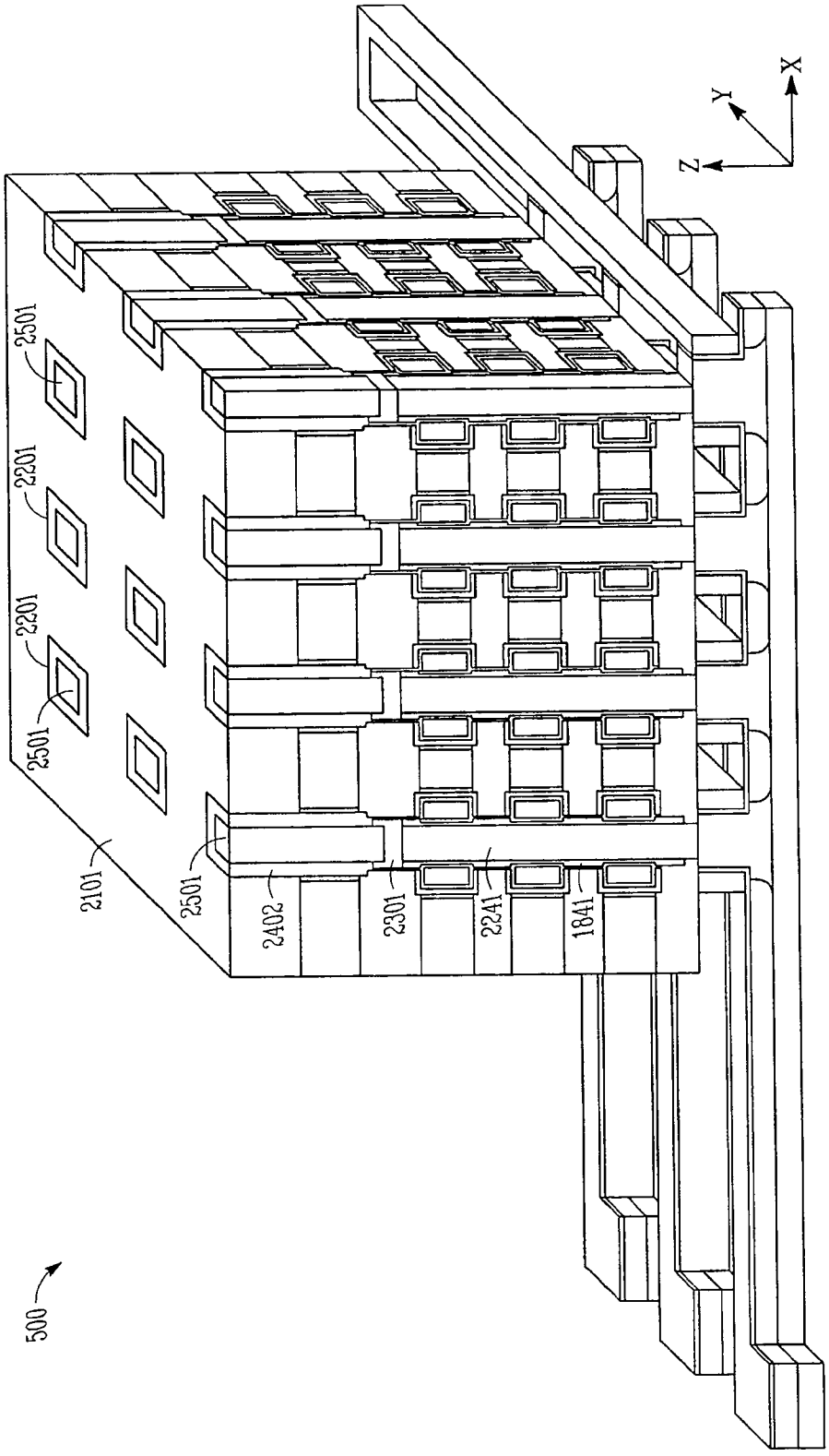


FIG. 25

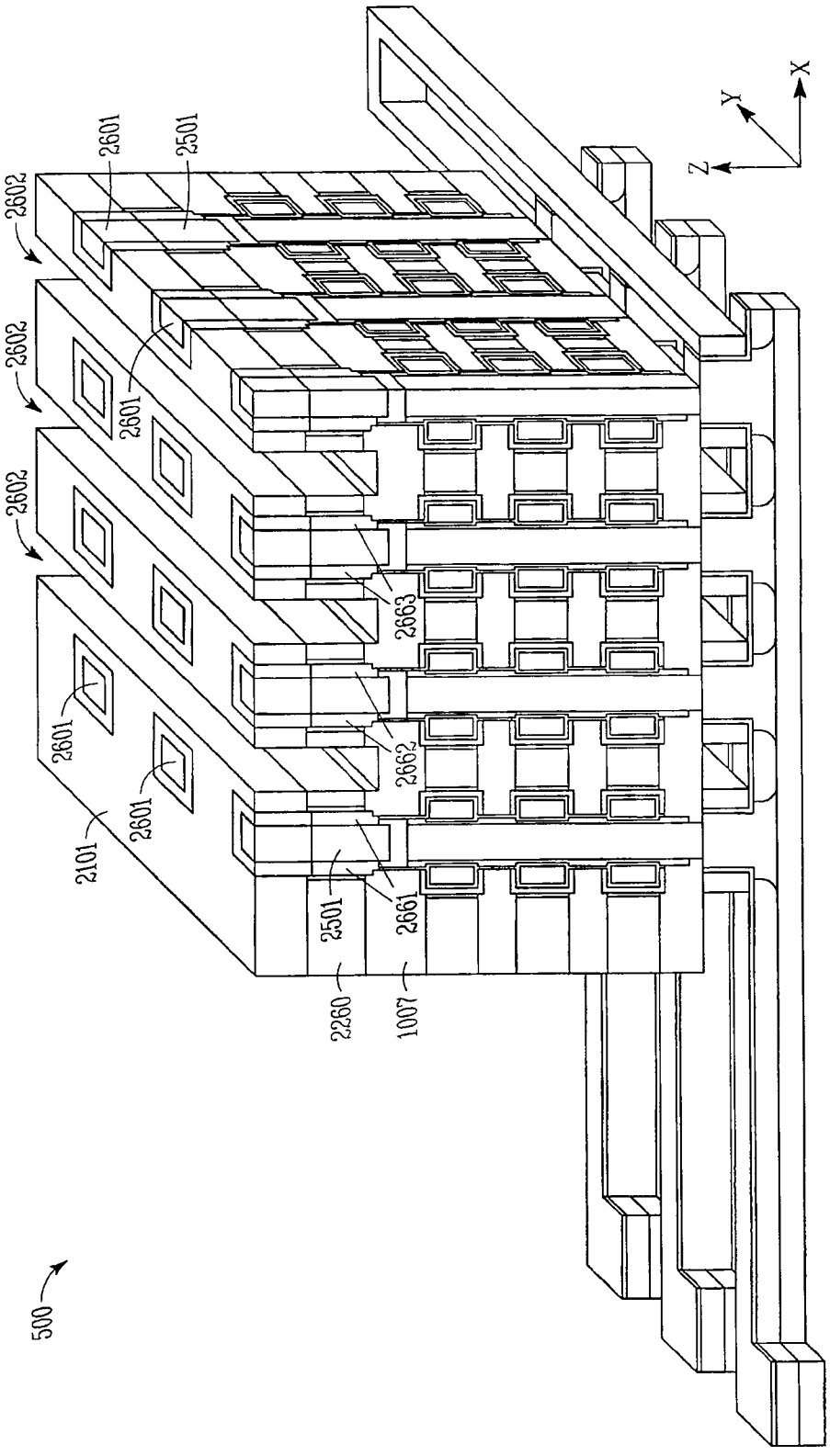

X
Y
Z
2602
2601
2501
2602
2601
2602
2663
2601
2662
2601
2101
2501
2661
2260
1007
500

FIG. 26

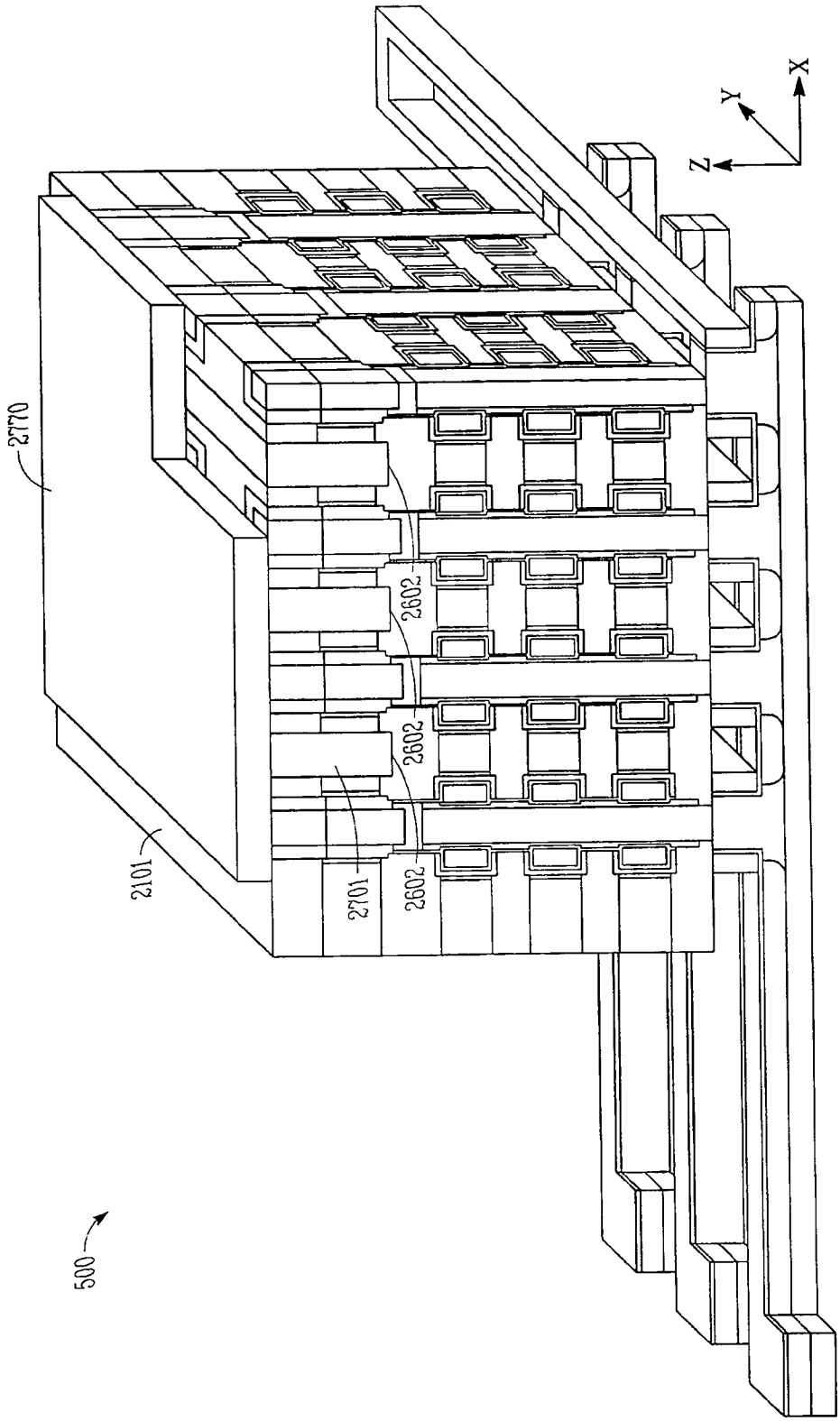


FIG. 27

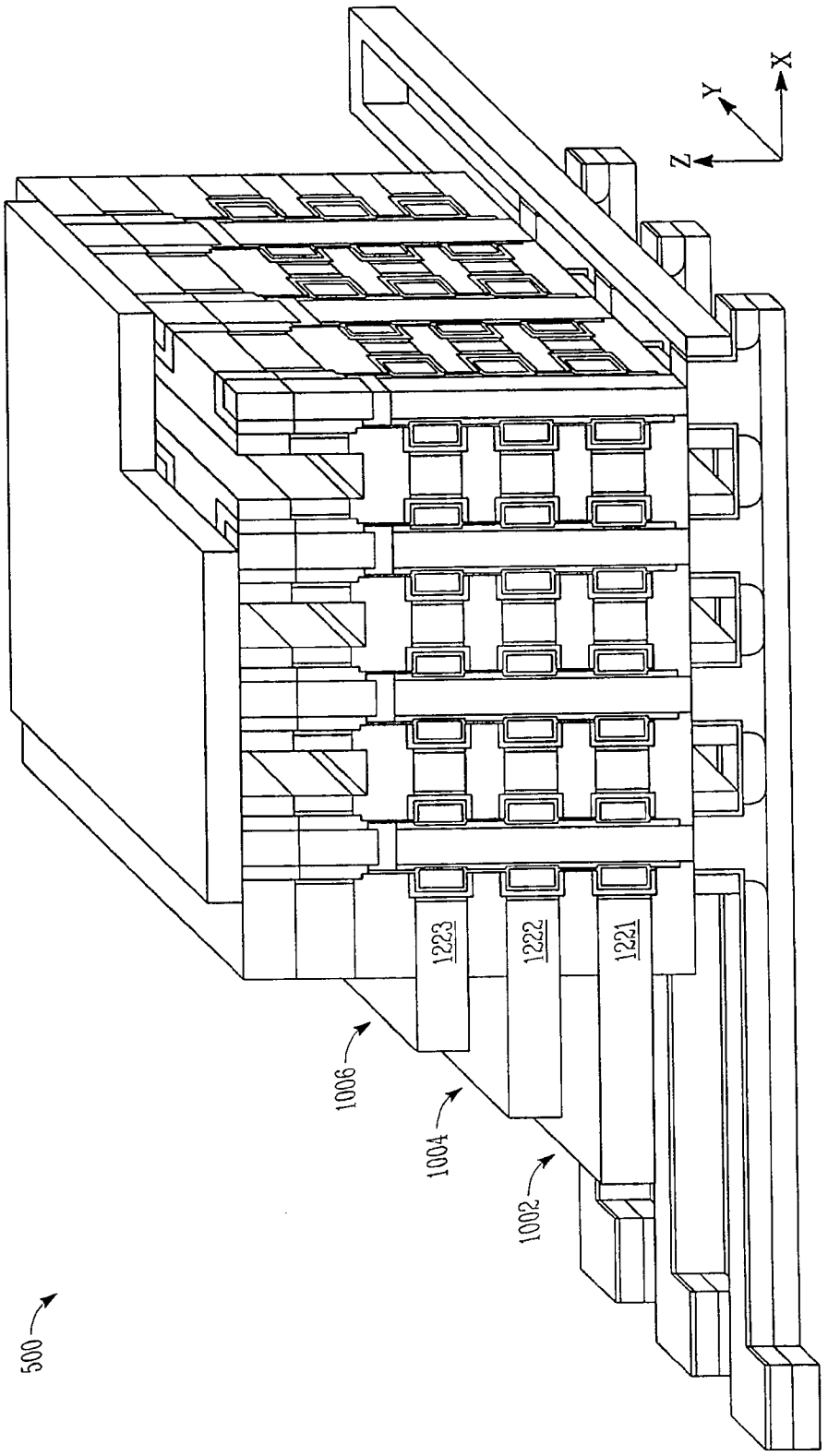


FIG. 28

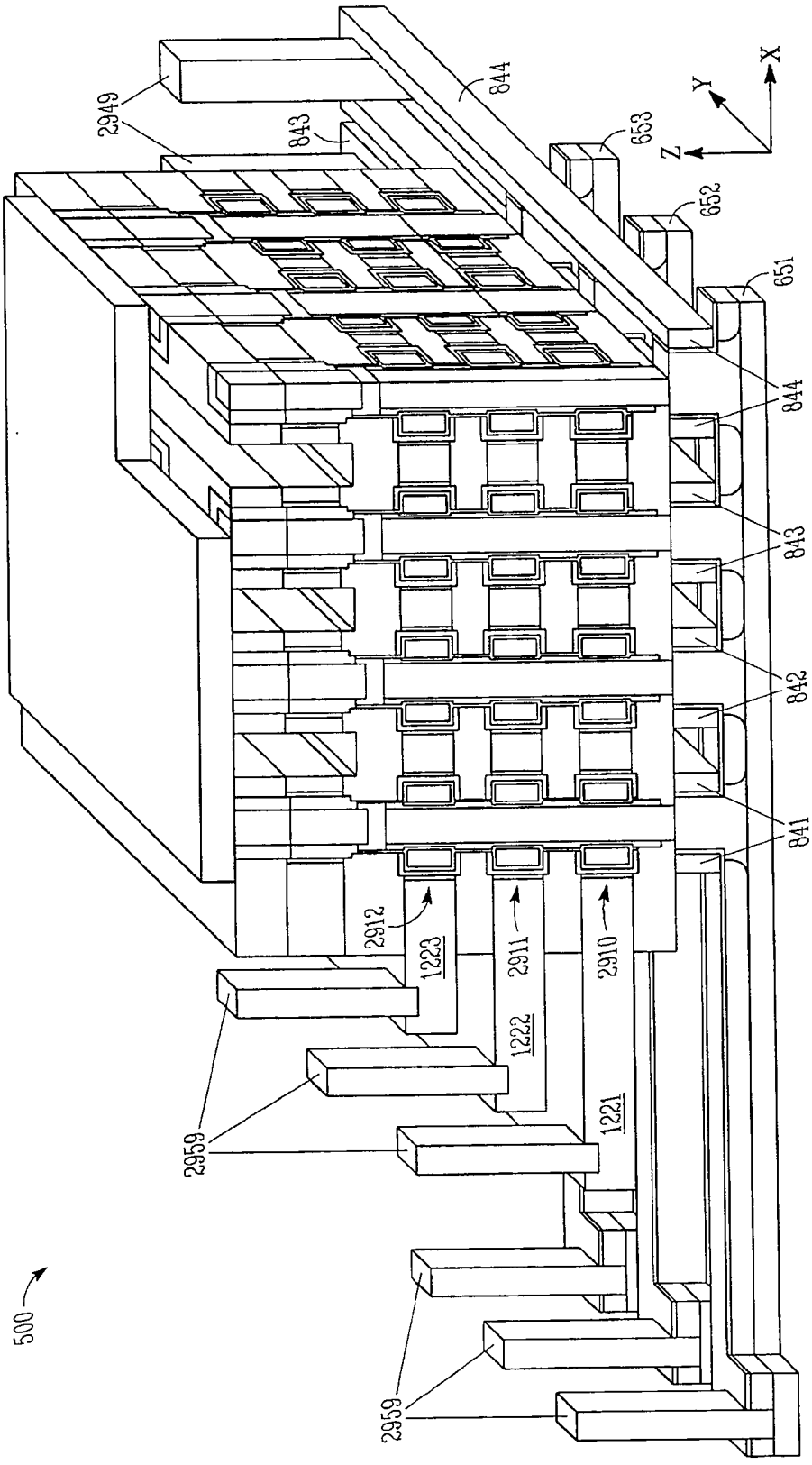

2949
843
844
653
Y
X
Z
652
651
844
843
842
841
2912
1223
2911
2910
1222
1221
2959
2959
500

FIG. 29

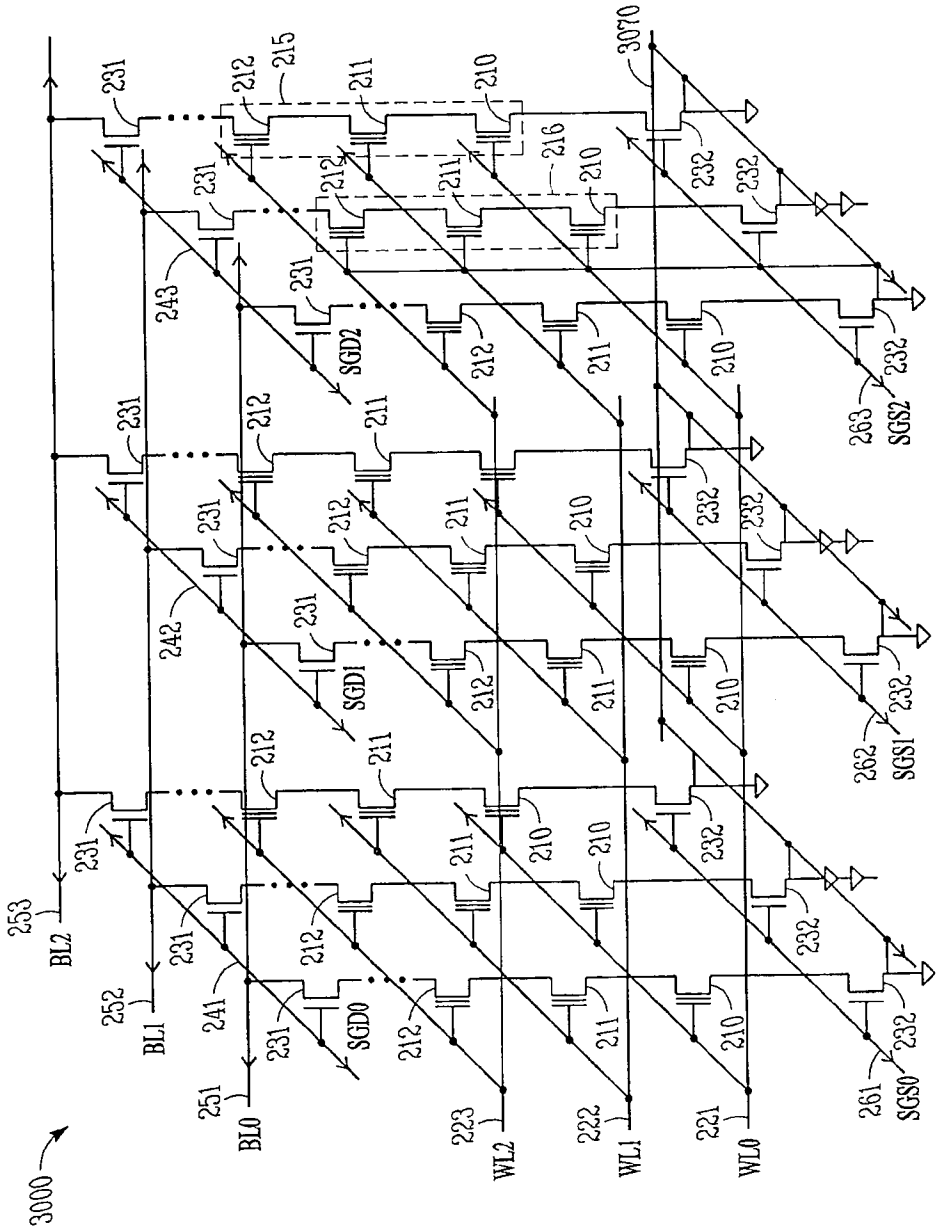

3000
3070
BL2
BL1
BL0
WL2
WL1
WL0
SGD2
SGD1
SGD0
SGS2
SGS1
SGS0
210
211
212
215
216
221
222
223
231
232
241
242
243
251
252
253
261
262
263

FIG. 30

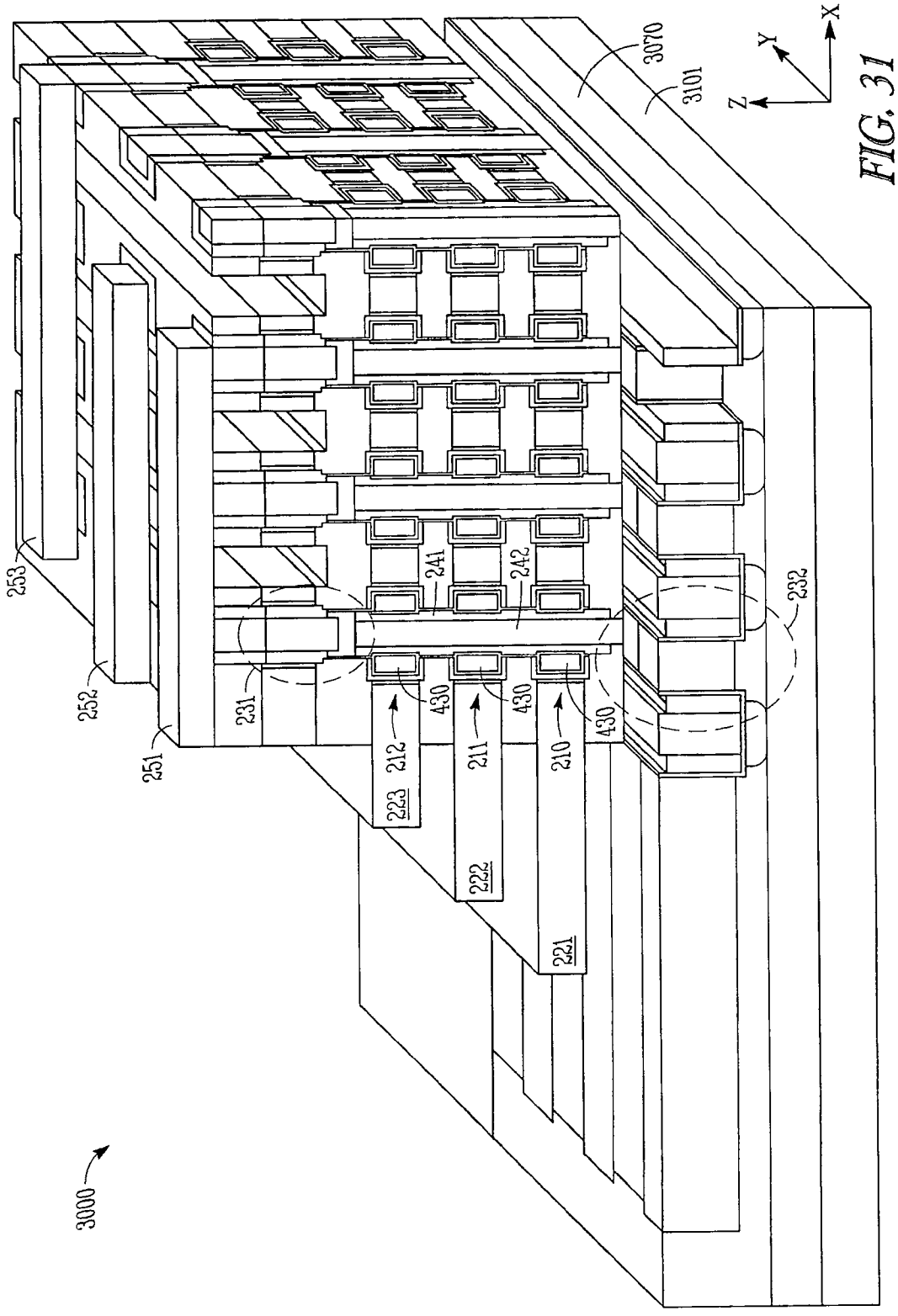

3070
3101
Z
Y
X
253
252
251
231
241
242
232
430
430
430
212
211
210
223
222
221
3000

FIG. 31

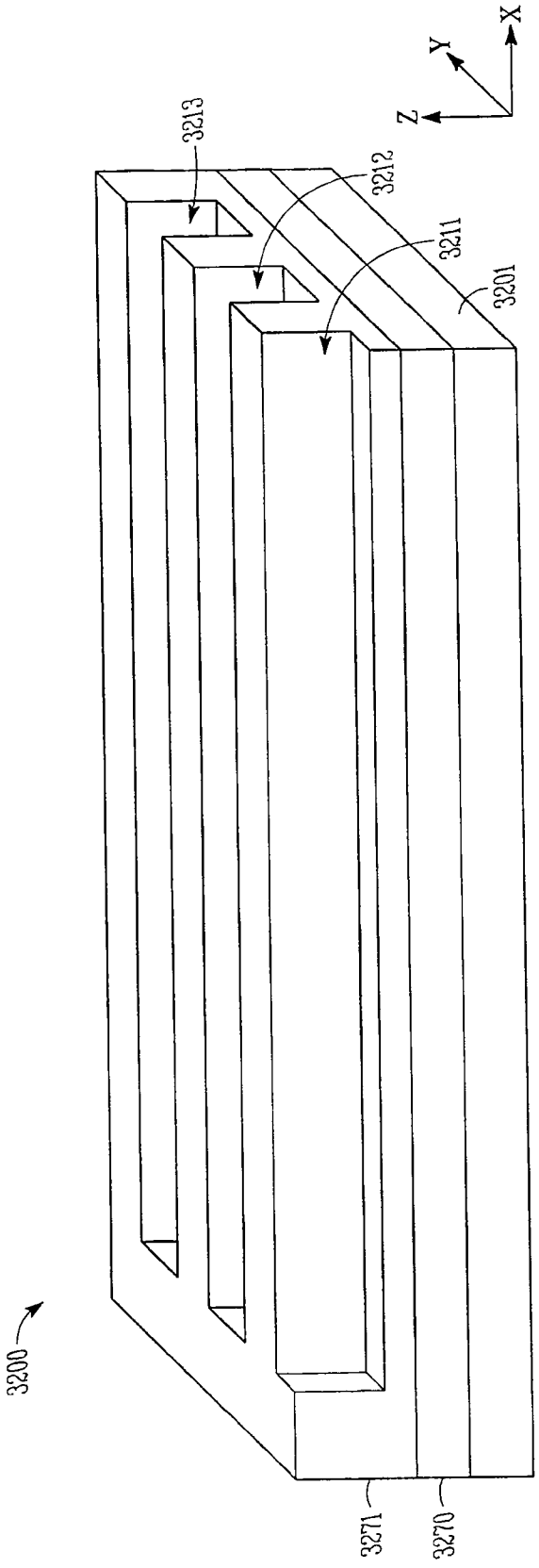


FIG. 32

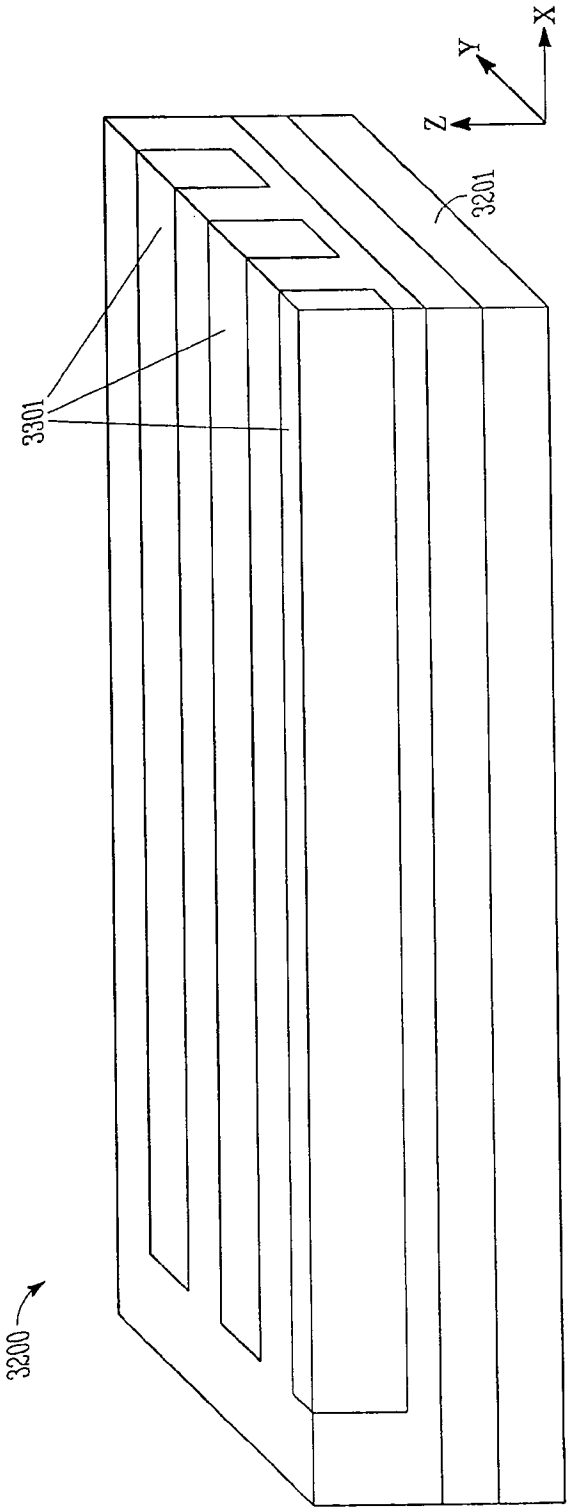


FIG. 33

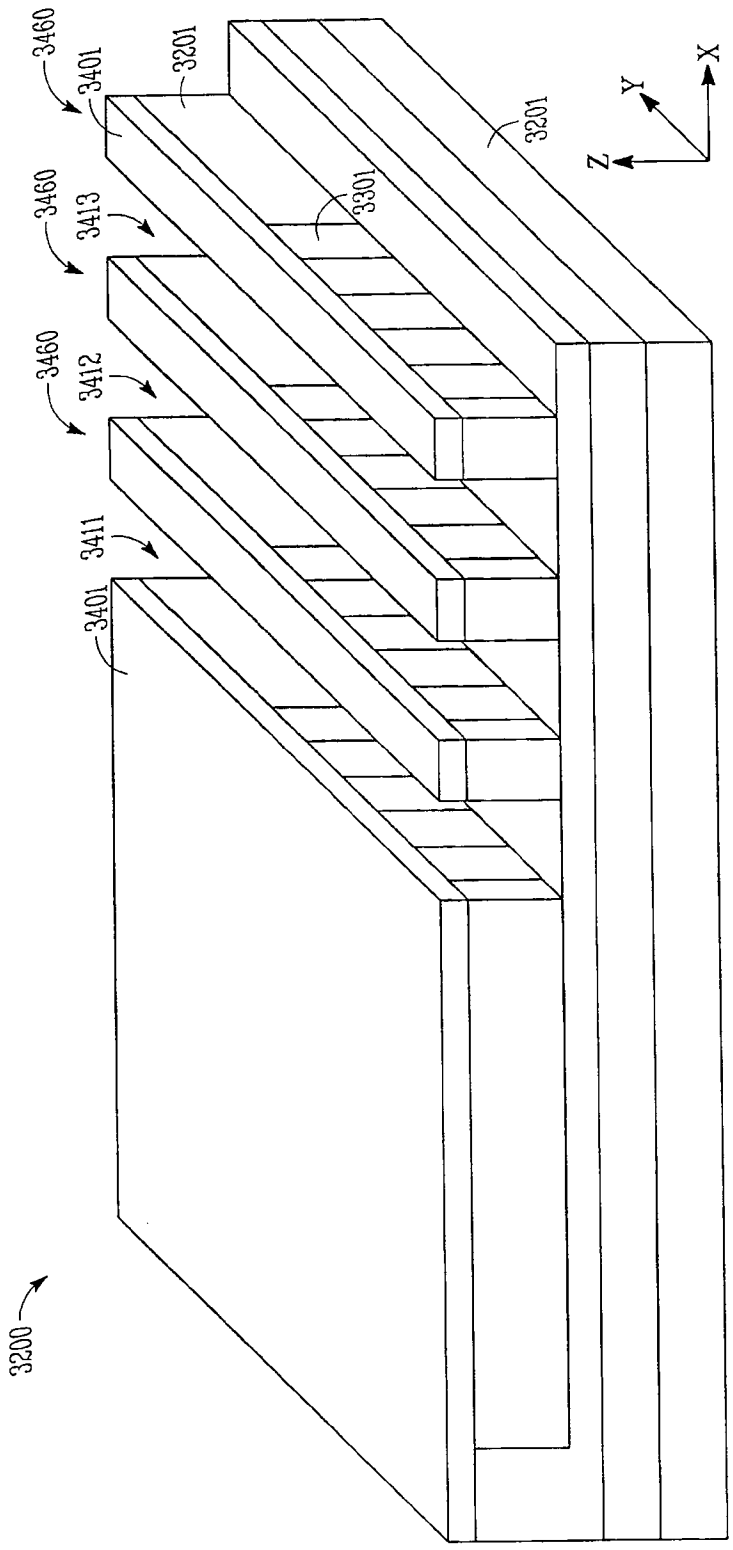

3460
3401
3201
3201
Y
X
Z
3460
3413
3301
3460
3412
3411
3401
3200

FIG. 34

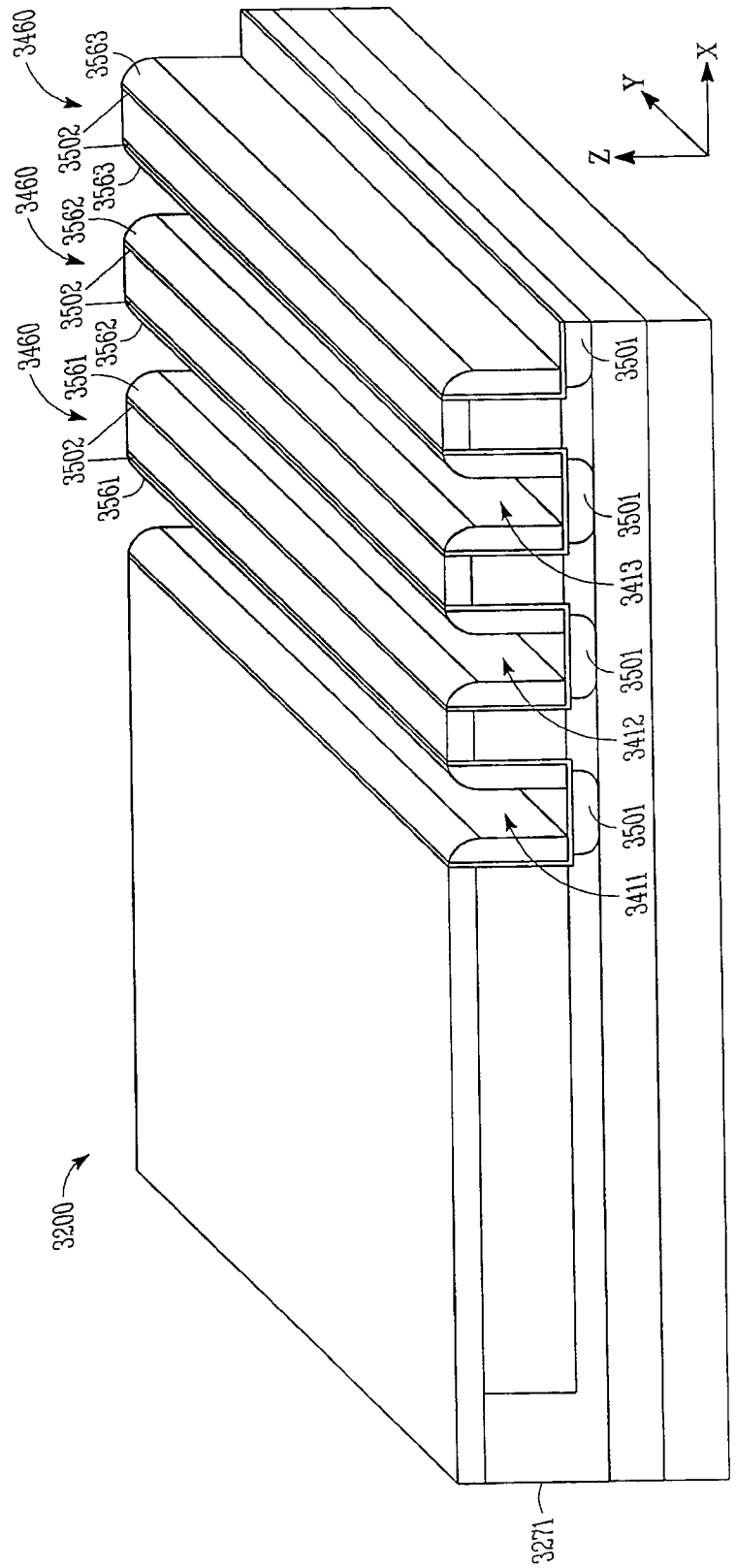

3460
3563
3502
3460
3562
3563
3502
3460
3562
3561
3502
3561
3501
3501
3413
3501
3412
3501
3411
3200
3271
Y
X
Z

FIG. 35

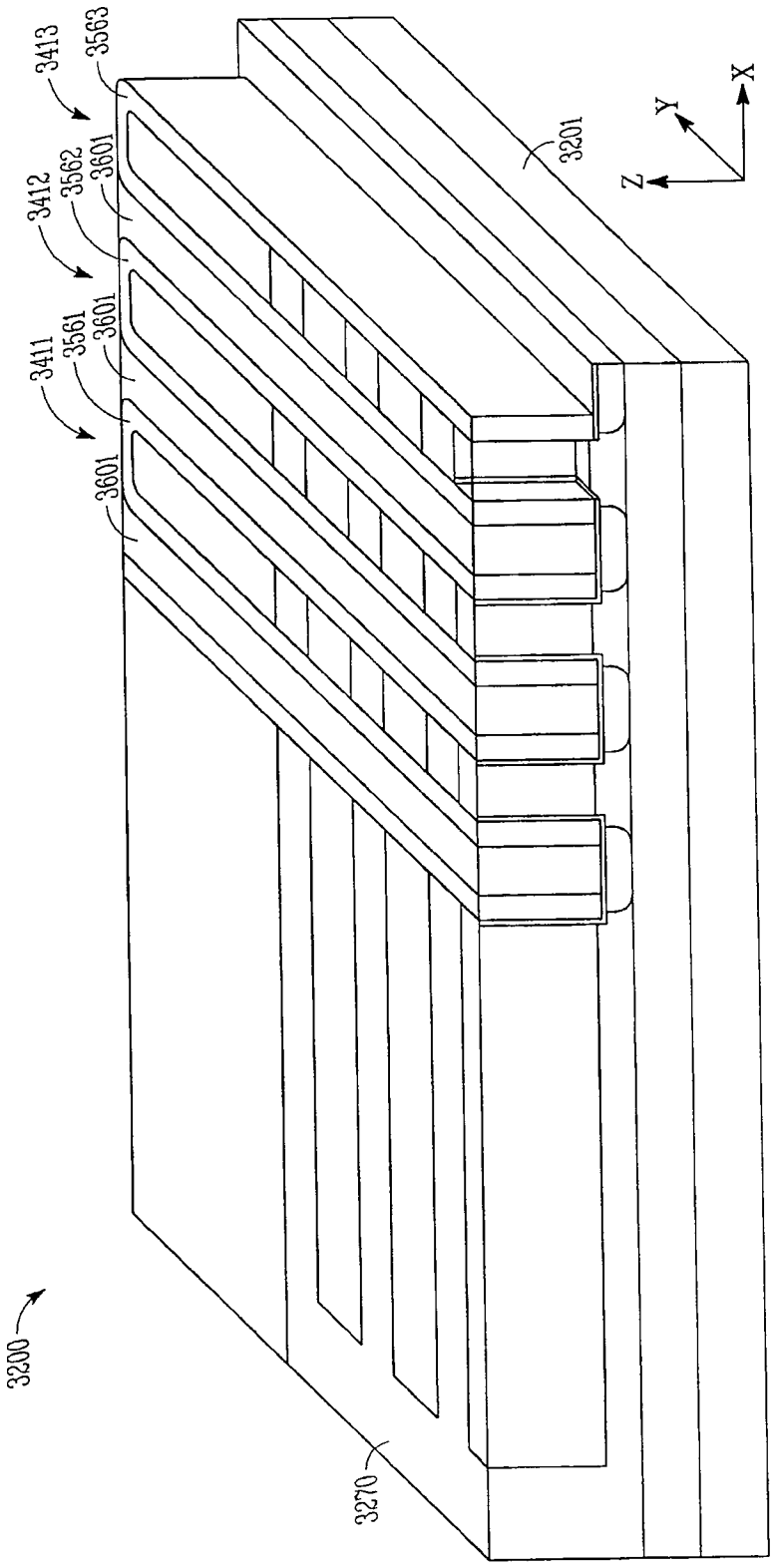

3413
3563
3412
3562
3601
3411
3561
3601
3601
3201
Y
X
Z
3200
3270

FIG. 36

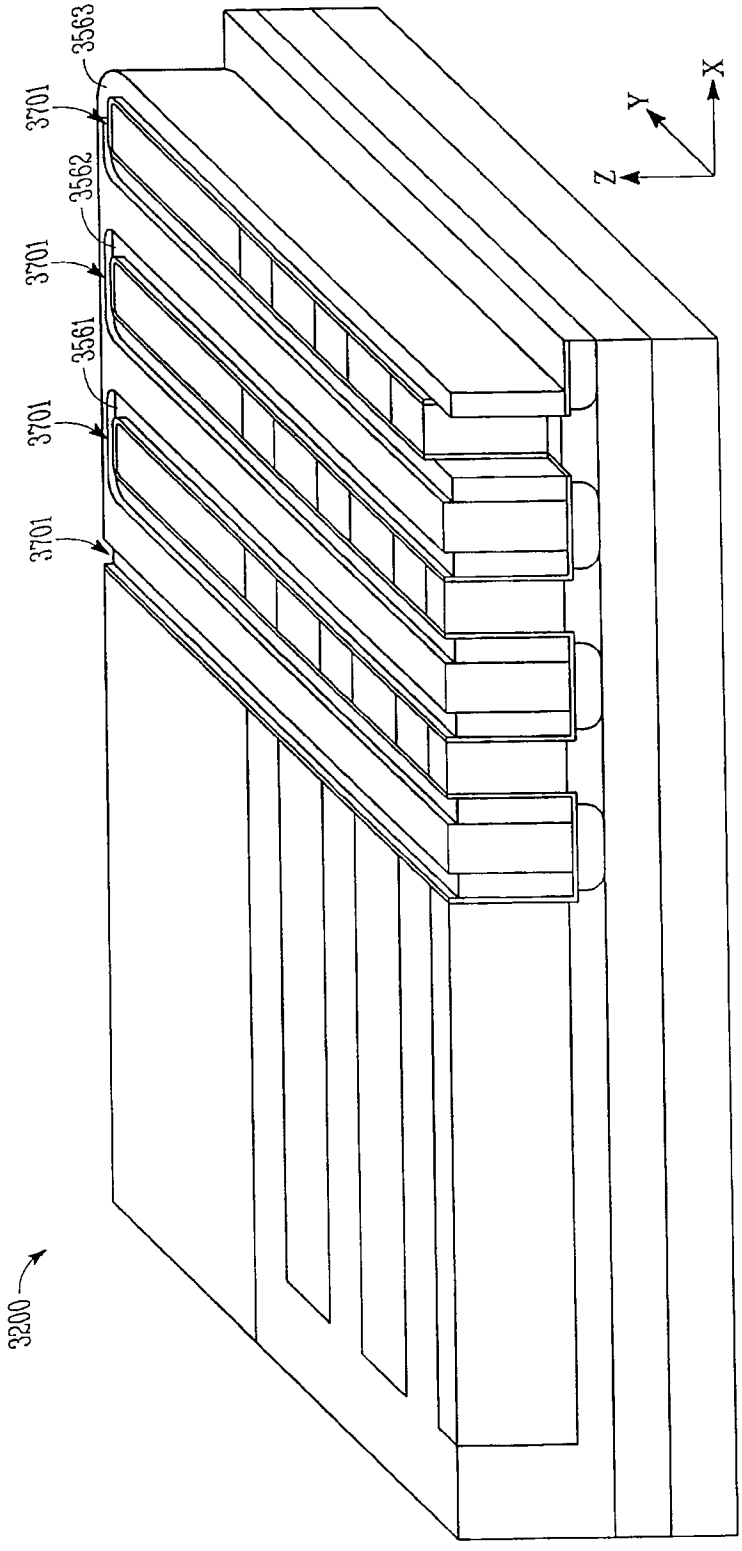


FIG. 37

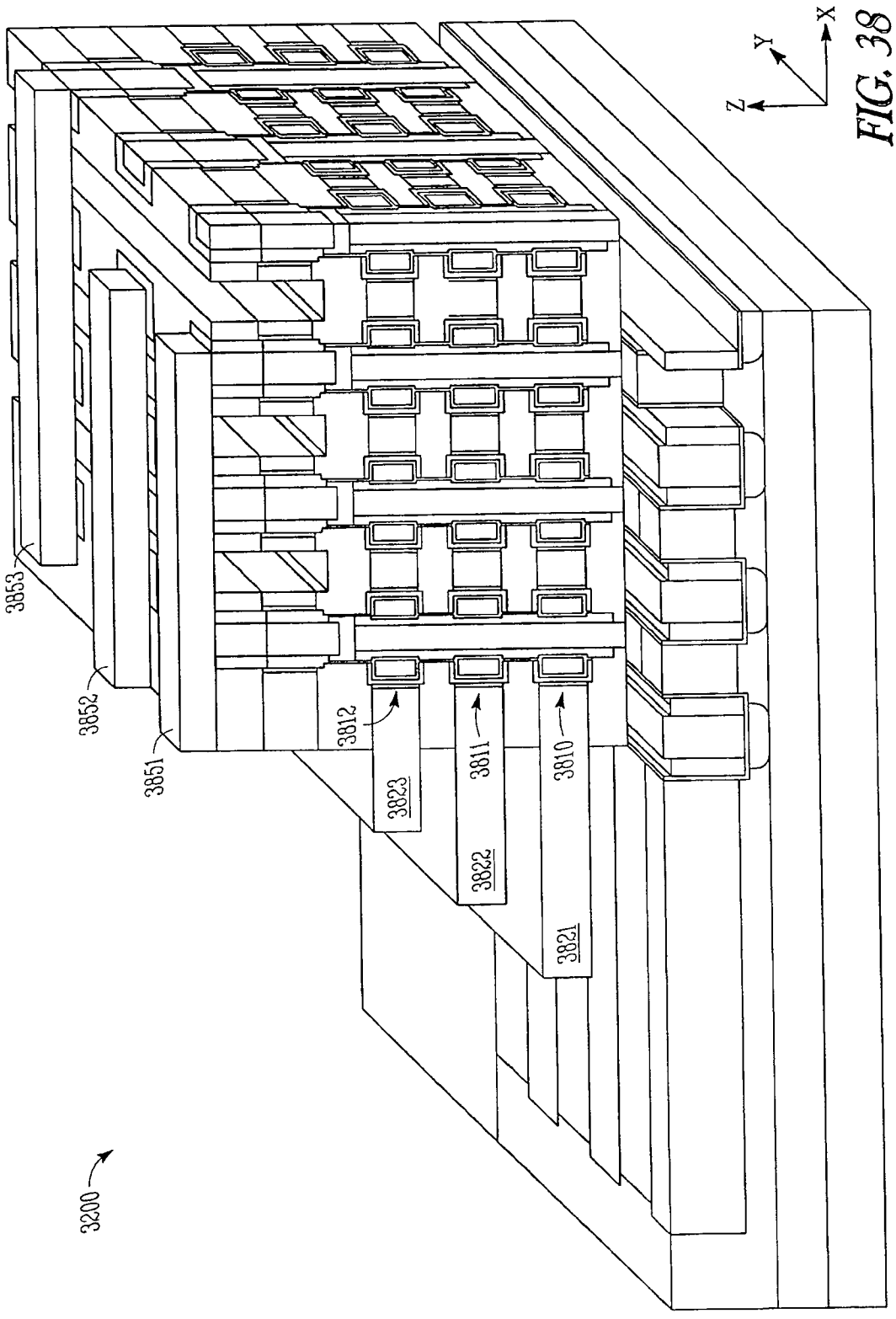


FIG. 38

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Filer:	David W. Black/Nicole Jack
Attorney Docket Number:	303.B12US1

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	14	52	728
Independent claims in excess of 3	1201	2	220	440
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2258**

Electronic Acknowledgement Receipt

EFS ID:	7909909
Application Number:	12825211
International Application Number:	
Confirmation Number:	1275
Title of Invention:	THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME
First Named Inventor/Applicant Name:	Sanh D. Tang
Customer Number:	73115
Filer:	David W. Black/Nicole Jack
Filer Authorized By:	David W. Black
Attorney Docket Number:	303.B12US1
Receipt Date:	28-JUN-2010
Filing Date:	
Time Stamp:	19:30:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$2258
RAM confirmation Number	7801
Deposit Account	190743
Authorized User	

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		303B12US1APPLICATION.pdf	2289169 c805889c05bfa28df6fae67ef754bce72f660925	yes	78

Multipart Description/PDF files in .zip description

Document Description	Start	End
Transmittal of New Application	1	1
Authorization to access Appl. by Trilateral Office	2	2
Oath or Declaration filed	3	5
Power of Attorney	6	10
Specification	11	32
Claims	33	39
Abstract	40	40
Drawings-only black and white line drawings	41	78

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Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	37938 f0e06b9716122d9f27e5e07e5b505ae9c65404fd	no	2

Warnings:

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New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT APPLICATION

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

INVENTORS

Sanh Tang
John Zahurak

Schwegman, Lundberg & Woessner, P.A.
1600 TCF Tower
121 South Eighth Street
Minneapolis, Minnesota 55402
ATTORNEY DOCKET 303.B12US1
MICRON 2009-0119.00/US

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

Background

[0001] Non-volatile memory devices such as flash memory devices are used in many computers and electronic devices to store information. A flash memory device usually has a write operation to store information (e.g., data and instruction codes), a read operation to retrieve the stored information, and an erase operation to clear information from the memory. As demand for higher density memory device increases, three-dimensional (3D) memory devices have been proposed. An example of a conventional 3D memory device is described by Jiyoung Kim et al. in an article titled "Novel 3-D Structure for Ultra High Density Flash Memory with Vertical-Array-Transistor (VRAT) and Planarized Integration on the same Plane (PIPE)", published in the 2008 Symposium on VLSI Technology Digest of Technical Papers, pages 22-23. Since 3D memory devices are relatively new, manufacturing these devices can pose fabrication process challenges.

Brief Description of the Drawings

[0002] FIG. 1 shows a block diagram of a memory device having a memory array with memory cells, according to an embodiment of the invention.

[0003] FIG. 2 shows a schematic diagram of a portion of a memory device having data lines located below memory cells, according to an embodiment of the invention.

[0004] FIG. 3 shows a three-dimensional view of a portion of the memory device of FIG. 2, according to an embodiment of the invention.

[0005] FIG. 4 shows a portion of a control gate and a memory cell of the memory device of FIG. 3, according to an embodiment of the invention.

[0006] FIG. 5 through FIG. 29 show various processes of forming a memory device having data lines located below memory cells, according to an embodiment of the invention.

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[0007] FIG. 30 shows a schematic diagram of a portion of a memory device having data lines located above memory cells, according to an embodiment of the invention.

[0008] FIG. 31 shows a three-dimensional view of a portion of the memory device of FIG. 30, according to an embodiment of the invention.

[0009] FIG. 32 through FIG. 38 show various processes of forming a memory device with data lines located above memory cells, according to an embodiment of the invention.

Detailed Description

[0010] FIG. 1 shows a block diagram of a memory device 100 having a memory array 102 with memory cells 110 according to an embodiment of the invention. Memory cells 110 can be arranged in rows and columns along with access lines 123 (e.g., wordlines having signals WL0 through WLM) and lines 124 (e.g., bit lines having signals BL0 through BLN). Memory device 100 uses lines 124 and 128 to transfer information within memory cells 110. Memory cells 110 can be physically located in multiple device levels such that one group of memory cells 110 can be stacked on one or more groups of other memory cells 110. Row decoder 132 and column decoder 134 decode address signals A0 through AX on lines 125 (e.g., address lines) to determine which memory cells 110 are to be accessed. Row and column level decoders 136 and 138 of row and column decoders 132 and 134, respectively, determine which of the multiple device levels of memory device 100 that the memory cells 110 to be accessed are located.

[0011] A sense amplifier circuit 140 operates to determine the value of information read from memory cells 110 and provide the information in the form of signals to lines 124 and 128. Sense amplifier circuit 140 can also use the signals on lines 124 and 128 to determine the value of information to be written to memory cells 110. Memory device 100 can include circuitry 150 to transfer information between memory array 102 and lines (e.g., data lines) 126. Signals DQ0 through DQN on lines 126 can represent information read from or written into memory cells

110. Lines 126 can include nodes within memory device 100 or nodes (e.g., pins or solder balls) on a package where memory device 100 resides. Other devices external to memory device 100 (e.g., a memory controller or a processor) may communicate with memory device 100 through lines 125, 126, and 127.

[0012] Memory device 100 performs memory operations such as a read operation to read information from memory cells 110 and a write operation (sometime referred to as a programming operation) to store information into memory cells 110. A memory control unit 118 controls the memory operations based on control signals on lines 127. Examples of the control signals on lines 127 include one or more clock signals and other signals to indicate which operation, (e.g., a write or read operation) that memory device 100 performs. Other devices external to memory device 100 (e.g., a processor or a memory controller) may control the values of the control signals on lines 127. Specific values of a combination of the signals on these lines can produce a command (e.g., a write or read command) that causes memory device 100 to perform a corresponding memory operation (e.g., a write or read operation).

[0013] Each of memory cells 110 can store information representing a value of a single bit or a value of multiple bits such as two, three, four, or other numbers of bits. For example, each of memory cells 110 can store information representing a binary value "0" or "1" of a single bit. In another example, each of memory cells 110 can store information representing a value of multiple bits, such as one of four possible values "00", "01", "10", and "11" of two bits, one of eight possible values "000", "001", "010", "011", "100", "101", "110" and "111, or one of other values of other number of multiple bits.

[0014] Memory device 100 can receive a supply voltage, including supply voltage signals Vcc and Vss, on lines 141 and 142, respectively. Supply voltage signal Vss may operate at a ground potential (e.g., having a value of approximately zero volts). Supply voltage signal Vcc may include an external voltage supplied to memory device 100 from an external power source such as a battery or an alternating-current to direct-current (AC-DC) converter circuitry.

[0015] Circuitry 150 of memory device 100 can include a select circuit 152 and an input/output (I/O) circuit 116. Select circuit 152 responds to signals SEL0 through SELn to select the signals on lines 124 and 128 that can represent the information read from or written into memory cells 110. Column decoder 134 selectively activates the SEL0 through SELn signals based on address signals A0 through AX. Select circuit 152 selects the signals on lines 124 and 128 to provide communication between memory array 102 and I/O circuit 116 during read and write operations.

[0016] Memory device 100 can be a non-volatile memory device and memory cells 110 can be non-volatile memory cells such that memory cells 110 can retain information stored thereon when power (e.g., Vcc or Vss, or both) is disconnected from memory device 100. For example, memory device 100 can be a flash memory device such as a NAND flash or a NOR flash memory device, or other kinds of memory devices, such as a variable resistance memory device (e.g., phase change random-access-memory (PCRAM), resistive RAM (RRAM), etc.).

[0017] One skilled in the art may recognize that memory device 100 may include other features that are not shown in FIG. 1, to help focus on the embodiments described herein.

[0018] Memory device 100 may include at least one of the memory devices and memory cells described below with reference to FIG. 2 through FIG. 38.

[0019] FIG. 2 shows a schematic diagram of a portion of a memory device 200 having data lines 251, 252, and 253 located below memory cells 210, 211, and 212, according to an embodiment of the invention. Memory cells 210, 211, and 212 can be grouped into groups, such as a group of memory cells 210, a group of memory cells 211, and a group of memory cells 212. As shown in FIG. 2, the memory cells in each group share the same control gate, such as control gate 221, 222, or 223 (with associated signals WL0, WL1, and WL2). The memory cells are coupled in series as strings, such as strings 215 and 216. Each string can include one of the memory cells from different groups and is coupled between one of transistors 231 and one of transistors 232.

[0020] As shown in FIG. 2, transistors 231 have gates coupled to select lines 241, 242, and 243 (with associated signals SGD0, SGD1, and SGD2). Transistors 231 have nodes (e.g., sources) coupled to data lines 251, 252, and 253 (with associated signals BL0, BL1, and BL2). Data lines 251, 252, and 253 sometimes correspond to bit lines or sense lines of a non-volatile memory device.

[0021] Transistors 232 have gates coupled to select lines 261, 262, and 263 (with associated signals SGS0, SGS1, and SGS2). Transistors 232 have nodes (e.g., drains) coupled to a common source 270 of memory cell strings in a non-volatile memory device.

[0022] FIG. 2 shows three groups of memory cells with associated components coupled to them, as an example. The number of groups of memory cells and their associated components (e.g., control gates and data lines) can vary.

[0023] Memory device 200 uses control gates 221, 221, and 223 to control access to memory cells 210, 211, and 212 during a read operation to sense (e.g., read) information stored in memory cells 210, 211, and 212, and during a write operation to store information into memory cells 210, 211, and 212. Memory device 200 uses data lines 251, 252, and 253 to transfer the information read from these memory cells during a read operation.

[0024] Transistors 231 and 232 are responsive to signals SGD0, SGD1, and SGD2, and signals SGS0, GS1, and SGS2, respectively, to selectively couple the memory cells to data lines 251, 252, and 253 and common source 270 during a read or write operation.

[0025] To help focus on the description herein, the description herein omits detailed description of operations of memory device, such as write, read, and erase operation. One skill in the art would recognize these operations. For example, in an erase operation of memory device 200, a voltage of approximately 20 volts can be applied to data lines 251, 252, and 253 while control gates 221, 221, and 223, select lines 241, 242, and 243, and select lines 261, 262, and 263 can be "floated" (e.g., leave unconnected to a voltage). In this erase operation, electrons from memory

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elements of memory cells 210, 211, and 212 may move to data lines 251, 253, and 253.

[0026] FIG. 3 shows a 3D view of a portion of memory device 200, according to an embodiment of the invention. FIG. 3 also shows X, Y, and Z directions, and device levels 301, 302, and 303 arranged in the Z-direction. Memory cells 210 of the same group can be arranged in rows and columns in the X-direction and Y-direction. Each group of memory cells is located in different device levels 301, 302, or 303. For example, the group having memory cells 210 is located in device level 301. The group having memory cells 211 is located in device level 302. The group having memory cells 212 is located in device level 303.

[0027] As shown in FIG. 3, memory cells 210, 211, and 212 in each string (e.g., memory cells between transistors 231 and 232) are substantially vertically aligned in the Z-direction with respect to a substrate underneath data lines 251, 252, and 253. The substrate is not shown in FIG. 3, but can be similar to substrate 503 of FIG. 5 and FIG. 6. FIG. 3 also shows a channel 241 and a conductive material portion 242 extending vertically in the Z-direction and through memory element 430 of memory cells 210, 211, and 212 in the same string between transistors 231 and 232, which corresponds to transistors 231 and 232 of FIG. 2. As shown in FIG. 3, transistor 231 can include a double-gate coupled to a body 391 (e.g., transistor channel) to control (turn on or off) the transistor. The structure of the double-gate can include two segments of the same select line 241 (as shown in FIG. 3), such that the two segments are located on only two respective sides of body 391.

[0028] Memory device 200 in FIG. 3 also can include contacts 329, 349, and 359. Contacts 329 provide electrical connections to control gates 221, 222, and 223. Contacts 349 provide electrical connections to select lines 241, 242, 243, and 244. Contacts 359 provide electrical connections to and from data lines 251, 252, and 253. Select line 244 and the memory cell associated with it in the Z-direction are not shown in FIG. 2.

[0029] FIG. 4 shows a portion of control gate 221 and a memory cell 210 of memory device 200 of FIG. 3. Control gates 222 and 223 and memory cells 211

and 212 of FIG. 2 have structures similar to control gate 221 and memory cell 210, respectively. As shown in FIG. 4, control gate 221 can include a homogenous material with cavities 420, each cavity being filed with various components, including materials different from the homogenous material. The various components include: a memory element 430; a channel 441, a conductive material portion 442, and dielectrics 421 and 427. Dielectric 421 can include multiple materials 422, 423, and 424 arranged as different layers. As shown in FIG. 4, memory element 430 of each memory cell 210 has a ring shape (e.g., donut shape) with an inner side 451 and an outer side 452. Each of the other memory cells 211 and 212 shown in FIG. 3 also has a ring shape. As shown in FIG. 3, within memory cells 210, 211, and 212 in the same string (e.g., between transistors 231 and 232), the entire ring-shape memory element 430 of each memory cell is substantially vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

[0030] Each memory element 430 can store information, such as based on the amount of charge (e.g., number of electrons) therein. In each such memory element 430, the amount of charge corresponds to the value of information store that memory element. The amount of charge can be controlled in a write operation or in erase operation. For example, electrons from channel 441 or conductive material portion 442, or both, can move to memory element 430 during a write operation due to a tunneling effect known to those skilled in the art. In an erase operation, electrons from memory element 430 can move back to channel 441 or conductive material portion 442, or both, to data lines 251, 253, and 253 (FIG. 2 and FIG. 3). Alternative embodiments might use a memory element 430 that can store information, such as based on the resistance of the element 430, for example.

[0031] Memory device 200 of FIG. 3 can be formed using processes similar to or identical to those described below with reference to FIG. 5 through FIG. 29.

[0032] FIG. 5 through FIG. 29 show various processes of forming a memory device 500 having data lines located below memory cells, according to an

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embodiment of the invention. Memory device 500 (shown in more details in FIG. 29) can correspond to memory device 300 of FIG. 3.

[0033] FIG. 5 shows memory device 500 having a substrate 503, which can include materials 501 and 502 arranged as layers. Material 501 can include bulk silicon or could be another semiconductor material. Material 502 can be a dielectric material, for example, silicon oxide. FIG. 5 also shows materials 504 and 505 formed over substrate 503. Forming materials 504 and 505 can include depositing a conductive material over substrate 503 and then depositing another conductive material over material 504. Material 504 can include a metal or other conductive materials. Material 505 can include undoped polysilicon or doped polysilicon, such as p-type silicon or another conductive materials.

[0034] FIG. 5 also shows an X-direction, a Y-direction perpendicular to the X-direction, and a Z-direction perpendicular to both the X-direction and the Y-direction. As shown in FIG. 5, materials 504 and 505 can be formed as different layers, one layer over (e.g., on) one or more other layers in the Z-direction.

[0035] As used herein, the term "on" used with respect to two or more materials, one "on" the other, means at least some contact between the materials, while "over" or "overlaying" could refer to either a material being "on" another material or where there is one or more additional intervening materials between the materials (e.g., contact is not necessarily required). The term "on", "over", or "overlying" does not imply any directionality as used herein unless otherwise explicitly stated as such.

[0036] FIG. 6 shows memory device 500 after data lines 651, 652, and 653 and device structures 605 have been formed. A process such as etching (e.g., dry etching) can be used to remove portions of materials 504 and 505 (FIG. 5) to form trenches 511 and 512, which have trench bottoms at material 502. Each of data lines 651, 652, and 653 and each of device structures 605 has a greater dimension (e.g., length) extending in the X-direction. A mask (not shown in FIG. 6) having separate openings extending in the X-direction can be used to form trenches 511 and 512. As shown in FIG. 6, trenches 511 and 512 divide material 504 (FIG. 5) into

separate data lines 651, 652, and 653, which can correspond to data lines 251, 252, and 253 of FIG. 2.

[0037] FIG. 7 shows memory device 500 after pillars 705 have been formed in area 701 of memory device 500. Pillars 705 are not formed in area 702 of memory device 500. For simplicity, FIG. 7 through FIG. 29 do not show substrate 503 of FIG. 6. In FIG. 7, a process such as etching (e.g., dry etch) can be used to remove portions of device structures 605 to form trenches 711, 712, and 713 in the Y-direction, perpendicular to trenches 511 and 512, such that pillars 705 can be formed as shown in FIG. 7. A mask (not shown in FIG. 7) having separate openings extending in the Y-direction can be used to form trenches 711, 712, and 713. Each pillar 705 can include a height in the Z-direction of approximately 20 to 50 nanometers. As shown in FIG. 7, pillars 705 are arranged in rows and columns (e.g., in a matrix) in the X-direction and Y-direction. For simplicity, FIG. 7 does not show a dielectric material filled in trenches 511 and 512. However, forming memory device 500 in FIG. 7 also can include forming a dielectric material (e.g., silicon oxide) to fill trenches 511 and 512 up to a top surface 715 of device structure 605.

[0038] FIG. 8 shows memory device 500 after dielectric 831 and select lines 841, 842, 843, and 844 have been formed. Select lines 841, 842, 843, and 844 can correspond to select lines 241, 242, 243, and 244, respectively, of FIG. 3. In FIG. 8, dielectrics 831 are formed to electrically isolate select lines 841, 842, 843, and 844 from pillars 705. Dielectrics 831 can be formed by, for example, depositing a dielectric material (e.g., silicon oxide) on at least two sides of each pillar 705 or by oxidizing pillars 705. After dielectrics 831 are formed, select lines 841, 842, 843, and 844 can be formed by, for example, depositing a conductive material over pillars 705 and trenches 711, 712, and 713 (FIG. 7) and then removing (e.g., etching) a portion of the conductive material to form select lines 841, 842, 843, and 844 having the structure shown in FIG. 8. Examples of the conductive materials for select lines 841, 842, 843, and 844 include polysilicon, metal, or other conductive materials, such as TiN and TaN.

[0039] FIG. 8 also shows doped regions 833, which can be formed by inserting (e.g., implanting) n-type impurities into selective portions of device structure 605. Examples of n-type impurities include elements such as phosphorus (P) or arsenic (As). The remaining portion of device structures 605 that has not been inserted with n-type impurities may maintain its original material, such as p-type silicon, as described above with reference to FIG. 5.

[0040] FIG. 9 shows memory device 500 with select lines 941, 942, 943, and 944, which are alternative structures for select lines 841, 842, 843, and 844 of FIG. 8. In FIG. 8, opposite sides of each pillar 705 are associated with two different segments of the same select line 841, 842, 843, or 844. In FIG. 9, except for the top surfaces of pillars 705, each pillar 705 can be completely surrounded by the material of one of the select line 941, 942, 943, or 944 (e.g., four sides of each pillar 705 are associated with four different segments of the same select line). Higher efficient memory device may be achieved with select lines 941, 942, 943, and 944 in comparison to select lines 841, 842, 843, and 844. Select lines 941, 942, 943, and 944 can also be alternative structures for select lines 241, 242, 243, and 244, respectively, of FIG. 3. Thus, each transistor 231 of FIG. 2 and FIG. 3 can include a surrounded gate with a structure shown in FIG. 9. Thus, instead of a double-gate shown in FIG. 3, each transistor 231 of FIG. 3 can alternatively include a surrounded gate having four different segments of the same select line (such as select line 941) surrounding body 391 (FIG. 3).

[0041] FIG. 10 shows memory device 500 after materials 1001 through 1007 are formed over pillars 705 and select lines 841, 842, 843, and 844. Materials 1001 through 1007 can be formed in both areas 701 and 702 of memory device 500. However, to focus on the description herein, FIG. 10 does not show some portions of materials 1001 through 1007 in area 702. The description below with reference to FIG. 28 and FIG. 29 describes forming additional components (e.g., components similar to contacts 329 of FIG. 3) in area 702 of memory device 500.

[0042] In FIG. 10 through FIG. 29, for simplicity, some number designations associated with some components of memory device 500 may not be

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repeated from one figure to another figure. In FIG. 10, before forming materials 1001 through 1007, a dielectric material (not shown in FIG. 10), such as silicon oxide, can be formed to fill gaps 1041, 1042, and 1043. Forming materials 1001 through 1007 can include alternately depositing dielectric material and conductive material in an interleave fashion, such that these materials are alternately stacked over each other in the Z-direction, as shown in FIG. 10. Materials 1001, 1003, 1005, and 1007 can include dielectric materials, such as silicon oxide. Materials 1002, 1004, and 1006 can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon). As shown in FIG. 10, materials 1001 through 1007 are formed such that materials 1002, 1004, and 1006 are electrically isolated from each other by materials 1001, 1003, 1005, and 1007.

[0043] FIG. 11 shows memory device 500 after openings (e.g., holes) 1101 have been formed in material 1002 through 1107. Holes 1101 are formed such that each hole 1101 can be aligned substantially directly over a corresponding pillar 705, as illustrated in FIG. 11. Forming holes 1101 can include removing (e.g., etching) a portion of each of materials 1002 through 1007, stopping at material 1001, such that at least a portion of material 1001 or the entire material 1001 remains to separate holes 1101 from pillars 705. Forming holes 1101 results in forming cavities 1110 in each of materials 1003, 1005, and 1007, and cavities 1120 in each of materials 1002, 1004, and 1006. As shown in FIG. 12, cavities 1110 in the materials 1003, 1005, and 1007 are substantially aligned directly over cavities 1120 in the other materials 1002, 1004, and 1006. Each cavity 1110 and each cavity 1120 may have substantially the same diameter, D1. Diameter D1 can also be considered the diameter of each hole 1101 at the location of each cavity 1110 and each cavity 1120.

[0044] FIG. 12 shows memory device 500 after cavities 1220 have been formed in materials 1002, 1004, and 1006 (used to form control gates 1221, 1222, and 1223). Forming cavities 1220 can include enlarging the size of cavities 1120 (FIG. 11) while keeping the size of cavities 1110 substantially unchanged (e.g., remaining substantially at diameter D1). For example, enlarging the size of cavities 1120 (FIG. 11) can include selectively removing (e.g., selective wet or dry etching)

a portion of each of materials 1002, 1004, and 1006 at each cavity 1120 (FIG. 11) such that the diameter of each cavity 1220 increases to substantially diameter D2, while the diameter D1 at each cavity 1110 remains substantially unchanged. Diameter D2 is greater than diameter D1. Forming cavities 1120 in materials 1002, 1004, and 1006 also form control gates 1221, 1222, and 1223, which can correspond to control gates control gates 221, 222, and 223 of FIG. 2.

[0045] FIG. 13 shows more details of control gate 1221 of FIG. 12. Control gates 1222 and 1223 of FIG. 12 have a similar structure as control gate 1221. As shown in FIG. 13, control gate 1221 can include a homogenous material with cavities 1220 of FIG. 11 being arranged in rows and columns in the X-direction and Y-direction. Each cavity 1220 can include a sidewall 1225.

[0046] FIG. 14 and FIG. 15 shows memory device 500 after dielectrics 1421 and memory elements 1430 have been formed in cavities 1220. For simplicity, FIG. 15 does not show dielectrics 1421 and memory elements 1430 in all cavities 1220. Each dielectric 1421 can be formed on sidewall 1225, such that each dielectric 1421 and can be located between the material of control gate 1221 and memory element 1430, and such that memory element 1430 can be electrically isolated from the material of control gate 1221 by at least a portion of dielectric 1421. Forming dielectric 1421 can include forming multiple materials 1422, 1423, and 1424 (FIG. 15) at different times, one material after another. Forming material 1422 can include oxidizing a portion (e.g., a surface) of sidewall 1225 to form dielectric material (e.g., silicon oxide) on sidewall 1225. Alternatively, forming material 1422 can include depositing dielectric material (e.g., silicon oxide) on sidewall 1225. Forming material 1423 can include depositing dielectric material (e.g., silicon nitride) on material 1422, wherein a portion of that dielectric material may also form on sidewall 1425 of each cavity 1110. Forming material 1424 can include depositing dielectric material (e.g., silicon oxide) on material 1423.

[0047] Memory elements 1430 can be formed after dielectrics 1421 are formed. As shown in FIG. 15, each memory element 1430 has a ring shape (e.g., a donut shape) with an inner side 1451 and an outer side 1452 of FIG. 14. Forming

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memory elements 1430 can include depositing a material in holes 1101. Since cavities 1220 of FIG. 14 are substantially aligned with cavities 1110, the material (that forms memory element 1430) may fill both cavities 1110 and 1120. Then, a portion (e.g., center portion in each hole) of the material that forms memory elements 1430 can be removed (e.g., by etching in the same, single, etching step) such that the material in cavities 1110 can be removed (e.g., completely removed) and the material in cavities 1220 is not completely removed but partially removed. As shown in FIG. 14, after the material that forms memory elements 1430 is removed from cavities 1110, a portion of dielectric material 1423 (e.g., silicon nitride, that was formed on material 1422) may be exposed. As shown in FIG. 14, after the material that forms memory elements 1430 is partially removed from cavities 1220, memory element 1430 (formed by the remaining material in a cavity 1220) associated with the same hole 1101 may have its inner side 1451 substantially aligned with sidewall 1425 (or sidewall 1425 with portions of materials 1422 and 1423 of cavities 1110) of cavities 1110.

[0048] The material of memory elements 1430 can include, for example, semiconductor material (e.g., polysilicon), dielectric charge trapping material, such as silicon nitride or other dielectric charge trapping materials, or a variable resistance material, such as a phase change material (e.g., GST). During removing (e.g., etching) a portion of the material that forms memory elements 1430, portions 1401 of material 1001 located over pillars 705 can also be removed to reduce the thickness of portions 1401.

[0049] FIG. 16 and FIG. 17 show memory device 500 after dielectric 1627 has been formed on inner side 1451 of memory element 1430 and in cavities 1110. Forming dielectric 1627 can include depositing dielectric material (e.g., silicon oxide) on inner side 1451. Alternatively, forming dielectric 1627 can include oxidizing a portion (e.g., inner side 1451) of memory element 1430. Forming dielectric 1627 (e.g., by oxidation) may also consume material 1423 (FIG. 14) formed on material 1422, which formed on sidewall 1425 of cavities 1110. Thus, dielectric 1627 may also form in cavities over material 1422.

[0050] FIG. 18 and FIG. 19 show memory device 500 after channels 1841 have been formed on dielectrics 1627 in both cavities 1110 and 1220. Forming channels 1841 can include depositing a conductive material on dielectrics 1627. An etching process can be used to reduce the thickness of the conductive material after it is deposited. The conductive material of channels 1841 can include doped polysilicon, which can have the same material type (e.g., p-type) as pillars 705. FIG. 18 also shows a formation of openings 1801, which can be formed by removing (e.g., by etching) portions 1401 (FIG. 14) located over pillars 705. As shown in FIG. 19, channel 1841 is facing memory elements 1430 and is electrically isolated from memory element 1430 by at least a portion of dielectric 1627.

[0051] FIG. 20 shows memory device 500 after a conductive material 2001 has been formed by, for example, depositing undoped or lightly doped polysilicon to place channels 1841 in electrical communication with pillars 705. As shown in FIG. 20, conductive material 2001 forms a continuous conductive path between channels 1841 and data lines 651, 652, and 653 through pillars 705.

[0052] FIG. 21 shows memory device 500 after dielectric material 2101 (e.g., silicon oxide) has been formed over conductive material 2001.

[0053] FIG. 22 shows memory device 500 after a formation of openings (e.g., holes 2201), a conductive material portion 2260, and conductive material portions 2241. Holes 2201 are formed such that each hole 2201 can be aligned substantially directly over channels 1841, as illustrated in FIG. 22. Forming holes 2201 can include removing (e.g., etching) a portion of dielectric material 2101 and a portion of conductive material 2001 (FIG. 21), stopping at a location in material 1007. Holes 2201 can be formed such that after a portion of conductive material 2001 is removed during the formation of holes 2201, conductive material 2001 is separated into conductive material portion 2260 and conductive material portions 2241, as illustrated in FIG. 22.

[0054] FIG. 23 shows memory device 500 after doped regions 2301 have been formed. Forming doped regions 2301 can include inserting (e.g., implanting) n-type impurities into top parts of conductive material portions 2241. Doped

regions 2301 can provide a relatively low resistance connection between channels 1841 and other components of memory device 500.

[0055] FIG. 24 shows memory device 500 after dielectrics 2401 and channels 2402 have been formed. Dielectrics 2401 (e.g., silicon oxide) is formed on sidewalls of conductive material portion 2260 at the location of holes 2201. Channels 2402 are formed on sidewalls of dielectric material 2101 and on dielectrics 2401.

[0056] FIG. 25 shows memory device 500 after conductive material 2501 has been formed in each of holes 2201, such that channel 2402 can be electrically coupled to channel 1841 through conductive material 2501, doped region 2301, and conductive material portion 2241. Forming conductive material 2501 in each of holes 2201 can include depositing a conductive material (e.g., polysilicon) over material, such that the conductive material fills holes 2201. Then, a top portion of the conductive material can be removed by, for example, etching back the conductive material or by chemical mechanical planarization (CMP).

[0057] FIG. 26 shows memory device 500 after doped regions 2601 and select lines 2661, 2662, and 2663 have been formed. Forming doped regions 2601 can include inserting (e.g., implanting) n-type impurities into top portions of conductive material 2501. Forming select lines 2661, 2662, and 2663 can include removing parts of dielectric material 2101 and conductive material portion 2260 to form trenches 2602, which have trench bottoms partially extending into material 1007. As shown in FIG. 26, trenches 2602 separate conductive material portion 2260 into select lines 2661, 2662, and 2663, which can correspond to select lines 261, 262, and 263 of FIG. 2.

[0058] FIG. 27 shows memory device 500 after material 2701 and a common source 2770 have been formed. Forming material 2701 can include depositing a dielectric material (e.g., silicon dioxide) over material 2101, such that the dielectric material fills trenches 2602. Then, a top portion of the dielectric material can be removed by, for example, etching back the dielectric material or by

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CMP. Forming common source 2770 can include depositing a conductive material (e.g., metal) over materials 2701 and 2101.

[0059] FIG. 28 shows memory device 500 after materials 1001 through 1007 in area 702 (FIG. 10) are processed (e.g., by patterning) to form a stair like pattern with material between the stairs are not shown in FIG. 28. As mentioned above in the description of FIG. 10, some portions of materials 1001 through 1007 are omitted from area 702 of FIG. 10 through FIG. 27 for clarity. FIG. 28 shows material 1001 through 1007 in area 702 after they have been processed to form the stair like pattern. As shown in FIG. 28, control gates 1221, 1222, and 1223 are formed from materials 1002, 1004, and 1006, respectively, which are formed in the stair like pattern.

[0060] FIG. 29 shows memory device 500 after contacts 2929, 2949, and 2959 have been formed. Contacts 2929 provide electrical connections to control gates 1221, 1222, and 1223. Contacts 2949 provide electrical connections to select lines 841, 842, 843, and 844. Contacts 2959 provide electrical connections to and from data lines 651, 652, and 653.

[0061] As shown in FIG. 29, memory device 500 can include components and memory cells 2910, 2911, and 2912 similar to or identical to components and memory cells 210, 211, and 212 of memory device 300 described above with reference to FIG. 2 and FIG. 3.

[0062] One skilled in the art may readily recognize that additional processes may be performed to form additional features of a memory device, such as memory device 500 described above. Thus, to help focus on the embodiments described herein, FIG. 5 through FIG. 29 described above and FIG. 30 through FIG. 38 described below show only some of the features of a memory device, such as memory device 500.

[0063] FIG. 30 shows a schematic diagram of a portion of a memory device 300 having data lines 251, 252, and 253 located above memory cells 210, 211, and 212, according to an embodiment of the invention. Memory device 300 can include components similar to those of memory device 200 of FIG. 3. Thus, for simplicity,

similar or same components between memory device 200 and memory device 3000 are given the same number designations. The detailed description of these similar components is not repeated in FIG. 30. Main differences between memory device 3000 and memory device 200 include the locations of data lines 251, 252, and 253 and common source 3070 of memory device 3000 to enable global erase operation. As shown in FIG. 30, data lines 251, 252, and 253 are located above memory cells 210, 211, and 212. Common source 3070 is located below memory cells 210, 211, and 212 and can couple directly to at least a portion of a substrate of memory device 3000 (e.g., substrate 3101 in FIG. 31). This main difference may allow voltages to be applied to various components of memory device 3000 in a different way during an erase operation and memory device 3000 function differently (e.g., during the global erase operation) in comparison with the erase operation (e.g., local erase operation) of memory device 200. For example, in an erase operation of memory device 3000, a voltage of approximately 20 volts can be applied to common source 3070, while control gates 221, 221, and 223, data lines 251, 252, and 253, select lines 241, 242, and 243, and select lines 261, 262, and 26 can be "floated". In this erase operation, electrons from memory elements of memory cells 210, 211, and 212 may move (e.g., by tunneling) to common source 3070 (e.g., global erase). In memory 200, as described above with reference to FIG. 2, FIG. 3, and FIG. 4, during an erase operation, electrons from memory elements of memory cells 210, 211, and 212 may move to data lines 251, 253, and 253 (e.g., local erase)

[0064] FIG. 31 shows a 3D view of a portion of the memory device 3000 of FIG. 30, according to an embodiment of the invention. As shown in FIG. 31, data lines 251, 252, and 253 are located above memory cells 210, 211, and 212, common source 3070 is located below memory cells 210, 211, and 212 and is coupled to a substrate 3101. Substrate 3101 can include semiconductor material, such as p-type silicon.

[0065] As shown in FIG. 31, memory cells 210, 211, and 212 in each string (e.g., memory cells between transistors 231 and 232) are substantially vertically aligned in the Z-direction with respect to substrate 3101. Transistor 232 can include

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a double-gate or surrounded gate similar to the double-gate (FIG. 3) or surrounded gate (FIG. 9) of transistor 231 of FIG. 3. FIG. 31 also shows a channel 441 and a conductive material portion 442 extending vertically in the Z-direction and through memory element 430 of memory cells 210, 211, and 212 in the same string between transistors 231 and 232, which corresponds to transistors 231 and 232 of FIG. 30.

[0066] Memory element 430 in each of memory cells 210, 211, and 212 has a ring shape. As shown in FIG. 31, within memory cells 210, 211, and 212 in the same string, the entire ring-shape memory element 430 of each memory cell is substantially vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

[0067] FIG. 32 through FIG. 38 show various processes of forming a memory device 3200 having data lines located above memory cells, according to an embodiment of the invention. Memory device 3200 (shown in more details in FIG. 38) can correspond to memory device 3000 of FIG. 31.

[0068] FIG. 32 shows memory device 3200 having a substrate 3201 and trenches 3211, 3212, and 3213, and substrate portions 3270 and 3271 formed on a top portion of substrate 3201. Substrate 3201 can include semiconductor material, such as bulk silicon. Top substrate portions 3270 and 3271 can be formed by inserting (e.g., implanting) p-type impurities into a top portion of substrate 3201. Thus, substrate portions 3270 and 3271 can include p-type silicon. Forming trenches 3211, 3212, and 3213 and substrate portion 3270 can include removing (e.g., etching) a portion of substrate portion 3271. During a write or read operation of memory device 3200, substrate portion 3270 can be coupled to a potential, such as to ground. During an erase operation of memory device 3200, substrate portion 3270 can be coupled to a voltage, for example, approximately 20 volts.

[0069] FIG. 33 shows memory device 3200 after material 3301 has been formed in trenches 3211, 3212, and 3213 (FIG. 32). Forming material 3301 can include depositing dielectric material (e.g., silicon oxide) over substrate 3201 to fill trenches 3211, 3212, and 3213. Then, a top portion of the dielectric material can be removed by, for example, CMP.

[0070] FIG. 34 shows memory device 3200 after material 3401 and trenches 3411, 3412, and 3413, and device structures 3460 have been formed. Forming material 3401 can include depositing dielectric material (e.g., silicon oxide, or silicon nitride) over substrate 3201 and material 3301. Forming trenches 3411, 3412, and 3413 can include removing (e.g., etching) portions of substrate 3201, material 3301, and material 3401. Device structures 3460 are formed as a result of the formation of trenches 3411, 3412, and 3413.

[0071] FIG. 35 shows memory device 3200 after a formation of doped regions 3501, material 3502, and select lines 3561, 3562, and 3563. Forming doped regions 3501 can include inserting (e.g., implanting) n-type impurities into selective portions of substrate portion 3271. Material 3502 (e.g., silicon oxide) can be formed on both sides of each device structure 3460 to electrically isolate select lines 3561, 3562, and 3563 from device structures 3460. Materials of select lines 3561, 3562, and 3563 can include one or more conductive materials, such as one or more metals, alloys, other conductive materials, or a combination thereof. Select lines 3561, 3562, and 3563 can correspond to select lines 261, 262, and 263 of memory device 3000 of FIG. 30.

[0072] FIG. 36 shows memory device 3200 after material 3601 have been formed in trenches 3411, 3412, and 3413. Forming material 3601 can include depositing dielectric material (e.g., silicon dioxide) to fill trenches 3411, 3412, and 3413. Then, a top portion of the dielectric material can be removed by, for example, etching back the conductive material or by CMP, stopping at substrate portion 3270.

[0073] FIG. 37 shows memory device 3200 after grooves 3701 have been formed by removing (e.g., by wet etching) a top portion of the material used to form select lines 3561, 3562, and 3563. Alternatively, forming grooves 3701 can be omitted.

[0074] FIG. 38 shows memory device 3200 after other components have been formed. The processes for forming the components of memory device 3200 in FIG. 38 can include similar or identical processes for forming the component of memory device 500 described above with reference to FIG. 10 through FIG. 29.

For example, control gates 3821, 3822, and 3823 of FIG. 38 can be formed using processes similar to or identical to those of forming control gates 1221, 1222, and 1223 of memory device 500 described above with described above with reference to FIG. 5 through FIG. 29. Data lines 3851, 3852, and 3853 of FIG. 38, can correspond to data lines 251, 252, and 253 of FIG. 30 and FIG. 31. As shown in FIG. 38, memory device 3200 can include memory cells 3810, 3811, and 3812, which can be formed using processes similar to or identical to those of forming memory cells 2910, 2911, and 2912 of memory device 500 described above with reference to FIG. 5 through FIG. 29.

[0075] One or more embodiments described herein include a memory device and methods of forming the memory device. One such memory device can include a first group of memory cells, each cell of the first group being formed in a respective cavity of a first control gate located in one device level of the memory device. The memory device also can include a second group of memory cells, each cell of the second group being formed in a cavity of in a second control gate located in another device level of the memory device. Additional apparatus and methods are described. Other embodiments including additional apparatus and methods are described above with reference to FIG. 1 through FIG. 38.

[0076] The illustrations of apparatus such as memory devices 100, 200, 500, 3000, and 3200, and memory cells 210, 211, 212, 2910, 2911, 2912, 3010, 3811, and 3812 are intended to provide a general understanding of the structure of various embodiments and not a complete description of all the elements and features of the apparatus that might make use of the structures described herein.

[0077] The apparatus of various embodiments may include or be included in electronic circuitry used in high-speed computers, communication and signal processing circuitry, memory modules, portable memory storage devices (e.g., thumb drives), single or multi-processor modules, single or multiple embedded processors, multi-core processors, data switches, and application-specific modules including multilayer, multi-chip modules. Such apparatus may further be included as sub-components within a variety of electronic systems, such as televisions,

cellular telephones, personal computers (e.g., laptop computers, desktop computers, handheld computers, tablet computers, etc.), workstations, radios, video players, audio players (e.g., MP3 (Motion Picture Experts Group, Audio Layer 3) players), vehicles, medical devices (e.g., heart monitor, blood pressure monitor, etc.), set top boxes, and others.

[0078] The above description and the drawings illustrate some embodiments of the invention to enable those skilled in the art to practice the embodiments of the invention. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Examples merely typify possible variations. Portions and features of some embodiments may be included in, or substituted for, those of others. Many other embodiments will be apparent to those of skill in the art upon studying and understanding the above description.

[0079] The Abstract is provided to comply with 37 C.F.R. §1.72(b) requiring an abstract that will allow the reader to quickly ascertain the nature and gist of the technical disclosure. The Abstract of the Disclosure is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

What is claimed is:

1. An apparatus comprising:

first memory cells located in a first device level of a memory device;

second memory cells located in a second device level of the memory device;

a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate; and

a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate.

2. The apparatus of claim 1, wherein each of the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, further comprising:

a common source; and

data lines configured to be selectively coupled to the common source and the memory cells through a conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

5. The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.

6. The apparatus of claim 1, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

7. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

8. The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

9. An apparatus comprising:

a first non-volatile memory cell including a first memory element, the first memory element having a ring shape;

a second non-volatile memory cell including a second memory element, the second memory element having a ring shape; and

a conductive material extending through the first and second memory elements.

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10. The apparatus of claim 9, further comprising:

a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in a first device level of a memory device in which the first and second memory cells are located; and

a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in a second device level of the memory device.

11. The apparatus of claim 10, wherein each of the memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. The apparatus of claim 11, wherein each of the memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the data line is located between the substrate and the first memory cell.

14. The apparatus of claim 9, further comprising a data line over a substrate to carry signals representing values of information stored in the first and second memory cells, wherein the first and second memory cells are located between the substrate and the data line.

15. An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

16. The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.

17. The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material.

18. The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.

19. The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.

20. The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

21. The apparatus of claim 15, further comprising:

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

22. A method comprising:

forming a first non-volatile memory cell including a first memory element having a ring shape;

forming a non-volatile second memory cell including a second memory element having a ring shape; and

forming a conductive material extending through the first and second memory elements.

23. The method of claim 22, wherein forming the first memory cell comprises forming a first cavity in a first conductive material, wherein the first memory element is formed in the first cavity, wherein forming the second memory cell comprises forming a second cavity in a second conductive material, and wherein the second memory element is formed in the second cavity.

24. The method of claim 23, wherein the first cavity is substantially aligned over the second cavity.

25. The method of claim 22, further comprising:

forming a data line over a substrate, wherein the data line is located between the substrate and the first and second memory cells.

26. The method of claim 22, further comprising:

forming a data line over a substrate, wherein the first and second memory cells are located between the substrate and the data line.

27. A method comprising:

forming conductive material layers and dielectric material layers such that the conductive material layers are electrically isolated from each other by the dielectric material layers;

forming cavities in each of the conductive material layers; and

forming a memory element in each of the cavities.

28. The method of claim 27, wherein each of the conductive material layers is between two of the dielectric material layers and at least one of the conductive material layers is between two of the conductive material layers.

29. The method of claim 27, wherein the memory element comprises polysilicon.

30. The method of claim 27, wherein the memory element comprises a dielectric material.

31. The method of claim 27, wherein forming the cavities includes:

forming initial cavities in the conductive material layers; and

enlarging a size of the initial cavities to form the cavities in each of the conductive material layers.

32. The method of claim 31, further comprising:

forming openings through the conductive material layers and the dielectric material layers to form the initial cavities.

33. The method of claim 32, wherein second cavities are formed in each of the dielectric material layers when the openings are formed, and a size of the second cavities remains substantially unchanged when the size of the initial cavities is enlarged.

34. The method of claim 33, wherein each of the second cavities and each of the initial cavities has a substantially same diameter.

Abstract of the Disclosure

Some embodiments include a memory device and methods of forming the memory device. One such memory device includes a first group of memory cells, each of the memory cells of the first group being formed in a cavity of a first control gate located in one device level of the memory device. The memory device also includes a second group of memory cells, each of the memory cells of the second group being formed in a cavity of a second control gate located in another device level of the memory device. Additional apparatus and methods are described.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 12/825,211

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**34** minus 20 =	**14**	x$26		OR	x$52	**728**
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**5** minus 3 =	* **2**	x$110			x$220	**440**
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	**2258**

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

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