

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner

v.

MICRON TECHNOLOGY, INC.

Patent Owner

IPR2025-00498

U.S. PATENT 8,803,214

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,803,214

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EX1005	Korean Patent Application Publication No. 10-2010-0034612 in the Name of Ahn <i>et al.</i>
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EX1007	U.S. Patent Application Publication No. 2009/0146190 in the Name of Fukuzumi <i>et al.</i>
EX1008	Joint Claim Construction and Prehearing Statement and Appendices (Patent Local Rule 4-3), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 105 (N.D. Cal. August 19, 2024)
EX1009	U.S. Patent Application Publication No. 2010/0240205 in the Name of Son <i>et al.</i>
EX1010	U.S. Patent No. 7,425,742 to Nazarian
EX1011	Y. Chen <i>et al.</i> , “Flash Memory Reliability NEPP 2008 Task Final Report,” JPL Publication, (2009), Available Online at https://nepp.nasa.gov/files/16376/08_106_1%20JPL%20Chen%20Flash%20Memory.pdf
EX1012	F. Arai <i>et al.</i> , “Extended Data Retention Process Technology for Highly Reliable Flash EEPROMs of 10 ⁶ to 10 ⁷ W/E Cycles,” 1998 IEEE International Reliability Physics Symposium Proceedings. 36th Annual, Reno, NV, USA, 1998, pp. 378-382
EX1013	S. Wang <i>et al.</i> , “A High-Endurance (>100K) BE-SONOS NAND Flash With a Robust Nitrided Tunnel Oxide/Si Interface,” 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2010, pp. 951-955
EX1014	C. Sandhya <i>et al.</i> , “Nitride Engineering and the Effect of Interfaces on Charge Trap Flash Performance and Reliability,” 2008 IEEE International Reliability Physics Symposium, Phoenix, AZ, USA, 2008, pp. 406-411

Exhibit	Description
EX1015	U.S. Patent Application Publication No. 2009/0310425 in the Name of Sim <i>et al.</i>
EX1016	U.S. Patent Application Publication No. 2010/0120214 in the Name of Park <i>et al.</i>
EX1017	U.S. Patent Application Publication No. 2011/0286283 in the Name of Lung <i>et al.</i>
EX1018	U.S. Patent Application Publication No. 2007/0057328 in the Name of Taniguchi <i>et al.</i>
EX1019	U.S. Patent Application Publication No. 2010/0133598 in the Name of Chae <i>et al.</i>
EX1020	K. Joo <i>et al.</i> , “Novel Transition Layer Engineered Si Nanocrystal Flash Memory with MHSOS Structure Featuring Large V_{th} Window and Fast P/E Speed,” IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest., Washington, DC, USA, 2005, pp. 865-868
EX1021	S. Park <i>et al.</i> , “A New Operating Scheme by Switching the Polarity of Program/Erase Bias for Partially Oxidized Amorphous-Si-Based Charge-Trap Memory,” IEEE Transactions on Electron Devices, vol. 53, no. 11, Nov. 2006, pp. 2847-2849
EX1022	M. Rosmeulen <i>et al.</i> , “Silicon Rich Oxides as an Alternative Charge Trapping Medium in Fowler-Nordheim and Hot Carrier Type Non-Volatile-Memory Cells,” Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 189-192
EX1023	Counterclaim Plaintiff Micron Technology’s Disclosure of Asserted Claims and Infringement Contentions and Document Production Accompanying Disclosure (Patent Local Rules 3-1 and 3-2), <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL (N.D. Cal.)
EX1024	J. Jang <i>et al.</i> , “Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193
EX1025	Defendant’s Answer To First Amended Complaint And Counterclaims, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 35 (N.D. Cal. February 16, 2024)
EX1026	Order Granting Motion To Dismiss Counterclaims, <i>Yangtze Memory</i>

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	<i>Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 78 (N.D. Cal. July 16, 2024)
EX1027	Defendant's First Amended Counterclaims, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 93 (N.D. Cal. August 1, 2024)
EX1028	Defendant's Unopposed Motion To Modify The Case Schedule To Permit Defendant To Reassert Counterclaims, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 213 (N.D. Cal. January 29, 2025)

All citations to 35 U.S.C. §§ 102 and 103 in this paper refer to the Pre-AIA statutes.

All emphases in quotations are added unless otherwise noted.

Direct quotations of claim language are italicized.

This paper includes color illustrations and should be viewed in color.

I. INTRODUCTION

Yangtze Memory Technologies Company, Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1-7, 9-12, and 14-20 (“challenged claims”) of U.S. Patent No. 8,803,214 (“’214 patent,” EX1001) assigned to Micron Technology, Inc. (“PO”).

The challenged claims recite features related to three-dimensional (3D) NAND memory devices, all of which were well-known and conventional before the ’214 patent. Notably, the purportedly allowable subject matter, as well as every other limitation of the challenged claims, are explicitly disclosed by each of two prior art references alone: U.S. Patent Application Publication No. 2010/0140685 in the name of Kang *et al.* (“Kang,” EX1004) and U.S. Patent Application Publication No. 2009/0146190 in the name of Fukuzumi *et al.* (“Fukuzumi,” EX1007).

Petitioner’s expert, Dr. Kelin Kuhn—a semiconductor industry veteran with four decades of experience—has thoroughly analyzed the prior art and confirms that the challenged claims are unpatentable over these references and other prior art predating the ’214 patent.

Petitioner thus respectfully requests the Board cancel the challenged claims.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest

The real parties-in-interest are Yangtze Memory Technologies Company, Ltd.

and Yangtze Memory Technologies, Inc.

B. Related Matters

The '214 patent is not currently asserted in any pending civil action. In *Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. et al.*, No. 3:23-cv-05792-RFL (N.D. Cal.) (“NDCA case”), however, PO has filed an unopposed motion for leave to amend its counterclaims to assert the '214 patent in the NDCA case.¹ That motion remains pending.

Petitioner filed an IPR (Case IPR2025-00099, “'099 IPR”) on November 18, 2024, against U.S. Patent No. 10,872,903 (“'903 patent”), which is one of the child patents of the '214 patent and asserted in the NDCA case. The '099 IPR is currently pending institution decision.

Petitioner is concurrently filing another IPR (Case IPR2025-00499, “'499 IPR”) on the same day, challenging a different set of claims of the '214 patent: claims 8, 13, and 21.

C. Lead and Back-up Counsel and Service Information

Petitioner identifies the following lead and back-up counsels:

¹ The '214 patent was initially included in PO’s February 16, 2024 Answer and Counterclaim, but the Court dismissed it under FRCP 12(b)(6), with leave to amend. EX1025, EX1026. Rather than amending the pleadings, PO chose to drop the '214 patent on August 1, 2024. EX1027. Months later, PO now seeks to reassert the '214 patent. EX1028.

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Petitioner consents to electronic service at YMTC-Micron-IPR@bayes.law, as well as the above email addresses.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that the '214 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified in this Petition.

IV. RELIEF REQUESTED

Under 35 U.S.C. § 311, Petitioner requests IPR of claims 1-7, 9-12, and 14-20 of the '214 patent.

A. Claims for Which Review Is Requested

Petitioner requests IPR and cancellation of challenged claims 1-7, 9-12, and 14-20 of the '214 patent under 35 U.S.C. § 311 based on the following grounds. This

Petition is supported by the Declaration of Dr. Kelin Kuhn (“Kuhn Decl.,” EX1003).

B. Statutory Grounds of Challenge

Petitioner relies on the following prior art and statutory grounds of challenge to the challenged claims:

Name	Ex.	Publication No.	Filed	Published	Prior art under at least
Kang	1004	US2010/0140685	12/10/2009	6/10/2010	§§102(a) & (e)
Ahn ²	1005	KR10-2010-0034612	9/24/2008	4/1/2010	§102(a)
Fukuzumi	1007	US2009/0146190	12/1/2008	6/11/2009	§102(b)

Ground	Claims	Basis	References
1 & 2	1-7, 9-12, and 14-20	§§102/103	Kang
3	16	§103	Kang in view of Ahn
4 & 5	1-7, 9-12, and 14-20	§§102/103	Fukuzumi
6	6	§103	Fukuzumi in view of Kang
7	16	§103	Fukuzumi in view of Ahn

Each of Kang and Ahn was published before the filing date of the ’214 patent, June 28, 2010, and therefore qualifies as prior art under pre-AIA 35 U.S.C. §102(a). Kang also qualifies as prior art under pre-AIA 35 U.S.C. §102(e), as its filing date precedes June 28, 2010. Fukuzumi was published more than one year before June 28, 2010, and thus qualifies as prior art under at least pre-AIA 35 U.S.C. §102(b).

V. THE ’214 PATENT

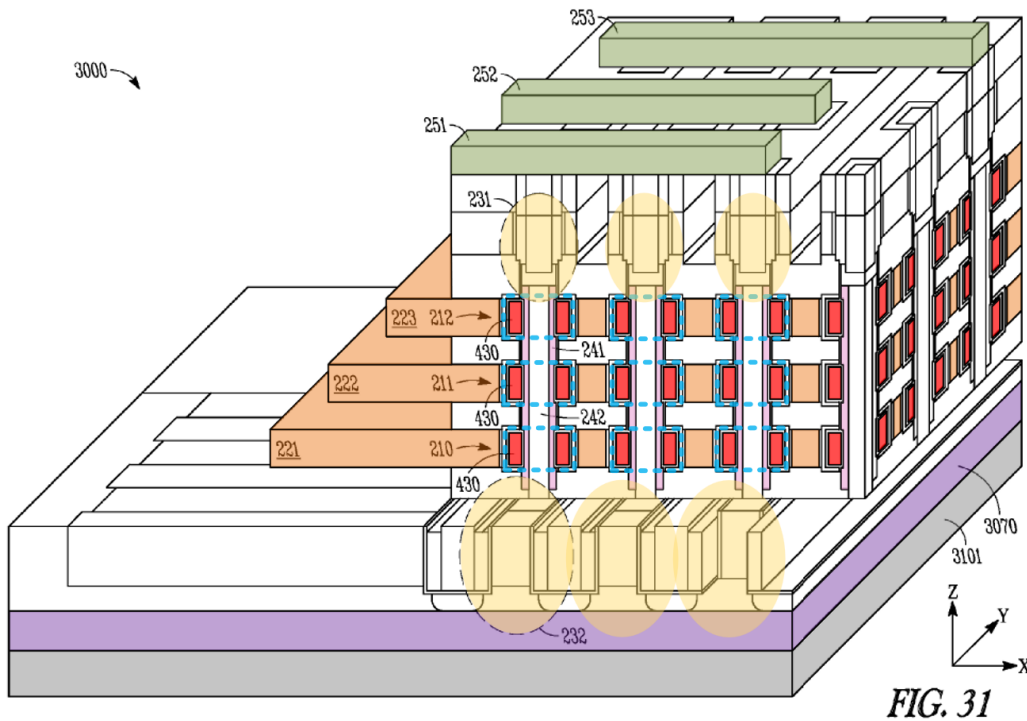
A. Overview

The ’214 patent relates to nonvolatile memory devices. EX1001, 1:6-8; 2:63-

² A certified English translation of Ahn is submitted herewith (EX1006).

67. The '214 patent recognizes that “[s]ince 3D memory devices are relatively new, manufacturing these devices can pose fabrication process challenges,” and thus, proposes embodiments related to memory devices and methods of forming the devices. EX1001, 1:20-22, 12:30-31. The memory devices include multiple groups of memory cells in different device levels. EX1001, 12:32-41.

FIG. 31 of the '214 patent below (annotated in Kuhn Decl. as FIG. B) shows the embodiment of a memory device 3000 related to the challenged claims. EX1003, ¶57.



EX1003 — FIG. B

Memory device 3000 includes a string of memory cells 210-212 in the Z-direction, and channels 241 (in pink) extending in the Z-direction through ring-

shaped memory elements 430 (in red) of memory cells 210-212. EX1001, 10:61-11:19; EX1003, ¶¶57-58. Memory elements 430, formed in cavities (in blue dashed boxes) of control gates 221-223 (in orange), store charge. EX1001, 4:34-5:3, 7:43-8:38, 10:30-35; EX1003, ¶59. A common source 3070 (in purple) is formed between memory cells 210-212 and a substrate 3101 (in gray) and is coupled with channels 241 through lower select transistors 232 (in yellow), while data lines 251-253 (in green) are formed above memory cells 210-212 and are coupled with channels 241 through upper select transistors 231 (in yellow). EX1001, 10:27-67. EX1003, ¶60.

B. Prosecution History

In the first Office Action on the merits, the Examiner rejected claims 1-6 and 9-21 as being unpatentable over U.S. Patent Application Publication No. 2009/0230454 in the name of Pekny (“Pekny”) under Pre-AIA 35 U.S.C. § 103(a), and rejected claims 7 and 8 as being unpatentable over Pekny in view of U.S. Patent Application Publication No. 2007/0057310 in the name of Matsui *et al.* (“Matsui”) under pre-AIA 35 U.S.C. §103(a). EX1002, 206-215. In response, PO amended the claims and argued, relevant to the challenged claims, that Pekny failed to disclose first memory cells/first control gate/first conductive material and second memory cells/second control gate/second conductive material being formed in different device levels (claims 1 and 15), and memory elements having a ring shape (claim 9). EX1002, 149-159.

In the Final Office Action, the Examiner maintained the rejection of claims 9-14 over Pekny. EX1002, 138-141. The Examiner also indicated that claims 1-8 and 5-21 were allowed, and the allowable subject matter related to “*a plurality of second memory cells*” in claim 1, “*a common source*,” “*data lines*,” and the relative positions between “*the first and second memory cells*,” “*the common source*,” and “*the substrate*” in claim 4 (now claim 8), and “*a second conductive material*” in claims 15 and 20 (now claim 21) EX1002, 141-142.

In response, PO amended independent claim 9 to include the limitation that the first and second memory elements are in different device levels. EX1002, 122-128.

The Examiner eventually allowed all claims in the Notices of Allowance, noting that the prior art on the record failed to teach claim limitations related to “*a second control gate*” and “*data lines*” in claims 1, 4, 9, and 20, and “*a second dielectric*” and “*a conductive channel*” in claim 15. EX1002, 40-41, 102-103.

C. The Level of Ordinary Skill in the Art

A POSITA at the time of the claimed invention would have had a Bachelor’s degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. EX1003, ¶31. A higher level of education might make up for less experience, and

vice versa. EX1003, ¶31.

VI. CLAIM CONSTRUCTIONS

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Because the prior art asserted herein discloses embodiments within the claims' indisputable scope, the Board need not construe the claims' outer bounds. Other than the term “*cavity*” recited in challenged claims 1 and 15 as noted below, all claim terms should be construed according to their plain and ordinary meaning as would have been understood by a POSITA.

In the NDCA case³, Petitioner proposes that “a [first-fourth] cavity of [first/second] control gate” should be construed as “a [first-fourth] hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate.” EX1008, 17-18. PO asserts those terms should be given their plain and ordinary meaning, without specifying the meaning. EX1008, 17-18. The court in the NDCA case has not construed the term yet.

Regardless, the prior art discloses this limitation under either party's

³ The same term “*cavity*” is recited in claims 1 and 17 of the child '903 patent, which is asserted in the NDCA case.

construction (*see* Grounds 1, 2, 4, and 5).

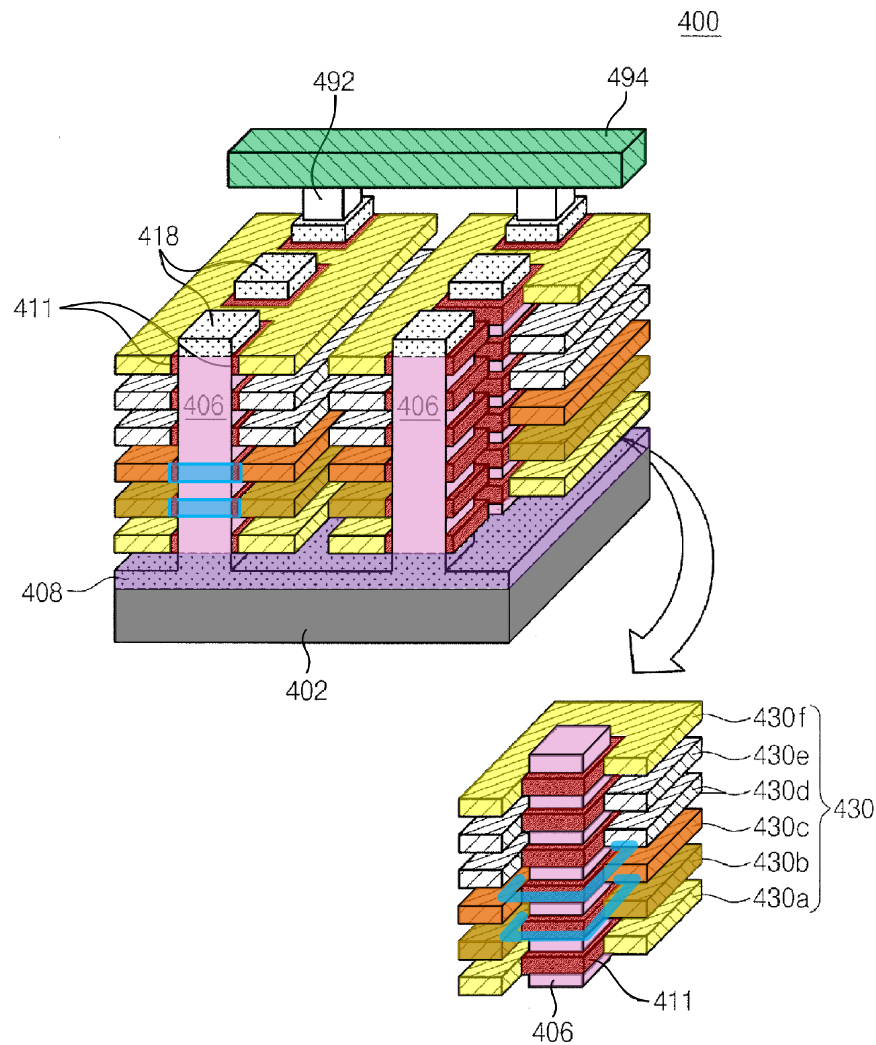
VII. GROUNDS 1 AND 2: KANG ANTICIPATES OR OTHERWISE RENDERS OBVIOUS CLAIMS 1-7, 9-12, AND 14-20

A. Overview of Kang

Kang relates to nonvolatile memory devices and their fabricating methods. EX1004, [0002]. Similar to the '214 patent, Kang recognizes the importance of increasing the integration of semiconductor memory devices and proposes various 3D designs of stacking memory cell arrays and their manufacturing methods. EX1004, [0003]-[0013], FIGs. 1A-1E; EX1003, ¶70.

In one embodiment of Kang regarding FIG. 1E (referred to herein as “FIG. 1E embodiment”) as shown with annotations below, a nonvolatile memory device 400 is a vertical NAND flash memory device including an active pillar 406 (in pink), vertically extending from a semiconductor substrate 402 (in gray), and a gate group 430. EX1004, [0059]; EX1003, ¶¶72-73. Gate group 430 includes a lower select gate 430*a* (in yellow), an upper select gate 430*f* (in yellow), and multiple control gates 430*b*-430*e* (in orange and brown), each having a horizontal plate shape. EX1004, [0060]. Active pillar 406 vertically penetrates through cavities (in blue) of gate group 430, and is electrically coupled with a bit line 494 (in green) through an upper select transistor having upper select gate 430*f*. EX1004, [0059]-[0060]; EX1003, ¶73.

Fig. 1E



EX1003 — FIG. C

Active pillar 406 is also electrically coupled with a common source 408 (in purple) through a lower select transistor having lower select gate 430a. EX1004, [0059]-[0060]; EX1003, ¶73. A ring-shaped charge storage layer 411 (in red) is formed in each cavity between a respective one of control gates 430b-430e and active pillar 406. EX1004, [0061]; EX1003, ¶74. Charge storage layer 411 is an

ONO layer—“a silicon nitride layer for trapping charges to store data and any one of two silicon oxide layers being used as a tunnel insulating layer and the other being used as a blocking insulating layer.” EX1004, [0038]⁴.

As shown in FIG. 1E above, the upper select transistors, memory transistors, and lower select transistors, which are formed at the intersections between active pillars 406 and plate-shaped upper select gate 430f, control gates 430b-430e, and lower select gates 430a, respectively, in this embodiment, have surrounded gates. EX1004, [0041], [0042], [0060]; EX1003, ¶75.

In another embodiment of Kang regarding FIG. 1C (referred to herein as “FIG. 1C embodiment”), the upper select transistors and lower select transistors—formed at the intersections between active pillars 206 and line-shaped upper select gate 230f and lower select gates 230a, respectively—each have an independent gate on either side of active pillar 206. EX1004, [0041], [0052]. This design, known as double-gate configuration, differs from the surrounded-gate configuration. EX1003, ¶76.

B. Independent Claim 1

1. Kang discloses “[a]n apparatus” [1.P].

Kang discloses a flash memory system 1310 (“[a] apparatus”). EX1004,

⁴ A POSITA would have understood that the descriptions of common features shared among multiple embodiments, although described in connection with one embodiment (*e.g.*, FIG. 1A), are equally applicable to other embodiments that include these shared features. EX1004, [0043], [0050], [0054], [0058]; EX1003, ¶71.

[0107], FIG. 5B. Thus, Kang discloses [1.P].

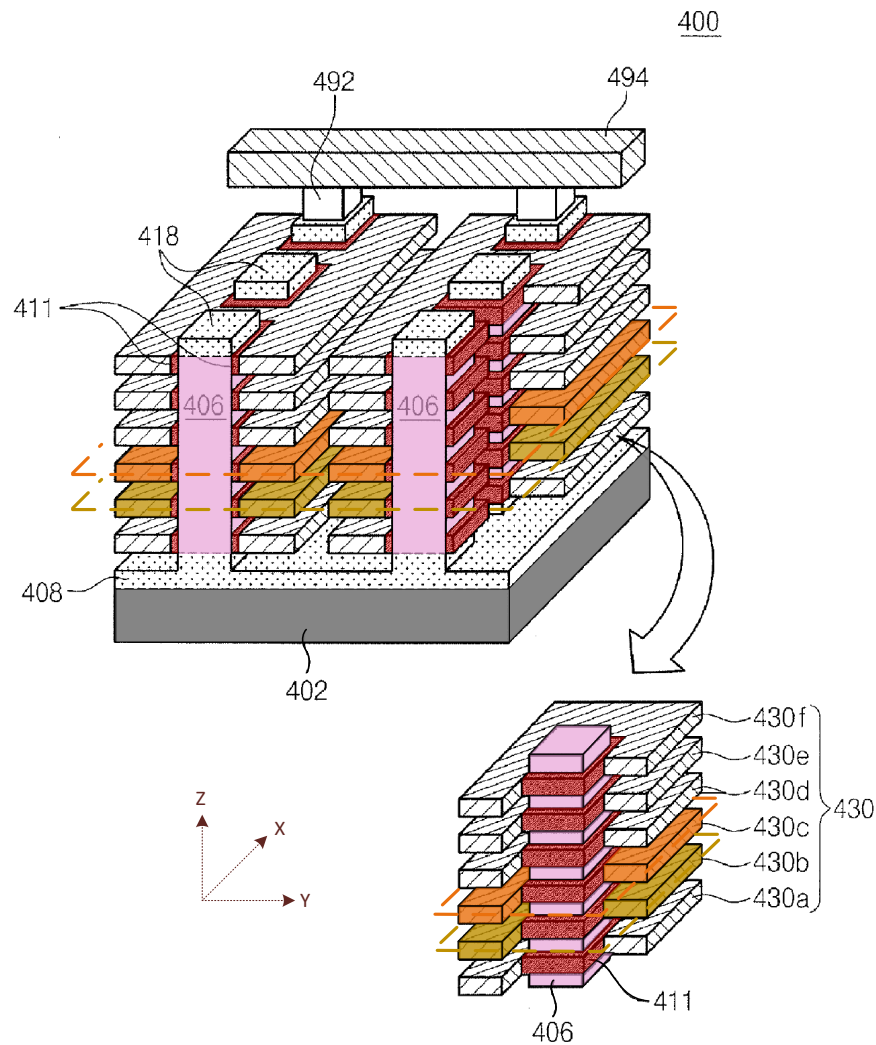
2. Kang discloses “*a substrate of a memory device*” [1.a].

Kang discloses a semiconductor substrate 402 of nonvolatile memory device 400 (“*a memory device*”) in its FIG. 1E embodiment, which is included in flash memory system 1310. EX1004, [0059], [0107], FIG. 1E. Thus, Kang discloses [1.a].

3. Kang discloses “*a plurality of first memory cells located in a first device level of the memory device over the substrate*” [1.b], and “*a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level*” [1.c].

Kang discloses a plurality of cell strings 103, each including a plurality of memory transistors 133 vertically and serially connected to each other on a semiconductor substrate 102 in a nonvolatile memory device 100. EX1004, [0041]. Kang further discloses that memory transistors 133 in nonvolatile memory device 100 are respectively formed at the intersections between active pillars 106 and control gates 130*b*-130*e* in a 3D arrangement. EX1004, [0041]-[0042]. Since the 3D arrangement of memory transistors with respect to the control gates is one of the common features across all the embodiments (*see* FN4), a POSITA would have understood that memory transistors are also formed in the intersections between active pillars 406 and control gates 430*b*-430*e* in a 3D arrangement in nonvolatile memory device 400 of FIG. 1E. EX1003, ¶89.

Fig. 1E



EX1003 — FIG. J

As illustrated in annotated FIG. 1E above, nonvolatile memory device 400 also includes a first group of memory transistors (in brown dashed box) located in a first level (e.g., the same level as first control gates 430b, in brown) over semiconductor substrate 402 (“a plurality of first memory cells located in a first device level of the memory device over the substrate”), and a second group of

memory transistors (in orange dashed box) located in a second level (e.g., the same level as second control gates 430c, in orange) over semiconductor substrate 402 (“a plurality of second memory cells located in a second device level of the memory device over the substrate”). EX1003, ¶¶90-91. FIG. 1E clearly shows that the first level is positioned below and thus, different from the second level in the 3D arrangement (“the first device level is different from the second device level”). EX1003, ¶91.

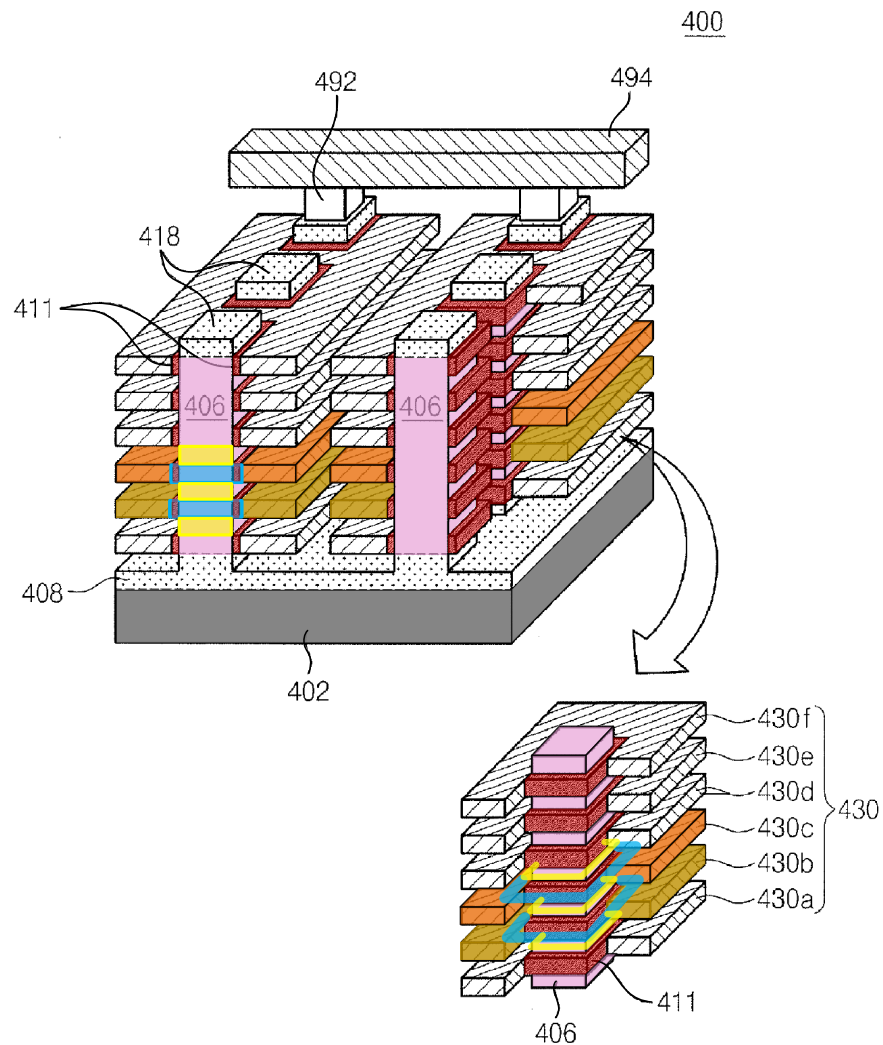
4. **Kang discloses “a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate” [1.d], and “a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate” [1.e].**

Kang discloses control gates 430b-430e, each having a horizontal plate shape located at a corresponding level and functioning to control the corresponding memory transistors. EX1004, [0038], [0060]-[0061], [0080]; EX1003, ¶94. As shown in annotated FIG. 1E below, first control gate 430b (in brown, “a first control gate formed in the first device level”) is used to control access to the first group of memory transistors (“the first control gate to control access to the first memory cells”), and second control gate 430c (in orange, “a second control gate formed in the second device level”) is used to control access of the second groups of memory

transistors (“the second control gate to control access to the first memory cells”).

EX1003, ¶94.

Fig. 1E



EX1003 — FIG. K

Kang discloses that control gates 130b-130e are “vertically stacked” and electrically connect a word line driving circuit and thus, control access to the groups of memory transistors in different levels, respectively. EX1004, [0037], [0042];

EX1003, ¶95; FN 4. Further, Kang discloses that each memory transistor includes a charge storage layer, which “may be used as a charge storage layer which traps charges to store data.” EX1004, [0038]. Kang specifies that the charge storage layer includes “an ONO layer, [*i.e.*,] a silicon nitride layer [that] may actually trap charges to store data and any one of two silicon oxide layers [that] may be used as a tunnel insulating layer and the other may be used as a blocking insulating layer.” EX1004, [0038]. Thus, a POSITA would have understood that the silicon nitride layer in charge storage layer 411 is the claimed “*memory element*.” EX1003, ¶96.

Moreover, since Kang further discloses that active pillar 406 “may vertically penetrate the gate group 430,” and that charge storage layer 411 “is limited between the active pillar 406 and the gate group 430,” a POSITA would have understood that active pillar 406 and charge storage layers 411 create holes through gate group 430, respectively, in which active pillar 406 and charge storage layers 411 occupy. EX1004, [0060]-[0061]; EX1003, ¶97. Thus, Kang discloses “*a cavity of the first/second control gate*” in which corresponding parts of active pillar 406 and charge storage layers 411 are positioned. EX1003, ¶97. This is further illustrated in annotated FIG. 1E above, where two charge storage layers 411 (in red) are formed in two cavities (in blue) of two control gates 430*b* and 430*c* (in brown and orange), respectively. EX1003, ¶98.

As discussed in Section VI, to the extent that “*cavity*” requires a hole in the

control gate to have a larger diameter than the holes in the layers above and below the control gate, Kang's FIG. 1E still discloses the "*cavity*" as it further discloses that charge storage layer 411 "have a separated shape divided according to each of the gates 430*a* through 430*f*," and that "a charge storage layer is divided according to each gate, so an operation error can be substantially reduced." EX1004, [0061], [0111]; EX1003, ¶99. Thus, a POSITA would have understood, or at least found it obvious that, as further illustrated in annotated FIG. 1E above, the holes (in blue) in each of control gates 430*b* and 430*c* (in brown and orange) have a diameter larger than the holes (in yellow) in insulating layers 460/260⁵ above and below the respective control gate 430*b* or 430*c*. EX1003, ¶101.

Thus, Kang discloses "*cavity*" under either party's construction.

Accordingly, Kang discloses [1.d] and [1.e].

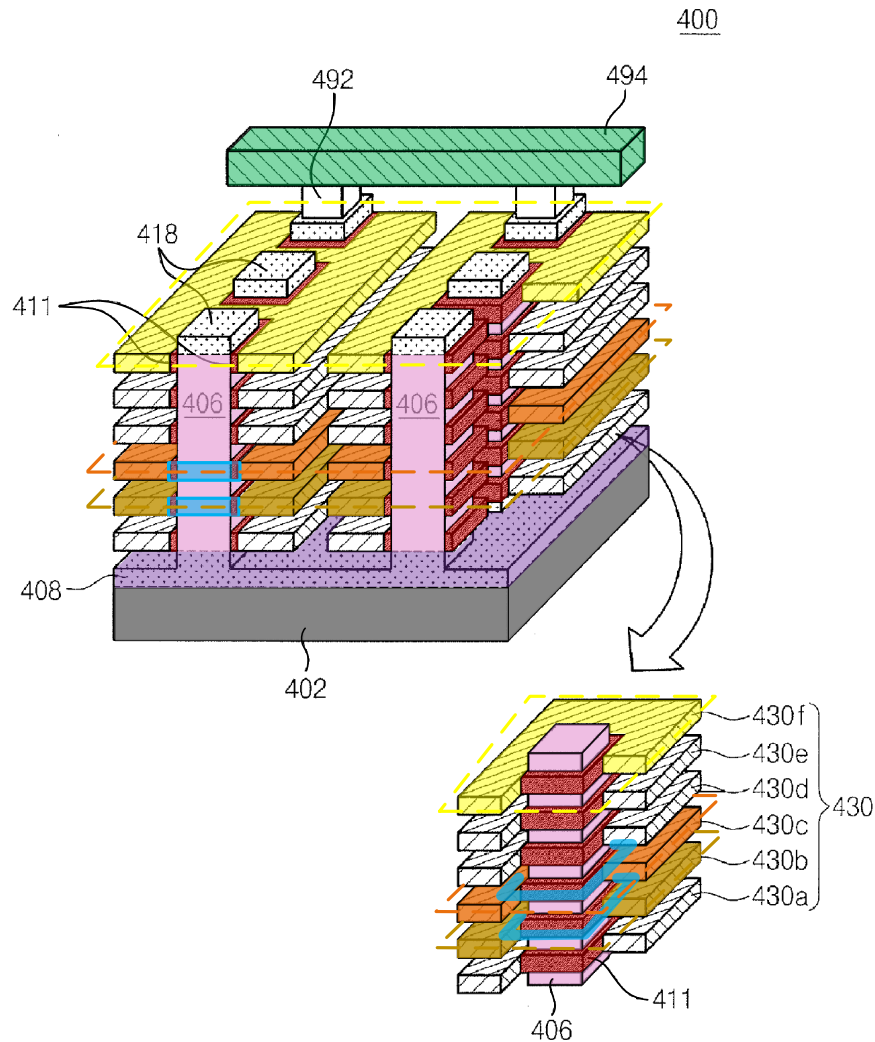
5. Kang discloses or suggests "*data lines configured to be selectively coupled to a common source and the memory cells through conductive material*" [1.f].

As shown in annotated FIG. 1E below, Kang discloses bit lines 494 (in green, "*data lines*") electrically connected to a source 408 (in purple) and the first and

⁵ Insulating layers 460 are not shown in FIG. 1E since "FIG. 1E is the nonvolatile memory device 400 from which the insulating layers 460 is removed." EX1004, [0101]. A POSITA would have understood that in FIG. 1E, recesses vertically between adjacent control gates 430 and laterally contacting active pillars 406 represent insulating layers 460. EX1004, [0087], [0101]; EX1003, ¶100.

second groups of memory transistors (in brown and orange dashed boxes, “*the memory cells*”) via active pillars 406 (in pink). EX1004, [0059]-[0060]; EX1001, 3:29-31; EX1003, ¶103.

Fig. 1E



EX1003 — FIG. L

A POSITA would have understood that source 408 is commonly connected to multiple active pillars 406 and functions as a common source of multiple cell strings,

for example, through “a common source line,” and thus, is a “*common source*.” EX1004, [0037]; EX1003, ¶104.

Kang also discloses bit lines 494/194⁶ being electrically connected to active pillars 406/106 via upper select transistors (*e.g.*, 135, in yellow dashed box), which include upper select gates 430f/130f (in yellow) electrically connected to an upper select line driving circuit. EX1004, [0037], [0041], [0060], FIGs. 1A-1B, 1E, EX1003, ¶105. A POSITA would have understood that the electrical connection between bit lines 494 and active pillars 406 is controlled by the upper select transistors. EX1004, [0041], [0045]; EX1003, ¶106. A POSITA would have also understood that the upper select line driving circuit selects/deselects each cell string by turning upper select transistors on or off to control the connections between bit lines 494 and active pillars 406, through upper select gates 430f of the corresponding upper select transistors. EX1004, [0037]; EX1003, ¶106. Therefore, Kang discloses that bit lines 494 are configured to be “*selectively*” coupled to the memory transistors and source 408 through active pillar 406.

Since Kang discloses that active pillar 406/106 includes “a single crystalline silicon of p-type,” a POSITA would also have understood, or at least found it

⁶For clarity and ease of reference, when a common feature across different embodiments of Kang is discussed, it may be referred to by collectively using the respective numerical labels of that feature from those embodiments, *e.g.*, bit lines 494/194 refers to common feature “bit lines” in two different embodiments. FN4.

obvious, that Kang's active pillar 406 having p-type doped single crystalline silicon includes a "*conductive material*," consistent with the '214 patent. EX1004, [0034]; EX1001, 8:64-67; EX1003, ¶107. Thus, Kang discloses or suggests [1.f].

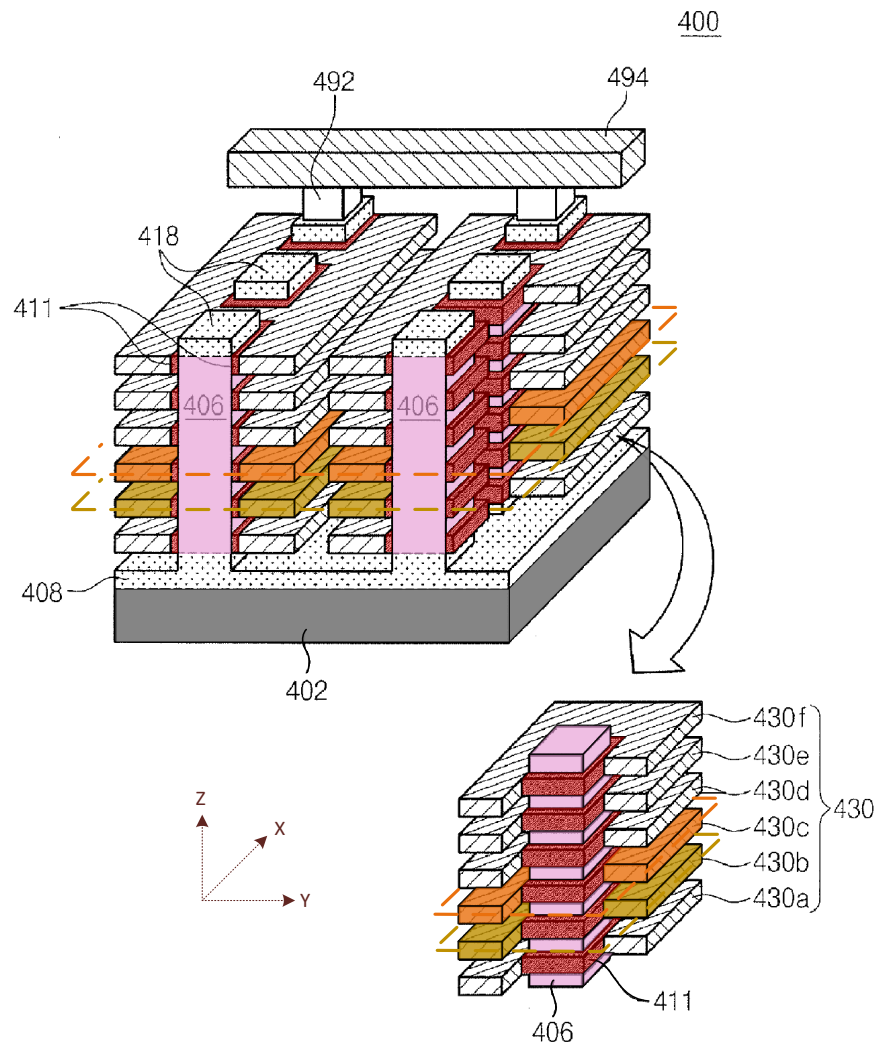
From the foregoing, Kang anticipates or otherwise renders obvious claim 1.

C. Dependent Claim 2

Kang further discloses that "*the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction*," and "*the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions*," additionally required by claim 2.

As shown in annotated FIG. 1E below, each of the first and second groups of memory transistors (in brown and orange dashed boxes, "*the first and second memory cells*") are arranged in an array including multiple memory transistors along an X-direction/word line direction ("*in a first direction*") and a Y-direction/bit line direction ("*in a second direction*"). EX1004, [0040], [0042], FIG. 1B; EX1003, ¶109.

Fig. 1E



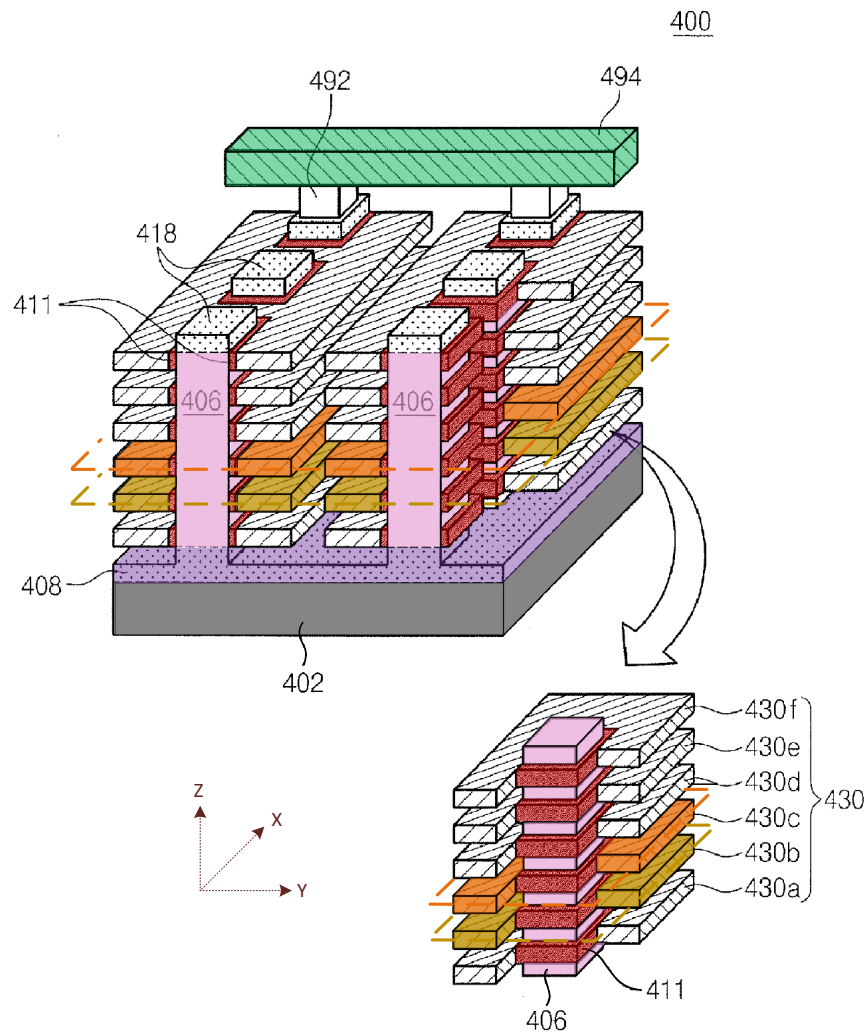
EX1003 — FIG. M

Kang also discloses that active pillar 406/106 (“*conductive material*”) extends through the first and second levels in which the first and second groups of memory transistors are located (“*first and second memory cells*”) along a Z-direction/vertical direction (“*in a third direction*”) perpendicular to the X- and Y- directions (“*first and second directions*”). EX1004, [0034], [0060]; EX1003, ¶110.

D. Dependent Claim 3

Kang further discloses or otherwise renders obvious that “*the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation,*” additionally required by claim 3.

Fig. 1E



EX1003 — FIG. N

As shown in annotated FIG. 1E above, Kang further discloses that source 408 (in purple, “*common source*”) is over substrate 402 (in gray) and below the first and second groups of memory transistors (in brown and orange dashed boxes, “*first and second memory cells*”), *i.e.*, source 408 between the first and second groups of memory transistors and substrate 402. EX1004, [0059]-[0060]; EX1003, ¶112.

Kang further discloses that “electrons generated by GIDL are discharged to the semiconductor substrate 102,” and “electrons accumulated in the memory transistor 133 are discharged, so data erasing operation can be embodied.” EX1004, [0048]. A POSITA would have understood, or at least found it obvious from Kang’s teaching that, during an erasing operation of Kang’s nonvolatile memory device 400, the electrons accumulated in the silicon nitride layer of charge storage layer 411 (in red in FIG. 1E above, “*memory element*”) are discharged to substrate 402/102 (in gray) through source 408 (in purple, “*moved to the common source*”). EX1004, [0038]; EX1003, ¶114.

Notably, the ’214 patent characterizes the claimed erase operation as one of these operations that can be recognized by one skilled in the art, of which the detailed descriptions are omitted to help focus on the description therein. EX1001, 3:54-64, 10:44-60; EX1003, ¶113.

E. Dependent Claims 4 and 5

Kang further discloses that “*the first memory cells are substantially vertically*

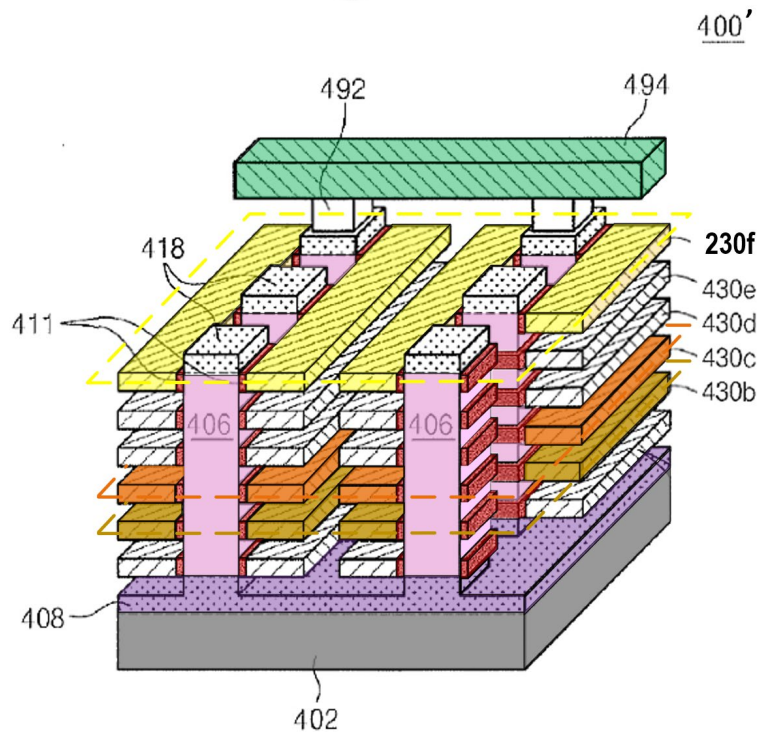
aligned with the second memory cells,” additionally required by claim 4, and that *“the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells,”* additionally required by claim 5.

Kang further discloses that the memory transistors are vertically and serially connected to form a cell string, with each active pillar 406/106 extending vertically through gate group 430/130. EX1004, [0041]. Additionally, the silicon nitride layer in charge storage layer 411/110 of each memory transistor within a cell string surrounds one side of active pillar 406/106. EX1004, [0038], [0041].

Thus, as shown in annotated FIG. 1E below, a POSITA would have understood that the memory transistors in each cell string are substantially vertically aligned (*“the first memory cells are substantially vertically aligned with the second memory cells”*), and that charge storage layers 411 (in red) including the silicon nitride layers (*“memory elements”*) surround active pillar 406, thereby being vertically aligned (*“the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells”*). EX1003, ¶117.

or otherwise renders obvious claim 1. Additionally, Kang's FIG. 1C embodiment discloses that "gate group 230 may include a lower select gate 230a, an upper select gate 230f... formed to have **a line shape on both sides** of active pillar 206." EX1004, [0052]. A POSITA would have understood that the upper selection transistors include upper select gate 230f, which is a "*double-gate*." EX1003, ¶122.

Fig. 1E



EX1003 — FIG. Q
(Annotated and Modified FIG. 1E of Kang)

A POSITA would have been motivated to modify Kang's FIG. 1E embodiment in view of FIG. 1C embodiment by incorporating the double-gate-type select gate 230f from the FIG. 1C embodiment in place of the surrounded-gate-type upper select gate 430f, while maintaining the surrounded gate configuration for

control gates 430*b*-430*e*, as illustrated in annotated and modified FIG. 1E of Kang above. EX1003, ¶123.

Such a modification would reduce gate and parasitic capacitance and limit parasitic effects caused by the electric field overlap between the drain and gate regions. EX1003, ¶124. A POSITA would have a reasonable expectation of success in applying this modification, as the use of a double-gate structure for selection transistors was well-known in the art. EX1015, [0103]-[0106], FIGs. 31, 36, 37; EX1016, [0075]-[0080], FIG.11; EX1017, [0012]; EX1019, [0070], FIGs. 6-7, 12; EX1003, ¶125. It would have been obvious to POSITA to substitute double-gate-type upper select gate 230*f* from FIG. 1C embodiment for surrounded-gate-type upper select gate 430*f* in FIG. 1E embodiment for the predictable results of reduced gate and parasitic capacitance and suppressed parasitic effects. EX1003, ¶126.

As shown in modified FIG. 1E above, bit lines 494 (in green, “*data lines*”) are electrically connected to first and second groups of memory transistors (in brown and orange dashed boxes, “*first and second memory cells*”) via active pillars 406 (in pink). EX1004, [0059]-[0061]; EX1003, ¶127. Bit lines 494 are electrically connected to active pillars 406 via modified upper select transistors (in yellow dashed box, “*transistors*”), which include double-gate-type upper select gates 230*f* (in yellow) electrically connected to an upper select line driving circuit. EX1004, [0037], [0041], [0052], FIGs. 1A-1C; EX1003, ¶127. A POSITA would have

understood that bit lines 494 are coupled with the first and second groups of memory transistors through the modified upper select transistors, and that the upper select line driving circuit selects/deselects each cell string by turning the modified upper select transistors on or off to control the connections between bit lines 494 and the memory transistors, through upper select gates 230f of the corresponding modified upper select transistors. EX1004, [0045]; EX1003, ¶128.

Thus, Kang's modified FIG. 1E embodiment in view of FIG. 1C embodiment discloses the upper select transistors, which includes a “*double-gate*” upper select gate 230f, to “*selectively*” couple the first and second groups of memory transistors to bit lines 494 during a memory operation of nonvolatile memory device 400. EX1003, ¶129.

Therefore, Kang's FIG. 1E embodiment modified in view of FIG. 1C embodiment renders obvious claim 6.

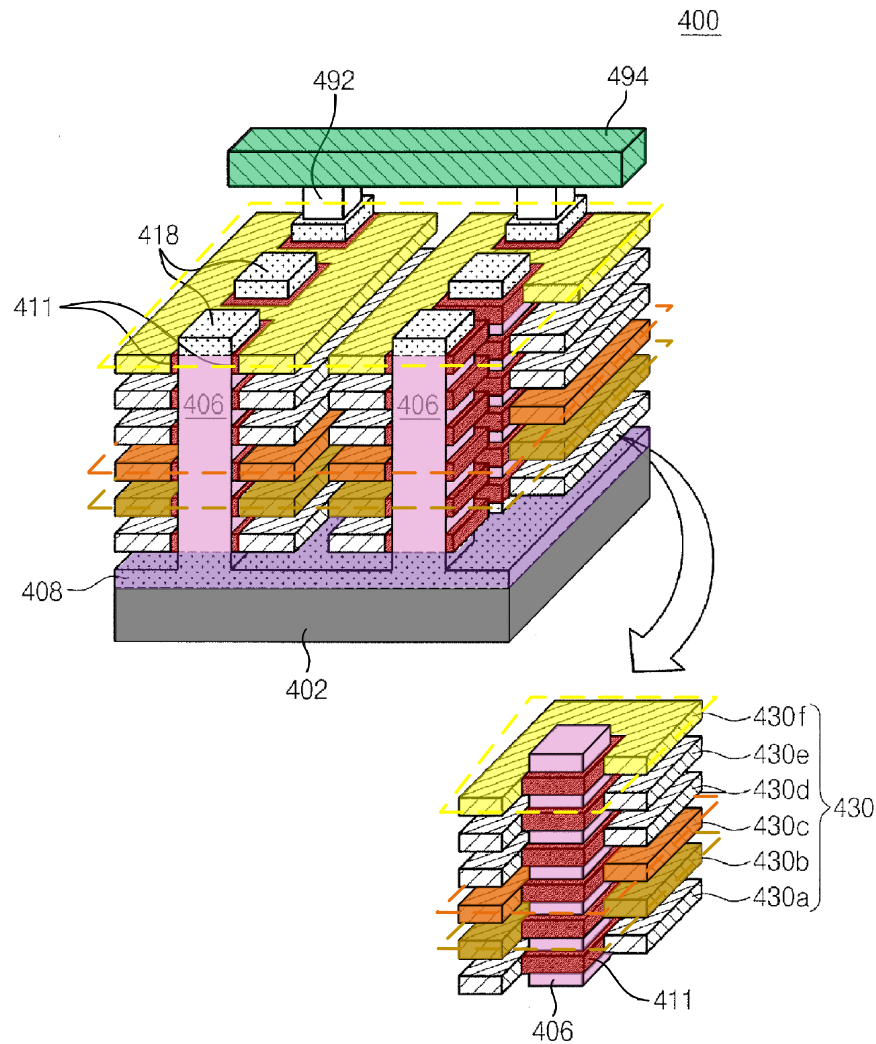
G. Dependent Claim 7

Claim 7 depends on claim 1 and further requires “*transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device*” [7.a], and “*at least one of the transistors comprises a surrounded gate*” [7.b].

Referring back to Kang's FIG. 1E embodiment by which mapping to claim 1 is made in Section VII.B, similar to the discussion above in Section VII.F with

respect to [6.1], bit lines 494 (in green), as shown in annotated FIG. 1E below, are coupled with the first and second groups of memory transistors (in brown and orange dashed boxes, “*first and second memory cells*”) through the upper select transistors (e.g., 135, in yellow dashed box, “*transistors*”). EX1004, [0037], [0041], [0052]; EX1003, ¶131.

Fig. 1E



EX1003 — FIG. R

A POSITA would have understood that the upper select line driving circuit selects/deselects each cell string by turning the upper select transistors on or off to control the connections between bit lines 494 and the memory transistors, through upper select gates 430f (in yellow) of the corresponding upper select transistors. EX1004, [0045]; EX1003, ¶131.

Therefore, Kang's FIG. 1E embodiment discloses the upper select transistors to “*selectively*” couple the first and second groups of memory transistors to bit lines 494 during a memory operation of nonvolatile memory device 400. EX1003, ¶132.

Kang's FIG. 1E embodiment further discloses that “gate group 430 may include a lower select gate 430a, an upper select gate 430f ... formed to have a **horizontal plate shape**” and that “active pillar 406 may vertically **penetrate** the gate group 430.” EX1004, [0060]. Thus, a POSITA would have understood that the upper selection transistors include upper select gate 430f surrounding active pillar 406 and thus, is a “*surrounded gate*.” EX1003, ¶133.

Thus, Kang's FIG. 1E embodiment discloses [7.a] and [7.b].

H. Independent Claim 9

1. Kang discloses “[a]n apparatus” [9.P].

As discussed in Section VII.B.1, Kang discloses “[a]n apparatus.”

2. **Kang discloses or suggests “a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device” [9.a], and “a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level” [9.b].**

As discussed in Sections VII.B.3 and VII.B.4, Kang discloses “a plurality of first/second memory cells located in a first/second device level of the memory device over the substrate, wherein the first device level is different from the second device level,” and “each of the first/second memory cells includes a memory element.”

Since the first and second groups of memory transistors discussed in Sections VII.B.3 and VII.B.4 are in **nonvolatile** memory device 400, Kang also discloses a “first non-volatile memory cell” in the first group of memory transistors and a “second non-volatile memory cell” in the second group of memory transistors. EX1004, [0059]; EX1003, ¶138.

Kang further discloses that “charge storage layer 411 may have a **ring** or band shape surrounding a side of active pillar 406,” and that an insulating layer 110 from which charge storage layer 411/111 is formed is “**conformally** formed using a deposition process.” EX1004, [0061], [0066], FIG. 1E. Kang thus also discloses or suggests that the silicon nitride layers of charge storage layers 411 (“memory

element”) have “*a ring shape*.” EX1003, ¶139.

Accordingly, Kang discloses or suggests [9.a] and [9.b].

3. **Kang discloses or suggests “*a conductive material extending through the first and second memory elements*” [9.c], and “*a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material*” [9.d].**

As discussed in Sections VII.B.5 and VII.C, Kang discloses or suggests “*data lines configured to be selectively coupled to a common source and the memory cells through conductive material*” and “*the conductive material extending through the first and second memory cells in a third direction*.” Thus, Kang also discloses or suggests [9.c] and [9.d]. EX1003, ¶141.

From the foregoing, Kang anticipates or otherwise renders obvious claim 9.

I. Dependent Claim 10

Kang further discloses “*a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in the first device level of the memory device*,” and “*a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in the second device level of the memory device*,” additionally recited in

claim 10.

As explained in Section VII.B.4, Kang discloses “*a first/second control gate formed in the first/second device level, the first/second control gate to control access to the first/second memory cells.*” Kang further discloses that “conductive group 130 may be comprised of a conductor, *e.g.*, silicon, metal or combinations thereof so that the conductive group 130 is used as a gate,” and that “the medium conductive layers 130*b* through 130*e* may be used together with the term ‘control gate.’” EX1004, [0036], [0038], [0060]. Thus, Kang also discloses first control gate 430*b*/130*b* (“*a first additional conductive material configured to operate as a control gate*”) to access the first group of memory transistors, and second control gate 430*c*/130*c* (“*a second additional conductive material configured to operate as a control gate*”) to access the second group of memory transistors. EX1003, ¶143.

J. Dependent Claims 11 and 12

Kang further discloses or suggests “*each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material,*” additionally required by claim 11, and “*each of the first and second memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material,*” additionally required by claim 12.

Kang discloses that each memory transistor includes charge storage layer

411/111 having “an ONO structure, an ONO layer, [including] a silicon nitride layer [which] may actually trap charges to store data and any one of two silicon oxide layers [which] may be used as a tunnel insulating layer and the other [which] may be used as a blocking insulating layer” and “in which a silicon nitride is interposed between the silicon oxide layers.” EX1004, [0035], [0066].

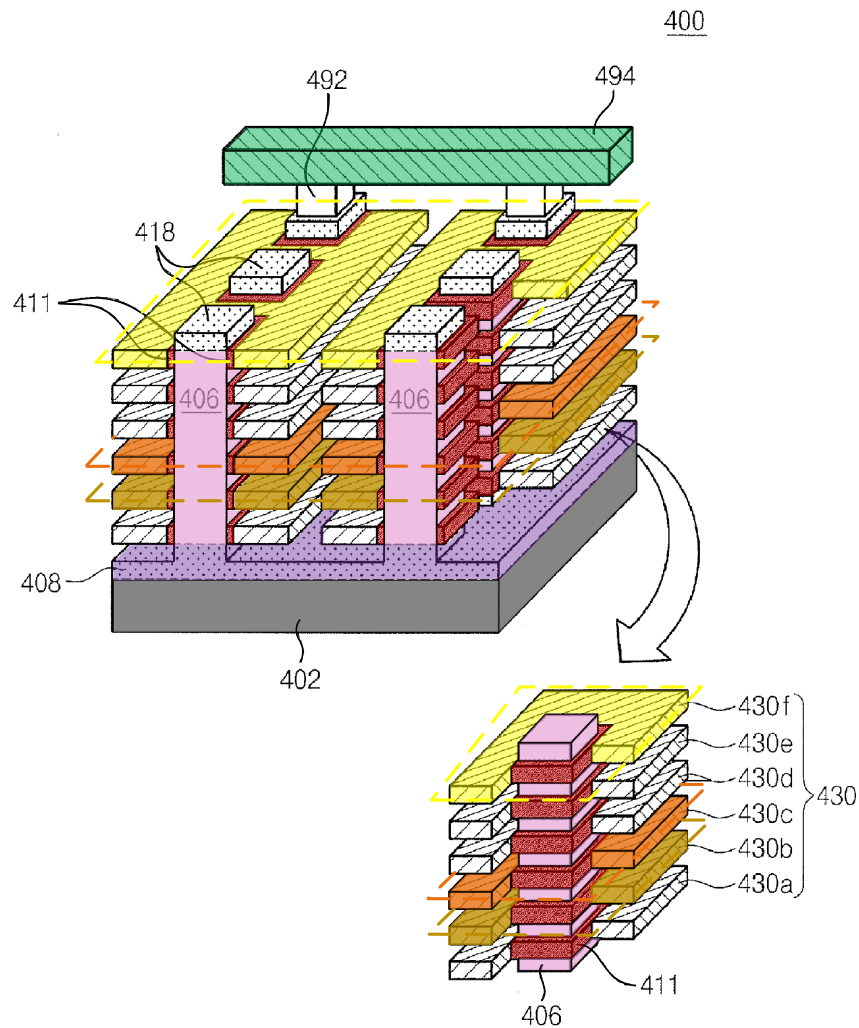
Thus, a POSITA would have understood, or at least found it obvious, that each memory transistor includes: (i) one silicon oxide layer (“*a first dielectric*”) of charge storage layer 411 located between the respective silicon nitride layer of charge storage layer 411 (“*memory element*”) and active pillar 416 (“*conductive material*”), and (ii) the other silicon oxide layer of charge storage layer 411 (“*a second dielectric*”) between the respective silicon nitride layer of charge storage layer 411 (“*memory element*”) and the respective control gate 430b or 430c (“*additional conductive material*”). EX1003, ¶¶145-146.

K. Dependent Claim 14

Kang further discloses that “*the first and second memory cells are located between the substrate and the data line,*” additionally required by claim 14.

As shown in annotated FIG. 1E below, Kang further discloses that the first and second groups of memory transistors (in brown and orange dashed boxes, “*first and second memory cells*”) are located between semiconductor substrate 402 (in gray) and bit lines 494 (in green, “*data lines*”). EX1004, [0059]; EX1003, ¶147.

Fig. 1E



EX1003 — FIG. S

L. Independent Claim 15

1. Kang discloses “[a]n apparatus” [15.P].

Kang discloses [15.P], which is the same as [1.P]. Section VII.B.1.

2. Kang discloses “a substrate of a memory device” [15.a].

Kang discloses [15.a], which is the same as [1.a]. Section VII.B.2.

3. **Kang discloses or suggests “a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall” [15.b], and “a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level” [15.c].**

As discussed in Section VII.B.3-VII.B.4, Kang discloses “a first/second control gate formed in the first/second device level,” “a cavity of the first/second control gate,” and “the first device level is different from the second device level.”

Kang further discloses first and second control gates 430b/130b and 430c/130c are “formed of a conductor such as silicon or metal.” EX1004, [0069]. Regarding the “first/second conductive material located in a first/second device level, ... including a first/second cavity” recited in claim 15, the specification of the ’214 patent describes that “[m]aterials 1002, 1004, and 1006 can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon),” and “[f]orming cavities 1120 in materials 1002, 1004, and 1006 also form control gates 1221, 1222, and 1223, which can correspond to control gates control gates 221, 222, and 223 of FIG. 2.” EX1001, 7:3-5, 39-42. Thus, the metal or silicon control gates 430b and 430c are the claimed “first conductive material” and “second conductive material,” respectively, consistent with the ’214 patent. EX1003, ¶152.

As discussed in Section VII.B.4, a POSITA would have understood, or at least found it obvious, that the hole (“*first/second cavity*”) in which corresponding parts of active pillar 406 and charge storage layer 411 are formed has a respective sidewall (“*a first/second sidewall*”) on first or second control gate 430*b* or 430*c* under either party’s interpretation of “*cavity*.” EX1003, ¶153.

Thus, Kang discloses or suggests [15.b] and [15.c].

4. **Kang discloses or suggests “*a first dielectric formed on the first sidewall and the second sidewall*” [15.d], “*a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric*” [15.e], “*a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric*” [15.f], and “*a second dielectric formed on a side of the first memory element and on a side of the second memory element*” [15.g].**

As discussed in Section VII.B.4, Kang discloses that “*each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.*”

Kang further discloses charge storage layer 411 being “an ONO layer” in which the silicon nitride layer “N” (“*first/second memory element*”) is “inserted between silicon oxide layers” laterally. EX1004, [0038], [0066]; EX1003, ¶155. A POSITA would have understood, or at least found it obvious, that nonvolatile memory device 400 further includes one of the silicon oxide layers (“*a first*

dielectric”) of charge storage layer 411, which is formed on the sidewalls of the holes through which active pillar 416 and charge storage layers 411 penetrate (*“first/second sidewalls”*). EX1003, ¶156; Section VII.J. A POSITA would further have understood, or at least found it obvious, that nonvolatile memory device 400 further includes the other one of the silicon oxide layers (*“a second dielectric”*) of charge storage layer 411, which is formed on the sides of the corresponding silicon nitride layers (*“first/second memory elements”*). EX1003, ¶156; Section VII.J.

Since the silicon nitride layer is “inserted between silicon oxide layers” laterally in the ONO structure of charge storage layer 411, a POSITA would have understood, or at least found it obvious, that the silicon nitride layer in a respective charge storage layer 411 (*“first/second memory element”*) is electrically isolated from the respective first or second control gate 430*b* or 430*c* (*“first/second conductive material”*) by a respective portion of the silicon oxide layer (*“first/second portion of the first dielectric”*). EX1003, ¶157.

Therefore, Kang discloses or suggests [15.d]-[15.g].

5. **Kang discloses or suggests “a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric” [15.h].**

Kang discloses that “nonvolatile memory device 400 may be a vertical NAND

flash memory device” and “gate group 430 us[es] active pillar 406 as a channel.” EX1004, [0059]. A POSITA would have understood that, during certain operations of the vertical NAND flash memory device, a channel forms in the vertical outermost layer of active pillar 406 and does not extend throughout the entire active pillar 406. EX1015, [0063], [0070], FIG. 11; EX1003, ¶¶159-160. Thus, Kang discloses “*a conductive channel*.”⁷

Kang also discloses that “active pillar 406 may vertically penetrate the gate group 430.” EX1005, [0060]. As discussed in Section VII.B.4, Kang further discloses that first and second control gates 430*b* and 430*c*, which are parts of gate group 430, are in the first and second device levels. Thus, Kang discloses that active pillar 406, including its vertical outermost layer (“*conductive channel*”), extends from the first device level to the second device level. EX1003, ¶161.

As discussed in Sections VII.J and VII.L.4, a POSITA would have understood, or at least found it obvious, that the other one of the silicon oxide layers (“*second dielectric*”) is formed laterally between the corresponding silicon nitride layers (“*first/second memory elements*”) and the vertical outermost layer of active pillar 406 (“*conductive channel*”), such that the vertical outermost layer of active pillar

⁷ To the extent PO alleges that the “*conductive material*” in claims 1 and 9 and the “*conductive channel*” in claim 15 are mapped to the same component of Kang (which Petitioner does not concede), the alleged mapping aligns with PO’s own mapping of these limitations in the NDCA case. EX1023, Ex. C-2 at 23, 37-39.

406 faces the silicon nitride layers, but is electrically isolated from, the silicon nitride layers by the other one of the silicon oxide layer (“*a respective portion of the second dielectric*”). EX1003, ¶162.

Thus, Kang discloses or suggests [15.h].

From the foregoing, Kang anticipates or otherwise renders obvious claim 15.

M. Dependent Claim 16

Kang renders obvious that “*the first and second memory elements comprise polysilicon,*” additionally required by claim 16.

Kang discloses silicon nitride layers (or silicon oxynitride layers) of charge storage layers 411 (“*the first and second memory elements*”). EX1004, [0038]. A POSITA would have found replacing the silicon nitride layer with a polysilicon silicon layer is merely an obvious design choice from the only three possible materials—polysilicon, silicon nitride, and silicon oxynitride—that “trap charges to store data” in 3D NAND memory devices, as known in the art at the time of the invention. EX1020, Table 1; EX1021, 2847, §I; EX1022, 189; EX1003, ¶165.

A POSITA would also have found it obvious to replace silicon nitride or silicon oxynitride with polysilicon to form an OPO structure for charge storage layer 411 because a POSITA would have recognized that polysilicon was commonly used for memory elements at the time of invention due to silicon nitride and silicon oxynitride’s reliability issues, as well as polysilicon’s better long-term data retention.

EX1009, [0080]; EX1010, 1:46-56, 5:26-50; EX1012, 3; EX1014; EX1003, ¶¶167-170.

N. Dependent Claims 17 and 18

Kang further discloses that “*the first and second memory elements comprise a dielectric material,*” additionally required by claim 17, and that “*the dielectric material comprises silicon nitride,*” additionally required by claim 18. Specifically, Kang discloses a silicon nitride layer in charge trapping layer 411/111 used to “trap charges to store data” (and thus, “*first and second memory elements*”). EX1004, [0038]; EX1003, ¶172.

O. Dependent Claim 19

Kang further discloses “*dielectric material between the first and second conductive materials,*” additionally required by claim 19. Specifically, Kang discloses that insulating layers 460/260 filling trenches 240 between control gates 430b-430e (“*first and second conductive materials*”) in different device levels. EX1004, [0087], [0101]; EX1003, ¶173.

P. Dependent Claim 20

Kang further discloses, “*a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate,*” additionally required by claim 20.

Kang discloses that bit line 494 (“*data line*”) is configured to be selectively

coupled to active pillar 406 via the upper select transistor. Section VII.B.5. Thus, a POSITA would have understood, or at least found it obvious, that data line 494 is also configured to be selectively coupled to the vertical outermost layer of active pillar 406 (“*conductive channel*”). EX1003, ¶175.

Kang further discloses that the silicon nitride layers of the first and second groups of memory transistors (“*first and second memory elements*”) are located vertically between bit line 496 and semiconductor substrate 402. EX1004, FIG. 1E; EX1003, ¶176.

VIII. GROUND 3: KANG IN VIEW OF AHN RENDERS OBVIOUS CLAIM 16

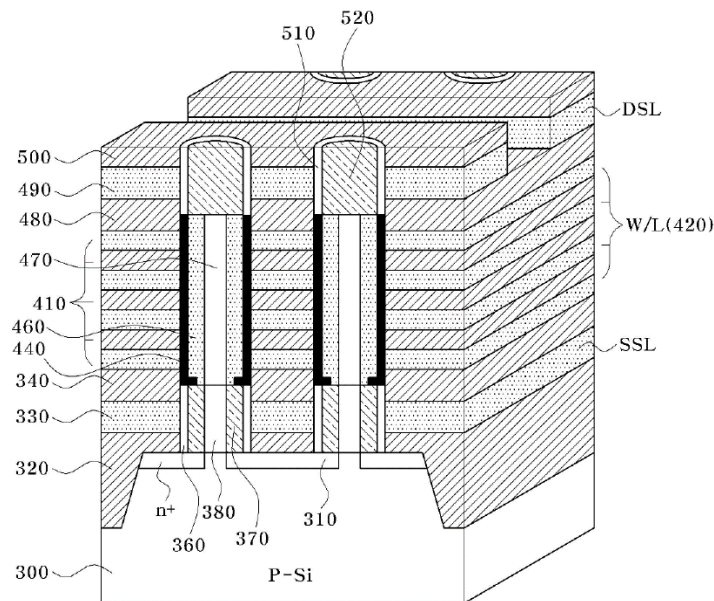
A. Overview of Ahn

Ahn relates to 3D flash memory device manufacturing, allowing higher integration density due to the vertical memory cell arrangement. EX1006, [0002], [0022]. Ahn’s memory device includes “cell strings[] arranged vertically on a substrate,” and each cell string includes “source select transistor, a plurality of memory cells, and a drain select transistor.” EX1006, [0026].

As shown in Ahn’s FIG. 12 reproduced below, Ahn’s memory device includes a channel region (460) (“*conductive channel*”) by which memory cells are formed, and “an ONO dielectric layer (440) for charge storage, *i.e.*, a blocking layer, a charge trap layer, and a tunneling layer, [which] are sequentially formed on the inner wall

of the above through hole (330).” EX1006, [0052], [0065]. EX1003, ¶78. Ahn further discloses that through holes (430) (“*cavities*”) through which channel region (460) is formed passes through conductive layers (420) (“*control gates*”), and that the charge trap layer (“*memory element*”) of ONO dielectric layer (440) including “a silicon nitride film or a polysilicon film” is “formed on the inner wall” of through hole (430) in each conductive layer (420). EX1006, [0064]-[0067]; EX1003, ¶79.

Figure 12



B. Dependent Claim 16

As discussed in Section VII.L, Kang anticipates or otherwise renders obvious claim 15 on which claim 16 depends. Should the Board find Kang alone does not render obvious claim 16, Ahn is introduced in this Ground.

Kang discloses “*the first and second memory elements*” being silicon nitride layers or silicon oxynitride layers. EX1004, [0038].

Ahn explicitly teaches that “a charge trap layer is formed by depositing, for example, a silicon nitride film **or a polysilicon film** to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (430). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD).” EX1006, [0067].

Kang and Ahn are analogous art in the same field as the '214 patent, which is related to nonvolatile memory devices. EX1001, 1:6-8; 2:63-67; EX1004, [0002]; EX1006, [0001]. Also, both Kang and Ahn are pertinent to the purported problem addressed by the '214 patent, *e.g.*, increasing integration or density of memory devices. EX1001, 1:7-22; EX1004, [0003]-[0004]; EX1006, [0005]. EX1003, ¶180. It would have been obvious to apply Ahn's teachings of a polysilicon charge trap layer to Kang's charge storage layer 411 because polysilicon was commonly used for memory elements at the time of the invention, and it is a mere design choice to select from polysilicon, silicon nitride, and silicon oxynitride as the material to form the charge trap layer. EX1003, ¶181.

A POSITA also would have been motivated to replace the silicon nitride layer with Ahn's polysilicon layer in Kang's charge storage layer 411 because, at the time of the invention, polysilicon has better reliability and data retention than silicon nitride used in the flash memory devices. EX1003, ¶182; Section VII.M.

A POSITA would have had a reasonable expectation of success for replacing the silicon nitride layer with Ahn's polysilicon layer in Kang's charge storage layer 411. EX1003, ¶183. Ahn discloses its charge trap layer inside the ONO layer is "formed by depositing, for example, a silicon nitride film or a polysilicon film," noting the interchangeability of the two materials of its charge trap layer. EX1006, [0067]. Ahn also provides specific examples of deposition parameters (*e.g.*, "a thickness of 10 to 1,000 Å") and deposition methods (*e.g.*, atomic layer deposition (ALD) or chemical vapor deposition (CVD)) for forming its polysilicon charge trap layer. EX1006, [0067]; EX1003, ¶184. A POSITA would have thus found it routine and straightforward to apply Ahn's teachings of using a polysilicon memory element to replace the silicon nitride in Kang's charge storage layer 411, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality. EX1003, ¶185.

IX. GROUNDS 4 AND 5: FUKUZUMI ANTICIPATES OR OTHERWISE RENDERS OBVIOUS CLAIMS 1-7, 9-12, AND 14-20

A. Overview of Fukuzumi

Fukuzumi relates to a nonvolatile semiconductor memory device. EX1007, [0002]. Fukuzumi aims to overcome problems encountered in transferring semiconductor memory devices from 2D to 3D. EX1007, [0003], [0040].

Annotated FIG. 2 below shows a perspective view of a nonvolatile

As shown in the figures above, nonvolatile semiconductor memory device 100 includes a matrix of memory strings MS including memory cells MTr_{1mn} - MTr_{4mn} , where m and n indicate the memory cells' X- and Y-coordinates. EX1007, [0079]. Each memory string MS includes columnar semiconductor CL_{mn} (in pink) including source-side columnar semiconductor layer 25 formed on a substrate Ba (in gray), memory 38 (in pink), and drain-side columnar semiconductor layer 45 connecting bit line layer 47 (in green) and memory 38. EX1007, [0086], [0088]-[0089], [0096], [0103], [0108]-[0109]; EX1003, ¶82.

Memory cells MTr_{1mn} - MTr_{4mn} include memory 38 of columnar semiconductor CL_{mn} , portions of word lines WL1-WL4 (in brown and orange, *e.g.*, word line conduction layer 36*a-d*) that are connected to each gate of the memory cells, and charge storage layer 39*b* (in red) formed on sidewalls of word lines WL1-WL4 in memory hole 37 (in blue). EX1007, [0080], [0085], [0087]; EX1003, ¶83. Drain-side selection transistors $SDTr_{mn}$, including portions of the drain-side selection gate lines SGD, are at the upper parts of memory strings MS; source-side selection transistors $SSTr_{mn}$, including portions of the source-side selection gate lines SGS, are at the lower parts of memory strings MS. EX1007, [0082]-[0083], [0088]-[0089]; EX1003, ¶83.

Fukuzumi also discloses a second embodiment shown in FIG. 28, which is different from the first embodiment only by “a configuration of a memory layer 30b

as compare[d] with the memory layer 30 in the first embodiment,” while “the same or similar reference numerals in the second embodiment are applied to the same or similar parts and elements throughout the drawings as the first embodiment.” EX1007, [0146]-[0147]; EX1003, ¶84.

According to Fukuzumi, the nonvolatile semiconductor memory devices of the first and second embodiments, both have “an effect of higher integration and lower cost on the nonvolatile semiconductor memory device.” EX1007, [0144], [0150].

B. Independent Claim 1

1. Fukuzumi discloses [1.P].

Fukuzumi discloses a nonvolatile semiconductor memory device (“*[a]n apparatus*”). EX1007, [0073]. Thus, Fukuzumi discloses [1.P].

2. Fukuzumi discloses [1.a].

Fukuzumi discloses a semiconductor substrate Ba (“*a substrate*”) of a nonvolatile semiconductor memory device 100⁸ (“*a memory device*”). EX1007, [0078], [0081]; EX1003, ¶188. Thus, Fukuzumi discloses [1.a].

⁸ As explained in Section IX.A, although Fukuzumi describes nonvolatile semiconductor memory device 100 and its accompanying figures, including FIG. 2 cited in Grounds 4-7, in the context of the first embodiment, unless otherwise specified (*e.g.*, with respect to memory layer 30 and word line conduction layers 36), the disclosures regarding nonvolatile semiconductor memory device 100 are equally applicable to the second embodiment as well. EX1007, [0146]-[0148]; EX1003, ¶189.

3. Fukuzumi discloses [1.b] and [1.c].

Fukuzumi discloses that nonvolatile semiconductor memory device 100 also includes memory cell strings MS each including memory cells MTr1 mn -MTr4 mn vertically and serially connected to each other. EX1007, [0079]-[0080], [0085]. Thus, as shown in annotated FIG. 2 below, first memory cells MTr1 mn (in brown dashed box, “*a plurality of first memory cells*”) are located in a first level of nonvolatile semiconductor memory device 100 over semiconductor substrate Ba (in gray), and second memory cells MTr2 mn (in orange dashed box, “*a plurality of second memory cells*”) are located in a second level of nonvolatile semiconductor memory device 100 over both the first device level and semiconductor substrate Ba. EX1007, [0077], [0081]; EX1003, ¶191. Thus, Fukuzumi discloses [1.b] and [1.c].

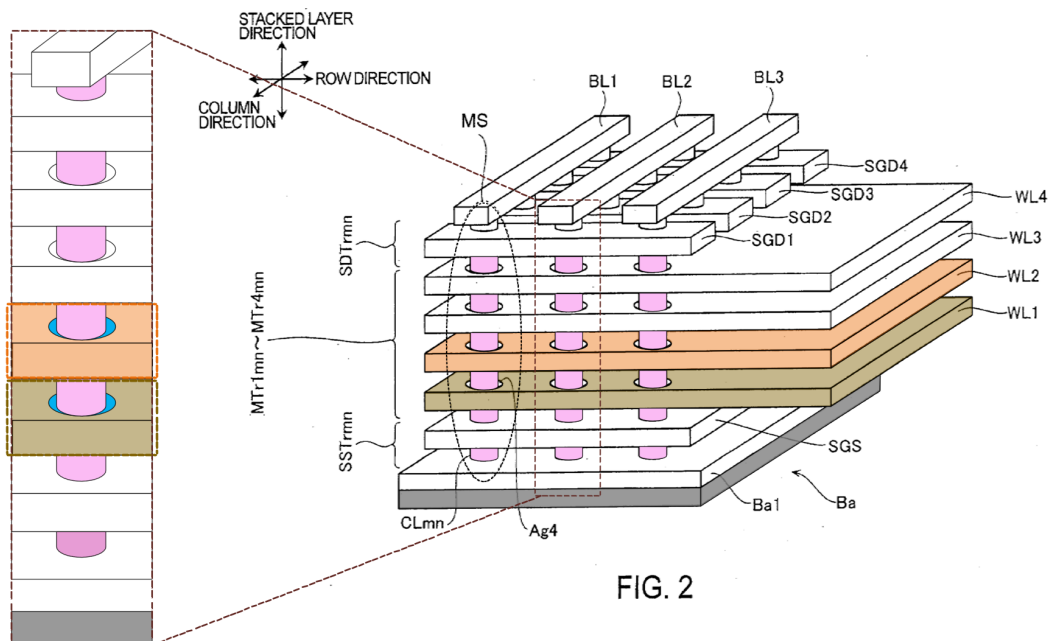


FIG. 2

EX1003 — FIG. AB

4. Fukuzumi discloses [1.d] and [1.e].

Fukuzumi discloses that the nonvolatile semiconductor memory device 100 includes vertically stacked word lines WL1–WL4 (*e.g.*, first–fourth word line conduction layers 36*a*–36*d* in the first embodiment or 361*a*–361*d* in the second embodiment). EX1007, [0101], [0148]. Each word line WL has a plane structure extending two-dimensionally and is connected to the gate of a corresponding layer of memory cells MTr1*mn*–MTr4*mn* within each memory string MS, with its end portions functioning as the control gates of the respective memory cells. EX1007, [0077], [0080], [0087], [0101], [0148]; EX1003, ¶193. Fukuzumi also discloses “word line driving circuit 13 controls voltage applied to a word line WL” and has “a function as control circuits controlling the memory strings MS.” EX1007, [0076], [0090].

As further shown in annotated FIGs. 2 and 28 below, Fukuzumi discloses a first word line WL1 (in brown, *e.g.*, first word line conduction layer 361*a*) in the first device level (“*a first control gate formed in the first device level*”) to control access to first memory cells MTr1*mn* in the first device level, and a second word line WL2 (in orange, *e.g.*, second word line conduction layer 361*b*) in the second device level (“*a second control gate formed in the second device level*”) to control access to second memory cells MTr2*mn* in the second device level. EX1003, ¶195.

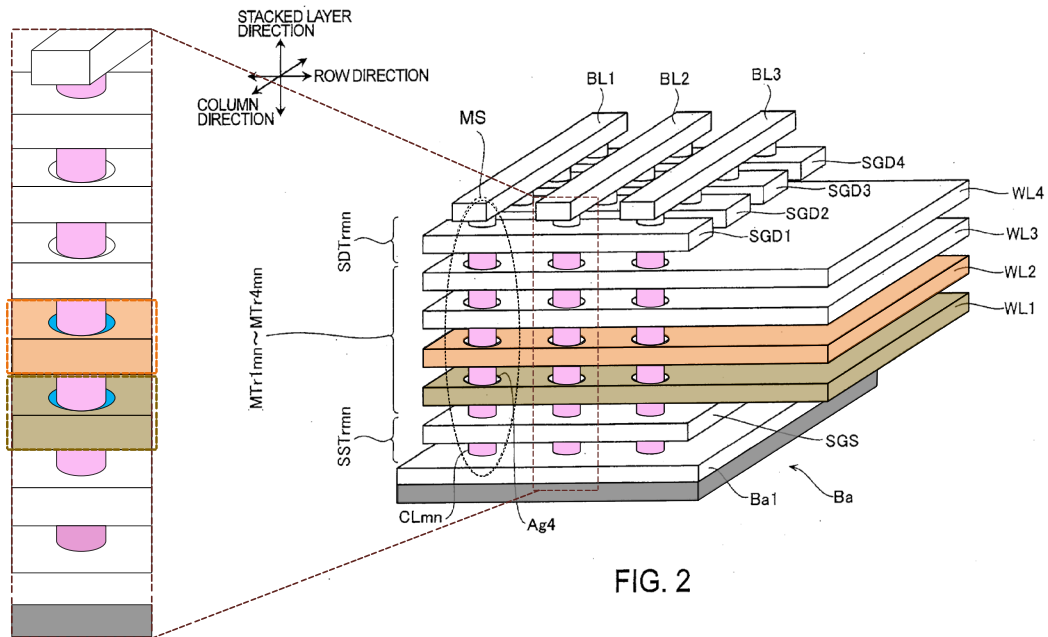


FIG. 2

EX1003 — FIG. AC

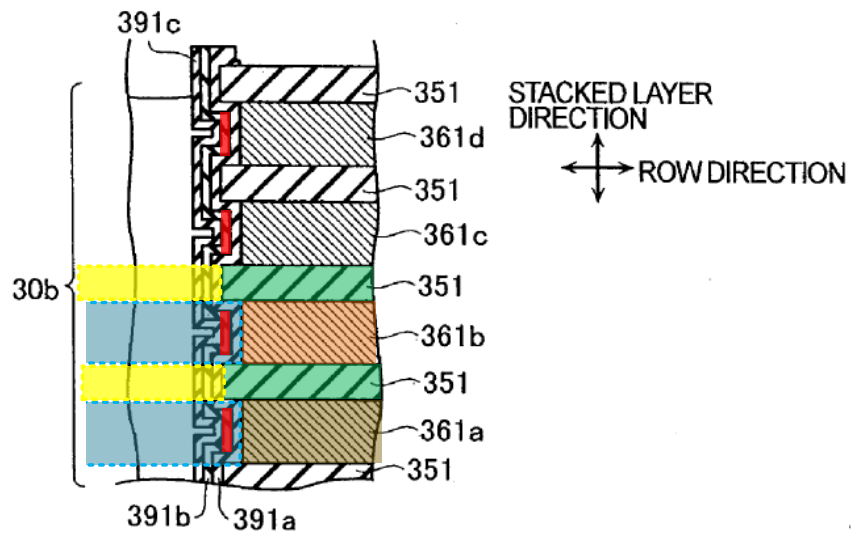


FIG. 28

EX1003 — FIG. AD

Further, Fukuzumi discloses that each memory cell MTr1 mn or MTr2 mn (“*each of the first/second memory cells*”) includes a charge storage layer 39 b /391 b ⁹, formed of silicon nitride, where memory 38 performs data writing and reading. EX1007, [0114], [0148], [0151]. Thus, a POSITA would have understood that charge storage layer 391 b is “*a memory element*.” EX1003, ¶196. Since Fukuzumi also discloses charge storage layer 39 b /391 b being formed in memory hole 37 passing through word line conduction layers 36 a /361 a -36 d /361 d , as shown in FIG. 28 above, a POSITA would have understood that Fukuzumi discloses that charge storage layer 391 b (in red) is formed in memory hole 37 (in blue, “*a cavity of the first/second control gate*”). EX1007, [0103]-[0104], [0148], FIG. 4; EX1003, ¶197.

As discussed in Section VI, to the extent that “*cavity*” requires a hole in the control gate to have a larger diameter than the holes in the layers above and below the control gate, memory hole 37 still qualifies as “*cavity*” as Fukuzumi specifically discloses that charge storage layers 391 b “are formed as the concavo-convex shape accompanying with the first-fourth word line conduction layer 361 a -361 d ,” and that “sidewall of first-fourth word line conduction layers 361 a -361 d faced to the fourth space Ag4 are formed as recesses corresponding to a side wall of an interlayer

⁹ Although Fukuzumi discloses the material and function of charge storage layer with respect to “39 b ” in the first embodiment, a POSITA would have understood that the same disclosures are equally applicable to “391 b ” in the second embodiment. EX1007, [0146]; EX1003, ¶196.

insulator 351.” EX1007, [0148], [0151].

Thus, a POSITA would have understood that, as illustrated in annotated FIG. 28 below, memory holes 37 (in blue) in each of word line conduction layers 361a and 361b have a diameter larger than memory holes 37 (in yellow) in interlayer insulators 351 (in green) above and below the respective word line conduction layer 361a or 361b. EX1003, ¶198. Thus, Fukuzumi discloses the “cavity” limitation under either party’s construction.

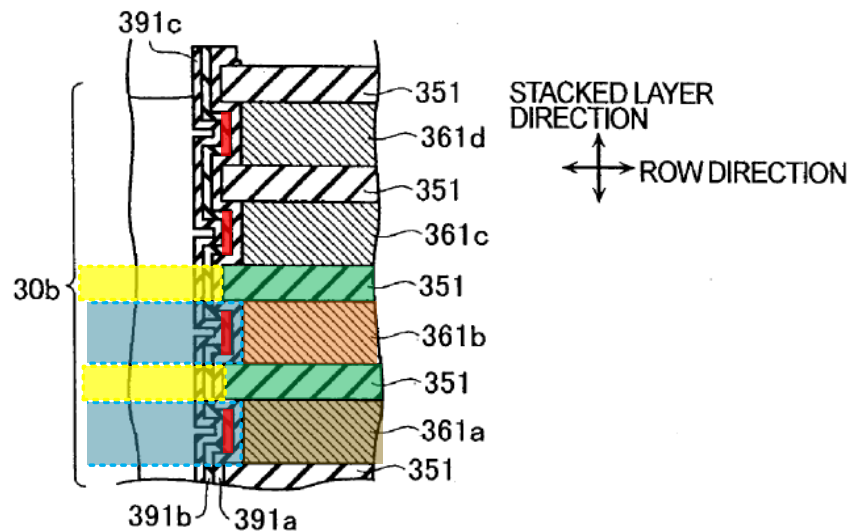


FIG. 28

EX1003 — FIG. AD

Accordingly, Fukuzumi discloses [1.d] and [1.e].

5. Fukuzumi discloses or suggests [1.f].

As shown in annotated FIG. 2 below, Fukuzumi discloses bit lines BL (in

green, “data lines”) electrically connected to a p-well region Ba1 (in purple) and memory cells Mtrmn through columnar semiconductor CLmn (in pink). EX1007, [0081], [0109]; EX1001, 3:29-31; EX1003, ¶201. Since Fukuzumi discloses “[e]ach of the memory strings MS includes columnar semiconductors CLmn on a p-well region Ba1 formed in an n+ region of a semiconductor substrate Ba” and “source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba,” p-well region Ba1 is a “common source” of multiple memory strings MS. EX1007, [0081], [0086]; EX1003, ¶202.

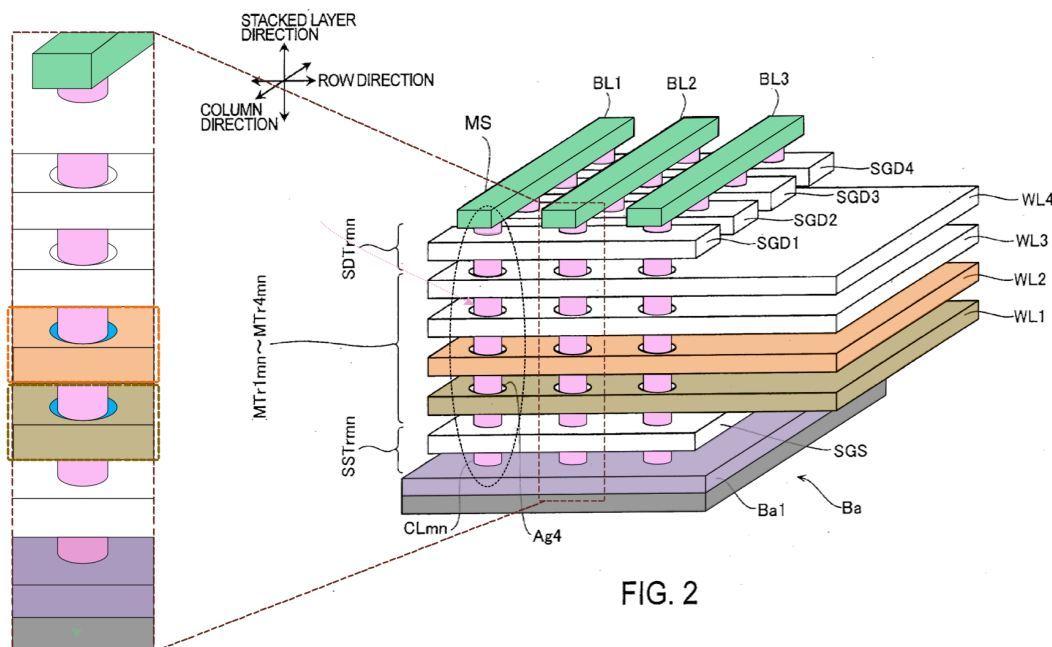


FIG. 2

EX1003 — FIG. AE

Fukuzumi also discloses bit lines BL being electrically connected to columnar semiconductor CLmn via drain-side selection transistor SDTrmn, which includes drain-side selection gate lines SGD electrically connected and controlled by drain-

side selection gate line SGD driving circuit 15. EX1007, [0076], [0083], [0085], [0089]; EX1003, ¶203. A POSITA would have understood that bit lines BL are coupled with memory cells *Mtrmn* and p-well region Ba1 through drain-side selection transistor *SDTrmn*, and that drain-side selection gate line SGD driving circuit 15 selects/deselects each memory string MS by turning drain-side selection transistor *SDTrmn* on or off to control the connections between bit lines BL and memory cells *Mtrmn*, through drain-side selection gate lines SGD. EX1007, [0076]; EX1003, ¶203. Therefore, Fukuzumi discloses that bit lines BL are configured to be “*selectively*” coupled to memory cells *Mtrmn* and p-well region Ba1 through columnar semiconductor *CLmn*. EX1003, ¶203.

Further, Fukuzumi discloses that memory 38, which is part of columnar semiconductor *CLmn* in the first and second embodiments, is formed of silicon. EX1007, [0103]. Thus, a POSITA would have understood, or at least found it obvious, that columnar semiconductor *CLmn* having silicon includes a “*conductive material*,” consistent with the ’214 patent. EX1001, 8:64-67; EX1003, ¶204.

Thus, Fukuzumi discloses or suggests [1.f].

From the foregoing, Fukuzumi anticipates or otherwise renders obvious claim 1.

C. Dependent Claim 2

Fukuzumi further discloses that “memory strings MS are also displaced like a

matrix in a plane perpendicular to the columnar semiconductors CL_{mn} .” EX1007, [0081], FIG. 2. Since Fukuzumi also discloses “memory strings MS being constituted with memory cells $MTr1_{mn}$ - $MTr4_{mn}$,” memory cells $MTr1_{mn}$ - $MTr4_{mn}$ are also arranged in a matrix (“*in a first direction*” and “*a second direction*”). EX1007, [0081]; EX1003, ¶206.

As Fukuzumi further discloses that columnar semiconductor CL_{mn} extends vertically through word lines WL1-WL4, including first and second word lines WL1 and WL2 in the first and second levels, columnar semiconductor CL_{mn} (“*conductive material*”) also extends through first and second memory cells $MTr1_{mn}$ and $MTr2_{mn}$ in the first and second levels in the vertical direction (“*a third direction*”) perpendicular to the matrix plane (“*the first and second directions*”) on which memory cells MTr_{mn} are formed. EX1007, [0081], FIG. 2; EX1003, ¶207.

Thus, Fukuzumi discloses or otherwise renders obvious the additional limitation required by claim 2.

D. Dependent Claim 3

Fukuzumi further discloses or otherwise renders obvious the additional limitation required by claim 3.

As shown in annotated FIG. 2 below, Fukuzumi discloses that p-well region Ba1 (in purple, “*common source*”) is over semiconductor substrate Ba (in gray) and below memory cells Mtr_{mn} and thus, is “*between the first and second memory cells*

and the substrate.” EX1007, [0081], [0086]; EX1003, ¶¶209-210.

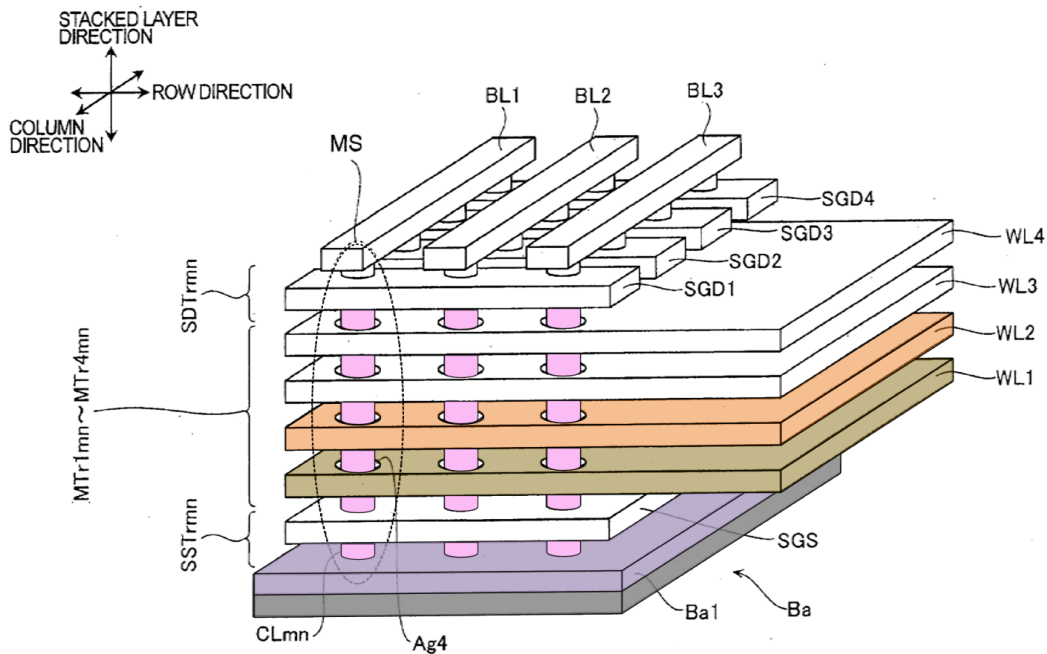


FIG. 2
EX1003 — FIG. AG

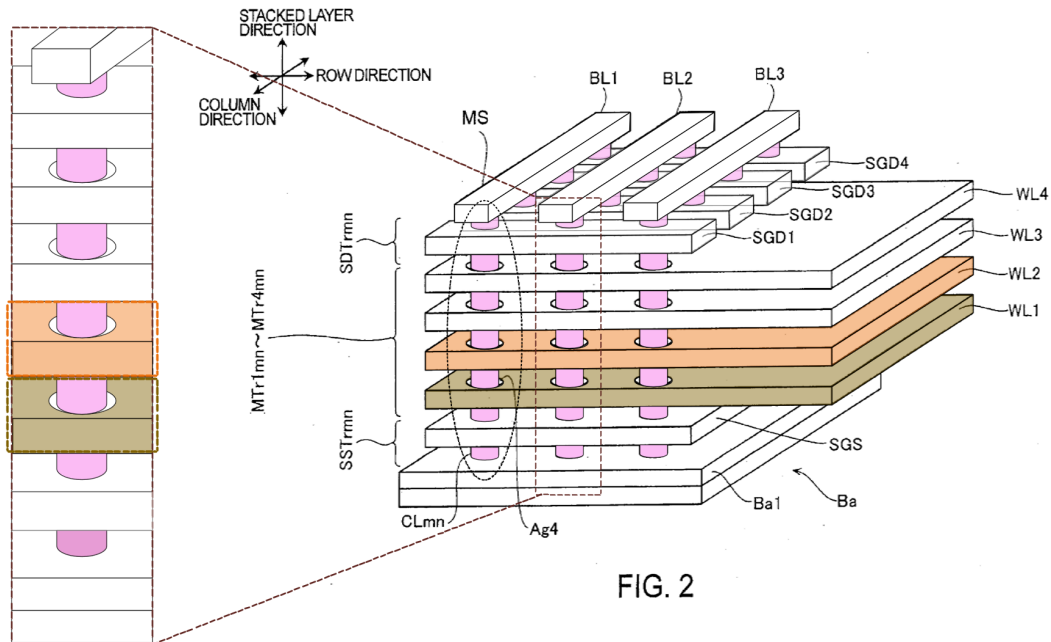
Fukuzumi further discloses “reading out data, writing in data and erasing data are performed by controlling electrical charges of the charge storage layer in the prescribed memory cell” and that “columnar semiconductor CLmn is formed on an n⁺-region formed in a p-type region (p-Well region) Ba1 of a semiconductor substrate Ba.” EX1007, [0086], [0090]. A POSITA would have understood, as common knowledge of a POSITA, that during the erasing operation of these memory devices, the electrons stored in charge storage layers 391b of memory cells MTr1mn-MTr4mn are to be discharged to (“moved to”) p-well region Ba1, so that they can be recombined with holes doped in the p-well. EX1004, [0048]; EX1003, ¶212.

Notably, the '214 patent characterizes the claimed erase operation as one of these operations that can be recognized by one skill in the art, of which the detailed descriptions are omitted to help focus on the description therein. EX1001, 3:54-64, 10:44-60; EX1003, ¶212.

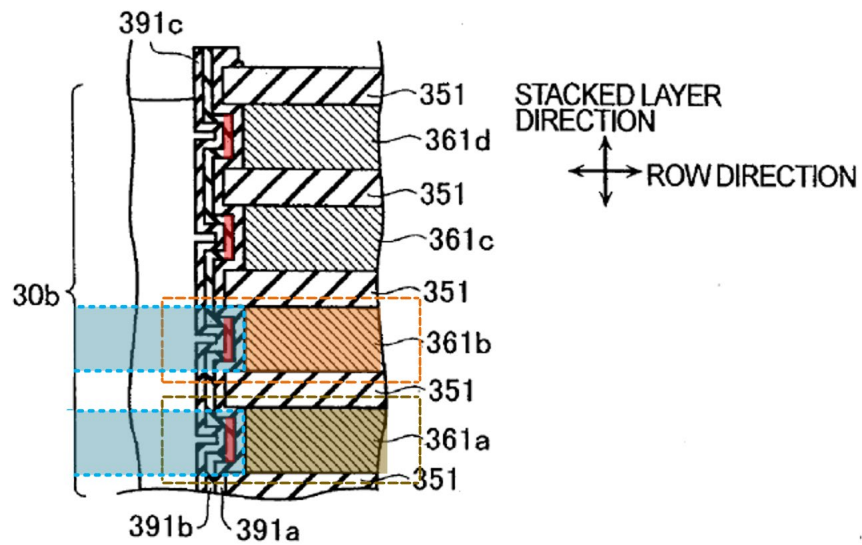
E. Dependent Claims 4 and 5

Fukuzumi further discloses the limitations additionally required by claims 4 and 5.

As shown in annotated FIGs. 2 and 28 below, Fukuzumi further discloses that memory cells $MTr1_{mn}$ - $MTr4_{mn}$ are vertically and serially connected to each other to form a memory string MS. EX1007, [0079]. Each columnar semiconductor CL_{mn} extends vertically, while charge storage layers 391*b* (in red, “*memory elements*”) are formed laterally between the recessed sidewalls of word line conduction layers 361*a*-361*d* and the sidewall of columnar semiconductor CL_{mn} . EX1007, [0081], [0148]; EX1003, ¶214. Therefore, a POSITA would have understood that memory cells $MTr1_{mn}$ - $MTr4_{mn}$ in each memory string MS are substantially vertically aligned, and charge storage layers 391*b* of memory cells $MTr1_{mn}$ - $MTr4_{mn}$ in each memory cell MS are also substantially vertically aligned. EX1003, ¶215.



EX1003 — FIG. AH



EX1003 — FIG. AI

F. Dependent Claim 6

Fukuzumi renders obvious the limitations additionally required by claim 6.

As discussed in Section IX.B.5, Fukuzumi discloses drain-side selection transistors *SDTrmn* to selectively couple memory cells *Mtrmn* (“*first and second memory cells*”) to bit lines BL (“*data lines*”) during memory operations. EX1007, [0076], [0083], [0085], [0089]; EX1003, ¶217. Thus, Fukuzumi discloses [6.a].

Regarding [6.b], Fukuzumi discloses “drain-side selection transistors *SDTrmn* include ... drain-side selection gate line SGD. ... An end portion of the drain-side selection gate line SGD contacting with the insulation layer acts as a control gate of each of the drain-side selection transistors *SDTrmn*” and “one end of the drain-side conductive layer 42 acts as a control gate of the drain-side selection transistor *SDTrmn* mentioned above.” EX1007, [0089], [0107]. A POSITA would have understood that drain-side conductive layer 42, one example of drain-side selection gate line SGD, includes the gate of drain-side selection transistor *SDTrmn*. EX1003, ¶218.

Fukuzumi’s third embodiment discloses a “slit” memory hole 371 where “both ends of the row direction in the memory hole 371 are formed like a line.” EX1007, [0155], FIG. 29. As illustrated in annotated FIG. 29 below, word line conduction layers 36*a-d* on two opposite long sides (in orange) of slit memory hole 371 (in blue) electrically interact with memory 38 (in pink), while portions (in dark

brown) of word line conduction layers 36a-d at the long ends of slit memory hole 371 are electrically isolated from and do not impact the operation of memory 38, thereby forming a “double-gate”. EX1007, [0155]; EX1003, ¶219.

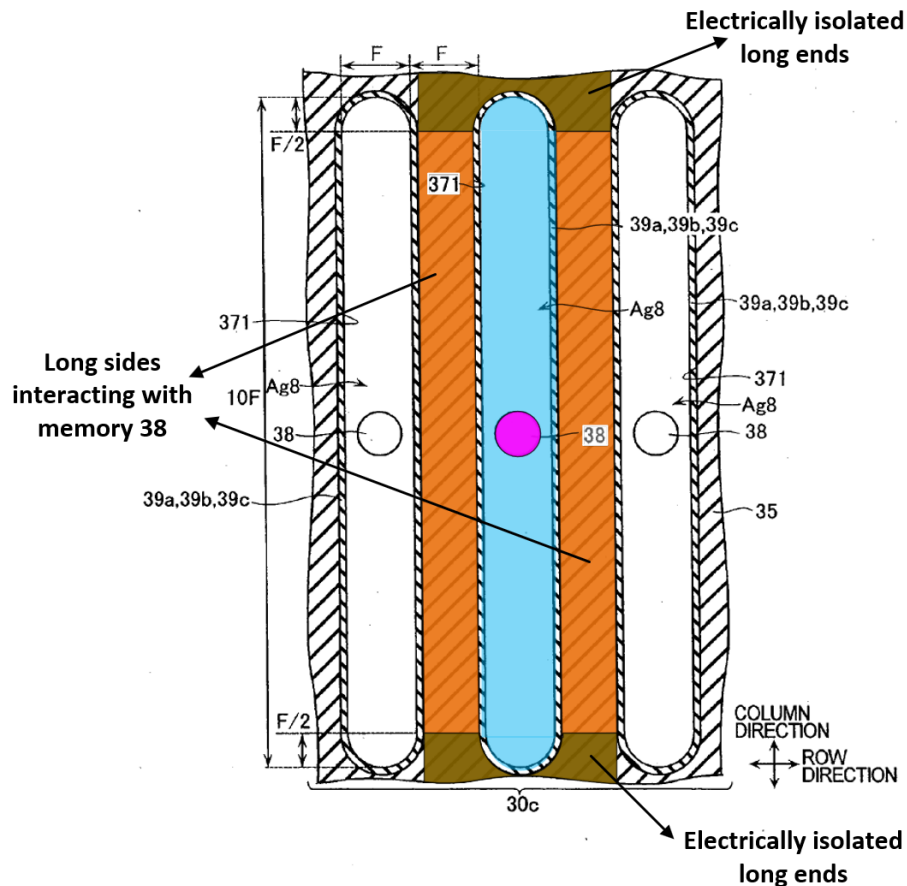
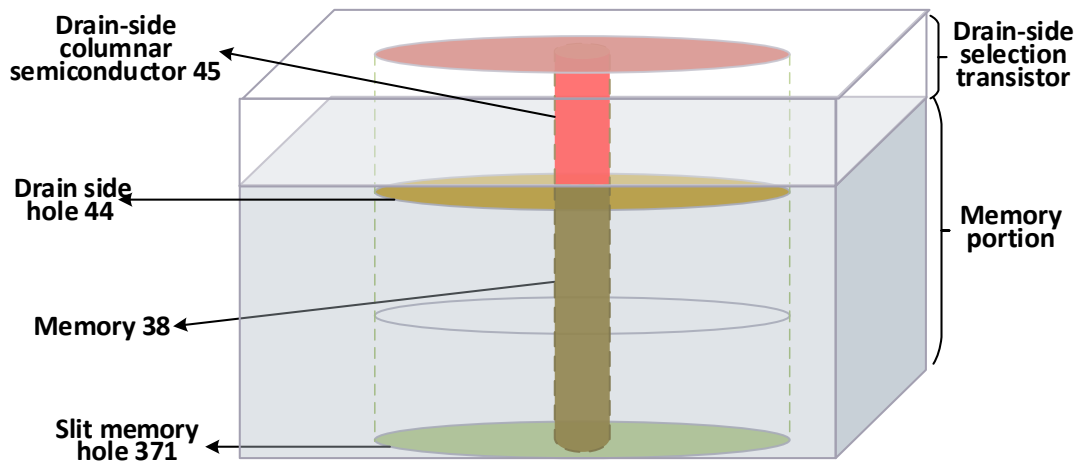


FIG. 29
EX1003 — FIG. AJ

A POSITA would have understood, or at least found it obvious, that the same slit structure would also be used for drain-side hole 44, as illustrated in FIG. AK of Kuhn Decl. below, such that drain-side conductive layer 42 (an example of drain-side selection gate line SGD) of drain-side selection transistor SDTrmn is a “double-gate.” EX1007, [0153], [0200]; EX1003, ¶220.



EX1003 — FIG. AK

Using the same slit memory hole structure for drain-side hole 44 would advantageously allow drain-side selection transistors $SDTrmn$ and memory cells $Mtrmn$ in a memory string MS to be formed using the same hole, thereby simplifying manufacturing. EX1018, [0034], [0036], [0042]-[0043], [0062], [0066]-[0067], [0142]; EX1003, ¶221. In this implementation, portions of drain-side gate insulation layer 46 separate the regions of drain-side conductive layer 42 from drain-side columnar semiconductor layer 45. EX1003, ¶221.

A POSITA would have had a reasonable expectation of success in applying the slit hole structure to the drain-side hole 44, as the use of such structure for drain-side selection transistors was well-known in the art. EX1015, [0103]-[0106], FIGs. 31, 36-37; EX1016, [0075]-[0080], FIG.11; EX1017, [0012]; EX1019, [0070], FIGs. 6-7, 12; EX1003, ¶222. Fukuzumi explains parts other than the slit memory hole structure omitted in the third embodiment are “the same or similar” as the first and

[0200]; FN 8.

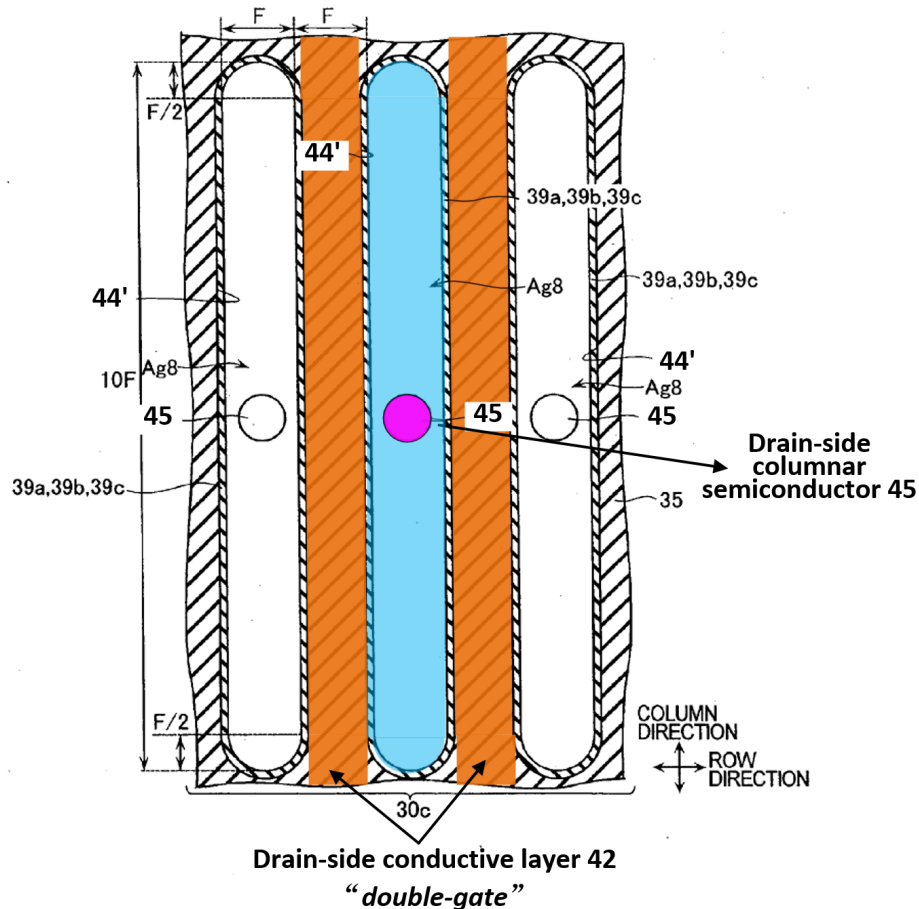


FIG. 29
EX1003 — FIG. AO
(Annotated and Modified FIG. 29 of Fukuzumi)

A POSITA would thus have understood, or at least found it obvious, that the analysis for other limitations relying on the first and second embodiments of Fukuzumi applies equally to Fukuzumi's third embodiment modified to include the modified slit drain-side hole 44' structure as shown above in a non-limiting example in FIG. AO of Kuhn Decl. EX1003, ¶223. As shown in modified FIG. 29 above, two

separate drain-side conductive layers 42 (in orange) on opposite sides of drain-side columnar semiconductor 45 (in pink) form a “*double-gate*” of drain-side selection transistor SDTrmn. EX1003, ¶224.

Accordingly, Fukuzumi renders obvious claim 6.

G. Dependent Claim 7

Claim 7 requires the same additional claim limitations as claim 6, except that the transistor includes “*a surrounded gate*.”

Fukuzumi further discloses, “drain-side selection transistors SDTrmn include the columnar semiconductors CLmn, the insulation layer **surrounding** the columnar semiconductor CLmn and the drain-side selection gate line SGD **surrounding** the insulation layer. ... end portion of the drain-side selection gate line SGD contacting with the insulation layer acts as a control **gate** of each of the drain-side selection transistors SDTrmn.” EX1007, [0088]-[0089]. Thus, Fukuzumi discloses drain-side selection transistor SDTrmn includes a “*surrounded gate*”—the end portion of drain-side selection gate line SGD. EX1003, ¶255.

Accordingly, Fukuzumi anticipates or otherwise renders obvious claim 7.

H. Independent Claim 9

1. Fukuzumi discloses [9.P].

As discussed in Section IX.B.1, Fukuzumi discloses [9.P].

2. Fukuzumi discloses or suggests [9.a] and [9.b].

As discussed in Sections IX.B.3 and IX.B.4, Fukuzumi discloses “*a plurality of first/second memory cells located in a first/second device level of the memory device over the substrate, wherein the first device level is different from the second device level,*” and “*each of the first/second memory cells includes a memory element.*”

Since first and second memory cells MTr1*mn* and MTr2*mn* discussed in Sections IX.B.3 and IX.B.4 are in **nonvolatile** semiconductor memory device 100, Fukuzumi also discloses a “*first non-volatile memory cell*” MTr1*mn*, and a “*second non-volatile memory cell*” MTr2*mn*. EX1007, [0080]; EX1003, ¶229.

Since Fukuzumi discloses “[e]ach of the memory cells Mtr*mn* includes the **columnar** semiconductor CL*mn*, the insulation layer surrounding the columnar semiconductor CL*mn* via the space Ag4 as shown in FIG. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) and the word line WL **surrounding** the insulation layer and the charge storage layer,” a POSITA would have understood, or at least found it obvious that, charge storage layer 391*b* (“*memory element*”) surrounding columnar semiconductor CL*mn*, e.g., a cylinder column, has “*a ring shape.*” EX1007, [0081], [0087], FIGs. 2, 7; EX1003, ¶¶230-231.

Thus, Fukuzumi discloses or suggests [9.a] and [9.b].

3. Fukuzumi discloses or suggests [9.c] and [9.d].

As discussed in Sections IX.B.5 and IX.C, Fukuzumi discloses or suggests “*data lines configured to be selectively coupled to a common source and the memory*

cells through conductive material” and “the conductive material extending through the first and second memory cells in a third direction.” Thus, Fukuzumi also discloses or suggests [9.c] and [9.d]. EX1003, ¶233.

From the foregoing, Fukuzumi anticipates or otherwise renders obvious claim 9.

I. Dependent Claim 10

Fukuzumi further discloses the additional limitations recited in claim 10.

As explained in Section IX.B.4, Fukuzumi discloses *“a first/second control gate formed in the first/second device level, the first/second control gate to control access to the first/second memory cells.”*

Fukuzumi specifically discloses that “[e]ach of the word lines WL1-WL4 is connected to each gate of the memory cells MTr1 mn -MTr4 mn in each of the memory strings MS and each of the word lines WL1-WL4 are formed of the same conductive layer and are common in plane each other.” EX1007, [0080]. As examples of word lines WL1-WL4, first and second word line conduction layers 361 a and 361 b are thus *“a first/second additional conductive material configured to operate as a control gate to access the first/second memory cell.”* EX1003, ¶235.

J. Dependent Claims 11 and 12

Fukuzumi further discloses or suggests the additional limitations required by

claims 11 and 12.

Fukuzumi discloses, “[e]ach of the memory cells $Mtrmn$ includes the columnar semiconductor $CLmn$, the insulation layer surrounding the columnar semiconductor $CLmn$ via the space $Ag4$ as shown in FIG. 2, a charge storage layer (not illustrated in FIGs. 2-3) and the word line WL surrounding the insulation layer and the charge storage layer.” EX1007, [0087]. As examples of the insulation layer and charge storage layer surrounding columnar semiconductor $CLmn$ and surrounded by the word line WL, Fukuzumi specifically discloses “surfaces of a block insulation layer 391a, a charge storage layer 391b and a tunnel insulation layer 391c faced to the fourth space $Ag4$.” EX1007, [0148]; EX1003, ¶237.

Thus, as shown in annotated FIG. 28 below, Fukuzumi discloses that each memory cell $Mtrmn$ includes: (i) tunnel insulation layer 391c (in green, “*a first dielectric*”) between a respective charge storage layer 391b (in red, “*memory element*”) and columnar semiconductor $CLmn$ (in pink, “*conductive material*”), and (ii) block insulation layer 391a (in yellow, “*a second dielectric*”) between the respective charge storage layer 391b and the respective word line conduction layer 361b or 361c (in brown or orange, “*additional conductive material*”). EX1003, ¶238.

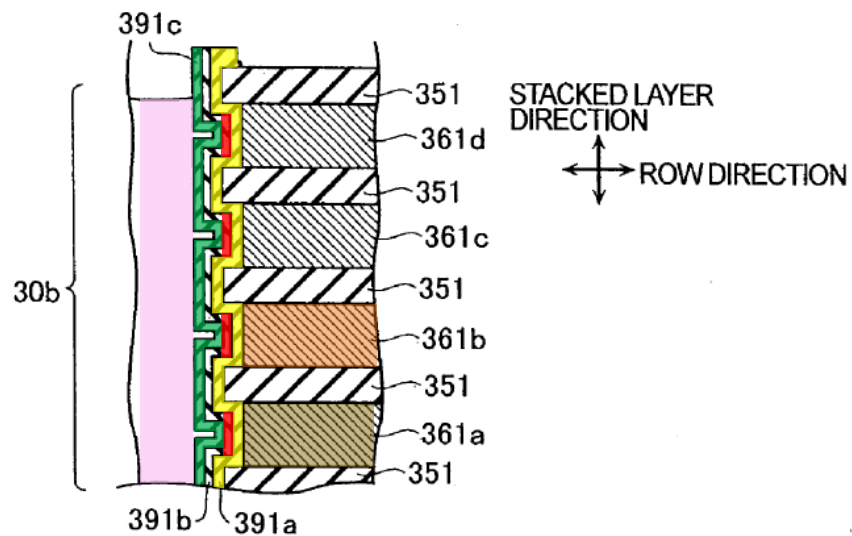


FIG. 28

EX1003 — FIG. AQ

K. Dependent Claim 14

Fukuzumi further discloses that “*the first and second memory cells are located between the substrate and the data line,*” additionally required by claim 14. As shown in annotated FIG. 2 below, Fukuzumi discloses that memory cells *Mtrmn* are located vertically between semiconductor substrate Ba (in gray) and bit lines BL (in green). EX1007, [0081], [0109]; EX1003, ¶240.

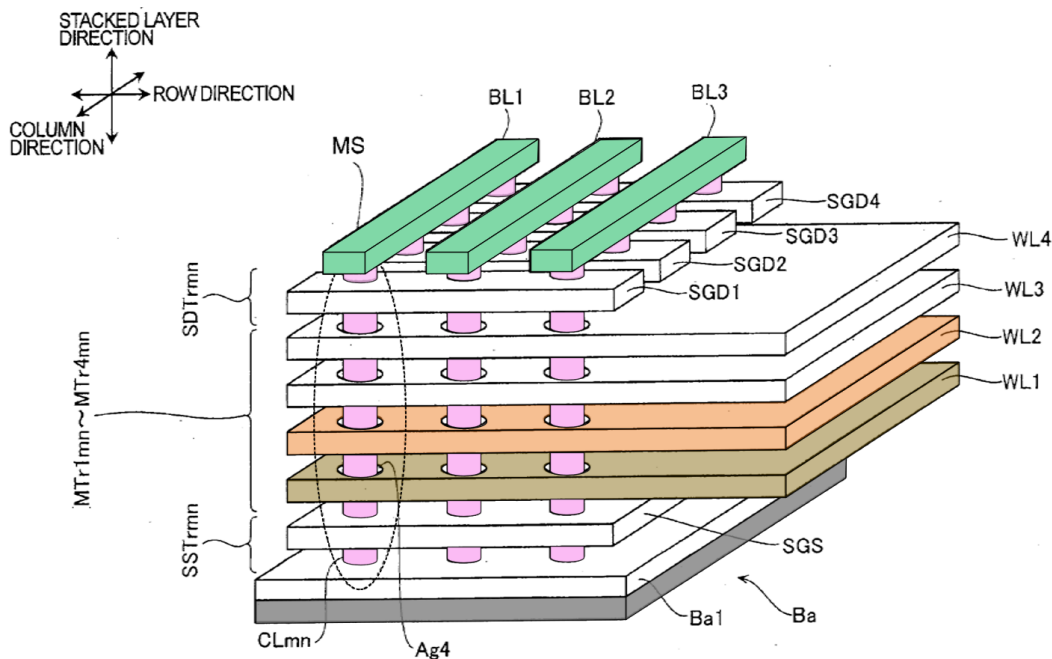


FIG. 2
EX1003 — FIG. AR

L. Independent Claim 15

1. Fukuzumi discloses [15.P].

Fukuzumi discloses [15.P], which is the same as [1.P]. Section IX.B.1.

2. Fukuzumi discloses [15.a].

Fukuzumi discloses [15.a], which is the same as [1.a]. Section IX.B.2.

3. Fukuzumi discloses [15.b] and [15.c].

As discussed in Sections IX.B.3-IX.B.4, Fukuzumi discloses “a first/second control gate formed in the first/second device level,” “a cavity of the first/second control gate,” and “the first device level is different from the second device level.”

Fukuzumi specifically discloses that “[e]ach of the word lines WL1-WL4 is connected to each gate of the memory cells MTr1mn-MTr4mn in each of the memory

strings MS and each of the word lines WL1-WL4 are formed of the same **conductive layer** and are common in plane each other.” EX1007, [0080]. As examples of word lines WL1-WL4, first and second word line conduction layers 361a and 361b are thus “*first and second conductive materials*,” consistent with the ’214 patent. EX1001, 7:3-5, 39-42; EX1003, ¶244.

As shown in annotated FIGs. 2 and 28 below, a POSITA would have understood that each portion of memory hole 37 (in blue, “*first/second cavity*”), in which charge storage layer 311b (in red, “*first/second memory element*”) is formed, has a respective sidewall (“*a first/second sidewall*”) on first or second conductive layer 361a or 361b (in brown or orange) under either party’s interpretation of “*cavity*.” EX1003, ¶245; Section IX.B.4.

Thus, Fukuzumi discloses [15.b] and [15.c].

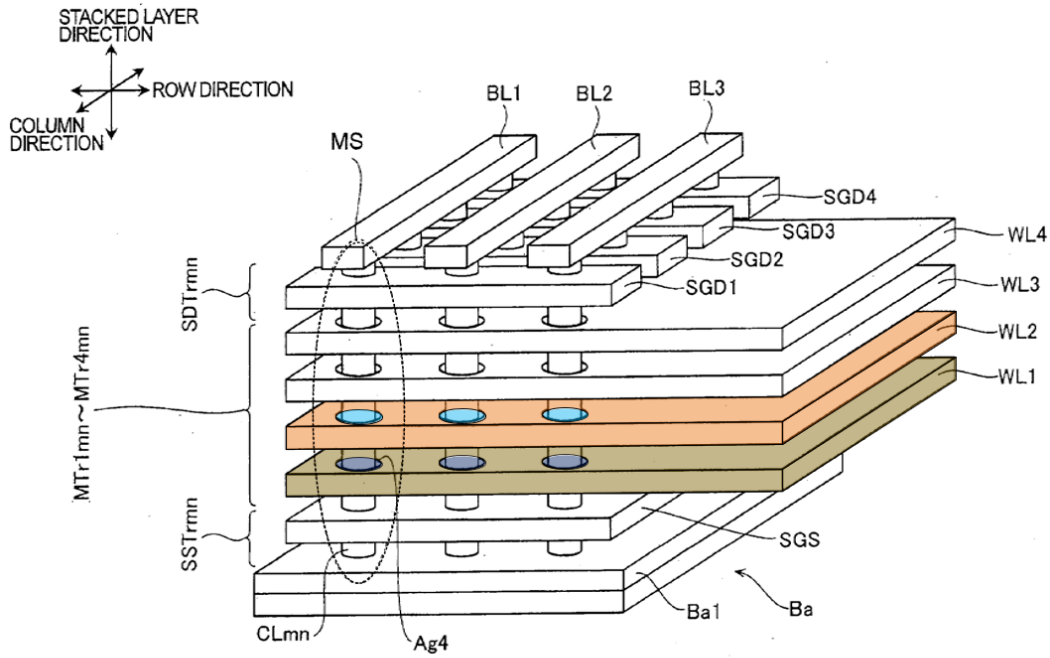


FIG. 2
EX1003 — FIG. AS

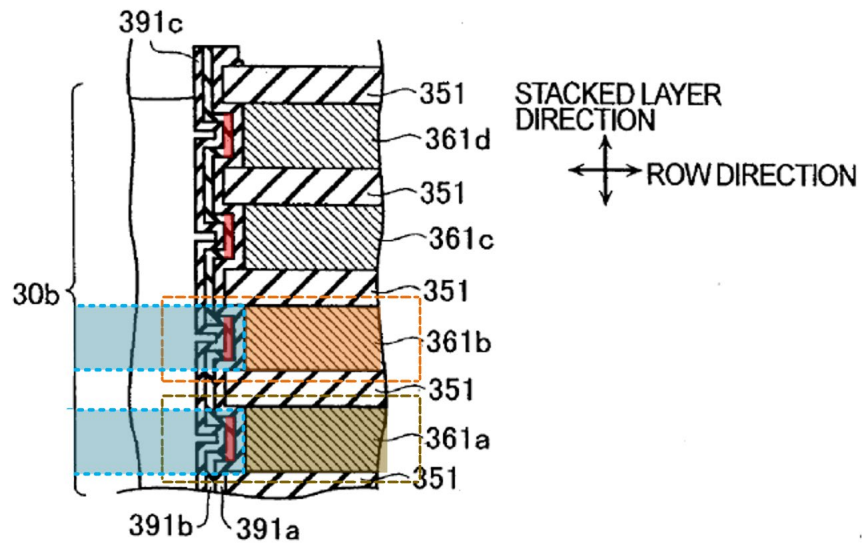


FIG. 28
EX1003 — FIG. AT

4. Fukuzumi discloses [15.d], [15.e], [15.f], and [15.g].

As discussed in Section IX.B.4, Fukuzumi also discloses that “*each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.*”

Fukuzumi discloses, “[e]ach of the memory cells M_{trmn} includes the columnar semiconductor CL_{mn} , the insulation layer surrounding the columnar semiconductor CL_{mn} via the space Ag_4 as shown in FIG. 2, a charge storage layer (not illustrated in FIGs. 2-3) and the word line WL surrounding the insulation layer and the charge storage layer.” EX1007, [0087]. As examples of the insulation layer and charge storage layer surrounding columnar semiconductor CL_{mn} and surrounded by word line WL, Fukuzumi specifically discloses “surfaces of a block insulation layer 391a, a charge storage layer 391b and a tunnel insulation layer 391c faced to the fourth space Ag_4 .” EX1007, [0148]; EX1003, ¶248.

Thus, as shown in annotated FIG. 28 below, Fukuzumi discloses block insulation layer 391a (in yellow, “*first dielectric*”) formed on the sidewalls of memory hole 37 (in blue, “*first/second cavity*”), and tunneling insulation layer 391c (in green, “*second dielectric*”) formed on the sides of charge storage layers 391b (in red, “*first/second elements*”). EX1003, ¶249; Section IX.J.

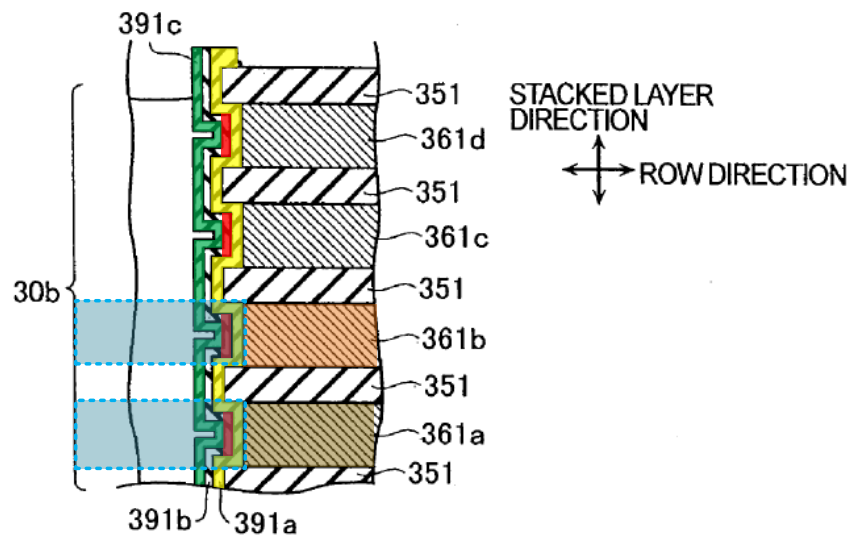


FIG. 28

EX1003 — FIG. AU

A POSITA would have understood, or at least found it obvious, that charge storage layer 391b is electrically isolated from the respective first or second word line conduction layer 361a or 361b (in brown and orange, “*first/second conductive material*”) by a respective portion of block insulation layer 391a (in yellow, “*a first/second portion of the first dielectric*”). EX1003, ¶250; Section IX.J.

Therefore, Fukuzumi discloses [15.d]-[15.g].

5. Fukuzumi discloses or suggests [15.h].

Fukuzumi discloses each memory string MS includes columnar semiconductor CL_{mn}, and the source and drain of the memory string MS are formed in columnar semiconductor CL_{mn}. EX1007, [0081], [0085], [0087]. Regarding

memory 38, which is part of columnar semiconductor CL_{mn} in the first and second embodiments, Fukuzumi discloses that “when the fourth word line conduction layer 36*d* is applied to voltage, the memory 38 is performed to write in data into the approached portion of the charge storage layer 39*b* and read out data from the approached portion of the charge storage layer 39*b*.” EX1007, [0114]; EX1003, ¶252.

A POSITA would have understood that, during certain operations of Fukuzumi’s memory device, a channel of memory string MS forms in the vertical outermost layer of columnar semiconductor CL_{mn} and does not extend throughout the entire columnar semiconductor CL_{mn} . EX1015, [0063], [0070], FIG. 11; EX1003, ¶¶253-254. Thus, Fukuzumi discloses “*a conductive channel*.”¹⁰

Fukuzumi further discloses that columnar semiconductor CL_{mn} extends vertically through word lines, including first and second word lines WL in the first and second device levels. EX1007, [0081], FIG. 2. Thus, Fukuzumi discloses that columnar semiconductor CL_{mn} , including its vertical outermost layer (“*conductive channel*”), extends from the first device level to the second device level. EX1003, ¶255.

As discussed in Sections IX.J and IX.L.4 and further shown in annotated FIG.

¹⁰ To the extent PO alleges that the “*conductive material*” in claims 1 and 9 and the “*conductive channel*” in claim 15 are mapped to the same component of Fukuzumi (which Petitioner does not concede), the alleged mapping aligns with PO’s own mapping of these limitations in the NDCA case. EX1023, Ex. C-2 at 23, 37-39.

28 below, a POSITA would further have understood, or at least found it obvious, that tunneling insulation layer 391c (in green, “*second dielectric*”) is formed laterally between charge storage layers 391b (in red, “*first/second memory elements*”) and the vertical outermost layer of columnar semiconductor CL_{mn} (in black, “*conductive channel*”), such that the vertical outermost layer of columnar semiconductor CL_{mn} faces charge storage layers 391b, but is electrically isolated, from charge storage layers 391b by tunneling insulation layer 391c (“*a respective portion of the second dielectric*”). EX1003, ¶256. Thus, Fukuzumi discloses or suggests [15.h].

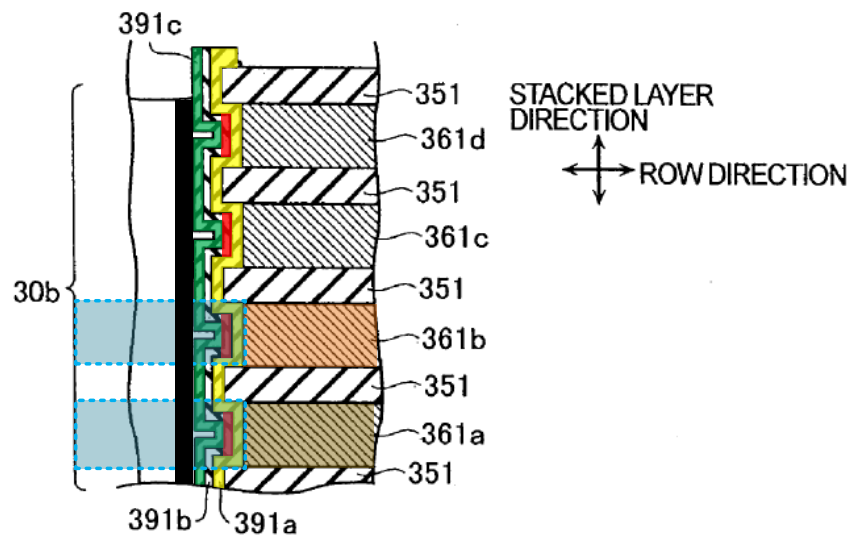


FIG. 28

EX1003 — FIG. AV

From the foregoing, Fukuzumi anticipates or otherwise renders obvious claim

15.

M. Dependent Claim 16

Fukuzumi renders obvious that “*the first and second memory elements comprise polysilicon,*” additionally required by claim 16.

Fukuzumi discloses charge storage layers (“*the first and second memory elements*”) are made of silicon nitride. EX1007, [0104]. A POSITA would have found replacing the silicon nitride layer with polysilicon silicon is merely an obvious design choice from the only three possible materials—polysilicon, silicon nitride, and silicon oxynitride—that “trap charges to store data” in 3D NAND memory devices, as known in the art at the time of the invention. EX1020, Table 1; EX1021, 2847, §I; EX1022, 189; EX1003, ¶259.

A POSITA would also have found it obvious to replace silicon nitride or silicon oxynitride with polysilicon to form an OPO structure for charge storage layer 411 because a POSITA would have recognized that polysilicon was commonly used for memory elements at the time of invention due to silicon nitride and silicon oxynitride’s reliability issues, as well as polysilicon’s better long-term data retention. EX1009, [0080]; EX1010, 1:46-56, 5:26-50; EX1012, 3; EX1014; EX1003, ¶¶261-264.

N. Dependent Claims 17 and 18

Fukuzumi further discloses that “*the first and second memory elements comprise a dielectric material,*” additionally required by claim 17, and “*the*

dielectric material comprises silicon nitride,” additionally required by claim 18. Specifically, Fukuzumi discloses that charge storage layers are formed of silicon nitride. EX1007, [0104].

O. Dependent Claim 19

Fukuzumi further discloses “*dielectric material between the first and second conductive materials,*” additionally required by claim 19. Specifically, Fukuzumi discloses that interlayer insulators 351 are formed between adjacent word line conduction layers 361a-361d (“*first and second conductive materials*”). EX1007, [0148].

P. Dependent Claim 20

Fukuzumi further discloses the additional limitations required by claim 20.

Fukuzumi discloses that bit line BL (“*data line*”) is configured to be selectively coupled to columnar semiconductor CL_{mn} via drain-side selection transistor SDTr_{mn}. Section IX.B.5. Thus, a POSITA would have understood, or at least found it obvious, that data line BL is also configured to be selectively coupled to the vertical outermost layer of columnar semiconductor CL_{mn} (“*conductive channel*”). EX1003, ¶268.

Fukuzumi further discloses that charge storage layers 391b (“*first and second memory elements*”) are located vertically between bit line BL and semiconductor substrate Ba. EX1007, FIG. 2; EX1003, ¶269.

**X. GROUND 6: FUKUZUMI IN VIEW OF KANG RENDERS
OBVIOUS CLAIM 6**

As discussed in Section IX.B, Fukuzumi anticipates or otherwise renders obvious claim 1 on which claim 6 depends. Should the Board find Fukuzumi alone does not render obvious that “*at least one of the transistors comprises a double-gate,*” Kang is introduced in this Ground.

As discussed above in Section IX.F, Fukuzumi discloses drain-side selection transistors SDTrmn to selectively couple memory cells Mtrmn (“*first and second memory cells*”) to bit lines BL (“*data lines*”) during memory operations. EX1007, [0076], [0083], [0085].

As discussed in Section VII.F, Kang further discloses the upper selection transistors being a “*double-gate*” in which “a lower select gate 230a, an upper select gate 230f... formed to have a line shape on both sides of active pillar 206.” EX1004, [0052], FIG. 1C.

Fukuzumi and Kang are analogous art in the same field as the '214 patent, which is related to nonvolatile memory devices. EX1001, 1:6-8; 2:63-67; EX1007, [0002]; EX1004, [0002]. Also, both Fukuzumi and Kang are pertinent to the purported problem addressed by the '214 patent, *e.g.*, increasing integration or density of memory devices. EX1001, 1:7-22; EX1007, [0004], [0144], [0150]; EX1004, [0003]-[0004]; EX1003, ¶274.

A POSITA would have been motivated to modify the surrounded gate structure of Fukuzumi's drain-side selection transistor to the double-gate structure in view of the teachings of Kang because such modification can reduce both gate and parasitic capacitance, as well as limit parasitic effects due to the electric field overlap between the drain and gate regions. EX1003, ¶275.

A POSITA would have had a reasonable expectation of success applying Kang's teachings of double-gate structure to Fukuzumi's drain-side selection transistor as the use of such structure for selection transistors was well-known in the art. EX1015, [0103]-[0106], FIGs. 31, 36-37; EX1016, [0075]-[0080], FIG.11; EX1017, [0012]; EX1019, [0070], FIGs. 6-7, 12; EX1003, ¶276. A POSITA would have found it routine and straightforward to apply Kang's teachings of using the double-gate structure to replace the surrounded-gate structure to form Fukuzumi's drain-side selection transistors, and would have known such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality. EX1003, ¶277. In fact, Fukuzumi's third embodiment strongly indicates that modifying the gate from the surrounded gate structure to the double-gate structure would be compatible with its drain-side selection transistors. EX1003, ¶278; Section IX.F.

**XI. GROUND 7: FUKUZUMI IN VIEW OF AHN RENDERS
OBVIOUS CLAIM 16**

As discussed in Section IX.L, Fukuzumi anticipates or otherwise renders obvious claim 15 on which claim 16 depends. Should the Board find Fukuzumi alone does not render obvious claim 16, Ahn is introduced in this Ground.

Fukuzumi discloses that the charge storage layers 391*b* (“*the first and second memory elements*”) are made of silicon nitride. EX1007, [0104].

Ahn explicitly teaches that “a charge trap layer is formed by depositing, for example, a silicon nitride film **or a polysilicon film** to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (430). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD).” EX1006, [0067].

Fukuzumi and Ahn are analogous art in the same field as the ’214 patent, which is related to nonvolatile memory devices. EX1001, 1:6-8; 2:63-67; EX1007, [0002]; EX1006, [0001]. Also, both Fukuzumi and Ahn are pertinent to the purported problem addressed by the ’214 patent, *e.g.*, increasing integration or density of memory devices. EX1001, 1:7-22; EX1007, [0004], [0144], [0150]; EX1006, [0005]; EX1003, ¶283.

At least for the similar reasons discussed in Section VIII.B, a POSITA would also have found it obvious to replace silicon nitride with Ahn’s polysilicon as the

material of Fukuzumi's charge trap layer 391*b* because it is a mere design choice, and polysilicon has better reliability and data retention than silicon nitride used in the flash memory device. EX1003, ¶284. A POSITA would have had a reasonable expectation of success for such a modification because of the interchangeability of the two materials, as well as the guidance provided by Ahn. EX1003, ¶285; Section VIII.B.

Thus, Fukuzumi in view of Ahn renders obvious claim 16. EX1003, ¶286.

XII. DISCRETION DENIAL DOES NOT APPLY

A. 35 U.S.C. § 325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion to deny institution under 35 U.S.C. § 325(d).

Kang, Fukuzumi, and Ahn have never been presented or otherwise considered by the Office during the original examination of the '214 patent. *See generally* EX1002. None of the grounds raised in this Petition have ever been presented, much less discussed, during the original examination. The disclosures considered by the Examiner in the original examination are not substantially similar to those of the references relied upon in this Petition.

Even if any of Kang, Fukuzumi, and Ahn, or arguments in this Petition, were considered substantially the same as those raised during the prosecution of the '214 patent, the Examiner erred in a manner material to the patentability of the challenged

claims by not rejecting the challenged claims over the prior art and arguments in the grounds presented herein. For instance, the alleged allowable subject matter with respect to issued independent claims 1, 9, and 15 (Section V.B) is disclosed or otherwise rendered obvious by each of Kang and Fukuzumi in Grounds 1, 2, 4, and 5.

B. 35 U.S.C. § 314(a)

As stated in Section II.B, there is no currently pending parallel district court litigation addressing the '214 patent. To the extent the potential addition of the '214 patent to the NDCA case warrants a *Fintiv* analysis¹¹, discretionary denial would be improper due to exceptional circumstances. *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020).

As noted above at FN1, after the Court dismissed PO's counterclaims for alleged infringement of the '214 patent with leave to amend, PO declined to amend its pleadings and instead withdrew its assertion of the '214 patent in August 2024. Moreover, minimal investment was made in the '214 patent before its dismissal—indeed, PO's counterclaims were dismissed due to deficiencies in pleading infringement. EX1026, 1.

This Petition is being filed before the Court decides whether to allow PO to

¹¹ Petitioner reserves the right to address *Fintiv* in view of the facts and the law as they stand following the POPR, should the PO argue for denial under *Fintiv*.

amend its counterclaims, and only two weeks after PO's motion to reassert the '214 patent. EX1028. In addition to the compelling merits of the grounds in this Petition—including multiple anticipation and single-reference obviousness grounds—these exceptional circumstances warrant institution as a matter of fairness.¹²

Finally, as explained in the Ranking Notice, claims challenged in the concurrently filed parallel petition (the '499 IPR) against the '214 patent do not overlap with claims challenged in this Petition. This Petition is the sole challenge to the identified challenged claims before the Board, favoring institution. *Google LLC v. Uniloc 2017 LLC*, IPR2020-00115, Paper 10 at 6 (May 12, 2020).

XIII. CONCLUSION

Based on the grounds specified above, IPR of all challenged claims is respectfully requested.

¹² To the extent the '214 patent becomes reasserted in the NDCA case, if this IPR is instituted, Petitioner will not pursue the same grounds of invalidity in the district court litigation. *Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 11-12 (PTAB June 16, 2020).

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

This Petition complies with the requirements of 37 C.F.R. § 42.24. As calculated by the word count feature of Microsoft Word, it contains 13,922 words, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices, Certification Under § 42.24(d), and Certificate of Service.

/Zhiwei Zou/

Zhiwei (Wayne) Zou

Registration No. 66,041

Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing **Petition for *Inter Partes* Review**, **the associated Power of Attorney, and Exhibits 1001-1028** are being served on February 14, 2025, by U.S. Priority Express Mail at the following address of record for the subject patent.

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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel at the following addresses:

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