

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.
Petitioner

v.

MICRON TECHNOLOGY, INC.
Patent Owner

IPR2025-00498
U.S. Patent No. 8,803,214

**DECLARATION OF DR. KELIN J. KUHN IN SUPPORT OF PETITION
FOR *INTER PARTES REVIEW* OF U.S. PATENT 8,803,214**

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I, Kelin Kuhn of Winthrop, Washington, declare that:

I. Introduction

1. My name is Dr. Kelin J. Kuhn, and I am an adjunct professor in the Materials Science and Engineering Department at Cornell University. I have been retained on behalf of Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Petitioner”), to provide my opinions on certain issues related to U.S. Patent No. 8,803,214 (“the ’214 patent”) in connection with the above-captioned *inter partes* review (IPR) proceeding. In particular, I have been asked to provide my insights, analysis, and opinions regarding whether claims 1-7, 9-12, and 14-20 of the ’214 patent (“challenged claims”) are anticipated by and/or obvious over the prior art references identified below.

2. I understand that the ’214 patent is titled “Three Dimensional Memory and Methods of Forming the Same,” names inventors Sanh D. Tang and John K. Zahurak, and is currently owned by Micron Technology, Inc. (“Micron” or “Patent Owner”). I have considered the ’214 patent. I understand that the ’214 patent has been provided as EX1001.

3. I understand that the file history of the ’214 patent has been provided as EX1002. I have considered this file history, and I will refer to it as “the ’214 file history.”

4. I understand that the ’214 patent is issued from U.S. Patent Application

No. 12/825,211, with a filing date of June 28, 2010. The '214 patent does not claim any priority date before June 28, 2010. I have been asked to assume that June 28, 2010 filing date as the purported invention date for purposes of rendering my opinions in this declaration.

5. My analysis and conclusions set forth in this declaration are based on my educational background and experiences in the field (see Section II). Before June 28, 2010, my level of skill in the art was at least that of a person of ordinary skill in the art ("POSITA"). I am qualified to opine concerning what a POSITA would have known and understood at the time of the '214 patent's purported invention. My analysis and conclusions herein are from the perspective of a POSITA as of June 28, 2010.

6. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this art during the time before the earliest claimed priority date for the '214 patent; my own knowledge and experiences gained from my work experience in the field of the '214 patent and related disciplines; and my experience in working with others involved in this field and related disciplines.

7. I am being compensated by YMTC at my standard hourly consulting rate of \$600 for my time on this matter. My compensation is not dependent on the

outcome of this proceeding or any other proceeding between the parties.

8. As set forth herein, I have concluded that each of the challenged claims is anticipated and/or rendered obvious by the prior art based on the references described below and as described herein. In forming my opinions, I relied on the documents cited in this declaration, which are identified in Section IV. These documents include patents, file histories, printed publications, and other related documents. As discussed below, each document is a type that experts in my field would have reasonably relied upon when forming their opinions. Further, experts in my field would have had access to each document either through the applicable patent offices and/or well-known libraries, conferences, or publications in the field. My opinions are also based upon my personal and professional experience.

II. Background and Qualifications

9. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

10. I am qualified by education and experience to testify as an expert in the field of nonvolatile memory devices. Additionally, the following overview of my background pertains to my qualifications for providing expert testimony in this matter. I am over the age of 18 and am competent to write this declaration. I have personal knowledge, or have developed knowledge, of these technologies based

upon education, training, or experience of the matters set forth herein.

11. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

12. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

13. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

14. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam epitaxy and optoelectronics, and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

15. In 1997, I joined Intel Corporation ("Intel") at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel

0.35 μ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

16. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

17. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel's 90 nm communications process technology. Over a three-year period, my team developed a derivative analog/RF technology (including a SiGe bipolar junction transistor ("BJT")) on top of Intel's premium 90 nm microprocessor process.

18. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel's 45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

19. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement

within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel's FinFET device). I received a second Intel achievement award in 2008 for my work on Intel's FinFET device.

20. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten year time frame.

21. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond: Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper "Considerations for Ultimate CMOS Scaling" (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

22. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course, protected by client confidentiality, these projects include FinFETs, vertical power

transistors, solar cells, conventional (planar) MOS, and flash.

23. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

24. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

25. A few representative book chapters include, “The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).

26. I am an inventor of approximately 80 granted U.S. patents in the field

of semiconductor technology.

27. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.

28. As specifically relevant to this project, I want to highlight the 3’D gate-last vertical gate-all-around (GAA) devices and the 3’D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight recent proprietary and confidential work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

29. Attached as Appendix A to this report is a current copy of my curriculum vitae, which outlines my academic, professional and experiential qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

III. Level of Ordinary Skill in the Art

30. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a POSITA at the time

of the alleged invention. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field, the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art including the art cited below.

31. Upon consideration of the relevant factors listed above, in my opinion, a POSITA at the time of the claimed invention, would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa.

32. Well before June 28, 2010, my level of skill in the art was at least that of a person having ordinary skill. I am qualified to opine concerning what a POSITA would have known and understood at the time of the '214 patent's purported invention. My analysis and conclusions herein are from the perspective of a POSITA as of June 28, 2010. A different invention date would not change my opinions as long as the identified prior art were still prior art.

IV. Materials Considered and Relied Upon

33. In reaching the conclusions described in this declaration, I have relied on the documents and materials cited herein as well as those identified in this Declaration, including but not limited to, the '214 patent, the prosecution history of the '214 patent, and prior art references cited herein. These materials include patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions.

34. In the cited references, all emphasis is added unless otherwise noted.

35. I have also relied on my education, training, research, knowledge, and personal and professional experience in the relevant technologies that were already in use prior to the claimed invention.

- EX1001: U.S. Patent No. 8,803,214 to Tang *et al.* (“the '214 patent”).
- EX1002: Prosecution History of the '214 patent (“the '214 file history”).
- EX1004: U.S. Patent Application Publication No. 2010/0140685 in the name of Kang *et al.* (“Kang”).
- EX1005 & EX1006: Korean Patent Application Publication No. 10-2010-0034612 in the name of Ahn *et al.*; Certified English Translation of Korean Patent Application Publication No. KR10-2010-0034612 (EX1005 & EX1006 collectively as “Ahn”).

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- EX1007: U.S. Patent Application Publication No. 2009/0146190 in the name of Fukuzumi *et al.* (“Fukuzumi”).
 - EX1008: Joint Claim Construction and Prehearing Statement and Appendices (Patent Local Rule 4-3), *Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.*, No. 3:23-cv-05792-RFL, D.I. 105 (N.D. Cal. August 19, 2024) (“Claim Construction”).
 - EX1009: U.S. Patent Application Publication No. 2010/0240205 in the name of Son *et al.* (“Son”).
 - EX1010: U.S. Patent No. 7,425,742 to Nazarian (“Nazarian”).
 - EX1011: Y. Chen *et al.*, “Flash Memory Reliability NEPP 2008 Task Final Report,” JPL Publication, (2009), Available Online at https://nepp.nasa.gov/files/16376/08_106_1%20JPL%20Chen%20Flash%20Memory.pdf (“Chen”).
 - EX1012: F. Arai *et al.*, “Extended Data Retention Process Technology for Highly Reliable Flash EEPROMs of 10^6 to 10^7 W/E Cycles,” 1998 IEEE International Reliability Physics Symposium Proceedings. 36th Annual, Reno, NV, USA, 1998, pp. 378-382 (“Arai”).

- EX1013: S. Wang *et al.*, “A High-Endurance (>100K) BE-SONOS NAND Flash With a Robust Nitrided Tunnel Oxide/Si Interface,” 2010 IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 2010, pp. 951-955 (“Wang”).
- EX1014: C. Sandhya *et al.*, “Nitride Engineering and the Effect of Interfaces on Charge Trap Flash Performance and Reliability,” 2008 IEEE International Reliability Physics Symposium, Phoenix, AZ, USA, 2008, pp. 406-411 (“Sandhya”).
- EX1015: U.S. Patent Application Publication No. 2009/0310425 in the name of Sim *et al.* (“Sim”).
- EX1016: U.S. Patent Application Publication No. 2010/0120214 in the name of Park *et al.* (“Park”).
- EX1017: U.S. Patent Application Publication No. 2011/0286283 in the name of Lung *et al.* (“Lung”).
- EX1018: U.S. Patent Application Publication No. 2007/0057328 in the name of Taniguchi *et al.* (“Taniguchi”).
- EX1019: U.S. Patent Application Publication No. 2010/0133598 in the name of Chae *et al.* (“Chae”).

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- EX1020: K. Joo *et al.*, “Novel Transition Layer Engineered Si Nanocrystal Flash Memory with MHSOS Structure Featuring Large V_{th} Window and Fast P/E Speed,” IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest., Washington, DC, USA, 2005, pp. 865-868 (“Joo”).
 - EX1021: S. Park *et al.*, “A New Operating Scheme by Switching the Polarity of Program/Erase Bias for Partially Oxidized Amorphous-Si-Based Charge-Trap Memory,” IEEE Transactions on Electron Devices, vol. 53, no. 11, Nov. 2006, pp. 2847-2849 (“Park”).
 - EX1022: M. Rosmeulen *et al.*, “Silicon Rich Oxides as an Alternative Charge Trapping Medium in Fowler-Nordheim and Hot Carrier Type Non-Volatile-Memory Cells,” Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 189-192 (“Rosmeulen”).
 - EX1024: J. Jang *et al.*, “Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193 (“Jang”).

V. Legal Standards

36. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims

from the perspective of a person skilled in the art.

37. In formulating my opinions, I have been informed of certain legal understandings relevant to my opinions. In formulating my opinions, I have relied on the legal understandings I have been provided with as set forth in this declaration.

38. I have been informed that in *inter partes review* proceedings, invalidity must be shown under a preponderance of the evidence standard.

A. My Understanding of Claim Construction

39. I have been informed that patent claims are construed from the viewpoint of a POSITA of the patent at the time of the invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a POSITA in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification, and the prosecution history (i.e., the intrinsic record).

40. I have further been informed that a POSITA must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office and may

contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or clearly and unambiguously disavowing claim coverage.

41. In interpreting the meaning of the claim language, I understand that a POSITA may also consider "extrinsic" evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. For example, this can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

B. My Understanding of Anticipation

42. I understand that a patent claim is invalid as "anticipated" if all the limitations of the claim are present, either expressly or inherently, in a single prior art publication or patent.

43. I also understand that a prior art reference can disclose a claimed feature because the feature is expressly described or because the feature is inherent in the disclosure. I understand that something is inherent in a prior art reference if the missing descriptive matter must necessarily be present, not merely probably or possibly present, and it would be so recognized by a POSITA as of the priority date of the patent. I understand that it is acceptable to examine evidence outside of the prior art reference (i.e., extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it.

44. I have further been informed that where a reference discloses multiple embodiments, the reference should not be limited to a preferred embodiment. Instead, each disclosed embodiment may anticipate.

45. Moreover, I have been informed that as part of an anticipation analysis, it is proper to take into account not only specific teachings of the reference, but also the inferences that one skilled in the art would reasonably be expected to draw therefrom. A reference can anticipate a claim even if it does not expressly spell out all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would at once envisage the claimed arrangement or combination.

C. My Understanding of Obviousness

46. I understand that a claim may be invalid if the subject matter described

by the claim as a whole would have been obvious to a hypothetical POSITA in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a hypothetical POSITA and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

47. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering their problem.

48. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

49. I have also been advised that in considering whether a claimed invention would have been obvious over a combination of prior art references, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a POSITA. I understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a POSITA can implement a predictable variation, the variation is likely obvious;

- If a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls whether the claim is obvious;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;
- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
- "Common sense" teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a POSITA will be able to fit the teachings of multiple patents together like pieces of a puzzle;

- A POSITA is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was “obvious to try,” particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a POSITA would have had good reason to pursue the known options within his or her technical grasp; and
- One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

50. I further understand that, in making a determination as to whether the claimed invention would have been obvious to a POSITA, the Board may consider certain objective factors if they are present, such as: commercial success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence, and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with

predictable results) that is sufficiently strong.

VI. Technology Background

51. Three-dimensional (3D)—or vertical—NAND flash memory is a type of nonvolatile memory in which the memory cells are stacked vertically in multiple layers/levels to increase storage density, compared with traditional two-dimensional (2D)—or planar—NAND flash memory, where the memory cells are arranged in a simple 2D matrix.

52. A typical 3D NAND memory device includes memory cells and their gate lines (e.g., word lines) are arranged at different vertical levels in 3D. One example of 3D NAND memory device back in 2009 is shown in FIG. A of my Declaration below below (FIG. 1 of Jang), which shows a perspective view of a 3D memory structure. EX1024, FIG. 1.

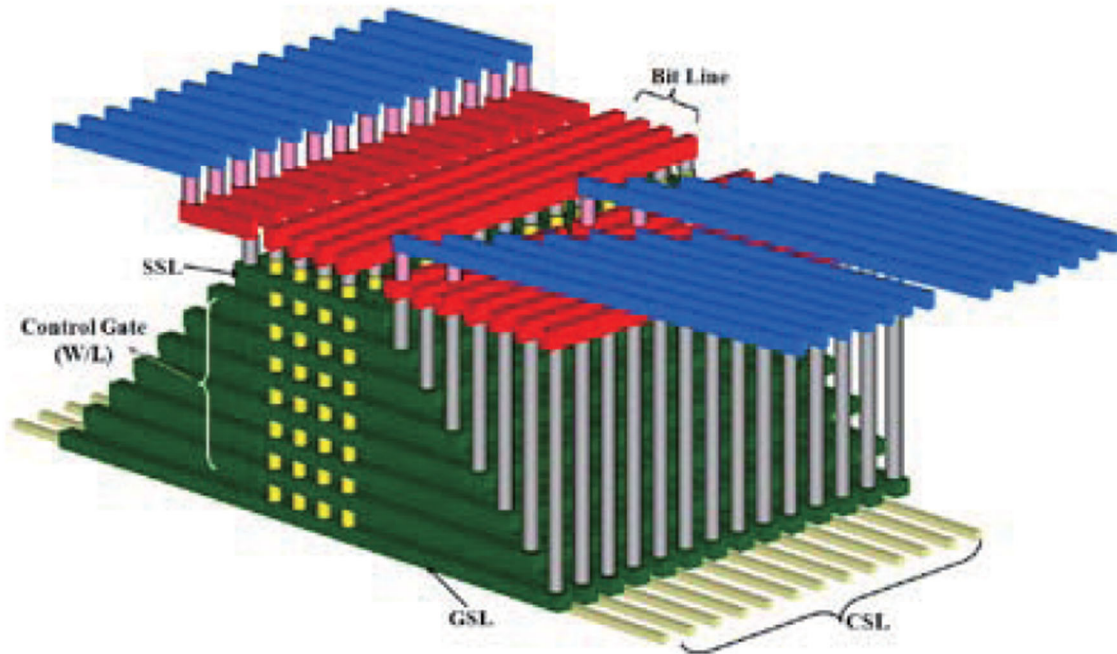


FIG. A – FIG. 1 of Jiang

53. As shown in FIG. A above, the 3D memory device includes bit lines (in red), multiple levels of gate lines (in dark green), such as control gates/word lines W/L and select lines SSL/GSL. A common source line CSL (in light yellow) is formed on a substrate (not shown). EX1024, p. 192, Architecture and Key Features of TCAT Flash.

54. A vertical structural component of Jang's memory device is the semiconductor pillars (in yellow), which penetrate the select lines SSL/GSL and word lines W/L to electrically connect the bit lines with the common source line CSL at opposite ends. These semiconductor pillars correspond to NAND cell strings, where each string includes multiple memory cells connected in series between

a drain-side select transistor and a source-side select transistor. Memory cells are formed at the cross-points between the control gates/word lines W/L and the semiconductor pillars. Each memory cell has a “SONOS” type cell structure, which refers to “silicon-oxide-nitride-oxide-silicon,” where the middle silicon nitride layer “N” is used as the charge storage memory element. EX1024, p. 192, Architecture and Key Features of TCAT Flash.

VII. Overview of the '214 Patent

A. Subject Matter Overview

55. The '214 patent was issued on August 12, 2014, from U.S. Patent Application No. 12/825,211 (“the '211 application”), filed on June 28, 2010. EX1001, (10), (21), (22).

56. The '214 patent is directed to nonvolatile memory devices and addresses fabrication challenges associated with three-dimensional (3D) memory structures. EX1001, 1:6-8; 2:63-67. The '214 patent states that “[s]ince 3D memory devices are relatively new, manufacturing these devices can pose fabrication process challenges,” and thus, seeks to mitigate through novel device structures and fabrication methods. EX1001, 1:20-22, 12:30-31.

57. The disclosed memory devices include multiple groups of memory cells arranged at different device levels. EX1001, 12:32-41. One such embodiment related to the challenged claims is depicted in FIG. 31 of the '214 patent, illustrating

a memory device 3000, which includes a string of memory cells 210-212 along the Z-direction. EX1001, 10:61-11:19. FIG. B of my Declaration with annotations below shows FIG. 31 of the '214 patent with my annotations.

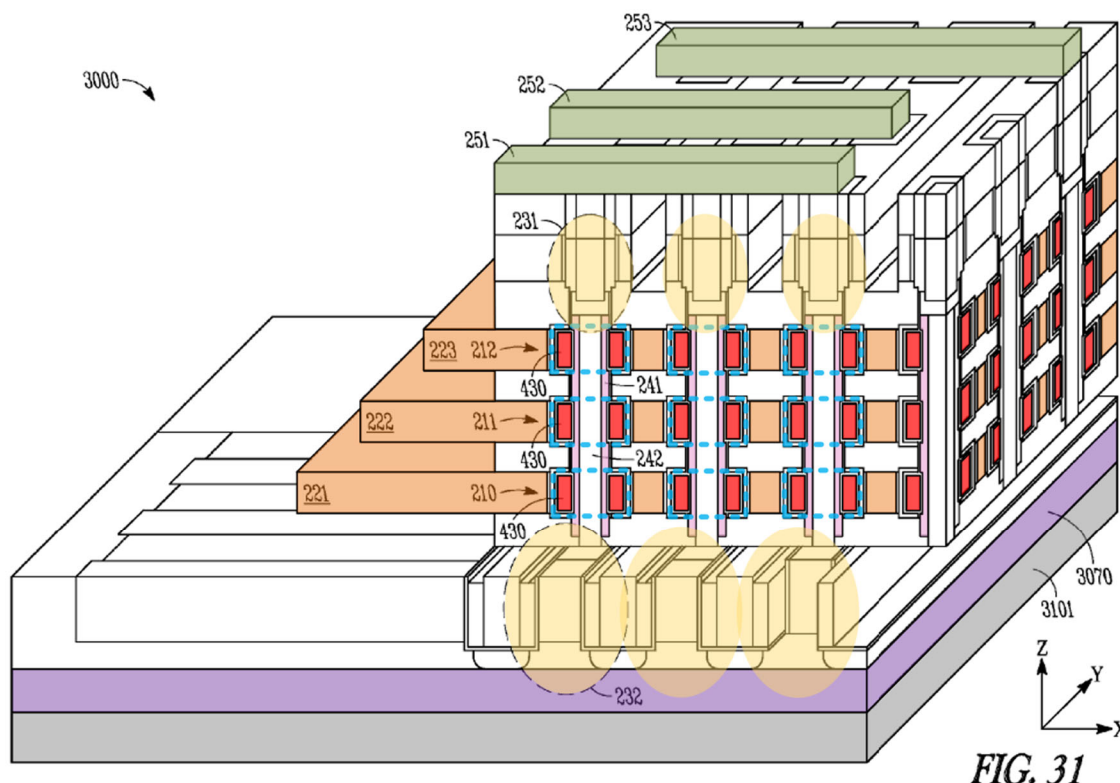


FIG. B – FIG. 31 of the '214 patent (annotated)

58. I noted that the specification recites “FIG. 31 also shows a channel 441 ...” (EX1001, 11:7), although the numerical “441” is not shown in FIG. 31. It is clear to me that the reference to “channel 441” actually pertains to channel “241” shown in FIG. 31. EX1001, 4:14-15, 10:30-35, FIG. 3.

59. Channels 241 (in pink) extend through the memory elements 430 (in red), which are ring-shaped and located within cavities of control gates 221-223. These memory elements are formed in cavities (in blue dashed boxes) of control

gates 221-223 (in orange), and are responsible for storing charges. EX1001, 4:34-5:3, 7:43-8:38, 10:30-35.

60. The memory device 3000 also features a common source 3070 (in purple) positioned between the memory cells and the substrate 3101 (in gray), which is electrically connected to the channels through lower select transistors 232 (in yellow). Meanwhile, data lines 251-253 (in green) are arranged above the memory cells and interface with channels 241 via upper select transistors 231 (in yellow). EX1001, 10:27-67.

B. File History of the '214 Patent

61. I have reviewed the file history of the '214 patent. Upon the issuance of the Non-Final Office Action dated June 7, 2012, claims 1-34 were pending in the application, wherein claims 22-34 were withdrawn, claims 1-6 and 9-21 were rejected under Pre-AIA 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2009/0230454 in the name of Pekny ("Pekny"), and claims 7 and 8 were rejected under Pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Pekny in view of U.S. Patent Application Publication No. 2007/0057310 in the name of Matsui *et al.* ("Matsui"). EX1002, 206-215.

62. In the Response to the Non-Final Office Action dated September 7, 2012, the applicant of the '214 patent amended the claims and argued that Pekny failed to disclose that the first memory cells/first control gate/first conductive

material and the second memory cells/second control gate/second conductive material are formed in different device levels (claims 1 and 15), and that the memory elements have a ring shape (claim 9). EX1002, 149-159.

63. Following these amendments, the Examiner maintained the rejection of claims 9-14 over Pekny while allowing claims 1-8 and 15-21 in the Final Office Action dated February 1, 2013. EX1002, 138-141. The allowable subject matter related to the claimed “a plurality of second memory cells” in claim 1, the claimed “a common source,” “data lines,” and the relative positions between “the first and second memory cells,” “the common source,” and “the substrate” in claim 4 (issued as independent claim 8), and the claimed “a second conductive material” in claims 15 and 20 (issued as independent claim 21). EX1002, 141-142.

64. In the Response to the Final Office Action dated April 30, 2013, the applicant of the '214 patent further amended claim 9 to specify that the first and second memory elements are in different device levels. EX1002, 122-128.

65. Finally, the Examiner allowed all claims in two Notices of Allowance dated May 28, 2013 and March 31, 2014, stating that the prior art on record did not teach certain claim limitations, including the claimed “a second control gate” and “data lines” in then-claims 1, 4, 9, and 20, as well as “a second dielectric” and “a conductive channel” in claim 15. EX1002, 40-41, 102-103.

C. Interpretation of the '214 Patent Challenged Claims

66. I have been instructed that the challenged claims of the '214 patent are to be given their ordinary and customary meaning as understood by a POSITA at the time of the alleged invention in light of the specification and the prosecution history pertaining to the patent, except as provided below. I have followed these principles in my analysis set forth in this document. I reserve the right to supplement my opinions in this declaration to the extent that any parties later propose claim constructions for any claim terms in the '214 patent.

67. I understand that the term “cavity” recited in challenged claims 1 and 15 is also recited in claims 1 and 17 of U.S. Patent No. 10,872,903 (“the '903 patent”), which is one of the continuations of the '214 patent and is asserted in a pending district court litigation between YMTC and Micron (“YMTC Litigation”).

68. I understand that in the YMTC Litigation, Petitioner proposes that “a [first-fourth] cavity of [first/second] control gate” should be construed as “a [first-fourth] hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate.” (“Petitioner’s Construction”). EX. 1008, 17-18. I also understand that Patent Owner asserts that those terms should be given their plain and ordinary meaning, without specifying what it believes the plain and ordinary meaning is (“PO’s Construction”). EX. 1008, 17-18. As I explain below with respect to Grounds 1, 2, 4, and 5, the challenged claims are anticipated and/or

rendered obvious by the prior art under either party's construction.

VIII. Overview of the Cited References

69. General descriptions provided for the following references and combinations thereof are incorporated into each subsection and mapping of the claims that include citations to these references.

A. Kang (EX1004)

70. Kang discloses various three-dimensional (3D) NAND flash memory architectures and fabrication methods, aiming at increasing integration density and optimizing memory cell stacking. Kang's embodiments explore different gate structures and transistor configurations to enhance performance and scalability. EX1004, [0002]-[0013], FIGs. 1A-1E.

71. According to Kang's descriptions in paragraphs [0043], [0050], [0054], and [0058], a POSITA would have understood that the descriptions of common features shared among multiple embodiments, although appearing in connection with one embodiment (e.g., FIG. 1A), are equally applicable to other embodiments that include these shared features.

72. One embodiment, illustrated in FIG. 1E (referred to herein as the "FIG. 1E embodiment") and shown below in FIG. C of my Declaration with annotations, describes a vertical NAND flash memory device 400 including an active pillar 406 (in pink) extending vertically from a semiconductor substrate 402 (in gray).

Fig. 1E

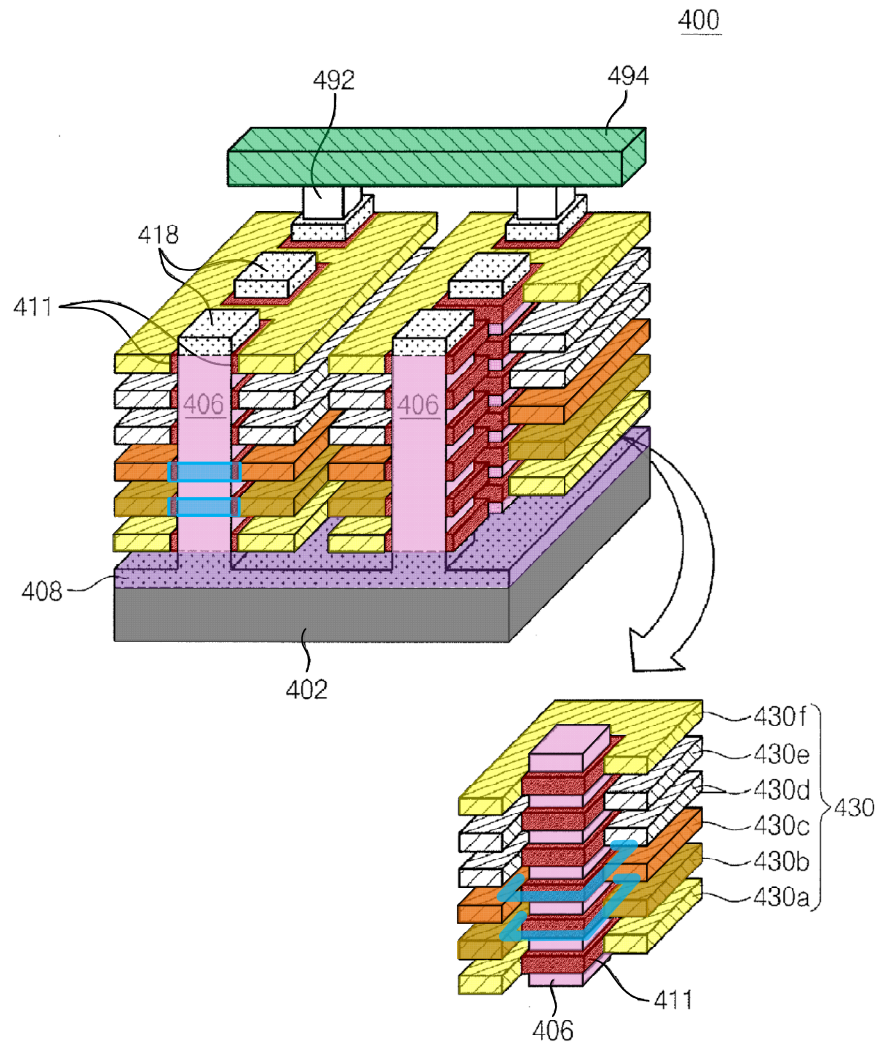


FIG. C – FIG. 1E of Kang (annotated)

73. Surrounding the active pillar 406 is a gate group 430, which includes a lower select gate 430a (in yellow), an upper select gate 430f (in yellow), and multiple control gates 430b-430e (in orange and brown), each with a horizontal plate-like structure. EX1004, [0060]. The active pillar 406 penetrates vertically through cavities (in blue) within the gate group 430 and is electrically connected to

a bit line 494 (in green) at the top via an upper select transistor having the upper select gate 430*f*. At the bottom, the active pillar 406 is electrically coupled with a common source 408 (in purple) through a lower select transistor having the lower select gate 430*a*. EX1004, [0059], [0060].

74. FIG. 1E embodiment is featured by the ring-shaped charge storage layer 411 (in red) within each cavity, located between the control gates 430*b*-430*e* and the active pillar 406. EX1004, [0061]. The charge storage layer follows an ONO (oxide-nitride-oxide) configuration, including a silicon nitride layer for charge trapping, sandwiched between two silicon oxide layers for tunneling and blocking functions. EX1004, [0038].

75. In Kang's FIG. 1E embodiment, the upper select transistors, memory transistors, and lower select transistors, which are formed at the intersections between active pillars 406 and plate-shaped upper select gate 430*f*, control gates 430*b*-430*e*, and lower select gates 430*a*, respectively, in this embodiment, have surrounded gates. EX1004, [0041], [0042], [0060].

76. In another embodiment, illustrated in FIG. 1C (referred to in my Declaration as the "FIG. 1C embodiment"), Kang presents a variation in select transistor design. Unlike the FIG. 1E embodiment where the upper and lower select transistors have a surrounded-gate configuration, the FIG. 1C embodiment features a double-gate design, in which the upper and lower select transistors are controlled

by independent gates positioned on either side of the active pillar 206. EX1004, [0041], [0052], FIGs. 1A-1C.

B. Ahn (EX1005, EX1006)

77. Ahn discloses a 3D flash memory device designed to improve integration density by adopting a vertical memory cell arrangement. EX1006, [0002], [0022]. The memory device comprises vertically arranged cell strings on a substrate, where each string consists of a source select transistor, multiple memory cells, and a drain select transistor. EX1006, [0026].

78. As depicted in FIG. 12 of Anh below (FIG. D of my Declaration with annotations), the memory device features a channel region (460) by which memory cells are formed, and “an ONO dielectric layer (440) for charge storage, *i.e.*, a blocking layer, a charge trap layer, and a tunneling layer, [which] are sequentially formed on the inner wall of the above through hole (430).” EX1006, [0052], [0065]. Although the through hole (430) is not depicted in Fig. 12, a POSITA would understand that through hole (430) in which channel region (460) and ONO dielectric layer (440) are formed passes through conductive layers (420) and interlayer insulating films (410).

Figure 12

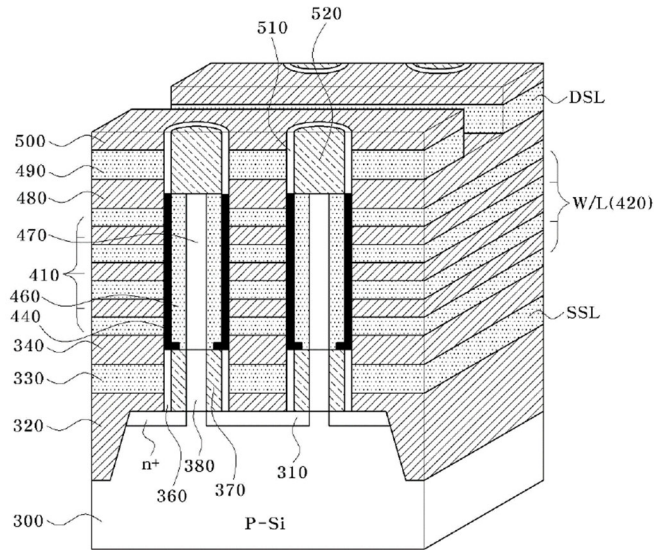


FIG. D – FIG. 12 of Anh

79. The ONO dielectric layer (440) includes a blocking layer, a charge trap layer, and a tunneling layer, all sequentially formed along the inner wall of through hole (430), through which channel region (460) is formed and passes through conductive layers (420). The charge trap layer of ONO dielectric layer (440) including “a silicon nitride film or a polysilicon film” is “formed on the inner wall” of through hole (430) in each conductive layer (420). EX1006, [0064]-[0067].

C. Fukuzumi (EX1007)

80. Fukuzumi discloses a nonvolatile semiconductor memory device designed to address challenges associated with transitioning semiconductor memory devices from 2D to 3D structures. EX1007, [0002], [0003], [0040].

81. FIG. 2 of Fukuzumi illustrates a perspective view of the nonvolatile semiconductor memory device 100 in the first embodiment, while FIG. 4 of

Fukuzumi presents a cross-sectional view of the same nonvolatile semiconductor memory device 100. EX1007, [0078], [0086]. FIG. E (including an insert to the left showing an expanded view of a memory string MS) and FIG. F below with my annotations, show FIGs. 2 and 4 of Fukuzumi, respectively.

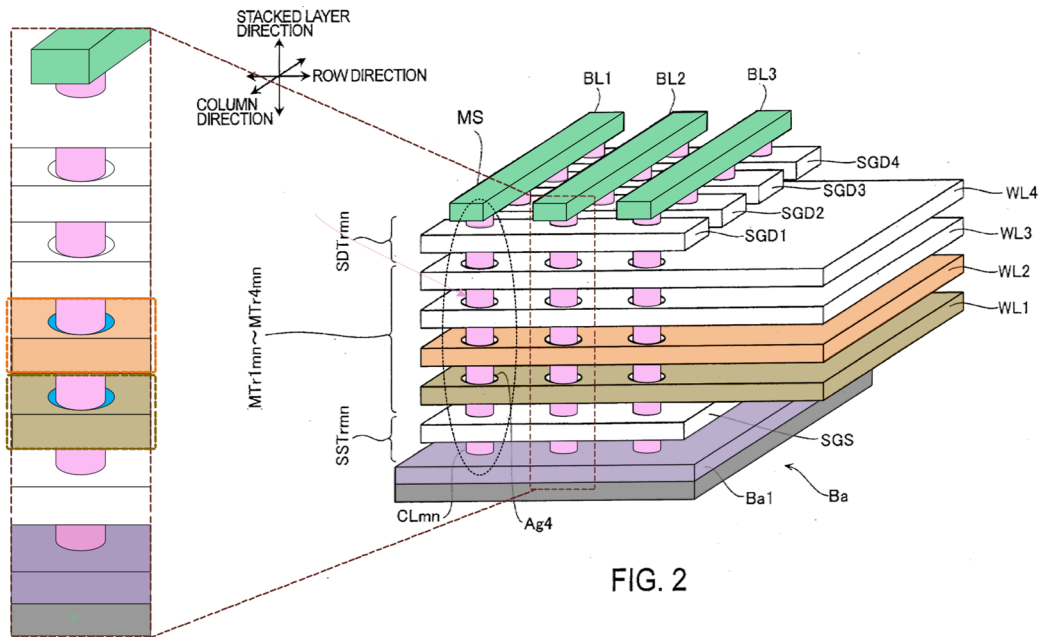


FIG. E – FIG. 2 of Fukuzumi (annotated)

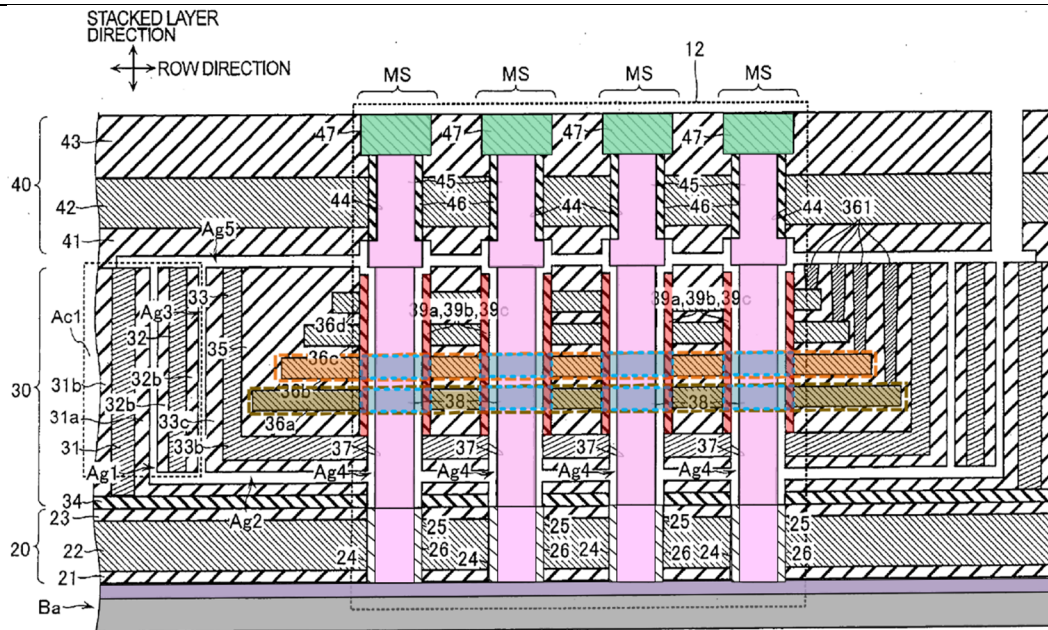


FIG. 4
FIG. F – FIG. 4 of Fukuzumi (annotated)

82. As depicted in FIGs. E and F above, the nonvolatile semiconductor memory device 100 of Fukuzumi includes a matrix of memory strings MS, each containing memory cells labeled MTr1mn through MTr4mn, where the indices m and n represent the X- and Y-coordinates of the memory cells. EX1007, [0079]. Each memory string MS includes a columnar semiconductor CL_{mn} (in pink), which includes a source-side columnar semiconductor layer 25, located on a substrate Ba (in gray), memory 38 (in pink), and a drain-side columnar semiconductor layer 45. Specifically, memory 38 is part of columnar semiconductor CL_{mn} described by, “[a]memory 38 is formed at a portion as aligning the source-side columnar semiconductor 25 in the memory hole 37”. EX1007, [0103]. The drain-side

semiconductor layer 45 connects to the bit line layer 47 (in green) and the columnar semiconductor CL_{mn} (in pink) along the column direction. EX1007, [0086], [0088]-[0089], [0096], [0103], [0108]-[0109].

83. The memory cells $MTr1_{mn}$ - $MTr4_{mn}$ include memory 38, which is part of the columnar semiconductor CL_{mn} , segments of word lines WL1-WL4 (in brown and orange, e.g., word line conduction layers 36a-d) that connect to each memory cell gate, and a charge storage layer 39b (in red) located on the sidewalls of the word lines WL1-WL4 within memory hole 37 (in blue). EX1007, [0080], [0085], [0087]. The drain-side selection transistors $SDTr_{mn}$, including portions of the drain-side selection gate lines SGD, are located at the upper portion of each memory string MS, while the source-side selection transistors $SSTr_{mn}$, with portions of the source-side selection gate lines SGS, are located at the lower portion of the memory strings MS. EX1007, [0082]-[0083], [0088]-[0089].

84. Fukuzumi also presents a second embodiment, shown in FIG. 28, which differs from the first embodiment primarily in “a configuration of a memory layer 30b as compare[d] with the memory layer 30 in the first embodiment,” while “the same or similar reference numerals in the second embodiment are applied to the same or similar parts and elements throughout the drawings as the first embodiment.” EX1007, [0146]-[0147]. Thus, it is clear to me that although Fukuzumi describes nonvolatile semiconductor memory device 100 and its accompanying figures,

including FIG. 2, in the context of the first embodiment, unless otherwise specified (e.g., with respect to memory layer 30 and word line conduction layers 36), the disclosures regarding nonvolatile semiconductor memory device 100 are equally applicable to the second embodiment as well.

85. Both embodiments of Fukuzumi's nonvolatile semiconductor memory devices provide "an effect of higher integration and lower cost on the nonvolatile semiconductor memory device." EX1007, [0144], [0150].

IX. Grounds 1 and 2: Kang Anticipates or Otherwise Renders Obvious Claims 1-7, 9-12, and 14-20

A. Independent Claim 1

86. Claim 1 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[1.P] An apparatus comprising:

[1.a] a substrate of a memory device;

[1.b] a plurality of first memory cells located in a first device level of the memory device over the substrate;

[1.c] a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level;

[1.d] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

[1.e] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate; and

[1.f] data lines configured to be selectively coupled to a common source and the memory cells through conductive material.

[1.P] An apparatus comprising

87. Kang discloses a flash memory system 1310 including a memory controller 1312 and a flash memory 1311 in FIG. 5B (FIG. G of my Declaration below). EX1004, [0107], FIG. 5B. The flash memory system 1310 qualifies as the claimed “apparatus.”

Fig. 5B

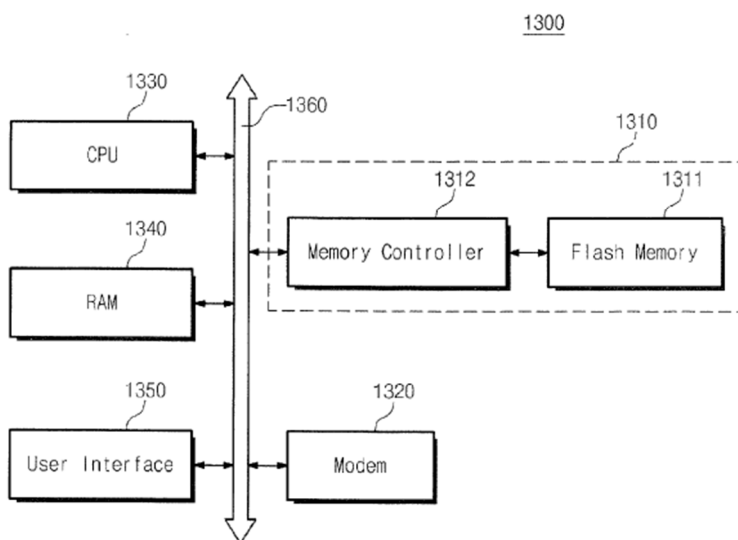


FIG. G – FIG. 5B of Kang

[1.a] a substrate of a memory device

88. In Kang's FIG. 1E embodiment shown in FIG. H below of my Declaration with annotations, Kang discloses a semiconductor substrate 402 (in gray) of nonvolatile memory device 400, which is included in flash memory system 1310. EX1004, [0059], [0107], FIG. 1E. Therefore, it is my opinion that Kang discloses "a substrate of a memory device."

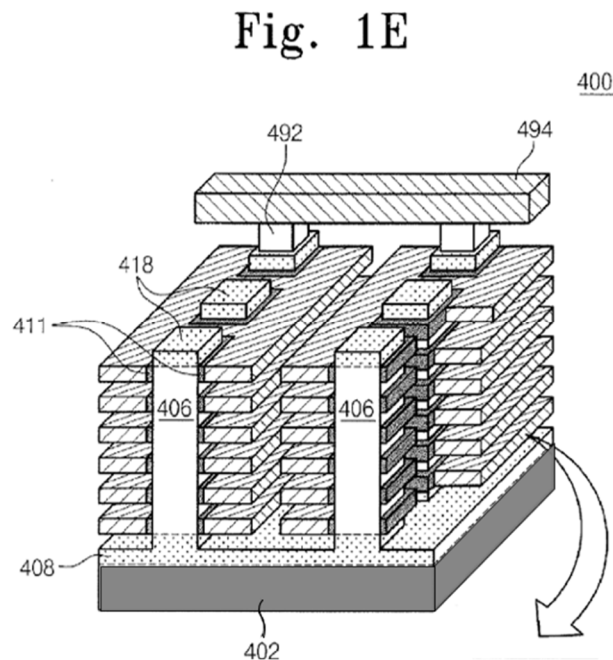


FIG. H – FIG. 1E of Kang (annotated)

[1.b] a plurality of first memory cells located in a first device level of the memory device over the substrate

[1.c] a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level

89. In the first embodiment shown in FIG. 1A below (FIG. I of my

Declaration), Kang discloses a nonvolatile memory device 100 including a plurality of cell strings 103, each including multiple memory transistors 133 that are vertically and serially connected on a semiconductor substrate 102. EX1004, [0041]. Kang further describes that memory transistors 133 in nonvolatile memory device 100 are respectively formed at the intersections of active pillars 106 and control gates 130b-130e, establishing a three-dimensional (3D) arrangement. EX1004, [0041]-[0042]. Given that the 3D arrangement of memory transistors relative to the control gates is a common characteristic across all disclosed embodiments as discussed above, a POSITA would understand that memory transistors are similarly formed at the intersections of active pillars 406 and control gates 430b-430e in nonvolatile memory device 400, as depicted in FIG. I below.

Fig. 1A

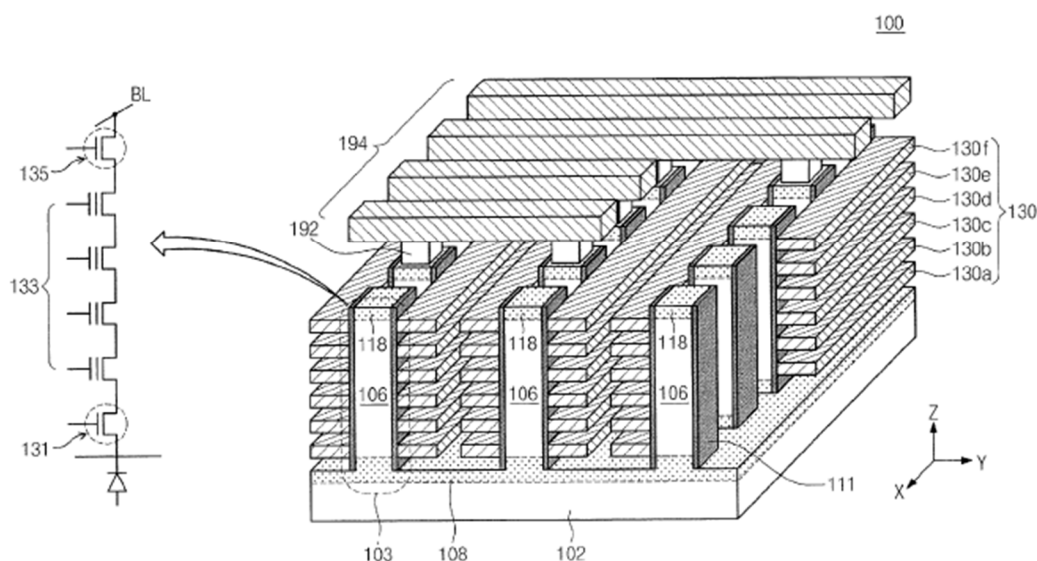


FIG. I – FIG. 1A of Kang

90. I noted that the specification of the '214 patent states that “‘over’ ... could refer to either a material being ‘on’ another material or where there is one or more additional intervening materials between the materials (*e.g.*, contact is not necessarily required).” EX1001, 5:30-38.

91. As illustrated in the annotated FIG. 1E below (FIG. J of my Declaration with annotations), nonvolatile memory device 400 includes a first group of memory transistors (enclosed within the brown dashed box) positioned at a first device level, corresponding to the level of first control gates 430*b* (in brown) above semiconductor substrate 402. This structure qualifies as the claimed “a plurality of first memory cells located in a first device level of the memory device over the substrate.” Additionally, a second group of memory transistors (enclosed within the orange dashed box) is positioned at a second device level, corresponding to the level of second control gates 430*c* (in orange) above semiconductor substrate 402. This structure qualifies as the claimed “a plurality of second memory cells located in a second device level of the memory device over the substrate.” FIG. 1E explicitly illustrates that the first device level is positioned below the second device level, confirming that these levels are distinct within the 3D arrangement.

Fig. 1E

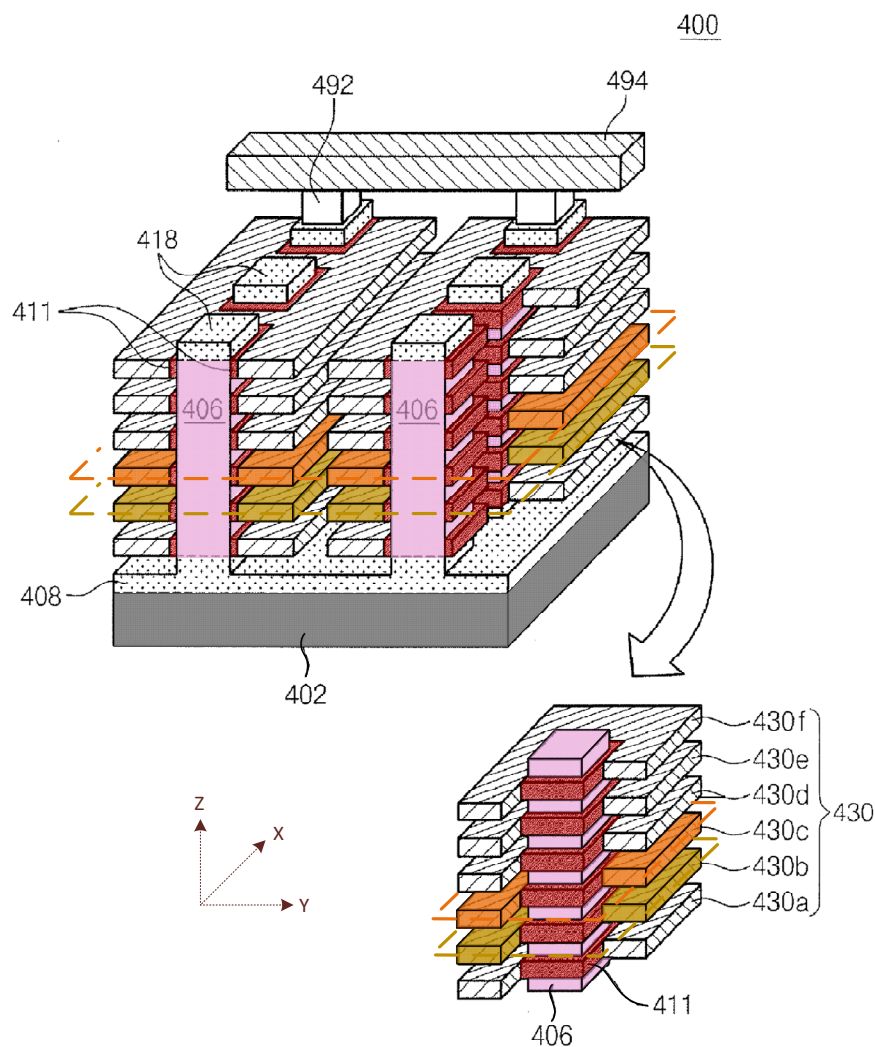


FIG. J – FIG. 1E of Kang (annotated)

92. Therefore, it is my opinion that Kang discloses the subject matter of elements [1.b] and [1.c].

[1.d] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate

[1.e] a second control gate formed in the second device level, the second control gate to control access to the second memory

cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate

93. As illustrated in annotated FIG. 1E below (FIG. K of my Declaration with annotations), Kang discloses multiple control gates 430b-430e, each having a horizontal plate-like structure positioned at a corresponding device level.

Fig. 1E

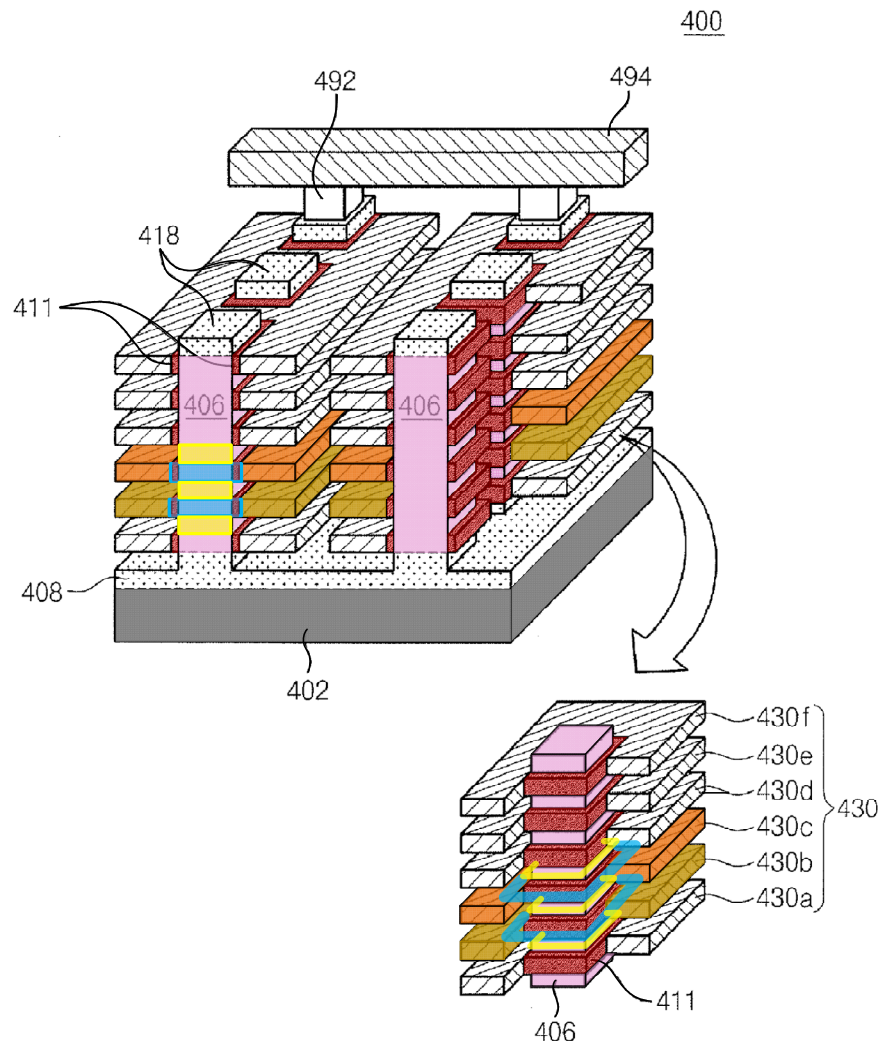


FIG. K – FIG. 1E of Kang (annotated)

94. These control gates function to regulate the operation of the

corresponding memory transistors by selectively applying a control voltage to enable or inhibit conduction through the memory cells. EX1004, [0038], [0060]-[0061], [0080]. Specifically, first control gate 430b (in brown) is positioned at the first device level and serves to control access to the first group of memory transistors. Similarly, second control gate 430c (in orange) is located at the second device level and controls access to the second group of memory transistors.

95. Kang further describes that control gates 130b-130e are “vertically stacked,” meaning they are arranged in distinct horizontal planes at different device levels. A POSITA would have understood that the descriptions of control gates 130b-130e being vertically stacked and connecting to the word line driving circuit common features across embodiments. These control gates are electrically connected to a word line driving circuit, which supplies the necessary control voltages to selectively activate or deactivate memory transistors at each level. This configuration enables independent control of the memory transistors across multiple stacked levels, facilitating the operation of a 3D memory array. EX1004, [0037], [0042].

96. Kang further discloses that each memory transistor includes a charge storage layer, which “may be used as a charge storage layer which traps charges to store data.” EX1004, [0038]. Specifically, Kang describes that the charge storage layer includes “an ONO layer, i.e., a silicon nitride layer that may actually trap

charges to store data, and any one of two silicon oxide layers that may be used as a tunnel insulating layer and the other may be used as a blocking insulating layer.” EX1004, [0038]. Given this disclosure, a POSITA would understand that the silicon nitride layer within charge storage layer 411 functions as the claimed “memory element” for storing charge.

97. Additionally, Kang discloses that active pillar 406 “may vertically penetrate the gate group 430” and that charge storage layer 411 “is limited between the active pillar 406 and the gate group 430.” EX1004, [0060]-[0061]. Based on this description, a POSITA would have understood that active pillar 406 and charge storage layers 411 create holes through gate group 430, with active pillar 406 occupying a central portion of the holes and charge storage layers 411 positioned around active pillar 406 in the holes. Consequently, Kang discloses the claimed “cavity of the first/second control gate” in which corresponding portions of active pillar 406 and charge storage layers 411 are positioned.

98. This structural configuration is further depicted in FIG. K, which is repeated below, where two charge storage layers 411 (in red) are formed within two cavities (in blue) of control gates 430*b* and 430*c* (in brown and orange), respectively.

Fig. 1E

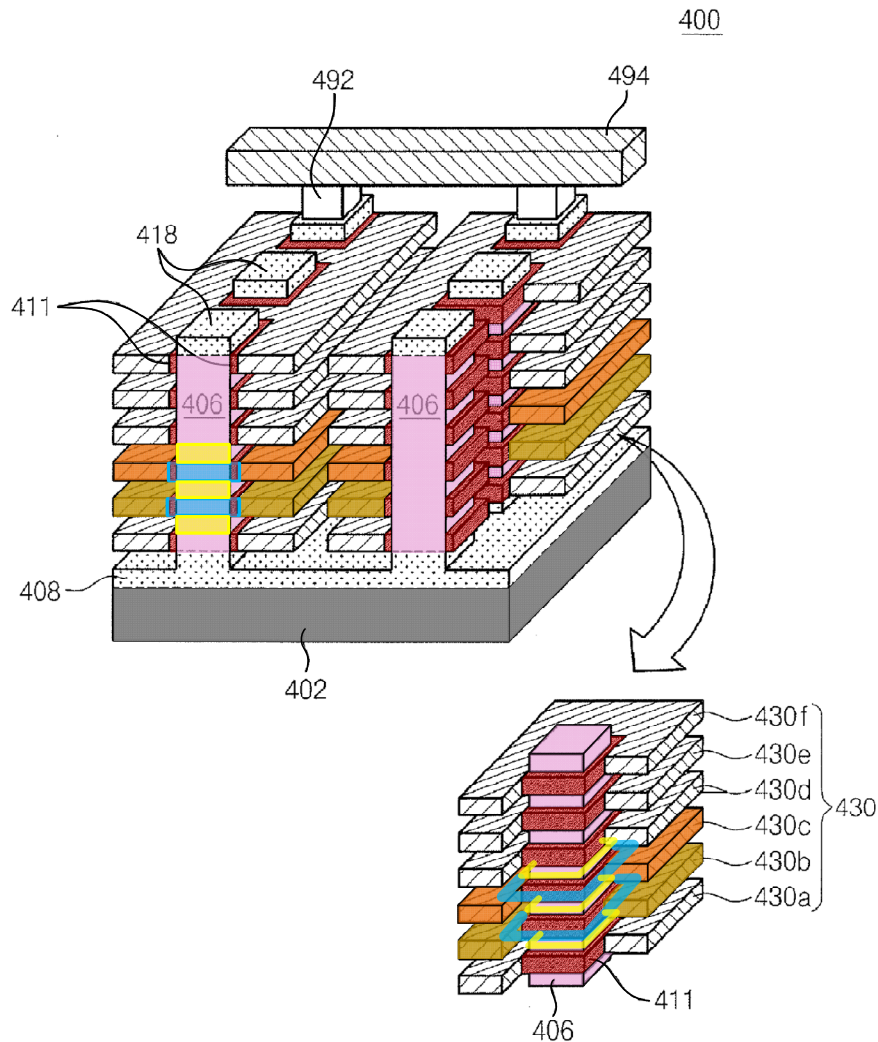


FIG. K – FIG. 1E of Kang (annotated)

99. As I discussed in Section VII.C, if the claim term “cavity” is construed to require that the hole within the control gate has a larger diameter than the corresponding holes in the layers above and below the control gate, Kang’s disclosure remains consistent with this interpretation. Specifically, Kang states that charge storage layer 411 has “a separated shape divided according to each of the

gates 430*a* through 430*f*” and that “a charge storage layer is divided according to each gate, so an operation error can be substantially reduced.” EX1004, [0061], [0111].

100. It is noted that, FIG. 1E does not show insulating layers 460/260 between adjacent control gates 430, as “FIG. 1E is the nonvolatile memory device 400 from which the insulating layers 460 is removed.” EX1004, [0101]. A POSITA would have understood that in FIG. 1E, those recesses that are vertically between adjacent control gates 430 and laterally contacting active pillars 406 represent insulating layers 460. EX1004, [0087], [0101].

101. Given the above disclosure, a POSITA would understand—or at the very least find it obvious—that, as illustrated in FIG. K above, the holes (in blue) in each of control gates 430*b* and 430*c* (in brown and orange, respectively) possess a larger diameter than the corresponding holes (in yellow) in insulating layers 460 located above and below the respective control gate 430*b* or 430*c*.

102. Therefore, it is my opinion that Kang discloses the subject matter of elements [1.d] and [1.e].

[1.f] data lines configured to be selectively coupled to a common source and the memory cells through conductive material

103. As illustrated in FIG. 1E of Kang below (FIG. L of my Declaration with annotations), bit lines 494 (in green) are electrically connected to a source 408

(in purple) and first and second groups of memory transistors (enclosed within brown and orange dashed boxes) via active pillars 406 (in pink). EX1004, [0059]-[0060]. It is clear to me that bit lines 494 qualify as the claimed “data lines” at least because the ’214 patent describes that “[d]ata lines 251, 252, and 253 sometimes correspond to bit lines or sense lines of a non-volatile memory device.” EX1001, 3:29-31.

Fig. 1E

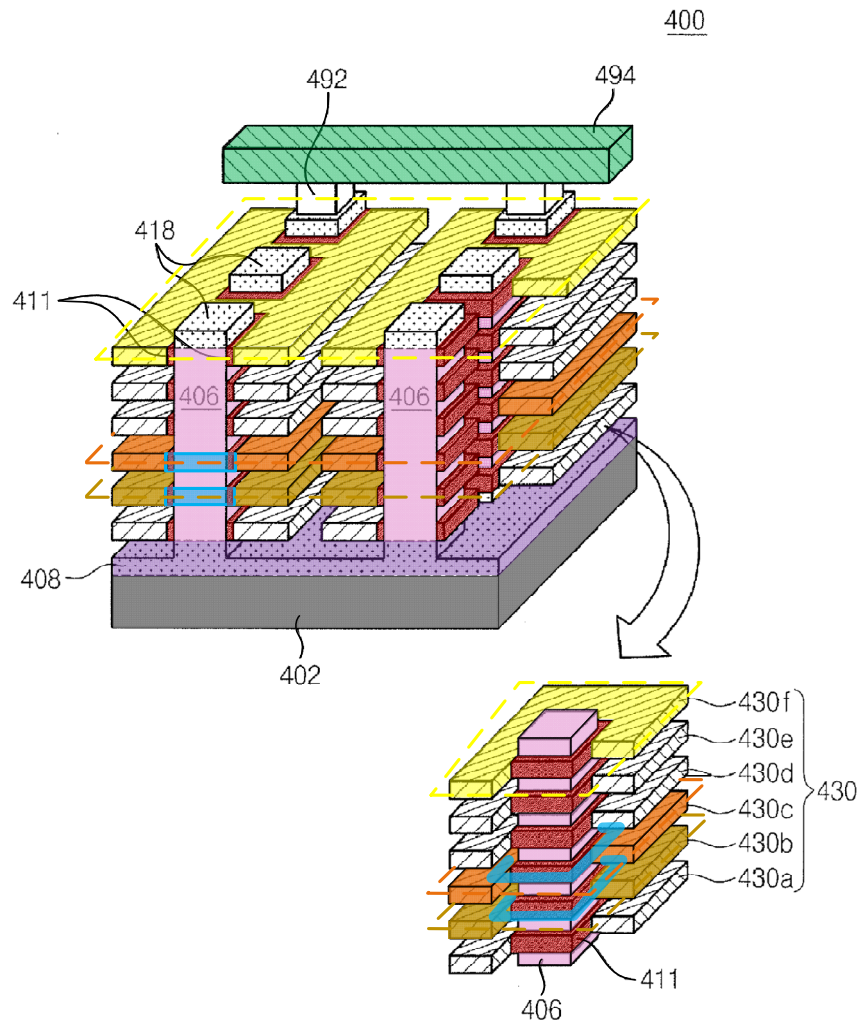


FIG. L – FIG. 1E of Kang (annotated)

104. A POSITA would recognize that source 408 is shared among multiple active pillars 406, functioning as a common source for multiple cell strings. Kang explicitly describes such a configuration where the source is connected through a “common source line,” which is indicative of a “common source” structure. EX1004, [0037]. This common source arrangement can facilitate the uniform operation of the memory array by ensuring a stable electrical reference across multiple memory transistors.

105. Kang further discloses that bit lines 494/194 are electrically connected to active pillars 406/106 through upper select transistors, such as upper select transistor 135 (enclosed within the yellow dashed box). These upper select transistors include upper select gates 430f/130f (in yellow), which are electrically connected to an upper select line driving circuit. EX1004, [0037], [0041], [0060], FIGs. 1A, 1B, and 1E. It is noted that, for clarity and ease of reference in this Declaration, those common features across different embodiments of Kang may be collectively referred to in my Declaration using their respective numerical labels from those embodiments, e.g., bit lines 494/194.

106. Therefore, a POSITA would understand that the electrical connection between bit lines 494 and active pillars 406 is controlled by the upper select transistors. Specifically, the upper select line driving circuit is responsible for selecting or deselecting each cell string by toggling the upper select gates 430f of the

corresponding upper select transistors. By activating or deactivating these gates, the circuit controls whether the bit lines 494 are electrically coupled to the memory transistors and the common source 408 via active pillars 406. EX1004, [0037], [0041], [0045]. Thus, Kang discloses a configuration in which bit lines 494 are “selectively” coupled to the memory transistors and the common source.

107. Kang further discloses that active pillar 406/106 includes “a single crystalline silicon of p-type.” EX1004, [0034]. Likewise, the ’214 patent also describes that “a **conductive material** 2001 has been formed by, for example, depositing **undoped or lightly doped polysilicon** to place channels 1841 in **electrical communication** with pillars 705.” EX1001, 8:64-67. Therefore, it is clear to me that Kang’s active pillar 406 having p-type doped single crystalline silicon includes the claimed “conductive material,” which also encompasses “undoped or lightly doped polysilicon in electrical communication with pillars 705.”

108. Therefore, it is my opinion that Kang discloses or at least suggests “data lines configured to be selectively coupled to a common source and the memory cells through conductive material.”

B. Dependent Claim 2: *The apparatus of claim 1, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.*

109. As illustrated in annotated FIG. 1E below (FIG. M of my Declaration with annotations), Kang discloses that each of the first and second groups of memory transistors (enclosed within the brown and orange dashed boxes) are arranged in an array with multiple memory transistors aligned along the X-direction (corresponding to the word line direction) and the Y-direction (corresponding to the bit line direction) perpendicular to the X-direction. This arrangement is further supported by Kang's disclosure in EX1004, [0040], [0042], FIG. 1B.

Fig. 1E

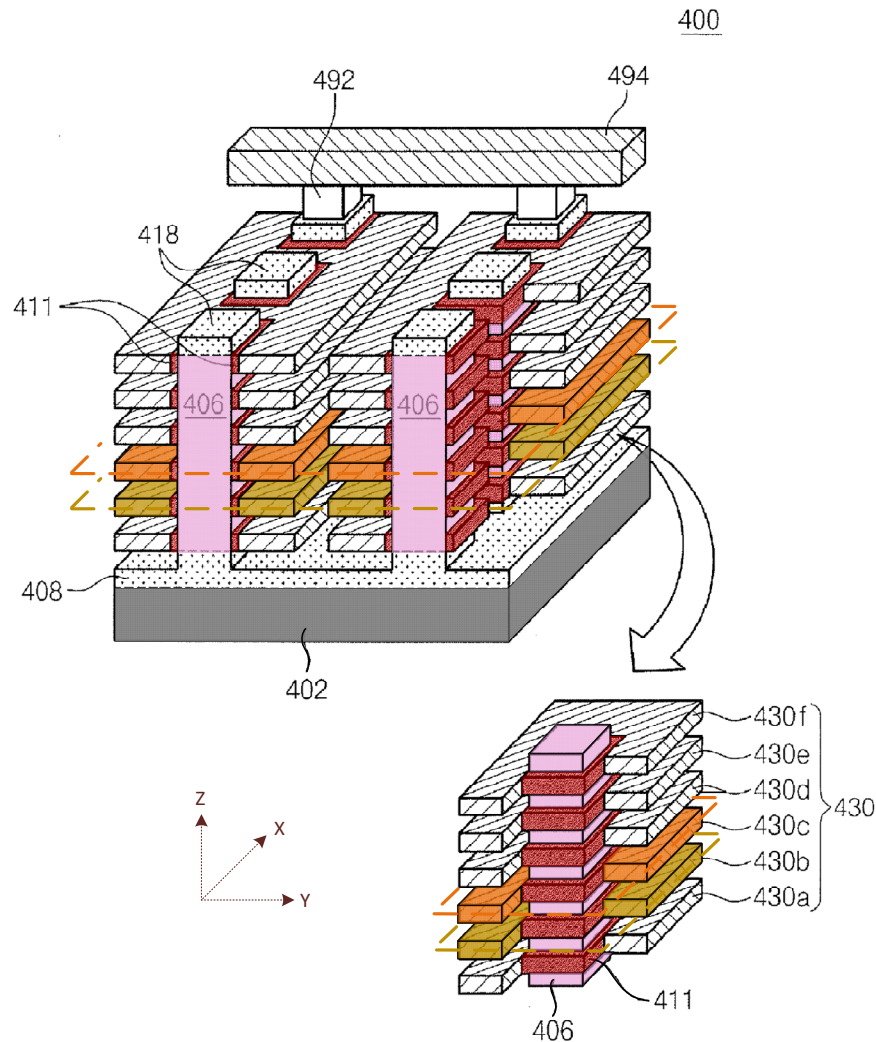


FIG. M – FIG. 1E of Kang (annotated)

110. Furthermore, Kang describes that active pillar 406 extends through the first and second levels where the first and second groups of memory transistors are located along a Z-direction/vertical direction, which is perpendicular to both the word line direction/X-direction and bit line direction/Y-direction. EX1004, [0034], [0060]. This vertical extension of active pillar 406 through multiple device levels

each having a group of memory cells meets the claim limitation of “extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions” of claim 2.

111. Therefore, it is my opinion that Kang discloses the subject matter of claim 2.

- C. Dependent Claim 3: *The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.***

112. As illustrated in annotated FIG. 1E below (FIG. N of my Declaration with annotations), Kang discloses that source 408 (in purple) is positioned over substrate 402 (in gray) and below the first and second groups of memory transistors (enclosed in brown and orange dashed boxes). In other words, source 408 is located between the first and second memory cells and substrate 402 along the vertical direction. EX1004, [0059]-[0060].

Fig. 1E

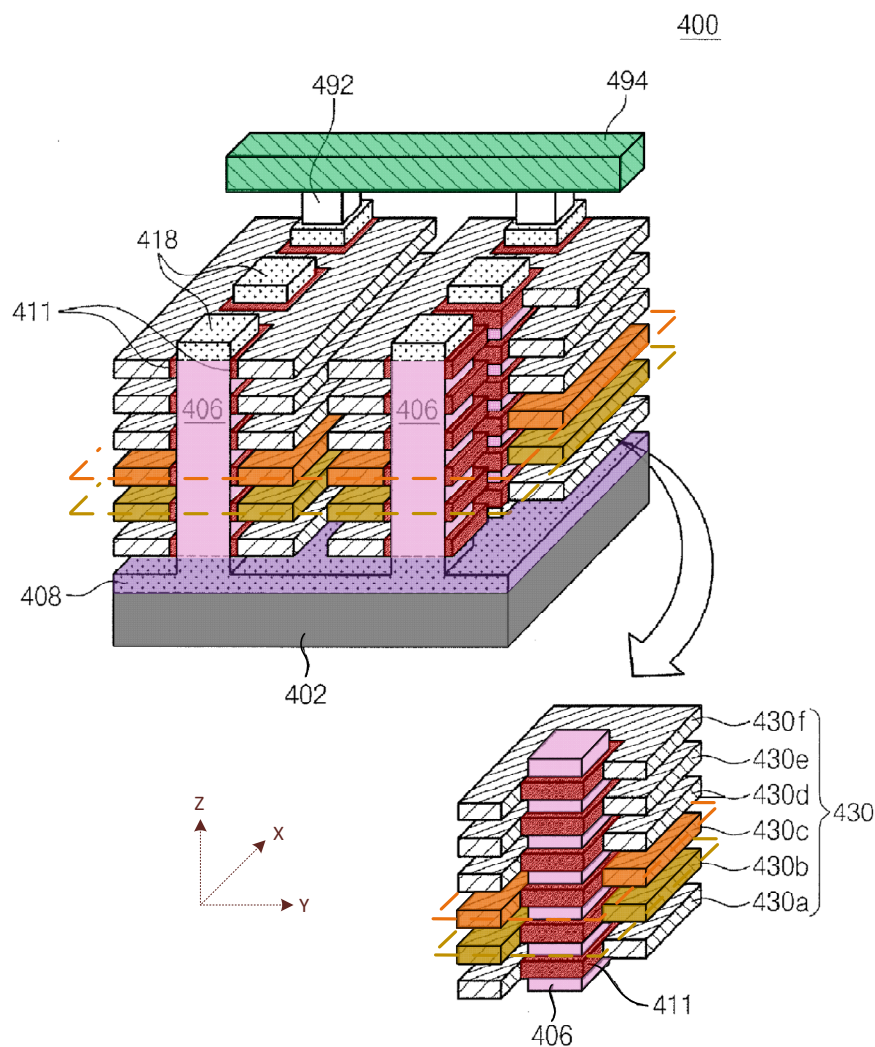


FIG. N – FIG. 1E of Kang (annotated)

113. I noted that the '214 patent characterizes the claimed erase operation as one of the well-known operations that a POSITA would recognize, and it omits detailed descriptions of the erase operation to focus on other aspects of the disclosure. EX1001, 3:54-64, 10:44-60.

114. I further noted that Kang explicitly describes that “electrons generated

by GIDL are discharged to the semiconductor substrate 102” and that “electrons accumulated in the memory transistor 133 are discharged, so data erasing operation can be embodied.” EX1004, [0048]. A POSITA would have understood, or at least found it obvious, that during an erase operation in Kang’s nonvolatile memory device 400, electrons stored in the silicon nitride layer of charge storage layer 411 (in red) are discharged to substrate 402/102 (in gray) through source 408 (in purple). EX1004, [0038]. This discharge pathway aligns with the requirement that electrons from the memory element of at least one of the first and second memory cells move to the common source during an erase operation.

115. Given Kang’s explicit teachings regarding electron discharge during erase operations and the common source’s position relative to the substrate and memory cells, it is my opinion that Kang discloses or otherwise renders obvious the subject matter of claim 3.

D. Dependent Claims 4 and 5: *The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells. & The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.*

116. Kang explicitly describes that memory transistors are vertically and serially connected to form a cell string, with each active pillar 406/106 extending vertically through gate group 430/130. EX1004, [0041]. Furthermore, Kang discloses that the silicon nitride layer within charge storage layer 411/110 of each

memory transistor in a given cell string surrounds one side of active pillar 406/106.
EX1004, [0038], [0041].

117. As shown in annotated FIG. 1E below (FIG. O of my Declaration with annotations), a POSITA would have understood that the memory transistors in each cell string are substantially vertically aligned, thereby satisfying the requirement of claim 4 that “the first memory cells are substantially vertically aligned with the second memory cells.” Additionally, because the charge storage layers 411 (in red), which contain the silicon nitride layers, surround active pillar 406 along its vertical axis, the charge storage layers 411 are likewise vertically aligned, thereby meeting the requirement of claim 5 that “the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.”

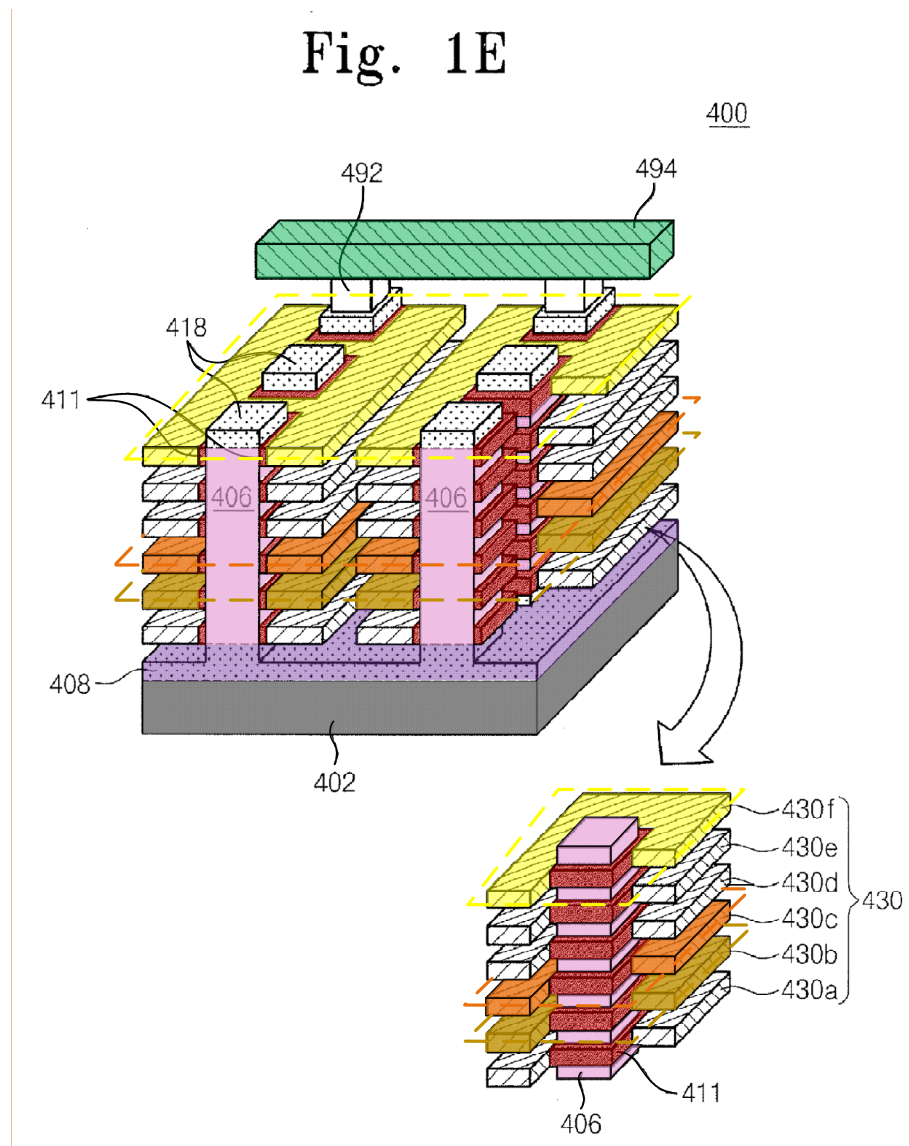
E. Dependent Claim 6: *The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.*

119. I have noted that claim 6 depends on claim 1 and further requires that the memory device includes “transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation” [6.a], and that “at least one of the transistors comprises a double-gate” [6.b].

120. As I discussed in Section IX.A, Kang’s FIG. 1E embodiment alone discloses or at least suggests the subject matter of claim 1.

121. As shown in FIG. P below with my annotations on FIG. 1E, Kang also discloses upper select transistors (e.g., 135, enclosed in yellow dashed box), which include upper select gates 430f/130f (in yellow) electrically connected to an upper select line driving circuit. EX1004, [0037], [0041], [0060], FIGs. 1A, 1B, 1E. A POSITA would have understood that the electrical connection between bit lines 494 (in green) and active pillars 406 (in pink) is controlled by the upper select transistors. EX1004, [0041], [0045]. A POSITA would have also understood that the upper select line driving circuit selects/deselects each cell string including the first and second memory cells, by turning the upper select transistors on or off during

a memory operation, in order to control the connections between bit lines 494 and active pillars 406, through upper select gates 430*f* of the corresponding upper select transistors. EX1004, [0037]. Therefore, Kang's FIG. 1E embodiment discloses the subject matter of element [6.a].



122. Kang's embodiment in FIG. 1C further explicitly discloses that “gate

group 230 may include a lower select gate 230*a*, an upper select gate 230*f*... formed to have **a line shape on both sides** of active pillar 206.” EX1004, [0052], FIG. 1C. A POSITA would understand the upper select gate 230*f* in Kang’s FIG. 1C embodiment qualifies as the claimed “double-gate,” and the upper selection transistor including upper select gate 230*f*, qualifies as the claimed “at least one of the transistors comprising a double-gate.”

123. Furthermore, a POSITA would have been motivated to modify Kang’s FIG. 1E embodiment by incorporating the double-gate-type upper select gate 230*f* from FIG. 1C as a replacement to the surrounded-gate-type upper select gate 430*f*, while keeping the surrounded-gate configuration for control gates 430*b*-430*e*. This modification, as illustrated in the annotated and modified FIG. 1E of Kang below (FIG. Q of my Declaration, with my modifications and annotations to FIG. 1E of Kang), would provide the predictable advantages.

Fig. 1E

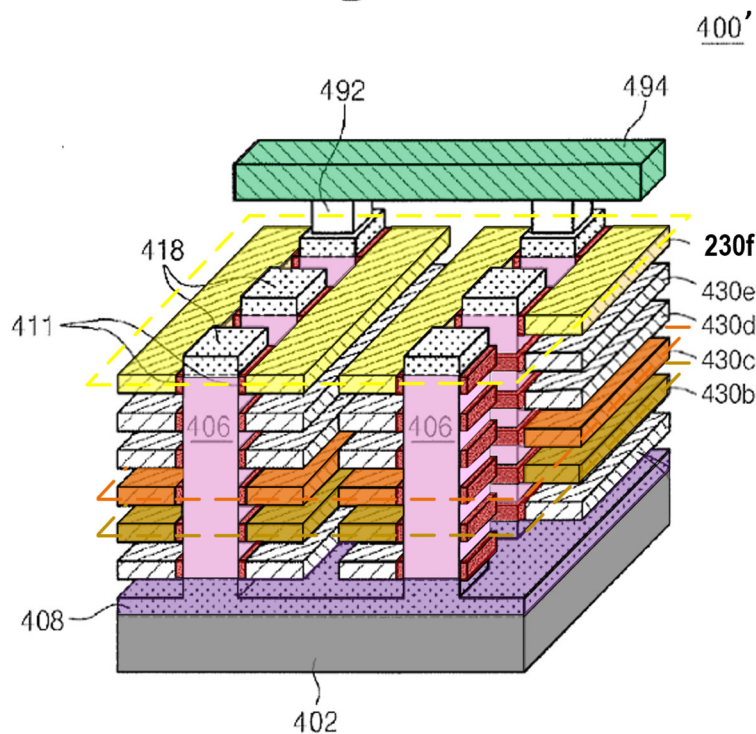


FIG. Q – FIG. 1E of Kang (annotated and modified)

124. By replacing the surrounded-gate-type upper select gate 430f with a double-gate-type structure, this adjustment would reduce gate and parasitic capacitance, which in turn improves switching speed and power efficiency. The reduced parasitic capacitance minimizes delays and enhances the overall performance of the memory cell by lowering power consumption during read and write operations. Additionally, this change would mitigate unwanted parasitic effects, particularly those arising from electric field overlapping between the drain and gate regions. Such overlap can lead to unintended leakage currents and degraded electrical performance, negatively impacting the reliability and stability of the

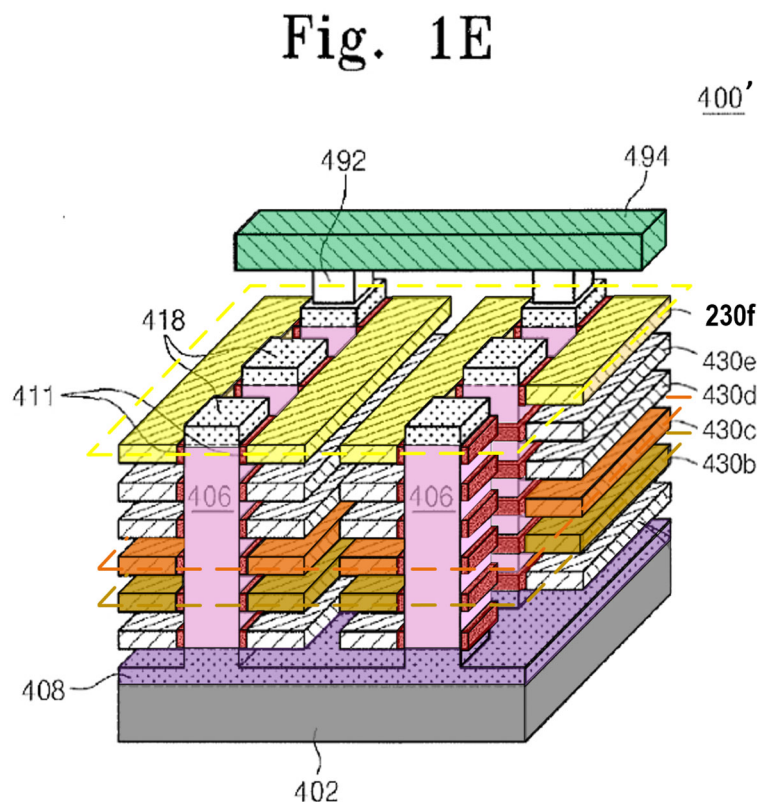
memory device. A POSITA would recognize that this modification aligns with well-known industry practices aimed at optimizing transistor performance by balancing control gate effectiveness with minimized parasitic influences.

125. Moreover, the feasibility of implementing a double-gate structure in select transistors is well-established, making the modification technically achievable. A POSITA would have had a reasonable expectation of success in implementing this modification, given that the use of a double-gate structure for selection transistors was well-documented and widely recognized in the art prior to the '214 patent. Numerous publications describe the benefits and feasibility of double-gate transistors in similar applications. See, e.g., EX1015, [0103]-[0106], FIGs. 31, 36, 37; EX1016, [0075]-[0080], FIG. 11; EX1017, [0012]; and EX1019, [0070], FIGs. 6-7, 12.

126. Moreover, implementing this modification would not have required fundamental changes to the overall fabrication process. Given the structural similarities between the double-gate and surrounded-gate configurations, a POSITA would recognize that the substitution could be seamlessly integrated into existing process flows with minimal design adjustments that are well-within their capabilities. The well-documented nature of double-gate transistors in prior art further reinforces that this modification would have been straightforward and achievable without undue experimentation, making it an evident and advantageous improvement for

optimizing the performance of the memory device.

127. As shown in FIG. Q , which is repeated below, bit lines 494 (in green) are electrically connected to the first and second groups of memory transistors (enclosed in brown and orange dashed boxes) via active pillars 406 (in pink). EX1004, [0059]-[0061]. The bit lines 494 are further connected to the active pillars 406 through modified upper select transistors (enclosed in yellow dashed box), which include double-gate-type upper select gates 230f (in yellow) electrically connected to an upper select line driving circuit. EX1004, [0037], [0041], [0052], FIGs. 1A-1C.



128. That is, bit lines 494 are coupled with the first and second groups of memory transistors via the modified upper select transistors, and that the upper select line driving circuit controls the selection and deselection of each cell string by toggling the connections between bit lines 494 and the memory transistors through upper select gates 230f of the corresponding modified upper select transistors. EX1004, [0045].

129. Accordingly, Kang's modified FIG. 1E embodiment, in view of FIG. 1C embodiment, renders obvious upper select transistors comprising a double-gate upper select gate 230f, which is configured to "selectively" couple the first and second groups of memory transistors to bit lines 494 during a memory operation of nonvolatile memory device 400.

130. For these reasons, it is my opinion that a POSITA would have found claim 6 obvious in view of Kang's modified FIG. 1E embodiment, which is modified in view of FIG. 1C embodiment.

F. Dependent Claim 7: *The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.*

131. In Kang's FIG. 1E embodiment, as shown below in FIG. R of my Declaration with annotations, bit lines 494 (in green) are electrically connected to

the first and second groups of memory transistors (enclosed in brown and orange dashed boxes) via upper select transistors (e.g., 135, enclosed in the yellow dashed box). A POSITA would have understood that the electrical connection between bit lines 494 (in green) and active pillars 406 (in pink) is controlled by the upper select transistors. EX1004, [0041], [0045]. A POSITA would have also understood that the upper select line driving circuit selects/deselects each cell string including the first and second memory cells, by turning the upper select transistors on or off during a memory operation, to control the connections between bit lines 494 and active pillars 406, through upper select gates 430 of the corresponding upper select transistors. EX1004, [0037].

Fig. 1E

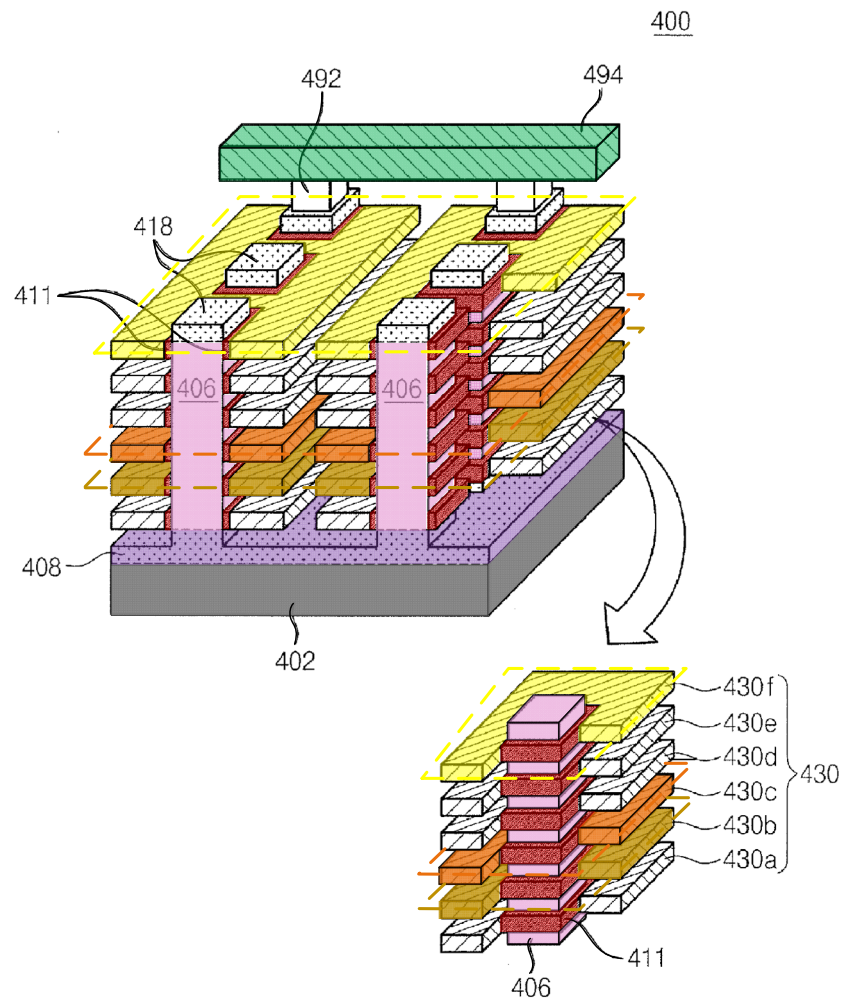


FIG. R – FIG. 1E of Kang (annotated)

132. Accordingly, Kang’s FIG. 1E embodiment alone discloses that the upper select transistors are configured to “selectively” couple the first and second groups of memory transistors to bit lines 494 during a memory operation of nonvolatile memory device 400.

133. Furthermore, Kang’s FIG. 1E embodiment explicitly discloses that “gate group 430 may include a lower select gate 430a, an upper select gate 430f ...

formed to have **a horizontal plate shape**” and that “active pillar 406 may vertically **penetrate** the gate group 430.” EX1004, [0060], FIG. 1E. It is clear to me from this disclosure, as well as in view of FIG. 1E, that the upper select transistors include upper select gate 430f, which surrounds active pillar 406. A POSITA would understand the upper select gate 430f in Kang’s FIG. 1E embodiment qualifies as the claimed “surrounded gate,” and the upper selection transistor including upper select gate 430f, qualifies as the claimed “at least one of the transistors comprising a surrounded gate.”

134. Thus, Kang’s FIG. 1E embodiment alone discloses the subject matter of claim 7.

G. Independent Claim 9

135. Claim 9 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[9.P] An apparatus comprising:

[9.a] a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device;

[9.b] a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level;

[9.c] a conductive material extending through the first and second memory elements; and

[9.d] a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material.

[9.P] An apparatus comprising

136. As I discussed in Section IX.A([1.P]), Kang discloses “[a]n apparatus.”

[9.a] a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device

[9.b] a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level

137. As I discussed in Section IX.A([1.b]-[1.e]), Kang discloses “a plurality of first/second memory cells located in a first/second device level of the memory device over the substrate, wherein the first device level is different from the second device level,” and “each of the first/second memory cells includes a memory element.”

138. Kang’s FIG. 1E embodiment describes **nonvolatile** memory device 400, which includes multiple groups of memory transistors arranged at different device levels. EX1004, [0059]. Since memory device 400 to which the first and second groups of memory transistors belong is a **nonvolatile** memory, each of first and

second groups of memory transistors is a claimed “non-volatile memory cell.”

139. Additionally, Kang discloses that each memory transistor includes a charge storage layer. Specifically, Kang states that “charge storage layer 411 may have a **ring** or band shape surrounding a side of active pillar 406.” EX1004, [0061], FIG. 1E. A POSITA would have understood that charge storage layer 411, which includes a silicon nitride layer, serves as the “memory element” for each nonvolatile memory cell. Kang further discloses that an insulating layer 110 from which charge storage layer 411/111 is formed, is “**conformally** formed using a deposition process,” including “chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process,” and insulating layer 110 includes “an oxide layer-a nitride layer-an oxide layer, for example, an ONO layer that a silicon nitride layer or a silicon oxynitride layer is inserted between silicon oxide layers.” EX1004, [0066]. Thus, a POSITA would have understood, or at least found it obvious that, the silicon nitride layer that is conformably deposited as the middle layer of insulating layer 110, for example, using ALD, has the same “ring or band shape” as charge storage layer 411.

140. Accordingly, Kang discloses or at least suggests the subject matter of elements [9.a] and [9.b].

[9.c] a conductive material extending through the first and second memory elements

[9.d] a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material

141. As I discussed in Sections X.A([1.f]) and IX.B above, Kang discloses or at least suggests “data lines configured to be selectively coupled to a common source and the memory cells through conductive material” and “the conductive material extending through the first and second memory cells in a third direction.” Thus, Kang also discloses or at least suggests the subject matters of elements [9.c] and [9.d].

H. Dependent Claim 10: *The apparatus of claim 9, further comprising: a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in the first device level of the memory device; and a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in the second device level of the memory device.*

142. As I explained in Section IX.A([1.d]-[1.e]) above, Kang discloses “a first/second control gate formed in the first/second device level, the first/second control gate to control access to the first/second memory cells.” Kang further states that “conductive group 130 may be comprised of a conductor, e.g., silicon, metal, or combinations thereof so that the conductive group 130 is used as a gate,” and that

“the medium conductive layers 130b through 130e may be used together with the term ‘control gate.’” EX1004, [0036], [0038], [0060].

143. Accordingly, Kang discloses first control gate 430b/130b, which operates as a first additional conductive material to access the first group of memory transistors, and second control gate 430c/130c, which operates as a second additional conductive material to access the second group of memory transistors. These disclosures satisfy the limitations of claim 10.

I. Dependent Claims 11 and 12: *The apparatus of claim 10, wherein each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material. & The apparatus of claim 11, wherein each of the first and second memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.*

144. Kang discloses that each memory transistor includes charge storage layer 411/111 having “an ONO structure, an ONO layer, [including] a silicon nitride layer [which] may actually trap charges to store data and any one of two silicon oxide layers [which] may be used as a tunnel insulating layer and the other [which] may be used as a blocking insulating layer,” where “a silicon nitride is interposed between the silicon oxide layers.” EX1004, [0035], [0066].

145. Thus, a POSITA would have understood, or at least found it obvious, that each memory transistor in Kang includes: (i) a first silicon oxide layer of charge storage layer 411 located between the respective silicon nitride layer of charge

storage layer 411 and active pillar 416, and (ii) a second silicon oxide layer of charge storage layer 411 between the respective silicon nitride layer of charge storage layer 411 and the respective control gate 430*b* or 430*c*.

146. The ONO structure disclosed in Kang, with silicon nitride interposed between two silicon oxide layers, is a well-known configuration in the field of nonvolatile memory devices and would have been readily understood by a POSITA at the time of the invention. Therefore, a POSITA would have recognized that Kang discloses, or at the very least suggests, the claimed subject matter in claims 11 and 12.

J. Dependent Claim 14: *The apparatus of claim 9, wherein the first and second memory cells are located between the substrate and the data line.*

147. Kang further discloses that the first and second groups of memory transistors are positioned vertically between the semiconductor substrate 402 and the bit lines 494. EX1004, [0059]. As illustrated in annotated FIG. 1E below (FIG. S of my Declaration with annotations), the first and second memory cells (enclosed in brown and orange dashed boxes, respectively) are arranged between the semiconductor substrate 402 (in gray) and the bit lines 494 (in green). Therefore, Kang discloses the subject matter of claim 14.

Fig. 1E

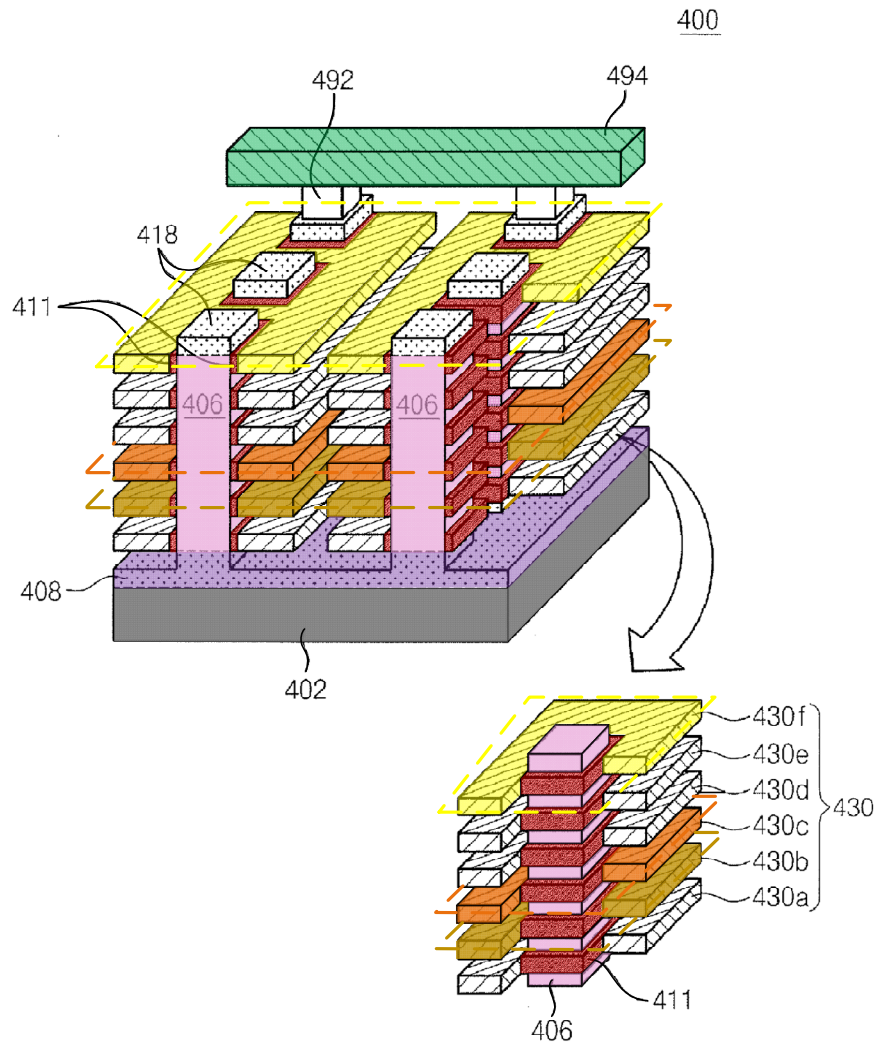


FIG. S – FIG. 1E of Kang (annotated)

K. Independent Claim 15

148. Claim 15 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[15.P] An apparatus comprising:

[15.a] a substrate of a memory device;

[15.b] a first conductive material located in a first device level of the

memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall;

[15.c] a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level;

[15.d] a first dielectric formed on the first sidewall and the second sidewall;

[15.e] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

[15.f] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

[15.g] a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

[15.h] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

[15.P] An apparatus comprising

149. As I discussed in Section IX.A([1.P]), Kang discloses “[a]n apparatus.”

[15.a] a substrate of a memory device

150. As I discussed in Section IX.A([1.a]), Kang discloses “a substrate of a memory device.”

[15.b] a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall

[15.c] a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level

151. As I discussed in Section IX.A([1.b]-[1.e]), Kang discloses “a first/second control gate formed in the first/second device level,” “a cavity of the first/second control gate,” and “the first device level is different from the second device level.”

152. Kang further discloses that first and second control gates 430b/130b and 430c/130c are “formed of a conductor such as silicon or metal.” EX1004, [0069]. Likewise, as to the claimed “first/second conductive material located in a first/second device level, ... including a first/second cavity” recited in claim 15, the specification of the '214 patent describes that “[m]aterials 1002, 1004, and 1006 can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon),” and “[f]orming cavities 1120 in materials 1002, 1004, and 1006

also form control gates 1221, 1222, and 1223, which can correspond to control gates control gates 221, 222, and 223 of FIG. 2.” EX1001, 7:3-5, 39-42. Thus, it is clear to me that the metal or silicon control gates 430*b* and 430*c* qualify as the claimed “first conductive material” and “a second conductive material,” respectively, according to the ’214 patent.

153. Further, a POSITA would have understood, at least found it obvious, that the hole in which corresponding parts of active pillar 406 and charge storage layer 411 are formed has a respective sidewall on first or second control gate 430*b* or 430*c* under either party’s interpretation of the claimed “cavity.” EX1004, FIG. 1E; See Sections VII.C, IX.A([1.d]-[1.e]).

154. Therefore, it is my opinion that Kang discloses or at least suggests the claim subject matter of elements [15.b] and [15.c].

[15.d] a first dielectric formed on the first sidewall and the second sidewall

[15.e] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric

[15.f] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric

[15.g] a second dielectric formed on a side of the first memory element and on a side of the second memory element

155. As I discussed in Section IX.A([1.d]-[1.e]), Kang discloses that “each of the first/second memory cells includes a memory element formed in a cavity of

the first/second control gate.” Kang further discloses that charge storage layer 411 can be “an ONO layer” in which the silicon nitride layer is “inserted between silicon oxide layers” laterally. EX1004, [0038], [0066]. That is, “N” represents a silicon nitride layer, and each “O” represents one of two silicon oxide layers.

156. A POSITA would have understood, or at least found it obvious, that a first silicon oxide layer (“O”) of charge storage layer 411 is formed on the sidewalls of the holes through which active pillar 416 and charge storage layers 411 penetrate. A POSITA would further have understood, or at least found it obvious, that a second silicon oxide layer (“O”) of charge storage layer 411 is formed on the sides of the corresponding silicon nitride layers (“N”). Therefore, Kang explicitly discloses claim elements [15.d] and [15.g].

157. Given that the silicon nitride layer is laterally inserted between silicon oxide layers within the ONO structure of charge storage layer 411, a POSITA would have understood, or at least found it obvious, that the silicon nitride layer within a respective charge storage layer 411 is electrically isolated from the corresponding first or second control gate 430*b* or 430*c* by a respective portion of the first silicon oxide layer functioning as a first dielectric, satisfying the requirements of claim elements [15.e] and [15.f].

158. Accordingly, it is my opinion that Kang discloses or at least suggests the claimed subject matter of elements [15.d]-[15.g].

[15.h] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric

159. Kang explicitly discloses that “nonvolatile memory device 400 may be a vertical NAND flash memory device” and that “gate group 430 us[es] active pillar 406 as a channel.” EX1004, [0059]. A POSITA would have understood that, during certain operations of the vertical NAND flash memory device, a channel forms in the vertical outermost layer of active pillar 406 and does not extend throughout the entire active pillar 406. Accordingly, Kang discloses the claimed “conductive channel.”

160. This understanding is well established in the art. For example, Sim discloses that “[a]pplication of the read voltage VREAD to the lower select line LSL causes vertical inversion regions 504B to be formed **along the outer walls** of lower portions of the vertical pillars PL formed of semiconducting material,” and “it can be seen that an inversion layer I is created **along the walls, or outer surface**, of the vertical pillars PL when a suitable word line voltage is applied to the word line plates WL_PT.” EX1015, [0063], [0070], FIG. 11 (reproduced below as FIG. T of my Declaration).

Fig. 11

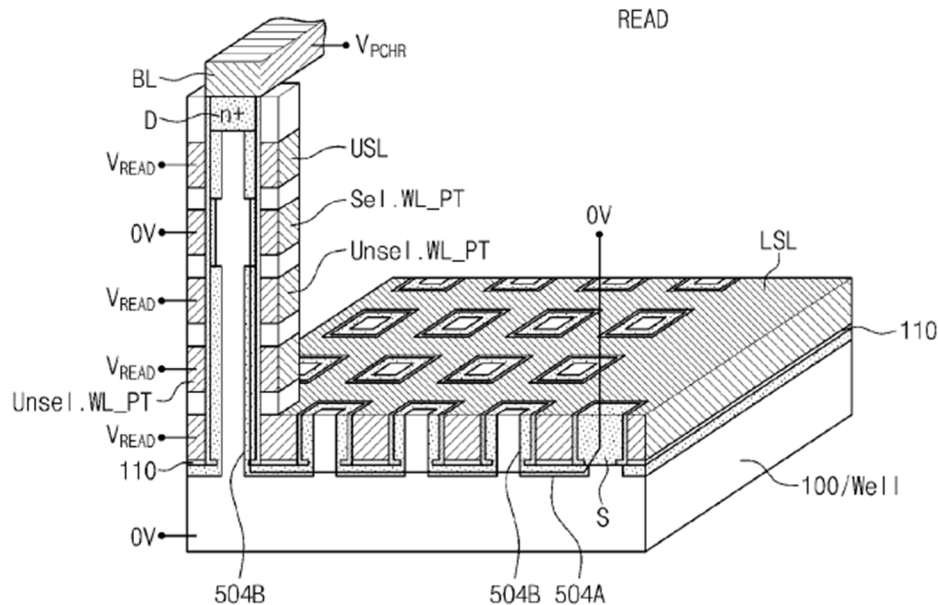


FIG. T – FIG. 11 of Sim

161. In addition, Kang discloses that “active pillar 406 may vertically penetrate the gate group 430.” EX1005, [0060]. As discussed in Section IX.A([1.d]-[1.e]), Kang further discloses that first and second control gates 430*b* and 430*c*, which are parts of gate group 430, are positioned in the first and second device levels. Therefore, Kang discloses that active pillar 406, including its vertical outermost layer, extends from the first device level to the second device level.

162. As I discussed in Sections IX.I and IX.K([15.g]), a POSITA would have understood, or at least found it obvious, that the second silicon oxide layer is formed

laterally between the corresponding silicon nitride layers and the vertical outermost layer of active pillar 406. This arrangement makes the vertical outermost layer of active pillar 406 face the silicon nitride layers but remain electrically isolated from them by the second silicon oxide layer.

163. Accordingly, Kang discloses or at least suggests the claimed subject matter of element [15.h].

L. Dependent Claim 16: *The apparatus of claim 16, wherein the first and second memory elements comprise polysilicon.*

164. Kang explicitly discloses silicon nitride layers (or silicon oxynitride layers) as part of charge storage layers 411, which qualify as the claimed “first and second memory elements.” EX1004, [0038].

165. A POSITA would have recognized that the selection of charge storage material is a matter of design choice, constrained by the known available options in the field. Specifically, at the time of the '214 patent, the three primary materials used for charge storage in 3D NAND memory devices were polysilicon, silicon nitride, and silicon oxynitride. EX1020, Table 1; EX1021, 2847, § I; EX1022, 189. A POSITA would have been aware of polysilicon as a viable alternative and understood that such a substitution would be a routine optimization based on the desired electrical characteristics of the memory device.

166. Specifically, a POSITA would have found it obvious to replace silicon

nitride or silicon oxynitride with polysilicon to form an “OPO” (oxide-polysilicon-oxide) structure for charge storage layer 411, as polysilicon was widely recognized as a standard material for memory elements at the time of the invention. This substitution would have been a logical design choice given the well-documented reliability concerns associated with silicon nitride and silicon oxynitride in charge-trapping applications.

167. At the time of the '214 patent, silicon nitride and silicon oxynitride were known to suffer from charge retention degradation over extended use, leading to reliability issues such as charge loss and data instability. EX1009, [0080]; EX1010, 1:46-56, 5:26-50; EX1012, 3.

168. In contrast, at the time of the '214 patent, polysilicon was well established as a reliable material for memory due to its superior charge retention capabilities and its ability to store and isolate charge more effectively over extended periods. A POSITA would have recognized that transitioning to a polysilicon structure in an OPO configuration could mitigate the known issues associated with silicon nitride, thereby enhancing device longevity and stability. This conclusion is further substantiated by the comparative analysis of EX1012 with EX1013, which demonstrates the improved charge retention characteristics of polysilicon over silicon nitride, and is further supported by EX1014.

169. Given these established industry understandings, a POSITA would

have had a reasonable expectation of success in making this substitution, as it represented a well-known and predictable design optimization within the field of 3D NAND memory development.

170. Accordingly, it would have been obvious to a POSITA to modify Kang's charge storage layer by replacing silicon nitride or silicon oxynitride with polysilicon, yielding a predictable and improved memory element.

171. Therefore, it is my opinion that Kang renders obvious claim 16.

M. Dependent Claims 17 and 18: *The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material. & The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.*

172. Kang explicitly discloses that charge trapping layer 411/111 includes a silicon nitride layer, which is used to "trap charges to store data." EX1004, [0038]. Thus, it is my opinion that Kang discloses the claimed subject matter of claims 17 and 18.

N. Dependent Claim 19: *The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.*

173. Kang explicitly discloses that insulating layers 460/260 fill trenches 240, which are located vertically between control gates 430b-430e that are positioned in different device levels. EX1004, [0087], [0101]. It is clear to me that insulating layers 460/260 include claimed "dielectric material."

174. Thus, it is my opinion that Kang discloses the claimed subject matter of claim 19.

O. Dependent Claim 20: *The apparatus of claim 15, further comprising: a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.*

175. As I discussed in Section IX.A([1.a.f]), Kang discloses that bit line 494 is configured to be selectively coupled to active pillar 406 via the upper select transistor. A POSITA would have understood, or at least found it obvious, that bit line 494 is also configured to be selectively coupled to the vertical outermost layer of active pillar 406.

176. Furthermore, Kang discloses in FIG. 1E that the silicon nitride layers in charge storage layers 411 of the first and second groups of memory transistors are positioned vertically between bit line 496 and semiconductor substrate 402. EX1004, FIG.1E.

177. Thus, it is my opinion that Kang discloses the claimed subject matter of claim 20.

X. Ground 3: Kang In View of Ahn Renders Obvious Claim 16

178. As I discussed in Section IX.K, Kang anticipates or otherwise renders obvious claim 15 on which claim 16 depends. To the extent further disclosure is required for claim 16, my opinion is that Kang in view of Ahn renders claim 16

obvious.

179. Kang discloses the claimed “the first and second memory elements” being silicon nitride layers or silicon oxynitride layers. EX1004, [0038]. Ahn further explicitly teaches that “a charge trap layer is formed by depositing, for example, a silicon nitride film or a polysilicon film to a thickness of 10 to 1,000 Å on the blocking layer formed on the inner wall of the through hole (430). The charge trap layer can be deposited using atomic layer deposition (ALD) or chemical vapor deposition (CVD).” EX1006, [0067].

180. I observe that Kang and Ahn are analogous prior art in the same field as the '214 patent, which relates to nonvolatile memory devices. EX1001, 1:6-8; 2:63-67; EX1004, [0002]; EX1006, [0001]. Additionally, both Kang and Ahn address the purported problem of increasing the integration or density of memory devices. EX1001, 1:7-22; EX1004, [0003]-[0004]; EX1006, [0005]. Given their shared focus on nonvolatile memory technology and integration density, a POSITA would have considered Ahn's disclosure relevant to Kang's memory device structure.

181. In my opinion, it would have been obvious to apply Ahn's teachings of a polysilicon charge trap layer to Kang's charge storage layer 411 because polysilicon was commonly used for memory elements at the time of the '214 patent. Moreover, the selection among polysilicon, silicon nitride, and silicon oxynitride for forming the charge trap layer was a known design choice. See Section IX.L.

182. A POSITA would have been motivated to replace Kang's silicon nitride layer with Ahn's polysilicon layer because polysilicon offered better reliability and data retention compared to silicon nitride in flash memory devices at the time of the '214 patent. EX1009, [0080]; EX1010, 1:46-56, 5:26-50; EX1012, 3; see Section IX.L. Given these advantages, a POSITA would have recognized that substituting polysilicon for silicon nitride in Kang's charge storage layer 411 would improve device performance.

183. Furthermore, a POSITA would have had a reasonable expectation of success in replacing the silicon nitride layer in Kang with Ahn's polysilicon layer, given the well-documented interchangeability of these materials for charge storage applications. Ahn explicitly states that its charge trap layer within the ONO (oxide-nitride-oxide) structure "is formed by depositing, for example, a silicon nitride film or a polysilicon film," confirming that both materials were viable alternatives for the same function. EX1006, [0067]. This statement directly suggests that the substitution of silicon nitride with polysilicon was not only known in the field but also an expected design variation depending on performance requirements.

184. Additionally, Ahn provides detailed guidance on the specific deposition parameters for forming a polysilicon charge trap layer, including a range of thickness values (e.g., "a thickness of 10 to 1,000 Å") and applicable deposition techniques such as atomic layer deposition (ALD) and chemical vapor deposition (CVD).

EX1006, [0067]. These parameters would have provided a POSITA with sufficient information to implement the material substitution without requiring undue experimentation.

185. A POSITA would have recognized that polysilicon offers advantages over silicon nitride in certain memory applications, particularly in terms of improved charge retention and reduced charge trapping degradation over extended use. Given that both Kang and Ahn address charge storage layers in similar memory structures, incorporating Ahn's polysilicon layer into Kang's device would have been a straightforward modification that leveraged known material properties and fabrication techniques. As a result, a POSITA would have had strong motivation and a reasonable expectation of success in making this substitution to improve the overall reliability and performance of the memory device.

186. Accordingly, it is my opinion that Kang in view of Ahn renders the subject matter of claim 16 obvious.

XI. Grounds 4 and 5: Fukuzumi Anticipates or Otherwise Renders Obvious Claims 1-7, 9-12, and 14-20

A. Independent Claim 1

[1.P] An apparatus comprising

187. Fukuzumi discloses a nonvolatile semiconductor memory device. EX1007, [0073]. Thus, Fukuzumi discloses an "apparatus."

[1.a] a substrate of a memory device

188. As shown in annotated FIG. 2 below (FIG. AA of my Declaration with annotations), Fukuzumi discloses a semiconductor substrate Ba (in gray) within a nonvolatile semiconductor memory device 100. EX1007, [0078], [0081], FIGs. 2, 4. Accordingly, Fukuzumi discloses “a substrate of a memory device.”

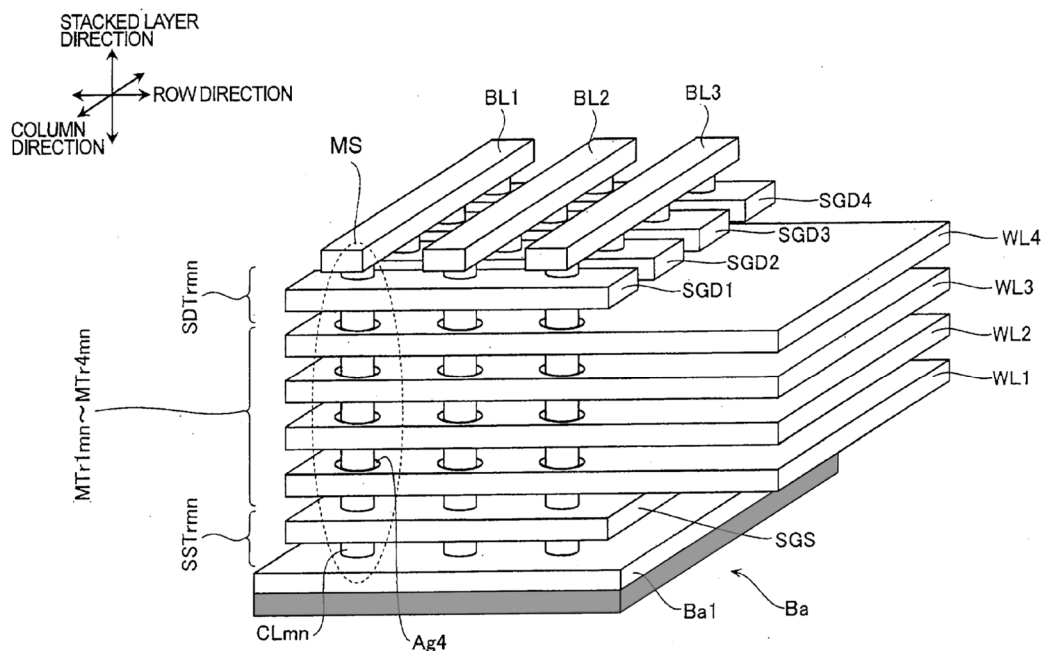


FIG. 2

FIG. AA – FIG. 2 of Fukuzumi (annotated)

189. As noted in Section VIII.C, although Fukuzumi describes nonvolatile semiconductor memory device 100 and its associated figures, including FIG. 2, in the context of the first embodiment, the disclosures regarding common features of nonvolatile semiconductor memory device 100 apply equally to the second embodiment. EX1007, [0146]-[0148]. Thus, a POSITA would have understood that

the teachings of Fukuzumi, as cited in Grounds 4-7, are applicable across embodiments, unless otherwise specified (e.g., with respect to memory layer 30 and word line conduction layers 36).

[1.b] a plurality of first memory cells located in a first device level of the memory device over the substrate

[1.c] a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level

190. Fukuzumi discloses that nonvolatile semiconductor memory device 100 includes memory cell strings MS, each of which includes memory cells MTr1 mn -MTr4 mn that are vertically and serially connected to each other. EX1007, [0079]-[0080], [0085].

191. As shown in annotated FIG. 2 below (FIG. AB of my Declaration with annotations), first memory cells MTr1 mn (enclosed within brown dashed box and corresponding to WL1) are located in a first device level of nonvolatile semiconductor memory device 100 over semiconductor substrate Ba (in gray), while second memory cells MTr2 mn (enclosed within orange dashed box and corresponding to WL2) are located in a second device level of nonvolatile semiconductor memory device 100 over both the first device level and semiconductor substrate Ba. EX1007, [0077], [0081].

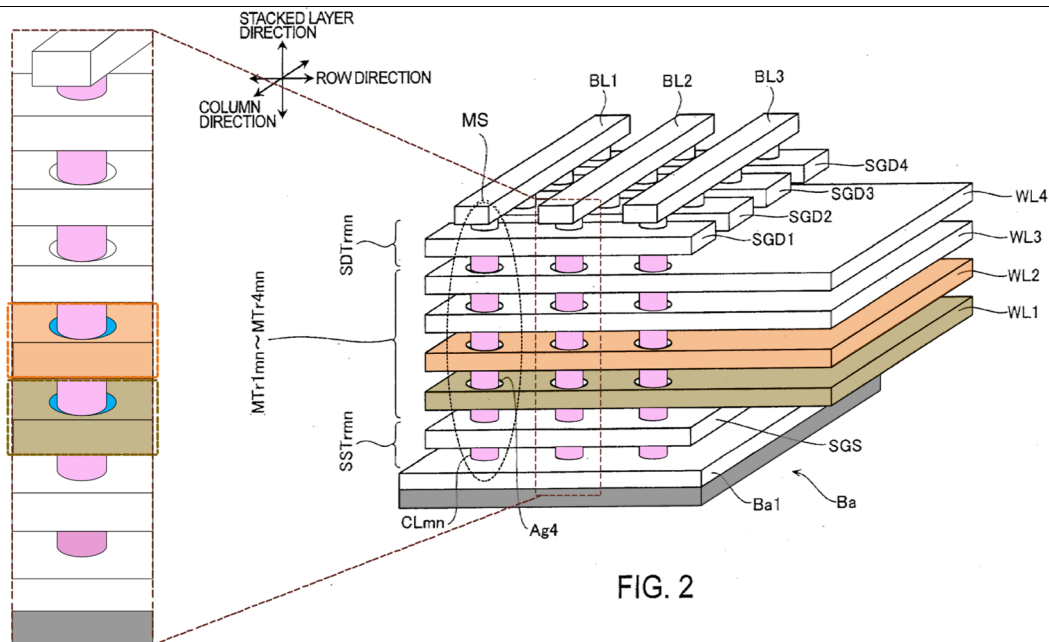


FIG. 2

FIG. AB – FIG. 2 of Fukuzumi

192. Accordingly, Fukuzumi discloses the claimed subject matter of elements [1.b] and [1.c].

[1.d] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate

[1.e] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate

193. Fukuzumi discloses that nonvolatile semiconductor memory device 100 includes vertically stacked word lines WL1–WL4, such as first–fourth word line conduction layers 36a–36d in the first embodiment or 361a–361d in the second embodiment. EX1007, [0101], [0148]. Each word line WL has a planar structure extending two-dimensionally and is connected to the gate of a corresponding layer

of memory cells $MTr1_{mn}$ – $MTr4_{mn}$ within each memory string MS, with its end portions functioning as the control gates of the respective memory cells. EX1007, [0077], [0080], [0087], [0101], [0148].

194. Fukuzumi further discloses that “word line driving circuit 13 controls voltage applied to a word line WL” and has “a function as control circuits controlling the memory strings MS.” EX1007, [0076], [0090].

195. Therefore, as shown in annotated FIGs. 2 and 28 below (FIGs. AC and AD of my Declarations, respectively, with annotations), Fukuzumi discloses a first word line WL1 (in brown, e.g., first word line conduction layer 361a) in the first device level to control access to first memory cells $MTr1_{mn}$ (enclosed in the brown dashed box in FIG. 2) in the first device level, and a second word line WL2 (in orange, e.g., second word line conduction layer 361b) in the second device level to control access to second memory cells $MTr2_{mn}$ (enclosed in the orange dashed box in FIG. 2) in the second device level.

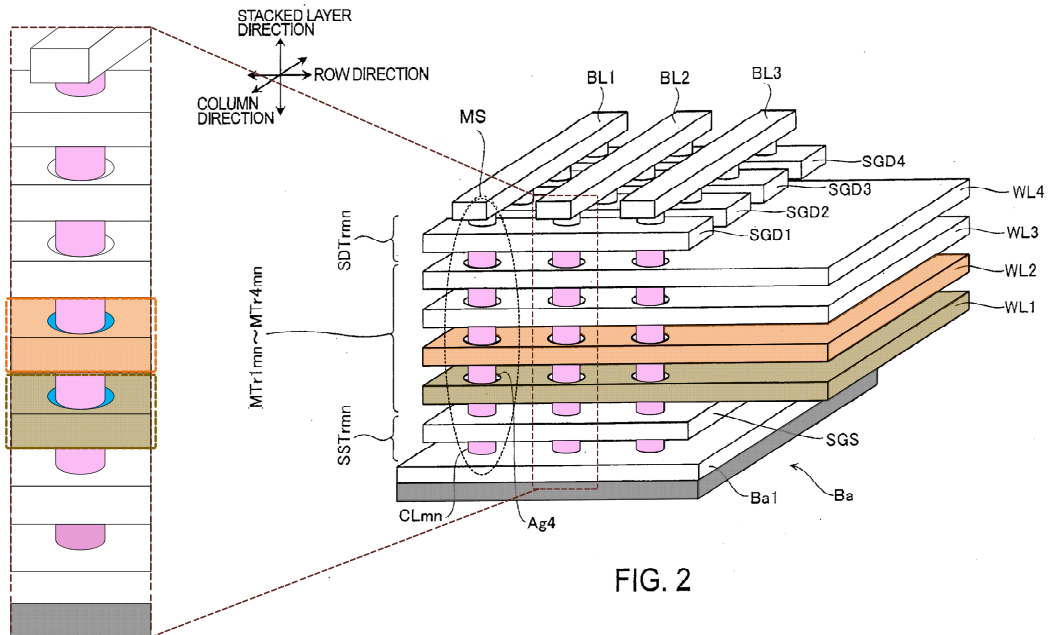


FIG. 2

FIG. AC – FIG. 2 of Fukuzumi (annotated)

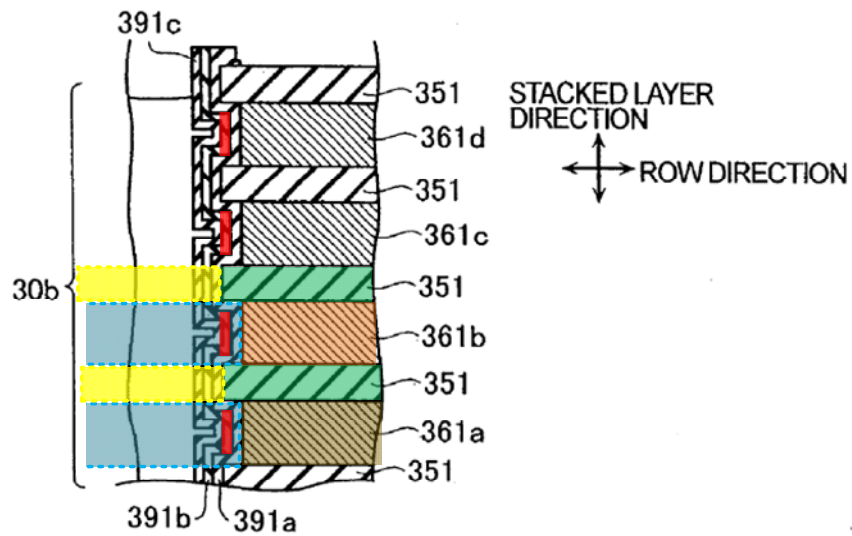


FIG. 28

FIG. AD – FIG. 28 of Fukuzumi (annotated)

196. Furthermore, Fukuzumi describes that each memory cell $MTr1mn$ or $MTr2mn$ contains a charge storage layer 39b/391b, composed of silicon nitride, to facilitate data writing and reading. EX1007, [0114], [0148], [0151]. While Fukuzumi explicitly details the material composition and function of charge storage layer 39b in the first embodiment, a POSITA would have recognized that the same disclosures apply to charge storage layer 391b in the second embodiment. EX1007, [0146]. Consequently, a POSITA would have understood that charge storage layer 391b qualifies as the claimed “memory element.”

197. Additionally, Fukuzumi discloses that charge storage layer 39b/391b is formed within memory hole 37, which extends through word line conduction layers 36a/361a-36d/361d, as depicted in FIG. AD above. A POSITA would have therefore recognized that charge storage layer 391b (in red) resides inside memory hole 37 (in blue). EX1007, [0103]-[0104], [0148], FIG. 4.

198. As I discussed in Section VII.C, if the claim term “cavity” is construed to require that a hole in the control gate has a larger diameter than the holes in the layers above and below, memory hole 37 still satisfies the “cavity” construction. Fukuzumi explicitly states that charge storage layers 391b “are formed as the concavo-convex shape accompanying with the first-fourth word line conduction layer 361a-361d” and that “sidewalls of first-fourth word line conduction layers 361a-361d facing the fourth space Ag4 are formed as recesses corresponding to

a side wall of an interlayer insulator 351.” EX1007, [0148], [0151]. A POSITA would have thus understood, as illustrated in FIG. AD above, memory holes 37 (in blue) within word line conduction layers 361a and 361b possess a greater diameter than memory hole 37 (in yellow) within the interlayer insulators 351 (in green) located above and below each respective word line conduction layer 361a or 361b.

199. Accordingly, in my opinion, Fukuzumi discloses the claimed “cavity” limitation under either party’s construction.

200. Therefore, in my opinion, Fukuzumi discloses the claimed subject matter of elements [1.d] and [1.e].

[1.f] data lines configured to be selectively coupled to a common source and the memory cells through conductive material

201. As illustrated in annotated FIG. 2 below (FIG. AE of my Declaration with annotations), Fukuzumi describes bit lines BL (in green) that are electrically connected to the p-well region Ba1 (in purple) and memory cells MTrmn via columnar semiconductor CLmn (in pink). EX1007, [0081], [0109]. It is clear to me that bit lines BL qualify as the claimed “data lines” at least because the ’214 patent describes that “[d]ata lines 251, 252, and 253 sometimes correspond to bit lines or sense lines of a non-volatile memory device.” EX1001, 3:29-31.

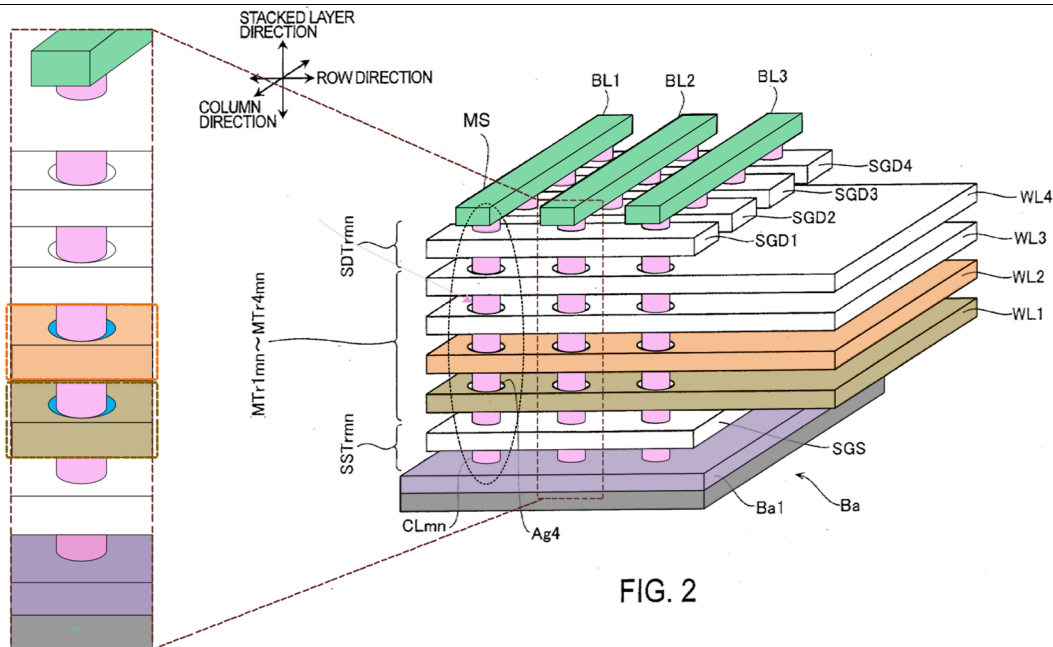


FIG. AE – FIG. 2 of Fukuzumi (annotated)

202. Fukuzumi further states that “[e]ach of the memory strings MS includes columnar semiconductors CL mn on a p-well region Ba1 formed in an n+ region of a semiconductor substrate Ba” and that “source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba.” EX1007, [0081], [0086]. Based on the above disclosure, it is clear to me that p-well region Ba1 qualifies as the claimed “common source” for multiple memory strings MS.

203. Additionally, Fukuzumi discloses that bit lines BL are electrically connected to columnar semiconductor CL mn through a drain-side selection transistor SDTrmn, which is controlled by drain-side selection gate lines SGD. These selection gate lines are driven by the drain-side selection gate line SGD driving circuit 15. EX1007, [0076], [0083], [0085], [0089]. A POSITA would have

understood that bit lines BL interact with memory cells MTrmn and p-well region Ba1 through drain-side selection transistor SDTrmn, and that the drain-side selection gate line SGD driving circuit 15 enables or disables each memory string MS by toggling drain-side selection transistor SDTrmn on or off. This, in turn, controls the connection between bit lines BL and memory cells MTrmn via drain-side selection gate lines SGD. EX1007, [0076]. Accordingly, Fukuzumi demonstrates that bit lines BL are configured to be “selectively” coupled to memory cells MTrmn and p-well region Ba1 through columnar semiconductor CLmn.

204. Furthermore, Fukuzumi states that memory 38, which is part of columnar semiconductor CLmn in both the first and second embodiments, is formed of silicon. EX1007, [0103]. Likewise, the '214 patent also describes that “a **conductive material** 2001 has been formed by, for example, depositing **undoped or lightly doped polysilicon** to place channels 1841 in electrical communication with pillars 705.” EX1001, 8:64-67. Therefore, it is clear to me that Fukuzumi’s columnar semiconductor CLmn, which contains silicon, includes the claimed “conductive material,” consistent with the disclosure of the '214 patent.

205. Therefore, Fukuzumi discloses or at least suggests the claim subject matter of element [1.f].

B. Dependent Claim 2: *The apparatus of claim 1, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.*

206. Fukuzumi also describes that “memory strings MS are displaced like a matrix in a plane perpendicular to the columnar semiconductors CL_{mn} .” EX1007, [0081], FIG. 2. Since these memory strings MS include memory cells $MTr1_{mn}$ – $MTr4_{mn}$, it follows that the memory cells themselves are likewise arranged in a matrix pattern, extending in both row direction and column direction. EX1007, [0081].

207. Furthermore, Fukuzumi explains that columnar semiconductor CL_{mn} extends vertically along a stacked layer direction through word lines $WL1$ – $WL4$, including first and second word lines $WL1$ and $WL2$ positioned at different device levels. As a result, columnar semiconductor CL_{mn} , including the claimed “conductive material,” also extends vertically through the first and second memory cells $MTr1_{mn}$ and $MTr2_{mn}$ at the corresponding device levels. The stacked layer direction shown in FIG. AF of my Declaration below (annotated version of FIG. 2 of Fukuzumi) is perpendicular to the matrix plane defined by the row direction and the column direction, thereby aligning with the claimed “third direction.” EX1007, [0081], FIG. 2.

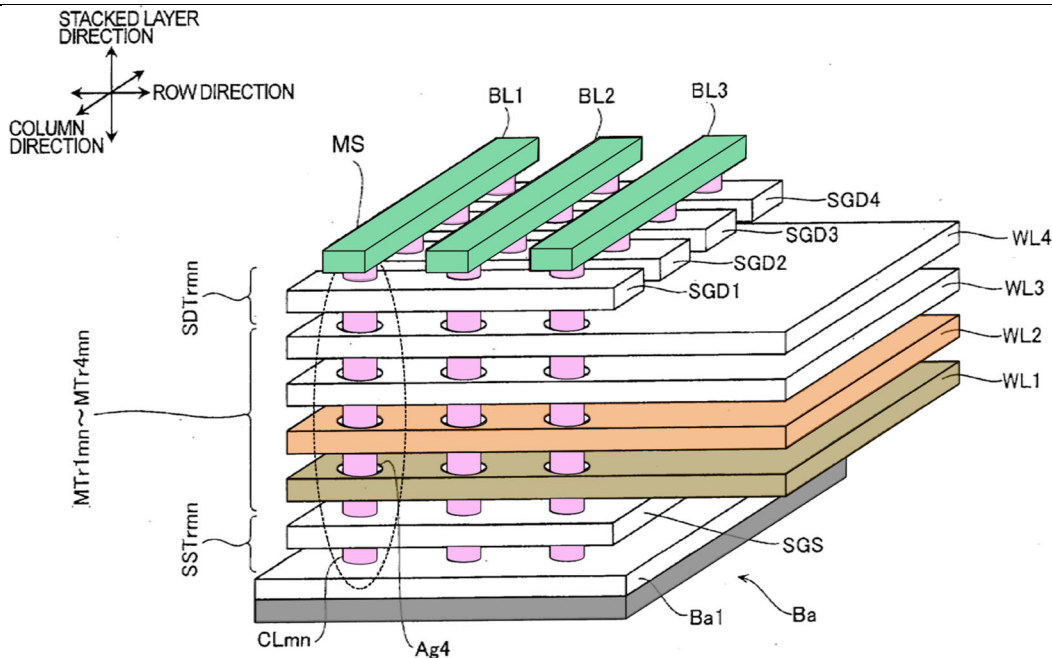


FIG. 2

FIG. AF – FIG. 2 of Fukuzumi (annotated)

208. Accordingly, it is my opinion that Fukuzumi discloses the subject matter of claim 2.

C. **Dependent Claim 3:** *The apparatus of claim 2, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.*

209. Fukuzumi states that “[e]ach of the memory strings MS includes columnar semiconductors CLmn on a p-well region Ba1 formed in an n+ region of a semiconductor substrate Ba” and that “source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba.” EX1007, [0081], [0086].

Based on the above disclosure, it is clear to me that p-well region Ba1 qualifies as the claimed “common source” for multiple memory strings MS.

210. As illustrated in annotated FIG. 2 below (FIG. AG of my Declaration with annotations), Fukuzumi describes p-well region Ba1 (in purple) as being positioned above semiconductor substrate Ba (in gray) and beneath memory cells MTrmn. EX1007, [0081], [0086]. This configuration satisfies the claimed location relationship that “the common source is between the first and second memory cells and the substrate.”

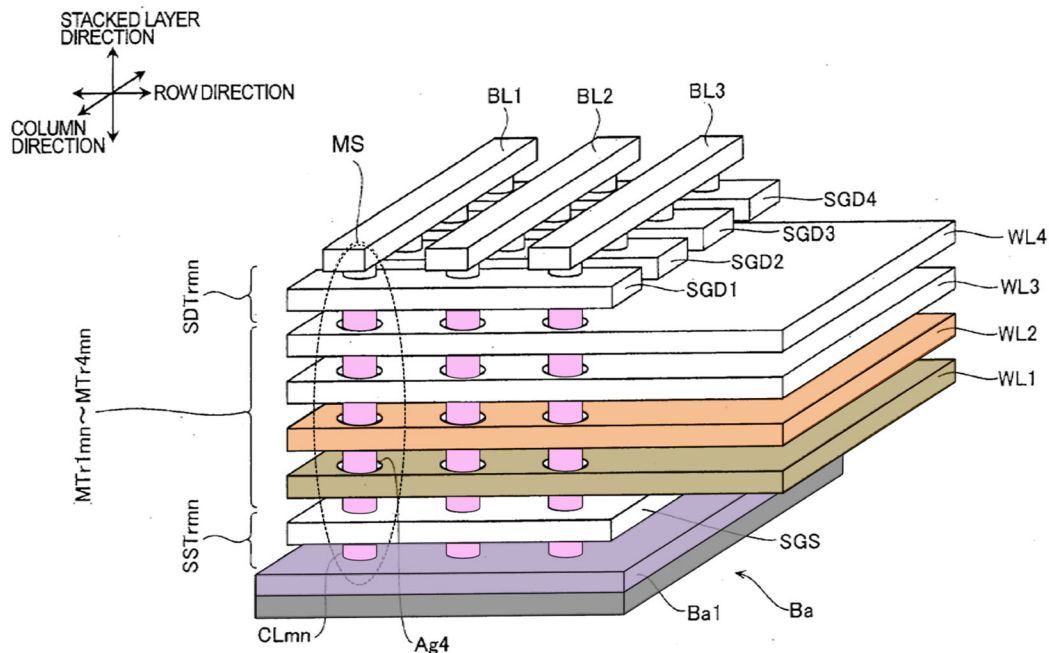


FIG. 2

FIG. AG – FIG. 2 of Fukuzumi (annotated)

211. Additionally, Fukuzumi explains that “reading out data, writing in data, and erasing data are performed by controlling electrical charges of the charge storage

layer in the prescribed memory cell,” and that “columnar semiconductor CL_{mn} is formed on an n⁺-region within a p-type region (p-well region) Ba1 of a semiconductor substrate Ba.” EX1007, [0086], [0090].

212. I have further noted that the '214 patent recognizes the claimed erase operation as a well-known process to a POSITA, omitting its detailed descriptions to focus on other aspects of the invention. EX1001, 3:54-64, 10:44-60. Therefore, a POSITA would understand, based on common knowledge, that during the erase operation of such memory devices, electrons stored in charge storage layers 391b of memory cells MTr1_{mn}–MTr4_{mn} are discharged to p-well region Ba1, where they recombine with holes doped in the p-well. EX1004, [0048].

213. Accordingly, it is my opinion that Fukuzumi further discloses or at least suggests the additional subject matter required by claim 3.

D. Dependent Claims 4 and 5: *The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells. & The apparatus of claim 1, wherein the first memory cells are substantially vertically aligned with the second memory cells.*

214. Fukuzumi describes memory cells MTr1_{mn}–MTr4_{mn} as being vertically and serially connected to form a memory string MS. EX1007, [0079]. As depicted in annotated FIGs. 2 and 28 below (FIGs. AH and AI of my Declarations, respectively, with annotations), each columnar semiconductor CL_{mn} (in pink) extends in the vertical direction (i.e., stacked layer direction), while charge storage

215. Accordingly, a POSITA would understand that the memory cells MTr1mn–MTr4mn within each memory string MS are substantially vertically aligned, and that the charge storage layers 391b associated with these memory cells within each memory string MS are also aligned in the vertical direction.

216. Therefore, it is my opinion that Fukuzumi discloses the claimed subject matter of claims 4 and 5.

E. Dependent Claim 6: *The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.*

217. As discussed in Section XI.A([1.f]), Fukuzumi describes drain-side selection transistors SDTrmn, which selectively couple memory cells MTrmn to bit lines BL during memory operations. EX1007, [0076], [0083], [0085], [0089]. Therefore, drain-side selection transistors SDTrmn, as described in Fukuzumi, qualify as the claimed “transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device.”

218. Fukuzumi further explains that “drain-side selection transistors SDTrmn include ... drain-side selection gate line SGD. ... [a]n end portion of the drain-side selection gate line SGD contacting the insulation layer acts as a control

gate of each of the drain-side selection transistors *SDTrmn*,” and that “one end of the drain-side conductive layer 42 acts as a control gate of the drain-side selection transistor *SDTrmn* mentioned above.” EX1007, [0089], [0107]. A POSITA would understand that drain-side conductive layer 42, which serves as an example of drain-side selection gate line SGD, includes the gate of drain-side selection transistor *SDTrmn*.

219. Additionally, Fukuzumi’s third embodiment, shown in FIG. 29 below (FIG. AJ of my Declaration with annotations), describes a “slit” memory hole 371, where “both ends of the row direction in the memory hole 371 are formed like a line.” EX1007, [0155]. As shown in annotated FIG. 29 below (FIG. AJ of my Declaration with annotations), the word line conduction layers 36*a*–36*d* along the two opposite long sides (in orange) of slit memory hole 371 (in blue) electrically interact with memory 38 (in pink), while the portions (in dark brown) of word line conduction layers 36*a*–36*d* at the long ends of slit memory hole 371 are electrically isolated and do not affect memory 38’s operation. A POSITA would understand that the structure shown in FIG. AJ below forms a claimed “double-gate.” EX1007, [0155].

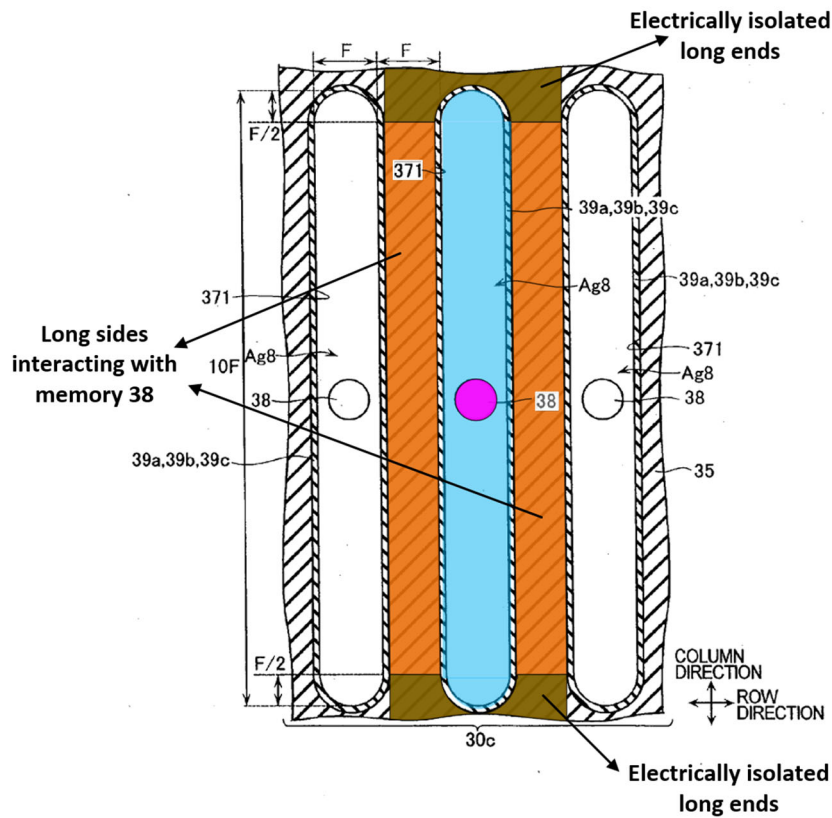


FIG. 29
FIG. AJ – FIG. 29 of Fukuzumi (annotated)

220. A POSITA would have understood, or at least found it obvious, that the same slit structure would also be applicable to drain-side hole 44, as shown in FIG. AK of my Declaration with annotations below. In this case, drain-side conductive layer 42 of drain-side selection transistor SDTrmn serves as an example of drain-side selection gate line SGD and also forms the claimed “double-gate.” EX1007, [0153], [0200].

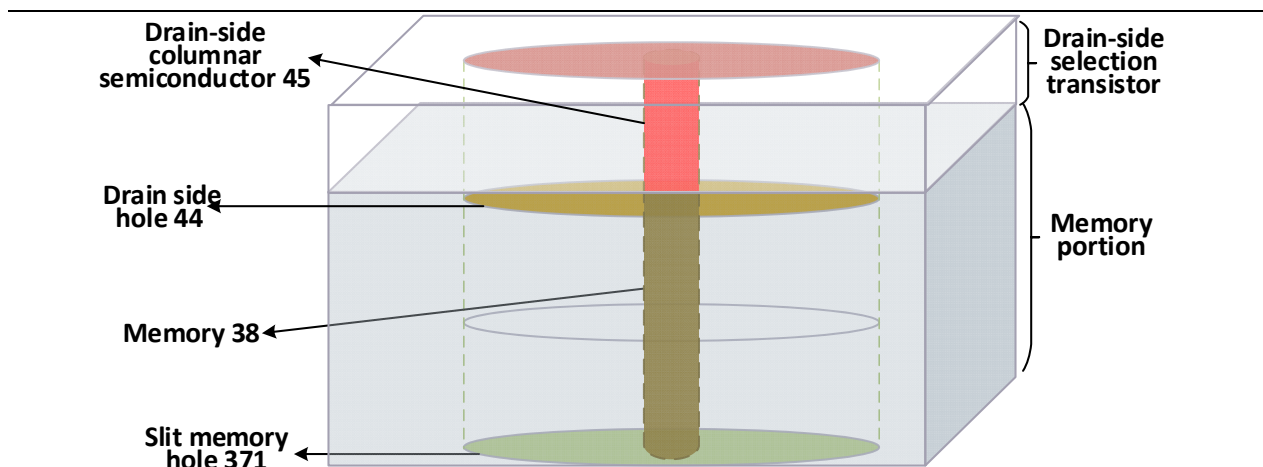


FIG. AK

221. It is clear to me that, using the same slit memory hole structure for drain-side hole 44 would offer the advantage of simplifying manufacturing, as it allows drain-side selection transistors $SDTrmn$ and memory cells $MTrmn$ in a memory string MS to be formed using the same hole. EX1018, [0034], [0036], [0042]-[0043], [0062], [0066]-[0067], [0142]. In this implementation, the portions of drain-side gate insulation layer 46 separate the regions of drain-side conductive layer 42 from the drain-side columnar semiconductor layer 45.

222. A POSITA would have had a reasonable expectation of success in applying the slit hole structure to the drain-side hole 44, as such structures for drain-side selection transistors were already well-known in the art, such as discussed in EX1015, [0103]-[0106], FIGs. 31, 36-37; EX1016, [0075]-[0080], FIG.11; EX1017, [0012]; EX1019, [0070], FIGs. 6-7, 12; etc.

223. I have noticed that, Fukuzumi explains that parts other than the slit

memory hole structure in the third embodiment are “the same or similar” to those in the first and second embodiments. EX1007, [0146], [0153], [0200]. Therefore, it is clear to me that the discussion of other limitations based on the first and second embodiments of Fukuzumi applies equally to Fukuzumi’s third embodiment, modified to incorporate the slit drain-side hole 44’ structure as shown in a non-limiting example in FIG. AO of my Declaration with annotations below.

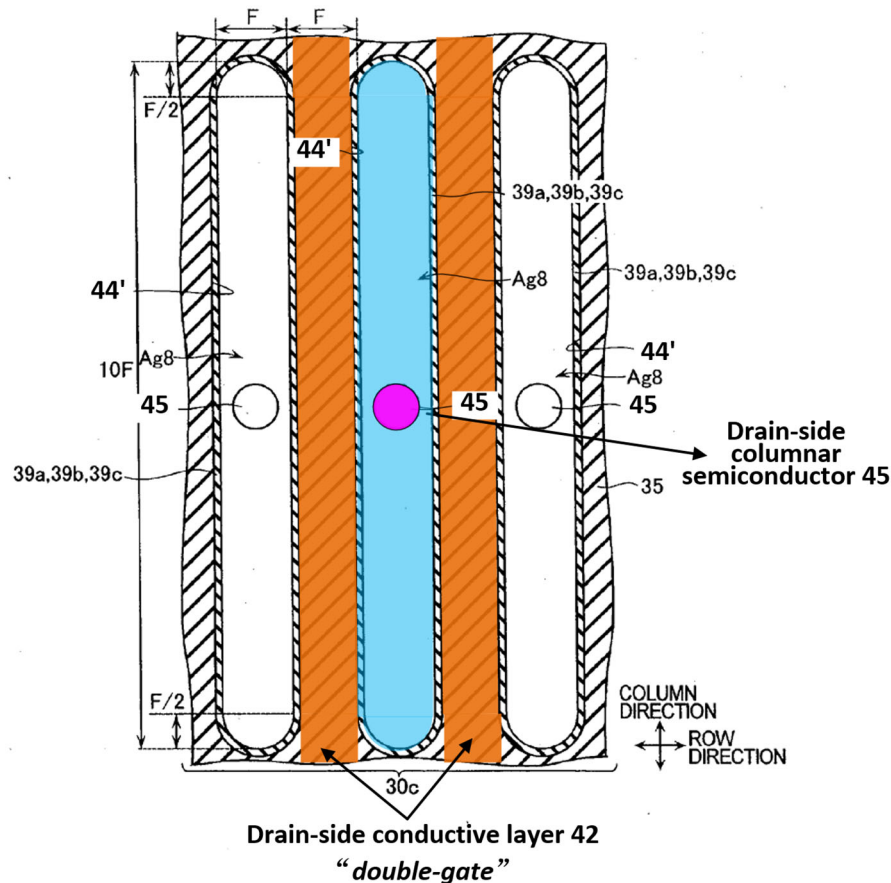


FIG. 29

FIG. AO – FIG. 29 of Fukuzumi (annotated and modified)

224. As illustrated in FIG. AO above, two separate drain-side conductive layers 42 (in orange) on opposite sides of drain-side columnar semiconductor 45

(in pink) form the claimed “double-gate” structure for drain-side selection transistor SDTrmn.

F. Dependent Claim 7: *The apparatus of claim 1, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.*

225. Fukuzumi further discloses that “drain-side selection transistors SDTrmn include the columnar semiconductors CLmn, the insulation layer **surrounding** the columnar semiconductor CLmn, and the drain-side selection gate line SGD **surrounding** the insulation layer. An end portion of the drain-side selection gate line SGD contacting with the insulation layer acts as a control gate of each of the drain-side selection transistors SDTrmn.” EX1007, [0088]-[0089], FIG. 2. This disclosure indicates that the drain-side selection transistor SDTrmn includes the claimed “surrounded gate”—the end portion of drain-side selection gate line SGD.

226. As such, Fukuzumi anticipates or otherwise renders obvious claim 7.

G. Independent Claim 9

[9.P] An apparatus comprising

227. As I discussed in Section XI.A([1.P]), Fukuzumi discloses “[a]n apparatus.”

[9.a] a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device

[9.b] a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level

228. As I discussed in Section XI.A([1.b]-[1.c]), Fukuzumi discloses “a plurality of first/second memory cells located in a first/second device level of the memory device over the substrate, wherein the first device level is different from the second device level,” and “each of the first/second memory cells includes a memory element.”

229. Since Fukuzumi’s first and second memory cells $MTr1mn$ and $MTr2mn$ are part of the **non-volatile** semiconductor memory device 100, a POSITA would have understood that Fukuzumi discloses a “first non-volatile memory cell” $MTr1mn$ and a “second non-volatile memory cell” $MTr2mn$. EX1007, [0080].

230. Fukuzumi further discloses that “[e]ach of the memory cells $Mtrmn$ includes the **columnar** semiconductor $CLmn$, the insulation layer surrounding the columnar semiconductor $CLmn$ via the space $Ag4$ as shown in FIG. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3), and the word line **WL surrounding** the insulation layer and the charge storage layer.” EX1007, [0081], [0087], FIG. 2. Thus, a POSITA would have understood, or at least found it obvious

that, columnar semiconductor CL_{mn} has a cylinder shape, and charge storage layer 391b is conformally formed to surround the cylinder columnar semiconductor CL_{mn} , thus has the claimed “ring shape.”

231. Moreover, as shown in annotated FIG. 7 of Fukuzumi below (FIG. AP of my Declaration with annotation), the charge storage layer 39b has the claimed “ring shape.” Although charge storage layer 39b and charge storage layer 391b are described in different embodiments, it is clear to me that the shape is a common feature between charge storage layer 39b and charge storage layer 391b as they both surround a cylinder column of columnar semiconductor CL_{mn} .

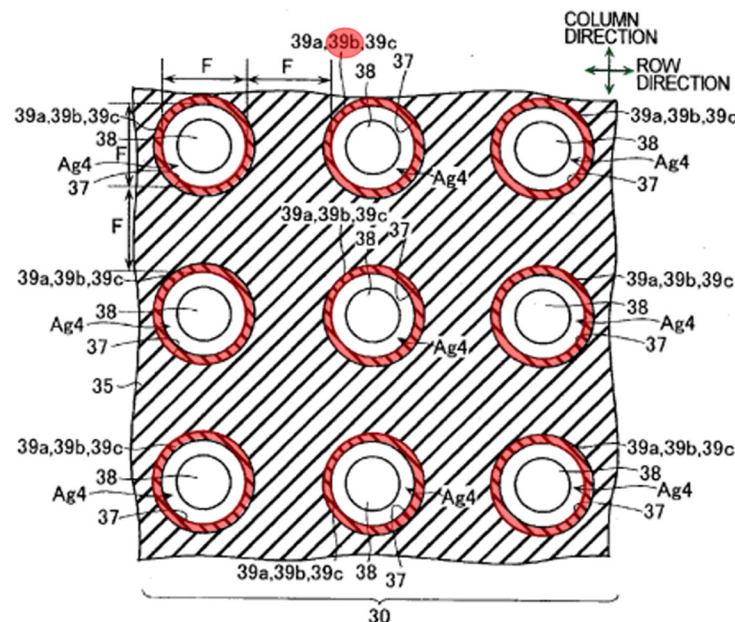


FIG. 7

FIG. AP – FIG. 7 of Fukuzumi (annotated)

232. Accordingly, Fukuzumi discloses or at least suggests the claimed

subject matter of elements [9.a] and [9.b].

[9.c] a conductive material extending through the first and second memory elements

[9.d] a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material

233. As I discussed in Sections XI.A([1.f]) and XI.B above, Fukuzumi discloses or at least suggests “data lines configured to be selectively coupled to a common source and the memory cells through conductive material” and “the conductive material extending through the first and second memory cells in a third direction.” Thus, Fukuzumi also discloses or at least suggests the claimed subject matter of elements [9.c] and [9.d].

H. Dependent Claim 10: *The apparatus of claim 9, further comprising: a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in the first device level of the memory device; and a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in the second device level of the memory device.*

234. As I explained in Section XI.A([1.d]-[1.e]) above, Fukuzumi discloses “a first/second control gate formed in the first/second device level, the first/second control gate to control access to the first/second memory cells.”

235. Fukuzumi further discloses that “[e]ach of the word lines WL1-WL4 is

connected to each gate of the memory cells $MTr1mn$ - $MTr4mn$ in each of the memory strings MS, and each of the word lines WL1-WL4 are formed of the same conductive layer and are common in plane to each other.” EX1007, [0080]. In this context, the first and second word line conduction layers 361a and 361b, which are examples of word lines WL1-WL4, thus qualify as the claimed “first/second additional conductive material configured to operate as a control gate to access the first/second memory cell.”

236. Accordingly, Fukuzumi discloses the subject matter of claim 10.

- I. Dependent Claims 11 and 12: *The apparatus of claim 10, wherein each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material. & The apparatus of claim 11, wherein each of the first and second memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.***

237. Fukuzumi discloses that “[e]ach of the memory cells $Mtrmn$ includes the columnar semiconductor $CLmn$, the insulation layer surrounding the columnar semiconductor $CLmn$ via the space Ag4 as shown in FIG. 2, a charge storage layer (not illustrated in FIGs. 2-3) and the word line WL surrounding the insulation layer and the charge storage layer.” EX1007, [0087]. Specifically, Fukuzumi describes the insulation and charge storage layers surrounding columnar semiconductor $CLmn$ and surrounded by word line WL, noting “surfaces of a block insulation layer 391a, a charge storage layer 391b, and a tunnel insulation layer 391c faced to the fourth

space Ag4.” EX1007, [0087], [0148].

238. Accordingly, a POSITA would have understood that, as shown in annotated FIG. 28 below (FIG. AQ of my Declaration with annotations), Fukuzumi discloses that each memory cell M_{trmn} includes: (i) a tunnel insulation layer 391c (in green) positioned between the respective charge storage layer 391b (in red) and the columnar semiconductor CL_{mn} (in pink), and (ii) a block insulation layer 391a (in yellow) positioned between the respective charge storage layer 391b and the respective word line conduction layer 361b or 361c (in brown or orange).

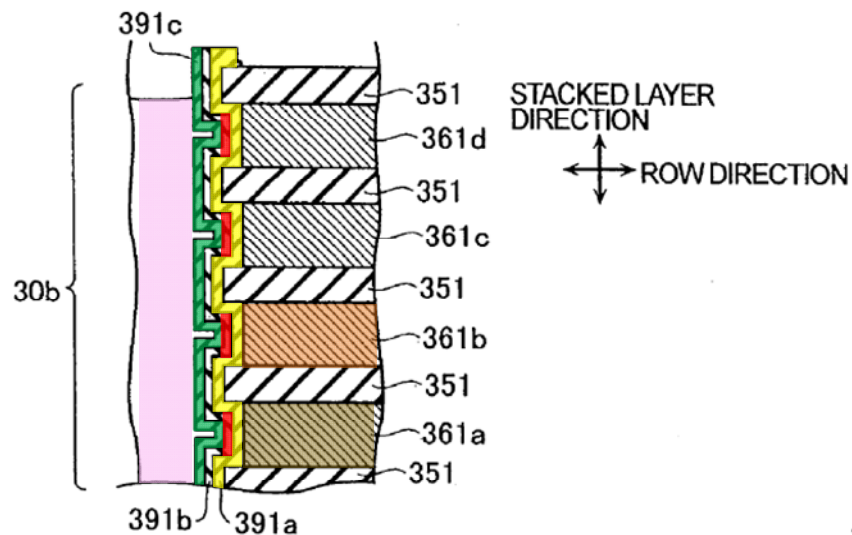


FIG. 28

FIG. AQ – FIG. 28 of Fukuzumi (annotated)

239. Therefore, it is my opinion, Fukuzumi discloses or at least suggests the subject matter of claims 11 and 12.

J. Dependent Claim 14: *The apparatus of claim 9, wherein the first and second memory cells are located between the substrate and the data line.*

240. As shown in annotated FIG. 2 below (FIG. AR of my Declaration with annotations), Fukuzumi discloses that memory cells Mtrmn are positioned vertically between the semiconductor substrate Ba (in gray) and bit lines BL (in green). EX1007, [0081], [0109]. Therefore, Fukuzumi discloses the subject matter of claim 14.

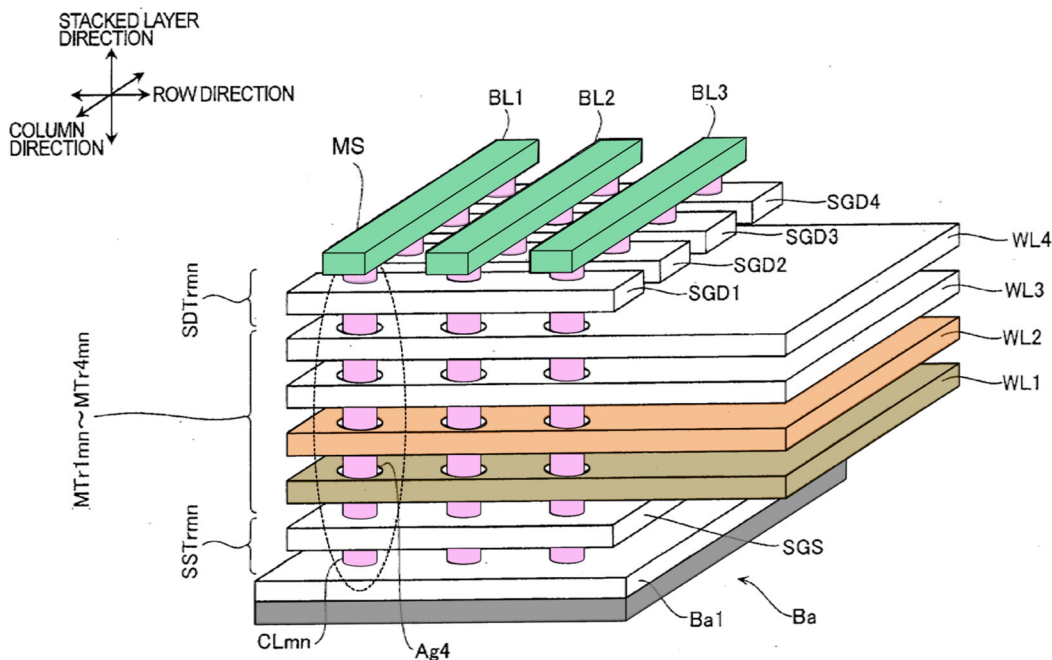


FIG. 2

FIG. AR – FIG. 2 of Fukuzumi (annotated)

K. Independent Claim 15

[15.P] *An apparatus comprising*

241. As I discussed in Section XI.A([1.P]), Fukuzumi discloses “[a]n

apparatus.”

[15.a] a substrate of a memory device

242. As I discussed in Section XI.A([1.a]), Fukuzumi discloses “a substrate of a memory device.”

[15.b] a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall

[15.c] a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level

243. As I discussed in Section XI.A[(1.b)-(1.e)], Fukuzumi discloses “a first/second control gate formed in the first/second device level,” “a cavity of the first/second control gate,” and “the first device level is different from the second device level.”

244. Fukuzumi further discloses that “[e]ach of the word lines WL1-WL4 is connected to each gate of the memory cells MTr1mn-MTr4mn in each of the memory strings MS and each of the word lines WL1-WL4 are formed of the same **conductive layer** and are common in plane each other.” EX1007, [0080]. As examples of word lines WL1-WL4, first and second word line conduction layers 361a and 361b thus qualify as the claimed “first and second conductive materials,”

consistent with the '214 patent. EX1001, 7:3-5, 39-42.

245. As shown in annotated FIGs. 2 and 28 below (FIGs. AS and AT of my Declarations, respectively, with annotations), a POSITA would have understood that each portion of memory hole 37 (in blue), in which charge storage layer 311*b* (in red) is formed, has a respective sidewall on first or second conductive layer 361*a* or 361*b* (in brown or orange) under either party's interpretation of "cavity," as I discussed in Section XI.A([1.d]-[1.e]).

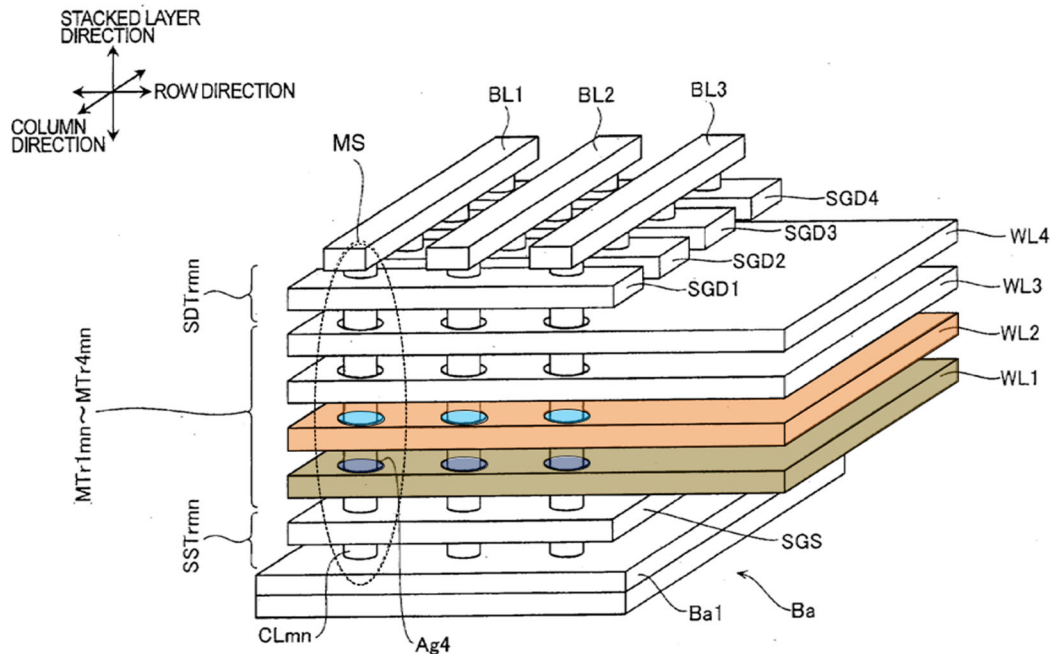


FIG. 2

FIG. AS – FIG. 2 of Fukuzumi (annotated)

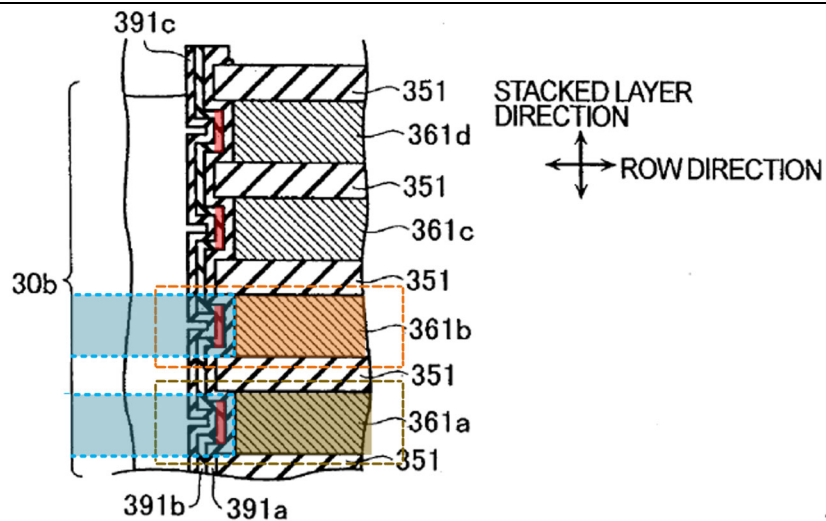


FIG. 28

FIG. AT – FIG. 28 of Fukuzumi (annotated)

246. Therefore, it is my opinion that Fukuzumi discloses the claimed subject matter of elements [15.b] and [15.c].

[15.d] a first dielectric formed on the first sidewall and the second sidewall

[15.e] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric

[15.f] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric

[15.g] a second dielectric formed on a side of the first memory element and on a side of the second memory element

247. As I discussed in Section XI.A([1.d]-[1.e]), Fukuzumi also discloses that “each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.”

248. Fukuzumi further states that “[e]ach of the memory cells M_{trmn} includes the columnar semiconductor CL_{mn} , the insulation layer surrounding the columnar semiconductor CL_{mn} via the space Ag_4 as shown in FIG. 2, a charge storage layer (not illustrated in FIGs. 2-3) and the word line WL surrounding the insulation layer and the charge storage layer.” EX1007, [0087]. Additionally, as examples of the insulation layer and charge storage layer surrounding columnar semiconductor CL_{mn} and surrounded by word line WL, Fukuzumi specifically describes that “surfaces of a block insulation layer 391a, a charge storage layer 391b and a tunnel insulation layer 391c faced to the fourth space Ag_4 .” EX1007, [0148].

249. As illustrated in annotated FIG. 28 below (FIG. AU of my Declaration with annotations), Fukuzumi discloses that block insulation layer 391a (in yellow) is formed on the sidewalls of memory hole 37 (in blue), while tunnel insulation layer 391c (in green) is formed on the sides of charge storage layers 391b (in red). See Section XI.I.

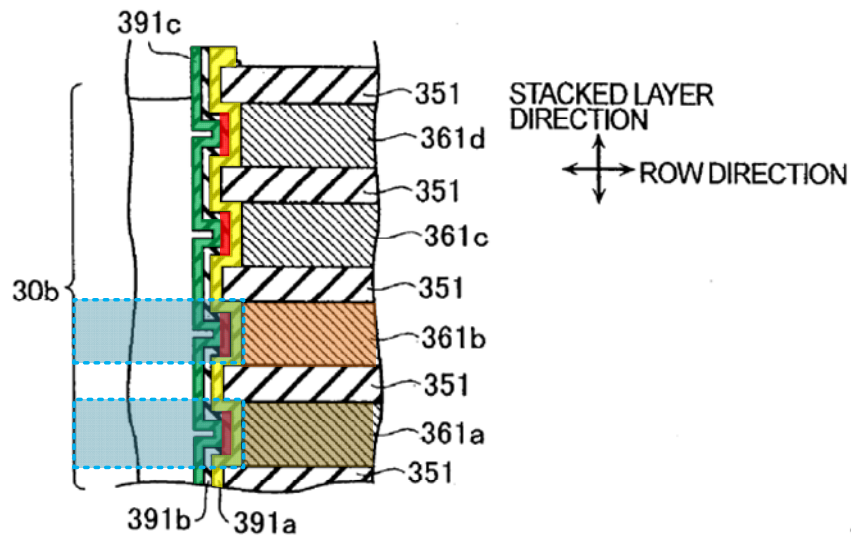


FIG. 28

FIG. AU – FIG. 28 of Fukuzumi (annotated)

250. A POSITA would have understood, or at least found it obvious, that charge storage layer 391b (in red) is electrically isolated from the respective first or second word line conduction layer 361a or 361b (in brown and orange) by a respective portion of block insulation layer 391a (in yellow). See Section XI.I.

251. Accordingly, it is my opinion that Fukuzumi discloses or at least suggests the claimed subject matter of elements [15.d]-[15.g].

[15.h] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric

252. Fukuzumi discloses that each memory string MS includes columnar

semiconductor CL_{mn} , with the source and drain of memory string MS formed within columnar semiconductor CL_{mn} . EX1007, [0081], [0085], [0087]. Regarding memory 38, which is part of columnar semiconductor CL_{mn} in the first and second embodiments, Fukuzumi states that “when the fourth word line conduction layer 36*d* is applied to voltage, the memory 38 is performed to write in data into the approached portion of the charge storage layer 39*b* and read out data from the approached portion of the charge storage layer 39*b*.” EX1007, [0114].

253. Thus, A POSITA would have understood that, during certain operations of Fukuzumi’s memory device, a channel of memory string MS forms in the vertical outermost layer of columnar semiconductor CL_{mn} and does not extend throughout the entire columnar semiconductor CL_{mn} . Accordingly, Fukuzumi discloses the claimed “conductive channel.”

254. This understanding is well established in the art. For example, Sim discloses that “[a]pplication of the read voltage VREAD to the lower select line LSL causes vertical inversion regions 504B to be formed **along the outer walls** of lower portions of the vertical pillars PL formed of semiconducting material,” and “it can be seen that an inversion layer I is created **along the walls, or outer surface**, of the vertical pillars PL when a suitable word line voltage is applied to the word line plates WL_PT.” EX1015, [0063], [0070], FIG. 11; see Section IX.K([15.h]).

255. Further, Fukuzumi discloses that columnar semiconductor CL_{mn}

extends vertically through word lines, including first and second word lines WL in the first and second device levels. EX1007, [0081], FIG. 2. Thus, Fukuzumi discloses that columnar semiconductor CL mn , including its vertical outermost layer, extends from the first device level to the second device level.

256. As illustrated in annotated FIG. 28 below (FIG. AV of my Declaration with annotations), a POSITA would have further understood, or at least found it obvious, that tunneling insulation layer 391c (in green) is formed laterally between charge storage layers 391b (in red) and the vertical outermost layer of columnar semiconductor CL mn (in black), such that the vertical outermost layer of columnar semiconductor CL mn faces charge storage layers 391b but is electrically isolated from charge storage layers 391b by tunneling insulation layer 391c (in green).

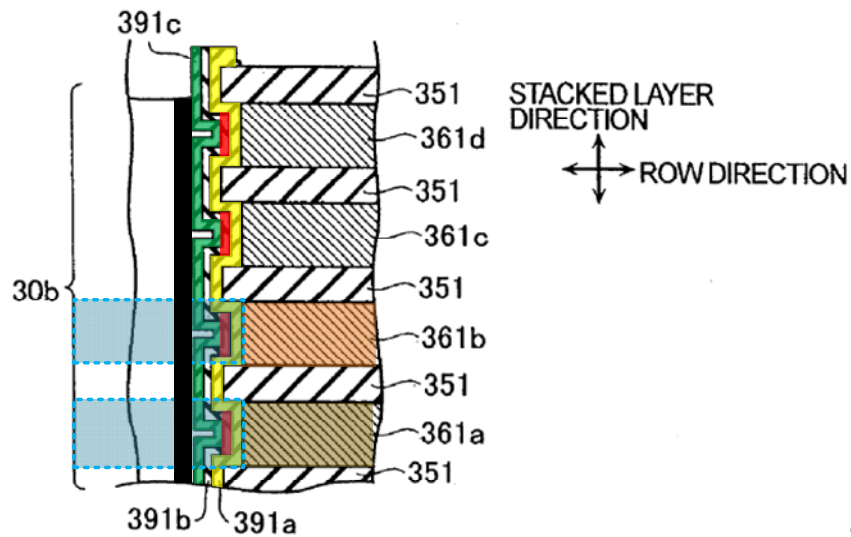


FIG. 28

FIG. AV – FIG. 28 of Fukuzumi (annotated)

257. Accordingly, it is my opinion that Fukuzumi discloses or at least suggests the claimed subject matter of element [15.h].

L. Dependent Claim 16: *The apparatus of claim 15, wherein the first and second memory elements comprise polysilicon.*

258. Fukuzumi discloses that the charge storage layers are made of silicon nitride. EX1007, [0104].

259. A POSITA would have recognized that the selection of charge storage material is a matter of design choice, constrained by the known available options in the field. Specifically, at the time of the '214 patent, the three primary materials used for charge storage in 3D NAND memory devices were polysilicon, silicon nitride,

and silicon oxynitride. EX1020, Table 1; EX1021, 2847, § I; EX1022, 189. A POSITA would have been aware of polysilicon as a viable alternative and understood that such a substitution would be a routine optimization based on the desired electrical characteristics of the memory device.

260. Specifically, a POSITA would have found it obvious to replace silicon nitride or silicon oxynitride with polysilicon to form an “OPO” (oxide-polysilicon-oxide) structure for block insulation layer 391*a*, charge storage layer 391*b*, and tunnel insulation layer 391*c*, as polysilicon was widely recognized as a standard material for memory elements at the time of the invention. This substitution would have been a logical design choice given the well-documented reliability concerns associated with silicon nitride and silicon oxynitride in charge-trapping applications.

261. At the time of the '214 patent, silicon nitride and silicon oxynitride were known to suffer from charge retention degradation over extended use, leading to reliability issues such as charge loss and data instability. EX1009, [0080]; EX1010, 1:46-56, 5:26-50; EX1012, 3.

262. In contrast, at the time of the '214 patent, polysilicon was well established as a reliable material for memory due to its superior charge retention capabilities and its ability to store and isolate charge more effectively over extended periods. A POSITA would have recognized that transitioning to a polysilicon structure in an OPO configuration could mitigate the known issues associated with

silicon nitride, thereby enhancing device longevity and stability. This conclusion is further substantiated by the comparative analysis of EX1012 with EX1013, which demonstrates the improved charge retention characteristics of polysilicon over silicon nitride, and is further supported by EX1014.

263. Given these established industry understandings, a POSITA would have had a reasonable expectation of success in making this substitution, as it represented a well-known and predictable design optimization within the field of 3D NAND memory development.

264. Accordingly, it would have been obvious to a POSITA to modify Fukuzumi's charge storage layer 391b by replacing silicon nitride or silicon oxynitride with polysilicon, yielding a predictable and improved memory element.

265. Therefore, it is my opinion that Fukuzumi renders obvious claim 16.

M. Dependent Claims 17 and 18: *The apparatus of claim 15, wherein the first and second memory elements comprise a dielectric material. & The apparatus of claim 17, wherein the dielectric material comprises silicon nitride.*

266. Fukuzumi explicitly discloses that charge storage layers are formed of silicon nitride. EX1007, [0104]. Accordingly, Fukuzumi discloses the subject matter of claims 17 and 18.

N. Dependent Claim 19: *The apparatus of claim 15, further comprising dielectric material between the first and second conductive materials.*

267. Fukuzumi explicitly discloses that interlayer insulators 351 are formed between adjacent word line conduction layers 361a-361d. EX1007, [0148]. Accordingly, a POSITA would understand that Fukuzumi discloses the subject matter of claim 19.

O. Dependent Claim 20: *The apparatus of claim 15, further comprising: a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.*

268. As I discussed in Section XI.A([1.f]), Fukuzumi discloses that bit line BL is configured to be selectively coupled to columnar semiconductor CL_{mn} via drain-side selection transistor SDTr_{mn}. Therefore, a POSITA would have understood, or at least found it obvious, that bit line BL is also configured to be selectively coupled to the vertical outermost layer of columnar semiconductor CL_{mn}.

269. Furthermore, Fukuzumi discloses in FIG. 2 that charge storage layers 391b are located vertically between bit line BL and semiconductor substrate Ba.

270. Therefore, it is my opinion that Fukuzumi discloses the subject matter of claim 20.

XII. Ground 6: Fukuzumi In View of Kang Renders Obvious Claim 6

271. As I discussed in Section XI.A, Fukuzumi anticipates or otherwise

renders obvious claim 1, on which claim 6 depends. To the extent further disclosure is required to render obvious that “at least one of the transistors comprises a double-gate,” Kang is introduced in this Ground.

272. As explained in Section XI.E, Fukuzumi discloses drain-side selection transistors *SDTrmn* that selectively couple memory cells *Mtrmn* to bit lines BL during memory operations. EX1007, [0076], [0083], [0085].

273. Additionally, as I discussed in Section IX.E, Kang discloses upper selection transistors implementing a “double-gate” structure, where “a lower select gate 230a, an upper select gate 230f ... [are] formed to have a line shape on both sides of active pillar 206.” EX1004, [0052], FIG. 1C.

274. Based on my understanding, Fukuzumi and Kang are analogous prior art in the same field as the '214 patent, which relates to nonvolatile memory devices. EX1001, 1:6-8; 2:63-67; EX1007, [0002]; EX1004, [0002]. Both references address the same problem as the '214 patent—namely, increasing the integration density of memory devices. EX1001, 1:7-22; EX1007, [0004], [0144], [0150]; EX1004, [0003]-[0004].

275. A POSITA would have been motivated to modify Fukuzumi's drain-side selection transistor, replacing its surrounded-gate structure with the double-gate structure of Kang. By replacing the surrounded-gate-type drain-side selection transistor with a double-gate-type structure, this adjustment would reduce gate and

parasitic capacitance, which in turn improves switching speed and power efficiency. The reduced parasitic capacitance minimizes delays and enhances the overall performance of the memory cell by lowering power consumption during read and write operations. Additionally, this change would mitigate unwanted parasitic effects, particularly those arising from electric field overlapping between the drain and gate regions. Such overlap can lead to unintended leakage currents and degraded electrical performance, negatively impacting the reliability and stability of the memory device. A POSITA would recognize that this modification aligns with well-known industry practices aimed at optimizing transistor performance by balancing control gate effectiveness with minimized parasitic influences.

276. Moreover, the feasibility of implementing a double-gate structure in select transistors is well-established, making the modification technically achievable. A POSITA would have had a reasonable expectation of success in implementing this modification, given that the use of a double-gate structure for selection transistors was well-documented and widely recognized in the art prior to the '214 patent. Numerous publications describe the benefits and feasibility of double-gate transistors in similar applications. See, e.g., EX1015, [0103]-[0106], FIGs. 31, 36, 37; EX1016, [0075]-[0080], FIG. 11; EX1017, [0012]; and EX1019, [0070], FIGs. 6-7, 12.

277. Moreover, implementing this modification would not have required

fundamental changes to the overall fabrication process. Given the structural similarities between the double-gate and surrounded-gate configurations, a POSITA would recognize that the substitution could be seamlessly integrated into existing process flows with minimal design adjustments that are well within their capabilities. The well-documented nature of double-gate transistors in prior art further reinforces that this modification would have been straightforward and achievable without undue experimentation, making it an evident and advantageous improvement for optimizing the performance of the memory device.

278. Notably, Fukuzumi's third embodiment strongly suggests that modifying the gate from a surrounded-gate structure to a double-gate structure would be compatible with its drain-side selection transistors.

279. Accordingly, it is my opinion that claim 6 would have been obvious in view of the combination of Fukuzumi and Kang.

XIII. Ground 7: Fukuzumi In View of Ahn Renders Obvious Claim 16

280. As I discussed in Section XI.K, Fukuzumi anticipates or otherwise renders obvious claim 15, on which claim 16 depends. Should the Board determine that Fukuzumi alone does not disclose or render obvious that "the first and second memory elements comprise polysilicon," as required by claim 16, Ahn is introduced in this Ground.

281. As I explained in Section XI.M, Fukuzumi discloses that charge storage

layers 391b are formed of silicon nitride. EX1007, [0104].

282. Additionally, as I discussed in Sections VIII.B, Ahn explicitly teaches forming a charge trap layer using either silicon nitride or polysilicon, providing exemplary processing methods and parameters for both materials. EX1006, [0067].

283. Based on my understanding, Fukuzumi and Ahn are analogous prior art in the same field as the '214 patent, which relates to nonvolatile memory devices. EX1001, 1:6-8; 2:63-67; EX1007, [0002]; EX1006, [0001]. Both references address the same problem as the '214 patent—namely, increasing the integration density of memory devices. EX1001, 1:7-22; EX1007, [0004], [0144], [0150]; EX1006, [0005].

284. In my opinion, it would have been obvious to apply Ahn's teachings of a polysilicon charge trap layer to Fukuzumi's charge storage layers 391b because polysilicon was commonly used for memory elements at the time of the '214 patent. Moreover, the selection among polysilicon, silicon nitride, and silicon oxynitride for forming the charge trap layer was a known design choice. See Section XI.L. A POSITA would have been motivated to replace Fukuzumi silicon nitride charge storage layer 391b with Ahn's polysilicon layer because polysilicon offered better reliability and data retention compared to silicon nitride in flash memory devices at the time of the '214 patent. EX1009, [0080]; EX1010, 1:46-56, 5:26-50; EX1012, 3; see Section XI.L. Given these advantages, a POSITA would have recognized that substituting polysilicon for silicon nitride in Fukuzumi's charge storage layer 391b

would improve device performance.

285. Furthermore, a POSITA would have had a reasonable expectation of success in replacing the silicon nitride charge storage layer 391*b* in Fukuzumi with Ahn's polysilicon layer, given the well-documented interchangeability of these materials for charge storage applications. Ahn explicitly states that its charge trap layer within the ONO (oxide-nitride-oxide) structure "is formed by depositing, for example, a silicon nitride film or a polysilicon film," confirming that both materials were viable alternatives for the same function. EX1006, [0067]. This statement directly suggests that the substitution of silicon nitride with polysilicon was not only known in the field but also an expected design variation depending on performance requirements. Additionally, Ahn provides detailed guidance on the specific deposition parameters for forming a polysilicon charge trap layer, including a range of thickness values (e.g., "a thickness of 10 to 1,000 Å") and applicable deposition techniques such as atomic layer deposition (ALD) and chemical vapor deposition (CVD). EX1006, [0067]. These parameters would have provided a POSITA with sufficient information to implement the material substitution without requiring undue experimentation.

286. A POSITA would have recognized that polysilicon offers advantages over silicon nitride in certain memory applications, particularly in terms of improved charge retention and reduced charge trapping degradation over extended use. Given

that both Fukuzumi and Ahn address charge storage layers in similar memory structures, incorporating Ahn's polysilicon layer into Fukuzumi's device would have been a straightforward modification that leveraged known material properties and fabrication techniques. As a result, a POSITA would have had strong motivation and a reasonable expectation of success in making this substitution to improve the overall reliability and performance of the memory device.

287. Accordingly, it is my opinion that Fukuzumi in view of Ahn renders the subject matter of claim 16 obvious.

XIV. Secondary Considerations

288. I have seen no evidence in the '214 patent's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any of the challenged claims. See generally EX1002. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the '214 patent were already well known. To the extent Patent Owner asserts the existence of any secondary considerations in its responses, I reserve my right to address any such evidence.

XV. Additional Remarks

289. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

290. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

291. I have reviewed the accompanying Petition for *Inter Partes* Review of the '214 patent and, given the information set forth in this declaration, I agree with the reasoning and conclusions of the grounds of challenge in the petition. Based on my own analysis, I agree that: (1) Kang anticipates or otherwise renders obvious claims 1-7, 9-12, and 14-20; (2) Kang in view of Ahn also renders obvious claim 16; (3) Fukuzumi also anticipates or otherwise renders obvious claims 1-7, 9-12, and 14-20; (4) Fukuzumi in view of Kang also renders obvious claim 6; and (5) Fukuzumi in view of Ahn also renders obvious claim 16.

* * *

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this proceeding.

Dated: 2/11/25

By: Kelin J. Kuhn
Dr. Kelin Kuhn
Winthrop, Washington

APPENDIX A

CURRICULUM VITAE
Dr. Kelin J. Kuhn

CONTACT INFORMATION:

Kelin J. Kuhn
P.O. Box 609
Winthrop, WA 98862
kjkuhn@confluence-tech.com

EDUCATION:

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980
(magna cum laude)

PRESENT ROLE:

**Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com);
present role**

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

**Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu)
2014 to date**

Position: Adjunct Professor
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:

Bayes PLLC: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *Inter Partes Review of U.S. Patent Nos. 8,803,214 And 10,475,737*.

Pillsbury Winthrop Shaw Pittman LLP: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

Ropes and Gray: Initiated 2023 and on-going. Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792.*

Heim, Payne & Chorush: Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc.* with regards to a dispute with *Taiwan Semiconductor Manufacturing Company.*

Smith Baluch LLP: Initiated 2022 and on-going. Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

Carter Arnett: Initiated 2022 and ongoing. Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S. 2 LLC.*

Mintz: Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

Heim, Payne & Chorush: Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

Quinn Emanuel Urquhart & Sullivan: Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

Ropes and Gray: Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Lawrence and Phillips: Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes* reviews (IPRs) filed by Samsung.

Wolf Greenfield: Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.* with regards to *inter partes* reviews (IPRs) filed by Micron.

Hueston Henningan: Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

Skadden Arps: Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

PARADIM: Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn

is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

Quinn Emanuel Urquhart & Sullivan: Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Susman Godfrey: Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

Womble Bond Dickinson: Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* (“EPR”) proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

Womble Bond Dickinson: Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al.* Dr. Kuhn supported this litigation for the plaintiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

Lathrop Gage: Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

Ropes & Gray: Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

GlaserWeil: Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314*. Dr. Kuhn supported this litigation for the plaintiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

yoR Labs Inc.: Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

Oregon State University, Department of Electrical Engineering and Computer Science: Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn’s role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

FORMER ROLES (2014 and PRIOR)

Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)

Grade level: 12 (Fellow)

Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59, No: 7, 2012, pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008

Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)

Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

Intel, Portland, OR, (90nm communication process manager) 2001-2004+

Grade level: 9/10 (Sr. Engineer / Principal engineer)

Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

Other Intel experience:

Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001

Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998

Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

Other relevant experience:

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Professor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

Highlights include:

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

BOOKS

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

BOOK CHAPTERS

“The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

AWARDS:

Elected to the National Academy of Engineering (2023)
IEEE Frederik Philips Award (2016)
IEEE Paul Rappaport Award (2013)
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)

Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)

Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996

University of Washington, Distinguished Teaching Award, 1995

College of Engineering, Outstanding Faculty Achievement Award, 1994

NSF Presidential Young Investigator award, 1991-6

NSF Research Initiation Award, 1989-91

IBM Graduate Fellowship, 1983-5

Hertz Graduate Fellowship, 1982-3

National Merit Scholar, 1976-80

JOURNAL PUBLICATIONS:

49. "First principles modeling of defects in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, J. Appl. Phys., Vol. 121, No. 7, Jan. 2017.

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46. "Adhesion Limits and Design Criteria for Nanorelays", Kevin L. Lin, Graham L. W. Cross, Peter Gleeson, Johann P. de Silva, Alejandro Levander, Jorge A. Muñoz, Chytra Pawashe, Alexis Potie, Patrick Theofanis, John J. Boland, and Dr. Kuhn J. Kuhn, IEEE Trans. on Elec. Dev., Vol. 63, No. 1, Jan. 2016, 465-470.

45. Distributive Quasi-Ballistic Drift Diffusion Model Including Effects of Stress and High Driving Field, Roza Kotlyar,, Rafael Rios, Cory E. Weber, Thomas D. Linton, Mark Armstrong and Dr. Kuhn Kuhn, IEEE Trans. on Elec. Dev., Vol. 62, No. 3, March 2015. Pp. 743-750.

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43. Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions, Monaghan, S. O'Connor, E., Rios, R., Ferdousi, F., Floyd, L., Ryan, E., Cherhaoui, K., Povey, I.M., Kuhn, K.J., Hurley, P.K. IEEE Transactions on Electron Devices, Vol. 61, No. 12, pp. 4176-85, Dec. 2014.

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41. Scaling Limits of Electrostatic Nanorelays, Pawashe, C., Lin, K., Kuhn, K.J., IEEE Transactions on Electron Devices, Vol. 60, No. 9, pp. 2936-42, Sept. 2013,
40. Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors, Kotlyar, R.; Avci, U.E.; Cea, S.; Rios, R.; Linton, T.D.; Kuhn, K.J.; Young, I.A., Applied Physics Letters, v 102, n 11, March 18, 2013.
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37. Does the low hole transport mass in <110> and <111> Si nanowires lead to mobility enhancements at high field and stress: a self-consistent tight-binding study, R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, Michael Povolotskyi, Tillmann Kubis, and Gerhard Klimeck, Vol: 111 , No: 12, 2012, pp 123718 - 123718-11
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27. Elevated temperature performance of pseudomorphic AlGaAs/InGaAs MODFETs. Zurek, S.J.; Darling, R.B.; Kuhn, K.J.; Foisy, M.C. IEEE Transactions on Electron Devices, vol.45, no.1, Jan. 1998. p. 2-8
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49. Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation, K. Kuhn, INFOS 2011 (June 22, 2011, France)
48. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET, Avci, U.E.; Rios, R.; Kuhn, K.J.; Young, I.A., IEEE Conference on Nanotechnology (IEEE-NANO), 2011 11th, pp. 869 – 872
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46. CMOS scaling for the 22nm node and beyond: Device physics and technology, Kuhn, K.J., 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2011 , pp. 1 – 2
45. Past, Present and Future: SiGe and CMOS Transistor Scaling. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, ECS 2010, Oct. 10, Las Vegas, CA, USA.
44. Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, K. J. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.
43. CMOS transistor scaling past 32nm and implications on variation, K. Kuhn, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA, pp. 241-246.
42. Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, K. Kuhn, Nikkei Electronics Symposium, June 29th, 2010.
41. Technology options for 22nm and beyond, K. Kuhn, Technology, Kuhn, K.J.; Liu, M.Y.; Kennel, H.; 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.
40. CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California
39. Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.
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PATENTS

	PAT. NO.	Title
1	11,302,777	Integration methods to fabricate internal spacers for nanowire devices
2	11,195,919	Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer
3	11,139,400	Non-planar semiconductor device having hybrid geometry-based active region
4	11,024,714	Nanowire transistor fabrication with hardmask layers
5	10,991,799	Silicon and silicon germanium nanowire structures
6	10,825,752	Integrated thermoelectric cooling
7	10,804,357	Integration methods to fabricate internal spacers for nanowire devices
8	10,636,871	Silicon and silicon germanium nanowire structures
9	10,593,804	Non-planar semiconductor device having hybrid geometry-based active region
10	10,586,868	Non-planar semiconductor device having hybrid geometry-based active region
11	10,580,899	Nanowire structures having non-discrete source and drain regions
12	10,580,860	Integration methods to fabricate internal spacers for nanowire devices
13	10,535,770	Scaled TFET transistor formed using nanowire with surface termination
14	10,424,580	Semiconductor devices having modulated nanowire counts
15	10,283,589	Integration methods to fabricate internal spacers for nanowire devices
16	10,121,861	Nanowire transistor fabrication with hardmask layers
17	10,121,856	Integration methods to fabricate internal spacers for nanowire devices
18	10,115,822	Methods of forming low band gap source and drain structures in microelectronic devices
19	10,109,711	CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel
20	10,074,573	CMOS nanowire structure
21	10,074,357	Integrated acoustic phase array
22	10,026,829	Semiconductor device with isolated body portion
23	9,978,636	Isolated and bulk semiconductor devices formed on a same bulk substrate
24	9,947,805	Nanowire-based mechanical switching device
25	9,935,205	Internal spacers for nanowire transistors and method of fabrication thereof
26	9,935,107	CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same
27	9,926,193	Magnetic nanomechanical devices for stiction compensation

28	9,911,835	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
29	9,893,167	Integration methods to fabricate internal spacers for nanowire devices
30	9,882,053	Molded dielectric fin-based nanostructure
31	9,859,368	Integration methods to fabricate internal spacers for nanowire devices
32	9,825,130	Leakage reduction structures for nanowire transistors
33	9,812,524	Nanowire transistor devices and forming techniques
34	9,691,843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
35	9,680,013	Non-planar device having uniaxially strained semiconductor body and method of making same
36	9,673,302	Conversion of strain-inducing buffer to electrical insulator
37	9,614,060	Nanowire transistor with underlayer etch stops
38	9,608,059	Semiconductor device with isolated body portion
39	9,595,581	Silicon and silicon germanium nanowire structures
40	9,583,602	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
41	9,583,491	CMOS nanowire structure
42	9,564,522	Nanowire structures having non-discrete source and drain regions
43	9,559,160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
44	9,508,796	Internal spacers for nanowire transistors and method of fabrication thereof
45	9,484,447	Integration methods to fabricate internal spacers for nanowire devices
46	9,472,613	Conversion of strain-inducing buffer to electrical insulator
47	9,425,212	Isolated and bulk semiconductor devices formed on a same bulk substrate
48	9,412,872	N-type and P-type tunneling field effect transistors (TFETs)
49	9,385,221	Nanowire transistor with underlayer etch stops
50	9,362,074	Nanowire-based mechanical switching device
51	9,355,242	Method and apparatus for managing and accessing personal data
52	9,343,559	Nanowire transistor devices and forming techniques
53	9,287,576	Self-powered internal medical device
54	9,258,114	Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)
55	9,224,810	CMOS nanowire structure
56	9,183,829	Integrated acoustic phase array

57	9,129,829	Silicon and silicon germanium nanowire structures
58	9,129,827	Conversion of strain-inducing buffer to electrical insulator
59	9,105,344	Shut-off mechanism in an integrated circuit device
60	9,087,863	Nanowire structures having non-discrete source and drain regions
61	9,064,944	Nanowire transistor with underlayer etch stops
62	9,029,221	Semiconductor devices having three-dimensional bodies with modulated heights
63	9,012,284	Nanowire transistor devices and forming techniques
64	8,890,120	Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs
65	8,853,741	Junctionless accumulation-mode devices on decoupled prominent architectures
66	8,766,372	Copper-filled trench contact for transistor performance improvement
67	8,753,942	Silicon and silicon germanium nanowire structures
68	8,558,279	Non-planar device having uniaxially strained semiconductor body and method of making same
69	8,507,948	Junctionless accumulation-mode devices on prominent architectures, and methods of making same
70	8,487,348	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
71	8,269,283	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
72	8,258,057	Copper-filled trench contact for transistor performance improvement
73	7,999,607	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
74	7,888,710	CMOS fabrication process utilizing special transistor orientation
75	7,737,770	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
76	7,312,485	CMOS fabrication process utilizing special transistor orientation
77	6,627,506	Thin tensile layers in shallow trench isolation and method of making same
78	6,368,931	Thin tensile layers in shallow trench isolation and method of making same
79	4,617,669	Method and apparatus for pumping laser slabs
80	4,563,763	Method and apparatus for cooling a slab laser

INVITED TECHNICAL PRESENTATIONS/SEMINARS :

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures ...and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17th, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California

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Invited – International Electron Device meeting – short course.
http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf

Invited seminar - “45nm High-k + Metal Gate Logic Technology,” K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.