UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner

v.

MICRON TECHNOLOGY, INC.

Patent Owner

IPR2025-00499

U.S. PATENT 8,803,214

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 8,803,214

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3. Lung discloses or suggests "*a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate*" [8.c], "*a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate,*" [8.d.1], and *"wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction*" [8.d.2].....14

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5. Lung discloses "*data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions*" [8.f.1] and "*wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate*" [8.f.2]. 20

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2. Park discloses "*a conductive material extending through the first and second memory elements*" [9.c], and "*a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material*" [9.d]. 51

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3. A POSITA would have a reasonable expectation of success in forming metal/silicide common source at the top of Fukuzumi's 3D memory device. 63

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EX1009	S. Zhang *et al*., "Metal Silicides in CMOS Technology: Past, Present, and Future Trends," Critical Reviews in Solid State and Materials Sciences, vol. 28, no. 1, pp. 1-129, March 2003
EX1010	J. Jang *et al.*, "Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory," 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193
EX1011	Defendant's Unopposed Motion To Modify The Case Schedule To Permit Defendant To Reassert Counterclaims, *Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*., No. 3:23-cv-05792-RFL, D.I. 213 (N.D. Cal. January 29, 2025)
EX1012	R. Katsumata *et al*., "Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Operation for Ultra High Density Storage Devices," 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 136-137
EX1013	T. Maeda *et al*., "Multi-Stacked 1G Cell/Layer Pipe-Shaped BiCS Flash Memory," 2009 Symposium on VLSI Circuits, Kyoto, Japan, 2009, pp. 22-23

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Exhibit	Description
EX1014	J. Trattles *et al*., "Three-dimensional Finite-Element Investigation of Current Crowding and Peak Temperatures in VLSI Multilevel Interconnections," IEEE Transactions on Electron Devices, vol. 40, no. 7, pp. 1344-1347, July 1993
EX1015	D. Hisamoto *et al*., "Sub-10-ps Gate Delay by Reducing the Current Crowding Effect at An Extension," International Electron Devices Meeting. IEDM Technical Digest, Washington, DC, USA, 1997, pp. 239-242
EX1016	H. Wong *et al*., "On the Reliability Issues of RF CMOS Devices," 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings, Shanghai, China, 2006, pp. 1105-1108
EX1017	U.S. Patent Application Publication No. 2009/0310425 in the Name of Sim *et al*.
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All citations to 35 U.S.C. §§ 102 and 103 in this paper refer to the Pre-AIA statutes.

All emphases in quotations are added unless otherwise noted.

Direct quotations of claim language are italicized.

This paper includes color illustrations and should be viewed in color.

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I. INTRODUCTION

Yangtze Memory Technologies Company, Ltd. ("Petitioner") petitions for *inter partes* review ("IPR") of claims 8, 13, and 21 ("challenged claims") of U.S. Patent No. 8,803,214 ("'214 patent," EX1001) assigned to Micron Technology, Inc. ("PO").

The challenged claims recite features related to three-dimensional (3D) NAND memory devices, all of which were well-known and conventional before the'214 patent. Notably, the purported novelty—a technique for forming a common source above data lines and the resulting relative vertical positions of related components—as well as every other limitation of the challenged claims, are explicitly disclosed by U.S. Patent Application Publication No. 2011/0286283 in the name of Lung *et al.* ("Lung," EX1004).

Moreover, U.S. Patent Application Publication No. 2008/0242028 in the name of Mokhlesi *et al*. ("Mokhlesi," EX1006) expressly teaches a person of ordinary skill in the art (POSITA) to rearrange the bottom semiconductor common source and the top bit lines. Mokhlesi explains that this modification allows the use of metal and/or silicide, rather than doped semiconductor material, for the common source. This reduces detrimental current crowding in the source due to better conductivity of metal and/or silicide compared to doped semiconductor materials. This express teaching would have motivated a POSITA to modify numerous prior art references,

such as U.S. Patent Application Publication No. 2010/0120214 in the name of Park *et al*. ("Park," EX1005) and U.S. Patent Application Publication No. 2009/0146190 in the name of Fukuzumi *et al*. ("Fukuzumi," EX1007), to achieve the claimed invention.

Petitioner's expert, Dr. Kelin Kuhn—a semiconductor industry veteran with four decades of experience—has thoroughly analyzed the prior art and confirms that the challenged claims are unpatentable over these references and other prior art predating the '214 patent.

Petitioner thus respectfully requests the Board cancel the challenged claims.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest

The real parties-in-interest are Yangtze Memory Technologies Company, Ltd. and Yangtze Memory Technologies, Inc.

B. Related Matters

The '214 patent is not currently asserted in any pending civil action. In *Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. et al.*, No. 3:23-cv-05792-RFL (N.D. Cal.) ("NDCA case"), however, PO has filed an unopposed motion for leave to amend its counterclaims to assert the '214 patent in the NDCA

case.[1] That motion remains pending.

Petitioner filed an IPR (Case IPR2025-00099, "'099 IPR") on November 18, 2024, against U.S. Patent No. 10,872,903 ("'903 patent"), which is one of the child patents of the '214 patent and asserted in the NDCA case. The '099 IPR is currently pending institution decision.

Petitioner is concurrently filing another IPR (Case IPR2025-00498, "'498 IPR") on the same day, challenging a different set of claims of the '214 patent: claims 1-7, 9-12, and 14-20.

C. Lead and Back-up Counsel and Service Information

Petitioner identifies the following lead and back-up counsels:

[1] The '214 patent was initially included in PO's February 16, 2024 Answer and Counterclaim, but the Court dismissed it under FRCP 12(b)(6), with leave to amend. EX1018, EX1019. Rather than amending the pleadings, PO chose to drop the '214 patent on August 1, 2024. EX1020. Months later, PO now seeks to reassert the '214 patent. EX1011.

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Petitioner consents to electronic service at YMTC-Micron-IPR@bayes.law, as well as the above email addresses.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that the '214 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified in this Petition.

IV. RELIEF REQUESTED

Under 35 U.S.C. § 311, Petitioner requests IPR of claims 8, 13, and 21 of the '214 patent.

A. Claims for Which Review Is Requested

Petitioner requests IPR and cancellation of challenged claims 8, 13, and 21 of the '214 patent under 35 U.S.C. § 311 based on the following grounds. This Petition

is supported by the Declaration of Dr. Kelin Kuhn ("Kuhn Decl.," EX1003).

B. Statutory Grounds of Challenge

Petitioner relies on the following prior art and statutory grounds of challenge to the challenged claims:

Name	Ex.	Publication No.	Filed	Published	Prior art under at least
Lung	1004	US2011/0286283	5/21/2010	11/24/2011	§102(e)
Park	1005	US2010/0120214	11/10/2009	5/13/2010	§§102(a) & (e)
Mokhlesi	1006	US2008/0242028	3/27/2007	10/2/2008	§102(b)
Fukuzumi	1007	US2009/0146190	12/1/2008	6/11/2009	§102(b)

Ground	Claims	Basis	References
1 & 2	8 and 21	§§102/103	Lung
3	8, 13, and 21	§103	Park in view of Mokhlesi
4	8 and 21	§103	Fukuzumi in view of Mokhlesi

Lung was filed before the filing date of the '214 patent, June 28, 2010, and therefore qualifies as prior art under pre-AIA 35 U.S.C. §102(e).

Park was published before June 28, 2010, and thus qualifies as prior art under pre-AIA 35 U.S.C. §102(a). Park also qualifies as prior art under pre-AIA 35 U.S.C. §102(e), as its filing date predates June 28, 2010.

Each of Mokhlesi and Fukuzumi was published more than one year before June 28, 2010, and thus qualifies as prior art under at least pre-AIA 35 U.S.C. §102(b).

V. THE ’214 PATENT

A. Overview

The ’214 patent relates to nonvolatile memory devices. EX1001, 1:6-8; 2:63-67. The ’214 patent recognizes that “[s]ince 3D memory devices are relatively new, manufacturing these devices can pose fabrication process challenges” and thus, proposes embodiments related to memory devices and methods of forming the devices. EX1001, 1:20-22, 12:30-31. The memory devices include multiple groups of memory cells in different device levels. EX1001, 12:32-41.

FIG. 3 of the ’214 patent below (annotated in Kuhn Decl. as FIG. B) shows the embodiment of a memory device 200 related to the challenged claims. EX1003, ¶57.

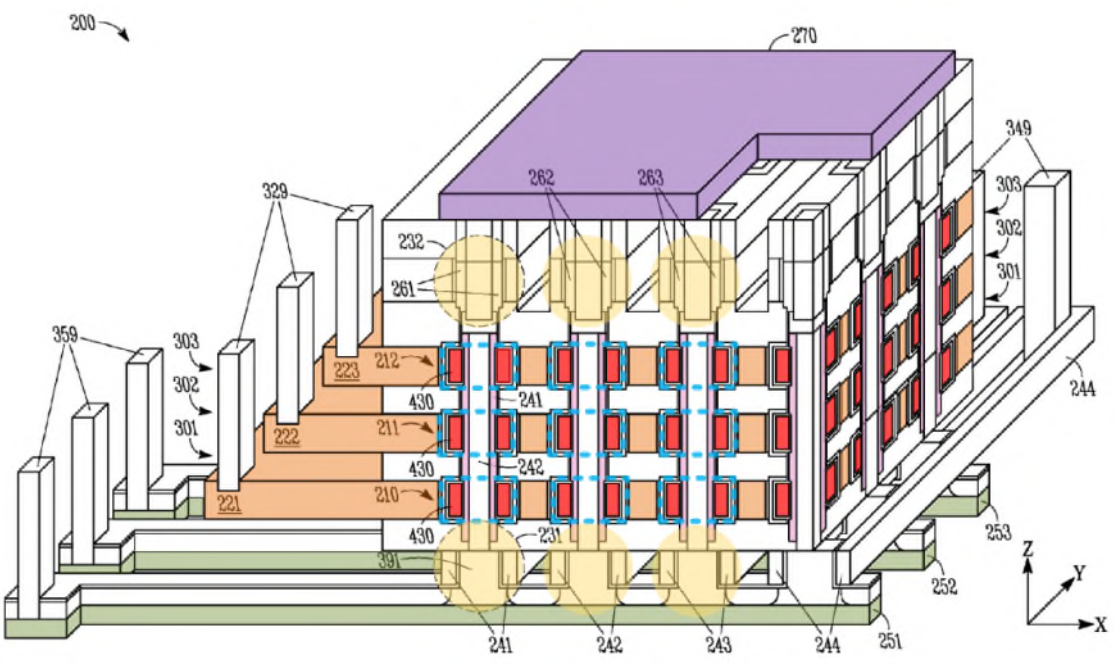


FIG. 3

EX1003 — FIG. B

Memory device 200 includes a string of memory cells 210-212 in the Z-direction, and channel 241 (in pink) extending in the Z-direction through ring-shaped memory elements 430 (in red) of memory cells 210-212. EX1001, 3:65-4:33. EX1003, ‖57. Memory elements 430, formed in cavities (in blue dashed boxes) of control gates 221-223 (in orange), store charge. EX1001, 4:34-5:3, 7:43-8:38; EX1003, ‖58. A common source 270 (in purple) is formed above memory cells 210-212 and is coupled with channels 241 through upper select transistors 232 (in yellow), while data lines 251-253 (in green) are formed below memory cells 210-212 and are coupled with channels 241 through lower select transistors 231 (in yellow). EX1001, 4:9-33, 5:7-11, 5:39-51, 9:56-64; EX1003, ¶59.

The ’214 patent also discloses “a substrate underneath data lines 251, 252, and 253,” although not shown in FIG. 3. EX1001, 4:9-14.

B. Prosecution History

In the first Office Action on the merits, the Examiner rejected claims 1-6 and 9-21 as being unpatentable over U.S. Patent Application Publication No. 2009/0230454 in the name of Pekny (“Pekny”) under pre-AIA 35 U.S.C. § 103(a), and rejected claims 7 and 8 as being unpatentable over Pekny in view of U.S. Patent Application Publication No. 2007/0057310 in the name of Matsui *et al.* (“Matsui”) under pre-AIA 35 U.S.C. §103(a). EX1002, 206-215. In response, PO amended, among other claims, claims 4 and 20 (now claims 8 and 21, respectively) and argued

that Pekny failed to disclose the claimed relative vertical positions between the common source, data line, substrate, memory cells/control gates: "*the first and second memory cells are between the common source and the substrate*" (claim 4), and "*the data line is located between the second conductive material and the substrate*" (claim 20). EX1002, 149-159.

In the Final Office Action, the Examiner maintained the rejection of claims 9-14 over Pekny. EX1002, 138-141. The Examiner also indicated that claims 1-8 and 15-21 were allowed, and the allowable subject matter related to "*a plurality of second memory cells*" in claim 1, "*a common source,*" "*data lines,*" and the relative positions between "*the first and second memory cells,*" "*the common source*," and "*the substrate*" in claim 4, and "*a second conductive material*" in claims 15 and 20. EX1002, 141-142.

In response, PO amended independent claim 9 to include the limitation that the first and second memory elements are in different device levels. EX1002, 122-128.

The Examiner eventually allowed all claims in the Notices of Allowance, noting that the prior art on the record failed to teach claim limitations related to "*a second control gate*" and "*data lines*" in then claims 1, 4, 9, and 20, and "*a second dielectric*" and "*a conductive channel*" in claim 15. EX1002, 40-41, 102-103.

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C. The Level of Ordinary Skill in the Art

A POSITA at the time of the claimed invention would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. EX1003, ¶31. A higher level of education might make up for less experience, and vice versa. EX1003, ¶31.

VI. CLAIM CONSTRUCTIONS

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor,* 868 F.3d 1013, 1017 (Fed. Cir. 2017). Because the prior art asserted herein discloses embodiments within the claims' indisputable scope, the Board need not construe the claims' outer bounds. Other than the term "*cavity*" recited in challenged claims 8 and 21, as noted below, all claim terms should be construed according to their plain and ordinary meaning as would have been understood by a POSITA.

In the NDCA case[2], Petitioner proposes that "a [first-fourth] cavity of [first/second] control gate" should be construed as "a [first-fourth] hole with a larger

[2] The same term "*cavity*" is recited in claims 1 and 17 of the child '903 patent, which is asserted in the NDCA case.

diameter than holes in the layers immediately above and below the [first/second] control gate." EX1008, 17-18. PO asserts those terms should be given their plain and ordinary meaning, without specifying the meaning. EX1008, 17-18. The court in the NDCA case has not construed the term yet.

Regardless, the prior art discloses this limitation under either party's construction (*see* Grounds 1-4).

VII. GROUNDS 1 AND 2: LUNG ANTICIPATES OR OTHERWISE RENDERS OBVIOUS CLAIMS 8 AND 21

A. Overview of Lung

Lung relates to 3D memory devices having multiple planes of memory cells. EX1004, [0002]. Lung recognizes that "the need for higher and higher memory capacity in integrated circuit memory devices continues to increase" and "[3D] stacking is an efficient way to reduce the cost per bit for semiconductor memory." EX1004, [0007], [0110]. Lung provides 3D memory devices having "a large number of stackable layers of cells, resulting a high density NAND architecture flash memory device which overcomes the prior art limitation on the number of stackable layers of cells imposed by the impedance of a vertical string of cells of a single NAND string." EX1004, [0009].

In the main embodiment of Lung, as shown in annotated FIG. 4 below, a 3D memory device 100 includes bit lines 134-136 (in green) over a substrate (not

shown), select lines 137-139 (in yellow) for bottom set of pillar select transistors 106 (shown in FIG. 1) over bit lines 134-136, word line 410-418 (in orange) in various levels over select lines 137-139, and a common source plane 147 (in purple) over word line 410-418. EX1004, [0054], [0057]; EX1003, ¶72.

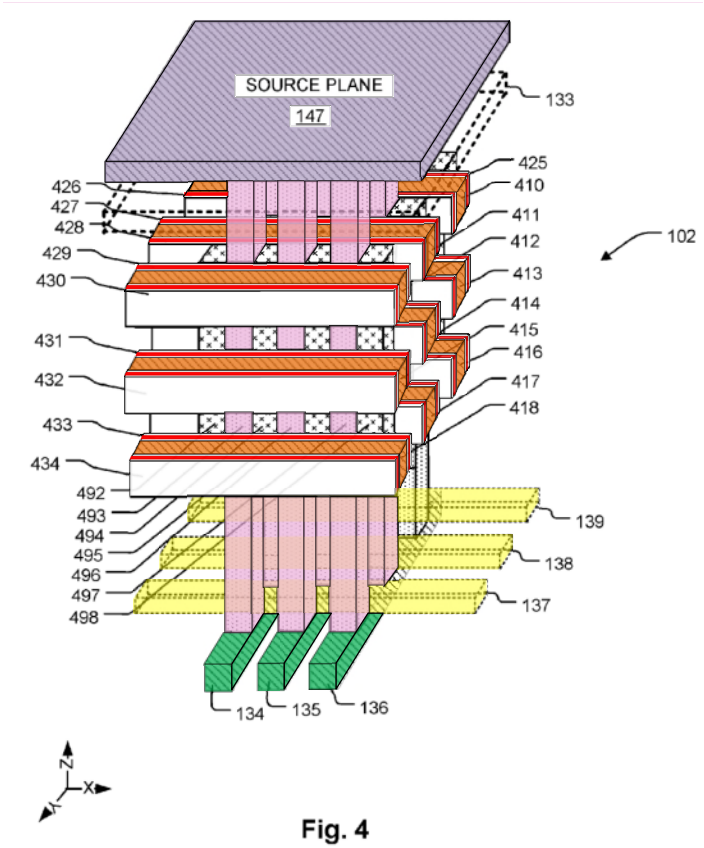


Fig. 4

EX1003 — FIG. C

3D memory device 100 also includes an array of semiconductor pillars 493, 495, and 497 (in pink) vertically extending between common source plane 147 and bit lines 134-136. EX1004, [0054], [0057]. 3D memory device 100 further includes charge storage structures 425-434 (in red) on the opposing sides of word line 410-418. EX1004, [0054], [0057]. Multiple levels of memory cells are formed at the

cross points of semiconductor pillars 493, 495, and 497 and charge storage structures 425-434 over bit lines 134-136. EX1004, [0057]; EX1003, ¶73.

Regarding the memory cells, annotated FIG. 5 of Lung below shows memory cells 500-L/R, 502-L/R, and 504-L/R in three different levels in the Z-direction, respectively. EX1004, [0058]-[0062]; EX1003, ¶74.

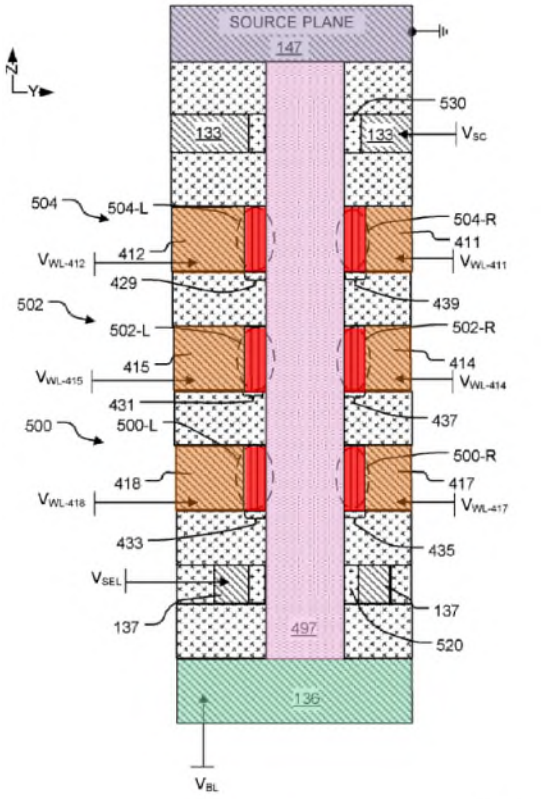


Fig. 5

EX1003 — FIG. D

Each memory cell 500-L/R, 502-L/R, or 504-L/R includes a portion of a respective word line 418, 417, 415, 414, 412, or 411 (in orange) as the gate, and a respective charge storage structure 433, 435, 431, 437, 429, or 439 (in red) as the charge storage element. EX1004, [0059]-[0061]. Each charge storage structure 429,

431, 433, 435, 437, or 439 is formed between the respective word line 412, 415, 418, 417, 414, or 411 and semiconductor pillar 497 (in pink). EX1004, [0058]; EX1003, ¶75. Lung further discloses that the charge storage structure has an "ONO" structure, including "a tunneling layer in contact with the word line, a charge trapping layer over the tunneling layer, and a blocking layer over the charge trapping layer." EX1004, [0011], [0052].

B. Independent Claim 8

1. Lung discloses "*[a]n apparatus*" [8.P].

Lung discloses an integrated circuit 1875 ("*apparatus*"). EX1004, [0108], FIG. 18. Thus, Lung discloses [8.P].

2. Lung discloses "*a plurality of first memory cells located in a first device level of a memory device*" [8.a], and "*a plurality of second memory cells located in a second device level of the memory device*" [8.b].

As illustrated in annotated FIGs. 4 and 5 below, Lung discloses that integrated circuit 1875 includes a first group of memory cells (in brown dashed box in FIG. 4), including 500-R (in brown dashed box in FIG. 5) ("*a plurality of first memory cells*") located in a "bottom level" of 3D memory device 100 ("*a first device level of a memory device*"), and a second group of memory cells (in orange dashed box in FIG. 4), including 502-R (in orange dashed box in FIG. 5) ("*a plurality of second memory cells*") located in a "next lower level" of 3D memory device 100 ("*a second device level of the memory device*"). EX1004, [0054], [0058]-[0060]; EX1003, ¶96. Thus,

Lung discloses [8.a] and [8.b].

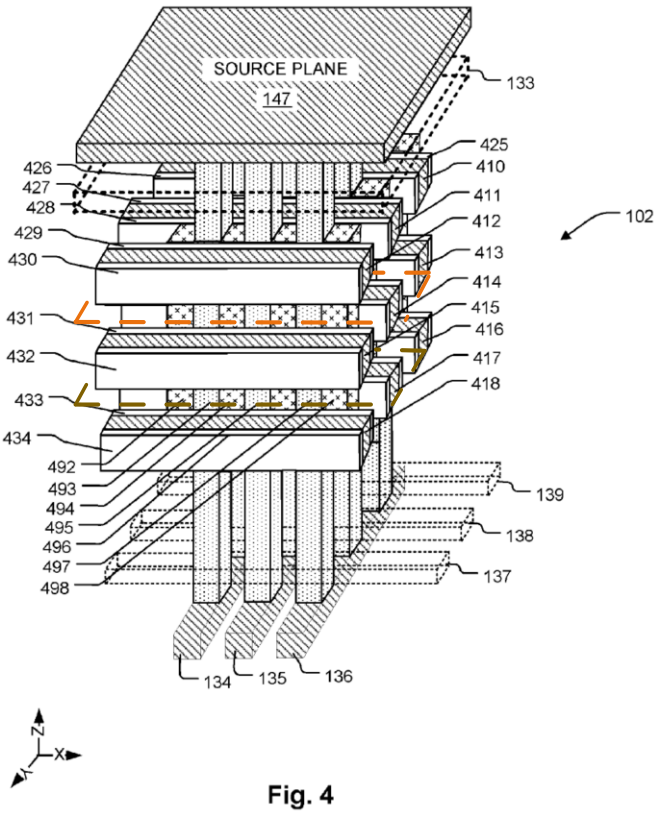


Fig. 4

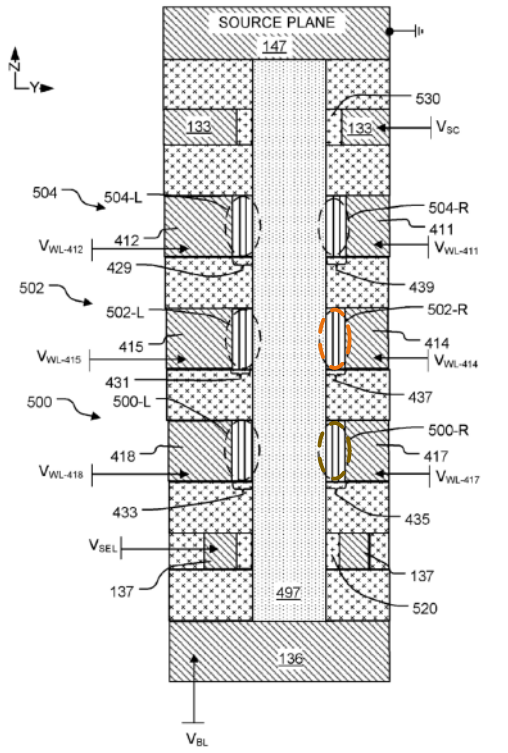


Fig. 5

EX1003 — FIG. I

3. Lung discloses or suggests "*a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate*" [8.c], "*a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate,*" [8.d.1], and "*wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction*" [8.d.2].

Lung discloses that "a next lower level includes word lines 413, 414 and 415,

and a bottom level includes word lines 416, 417 and 418." EX1004, [0054]. Lung also discloses "each cell including a charge trapping element and a gate," for example, "right cell 500-[R] includes word line 417 as the gate" and "right cell 502-[R] includes word line 414 as the gate." EX1004, [0051], [0059]-[0060].

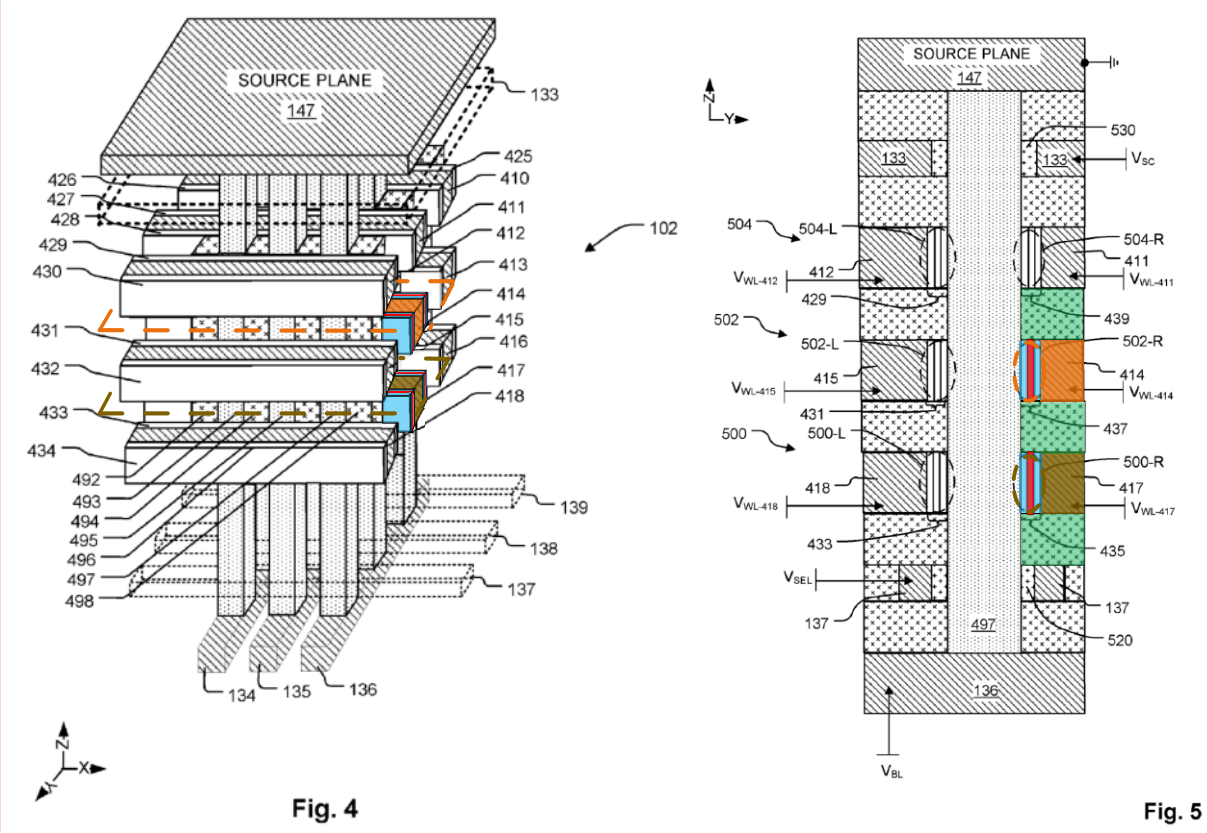


Fig. 4 Fig. 5

EX1003 — FIG. J

Thus, as shown in annotated FIGs. 4 and 5 above, 3D memory device 100 also includes, for instance, first word line 417 (in brown, "*a first control gate*") formed in the same bottom level ("*first device level*") as the first group of memory cells (in brown dashed box), including 500-R, as well as second word line 414 (in orange "*a second control gate*") formed in the same next lower level ("*second device level*")

as the second group of memory cells (in orange dashed box), including 502-R. EX1003, ¶¶99-100.

Lung further discloses applying bias voltages to word lines 410-418, including first and second word lines 417 and 414, when operating the first and second groups of memory cells, including first and second memory cells 500-R and 502-R. EX1004, [0064]-[0067]; EX1003, ¶101. Thus, a POSITA would have understood that first word line 417 controls access to the first group of memory cells, including 500-R ("*the first control gate to control access to the first memory cells"*), and that second word line 414 controls access to the second groups of memory cells, including 502-R ("*the second control gate to control access to the second memory cells"*). EX1003, ¶101.

Further, Lung discloses "each cell including a charge trapping element and a gate," for example, "right cell 500-[R] includes … charge storage structure 435 as the charge storage element" and "right cell 502-[R] includes … charge storage structure 437 as the charge storage element." EX1004, [0051], [0059]-[0060]. Specifically, Lung discloses that the charge storage structure includes a silicon nitride layer as a charge trapping layer. EX1004, [0052]. A POSITA would have understood that the silicon nitride charge trapping layer in charge storage structure 435/437 is the claimed "*memory element*." EX1003, ¶102.

Since Lung further discloses that "memory cells [are] formed at the cross

points of the semiconductor pillars 493, 495, 497 and the charge storage structures 425-430 on the opposing sides of the word lines (*e.g.*, 410-412)," a POSITA would have understood that each word line has openings where the corresponding charge storage structures are formed. EX1004, [0057]; EX1003, ¶103. That is, each charge storage structure creates an opening in the corresponding word line that controls access to the respective memory cell. EX1003, ¶103.

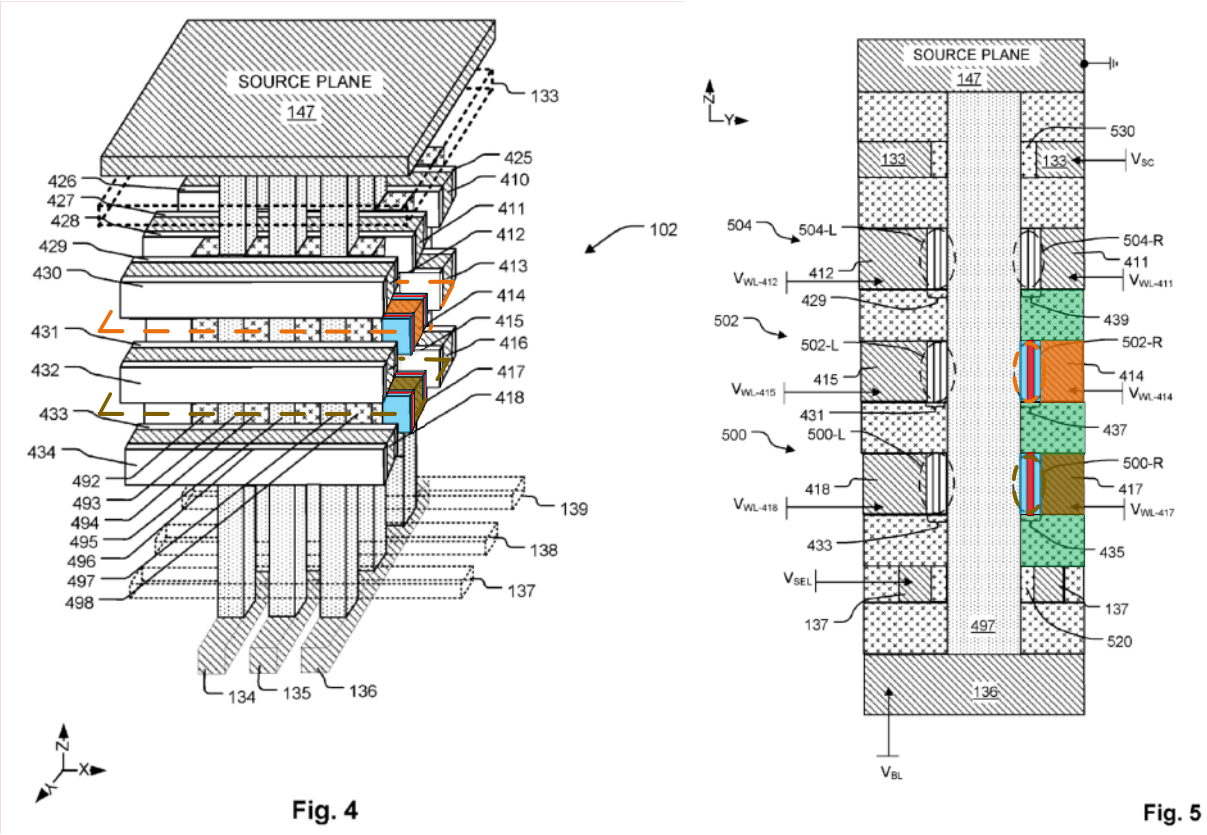


Fig. 4 Fig. 5

EX1003 — FIG. J

This is illustrated in annotated FIGs. 4 and 5 above, where charge trapping layers (in red, "*memory elements*") in the charge storage structures, including 435 and 437, of the first and second groups of memory cells, including 500-R and 502-

R, are formed in the openings (in blue,) of first and second word lines 417 and 414 (in brown and orange, "*first and second control gates*"), respectively. EX1003, ¶104. As shown in annotated FIG. 5 above, each opening (in blue) forms a recess within first or second word line 417 or 414 (in brown or orange) in a control gate layer, relative to the insulation material layers (in green) above and below the control gate layer. EX1004, [0062]; EX1003, ¶105.

As shown in annotated FIG. 4 above, each of the first and second first groups of memory cells (in brown and orange dashed box, "*the first and second memory cells*") includes a plurality of memory cells along the X-direction ("*a first direction*") and **two** memory cells along the Y-direction ("*a second direction*"). EX1004, [0057]; EX1003, ¶106. A POSITA would have understood, as shown in annotated FIG. 5 above, the two memory cells of the first memory group in the Y-direction include, for example, 500-R (in brown dashed box) and another one (not shown) on the opposite end of first word line 417 (in brown) in the Y-direction, and the two memory cells of the second memory group in the Y-direction include, for example, 502-R (in orange dashed box)and another one (not shown) on the opposite end of second word line 414 (in orange) in the Y-direction. EX1003, ¶107. Thus, Lung discloses [8.d.2].

Therefore, Lung discloses or suggests [8.c], [8.d.1], and [8.d.2].

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4. Lung discloses "*a common source*" [8.e].

As shown in annotated FIG. 4 below, Lung discloses a source plane 147 (in purple). EX1004, [0027], [0034], [0054], [0057]; EX1003, ¶109. Specifically, Lung discloses that source plane 147 is coupled to array of semiconductor pillars 493, 495, and 497 (in pink), which correspond to an array of NAND memory strings. EX1004, [0045]-[0046], [0056]-[0057]. A POSITA would have understood that source plane 147 in FIG. 4 is "common" to multiple NAND strings of memory cells, for example, for sourcing current. EX1003, ¶110. Thus, Lung discloses [8.e].

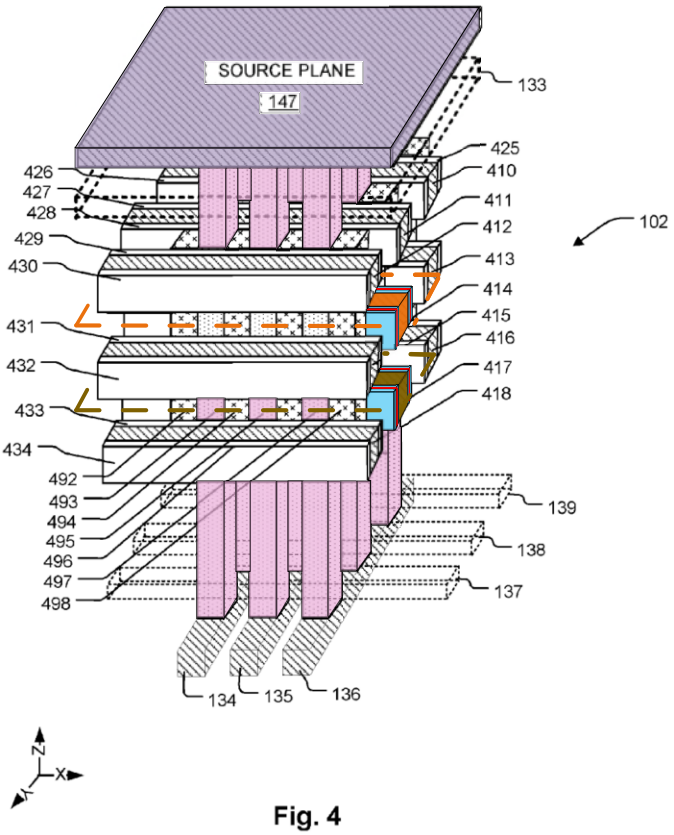


Fig. 4

EX1003 — FIG. K

5. Lung discloses "*data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions*" [8.f.1] and "*wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate*" [8.f.2].

As shown in annotated FIGs. 4 and 5 below, Lung discloses bit lines 134-136 (in green, "*data lines*") electrically connected to common source plane 147 (in purple, "*common source*") and the first and second groups of memory cells in the bottom and next lower levels (in brown and orange dashed boxes, "*first and second memory cells*") through semiconductor pillars 493, 495, and 497 (in pink). EX1004, [0039], [0045,] [0055]-[0057]; EX1001, 3:29-31; EX1003, ¶¶111-112.

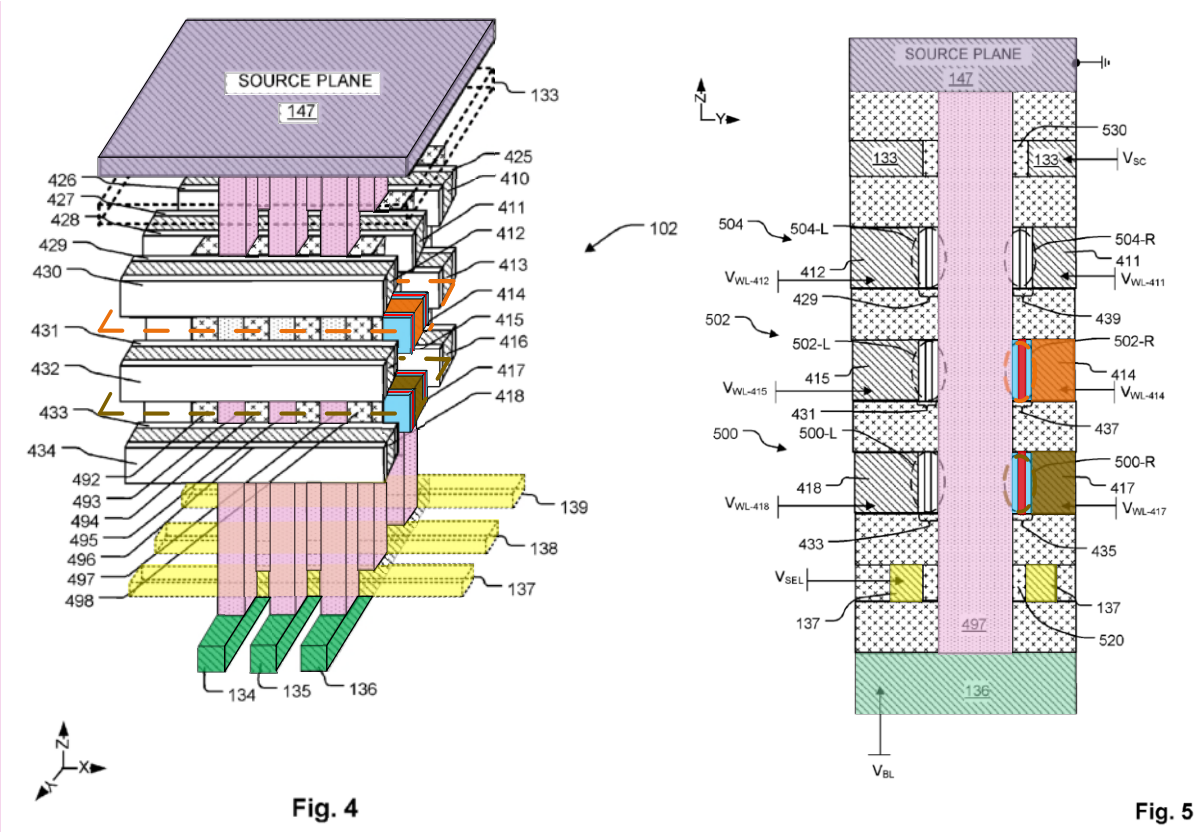


Fig. 4 Fig. 5

EX1003 — FIG. L

Lung also discloses a bottom set of pillar select transistors 106 (FIG. 1) coupled to select lines 137-139 (in yellow) "**selectively** couple a Z-direction column of the two-cell unit structures 120-128 to a corresponding bit line in a plurality of bit lines 134, 135, 136 extending in the Y-direction," such that "bit lines 134, 135, 136 are coupled to a column decoder." EX1004, [0010], [0031]-[0032], [0054]. A POSITA would have understood that the electrical connection between bit lines 134-136 and semiconductor pillars 493, 495, and 497 are controlled by bottom set of pillar select transistors 106, and that the column decoder selects/deselects each NAND string of memory cells along a respective semiconductor pillar 493, 495, or

497 by turning bottom set of pillar select transistors 106 on or off to control the connections between bit lines 134-136 and semiconductor pillars 493, 495, and 497, through select lines 137-139. EX1003, ¶113. Therefore, Lung discloses that bit lines 134-136 are configured to be "*selectively*" coupled to common source plane 147 and the first and second groups of memory cells through semiconductor pillars 493, 495, and 497. EX1003, ¶114.

Regarding semiconductor pillars 493, 495, and 497, since Lung discloses that they are formed of "doped semiconductor material," such as "p-type polysilicon," a POSITA would have understood that semiconductor pillars 493, 495, and 497 having p-type polysilicon material includes "*a conductive material*," consistent with the '214 patent. EX1004, [0073], claim 12; EX1001, 8:64-67; EX1003, ¶115.

Further, since Lung discloses semiconductor pillar 497 is in a Z-direction column, and the memory cells are formed along semiconductor pillars 493, 495, and 497, Lung likewise discloses "*conductive material*" of the semiconductor pillars extending through the first and second groups of memory cells (the "*first and second memory cells*") in the Z-direction ("*a third direction*") perpendicular to the X- and Y-directions (the "*first and second directions*"). EX1004, [0057]-[0058]; EX1003, ¶116. Thus, Lung discloses [8.f.1].

Regarding [8.f.2], FIGs. 4-5 of Lung disclose the claimed relative vertical positions of the "*common source*," "*substrate*," and "*memory cells*": the "*common*

source" is formed over the "*memory cells*," which are in turn formed over the "*substrate*." EX1001, 5:30-38; EX1003, ¶117. Specifically, Lung explicitly discloses that "FIG. 4 shows a memory device that comprises a plurality of bit lines 134, 135, 136 over a substrate," "memory cells … lie[] over the plurality of bit lines," and "source plane 147 is over the plurality of memory cells." EX1004, [0008], [0057].

From the foregoing, Lung anticipates or otherwise renders obvious claim 8.

C. Independent Claim 21

1. Lung discloses "*[a]n apparatus*" [21.P].

Lung discloses [21.P], which is the same as [8.P]. *See* Section VII.B.1.

2. Lung discloses or suggests "*a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall*" [21.a], and "*a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall*" [21.b].

As discussed in Section VII.B.3, Lung discloses or suggests "*a first/second control gate formed in the first/second device level, ..., wherein each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.*"

Lung further discloses, as parts of the process of manufacturing 3D memory device 100, forming "layers 722, 724, 726, and 728 of word line materials, such as

n+-polysilicon" EX1004, [0069]. A POSITA would have understood that word lines 410-418 are patterned from layers 722, 724, 726, and 728, such that first and second word lines 417 and 414 ("*first/second control gate*") are made of word line materials, such as n-type polysilicon. EX1004, [0070]; EX1003, ¶123.

Regarding the "*first/second conductive material located in a first/second device level, … including a first/second cavity*" recited in claim 21, the specification of the '214 patent describes that "[m]aterials 1002, 1004, and 1006 can include **conductive materials**, such as metal or polysilicon (*e.g.*, n-type silicon for p-type silicon)," and "[f]orming cavities 1120 in materials 1002, 1004, and 1006 also form control gates 1221, 1222, and 1223, which can correspond to [] control gates 221, 222, and 223 of FIG. 2." EX1001, 7:3-5, 39-42.

Thus, a POSITA would have understood that, as shown in annotated FIGs. 4 and 5 below, first word line 417 (in brown) made of n-type polysilicon is "*a first conductive material,*" consistent with the '214 patent. EX1001, 7:3-5, 39-42; EX1003, ¶125. Similarly, second word line 414 (in orange) made of n-type polysilicon is "*a second conductive material.*" EX1003, ¶125.

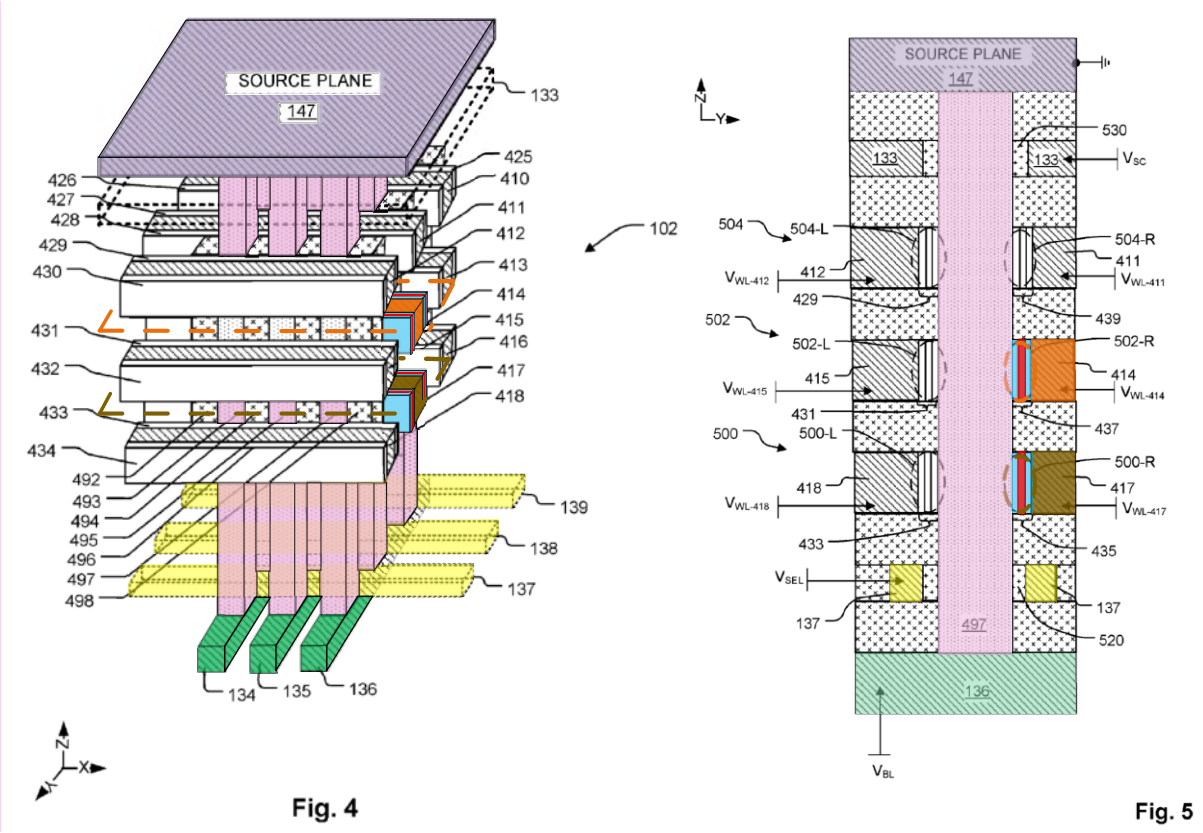


Fig. 4 Fig. 5

EX1003 — FIG. M

Lung further discloses "trenches having sidewalls 830-833 on which the layers of word line materials are exposed at each level of the structure," and "charge trapping structures (940-943) over and on the sidewalls of the trenches (845-848) contacting the layers of word line material." EX1004, [0070]-[0071]. As further shown in annotated FIGs. 4 and 5 above, a POSITA would also have understood, or at least found it obvious, that the opening (in blue, "*a first cavity*") in first word line 417 (in brown) has a respective sidewall (*e.g.*, 830-833) on which charge storage structures, *e.g.*, 435, are formed, and that the opening (in blue, "*a second cavity*") in second word line 414 (in orange) has a respective sidewall (*e.g.*, 830-833) on which

charge storage structures, *e.g.*, 437 are formed. EX1003, ¶127; Section VII.B.3.

Thus, Lung discloses or suggests [21.a] and [21.b].

3. Lung discloses "*a first dielectric formed on the first sidewall and the second sidewall*" [21.c], "*a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric*" [21.d], "*a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric*" [21.e], and "*a second dielectric formed on a side of the first memory element and on a side of the second memory element*" [21.f].

As discussed in Section VII.B.3, Lung discloses "*each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.*"

Lung further discloses that the charge storage structure includes an "ONO" structure, having "a tunneling layer in contact with the word line material, the charge trapping layer over the tunneling layer, and a blocking layer over the charge trapping layer, such as used in typical charge trapping memory devices." EX1004, [0052].

Thus, as shown in annotated FIG. 5 below, a POSITA would have understood that 3D memory device 100 further includes a tunneling layer (in green, "*a first dielectric*") of charge storage structures, *e.g.*, 435 and 437, which is formed on the sidewalls of the openings (in blue dashed box, "*first and second cavities*") in first and second word lines 417 and 414 (in brown and orange). EX1003, ¶131.

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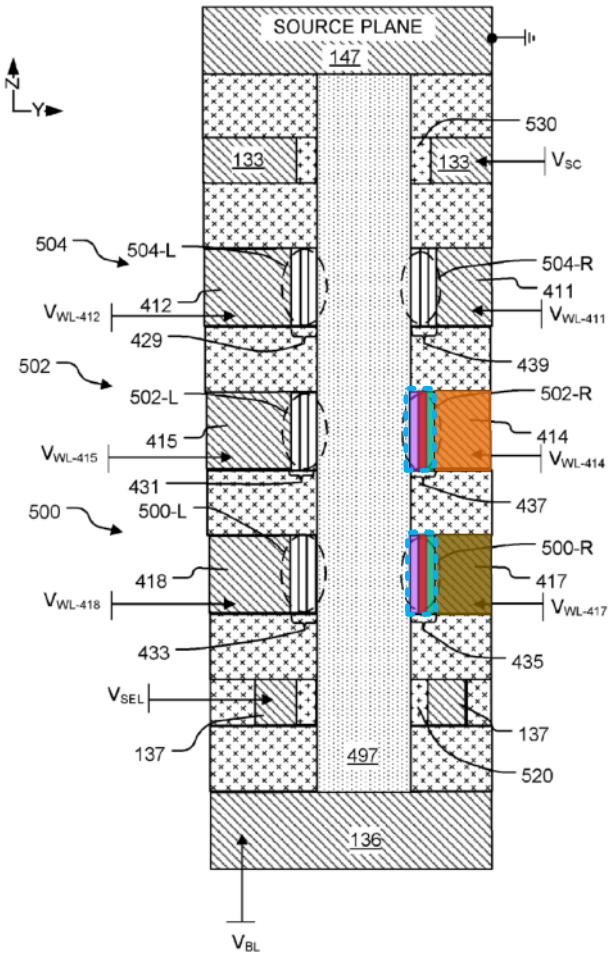


Fig. 5

EX1003 — FIG. N

A POSITA would have understood that 3D memory device 100 further includes a blocking layer (in purple, "*a second dielectric*") of charge storage structures, *e.g.*, 435 and 437, which is formed on the sides of the corresponding charge trapping layers (in red, "*first/second memory elements*"). EX1003, ¶132.

Lung specifically discloses that the tunneling layer may be "a layer of silicon dioxide or silicon oxide nitride" and "in contact with the word line material," and

that the charge trapping layer is "over the tunneling layer." EX1004, [0052]. As shown in annotated FIG. 5 above, a POSITA would have understood that the charge trapping layer (in red, "*first/second memory element*") is electrically isolated from the respective first or second word line 417 or 414 (in brown or orange, "*first/second conductive material*") by a respective portion of the tunneling layer (in green, "*first dielectric*"). EX1003, ¶134.

Thus, Lung discloses or suggests [21.c]-[21.f].

4. Lung discloses "*a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric*" [21.g].

Lung discloses that "memory cells [are] formed at the cross points of the semiconductor pillars 493, 495, 497 and the charge storage structures 425-430… at least one memory cell of the plurality of memory cells is over another one memory cell of the plurality of memory cells, such as by being on the same semiconductor pillar as a lower cell." EX1004, [0057]. Lung also discloses that in a read operation, "a current path is established between the bit line 134 and the source plane 147 via the particular NAND string to which the selected memory cell belongs." EX1004, [0045]. Thus, a POSITA would have understood that, during certain operations of Lung's memory device, a channel of NAND string of memory cells forms in the

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vertical outermost layer of the semiconductor pillar 493, 495, or 497 and does not extend throughout the entire semiconductor pillar. EX1004, 1600a in FIG. 16; EX1017, [0063], [0070], FIG. 11; EX1003, ¶¶138-139. Thus, Lung discloses the claimed "*conductive channel*."

Further, since Lung discloses semiconductor pillar 497 is in a Z-direction and the memory cells are formed along semiconductor pillars 493, 495, and 497, a POSITA would have understood that semiconductor pillar 497, including its vertical outermost layer ("*conductive channel*") extends from the bottom level to the next lower level where the first and second groups of memory cells are located, respectively. EX1004, [0057]-[0058], FIGs. 4-5; EX1003, ¶140.

As discussed in Section VII.C.3 and shown in annotated FIG. 5 below, since Lung further discloses that "blocking layer [is] between the dielectric charge trapping layer and the given semiconductor pillar," and that "the blocking layer may comprise a layer of silicon dioxide or a high-k material typical in SONOS type memory device," a POSITA would have understood that the vertical outermost layer of semiconductive pillar 497 (in black, "*conductive channel*") faces the charge trapping layers (in red, "*first and second memory elements*"), but is electrically isolated from the charge trapping layers by a respective portion of the blocking layer (in purple, "*a first/second portion of the second dielectric*"). EX1004, [0052], claim 5; EX1003, ¶141.

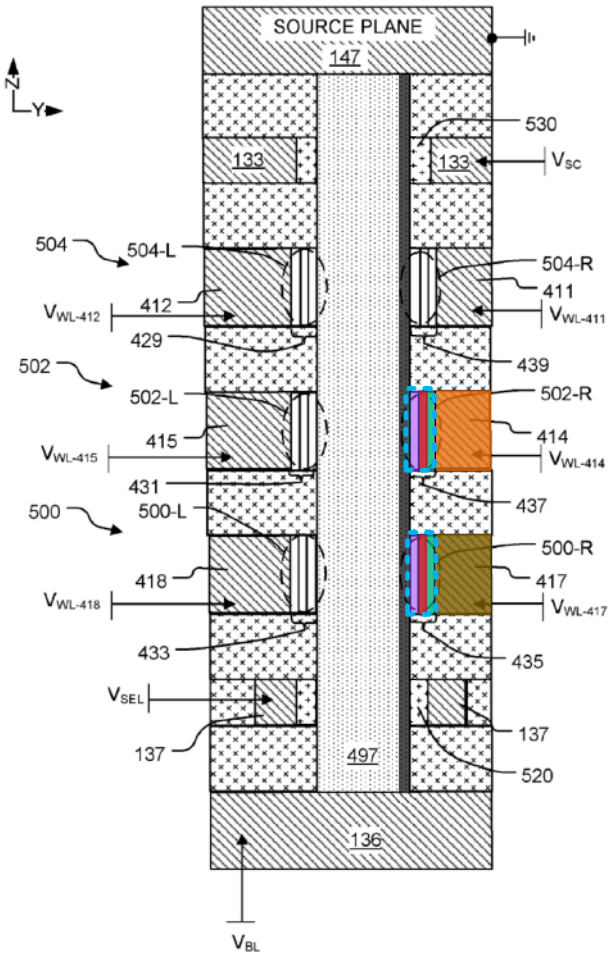


Fig. 5

EX1003 — FIG. P

Therefore, Lung discloses [21.g].

5. Lung discloses "*a substrate*" [21.h], and "*a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate*" [21.i].

As shown in annotated FIG. 5 below, a POSITA would have understood, or at least found it obvious, that bit line 136 (in green, "*data line*") is coupled to semiconductor pillar 497, including its vertical outermost layer (in black,

"*conductive channel*"). EX1004, [0055]; EX1003, ¶143.

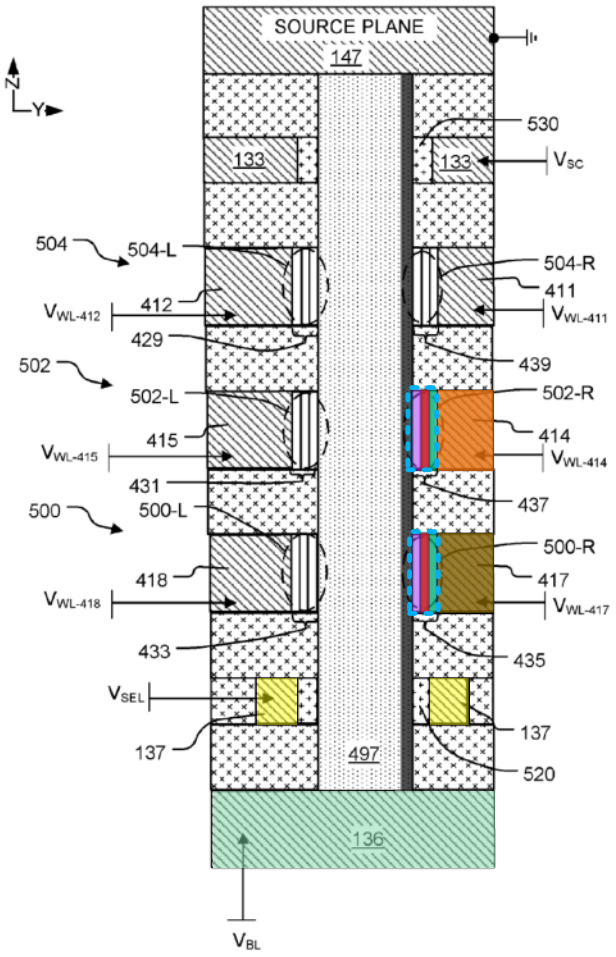


Fig. 5

EX1003 — FIG. Q

Lung also discloses a bottom set of pillar select transistors 106 (FIG. 1) coupled to select line 137 (in yellow) "**selectively** couple a Z-direction column of the two-cell unit structures 120-128 to a corresponding bit line in a plurality of bit lines 134, 135, 136 extending in the Y-direction," such that "bit lines 134, 135, 136 are coupled to a column decoder." EX1004, [0010], [0031]-[0032], [0054]. A

POSITA would have understood that the electrical connection between bit line 136 and semiconductor pillar 497 is controlled by the bottom set of pillar select transistors 106 through select line 137. EX1003, ¶145. Therefore, Lung discloses that bit line 136 ("*data line*") is configured to be "*selectively*" coupled to the vertical outermost layer of semiconductor pillar 497 ("*conductive channel*"). EX1003, ¶145.

Lung further discloses "memory device that comprises a plurality of bit lines 134, 135, 136 **over a substrate**," and "[a] plurality of memory cells … lies(sic) over the plurality of bit line." EX1004, [0057]. As shown annotated FIG. 5 above, second word line 414 (in orange, ("*second conductive material*") is formed over bit line 136 (in green, "*data line*"), such that bit line 136 is located between second word line 414 and the substrate (not shown) underneath bit line 136. EX1003, ¶146.

Accordingly, Lung discloses [21.h] and [21.i].

From the foregoing, Lung anticipates or otherwise renders obvious claim 21.

VIII. GROUND 3: PARK IN VIEW OF MOKHLESI RENDERS OBVIOUS CLAIMS 8, 13, AND 21

A. Overview of Park

Park relates to a "nonvolatile memory device having a three-dimensional structure" and the manufacturing method thereof. EX1005, [0002]. Park aims to

"improv[e] reliability" of the 3D memory devices. EX1005, [0002].

FIGs. 2-10 relate to the first embodiment of Park. EX1005, [0020]-[0022]. Annotated FIGs. 2 and 3 below show the perspective view and cross-sectional view of the first embodiment, respectively. EX1003, ¶178.

Fig. 2

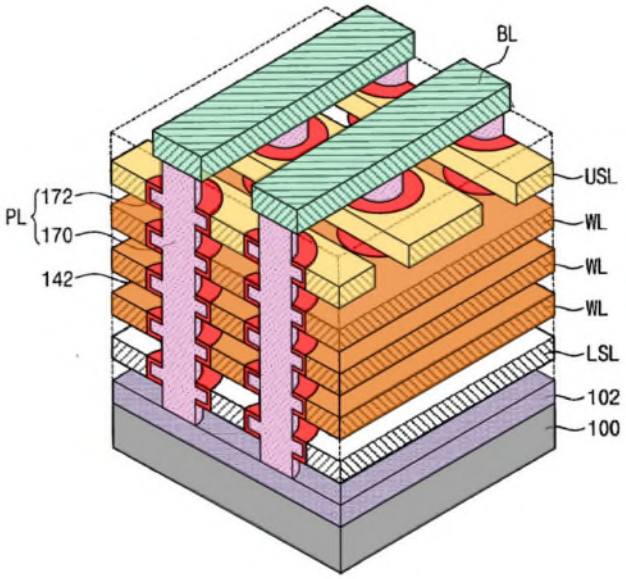
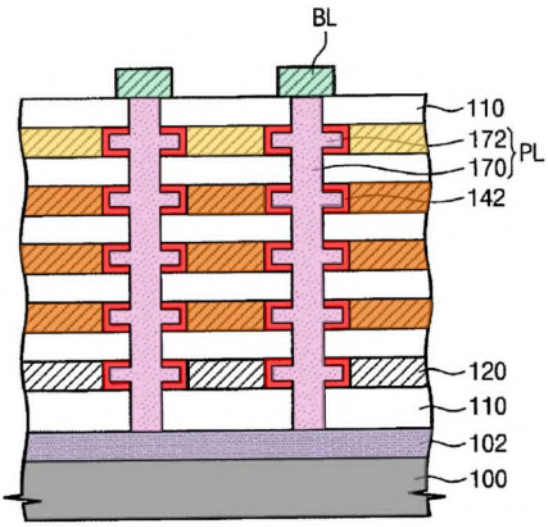


Fig. 3



EX1003 — FIG. E

The nonvolatile memory device includes bit lines BL (in green), upper select lines USL (in yellow), word lines WL (in orange), lower select lines LSL (white hatched), and an impurity region 102 (in purple) functioning as a common source line CSL on a semiconductor substrate 100 (in gray). EX1005, [0039], [0047]; EX1003, ¶79. The nonvolatile memory device also includes active pillars PL (in pink) penetrating upper select lines USL, word lines WL, and lower select lines LSL

120 to electrically connect bit lines BL and impurity region 102 on the opposite ends. EX1005, [0050]-[0051], [0056]; EX1003, ¶80. Bit lines BL are formed above impurity region 102, and impurity region 102 is disposed vertically between word lines WL and semiconductor substrate 100. EX1005, [0047], [0056]; EX1003, ¶80.

The nonvolatile memory device further includes charge storage layer patterns 142 (in red) disposed between protrusions 172 of active pillar PL and the sidewalls of each of the conductive layers (USL, WL, LSL). EX1005, [0054]. Charge storage layer pattern 142/charge storage layer 140 includes a charge blocking layer, a charge trapping layer, and a charge tunneling layer, such as an oxide layer, a nitride layer, and an oxide layer in this order (a.k.a. an ONO structure). EX1005, [0064]; EX1003, ¶81.

Park also discloses that the nonvolatile memory device includes a cell array arranged in a 3D structure and having a plurality of strings STR. EX1005, [0040]; EX1003, ¶82. Each string STR includes "a plurality of memory cells (MC) serially connected to each other between an upper transistor (UST) and a lower transistor (LST)." EX1005, [0040]. Active pillars PL correspond to the strings STR of the nonvolatile memory device, respectively. EX1005, [0050].

B. Overview of Mokhlesi

Mokhlesi relates to "three dimensional NAND strings and other three-dimensional devices." EX1006, [0002]. Similar to Park, Mokhlesi discloses 3D

memory devices including "an array of vertical NAND strings, [which] are vertically oriented, such that at least one memory cell is located over another memory cell." EX1006, [0013]; EX1003, ¶84. Mokhlesi explains that "[t]he array allows vertical scaling of NAND devices to provide a higher density of memory cells per unit area of silicon or other semiconductor material." EX1006, [0013].

Like Park, the nonvolatile memory devices of Mokhlesi also include memory cells having an ONO structure. EX1006, [0013], [0059]; EX1003, ¶85. Similar to Park, the memory array of Mokhlesi "have two or more memory cell levels," and "the select transistors for each NAND string[] may also be monolithically integrated into each NAND string above and/or below the memory cells." EX1006, [0013]; EX1003, ¶85.

Notably, Mokhlesi explicitly teaches that "source lines may be formed on top and the bit lines may be formed on the bottom. This allows formation of metal and/or silicide rather than semiconductor source lines, which leads to a decreased current crowding due to the lower resistivity source line material." EX1006, [0092]. Mokhlesi also explains that "source lines may be replaced by a common source region extending in both dimensions of the plane of the substrate and providing higher current sinking capability." EX1006, [0017], [0094].

C. Reasons to Combine Park and Mokhlesi

A POSITA would have found it obvious to modify Park's 3D memory device

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and fabrication method thereof in view of Mokhlesi's teaching of forming common source at the top and bit lines at the bottom of a 3D memory device for various reasons discussed below in detail. EX1003, ¶148.

1. The teaching, suggestion, and motivation in Park and Mokhlesi would have led a POSITA to rearrange Park's common source to the top with a metal/silicide material.

Park aims to improve the reliability of 3D NAND memory devices. EX1005, [0002]. Park discloses using impurity region 102 as a common source, which is formed of a semiconductor material. EX1005, [0040], [0047]; EX1003, ¶149.

As discussed in Section VIII.B, Mokhlesi explicitly teaches forming source lines at the top of the 3D NAND memory device, thereby "allow[ing] formation of metal and/or silicide rather than semiconductor source lines, which leads to a decreased current crowding due to the lower resistivity source line material." EX1006, [0092]; EX1003, ¶152.

Since Park's common source is also made of a semiconductor material, it suffers from the exact problem identified by Mokhlesi—"current crowding," which can cause reliability issues to Park's 3D memory device, including localized overheating, formation of thermal hotspots, aggravated electromigration effects, and formation of voids. EX1014, 1344; EX1015, 239, 242; EX1016, 1, 4; EX1003, ¶¶150-151, 153.

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Naturally, a POSITA would have been motivated to adopt Mokhlesi's solution to this problem—"source lines may be formed on top and the bit lines may be formed on the bottom" and "formation of metal and/or silicide rather than semiconductor source lines"—to Park's 3D memory device because doing so would "lead[] to a decreased current crowding due to the lower resistivity source line material," as explained by Mokhlesi. EX1006, [0092]; EX1003, ¶¶152-153. The decreased current crowding in the metal/silicide common source at the top of Park's modified 3D memory device would have advanced Park's goal of improving device reliability. EX1003, ¶154.

Although Mokhlesi's teaching is provided in an embodiment related to source lines, a POSITA would have understood that the same teaching applies equally to a common source region because Mokhlesi explicitly states that "the source lines 239 are be replaced by a common source region (source plane)." EX1006, [0094]; EX1003, ¶155.

Additionally or alternatively, a POSITA would have found it obvious to apply Mokhlesi's teaching regarding source lines to Park's common source (impurity region 102) because Mokhlesi explains that "common source plate provides a higher current sinking capability at the expense of loosing[sic] the ability to select individual source line voltage." EX1006, [0017], [0094]; EX1003, ¶156. Park's design can well accommodate it, since in Park's 3D memory device, the sources of

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all memory strings are commonly connected to impurity region 102, making it indifferent to the ability to select individual source line voltage. EX1005, [0039]-[0040], [0047], FIG. 2; EX1003, ¶156.

2. The proposed modification is merely applying Mokhlesi's known technique of forming metal/silicide common source at the top to Park's 3D memory device ready for improvement to yield predicable results.

Besides Mokhlesi's express teaching, it was well-known to a POSITA that metals/silicides have significantly improved resistivity in comparison to semiconductors. EX1009, 11; EX1003, ¶158. Notably, before the '214 patent, the memory industry had already recognized the resistivity issue associated with a common source located at the bottom of 3D NAND memory devices and proposed approaches similar to Mokhlesi's—forming common source at the top of 3D NAND memory devices to enable the use of low-resistivity metal materials. EX1012, 136-137; EX1013, 22-23; EX1003, ¶159. The industry also recognized the expected technical effect of reduced source resistance and the resulting performance improvement. EX1003, ¶159.

Therefore, POSITA would have understood that implementing Mokhlesi's modification in Park's structure would lead to a predictable reduction in current crowding, thereby enhancing the reliability and efficiency of the 3D memory device. EX1003, ¶¶160-161.

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3. A POSITA would have a reasonable expectation of success in forming metal/silicide common source at the top of Park's 3D memory device.

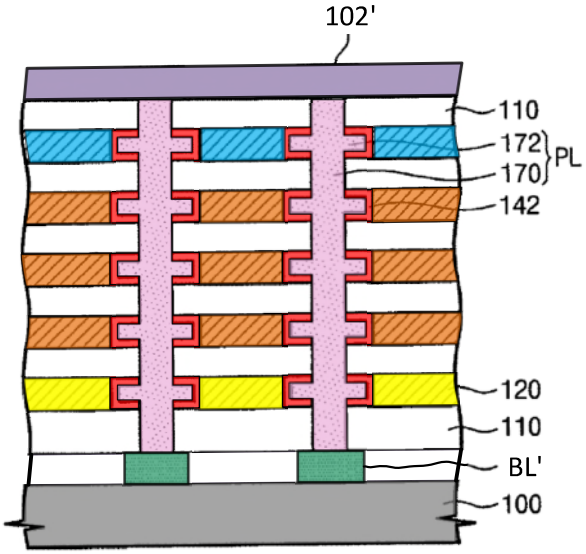
A POSITA would have a reasonable expectation of success for the proposed combination of Park and Mokhlesi. Mokhlesi's technique of forming a metal/silicide common source at the top of a 3D NAND memory device is directly applicable to Park's 3D NAND memory device because of the similarities between their devices, as discussed above in Section VIII.B. EX1003, ¶162.

Moreover, it would have been well within a POSITA's capabilities to form a metal/silicide common source above word lines WL in Park's 3D memory device without undue burden and with a reasonable expectation of success. EX1003, ¶164. Mokhlesi specifically teaches switching the relative positions of common source and bit lines. EX1006, [0094]; EX1003, ¶163. Following Mokhlesi's guidance, along with common knowledge in the art, a POSITA could easily modify Park's 3D memory device and fabrication process thereof to create a device where a metal/silicide common source is positioned at the top of the 3D memory device, replacing the semiconductor common source previously located at the bottom. EX1003, ¶164.

In a non-limiting example, as depicted in modified and annotated FIG. 3 of Park below, modified bit lines BL' (in green) are formed over semiconductor substrate 100 (in gray), drain-side select transistors and lines (in yellow) are formed

over modified bit lines BL', word lines (in orange) and charge storage layer patterns 142 (in red) are formed over the drain-side select transistors and lines, source-side select transistors and lines (in blue) are formed over word lines WL, and a metal/silicide common source 102' (in purple) is formed over the source-side select transistors and lines. EX1003, ¶165. The modification would neither impair the functionality of Park's 3D memory device nor complicate its manufacturing process. EX1003, ¶¶166-167.

Fig. 3



EX1003 — FIG. R
(Annotated and Modified FIG. 3 of Park)

D. Independent Claim 8

1. Park discloses [8.P].

Park discloses a memory system 1100 ("*apparatus*") including a memory

1130[3]. EX1005, [0106], [0108], FIG. 25. Thus, Park discloses [8.P].

2. Park discloses [8.a] and [8.b].

Park discloses that memory 1130 includes a nonvolatile memory device having a 3D structure, where "each xy plane includes m memory cells and the xy plane including m memory cells may be stacked to have n layers." EX1005, [0043].

Fig. 2

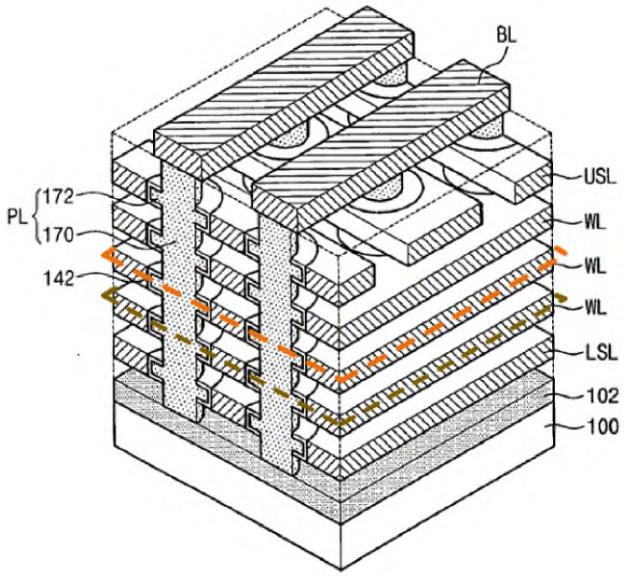
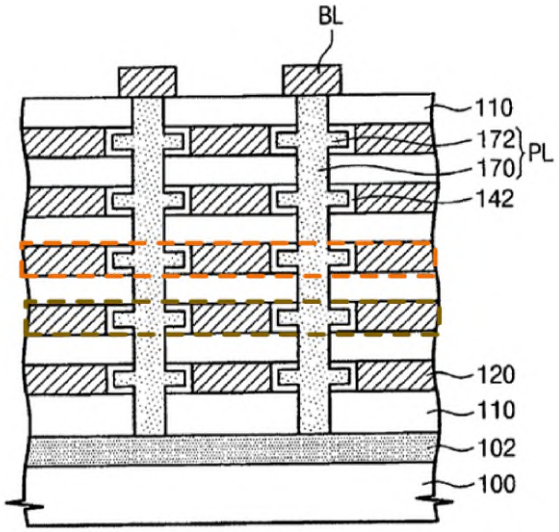


Fig. 3



EX1003 — FIG. T

With respect to the first embodiment, as shown in annotated FIGs. 2 and 3 above, Park discloses first memory cells (in brown dashed box) in a first layer of the nonvolatile memory device ("*a first device level of a memory device*"), and second memory cells (in orange dashed box) in a second layer of the nonvolatile memory

[3] Unless otherwise specified, Park's disclosures are applicable to the combination of Park and Mokhlesi used for mapping in Ground 3. EX1003, ¶¶167-168.

device ("*a second device level of the memory device*"). EX1005, [0043], [0048]; EX1003, ¶¶170-171. Thus, Park discloses [8.a] and [8.b].

3. Park discloses [8.c], [8.d.1], and [8.d.2].

As shown in annotated FIGs. 2 and 3 below, the nonvolatile memory device also includes a first conductive layer 120 (in brown, "*a first control gate*") formed in the first layer ("*first device level*") and used as a first word line WL to control access to the first memory cells in the first layer, as well as a second conductive layer 120 (in orange, "*a second control gate*") formed in the second layer ("*second device level*") and used as a second word line WL to control access to the second memory cells in the second layer. EX1005, [0041], [0047]-[0048]; EX1003, ¶¶174-175.

Fig. 2

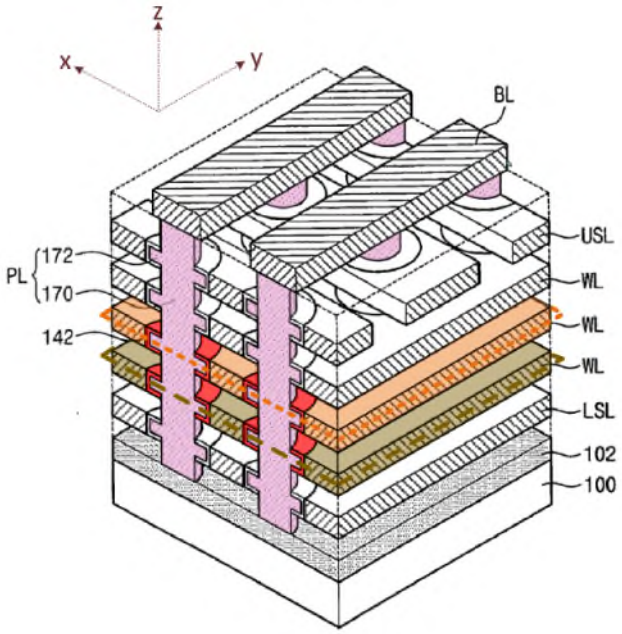
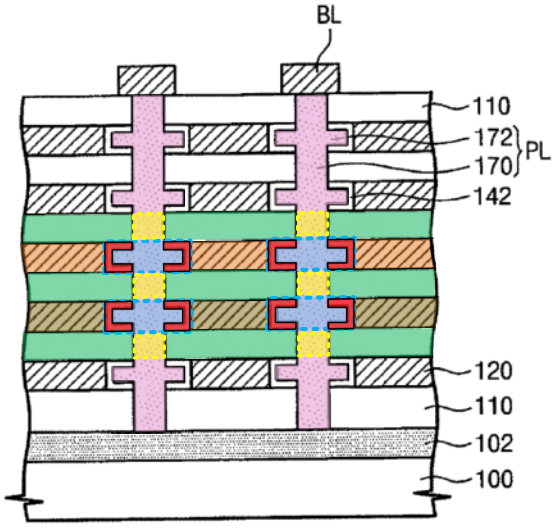


Fig. 3



EX1003 — FIG. U

Further, as shown in annotated FIG. 2 above, Park discloses that each of the first and second memory cells (in brown and orange dashed boxes) includes a charge storage layer pattern 142 (in red), which includes a charge trapping layer made of silicon nitride. EX1005, [0054], [0064]; EX1003, ¶176. A POSITA would have understood that a silicon nitride charge trapping layer is "*a memory element*." EX1003, ¶176.

Park also discloses "active pillars (PL) may penetrate the conductive layers (USL, WL, LSL)," and that "charge storage layer pattern 142 is disposed between the protrusion 172 of the active pillar (PL) and a sidewall of each of the conductive layers (USL, WL, LSL)." EX1005, [0050], [0054]. As shown in annotated FIG. 3 above, a POSITA would have understood that active pillar PL (in pink) and charge storage patterns 142 (in red) create a respective hole (in blue, "*cavity,*" *e.g.,* 136 and 134 in FIG. 5) through each of first and second conductive layers WL 120 ("*first/second control gate"*), in which active pillar PL and corresponding charge storage pattern 142 ("*memory element*") occupy. EX1003, ¶178. Thus, Park discloses "*a memory element formed i*n *a cavity of the first/second control gate.*"

As discussed in Section VI, to the extent that "*cavity*" requires a hole in the control gate layer to have a larger diameter than the holes in the layers above and below the control gate layer, Park's FIGs. 3 and 5 still disclose the "*cavity*." EX1003, ¶179.

Fig. 2

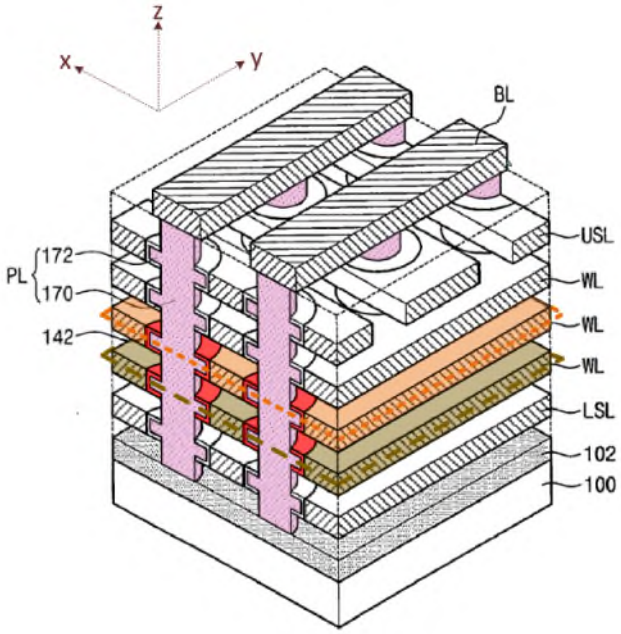
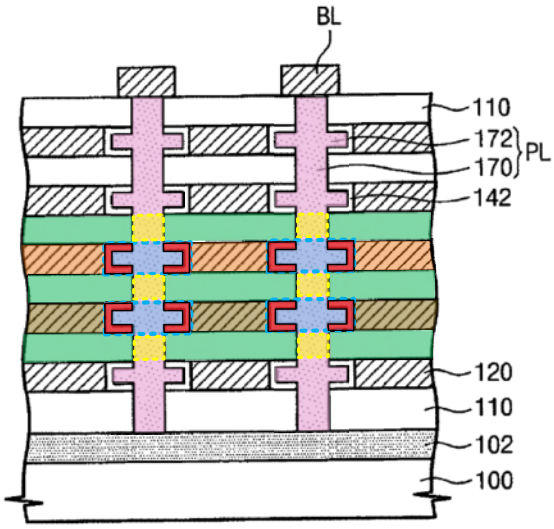


Fig. 3



EX1003 — FIG. U

As shown in annotated FIG. 3 above, a POSITA would have understood that the holes (in blue) in first and second conductive layers WL 120 (in brown and orange) have a larger diameter than the holes (in yellow) in interlayer insulating layers 110 (in green) above and below conductive layer WL 120. EX1005, [0052]; EX1003, ¶179. Specifically, Park discloses that "a diameter of a hole formed in the conductive layer 120 may be greater than a diameter of a hole formed in the interlayer insulating layer 110." EX1005, [0063]. Thus, Park discloses "*cavity*" under either party's construction.

Additionally, Park discloses that the memory cells in each xy plane/layer are arranged in an array form including multiple cells along the x-direction and y-

direction, respectively, as shown in FIG. 2 above, and thus, discloses that "*the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction*." EX1005, [0039], [0042]-[0043]; EX1003, ¶180.

Thus, Park discloses [8.c], [8.d.1], and [8.d.2].

4. Park discloses [8.e].

As shown in annotated FIGs. 2 and 3 below, Park further discloses "an impurity region 102 [(in purple)] (or a well) provided as a common source line" "to which the sources of the lower select transistors (LST) are commonly connected." EX1005, [0040], [0047]. EX1003, ¶182.

Fig. 2

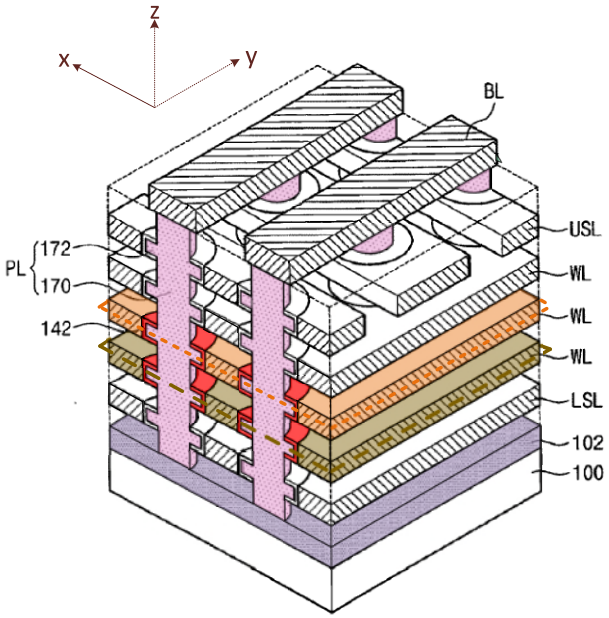
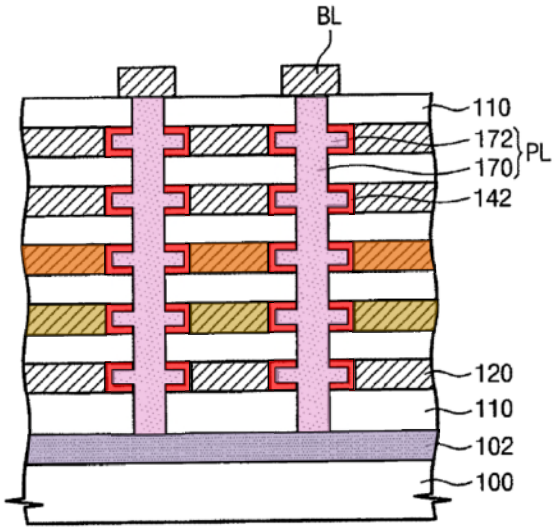


Fig. 3



EX1003 — FIG. V

A POSITA would have understood that impurity region 102 is a semiconductor common source because it is "formed in the semiconductor substrate 100" and connected to multiple active pillars PL/strings of memory cells. EX1005, [0047]; EX1003, ¶183.

5. Park in view of Mokhlesi renders obvious [8.f.1] and [8.f.2].

As shown in annotated FIGs. 2 and 3 below, Park discloses bit lines BL (in green, "*data lines*") electrically connected to impurity region 102 (in purple, "*common source*") and the first and second memory cells in the first and second layers (in brown and orange, "*first and second memory cells*") through active pillars PL (in pink). EX1005, [0047], [0050]-[0052], [0056]; EX1003, ¶185.

Fig. 2

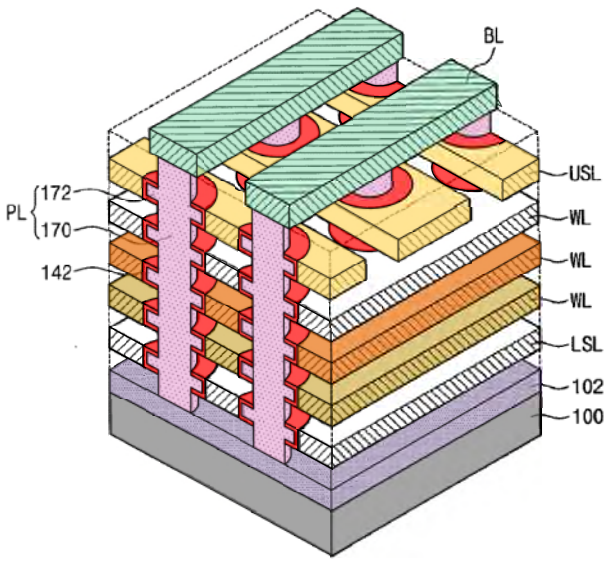
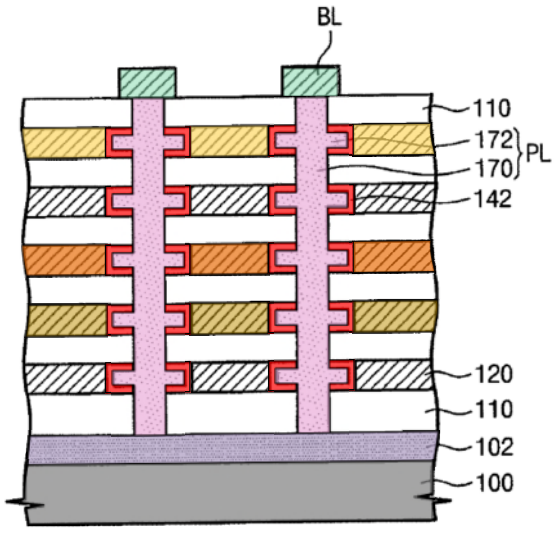


Fig. 3



EX1003 — FIG. W

Annotated FIGs. 2 and 3 above further illustrate that impurity region 102 is formed over semiconductor substrate 100 (in gray). EX1005, [0047]; EX1003, ¶194.

Park also discloses that "[e]ach string (STR) includes a plurality of memory cells (MC) serially connected to each other between an upper transistor (UST) and a lower transistor (LST). Drains of the upper select transistors (UST) are connected to the bit lines (BL1˜BL3) and sources of the lower select transistors (LST) are connected to the common source line (CSL)," "upper select transistors (UST) are connected to the upper select lines (USL1˜USL3) and the lower select transistors (LST) are connected to the lower select line (LSL)," and "bit lines (BL) cross the upper select lines (USL) and may be electrically connected to the active pillars (PL)." EX1005, [0040]-[0041], [0056]. As shown in the figures above, a POSITA would have understood that the electrical connections between bit lines BL (in green) and active pillars PL (in pink) are controlled by select transistors UST/LST, such that each string STR of memory cells along a respective active pillar PL can be selected/deselected by turning select transistors UST/LST on or off through select lines USL/LSL (in yellow/white hatched). EX1003, ¶187.

Therefore, Park discloses that bit lines BL are configured to be "*selectively*" coupled to impurity region 102 and the first and second memory cells in the first and second layers through active pillars PL. EX1003, ¶188.

Regarding active pillars PL, since Park discloses that it is formed of a

"polycrystalline semiconductor or a single crystalline semiconductor," a POSITA would have understood that active pillar PL having polycrystalline semiconductor (*e.g.*, polysilicon) includes "*a conductive material*," consistent with the '214 patent. EX1005, [0050], [0071]; EX1001, 8:64-67; EX1003, ¶190.

Further, since Park discloses that active pillar PL extends vertically through conductive layers, including first and second conductive layers WL 120, active pillar PL ("*conductive material*") also extends through the first and second memory cells in the first and second layers in the z-direction ("*a third direction*") perpendicular to the xy plane ("*first and second directions*") on which the first and second memory cells are formed. EX1005, [0042], [0052]; EX1003, ¶191.

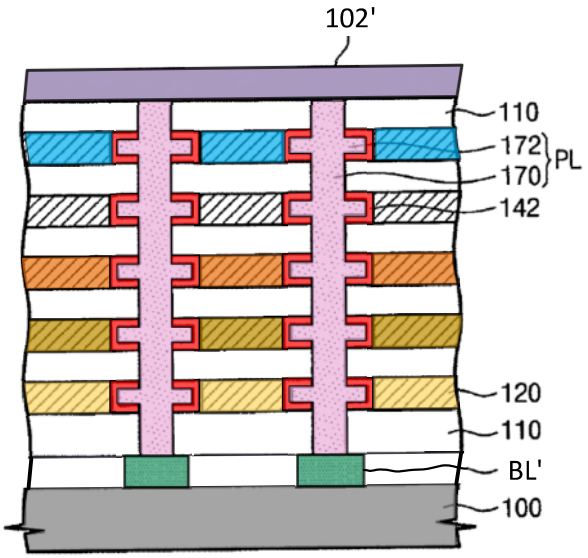
Thus, Park discloses [8.f.1].

Regarding [8.f.2], as discussed above in Section VIII.C, a POSITA would have found it obvious to modify Park's nonvolatile memory device shown in FIGs. 2 and 3 in view of Mokhlesi to form a metal/silicide common source at the top of the nonvolatile memory device. EX1003, ¶193.

For instance, as shown in FIG. X of Kuhn Decl. below, in the example modified nonvolatile memory device of Park in view of Mokhlesi, metal/silicide common source 102' (in purple) is formed over semiconductor substrate 100 (in gray), such that the first and second memory cells in the first and second layers as first and second conductive layers 120 (first and second word lines WL, in brown

and orange) are vertically between metal/silicide common source 102' and semiconductor substrate 100. EX1001, 5:30-38; EX1003, ¶¶194-195.

Fig. 3



EX1003 — FIG. X
(Annotated and Modified FIG. 3 of Park)

Thus, Park in view of Mokhlesi renders obvious [8.f.2].

From the foregoing, Park in view of Mokhlesi renders obvious claim 8.

E. Dependent Claim 13

Claim 13 includes all limitations of independent claim 9 from which it depends and further requires that "*the data line is located between the substrate and the first memory cell*."

Park discloses or otherwise renders obvious claim 9, as discussed below in detail.

1. Park discloses or suggests "[a]n apparatus comprising" [9.P], "*a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device*" [9.a], and "*a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level*" [9.b].

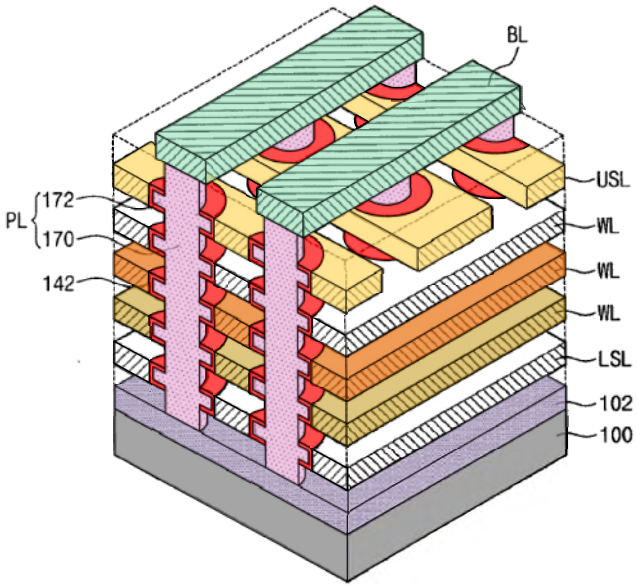
As discussed in Sections VIII.D.1-VIII.D.3, Park discloses "*an apparatus comprising,*" "*a plurality of first/second memory cells located in a first/second device level of a memory device*," and "*each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate*."

Since the first and second memory cells in the first and second layers discussed in Sections VIII.D.2- VIII.D.3 are in the **nonvolatile** memory device, Park also discloses a "*first non-volatile memory cell*" in the first memory cells and a "*second non-volatile memory cell*" in the second memory cells. EX1005, [0045]; EX1003, ¶200.

Park also discloses conformally forming charge storage layer 140 along a surface of second hole 136 by "sequentially depositing a charge blocking layer, a charge trapping layer and a charge tunneling layer." EX1005, [0064], FIGs. 5-6.

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Fig. 2



EX1003 — FIG. Y

Thus, as depicted in annotated FIG. 2 above, a POSITA would have understood, or at least found it obvious, that charge storage layer pattern 142 (in red) and the charge trapping layer therein ("*first/second memory element*") of each first and second memory cells has a "*ring shape*." EX1003, ¶¶201-203.

Accordingly, Park discloses or suggests [9.a] and [9.b].

2. Park discloses "*a conductive material extending through the first and second memory elements*" [9.c], and "*a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material*" [9.d].

As discussed in Sections VIII.D.4-VIII.D.5, Park discloses "*a common source*" and "*data lines configured to be selectively coupled to the common source and the*

first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions." Thus, Park also discloses [9.c] and [9.d].

From the foregoing, Park anticipates or otherwise renders obvious claim 9.

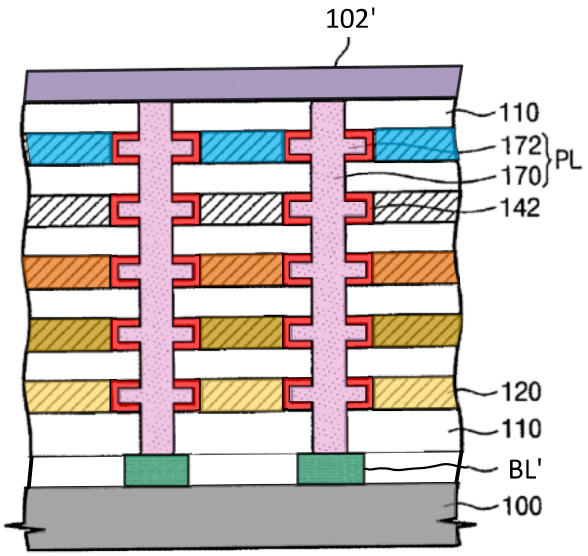
3. Park in view of Mokhlesi renders obvious that "*the data line is located between the substrate and the first memory cell*" [13].

As discussed above in Sections VIII.C and VIII.D.5, a POSITA would have found it obvious to modify Park's nonvolatile memory device shown in FIGs. 2 and 3 in view of Mokhlesi to form a metal/silicide common source at the top and bit lines BL at the bottom of the nonvolatile memory device. EX1003, ¶206.

For instance, as shown in FIG. Z of Kuhn Decl. below, in the example modified nonvolatile memory device of Park in view of Mokhlesi, modified bit line BL' (in green, "*data line*") is located vertically between semiconductor substrate 100 (in gray) and the first memory cell in the same first layer as first conductive layer WL 120 (in brown). EX1003, ¶207. Thus, Park in view of Mokhlesi renders obvious [13].

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Fig. 3



EX1003 — FIG. Z
(Annotated and Modified FIG. 3 of Park)

From the foregoing, Park in view of Mokhlesi renders obvious claim 13.

F. Independent Claim 21

1. Park discloses [21.P].

Park discloses [21.P], which is the same as [8.P]. *See* Section VIII.D.1.

2. Park discloses [21.a] and [21.b].

As discussed in Section VIII.D.3, Park discloses "*a first/second control gate formed in the first/second device level, …, wherein each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.*"

Park also discloses that "conductive layer 120 may be formed of a polysilicon layer or a metal layer." EX1005, [0060]. Thus, the metal or polysilicon first and

second conductive layers WL 120 are "*a first conductive material*" and "*a second conductive material*," respectively, consistent with the '214 patent. EX1001. 7:3-5, 39-42; EX1003, ¶¶211-212.

Park further discloses that "charge storage layer pattern 142 are in contact with sidewalls of the conductive layers (USL, WL, LSL)," and "charge storage layer 140 may be formed on … sidewalls of the conductive layers 120 … exposed by the second hole 136." EX1005, [0054], [0064]. Thus, Park also discloses that each hole ("*first/second cavity*") in first or second conductive layer WL 120 ("*first/second conductive material*") has a respective sidewall ("*a first/second sidewall*"). EX1003, ¶¶213-214.

Thus, Park discloses or suggests [21.a] and [21.b].

3. Park discloses or suggests [21.c], [21.d], [21.e], and [21.f].

As discussed in Section VIII.D.3, Park discloses that "*each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.*"

Park further discloses that charge storage layer pattern 142/charge storage layer 140 has an "ONO" structure—"charge storage layer 140 may be formed by **sequentially** depositing a charge blocking layer, a charge trapping layer and a charge tunneling layer. An oxide layer, a nitride layer and an oxide layer may be

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sequentially formed on a surface of the second hole 136." EX1005, [0064]; EX1003, ¶218. Park further discloses "charge storage layer pattern 142 is disposed between the protrusion 172 of the active pillar (PL) and a sidewall of each of the conductive layers (USL, WL, LSL)." EX1005, [0054]; EX1003, ¶219.

Accordingly, a POSITA would have understood, or at least found it obvious, that the nonvolatile memory device further includes a silicon oxide charge blocking layer ("*a first dielectric*") of charge storage layer pattern 142, which is formed on the sidewalls ("*first/second sidewalls*") of holes 136 ("*cavities*"). EX1005, FIGs. 3, 5; EX1003, ¶220. A POSITA would also have understood, or at least found it obvious, that the nonvolatile memory device further includes a silicon oxide charge tunneling layer ("*a second dielectric*") of charge storage layer pattern 142, which is formed on the sides of the corresponding charge trapping layers ("*first/second memory elements*"). EX1003, ¶221. A POSITA would have further understood, or at least found it obvious, that the respective charge trapping layer ("*first/second memory element*") is electrically isolated from the respective first or second conductive layer WL 120 ("*first/second conductive material*") by a respective portion of the silicon oxide charge blocking layer ("*a first/second portion of the first dielectric*") formed on the sidewalls. EX1003, ¶¶222-223.

Thus, Park discloses or suggests [21.c]-[21.f].

4. Park discloses or suggests [21.g].

Park further discloses that "through the active pillars (PL), a channel of string select transistors and memory cell transistors may be electrically connected," and that "a channel can be formed in the protrusion 172 when the nonvolatile memory device operates." EX1005, [0042], [0050], [0052]. Thus, a POSITA would have understood that protrusions 172 of active pillar PL function as "*conductive channel*" of a string STR of memory cells. EX1003, ¶224.

Since Park discloses "channels of the select transistors (UST, LST) and the memory cell transistors (MC) may be formed to be perpendicular to an xy plane," and "active pillars (PL) may penetrate the conductive layers (USL, WL, LSL)," a POSITA would have understood, or at least found it obvious, that the channel of active pillar PL extends from the first layer to the second layer ("*from the first device level to the second device level*") in which first and second conductive layers WL 120 are formed, respectively. EX1005, [0042], [0050]-[0052], EX1003, ¶226.

Since Park further discloses that "[a]n oxide layer, a nitride layer and an oxide layer may be sequentially formed on a surface of the second hole 136," and that "charge storage layer pattern 142 is disposed between the protrusion 172 of the active pillar (PL) and a sidewall of each of the conductive layers (USL, WL, LSL)," a POSITA would have understood that protrusions 172 of active pillar PL ("*conductive channel*") face the silicon nitride charge trapping layers ("*first and*

second memory elements"), but are electrically isolated from the silicon nitride charge trapping layers by a respective portion of the silicon oxide charge tunneling layer ("*a first/second portion of the second dielectric*"). EX1005, [0054], [0064]; EX1003, ¶228-230.

Therefore, Park discloses or suggests [21.g].

5. Park discloses [21.h].

Park discloses a semiconductor substrate 100. EX1005, [0047].

6. Park in view of Mokhlesi renders obvious [21.i].

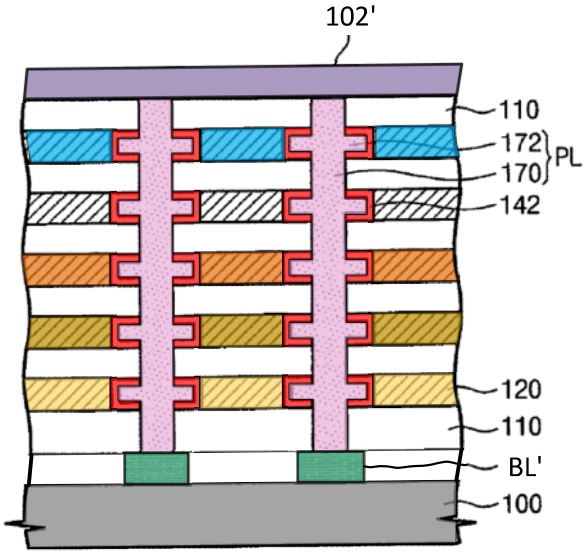
As discussed in Section VIII.D.5, a POSITA would have understood that the electrical connections between bit lines BL and active pillars PL are controlled by select transistors UST/LST, such that each string STR of memory cells along a respective active pillar PL can be selected/deselected by turning select transistors UST/LST on or off through select lines USLLST. EX1003, ¶233. Thus, Park discloses that bit line BL ("*data line*") is configured to be "*selectively*" coupled to active pillar PL, including protrusions 172 ("*conductive channel*"). EX1003, ¶234.

As discussed in Section VIII.C, a POSITA would have found it obvious to modify Park's nonvolatile memory device shown in FIGs. 2 and 3 in view of Mokhlesi to form a metal/silicide common source at the top and bit lines BL at the bottom of the nonvolatile memory device. EX1003, ¶235. For instance, as shown in FIG. AA of Kuhn Decl. below, in the example modified nonvolatile memory device

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of Park in view of Mokhlesi, modified bit line BL' (in green, "*data line*") is located vertically between the second conductive layer WL 120 (in orange, "*second conductive material*") and semiconductor substrate 100 (in gray). EX1003, ¶236. Thus, Park in view of Mokhlesi renders obvious [21.i].

Fig. 3



EX1003 — FIG. AA
(Annotated and Modified FIG. 3 of Park)

From the foregoing, Park in view of Mokhlesi renders obvious claim 21.

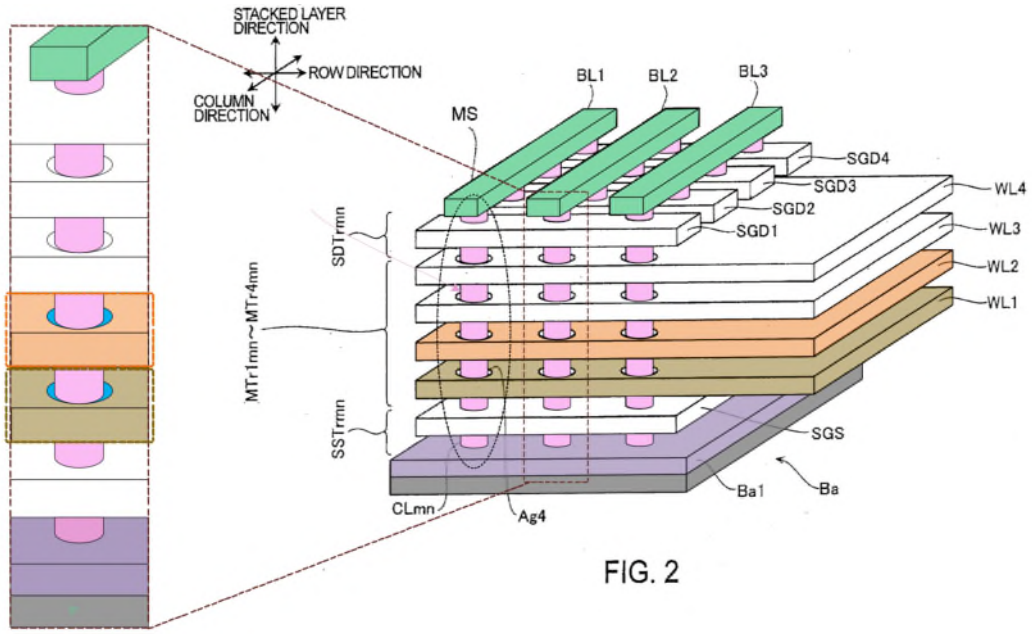
IX. GROUND 4: FUKUZUMI IN VIEW OF MOKHLESI RENDERS OBVIOUS CLAIMS 8 AND 21

A. Overview of Fukuzumi

Fukuzumi relates to nonvolatile semiconductor memory devices. EX1007, [0002]. Fukuzumi aims to overcome problems encountered in transferring

semiconductor memory devices from 2D to 3D. EX1007, [0003], [0040].

Annotated FIG. 2 below shows a perspective view of a nonvolatile semiconductor memory device 100 in the first embodiment of Fukuzumi. EX1007, [0078]; EX1003, ¶88.



EX1003 — FIG. F

As shown in annotated FIG. 2 above, Fukuzumi's nonvolatile semiconductor memory device includes a matrix of memory strings MS including memory cells MTr1*mn*-MTr4*mn*, where *m* and *n* indicate the memory cells' X- and Y-coordinates. EX1007, [0079]; EX1003, ¶89. Each memory string MS includes columnar semiconductor CL*mn* (in pink) extending through source-side selection gate lines SGS, word lines WL (in brown and orange), and drain-side selection gate lines SGD. EX1007, [0079]-[0082]; EX1003, ¶89. Columnar semiconductors CL*mn* connect bit

lines BL (in green) on the top and a p-well region Ba1 (in purple) on the bottom along the stacked layer (vertical) direction. EX1007, [0086]; EX1003, ¶89.

Since Fukuzumi discloses "[e]ach of the memory strings MS includes columnar semiconductors CL*mn* on a p-well region Ba1 formed in an n+ region of a semiconductor substrate Ba" and "source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba," p-well region Ba1 is a semiconductor common source of multiple memory strings MS. EX1007, [0081], [0086]; EX1003, ¶91.

Memory cells MTr1*mn*-MTr4*mn* include portions of word lines WL connected to each gate of the memory cells and the charge storage layer formed on the sidewalls of word lines WL in the memory holes (in blue). EX1007, [0080], [0085], [0087]; EX1003, ¶90.

B. Reasons to Combine Fukuzumi and Mokhlesi

A POSITA would have found it obvious to modify Fukuzumi's 3D memory device and fabrication method thereof in view of Mokhlesi's teaching of forming common source at the top and bit lines at the bottom of a 3D memory device for various reasons discussed below in detail. EX1003, ¶238.

1. The teaching, suggestion, and motivation in Fukuzumi and Mokhlesi would have led a POSITA to rearrange Fukuzumi's common source to the top with a metal/silicide material.

Fukuzumi aims to overcome problems encountered in transferring semiconductor memory devices from 2D to 3D. EX1007, [0003], [0040]. Fukuzumi discloses using a p-well region Ba1 formed in an n+ region of a semiconductor substrate Ba as the semiconductor common source. EX1007, [0081], [0086].

Since Fukuzumi's common source is also made of a semiconductor material, it suffers from the exact problem identified by Mokhlesi—"current crowding," which can cause reliability issues to Fukuzumi's 3D memory device, including localized overheating, formation of thermal hotspots, aggravated electromigration effects, and formation of voids. EX1006, [0092]; EX1003, ¶¶240-243. The problem becomes particularly pronounced when transitioning memory devices from 2D to 3D configurations. EX1003, ¶241.

Naturally, a POSITA would have been motivated to adopt Mokhlesi's solution to this problem—"source lines may be formed on top and the bit lines may be formed on the bottom" and "formation of metal and/or silicide rather than semiconductor source lines"—to Fukuzumi's 3D memory device. EX1006, [0092]; EX1003, ¶241. Doing so would "lead[] to a decreased current crowding due to the lower resistivity source line material," as explained by Mokhlesi. EX1006, [0092]; EX1003, ¶243.

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The decreased current crowding in the metal/silicide common source at the top of Fukuzumi's modified memory device would have advanced Fukuzumi's goal of overcoming problems encountered in transferring semiconductor memory devices from 2D to 3D. EX1003, ¶244.

As discussed above in Section VIII.C.1, Mokhlesi's teaching regarding source lines applies equally to a common source region. EX1006, [0094]; EX1003, ¶245. A POSITA would have found it obvious to apply Mokhlesi's teaching regarding source lines to Fukuzumi's common source (p-well region Ba1) because Mokhlesi explains that "common source plate provides a higher current sinking capability at the expense of loosing[sic] the ability to select individual source line voltage." EX1006, [0017], [0094]; EX1003, ¶246. Fukuzumi's design can well accommodate it since in Fukuzumi's memory device, the sources of all memory strings MS are commonly connected to p-well region Ba1, making it indifferent to the ability to select individual source line voltage. EX1007, [0081]; EX1003, ¶246.

2. The proposed modification is merely applying Mokhlesi's known technique of forming a metal/silicide common source at the top of Fukuzumi's 3D memory device ready for improvement to yield predictable results.

As discussed in Section VIII.C.2, it was well-known to a POSITA that metals/silicides have significantly improved resistivity compared to semiconductors, as well as that people have proposed approaches similar to Mokhlesi's—forming

common source at the top of 3D NAND memory devices to enable the use of low-resistivity metal materials. EX1003, ¶¶248-249. The industry recognized the expected technical effect of reduced source resistance and the resulting performance improvement. EX1003, ¶249.

Therefore, a POSITA would have found it obvious to enhance the performance and reliability of Fukuzumi's memory device by replacing its semiconductor common source with a metal/silicide common source. EX1003, ¶¶250-251.

3. A POSITA would have a reasonable expectation of success in forming metal/silicide common source at the top of Fukuzumi's 3D memory device.

A POSITA would have a reasonable expectation of success for the proposed combination of Fukuzumi and Mokhlesi. EX1003, ¶252. Mokhlesi's technique of forming metal/silicide common source at the top of a 3D memory device is directly applicable to Fukuzumi's 3D memory device because of the similarities between their devices, such as memory cells arranged in multiple levels in a 3D arrangement in the forms of NAND memory strings, "ONO" structure of memory cells, and selection transistors in each NAND memory string above and/or below the memory cells. EX1003, ¶252; Sections VIII.B, IX.A.

Moreover, it would have been well within a POSITA's capabilities to form a metal/silicide common source above word lines WL in Fukuzumi's 3D memory

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device without undue burden and with a reasonable expectation of success. EX1003, ¶254. Following Mokhlesi's specific guidance, along with common knowledge in the art, a POSITA could easily modify Fukuzumi's memory device and fabrication process thereof to create a device where a metal/silicide common source is positioned at the top of the memory device, replacing the semiconductor common source previously located at the bottom. EX1003, ¶254.

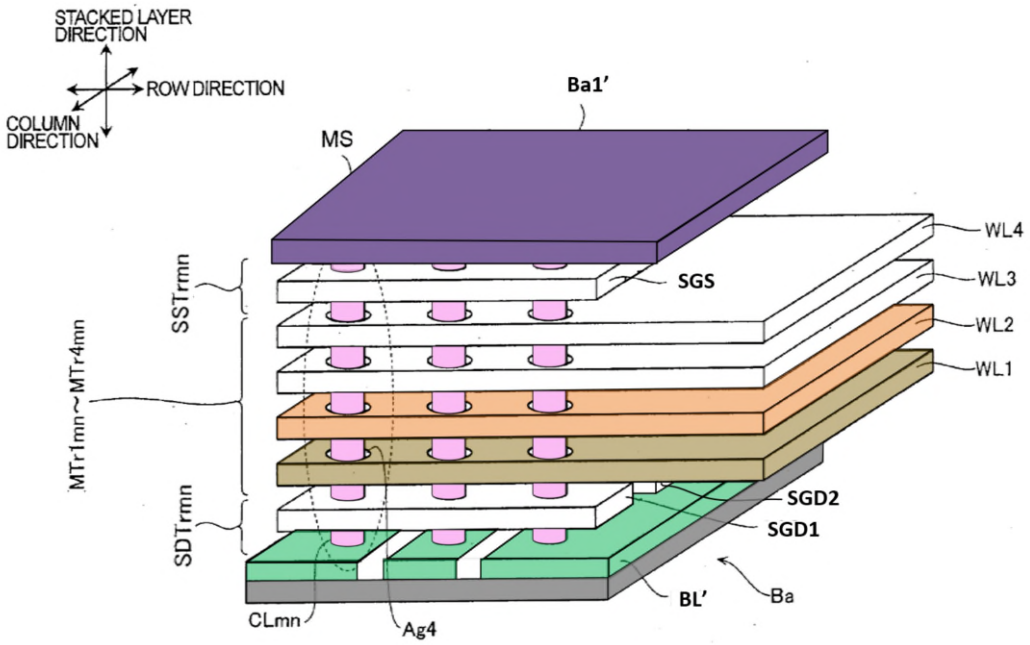


FIG. 2

EX1003 — FIG. AB
(Annotated and Modified FIG. 2 of Fukuzumi)

In a non-limiting example, as depicted in modified and annotated FIG. 2 of Fukuzumi above, modified bit lines BL' (in green) are formed over semiconductor substrate Ba (in gray), drain-side selection transistors and lines SDTr*mn* and SGD are formed over modified bit lines BL', word lines WL (in brown and orange) are

formed over drain-side selection transistors and lines SDTr*mn* and SGD, source-side selection transistors and lines SSTr*mn* and SGS are formed over word lines WL, and a metal/silicide common source Ba1' (in purple) is formed over source-side selection transistors and lines SSTr*mn* and SGS. EX1003, ¶255.

The modification would neither impair the functionality of Fukuzumi's 3D memory device nor complicate its manufacturing process. EX1003, ¶¶256-257.

C. Independent Claim 8

1. Fukuzumi discloses [8.P].

Fukuzumi discloses a nonvolatile semiconductor memory device ("*apparatus*")[4]. EX1007, [0073]. Thus, Fukuzumi discloses [8.P].

2. Fukuzumi discloses [8.a] and [8.b].

Fukuzumi discloses that nonvolatile semiconductor memory device 100[5] includes memory cell strings MS each including memory cells MTr1*mn*-MTr4*mn* vertically and serially connected to each other. EX1007, [0079]-[0080], [0085].

As shown in annotated FIG. 2 below, first memory cells MTr1*mn* (in brown

[4] Unless otherwise specified, Fukuzumi's disclosures are applicable to the combination of Fukuzumi and Mokhlesi used for mapping in Ground 4. EX1003, ¶¶257-258.

[5] Although Fukuzumi describes nonvolatile semiconductor memory device 100 and its accompanying figures, including FIG. 2 cited in Ground 4, in the context of the first embodiment, unless otherwise specified, the disclosures regrading nonvolatile semiconductor memory device 100 are equally applicable to the second embodiment as well. EX1007, [0146]-[0148]; EX1003, ¶259.

dashed box, "*a plurality of first memory cells*") are located in a first level of nonvolatile semiconductor memory device 100, and second memory cells MTr2*mn* (in orange dashed box, "*a plurality of second memory cells*") are located in a second level. EX1007, [0077], [0081]; EX1003, ¶260.

Thus, Fukuzumi discloses [8.a] and [8.b].

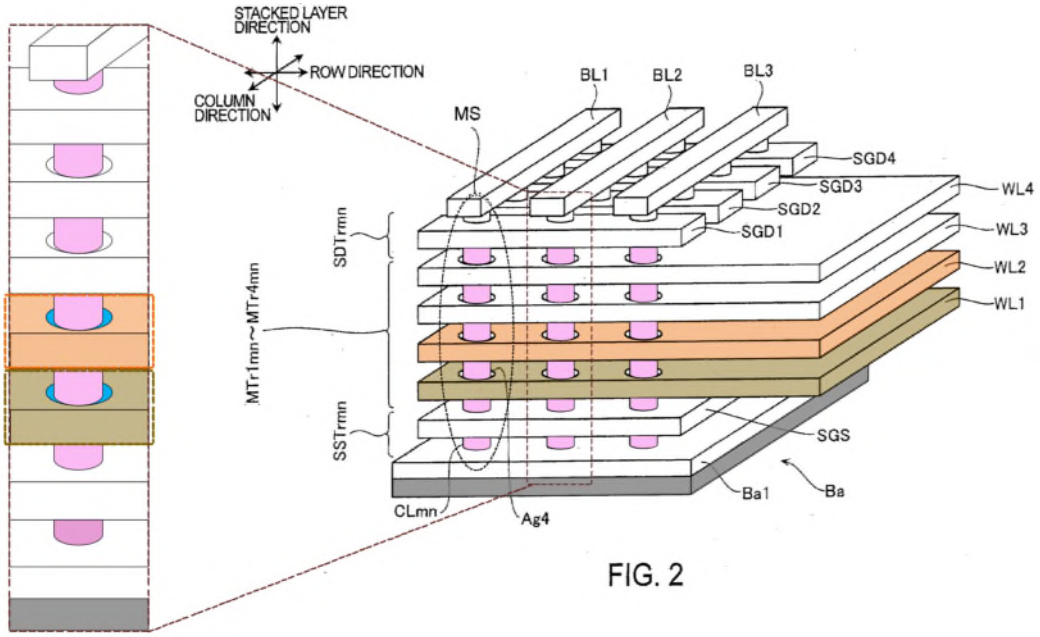


FIG. 2

EX1003 — FIG. AC

3. Fukuzumi discloses [8.c], [8.d.1], and [8.d.2].

Fukuzumi discloses that nonvolatile semiconductor memory device 100 also includes vertically stacked word lines WL1-WL4 (*e.g.*, first-fourth word line conduction layers 36*a*-36*d* in the first embodiment, or 361*a*-361*d* in the second embodiment). EX1007, [0101], [0148]. Each word line WL has a plane structure extending two-dimensionally and is connected to the gate of a respective layer of

memory cells MTr1*mn*-MTr4*mn* in each memory string MS, with its end portion acting as the control gate of the respective memory cell. EX1007, [0077], [0080], [0087], [0101], [0148]. Fukuzumi also discloses that "word line driving circuit 13 controls voltage applied to a word line WL" and has "a function as control circuits controlling the memory strings MS." EX1007, [0076], [0090].

Thus, as shown in annotated FIGs. 2 and 28 below, Fukuzumi discloses that a first word line WL1 (in brown, *e.g.*, first word line conduction layer 361*a*) in the first device level ("*a first control gate formed in the first device level*") to control access to first memory cells MTr1*mn* in the first device level, and a second word line WL2 (in orange, *e.g.*, second word line conduction layer 361*b*) in the second device level ("*a second control gate formed in the second device level*") to control access to second memory cells MTr2*mn* in the second device level. EX1003, ¶264.

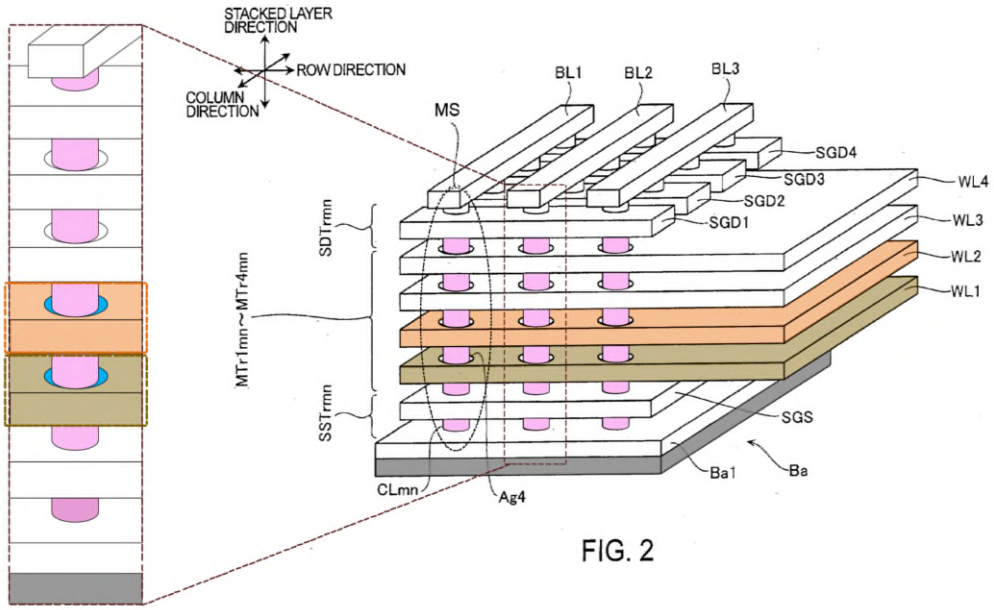


FIG. 2

EX1003 — FIG. AD

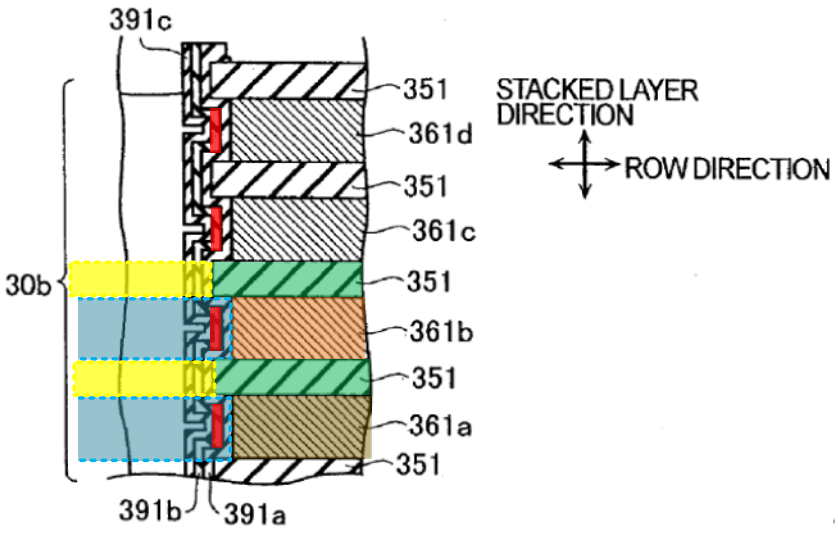


FIG. 28

EX1003 — FIG. AE

Further, Fukuzumi discloses that each memory cell MTr1*mn* or MTr2*mn* includes a charge storage layer 39*b*/391*b*[6], formed of silicon nitride, where memory 38 performs data writing and reading. EX1007, [0114], [0148], [0151]. Thus, a POSITA would have understood that charge storage layer 391*b* is "*a memory element*." EX1003, ¶265.

Since Fukuzumi also discloses charge storage layer 39*b*/391*b* being formed in memory hole 37 (*see* FIG. 4) passing through word line conduction layers 36*a*/361*a*-

[6] Although Fukuzumi discloses the material and function of charge storage layer with respect to "39b" in the first embodiment, a POSITA would have understood that the same disclosures are equally applicable to "391b" in the second embodiment as well. EX1007, [0146]; EX1003, ¶265.

36*d*/361*d*, as shown in FIG. 28 above, Fukuzumi discloses that charge storage layer 391*b* (in red) is formed in memory hole 37 (in blue, "*a cavity of the first/second control gate*"). EX1007, [0103]-[0104], [0148]; EX1003, ¶266.

As discussed in Section VI, to the extent that "*cavity*" requires a hole in the control gate to have a larger diameter than the holes in the layers above and below the control gate, memory hole 37 still qualifies as "*cavity*" as Fukuzumi specifically discloses that charge storage layers 391*b* "are formed as the concavo-convex shape accompanying with the first-fourth word line conduction layer 361*a*-361*d*," and that "sidewall of first-fourth word line conduction layers 361*a*-361*d* faced to the fourth space Ag4 are formed as recesses corresponding to a side wall of an interlayer insulator 351." EX1007, [0148], [0151].

Thus, a POSITA would have understood, as illustrated in annotated FIG. 28 below, memory hole 37 (in blue) in each of word line conduction layers 361*a* and 361*b* (in brown and orange) has a diameter larger than memory holes 37 (in yellow) in interlayer insulators 351 (in green) above and below the respective word line conduction layer 361*a* or 361*b*. EX1003, ¶267. Thus, Fukuzumi discloses "*cavity*" under either party's construction.

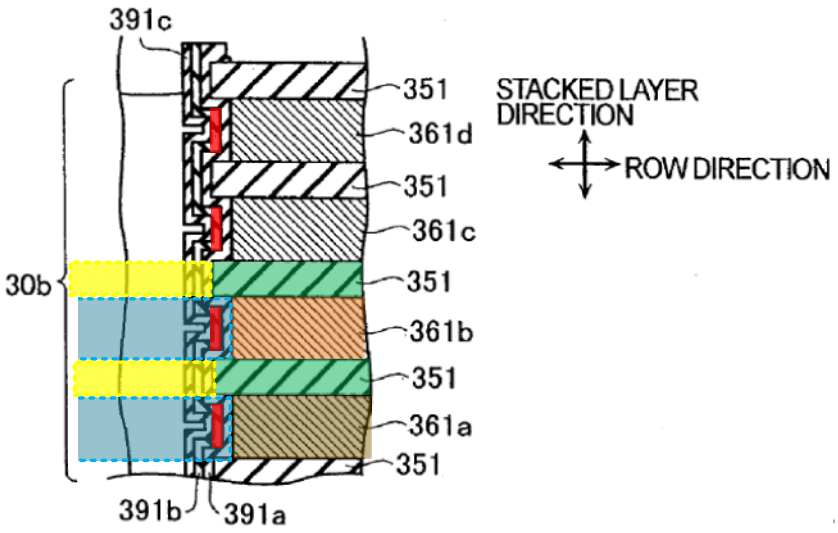


FIG. 28

EX1003 — FIG. AE

Accordingly, Fukuzumi discloses [8.c] and [8.d.1].

Regarding [8.d.2], Fukuzumi further discloses that "memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CL*mn*." EX1007, [0081]. Since Fukuzumi also discloses "memory strings MS being constituted with memory cells MTr1*mn*-MTr4*mn*," memory cells MTr1*mn*-MTr4*mn* are also arranged in a matrix ("*in a first direction*" and "*a second direction*"). EX1007, [0081]; EX1003, ¶270.

4. Fukuzumi discloses [8.e].

Since Fukuzumi discloses "**[e]ach** of the memory strings MS includes columnar semiconductors CL*mn* on a p-well region Ba1 formed in an n+ region of

a semiconductor substrate Ba," and "source means the n+-region formed in the p-well region Ba1 of the semiconductor substrate Ba," p-well region Ba1 is a "*common source*" of multiple memory strings MS. EX1007, [0081], [0086]; EX1003, ¶¶272-273. Thus, Fukuzumi discloses [8.e].

5. Fukuzumi in view of Mokhlesi renders obvious [8.f.1] and [8.f.2].

As shown in annotated FIG. 2 below, Fukuzumi discloses bit lines BL (in green, "*data lines*") electrically connected to p-well region Ba1 (in purple, "*common source*") and memory cells Mtr*mn* through columnar semiconductors CL*mn* (in pink). EX1007, [0081], [0109]; EX1003, ¶275. FIG. 2 below further illustrates that p-well region Ba1 is formed over semiconductor substrate Ba (in gray). EX1007, [0081], [0086]; EX1003, ¶281.

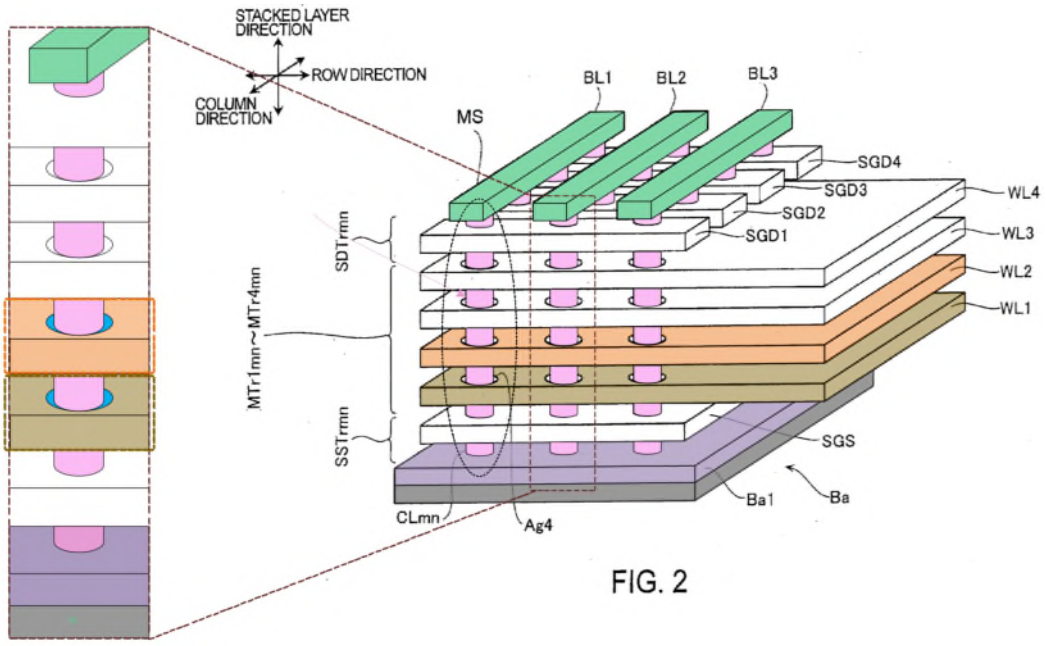


FIG. 2

EX1003 — FIG. AF

Fukuzumi also discloses bit lines BL being electrically connected to columnar semiconductors CL*mn* via selection transistors SDTr*mn*/SSTr*mn*, which include selection gate lines SGD/SGS electrically connected and controlled by selection gate line SGD/SGS driving circuit 14/15. EX1007, [0076], [0082]-[0083], [0085], [0088]-[0089]; EX1003, ¶276. A POSITA would have understood that bit lines BL are coupled with memory cells Mtr*mn* and p-well region Ba1 through selection transistors SDTr*mn*/SSTr*mn*, and that selection gate line SGD/SGS driving circuit 14/15 selects/deselects each memory string MS by turning selection transistors SDTr*mn*/SSTr*mn* on or off to control the connections between bit lines BL and memory cells Mtr*mn*, through selection gate lines SGD/SGS. EX1007, [0076]; EX1003, ¶276. Therefore, Fukuzumi discloses that bit lines BL are configured to be "*selectively*" coupled to memory cells Mtr*mn* and p-well region Ba1 through columnar semiconductors CL*mn*. EX1003, ¶276.

Further, Fukuzumi discloses that memory 38, which is part of columnar semiconductor CL*mn* in the first and second embodiments, is formed of silicon. EX1007, [0103]. Thus, a POSITA would have understood that columnar semiconductor CL*mn* having silicon includes a "*conductive material*," consistent with the '214 patent. EX1001, 8:64-67; EX1003, ¶277.

As Fukuzumi further discloses that columnar semiconductor CL*mn* extends vertically through word lines WL1-WL4, including first and second word lines WL1

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and WL2 in the first and second levels, columnar semiconductor CL*mn* ("*conductive material*") also extends through first and second memory cells MTr1*mn* and MTr2*mn* in the first and second device levels in the vertical direction ("*a third direction*") perpendicular to the matrix plane ("*the first and second directions*") on which memory cells MTr*mn* are formed. EX1007, [0081]; EX1003, ¶278.

Thus, Fukuzumi alone discloses [8.f.1].

Regarding [8.f.2], as discussed above in Section IX.B, a POSITA would have found it obvious to modify Fukuzumi's nonvolatile memory device shown in FIG. 2 in view of Mokhlesi to form a metal/silicide common source at the top of the nonvolatile memory device. EX1003, ¶280.

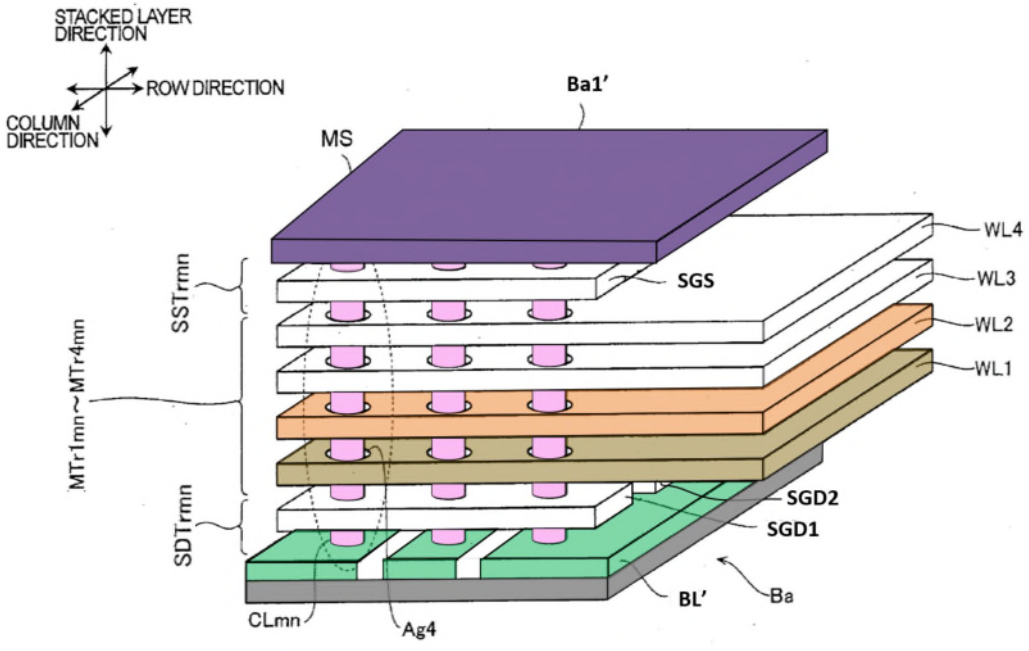


FIG. 2

EX1003 — FIG. AG
(Annotated and Modified FIG. 2 of Fukuzumi)

For instance, as shown in FIG. AG of Kuhn Decl. above, in the example modified nonvolatile memory device of Fukuzumi in view of Mokhlesi, a metal/silicide common source Ba1' (in purple) is formed over semiconductor substrate Ba (in gray), such that first and second memory cells MTr1*mn* and MTr2*mn* ("*first and second memory cells*") in the same first and second device levels as the first and second word lines WL (in brown and orange) are disposed vertically between metal/silicide common source Ba1' and semiconductor substrate Ba. EX1003, ¶¶281-283. Thus, Fukuzumi in view of Mokhlesi renders obvious [8.f.2].

From the foregoing, Fukuzumi in view of Mokhlesi renders obvious claim 8.

D. Independent Claim 21

1. Fukuzumi discloses [21.P].

Fukuzumi discloses [21.P], which is the same as [8.P]. Section IX.C.1.

2. Fukuzumi discloses [21.a] and [21.b].

As discussed in Section IX.C.3, Fukuzumi discloses "*a first/second control gate formed in the first/second device level,*" and "*a cavity of the first/second control gate.*"

Fukuzumi discloses that "[e]ach of the word lines WL1-WL4 is connected to each gate of the memory cells MTr1*mn*-MTr4*mn* in each of the memory strings MS and each of the word lines WL1-WL4 are formed of the same **conductive layer** and are common in plane each other." EX1007, [0080]. As examples of word lines WL1-

WL4, first and second word line conduction layers 361*a* and 361*b* are thus "*first and second conductive materials,*" consistent with the '214 patent. EX1001, 7:3-5, 39-42; EX1003, ¶288.

As shown in annotated FIGs. 2 and 28 below, a POSITA would have understood that each portion of memory hole 37 (in blue, "*first/second cavity*") in which charge storage layer 311*b* (in red, "*first/second memory element*") is formed has a respective sidewall ("*a first/second sidewall*") under either party's interpretation of "*cavity*." EX1003, ¶289; Section IX.C.3.

Thus, Fukuzumi discloses [21.a] and [21.b].

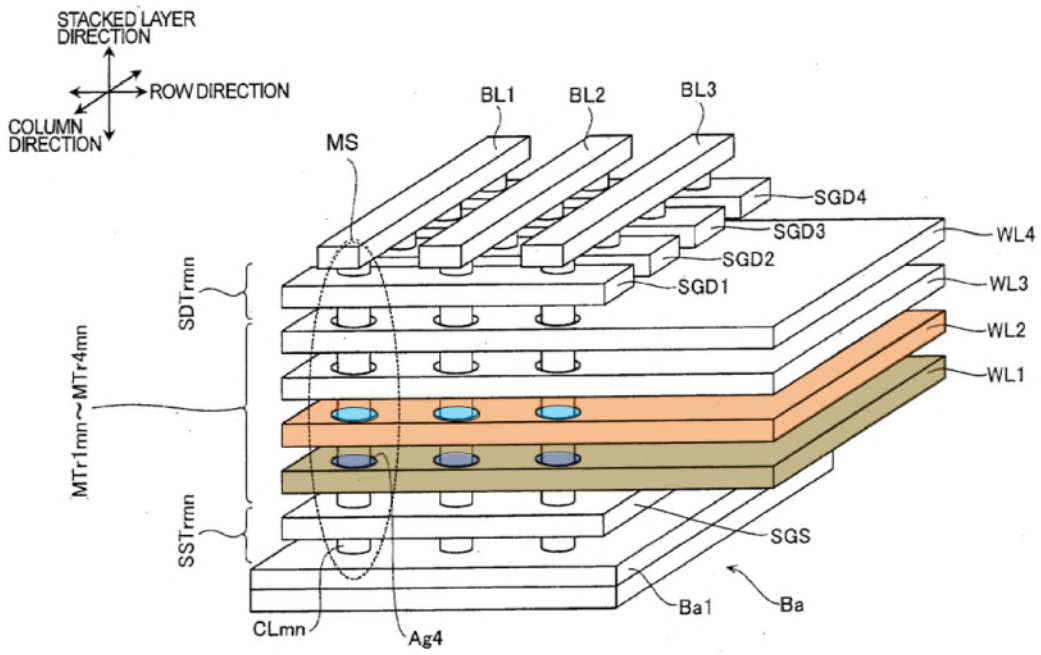


FIG. 2

EX1003 — FIG. AH

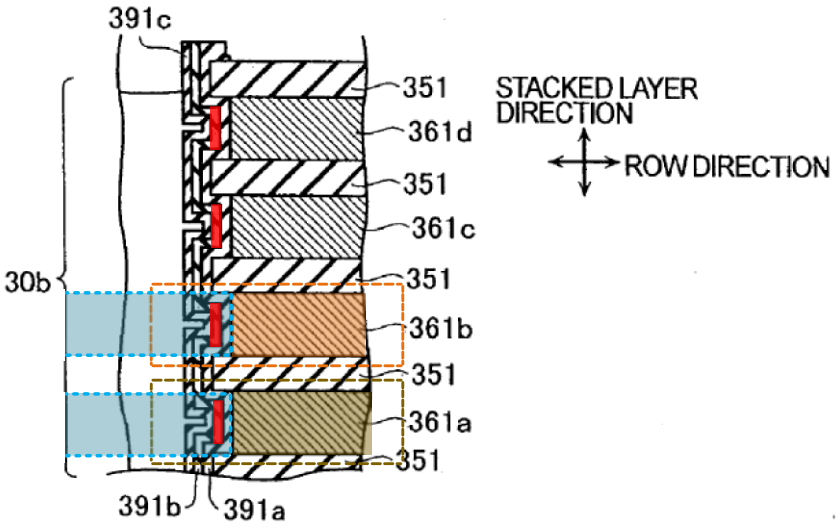


FIG. 28

EX1003 — FIG. AI

3. Fukuzumi discloses [21.c], [21.d], [21.e], and [21.f].

As discussed in Section IX.C.3, Fukuzumi discloses that "*each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.*"

Fukuzumi discloses that "[e]ach of the memory cells Mtr*mn* includes the columnar semiconductor CL*mn*, the insulation layer surrounding the columnar semiconductor CL*mn* via the space Ag4 as shown in FIG. 2, a charge storage layer (not illustrated in FIG. 2 and FIG. 3) and the word line WL surrounding the insulation layer and the charge storage layer." EX1007, [0087]. As examples of the insulation layer and charge storage layer surrounding columnar semiconductor CL*mn* and surrounded by the word line WL, Fukuzumi specifically discloses "surfaces of a block insulation layer 391*a*, a charge storage layer 391*b* and a tunnel insulation layer 391*c* faced to the fourth space Ag4." EX1007, [0148].

Thus, as shown in annotated FIG. 28 below, Fukuzumi discloses block insulation layer 391*a* (in yellow, "*first dielectric*") formed on the sidewalls of memory hole 37 (in blue, "*first/second cavity*"), and tunneling insulation layer 391*c* (in green, "*second dielectric*") formed on the sides of charge storage layers 391*b* (in red, "*first/second elements*"). EX1003, ¶293; Section VII.J.

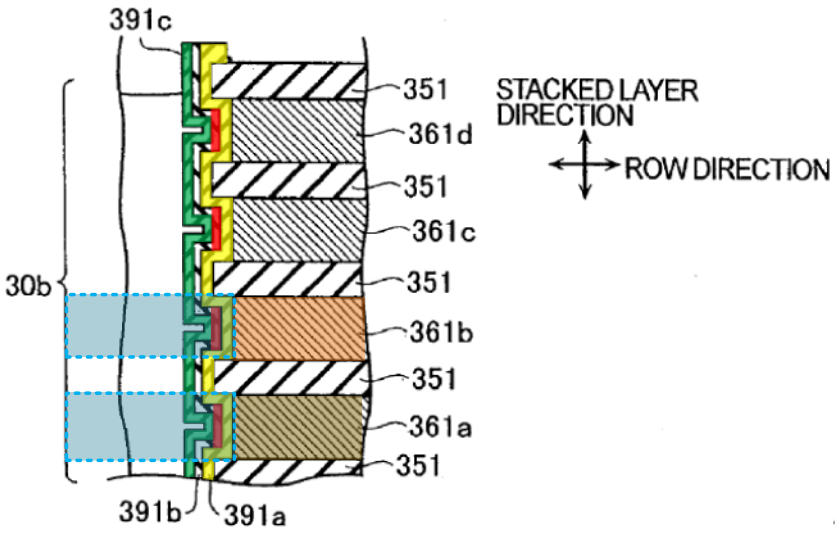


FIG. 28

EX1003 — FIG. AJ

A POSITA would have understood, or at least found it obvious, that charge storage layer 391*b* is electrically isolated from the respective first or second word line conduction layer 361*a* or 361*b* (in brown or orange, "*first/second conductive material*") by a respective portion of block insulation layer 391*a* (in yellow, "*a first/second portion of the first dielectric*"). EX1003, ¶294.

Therefore, Fukuzumi discloses [21.c]-[21.f].

4. Fukuzumi discloses or suggests [21.g].

Fukuzumi discloses each memory string MS includes columnar semiconductor CL*mn*, and the source and drain of the memory string MS are formed in columnar semiconductor CL*mn*. EX1007, [0081], [0085], [0087]. Regarding

memory 38, which is part of columnar semiconductor CL*mn* in the first and second embodiments, Fukuzumi discloses that "when the fourth word line conduction layer 36*d* is applied to voltage, the memory 38 is performed to write in data into the approached portion of the charge storage layer 39*b* and read out data from the approached portion of the charge storage layer 39*b*." EX1007, [0114].

A POSITA would have understood that, during certain operations of Fukuzumi's memory device, a channel of memory string MS forms in the vertical outermost layer of columnar semiconductor CL*mn* and does not extend throughout the entire columnar semiconductor CL*mn*. EX1017, [0063], [0070], FIG. 11; EX1003, ¶¶297-298. Thus, Fukuzumi discloses "*a conductive channel*."

Fukuzumi further discloses that columnar semiconductor CL*mn* extends vertically through word lines, including first and second word lines WL in the first and second device levels. EX1007, [0081], FIG. 2. Thus, Fukuzumi discloses that columnar semiconductor CL*mn*, including its vertical outermost layer ("*conductive channel*"), extends from the first device level to the second device level. EX1003, ¶299.

As discussed in Section IX.D.3 and further shown in the annotated FIG. 28 below, a POSITA would have understood, or at least found it obvious, that tunneling insulation layer 391*c* (in green, "*second dielectric*") is formed laterally between charge storage layers 391*b* (in red, "*first/second memory elements*") and the vertical

outermost layer of columnar semiconductor CL*mn* (in black, "*conductive channel*"), such that the vertical outermost layer of columnar semiconductor CL*mn* faces charge storage layers 391*b*, but is electrically isolated from charge storage layers 391*b* by tunneling insulation layer 391*c* ("*a respective portion of the second dielectric*"). EX1003, ¶300.

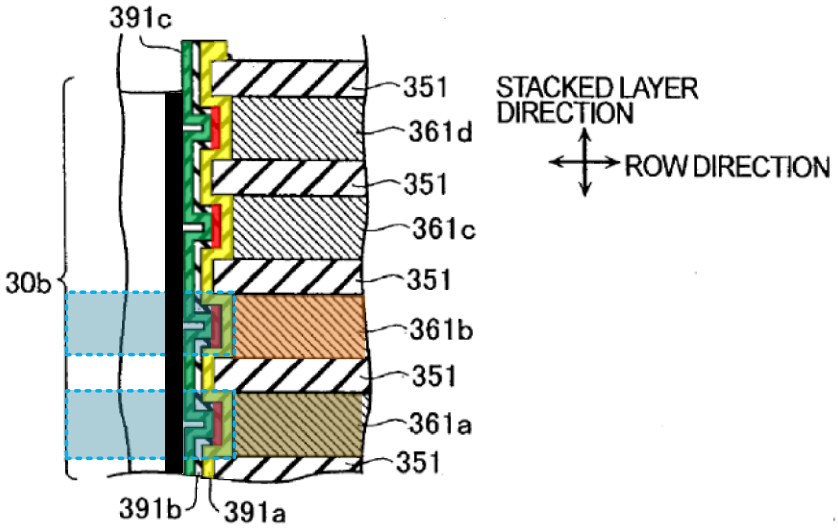


FIG. 28

EX1003 — FIG. AK

Thus, Fukuzumi discloses or suggests [21.g].

5. Fukuzumi discloses [21.h].

Fukuzumi discloses a semiconductor substrate Ba. EX1007, [0081].

6. Fukuzumi in view of Mokhlesi renders obvious [21.i].

As discussed in Section IX.C.5, a POSITA would have understood that the

electrical connections between bit lines BL and columnar semiconductors CL*mn* are controlled by selection transistors SDTr*mn*/SSTr*mn*, such that each memory string MS can be selected/deselected by turning selection transistors SDTr*mn*/SSTr*mn* on or off through selection gate lines SGD/SGS. EX1003, ¶303. Thus, a POSITA would have understood that Fukuzumi discloses that bit line BL ("*data line*") is configured to be "*selectively*" coupled to columnar semiconductor CL*mn*, including its vertical outermost layer ("*conductive channel*"). EX1003, ¶304.

As discussed in Sections IX.B, a POSITA would have found it obvious to modify Fukuzumi's nonvolatile memory device shown in FIG. 2 in view of Mokhlesi to form a metal/silicide common source at the top and bit lines BL at the bottom of the nonvolatile memory device. EX1003, ¶305.

For instance, as shown in FIG. AL of Kuhn Decl. below, in the example modified nonvolatile memory device of Fukuzumi's in view of Mokhlesi, modified bit line BL' (in green, "*data line*") is located vertically between second word line WL2 (in orange, "*second conductive material*") and semiconductor substrate Ba (in gray). EX1003, ¶306.

Thus, Fukuzumi in view of Mokhlesi renders obvious [21.i].

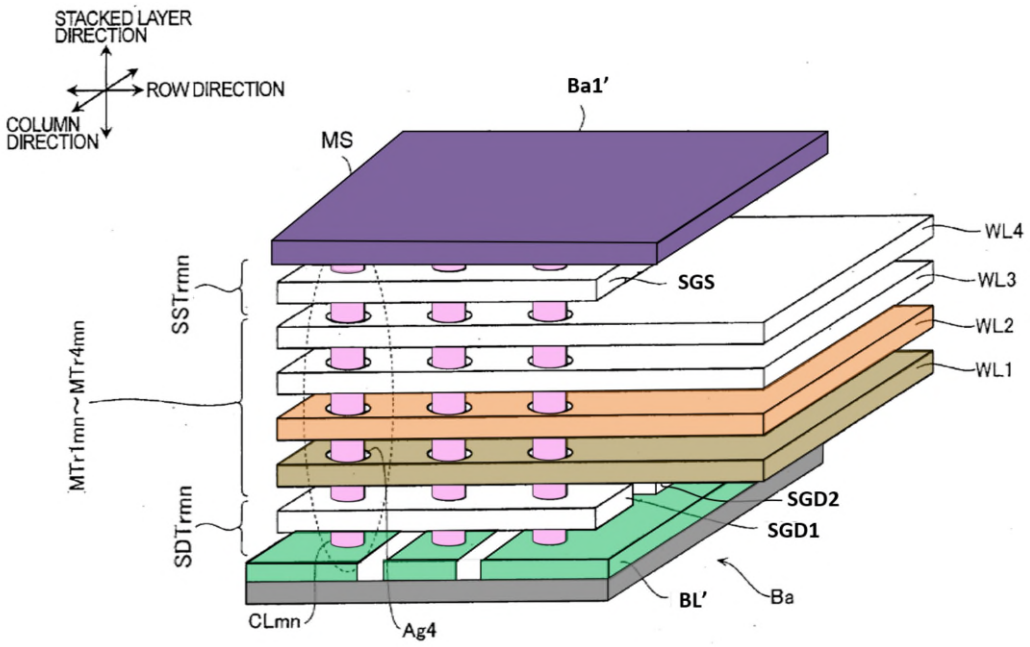


FIG. 2

EX1003 — FIG. AL
(Annotated and Modified FIG. 2 of Fukuzumi)

From the foregoing, Fukuzumi in view of Mokhlesi renders obvious claim 21.

X. DISCRETION DENIAL DOES NOT APPLY

A. 35 U.S.C. § 325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion to deny institution under 35 U.S.C. § 325(d).

Lung, Park, Mokhlesi, and Fukuzumi have never been presented or otherwise considered by the Office during the original examination of the '214 patent. *See generally* EX1002. None of the grounds raised in this Petition have ever been presented, much less discussed, during the original examination. The disclosures

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considered by the Examiner in the original examination are not substantially similar to those of the references relied upon in this Petition.

Even if any of Lung, Park, Mokhlesi, and Fukuzumi, or arguments in this Petition, were considered substantially the same as those raised during the prosecution of the '214 patent, the Examiner erred in a manner material to the patentability of the challenged claims by not rejecting the challenged claims over the prior art and arguments presented herein. For instance, the alleged allowable subject matter with respect to issued independent claims 8 and 21 (Section V.B), *e.g.*, forming a common source above data lines and the resulting relative vertical positions of related components, is disclosed or otherwise rendered obvious by Lung in Grounds 1 and 2 and is also rendered obvious by Park in view of Mokhlesi in Ground 3 and Fukuzumi in view of Mokhlesi in Ground 4.

B. 35 U.S.C. § 314(a)

As stated in Section II.B, there is no currently pending parallel district court litigation addressing the '214 patent. To the extent the potential addition of the '214 patent to the NDCA case warrants a *Fintiv* analysis[7], discretionary denial would be improper due to exceptional circumstances. *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020).

[7] Petitioner reserves the right to address *Fintiv* in view of the facts and the law as they stand following the POPR, should the PO argue for denial under *Fintiv*.

As noted above at FN1, after the Court dismissed PO's counterclaims for alleged infringement of the '214 patent with leave to amend, PO declined to amend its pleadings and instead withdrew its assertion of the '214 patent in August 2024. Moreover, minimal investment was made in the '214 patent before its dismissal—indeed, PO's counterclaims were dismissed due to deficiencies in pleading infringement. EX1019, 1.

This Petition is being filed before the Court decides whether to allow PO to amend its counterclaims, and only two weeks after PO's motion to reassert the '214 patent. EX1011. In addition to the compelling merits of the grounds in this Petition—including the anticipation and single-reference obviousness grounds—these exceptional circumstances warrant institution as a matter of fairness.[8]

Regardless of whether the '214 patent is admitted by the Court, none of the challenged claims in this Petition are asserted in PO's amended counterclaims, further minimizing any risk of overlapping between proceedings. EX1011, Ex. B at 17.

Finally, as explained in the Ranking Notice, claims challenged in the

[8] To the extent the '214 patent become reasserted in the NDCA case and the challenged claims are later asserted, if this IPR is instituted, Petitioner will not pursue the same grounds of invalidity in the district court litigation. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 11-12 (PTAB June 16, 2020).

concurrently filed parallel petition (the '498 IPR) against the '214 patent do not overlap with claims challenged in this Petition. This Petition is the sole challenge to the identified challenged claims before the Board, favoring institution. *Google LLC v. Uniloc 2017 LLC, IPR2020-00115*, Paper 10 at 6 (May 12, 2020).

XI. CONCLUSION

Based on the grounds specified above, IPR of all challenged claims is respectfully requested.

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

This Petition complies with the requirements of 37 C.F.R. § 42.24. As calculated by the word count feature of Microsoft Word, it contains 13,976 words, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices, Certification Under § 42.24(d), and Certificate of Service.

/Zhiwei Zou/
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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing **Petition for *Inter Partes* Review, the associated Power of Attorney, and Exhibits 1001-1020** are being served on February 14, 2025, by U.S. Priority Express Mail at the following address of record for the subject patent.

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P.O. BOX 2938
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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel at the following addresses:

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