Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory

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Abstract

Vertical NAND flash memory cell array by TCAT (Terabit Cell Array Transistor) technology is proposed. Damascened metal gate SONOS type cell in the vertical NAND flash string is realized by a unique 'gate replacement' process. Also, conventional bulk erase operation of the cell is successfully demonstrated. All advantages of TCAT flash is achieved without any sacrifice of bit cost scalability.

Introduction

Recently, in order to keep a trend of increasing bit density and reducing bit cost of NAND flash memories, three-dimensional Bit-Cost Scalable (BiCS) flash technology has been proposed [1]. However, there are two major concerns on the BiCS flash. First of all, it is almost impossible to implement metal gate structure for BiCS flash because it is very difficult to etch metal/oxide multilayer simultaneously. We cannot utilize various advantages of metal gate SONOS cell structure, for example, faster erase speed, wider Vth margin, and better retention characteristics [2]. Another concern is GIDL erase of BiCS flash. An extensive circuit change may be necessary to apply negative bias on word line during erase operation. Area penalty and limited erase voltage are expected.

In this paper, we propose vertical NAND flash memory cell array using TCAT technology for the first time. Above mentioned concerns can be cleared by the TCAT technology without any sacrifice of bit cost scalability.

Architecture and Key Features of TCAT Flash

Figure 1 and 2 show schematic Birds-eye view and the equivalent circuit of the TCAT flash memory. The process sequence is briefly displayed in Fig. 3. Distinctive structural differences with BiCS flash are i) oxide/nitride multilayer stack, ii) line-type 'W/L cut' etched through the whole stack between the each row array of channel poly plug, iii) line-type CSL formed by an implant through the 'W/L cut', iv) replaced metal gate lines for each row of poly plug. The most unique process is 'gate replacement' to achieve the metal gate SONOS structure. Figure 4 shows the detail. After 'W/L cut' dry etch and wet removal of sacrificial nitride layer, gate dielectric layers and gate metal are deposited in the conventional order. It is not 'gate first' process as for BiCS flash [3]. Separation of each gate node is followed by etch processes. Figure 5(a) and 5(b) show the cross sectional SEM images of the fabricated TCAT flash cell array. The cell string has six-NAND cell transistors with SSL transistor at the top and the GSL transistor at the bottom. The SSL and GSL transistors are formed simultaneously with cell transistors. The TEM view of the cell in Fig. 5(c) shows a perfect damascened metal gate SONOS structure in the vertical NAND flash cell string. The stair-like structure at the array edge for interconnection is shown in Fig. 6.

Figure 7 shows equivalent cell size trend of TCAT and BiCS flash. Despite of additional 'W/L cut' structure, cell size of TCAT flash is rather smaller than BiCS flash. It is due to 'gate first' process of BiCS flash. The minimum diameter of plug hole of BiCS flash is limited by the gate dielectric layers.

Another important feature of TCAT NAND flash memory is bulk erase operation. As shown in the schematic structure of Fig. 8, the channel poly plug in TCAT flash structure is connected to Si substrate, not n+ common source diffusion layer as in the BiCS flash. Therefore, conventional bulk erase operation can be achieved as displayed in the simulated profiles of Fig. 9 and the NAND string can be operated without any major peripheral circuit change.

Results and Discussions

Figure 10(a) and 10(b) show the Id-Vg characteristics of cell and selection transistors in a single string and the Vth distribution of cell transistors of 32 strings, respectively. Subthreshold slope is ~ 320mV/dec and the on-off ratio is more than 10^6. Despite poly Si channel, the Id-Vg characteristics and Vth distribution is excellent due to 'macaroni' body effect [3]. In order to suppress program disturb, Vth of selection transistors are adjusted by a device optimization. Figure 11 shows program/erase characteristics of a cell transistor. The erase operation is achieved by conventional bulk erase. The P/E speed of a cell is fast enough for multi-level cell operation. Erase saturation at ~-1V can be a concern, but it can be sufficiently lowered below -3V as the channel-hole diameter shrinks to a product level of ~45nm from 120nm of this paper. It is because that the electric field in tunnel layer becomes stronger as shown in Fig. 12. Endurance to 1E4 cycles is shown in Fig. 13 and long term data retention characteristics at 85℃ is shown in Fig. 14, respectively. Vth window of 5.6V remained after 10 years is good enough for multi-level operation.

Conclusion

We have successfully demonstrated the vertical NAND flash memory array by TCAT technology. Metal gate structure and bulk erase operation are key features of TCAT flash. With the metal gate structure, P/E characteristics and reliability is good enough for multi-level cell operation. TCAT flash is a more realistic future technology for ultra high density up to terabit

References

[1] H. Tanaka, et al, VLSI Symp. Tech. Dig., pp14-15, 2007
[2] Chang Hyun Lee, et al, IEDM Tech. Dig., pp613-616, 2003
[3] Y. Fukuzumi, et al., IEDM Tech. Dig., pp449-452, 2007

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Page 1 of 2

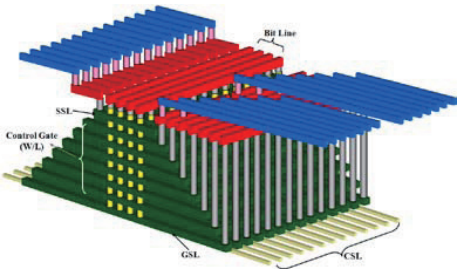

Fig.1 Birds-eye view of TCAT flash memory.

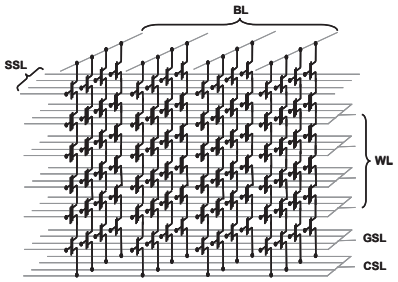

Fig. 2 Equivalent circuit of TCAT flash memory cell array.

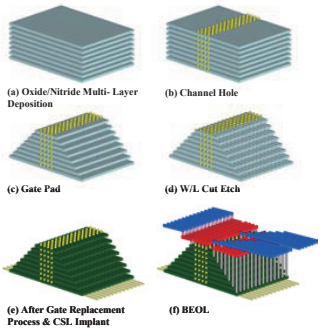

Fig. 3 Process sequence of TCAT flash memory.

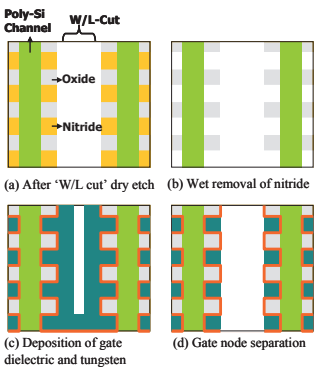

Fig. 4 Concept of the process flow named with 'gate replacement'.

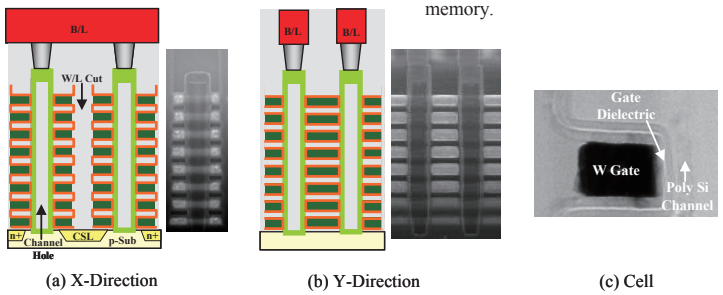

Fig. 5 Cross-sectional SEM images of TCAT flash memory cell strings, (a) X-direction, (b) Y-Direction (c) Enlarged TEM view of a cell in the vertical NAND string.

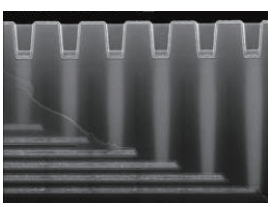

Fig. 6 Cross-sectional SEM image at cell array edge showing stair-like shaped word-line pad structure.

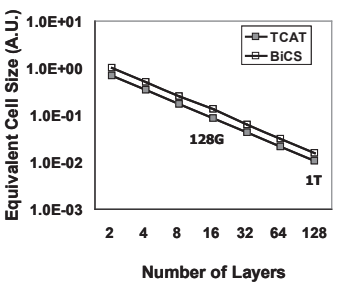

Fig. 7 Equivalent cell size trend of vertical NAND flash memories as stacked layers are doubled for each generation.

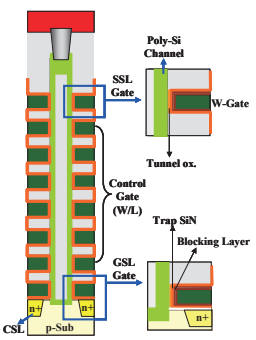

Fig.8 Schematic structures of TCAT flash cell string. Details of selection transistors are shown.

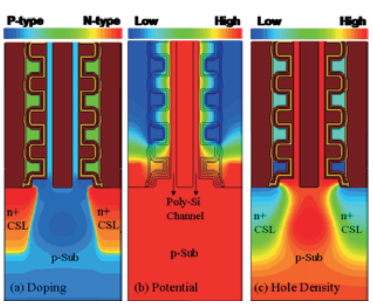

Fig. 9 Simulated profiles during bulk-erase operation of TCAT flash, (a) Doping, (b) Potential, (c) Hole density.

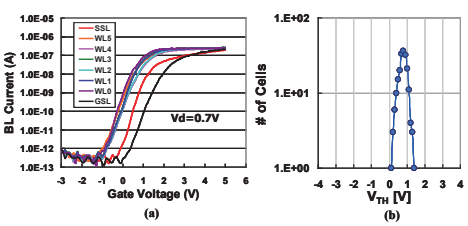

Fig. 10 (a) Id-Vg characteristics of cell and selection transistors in a single string, (b) Vth distribution of cells of 32 strings.

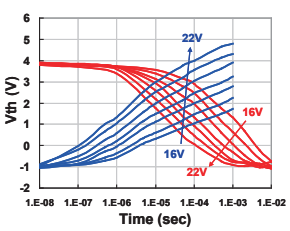

Fig. 11 P/E speed characteristics. Erase operation is achieved by conventional bulk-erase method.

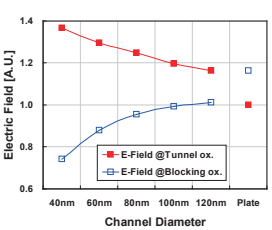

Fig. 12 Electric field in tunnel layer and blocking layer versus channel hole diameter.

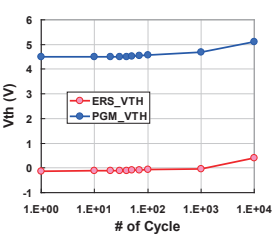

Fig. 13 Endurance characteristics of a TCAT flash cell.

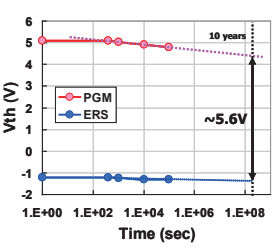

Fig. 14 Long term data retention characteristics of a TCAT flash cell at 85℃.

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Page 2 of 2