

Multi-stacked 1G cell/layer Pipe-shaped BiCS Flash Memory

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Abstract

A three-dimensional 16 stacked 1G cell/layer Pipe-shaped Bit-Cost Scalable (P-BiCS) flash memory test chip with 60nm technology has been developed. The effective 1-bit cell size is $0.00082 \text{ } \mu\text{m}^2$. This paper describes the branched control gate configuration and the new erase operation which are suitable for P-BiCS flash memory. P-BiCS flash memory is one of the most promising candidates for realizing the future T-bit storage device.

Introduction

Three-dimensional memories attract a great deal of attention as an ultra-high density, low bit cost memories. Among several approaches [1-5], Bit-Cost Scalable (BiCS) flash technology [1-4] is one of the most promising candidates for these three-dimensional memories.

The BiCS technology has been demonstrated [1-4]. The BiCS cell array consists of multi-stacked control gate plates and poly-silicon pillars fabricated through control gate plates. Intersections of control gate plates and poly-silicon pillars form SONOS-type memory cells. The source line of diffusion on the silicon substrate has high resistance and degrades the read margin. This issue is solved by a new folded structure of the cell string, named P-BiCS, since the source line is formed by the metal layer. Figure 1 shows a cross section of the P-BiCS cell array. The cell string consists of two pillars and one pipe connecting two pillars at the bottoms. Select gates of the drain side (SGD) and those of the source side (SGS) lie over the control gate plates. The new structure of the cell string requires the new configuration of control gates and row decoders.

In this paper we focus on such a new control gate configuration and the new erase scheme for P-BiCS flash memory to demonstrate the feasibility of P-BiCS flash technology for the future T-bit storage device.

Organization

In the original BiCS flash memory, the control gates are shared by several neighboring rows of cell strings to suppress the area explosion. In P-BiCS flash memory, it is embodied with a branched control gate configuration drawn in Fig. 2. Control gates are realized by fork-shaped plates with four branches. Each branch controls cells of two pages. The block in P-BiCS is formed by vertically stacked 16 pairs of control gates. Each pair of control gate plates is arranged in a staggered layout. (See CG0 and CG31 in Fig. 2 as an example.) Thanks to the high boost efficiency cell, program/erase disturbances are not a serious concern in BiCS [4] and then in P-BiCS.

Unlike control gates, select gates are individually separated for the selectivity of cell strings. Figure 3 shows a schematic of row decoders. Two row decoders are placed on both sides of the cell array, one for CG0 to CG15 and the other for CG16 to CG31. Row decoders only decode the block address. The selectivity of eight select gates in a block is ensured by eight

buses and drivers of select gates. Since the pipe forms a transistor, the pipe gate driver is needed.

Figure 4 depicts the effect of stacking array on the chip size. Since the peripheral circuits are not stacked, the chip size of the simply stacked three-dimensional NAND flash increases with stacking array. On the other hand, there is no area penalty in P-BiCS flash memory except for select gate buses.

In conventional NAND flash, the number of cell strings connected to a bit line has an upper limit because of increasing off currents from unselected strings. This is imposed on the simply stacked three-dimensional NAND flash, too [6]. However, it is not so much worse in P-BiCS flash memory because there is no junction leakage current which is the majority of the leakage current in the planar NAND structure. (See Fig. 5.) This feature enhances scalability of P-BiCS.

Operations

Read and program operations are the same as the conventional NAND flash. Since the P-BiCS cell is a three terminal device not connected with the well for applying erase voltage, a new bias method that is the erase voltage is transferred from source lines to pillars is developed.

The circuit operation and timing diagram of the new erase operation is drawn in Fig. 5. First, the source line voltage is raised with the SGS voltage fixed to 0 in period t1. The voltage difference between the source line and the SGS causes BTB tunneling and electron-hole pairs are generated. Next, SGS is separated from the select gate driver and the source line voltage is raised in period t2. SGS is in the floating condition and its voltage is raised by the coupling with the source line. The hole current transfers the source line voltage to the pillar. In this way, the pillar attains the voltage level required for the erase operation. Finally, control gate voltages are fixed to 0. By the voltage difference between the pillar and control gates, the erase operation is performed.

The floating conditions of control gates and SGS are key technology to realize reliable erase operation against the previous method [1, 2]. Since the erase voltage is supplied from the source line, cells near the source line have a greater tendency to erase than cells near the bit line. The floating condition of control gates in period t1 and t2 is designed for distributing holes evenly over pillars before erase. To avoid SGS gate oxide breakdown, the floating condition of SGS is designed without complex ramp up circuits.

Conclusion

Figure 7 shows a micrograph of the test chip. The string length is 32. The three-dimensionally 16 stacked control gates embody the effective 1-bit cell size of $0.00082 \text{ } \mu\text{m}^2$. Every layer has 1G memory cells. The chip contains 1K blocks with a page size of 8K Byte. Because this chip is as for a first step for realizing the ultra-high density, low bit cost flash memory, peripheral circuits are designed by the relaxed design rule. A commercial 64Gb P-BiCS Multi-Level-Cell flash memory die size is estimated at $10.5 \text{ mm} \times 12.3 \text{ mm}$.

References

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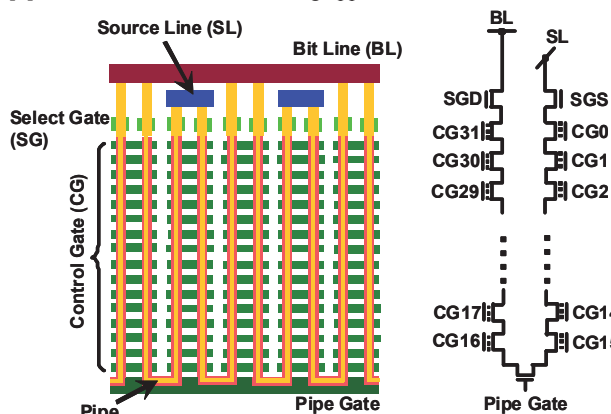


Fig. 1: Cross section of the P-BiCS

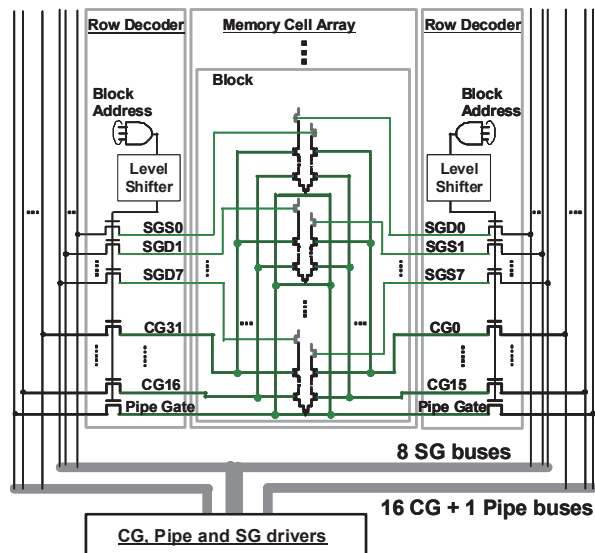


Fig. 3: Row Decoder Configuration

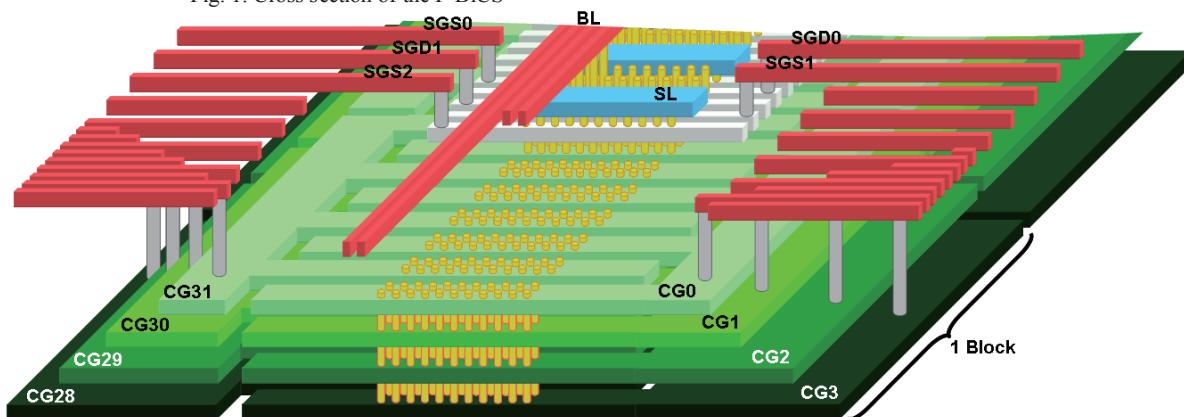


Fig. 2: Branched Control Gate Structure (upper four control gate layers)

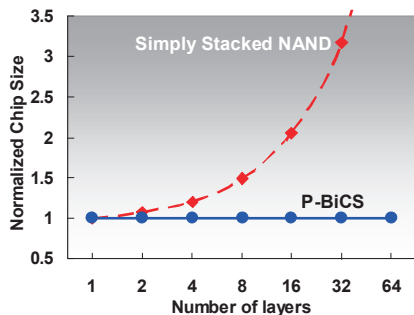


Fig. 4: Effect of Stacking Layer on Chip Size

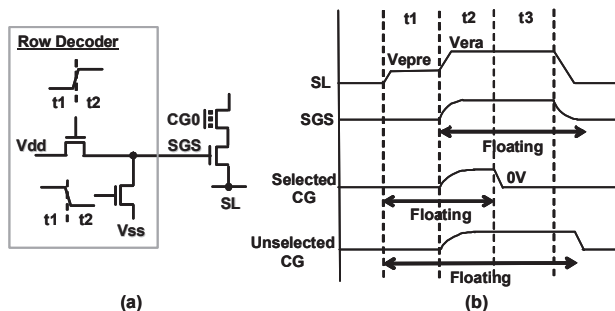


Fig. 6: (a) Circuit Operation for Erase, (b) Timing Diagram for Erase

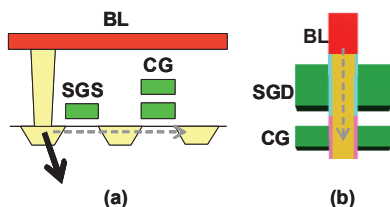


Fig. 5: Leakage Path of Conventional NAND (a) and P-BiCS (b)

Density	1Gcell/layer
Cell Size	0.00082um ²
Number of Layers	16 layers
Block Size	2M Byte(SLC) 4M Byte(MLC)
Page Size	8K Byte
Die Size	10.11x15.52mm ²

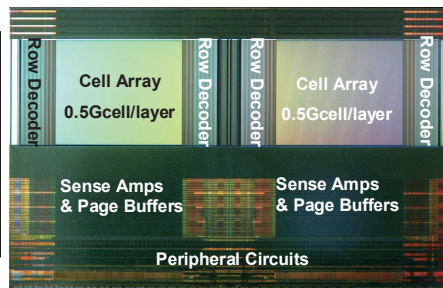


Fig. 7: Chip Image