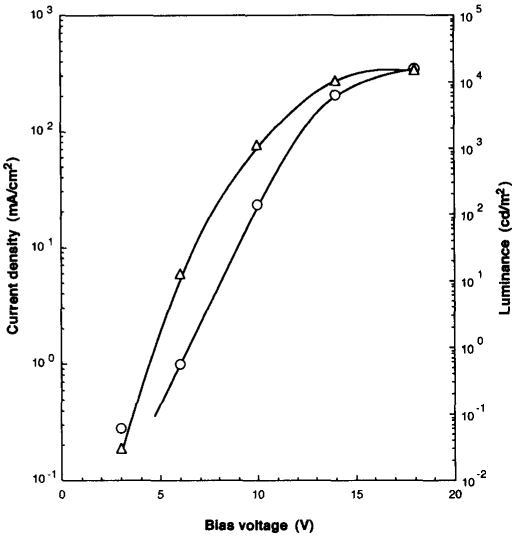


Fig. 3. Luminance (△)–voltage and current (O)–voltage characteristics of a typical ITO/TPD(400 Å)/Alq(400 Å)/Li(10 Å)/Ag(2000 Å).

work function such as alkaline metals. The example of such device with lithium (ϕ = 2.9 eV) as the first metal was constructed, and typical current (I)–voltage (V) and luminance (L)–voltage (V) curves are shown in Fig. 3. The luminescence was observed at a lower threshold voltage (3 V) than that for the Mg cell, and luminance of 15 100 cd/m^2 was achieved at 18 V. This lower drive voltage, or smoother electron injection, was made possible by the low work function of the contact electrode. The barrier existing for the injection of electrons may be reduced by using lithium as the contact electrode. Since EL from Alq has been reported to be enhanced by the factor of 2–3 by doping the Alq layer with other organic dyes [3], the Alq layer in this system was also doped with 1 mol % of coumarin 6. The luminance was drastically enhanced to 40 400 cd/m^2 at 18 V. This extremely intense electroluminescence was the highest luminance so far observed from organic as well as inorganic electroluminescent devices, which is about 5 times brighter than that of a regular fluorescent lamp.

In conclusion, the use of double-layer cathode in organic EL cell enables injection of electrons into organic layer and efficient electroluminescence from the emitting layer, and the stability of the first metal electrode is much improved by the second electrode, which provides stable and efficient EL cells.

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Three-Dimensional Finite-Element Investigation of Current Crowding and Peak Temperatures in VLSI Multilevel Interconnections

J. T. Trattles, A. G. O'Neill, and B. C. Mecrow

***Abstract*—Multilevel interconnection vias are investigated with a coupled thermal and electrical conduction model in three dimensions using the finite-element method. The concept of using a volume to quanitfy current crowding is introduced. Close to a contact via it is found that the peak temperature moves between the upper track and the via as a function of geometry.**

I. Introduction

Scaling down the geometry of integrated circuits increases the current density and associated Joule heating in interconnect tracks and vias, leading to a greater incidence of thermal stress and electromigration failure mechanisms [1], [2]. The temperature (T) and current density (J) dependencies can be described in terms of the mean time to failure (MTF) given by [3]

$$\text{MTF} = AJ^{-n} \exp(\Delta/kT) \quad (1)$$

where k is Boltzmann's constant, Δ is the electromigration thermal activation energy, and the terms A and n are empirical constants.

The ability to predict electromigration failure is crucial for the future development of reliable integrated circuit technology. Finite-element models solving the electrical and thermal diffusion equations have been developed in two [4], [5] and three [6]–[8] dimensions. Frequently, peak current densities are plotted as a function of various geometrical parameters. Unfortunately, quantitative conclusions cannot be drawn from these results, since the peak current density for any geometry containing sharp corners, such as those found at a track–via junction, is infinite [9]. The "peak" current densities will therefore be scaled according to the finite-element discretization. An alternative is to round off the corner but this then makes the solution dependent on the radius of curvature chosen. In this brief, a self-consistent model of the electrical and thermal properties of multilevel interconnects in three

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dimensions is used to quantify the susceptibility of a given track–via geometry to failure in terms of current-crowding volume.

II. Model

The electrical conduction is defined in three dimensions by the equations

$$\nabla \cdot J = 0$$

$$J = -\sigma \nabla \phi \qquad \text{in } \Omega_l \tag{2}$$

where σ is the electrical conductivity and ϕ is the electrical potential. The solution of this equation is restricted to metallic regions (the domain Ω_l). It is used to determine the current density and power loss density from which Joule heating is derived. In all cases a constant current scaling has been assumed rather than constant voltage scaling as this is believed to provide the most realistic guide to interconnect performance. A value of 22.5 mA was chosen, which corresponds to a current density of 10^6 A/cm^2 for a track having a cross section of 1.5 × 1.5 μm^2.

The thermal problem is governed by the equation

$$\nabla \cdot (\kappa \nabla T) = -Q \qquad \text{in } \Omega_a \tag{3}$$

where κ is the thermal conductivity and q is the internal heat generation term. Equation (3) is applied to the domain Ω_a, comprising both insulating and conducting regions, making Ω_l a subdomain of Ω_a. The electric and thermal fields are coupled in two ways: electric conduction in the metallic region gives rise to resistive Joule heating in the form

$$Q = \sigma(\nabla \phi)^2 \tag{4}$$

and the electric conductivity has a temperature dependence which is approximated here by

$$\sigma(T) = \frac{\sigma_0}{1 + \alpha T} \tag{5}$$

where σ_0 is the electrical conductivity at 0°C and α is the temperature coefficient of electrical resistivity which is assumed constant over the temperature range studied. The silicon substrate has a fixed temperature boundary condition corresponding to its function as a heat sink [4]–[8]. An adiabatic boundary condition is taken for the upper surface and all heat must be lost through the substrate. In this way, conditions are simulated close to those experienced by the interconnects during their working lifetime.

Equations (2)–(5) have been implemented in a finite-element scheme using the Galerkin method of weighted residuals [10]. The solver uses incomplete Cholesky decomposition with conjugate gradients (ICCG) to solve the matrix equation resulting from the application of the finite-element method to the original set of partial differential equations.

III. Results

Information on current crowding is important in order to identify those structures which are most susceptible to electromigration failure. Given the track and via dimensions it is straightforward to determine an approximate value for the current density by supposing it to be constant across the cross-sectional area of the track. At bends in the track and at contact vias the current density often exceeds these estimates by significant amounts, and can lead to a preferential failure at these points. The finite-element method is used here to determine the extent to which the geometry of the via or track bend increases the current density above this "one-dimensional" approximation.

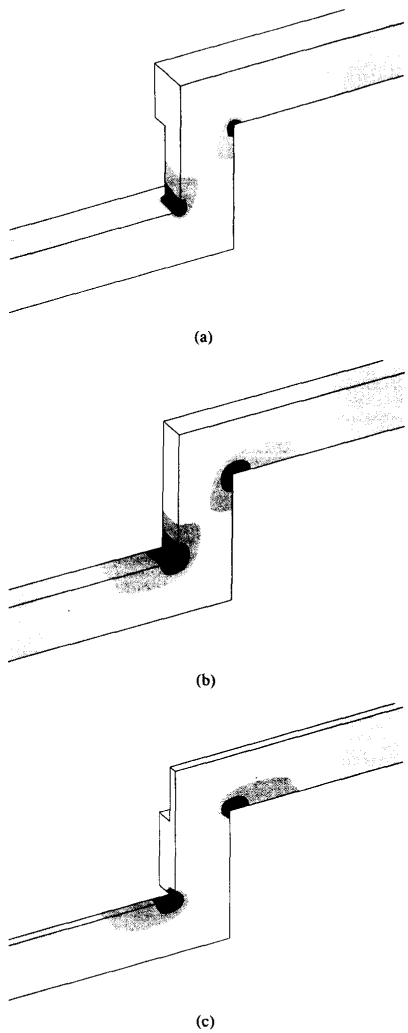


Fig. 1. Change in current-crowding volume as a function of changing track width w_t. (a) w_t = 0.5 μm, (b) w_t = 1.5 μm, and (c) w_t = 4 μm. The via width and track thickness are both held constant at 1.5 μm and the via height is 2 μm. The dark shaded volume represents current densities 20% in excess of the approximate uniform value while the light shaded volume represents current densities 1% in excess.

The effect of current crowding of changing the track width while holding the via width constant at 1.5 μm is shown in Fig. 1. The three plots show how the volume for which the current density exceeds the uniform approximation changes for the cases of: (a) the via width less than the track width, (b) the via and track widths being equal, and (c) the via width being greater than the track width. As expected from the results of two-dimensional conformal mapping [9], the current crowding is centered on the two inner sharp corners where via and track meet. The volumes for which the current density is 20% and 1% greater than the "one-dimensional" value are both shown. In all cases the current crowding volume is

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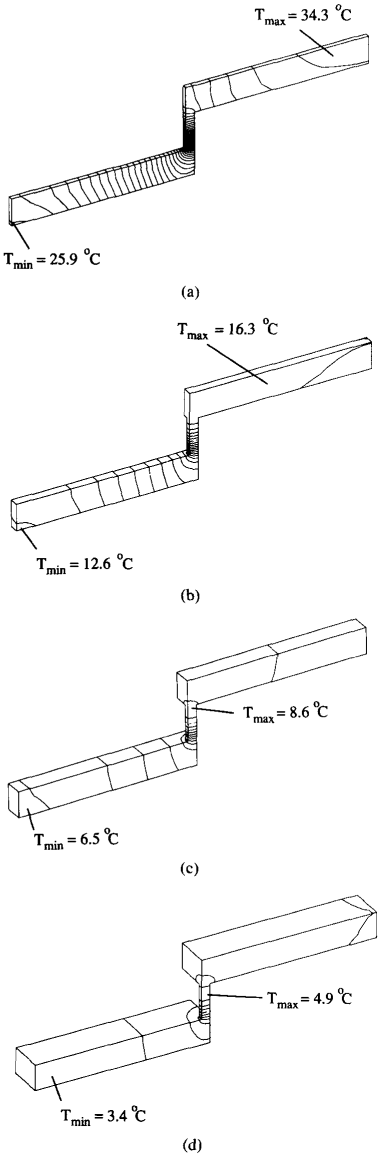


Fig. 2. Temperature contours in the metallic track as a function of changing track width w_t. (a) w_t = 0.5 μm, (b) w_t = 1.0 μm, (c) w_t = 2.0 μm, and (d) w_t = 4.0 μm. The contour separation is 0.15°C and the maximum and minimum temperatures are annotated. As the track width increases, the overall track temperature decreases and a hot spot forms and moves into the via. In all cases the track thickness is 1.5 μm, the via width is 0.5 μm, and the via height is 2 μm.

predominantly in that part of the structure where the cross-sectional area is smallest. For the case of equal via and track widths the volume is almost symmetrical and is equally split between track and via.

The identification of peak temperatures in multilevel interconnects is important because electromigration failure is temperature-dependent and because it can lead to stress gradients being set up inside the structure or even melting. In general, the peak temperature does not coincide with the peak current density but is found to be geometry-dependent. The effect on the temperature profile of increasing the track width from 0.5 to 4 μm has been investigated and temperature contours for the metallization are shown in Fig. 2. To generate these data the tracks were drawn 1.5 μm thick, the via width was 0.5 μm, and the input current was 22.5 mA in all cases. For the narrowest track width the peak temperature is in the upper track. This track is more isolated from the substrate, which serves as the heat sink, than any other part of the metallization and so this initial result is not a surprise. As the track width increases the current density in the track reduces so that the Joule heating is greatest in the via, where the current density is largest. Hence a temperature hot spot forms and eventually resides within the via for the maximum track width of 4 μm. The overall temperature of the track also reduces because the additional metal provides a more efficient thermal path to the heat sink.

IV. Summary

The volume for which current density exceeds that value predicted simply by dividing the input current by the minimum cross-sectional area is introduced in this brief as a quantitative measure of current crowding. The results draw attention to the shortcomings of the simple uniform current density approximation and identify those geometries where it is a particularly poor approximation. When the via width and track width are equal in the geometry chosen, some 22% of the via volume has a current density more than 20% above the uniform current density approximation. A two-dimensional approximation to the problem is not found to be satisfactory in predicting the extent of the current crowding, as in most cases it overestimates the effect.

The impact of via and track geometry on the temperature profile has revealed that the peak temperature moves between the upper track and the top of the via and depends on the aspect ratio of via and track widths. The position of the peak temperature depends on the relative contributions of Joule heating from track and via and therefore the current density, and in addition its magnitude is influenced by the thermal pathway provided by the metal track and insulating layers between the substrate (the heat sink) and the upper parts of the interconnect metallization. For the case where track and via widths are equal the peak temperature coincides with the volume of current crowding. This suggests that such structures are most susceptible to failure particularly if the definition of process design rules the impact of via geometry on current crowding and heating were neglected.

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Effects of High Field Generation of Charge Trapping in the Oxide and Interface Traps on MOS Capacitors and MOSFET's

Akira Ito

***Abstract*—Oxide charge trapping and interface state generation phenomena under the various high-field stress conditions have been investigated using capacitors fabricated on both p- and n-type substrates, and p- and n-channel MOSFET's. It was found that prediction based on MOSFET devices yielded shorter lifetimes than predictions based on capacitors.**

I. Introduction

A gate oxide thickness of less than 20 nm for 5-V processes is very common in VLSI circuits. In the case of high speed and high resolution circuits, such as D/A and A/D converters, a supply voltage of ± 5 V or more is often required. From a design standpoint, it is desirable that both 10-V analog devices and 5-V digital devices have the same gate oxide thickness to optimize the circuit performance. From a process standpoint, it is desirable to have the same gate oxide thickness for process simplicity. The maximum dielectric strength for time-dependent dielectric breakdown (TDDB) is reported to be 2–5.3 MV/cm, which translates to 4–10.6 V for a 20-nm oxide [1]. This is marginal at best for ± 5-V applications. However, this value is a function of defects or weak spots in the oxide and is not a fundamental limit of oxide integrity. Therefore, large dielectric strengths should be obtainable [1]. MOSFET device degradation due to the high-field stress of the gate oxide is a fundamental limit of device reliability since hot-electron device degradation can be minimized by optimizing the lightly doped drain structures (LDD). Measurements have been completed to investigate possible mechanisms responsible for low dielectric strengths.

In order to predict the reliability of gate oxide due to the high-field stress, MOS capacitors were stressed by a constant voltage and monitored by high-frequency C–V for the flatband voltage shift due to charge trapping in the oxide and interface state generation. MOSFET's were also stressed to determine the device degradation which resulted from the interface-state trap generation and the generation of positive charge in the oxide.

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II. Experimental Procedures

The devices used in this study were n^{++} polysilicon-gate capacitors with gate oxide thickness of 20 nm fabricated on 3–5-$\Omega \cdot$ cm n-type and 8–15-$\Omega \cdot$ cm p-type substrates. The gate-oxide films were thermally grown in partial pressure steam with HCl at 920°C for 60 min. A 0.55-μm thick polysilicon film was deposited and doped by $POCl_3$. p- and n-channel MOSFET devices were fabricated using the same gate oxidation process combined with a twin retrograde well CMOS process. The threshold voltages of p- and n-channel devices were -0.9 and 0.7 V, respectively.

Oxide integrity was evaluated by applying a constant voltage stress equivalent to 7–9 MV/cm. The tunneling current was used to monitor the time-dependent break-down of oxide. The capacitors were stressed in both the accumulation and inversion regimes with an applied light source to generate inversion charge. The high-frequency C–V was taken by HP4275 *LCR* meter at fixed intervals and logged until the oxide ruptured or until the flatband voltage shift reached 10 mV. It was necessary to interrupt the applied stress for measurements. It took approximately 1 min to measure the threshold voltage and subthreshold leakage slope, and 1 min to measure the C–V curve. In order to ensure measurement accuracy, two consecutive measurements were taken to evaluate the relaxation of traps. It was found that there were no differences in the threshold voltage or the C–V curve between the first and second measurement. Thus the interruption seemed to have negligible effects on the measured parameters. Relaxation of trapped charge may occur, but the time constant seemed to be longer than the time needed to take the measurements.

The MOSFET's were stressed under a constant gate voltage with source, drain, and body tied to ground. It should be noted here that this is a different stress condition than the nonuniform channel hot-electron stress. The subthreshold current slope, threshold voltage, and gate leakage current were measured at specified intervals until the increase in the subthreshold current slope reached 10 mV/decade or until the change in the threshold voltage at 1 μA with $V_{ds} = 0.1$ V reached 10 mV. If this criterion was not satisfied within the time period of 10^5 s, the lifetime was extrapolated using the least square linear regression. All measurements were performed at room temperature.

III. Results and Discussion

Fig. 1 shows the time to reach the failure criterion of 10-mV shift in the MOS capacitor flatband voltage stressed under the various field conditions. NSP and PSN are the negative and positive stresses under accumulation mode of operation for the p- and n-type substrate, respectively. Likewise, PSP and NSN are the positive and negative stresses under inversion mode of operation. MOS capacitor lifetime can be expressed by the following field dependence equation developed by Lee *et al.* [2]:

$$t_{\text{life}} = \tau_0 \exp\left(\frac{G\alpha}{E_{\text{ox}}}\right) \tag{1}$$

where G is a constant equal to 320 MV/cm, E_{ox} is the electric field in the gate oxide, t_{life} is the estimated lifetime of the gate oxide, τ_0 is the intrinsic lifetime, and α is a constant related to local defects

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