

Sub-10-ps Gate Delay by Reducing the Current Crowding Effect at an Extension

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Abstract: In short-channel CMOS devices with extension structures, current crowding was found to occur in the source extension, significantly degrading current drivability. Reducing this effect by using high-dose extensions and low parasitic capacitance provided by a localized punch-through stopper layer produced high drivability, enabling a sub-10-ps CMOS gate delay to be attained.

I. INTRODUCTION

Applying extension structures to 0.1- μm CMOS devices is attracting much attention as one way to achieve high-speed circuit operation and short-channel-effect (SCE) immunity. This is because the structure junction depth of an extension can be reduced by using rapid thermal processes. Low-energy ion implantation and solid-phase diffusion for fabricating extensions have been proposed [1]-[3]. However, these approaches do not increase the channel current as much as expected in spite of the reduced junction depth and reduced channel length. This will be a severe obstacle to achieving 0.1- μm CMOS devices.

The parasitic resistance of the extension has been evaluated by using the sheet resistance. This is because the extensions have a high impurity concentration, as high as 10^{19} cm^{-3} . So, device operation should be similar to that of a conventional single-drain structure, not to that of a lightly doped drain (LDD) structure. However, the sheet resistance can not fully explain the reduced current drivability of extension structures.

Using simulation and experiment, we have determined that for short-channel CMOS devices with extension structures, the current-crowding effect in the source extension dominates the current drivability. By reducing the process thermal budget, which reduces the current-crowding effect, while still maintaining SCE immunity.

2. Simulation Results

2.1 Current Drivability

We used a two dimensional process-device simulator to evaluate extension device structures with a gate length of 0.2 μm and a gate oxide thickness of 4 nm. Arsenic extension was activated by RTA of 950°C for 10 sec; the RTA dominated the total thermal budget. Compared with $1 \times 10^{14} \text{ cm}^{-2}$ and $2 \times 10^{15} \text{ cm}^{-2}$, 18 % current increase was obtained. We thus examined the

current-flow behavior around the extension structure more precisely.

2.2 Extension impurity profiles

The extension impurity profiles for doses of 1×10^{14} and $2 \times 10^{15} \text{ cm}^{-2}$ are shown in Fig. 1. Because the process thermal budget was reduced, the impurities spread slightly. The junction depth in the lateral and vertical directions are shown as a function of the doses in Fig. 2. Compared with that in the vertical direction, the lateral expansion was quite small. However, for extension doses as small as $1 \times 10^{14} \text{ cm}^{-2}$, the metallurgical junction located below the gate electrode. For doses ranging from 1×10^{14} to $2 \times 10^{15} \text{ cm}^{-2}$, the metallurgical junction length change in the lateral direction was small (less than 5 nm), as shown in Fig. 2. This resulted in a small difference in the SCE immunity, as will be discussed later.

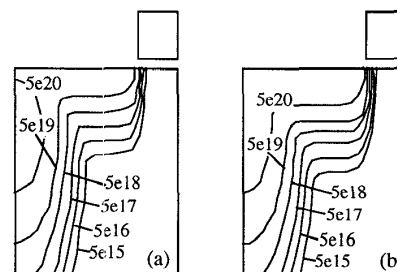


Fig. 1 Impurity distribution in an extension for dosages of (a) 1×10^{14} and (b) $2 \times 10^{15} \text{ cm}^{-2}$.

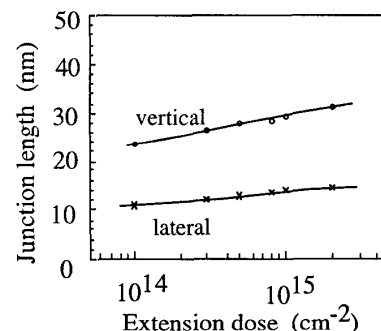


Fig. 2 Diffused junction length in lateral and vertical directions.

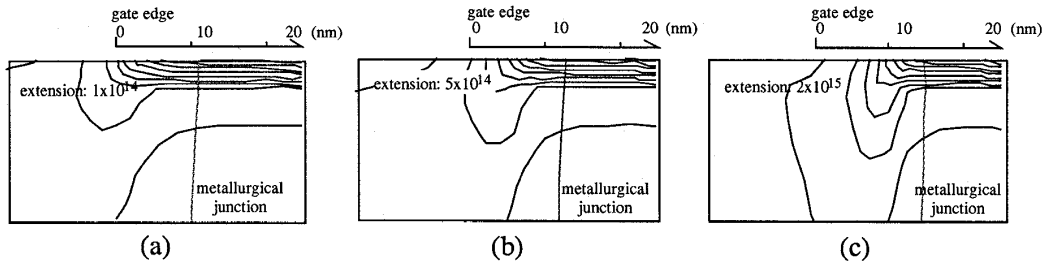


Fig. 3 Simulated current-density distributions around gate edge of source electrode for $V_{gs}=2.0$ V: (a) 1×10^{14} , (b) 5×10^{14} , and (c) 2×10^{15} cm^{-2} extensions.

2.3 Current Flow in Extension

We focused on the current flow around the source extension because the parasitic resistance effect appears in the source region, not in the drain region. The contours of the current density for devices with various dosage extensions are plotted in Fig. 3. For the high-dose extension, the current flow was widely spread in the source extension. When the flow approached the metallurgical junction, it suddenly rose to the surface. For the low-dose extension, the current crowded at the surface instead of spreading widely. To clarify this current crowding, we plotted the current density profile at 10 nm inside the gate edge. As shown in Fig. 4, for the low-dose extensions, the current density near the surface was higher than that for the high-dose extensions and did not spread into the substrate.

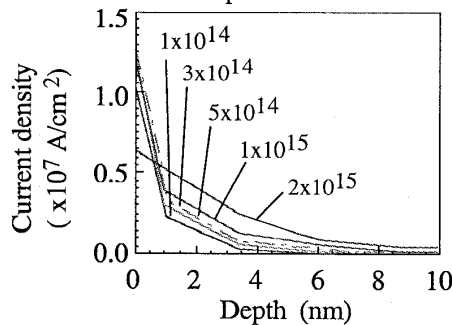


Fig. 4 Vertical current density profile at 10 nm inside the gate edge with extension dosage as a parameter.

The current crowding started outside the gate electrode for low-dose extensions. And, the current-crowded length of 10-20 nm is not negligible compared with a 100-nm gate length. Consequently, this current-crowding region, which we thought to be a low-resistance region because of the overlap effect, causes the high parasitic resistance.

3. Experimental Results

3.1 Sample Device Structure

Using selective CVD-W for a SALICIDE-like process and the parameters shown in Table 1, we fabricated the stacked-metal T-gate-structure CMOS device shown in Fig. 5 [4]. As described in Sec. 2, we performed impurity activation at 950 °C with 10-sec RTA. The typical source-and-

drain series resistance was reduced to 220 $\Omega\mu\text{m}$ for NMOS and 700 $\Omega\mu\text{m}$ for PMOS. The extension ion-implantation dose was the main parameter.

To make the best use of the high current drivability, we aimed to reduce the parasitic resistance. Using EB lithography to localize the punch-through stopper layers, we obtained junction capacitances as small as 0.3 fF/ μm^2 .

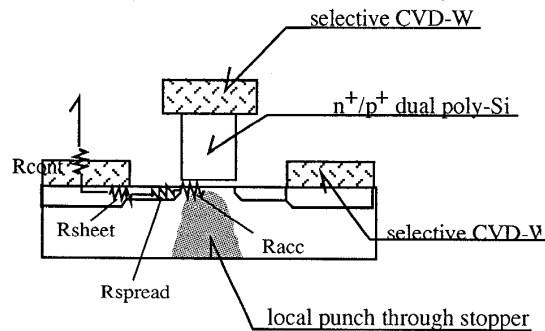


Fig. 5 Fabricated device structure, including four resistance components (R_{cont} , R_{sheet} , R_{spread} , and $R_{\text{accumulation}}$).

Table 1 Main process parameters

Gate dielectrics	NO	3.5 nm
Gate	Dual poly Si	200 nm
	Selective CVD-W	80 nm
S/D	Extension+S/D	As 15 keV
		BF2 10 keV
	+Selective CVD-W	80 nm
metal-1	CVD-W	300 nm
metal-2	TiN/Al	150 nm/ 900 nm

3.2 Extension Modulation

Because current crowding occurs in the extension region, the edge of the extension should be modulated by a gate electrode. We thus precisely measured the gate-extension overlap capacitance according to Ref. [5]. The gate bias dependences for the structure used in Fig. 6 are summarized in Fig. 7. PMOS showed the larger capacitance and stronger dependence. At a high-dose of 2×10^{15} cm^{-2} for NMOS, the overlap capacitance was slightly larger than those of the

low-dose extensions. The gate bias dependence was slightly small for low gate bias. Because the overlap capacitance depends on the gate bias for extension structure, the overlapped region was clearly modulated by the field effect of the gate. This suggests that current crowding occurs in the extensions.

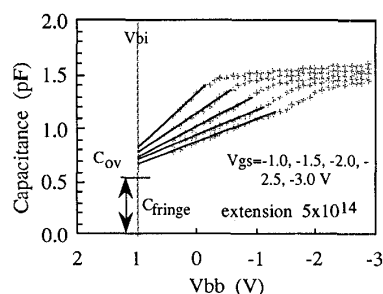


Fig. 6 Dependence of gate-source overlap capacitance on substrate bias with gate bias as a parameter.

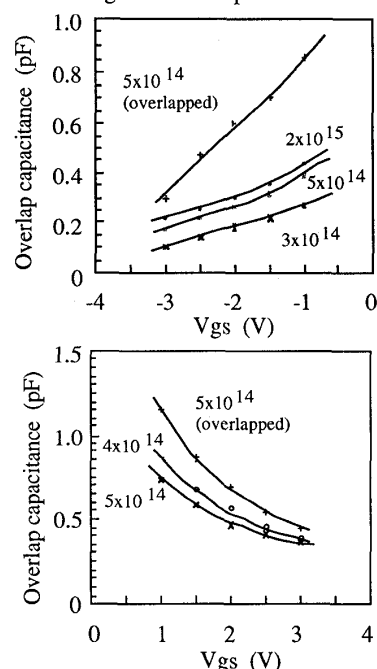


Fig. 7 Measured overlap capacitance of NMOS and PMOS with extension dose as a parameter. Long overlapped devices, which were processed using large thermal budgets, are plotted as a comparison.

3.3 Current Drivability and SCE

We measured the current drivability and short-channel characteristics because there is a trade-off between current drivability and SCE immunity. The measured device characteristics are shown in Figs. 8-10. For NMOS, the drain current strongly increased with extension dose. PMOS drivability was not sensitive to the extension structures. Therefore, NMOS drivability can be improved by increasing the extension dose. The current increase was so large that it is difficult to attribute it

to the different sheet resistances of $380 \Omega/\text{sq.}$ for $3 \times 10^{14} \text{ cm}^{-2}$ and $200 \Omega/\text{sq.}$ for $2 \times 10^{15} \text{ cm}^{-2}$.

In Fig. 5, the MOSFET resistance in the source region is shown schematically. Using these components, the series resistance is described as [6]:

$$R_{\text{total}} = R_{\text{cont}} + R_{\text{sheet}} + R_{\text{spread}} + R_{\text{accumulation}}$$

In the equation, the current-crowding effect is included in R_{spread} and $R_{\text{accumulation}}$. Based on the measured contact resistance and the difference in R_{sheet} , the difference in total resistance is about $620 \Omega \mu\text{m}$ which corresponds to 20-nm channel-length modulation. Because this length is almost the same as the crowding length, current crowding is the main factor in reducing the current drivability for low-dose extension. Therefore, current crowding in an extension is described as channel length expansion, not as spreading resistance effect. For experimental low-dose devices, the gate edge became a non-overlap "offset"-like structure, and a large current-drivability difference was observed.

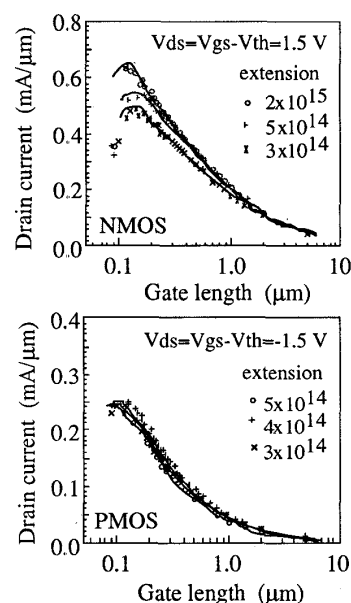


Fig. 8 Drain current dependence on gate length with extension dose as a parameter.

The roll-off characteristics are shown in Fig. 9. For the $2 \times 10^{15} \text{ cm}^{-2}$ extension dose for NMOS, the roll-off started from the long channel region, but the roll-off slope was gentle down to the $0.1 \mu\text{m}$ gate length. The large depletion layer of the high-dose extensions results in this difference due to the charge sharing effect. Even for high doses, such as $2 \times 10^{15} \text{ cm}^{-2}$ for NMOS, good subthreshold characteristics were obtained, as shown in Fig. 10. Therefore, by reducing the thermal budget, high current drivability and good SCE immunity can be achieved simultaneously.

9.7.3

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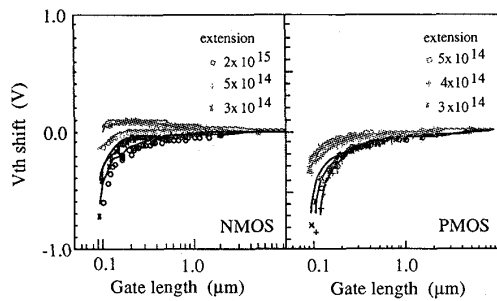


Fig. 9 Roll-off characteristics dependence on extension dose. Gray lines are extracted threshold voltage and black lines are threshold voltage defined by 1-nA/μm channel current with $V_{ds}=1.5$ V.

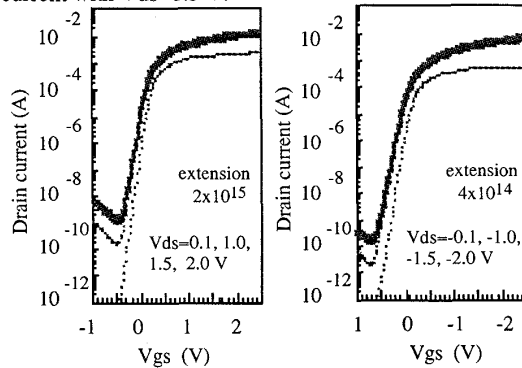


Fig. 10 Subthreshold characteristics with 95-nm channel length NMOS and 120-nm PMOS.

3.4 Circuit Performance

To evaluate the effect of drivability on circuit performance, we fabricated CMOS ring oscillators. When the current drivability was increased and the parasitic capacitance was reduced, a short oscillating waveform of 8.0-ps at 2.5 V was observed, as shown in Fig. 11. The gate-delay dependence on the length is shown in Fig. 12. By using CMOS devices, a sub-10-ps gate delay can be obtained for high current condition.

Based on the measured gate delay, we separated the effect of each delay component, as shown in Fig. 13. By dividing the junction capacitance (C_j), the gate capacitance (C_{gate}), and the wiring capacitance (C_{wire}) by the current drivability, these components were calculated. The remaining C_{op} is mainly due to the Miller effect and feed-forward effect, which degrades circuit performance. It is clear that the overlap capacitance severely constrains gate-delay performance in short-channel devices.

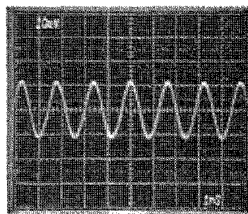


Fig. 11 Waveform of 0.1 μm-gate-length 10 1-stages CMOS ring oscillator at 2.5 V.

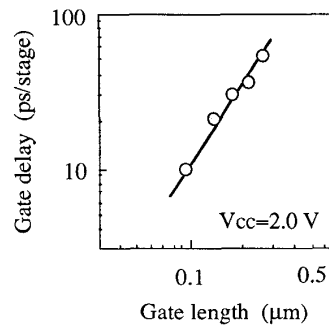


Fig. 12 Unloaded CMOS ring oscillator gate delay dependence on gate length.

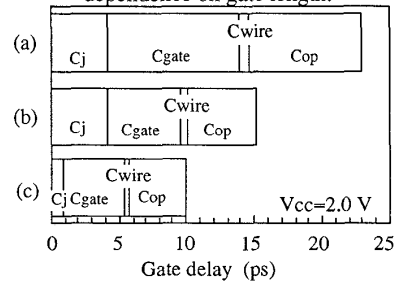


Fig. 13 Comparison of three types of CMOS measured gate delay. (a) large thermal budget, (b) low thermal budget, and (c) low thermal budget and low junction capacitance devices were used. Component contribution sensitivities were calculated based on the current drivability and capacitance.

4. Conclusion

We investigated extension MOSFET structures in detail and determined the following:

(1) reducing the thermal budget prevents the extension impurities from spreading toward the channel resulting in high short-channel-effect immunity.

(2) for low doses extensions, the current crowding occurs in the extension, dominating current drivability.

(3) by reducing the current-crowding effect, high current drivability can be obtained. High drivability and low parasitic capacitance can offer sub-10-ps gate delay performance in 0.1-μm CMOS devices.

Acknowledgments

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