

On the Reliability Issues of RF CMOS Devices

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Abstract

Although multi-finger MOS structures have demonstrated very attractive behaviors for high-frequency analog circuit applications, the shared drain and source regions for adjacent gate fingers have led to current crowding and results in the finger number-dependent current-voltage characteristics. In addition, the high current density spots near the drain region would deteriorate the MOS reliability in several aspects. Present results suggest that the common drain regions should be wider and more heavily doped in order to alleviate these effects.

1. Introduction

The continuous downsizing of MOS transistor to deep submicron range has enabled the application of MOS device in RF circuits [1-5]. The operation frequency of MOS transistor can be further enhanced by using multi-finger layout structure to minimize the parasitic gate capacitance and substrate resistance (Fig.1). However, this structure was found to have more significant hot carrier degradation when compared to the conventional layout. This work aims to study the physical mechanism of characteristics degradation associated with the multi-finger RF MOS structure. Devices with gate length ranging from 0.18 to 0.75 μm was fabricated with TSMC 1.8 V NMOS process. The gate oxide is 3.2 nm thick and the cutoff frequency f_t of the transistors is in the range of 40 to 80 GHz.

2. Results and Discussion

It was demonstrated that partitioning the large channel width to several interconnected narrow (with gate finger width W_f) MOSFETs should be electrically equivalent and can suppress the parasitic capacitance. However, experimental results indicate that the current-voltage (I-V) characteristics are not exactly the same. Fig.2 illustrates the I-V characteristics of MOS devices with gate length of 0.18 μm and channel widths are normalized to two finger width (20 μm). In the ohmic region the drain current of 8-finger device is much smaller than the 2-finger devices. In saturation

region, 8-finger device has slightly larger drain current than the 2-finger devices. It was also found that the threshold voltage also decreases as the number of fingers increases (see Fig.3). In addition, hot carrier induced device degradation is another major concern. Fig.4 shows the hot-carrier induced threshold voltage (V_{th}) and transconductance (g_m) degradation of 0.35- μm gate length transistor with eight 10 μm -width fingers. The hot-carrier induced degradation in such device is much larger than its single-finger counterpart [6]. The transconductance degradation can be as large as 28% with about 3 hour of stressing at constant gate current of 2.3 pA. Those effects cannot be explained with the existing theories and models for single-finger gate structure.

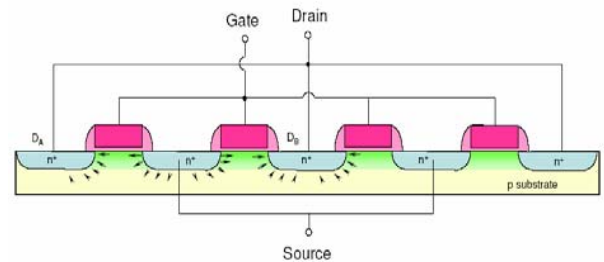


Fig.1 In a multi-finger MOSFET, source and drain regions are shared amongst different fingers

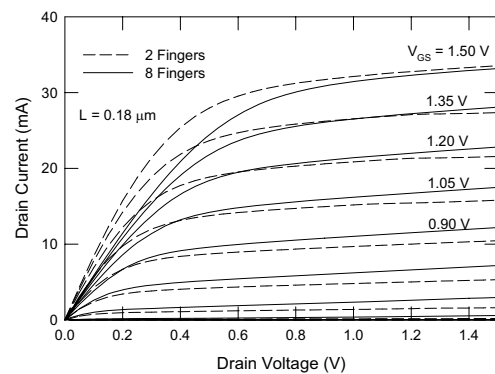


Fig.2 Plot of I-V characteristics for MOS devices with different number of fingers.

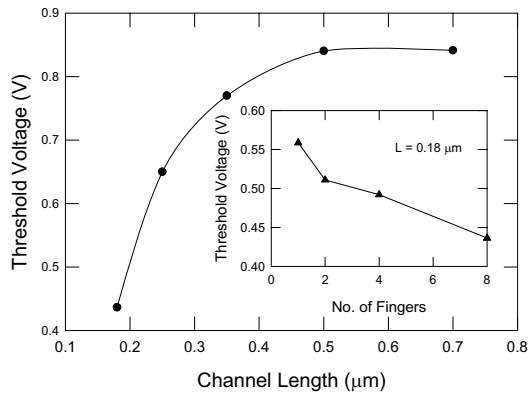


Fig.3 Plot of channel length dependent threshold voltage of 8 fingers transistors. Inset depicts the variation of threshold voltage as a function of finger number.

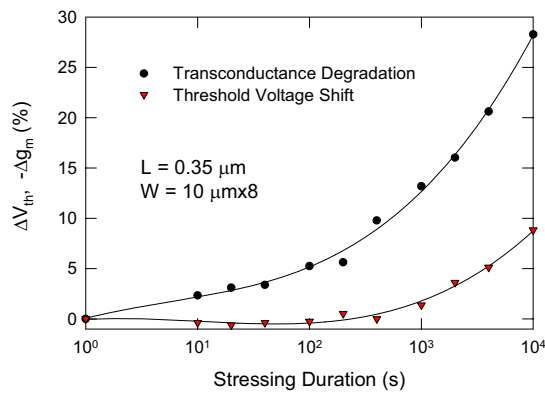


Fig.4 Significant degradations of threshold voltage and transconductance were recorded during hot carrier stressing of multi-finger transistor.

Multi-finger devices also have much smaller drain breakdown voltage. Fig.5 shows the drain breakdown characteristics a conventional (single finger) gate and a multi-finger device. The breakdown voltage of single-finger shifts to low-voltage side as the gate voltage becomes larger. The characteristic was explained and modeled with the parasitic bipolar transistor and the drain avalanche breakdown [7-8]. At large gate bias (> 0.9 V), the multi-finger devices experience soft drain breakdown instead of hard breakdown. Again, it is an unexpected result and cause serious reliability issue for modern and future RF MOS devices.

Fig.6 depicts the hot-carrier induced threshold voltage and transconductance degradations for devices with same gate length of 0.18 μm but with different number of fingers. It was found that the 8-finger device

has a significant degradation at a relatively low gate current fluence (~ 0.1 C/cm²). In addition, at very low fluences (< 0.01 C/cm²), although V_{th} degradation is very small, significant g_m degradation is still registered indicating mobility degradation is more serve in this device. For 2-finger device, both V_{th} and g_m degradations are minimal. Electric field distribution of the shared drain should not be the cause for the observed abnormal behaviors. 2-D device simulations using Silvaco were conducted to compute the current and electric field distributions. As depicted in Fig.7, the electric field distribution of the gate-to-drain region is essentially the same for single finger drain and shared drain. Although the electric field at the mid point of drain is enhanced in the shared drain of multi-finger devices, it should have little effect on the hot electron induced degradation.

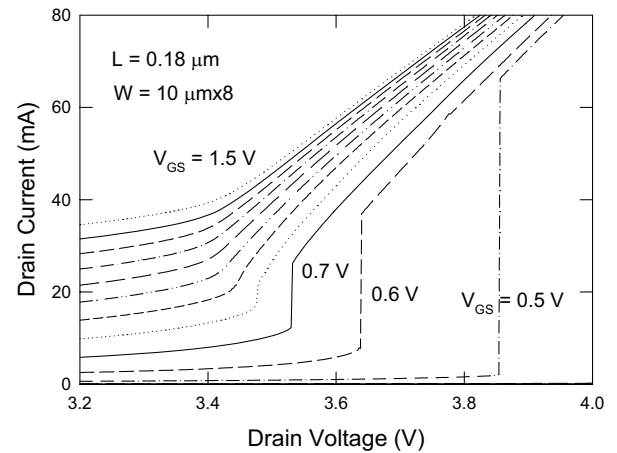
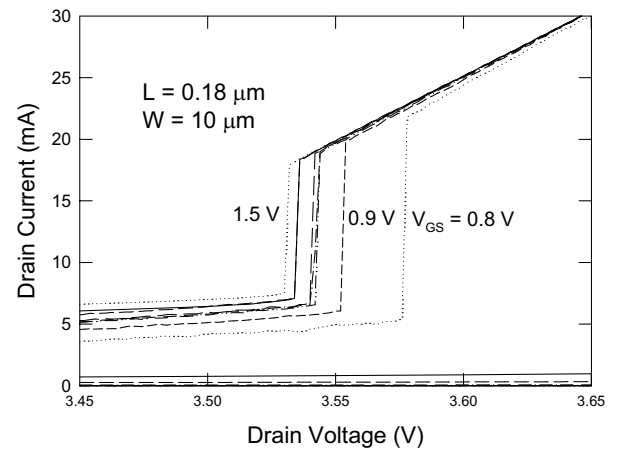


Fig.5 Comparison of drain breakdown characteristics of conventional and multi-finger MOS transistors. The gate length of the transistors are 0.18 μm .

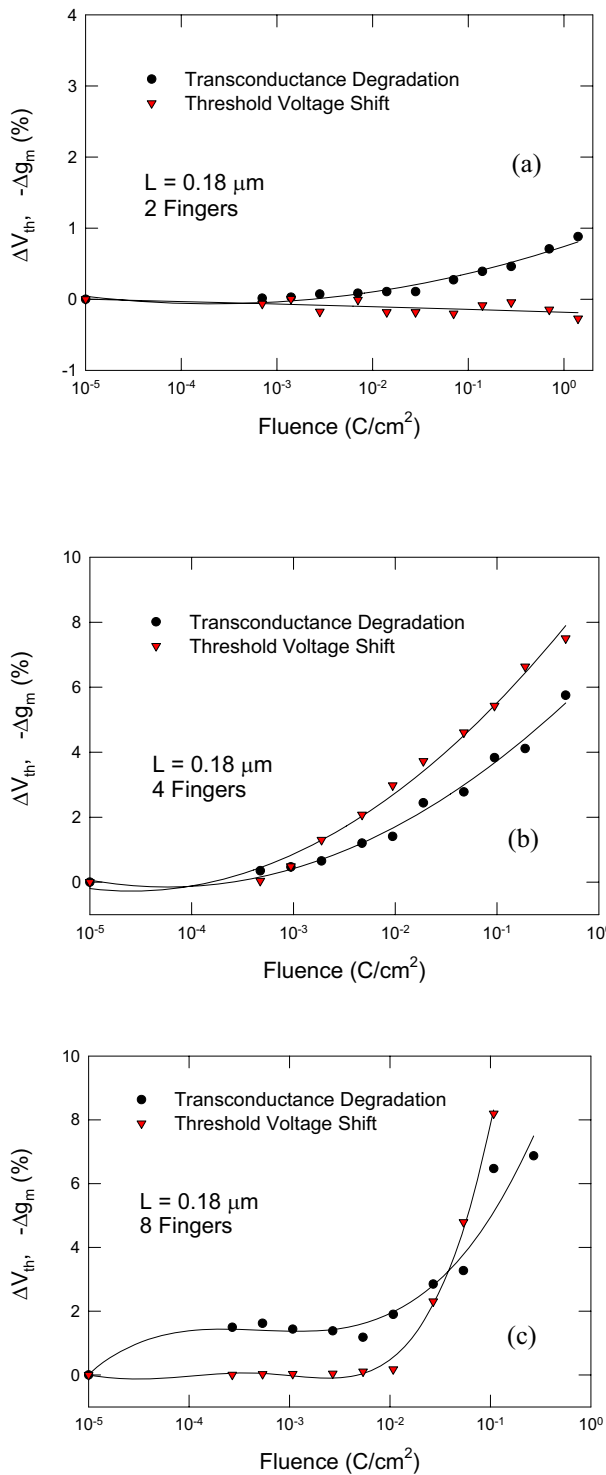


Fig.6 Comparison of hot carrier induced threshold voltage and transconductance degradations for multi-finger MOS transistors with $0.18 \mu m$ gate length.

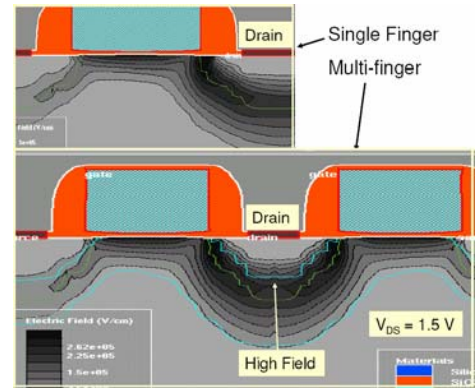


Fig.7 Electric field distribution of conventional and multi-finger (lower) MOS transistor.

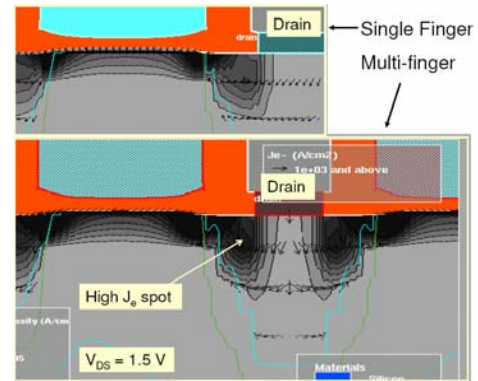


Fig.8 Current distribution in the drain region of a conventional (upper) and multi-finger (lower) MOS transistor biased at $V_{GS} = 1.5 V$ and $V_{DS} = 1.5 V$. Significant drain current crowding is observed multi-finger transistor.

Fig.8 shows the drain current distribution of a transistor with single finger and double fingers. For high drain voltage bias ($V_{DS} = 1.5 V$), significant drain current crowding was observed as a result of sharing the drain with limited draining capacity. This observation can be explained as follow. In single finger device, the drain region carries one unit of drain current which is distributed rather evenly over the whole drain. However, in multi-finger devices, the same drain has to carry two units of drain current and each unit take place in half of the drain region only. As a result, the drain current flows through the shared drain experiences larger resistance than in conventional drain. This limited draining capacity does not only impose a limit on the current-voltage characteristics (see Fig.2) but also gives rise to the current crowding effect in the drain high field region. The high current density spots in shared drains will increase the current density and temperature of the

impact ionization region which in term will enhance the hot carrier effects [6] and reduced the drain breakdown voltage [7-8]. The observed soft drain breakdown in multi-finger devices as depicted in Fig.5 can also be explained with the current crowding effect.

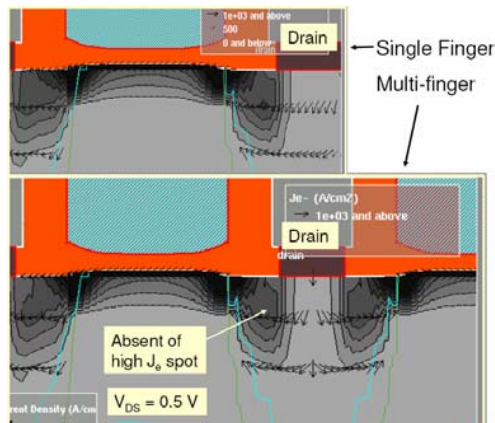


Fig.9 At drain bias of 0.5 V, drain current distribution of multi-finger (lower) MOS transistor is smaller than that of conventional transistor.

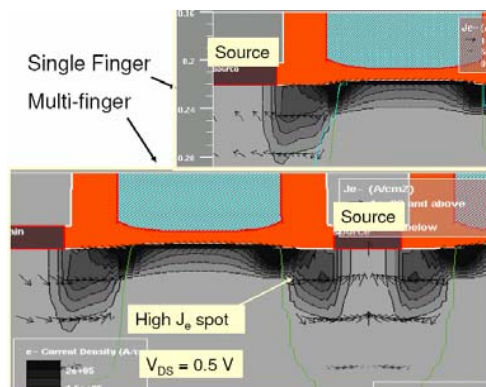


Fig.10 At drain bias of 0.5 V, high current density spot was found in the source region of multi-finger (lower) MOS transistor.

Figures 9 and 10 depict the drain current and source current distributions at a small drain bias of 0.5 V from Silvaco simulation. It is obvious that at small drain bias or in the linear region of MOS transistor, the drain region high current density spots disappeared but high current spots were found in the shared source region (Fig.10). The drain current may be saturated because the source current has reached the maximum. The source current crowding effects can be used to explain the observed smaller ohmic region current in multi-finger devices but should have less effect on the hot

carrier-induced characteristics degradation.

3. Summary

In summary, although multi-finger MOS structures have demonstrated very attractive behaviors for high-frequency analog circuit applications, the shared drain and source regions for adjacent gate fingers have led to current crowding and results in the finger number-dependent I-V characteristics. Particularly, the high current density spots near the drain would deteriorate the MOS reliability. Present results suggest that the common drain regions should be wider and more heavily doped in order to alleviate the current crowding effects. New design methodologies have to be developed for the device layout design of multi-finger transistors.

Acknowledgments

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