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Sim et al.

(54) MEMORY DEVICES INCLUDING VERTICAL PILLARS AND METHODS OF MANUFACTURING AND OPERATING THE SAME

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H01L 21/336 (2006.01)

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(57) ABSTRACT

In a semiconductor device and a method of forming such a device, the semiconductor device comprises a substrate of semiconductor material extending in a horizontal direction. A plurality of interlayer dielectric layers is provided on the substrate. A plurality of gate patterns is provided, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer. A vertical channel of semiconductor material extends in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconducting region.

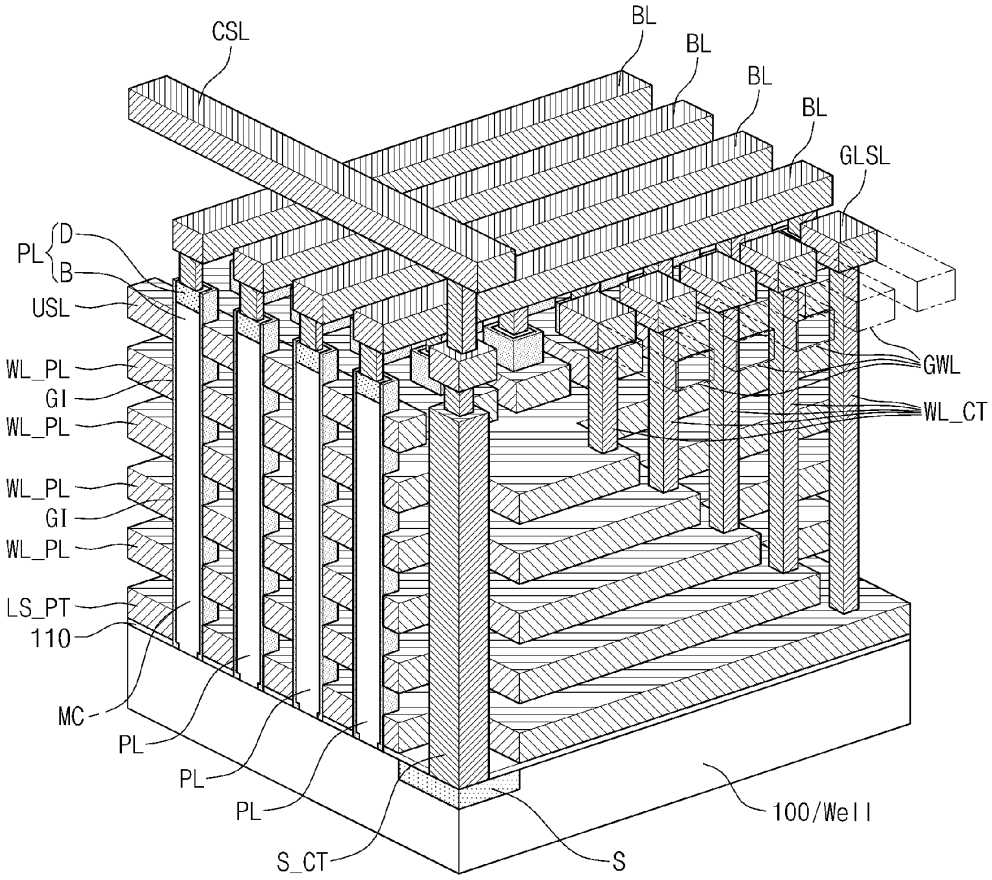


Fig. 1

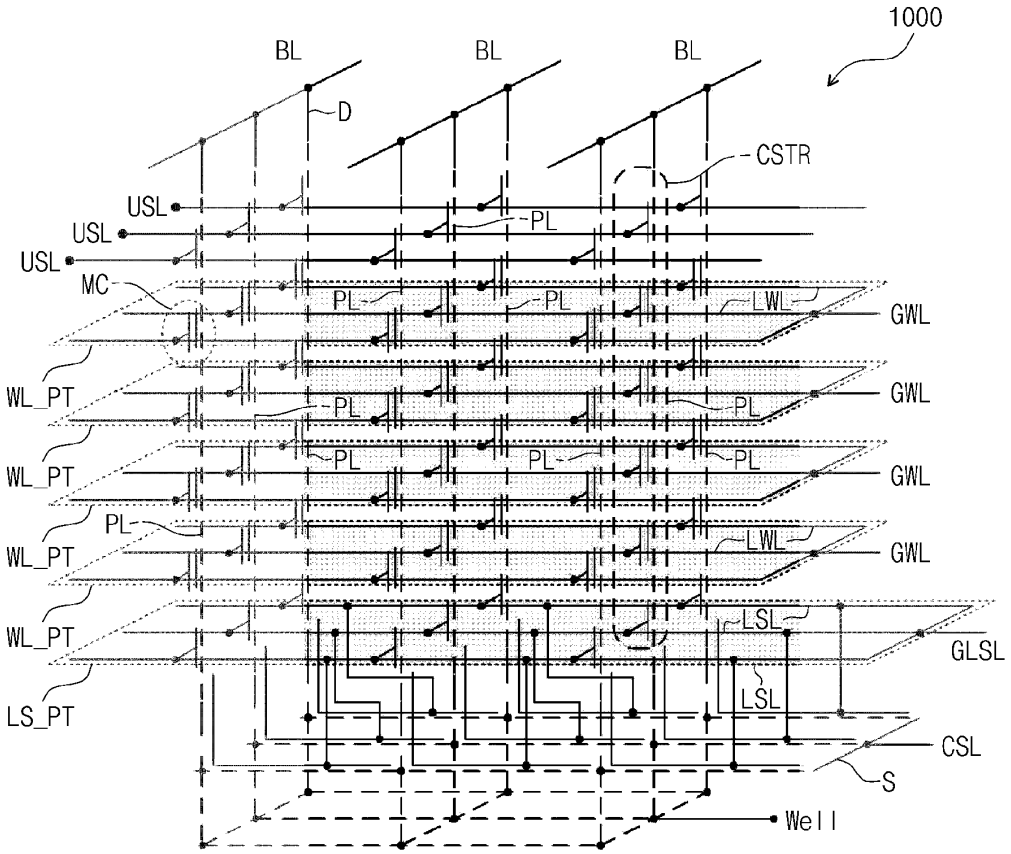

1000
BL
BL
BL
D
CSTR
USL
USL
USL
PL
MC
PL
PL
LWL
GWL
WL_PT
PL
PL
GWL
WL_PT
PL
PL
PL
GWL
PL
WL_PT
LWL
GWL
WL_PT
LSL
GLSL
LSL
LS_PT
CSL
S
Well

Fig. 2

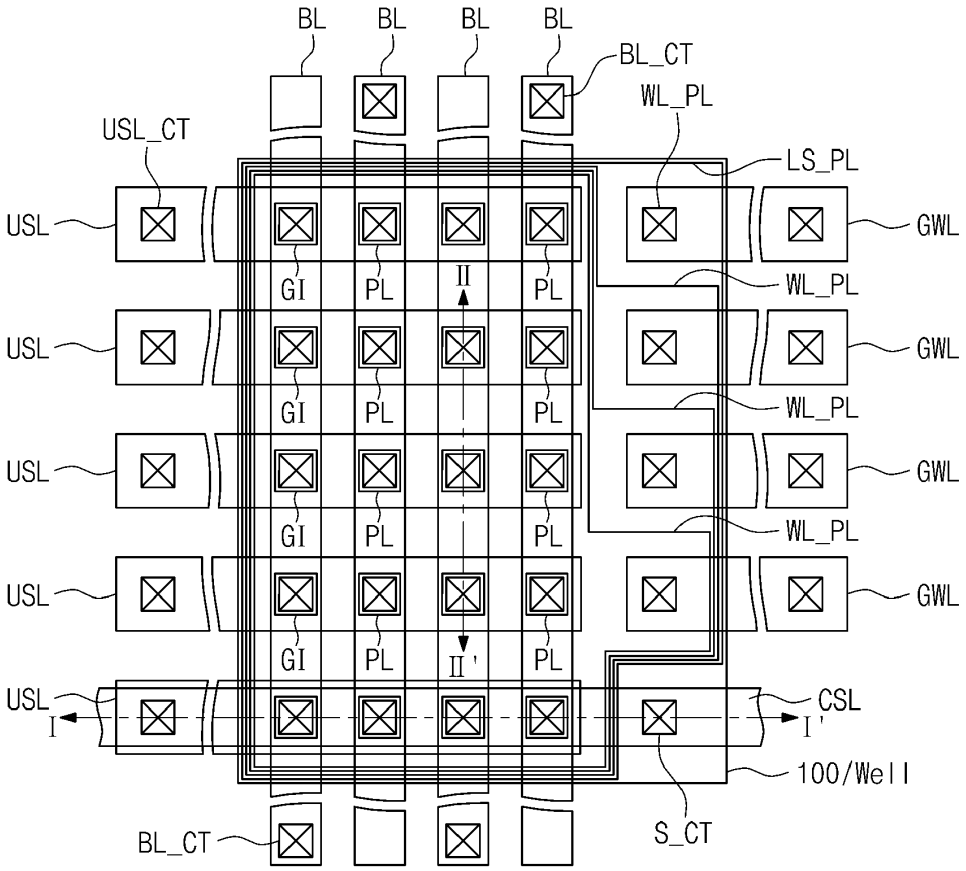

BL
BL
BL
BL
BL_CT
WL_PL
USL_CT
LS_PL
USL
GWL
GI
PL
II
PL
WL_PL
USL
GWL
GI
PL
PL
WL_PL
USL
GWL
GI
PL
PL
WL_PL
USL
GWL
GI
PL
II'
PL
USL
CSL
I
I'
100/Well
BL_CT
S_CT

Fig. 3

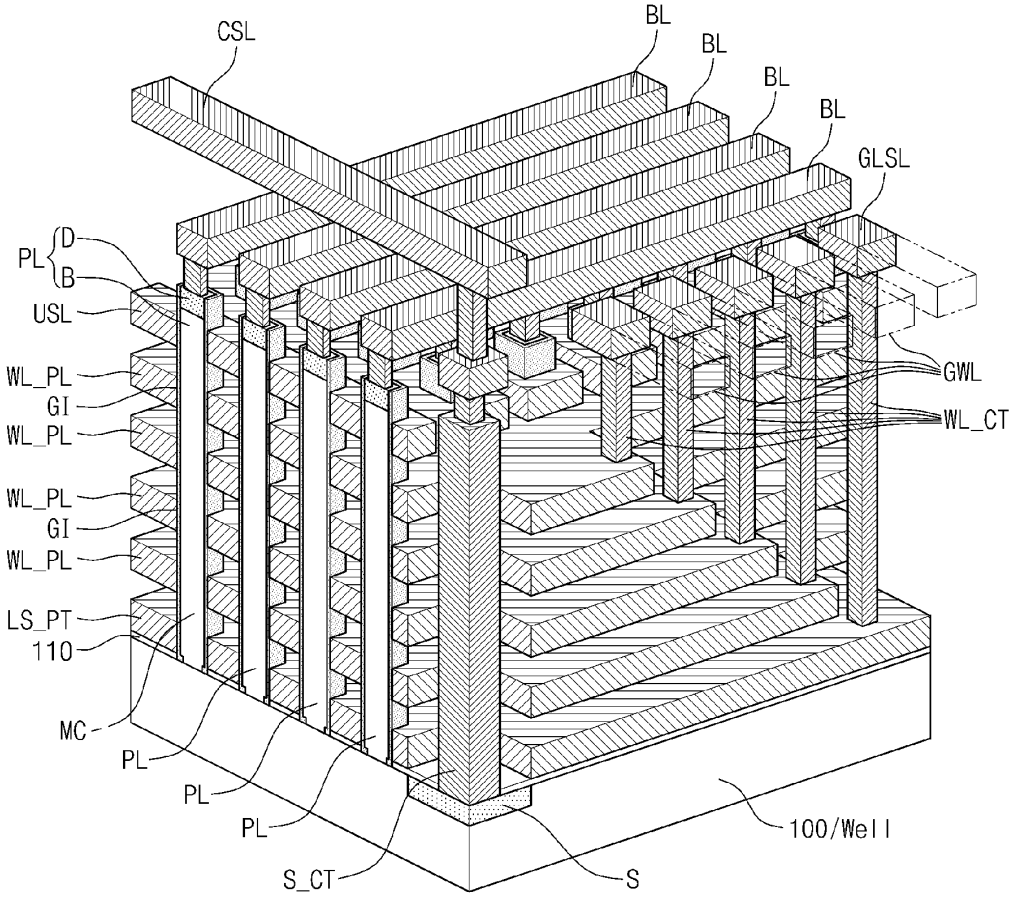

CSL
BL
BL
BL
BL
GLSL
PL
D
B
USL
WL_PL
GI
WL_PL
WL_PL
GI
WL_PL
LS_PT
110
MC
PL
PL
PL
S_CT
S
100/Well
GWL
WL_CT

Fig. 4

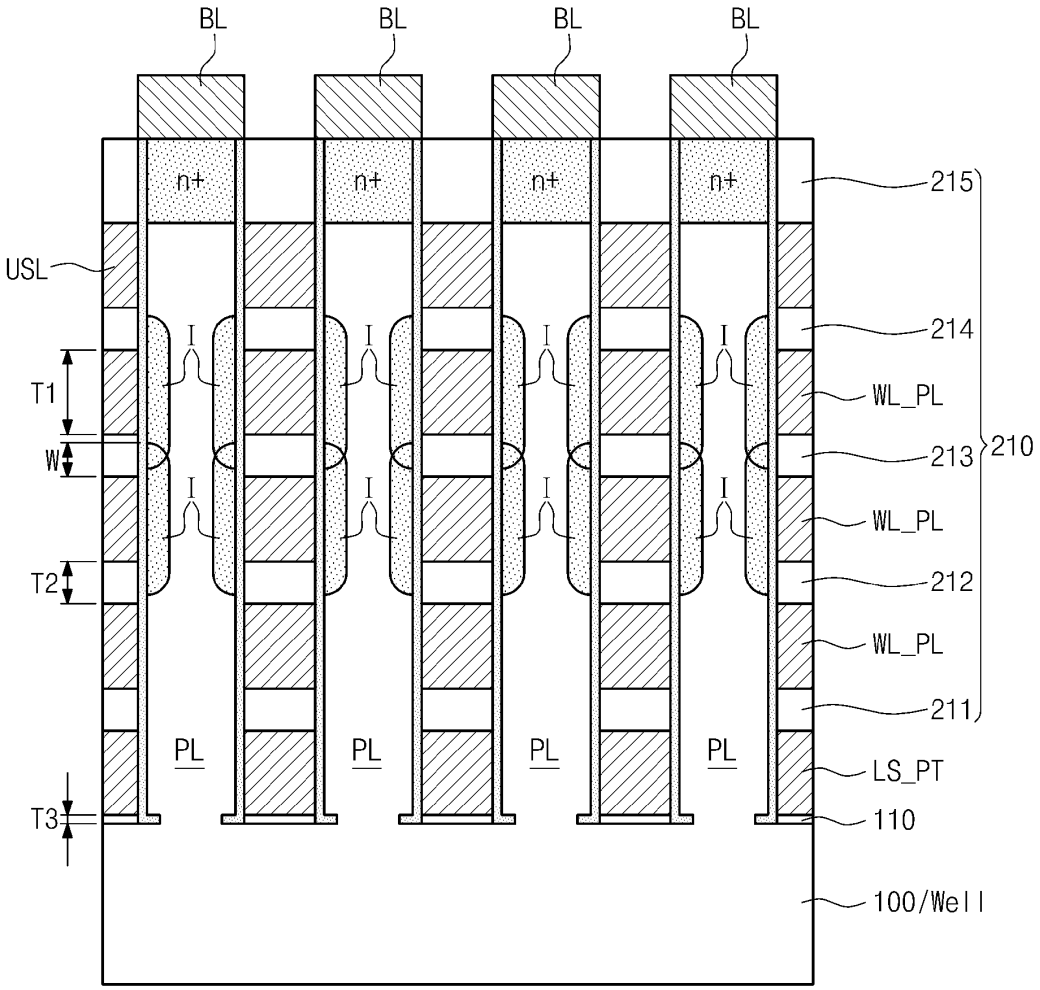

BL
BL
BL
BL
n+
n+
n+
n+
215
USL
214
I
T1
WL_PL
W
213
210
WL_PL
T2
212
WL_PL
211
PL
PL
PL
PL
LS_PT
T3
110
100/Well

Fig. 5

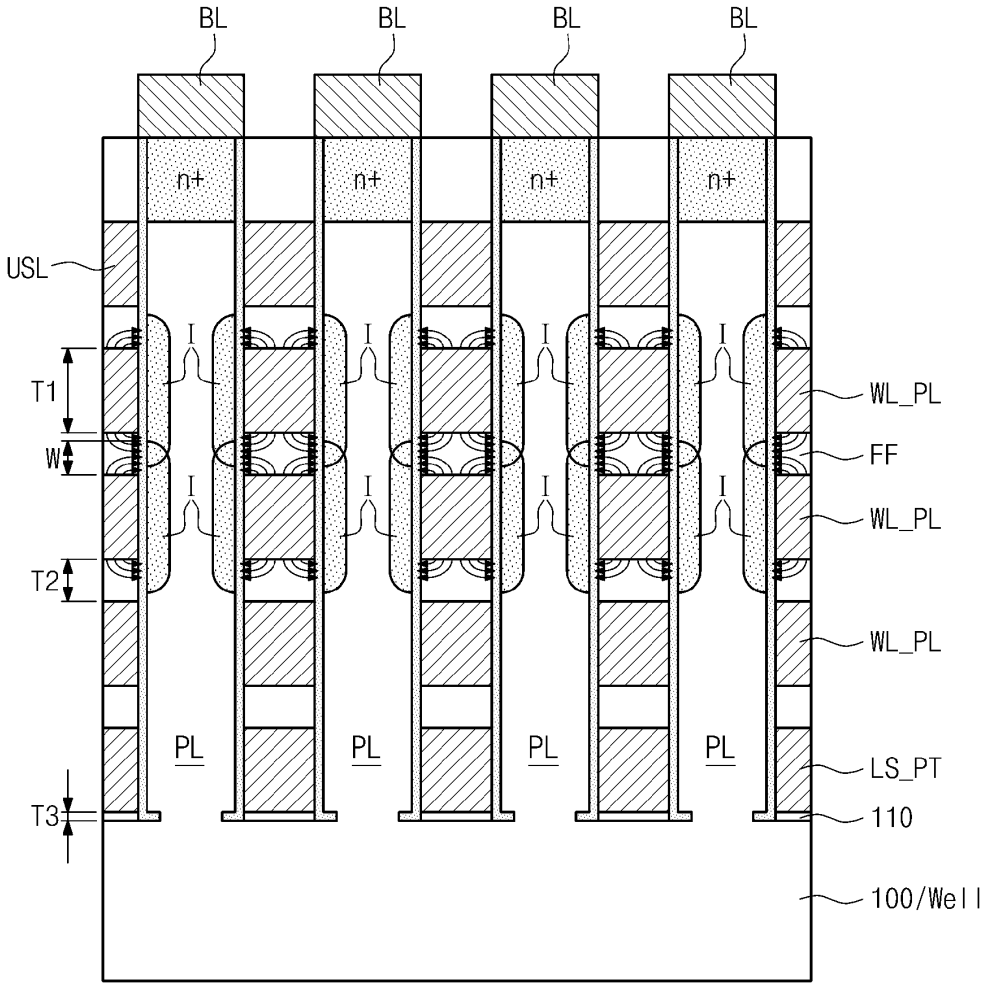

BL
BL
BL
BL
n+
n+
n+
n+
USL
I
T1
W
T2
T3
WL_PL
FF
WL_PL
WL_PL
PL
PL
PL
PL
LS_PT
110
100/Well

Fig. 6

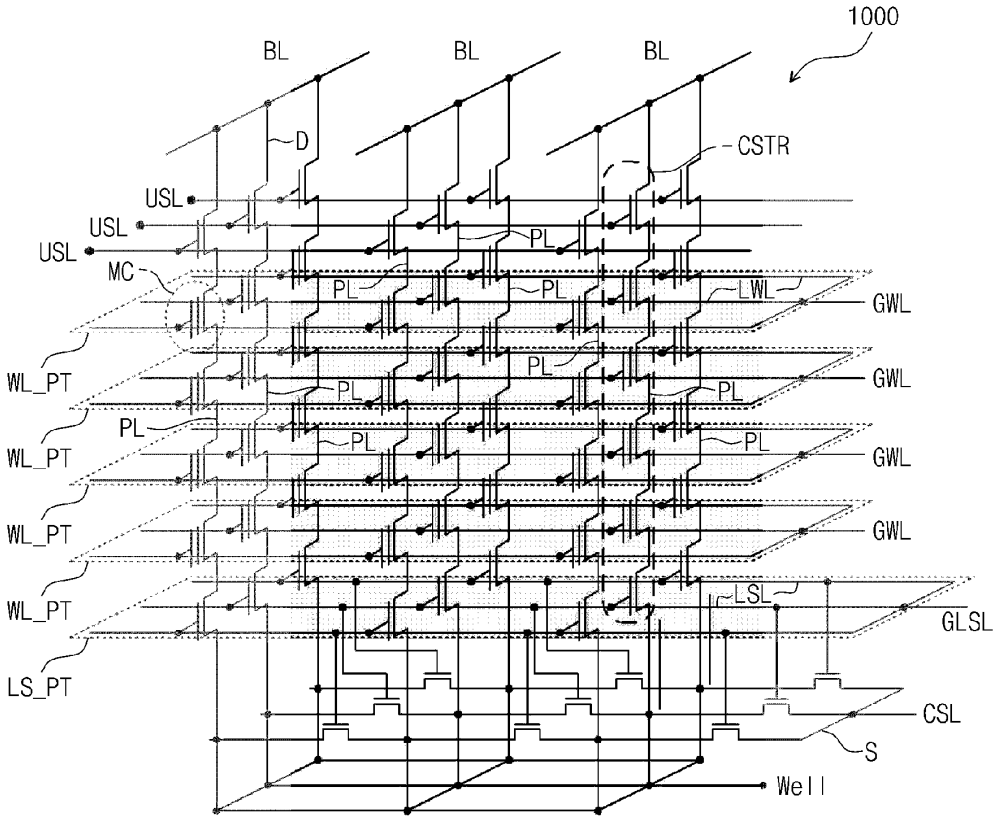

1000
BL
BL
BL
D
CSTR
USL
USL
USL
MC
PL
PL
PL
LWL
GWL
WL_PT
PL
PL
PL
GWL
PL
WL_PT
PL
PL
GWL
WL_PT
GWL
WL_PT
LSL
GLSL
LS_PT
CSL
S
Well

Fig. 7A

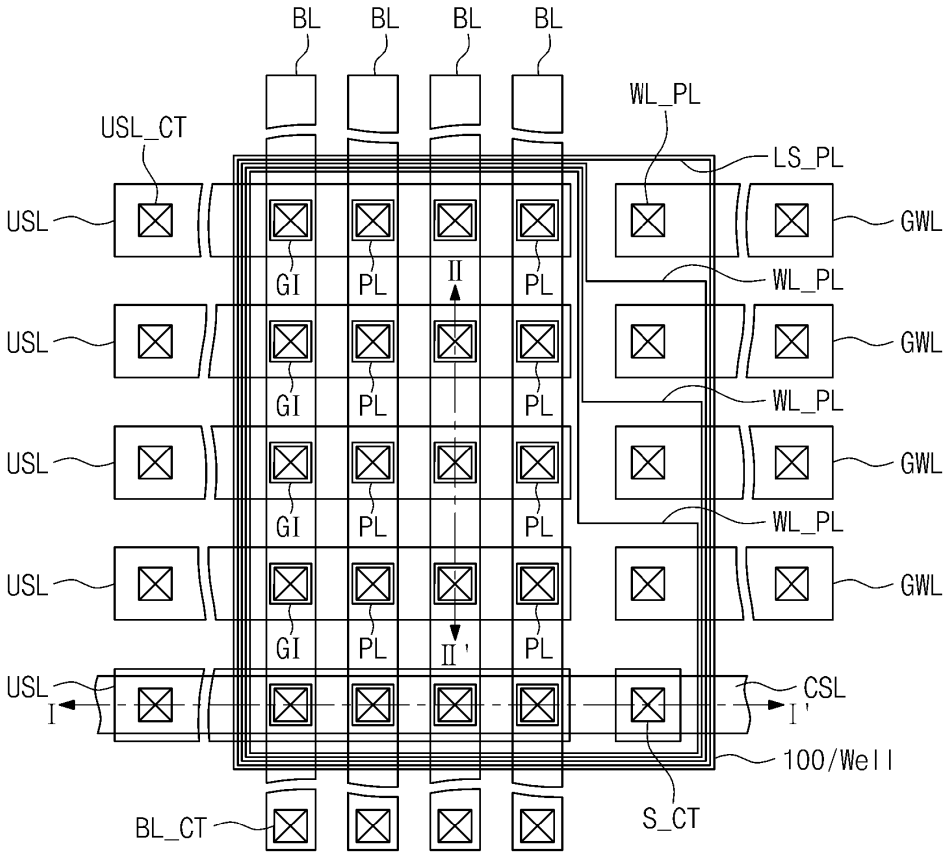

BL
BL
BL
BL
WL_PL
USL_CT
LS_PL
USL
GWL
GI
PL
II
PL
WL_PL
USL
GWL
GI
PL
PL
WL_PL
USL
GWL
GI
PL
PL
WL_PL
USL
GWL
GI
PL
II'
PL
USL
CSL
I
I'
100/Well
BL_CT
S_CT

Fig. 7B

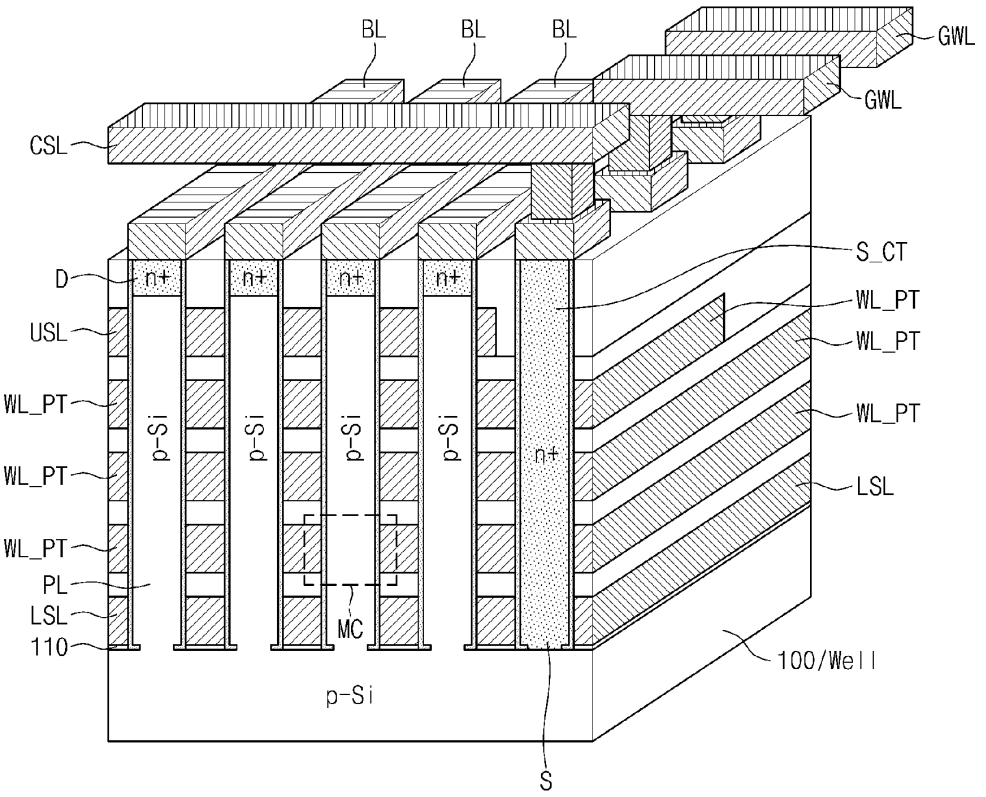

BL
BL
BL
GWL
GWL
CSL
S_CT
D
n+
n+
n+
n+
WL_PT
WL_PT
USL
WL_PT
p-Si
p-Si
p-Si
p-Si
n+
WL_PT
WL_PT
LSL
WL_PT
PL
LSL
MC
110
100/Well
p-Si
S

Fig. 8

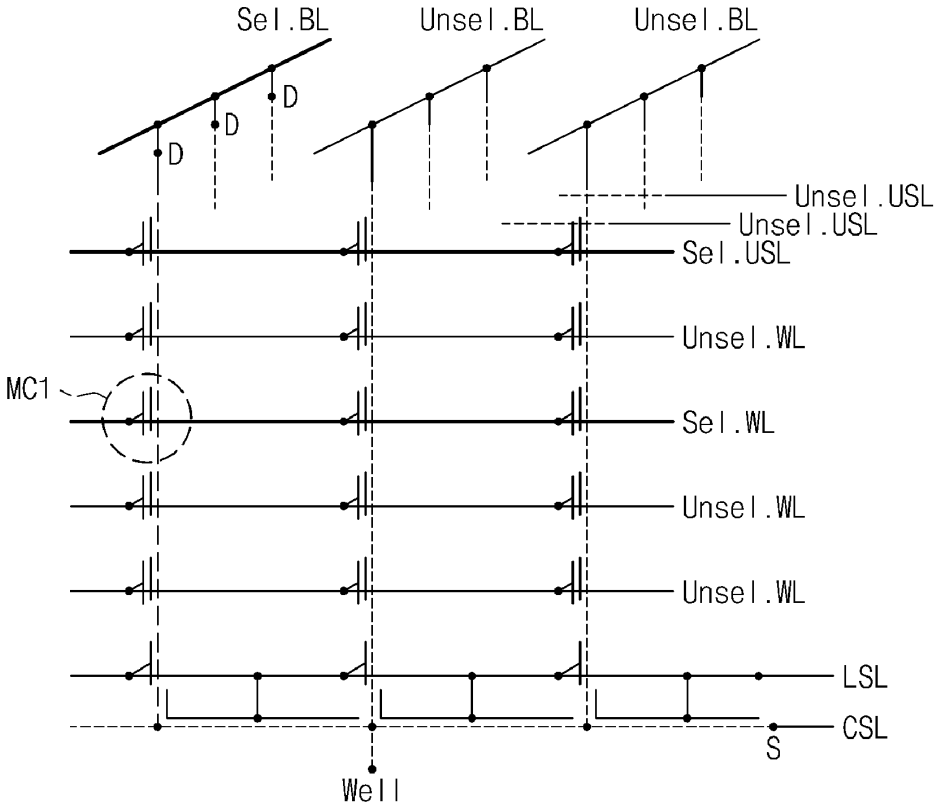

Sel.BL
Unsel.BL
Unsel.BL
D
D
D
Unsel.USL
Unsel.USL
Sel.USL
Unsel.WL
MC1
Sel.WL
Unsel.WL
Unsel.WL
LSL
CSL
S
Well

Fig. 9

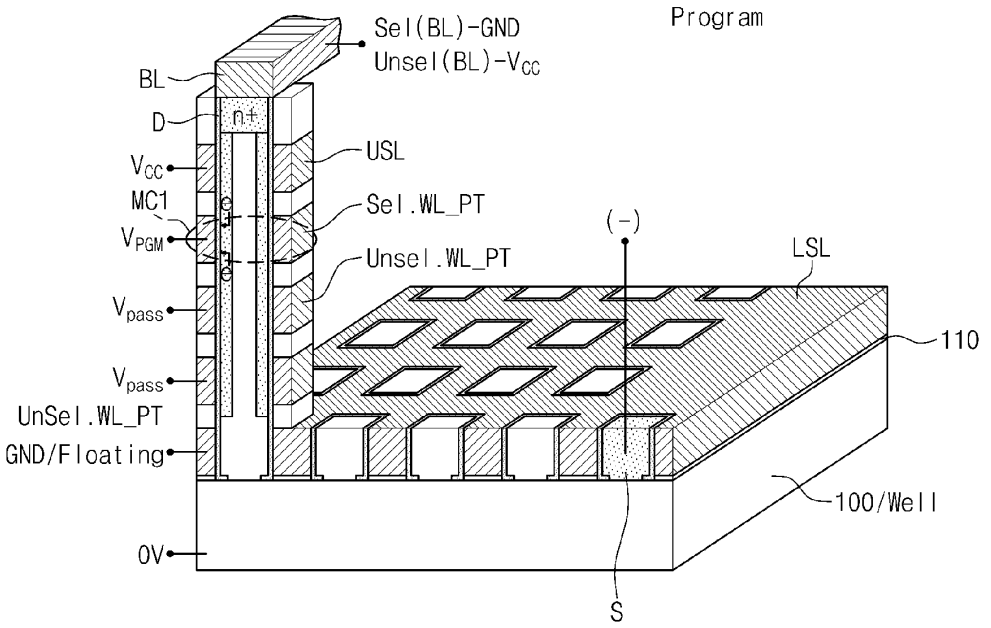

Program
Sel(BL)-GND
Unsel(BL)-V_{CC}
BL
D
n+
USL
V_{CC}
MC1
Sel.WL_PT
V_{PGM}
(-)
Unsel.WL_PT
LSL
V_{pass}
110
V_{pass}
UnSel.WL_PT
GND/Floating
100/Well
0V
S

Fig. 10

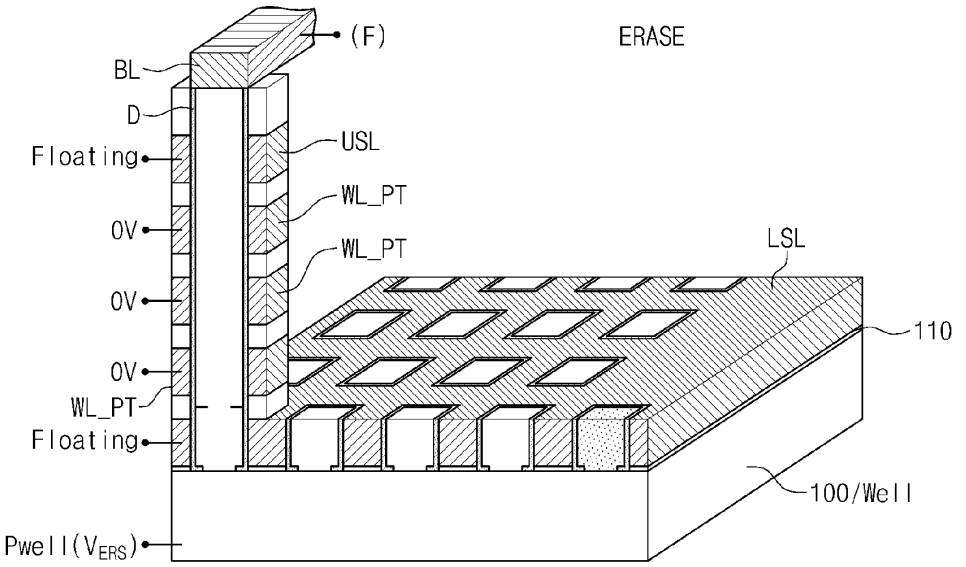

(F)
ERASE
BL
D
Floating
USL
WL_PT
0V
WL_PT
LSL
0V
110
0V
WL_PT
Floating
100/Well
Pwell(V_{ERS})

Fig. 11

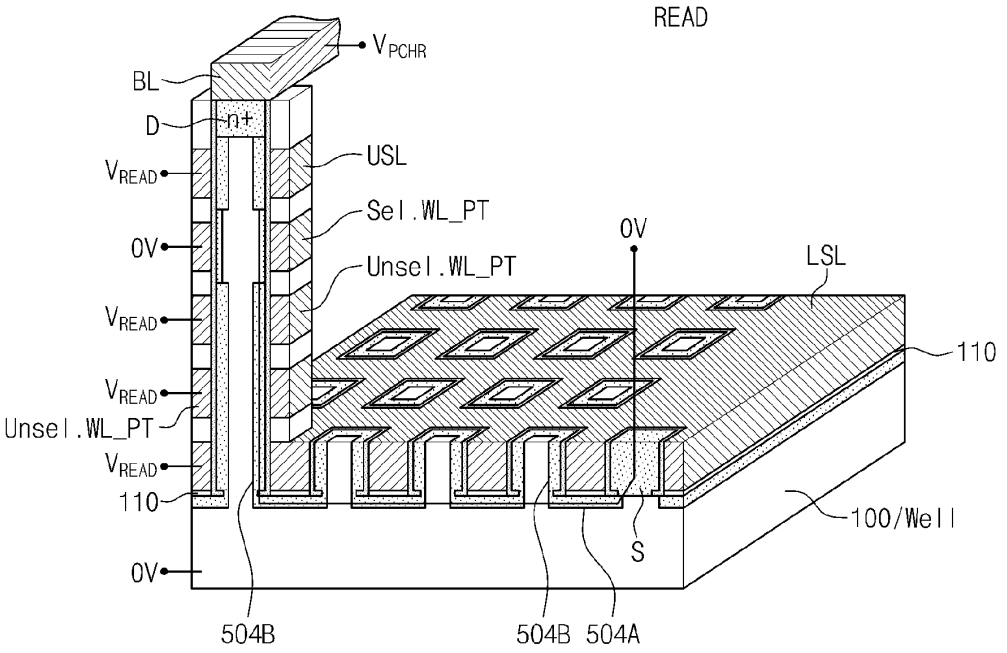

READ
V_{PCHR}
BL
D
n+
USL
V_{READ}
Sel.WL_PT
0V
Unsel.WL_PT
LSL
V_{READ}
110
V_{READ}
Unsel.WL_PT
V_{READ}
110
100/Well
S
0V
504B
504B
504A

Fig. 12A

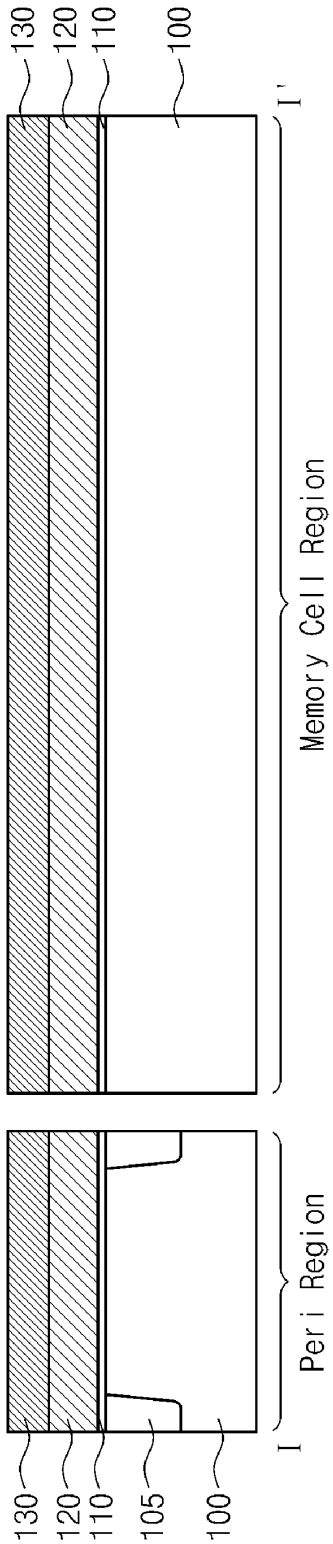

130
120
110
105
100
I
Peri Region
130
120
110
100
I'
Memory Cell Region

Fig. 12B

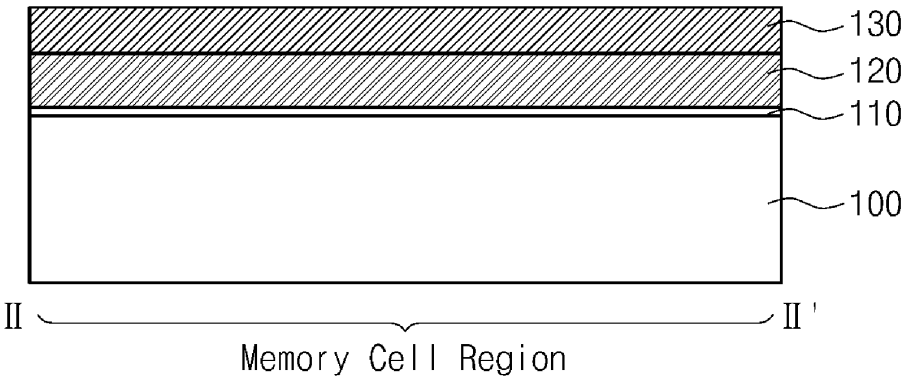


Fig. 13A

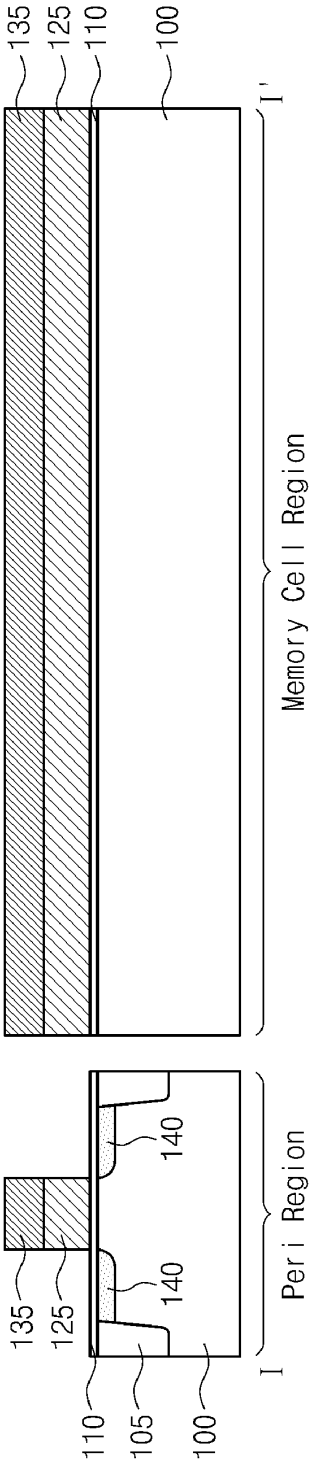

135
125
110
100
I'
Memory Cell Region
135
125
110
105
100
140
140
I
Peri Region

Fig. 13B

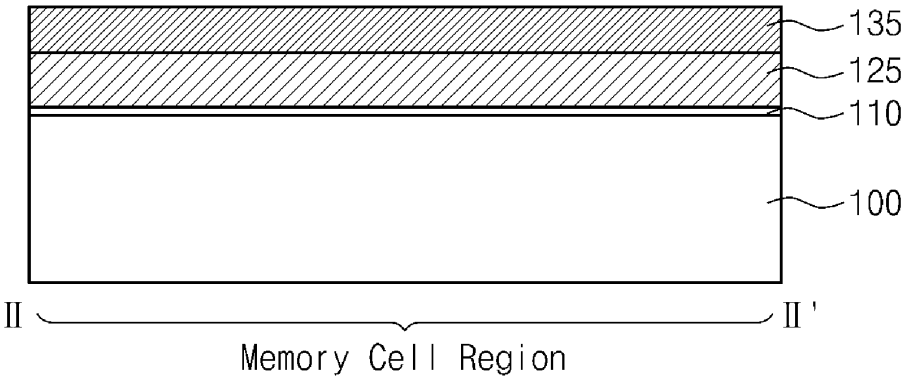


Fig. 14A

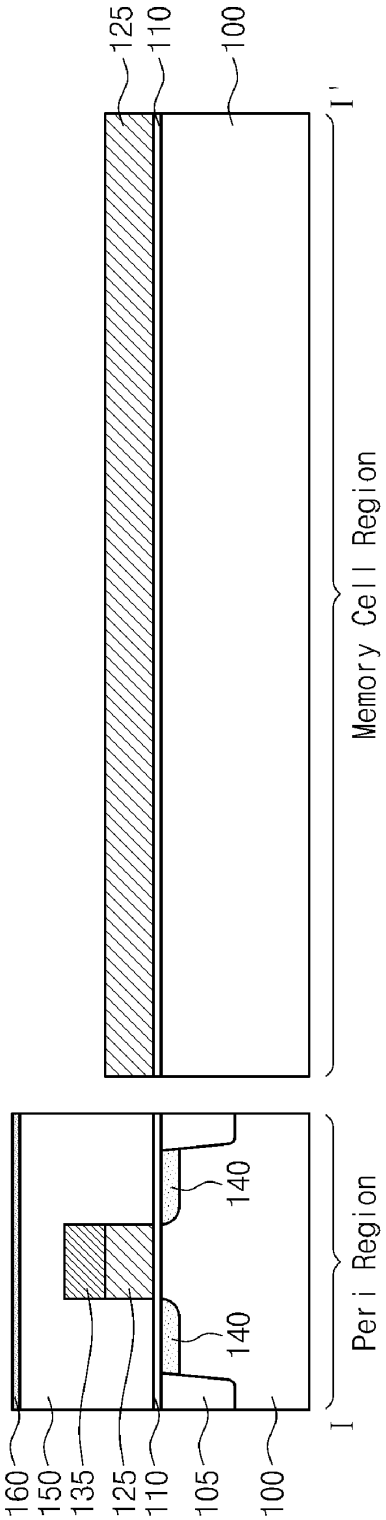

125
110
100
I'
Memory Cell Region
140
140
Peri Region
I
160
150
135
125
110
105
100

Fig. 14B

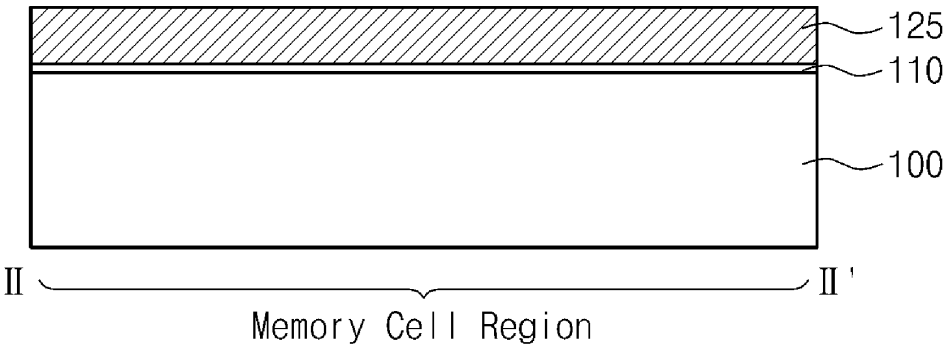


Fig. 15A

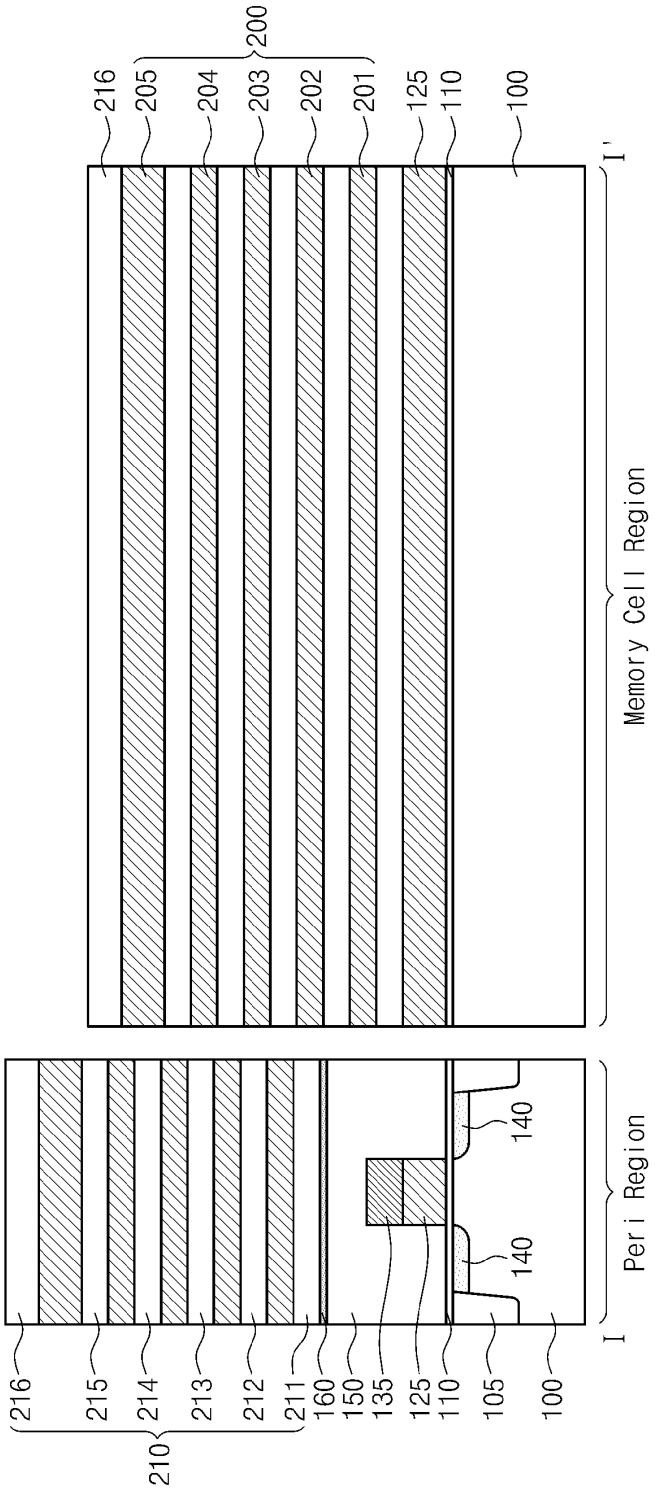

216
205
204
203
202
201
200
125
110
100
I'
Memory Cell Region
216
215
214
213
212
211
210
160
150
135
125
110
105
100
140
140
I
Peri Region

Fig. 15B

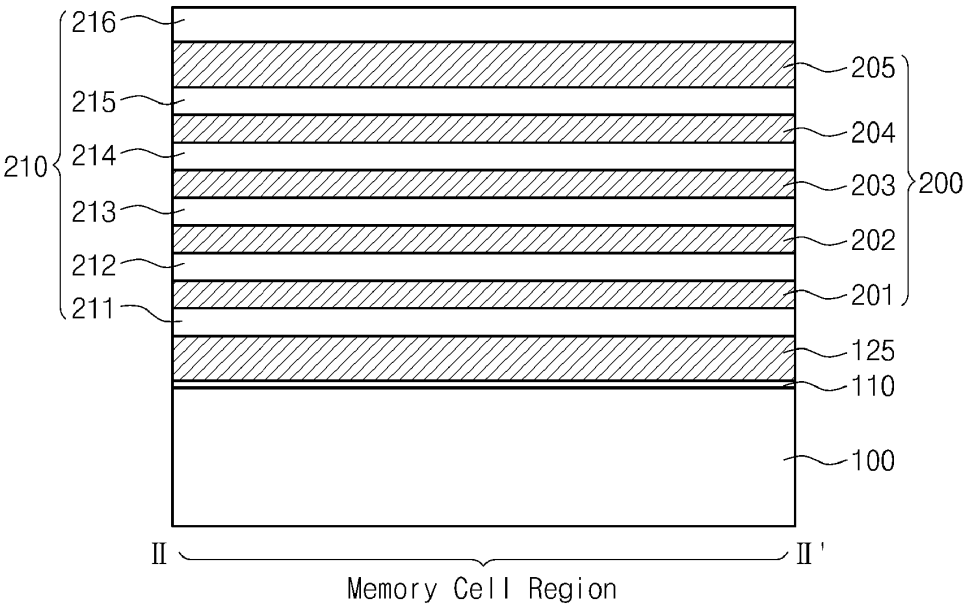

216
215
214
213
212
211
210
205
204
203
202
201
200
125
110
100
II
II'
Memory Cell Region

Fig. 16A

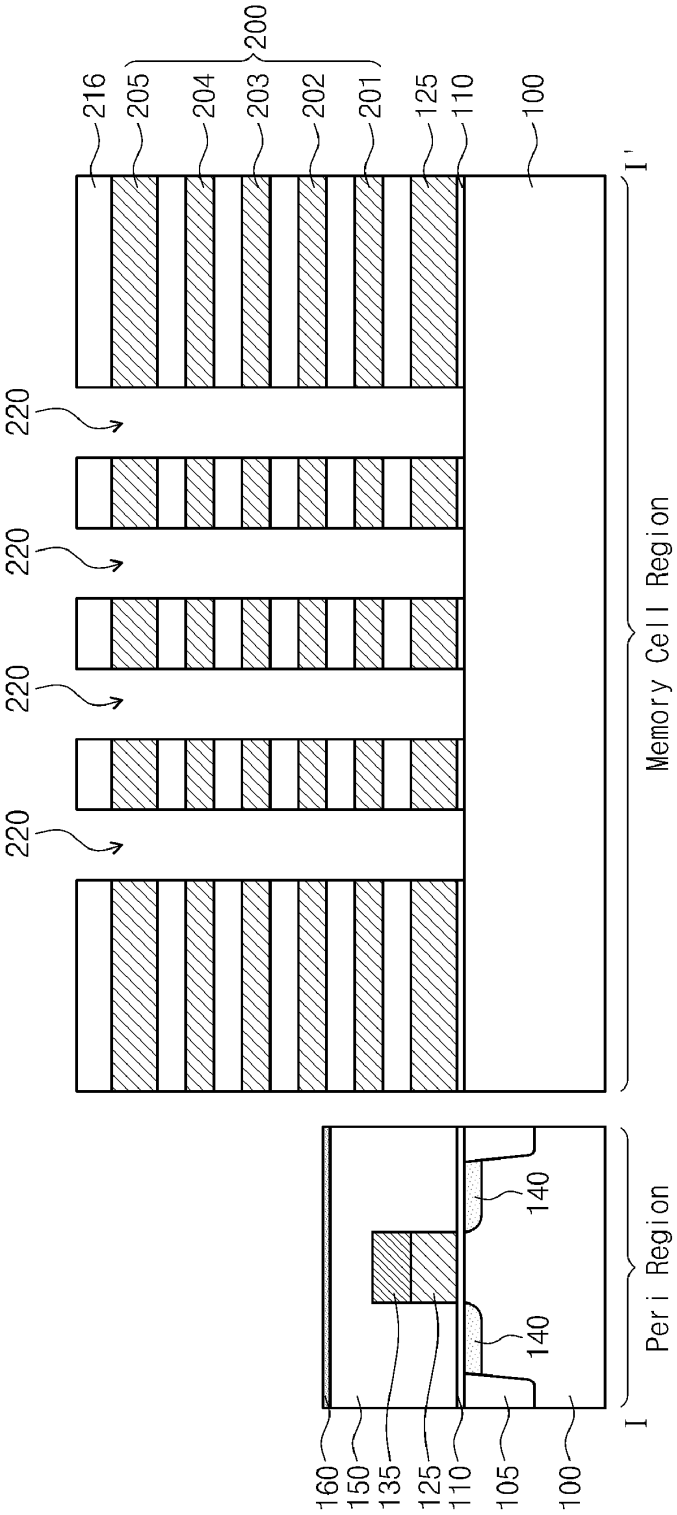

200
216
205
204
203
202
201
125
110
100
220
220
220
220
I'
Memory Cell Region
140
140
Peri Region
I
160
150
135
125
110
105
100

Fig. 16B

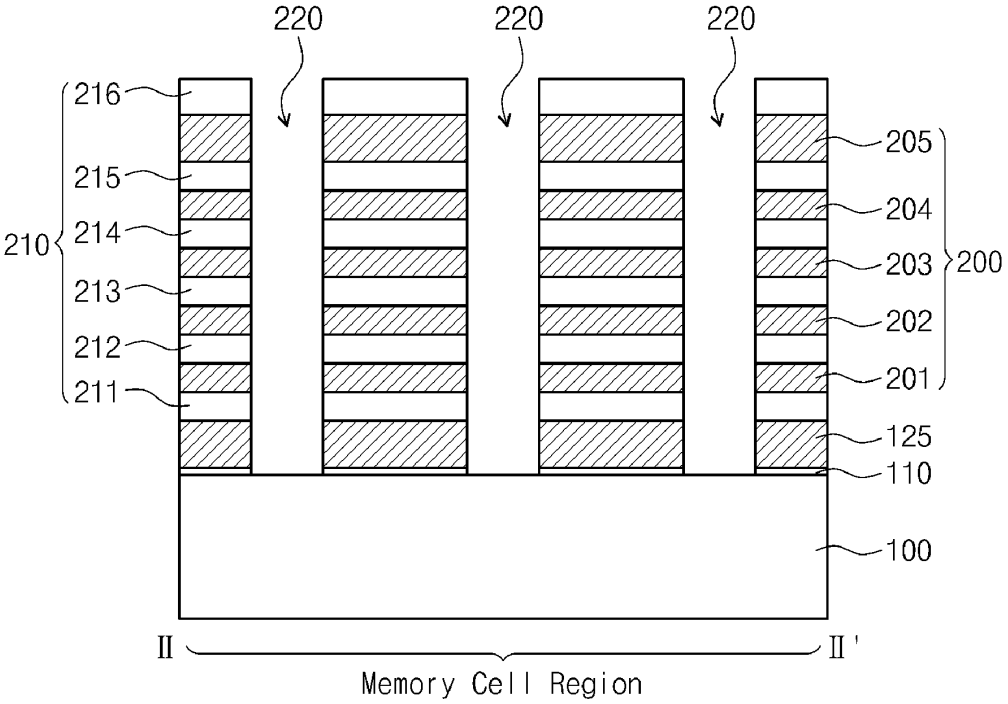

220
220
220
216
215
214
213
212
211
210
205
204
203
202
201
200
125
110
100
II
II'
Memory Cell Region

Fig. 17A

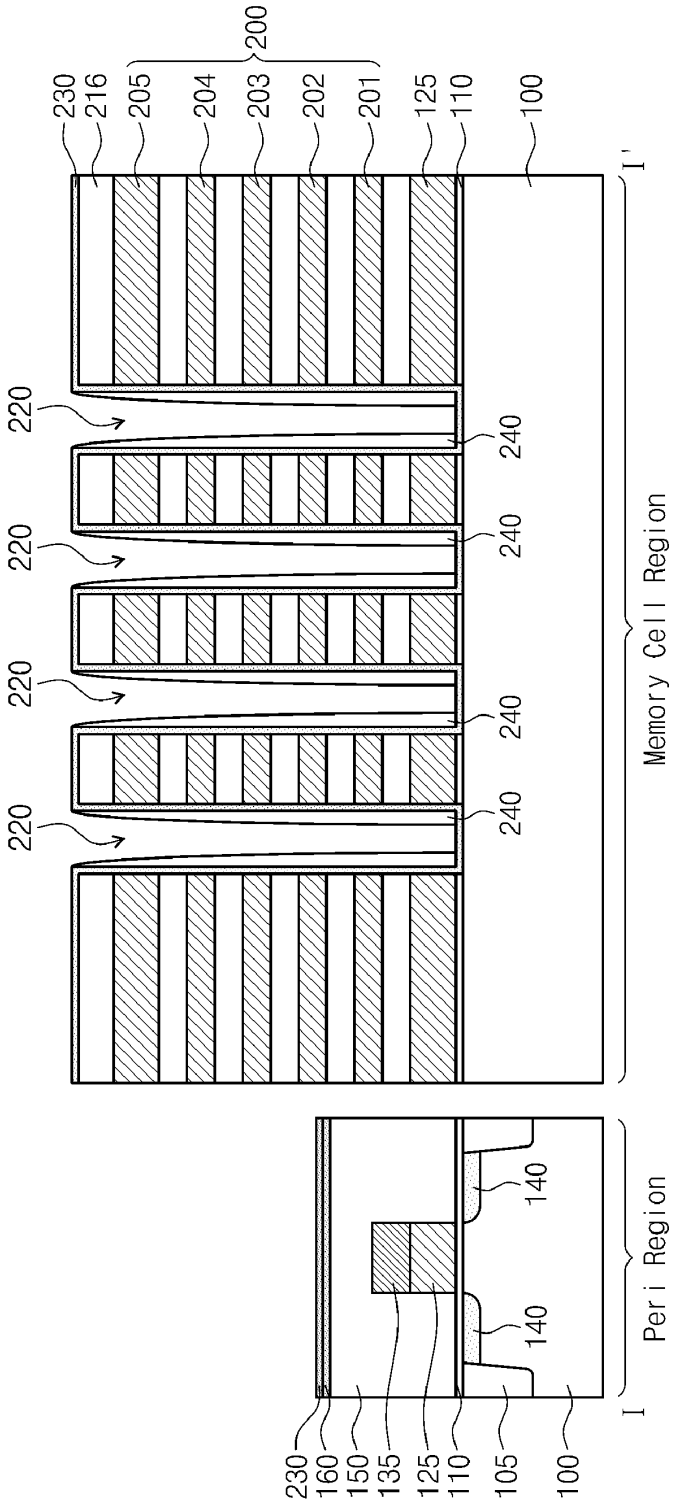

200
230
216
205
204
203
202
201
125
110
100
I'
220
240
Memory Cell Region
140
Peri Region
I
230
160
150
135
125
110
105
100

Fig. 17B

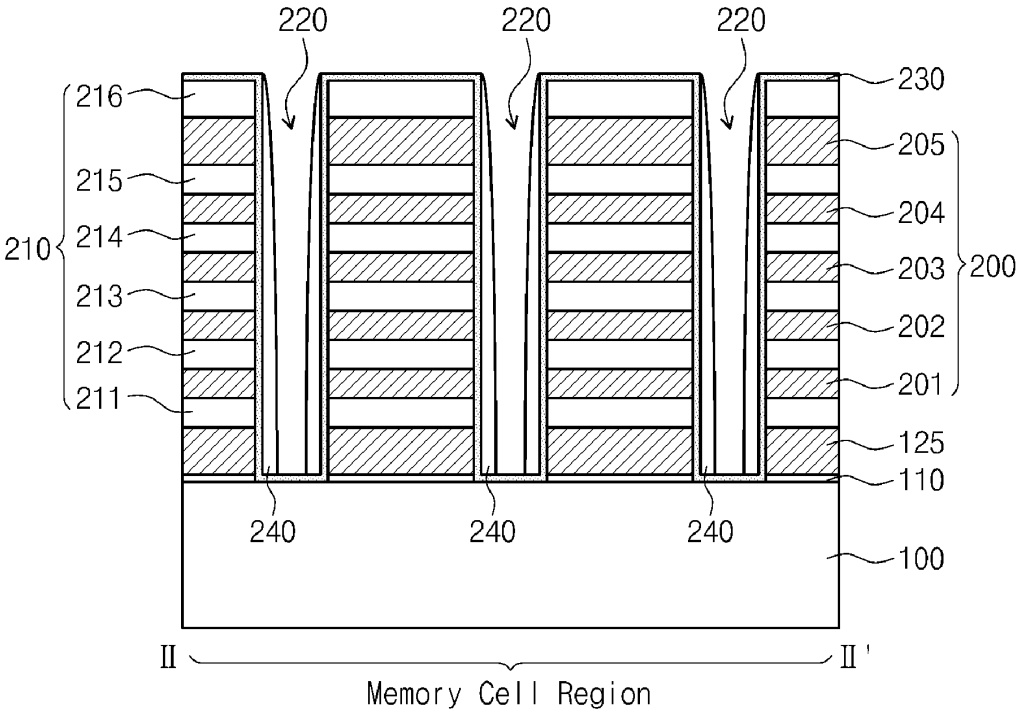

220
220
220
230
216
205
215
204
210
214
203
200
213
202
212
201
211
125
110
240
240
240
100
II
II'
Memory Cell Region

Fig. 18A

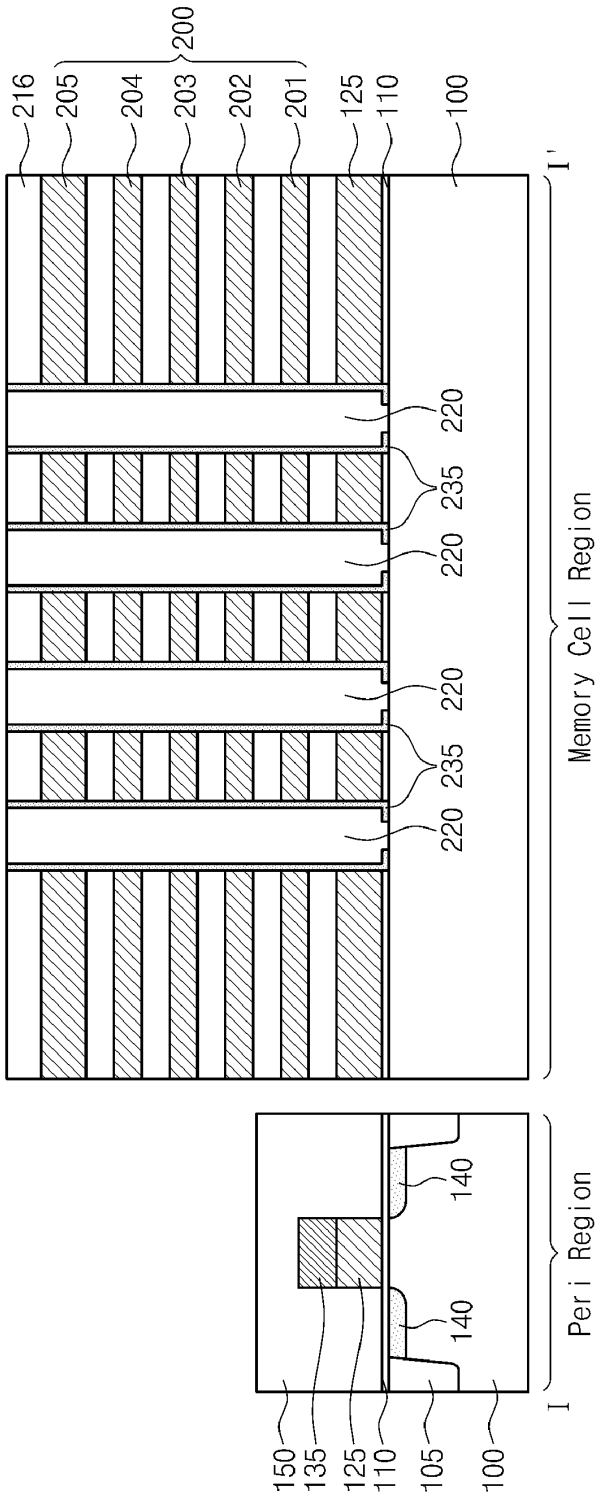

216
205
204
203
202
201
200
125
110
100
I'
220
235
220
220
235
220
Memory Cell Region
140
140
Peri Region
I
150
135
125
110
105
100

Fig. 18B

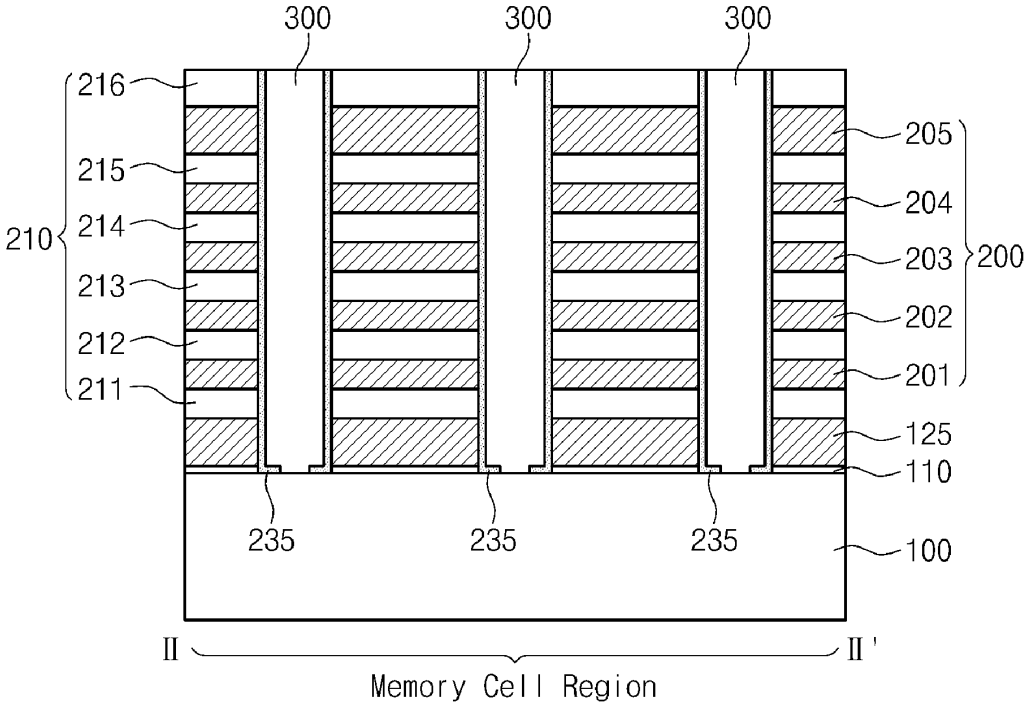

300
300
300
216
215
214
213
212
211
210
205
204
203
202
201
200
125
110
235
235
235
100
II
II'
Memory Cell Region

Fig. 19A

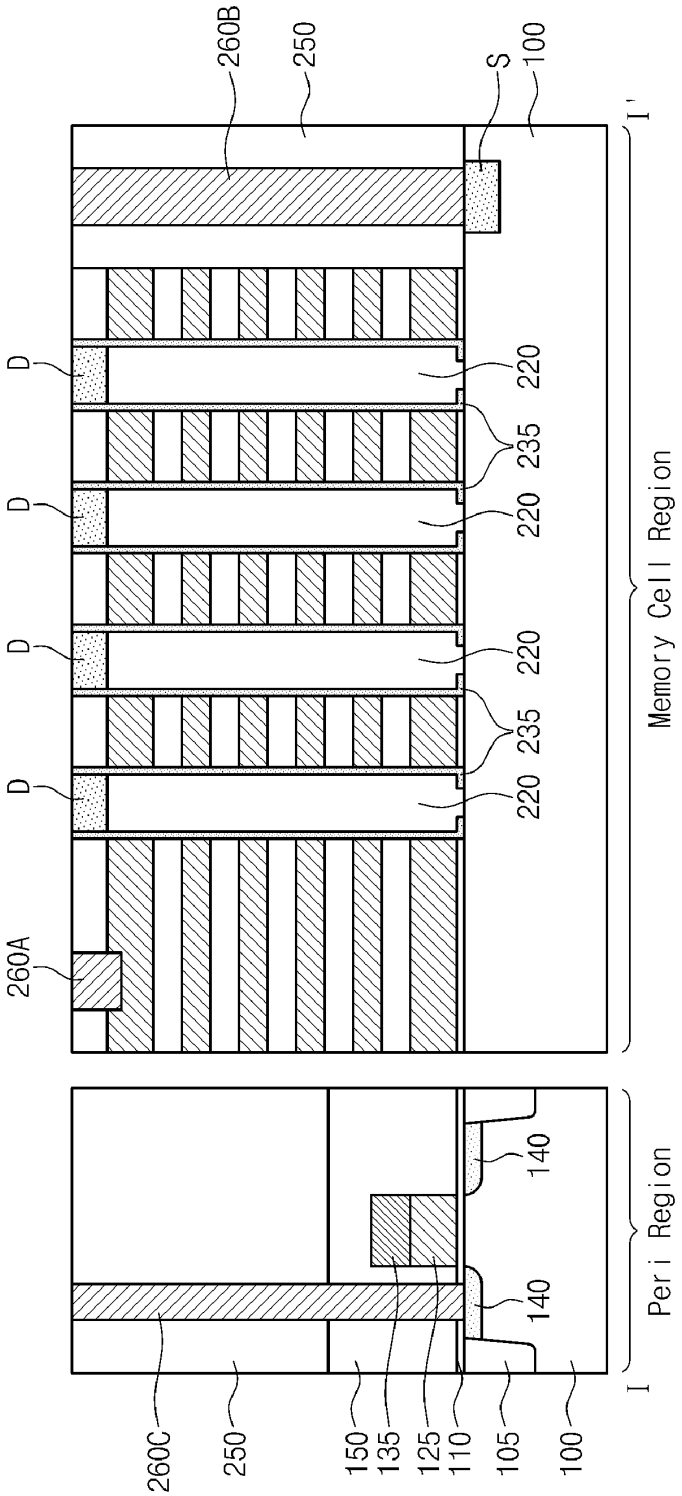

260B
250
S
100
I'
D
D
D
D
220
235
220
220
235
220
260A
Memory Cell Region
140
140
Peri Region
I
260C
250
150
135
125
110
105
100

Fig. 19B

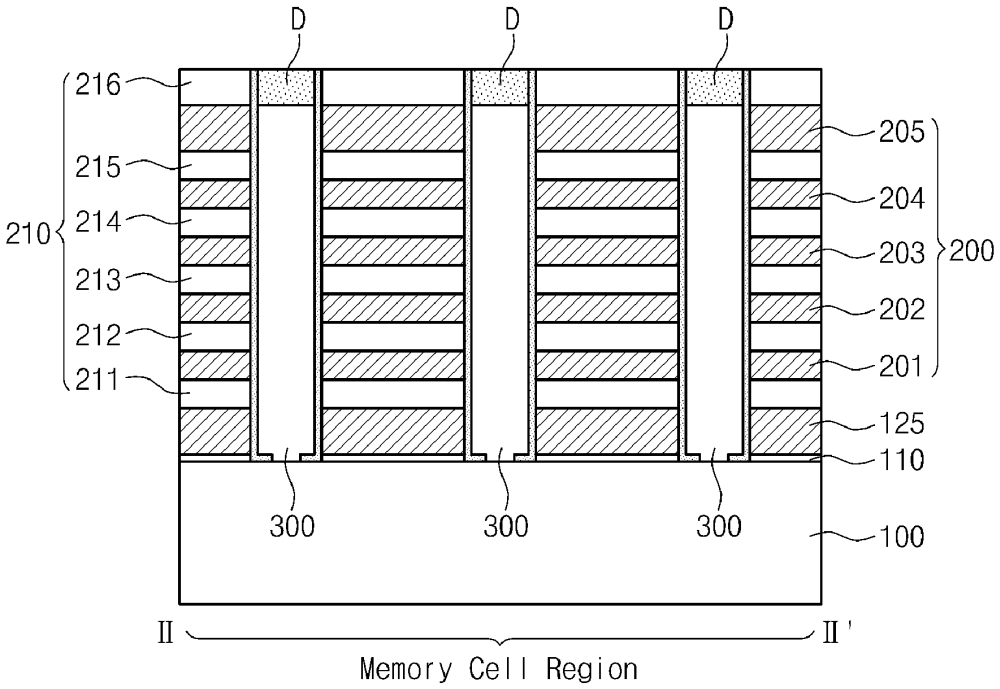

D
D
D
216
215
214
213
212
211
210
205
204
203
202
201
200
125
110
300
300
300
100
II
II'
Memory Cell Region

Fig. 20A

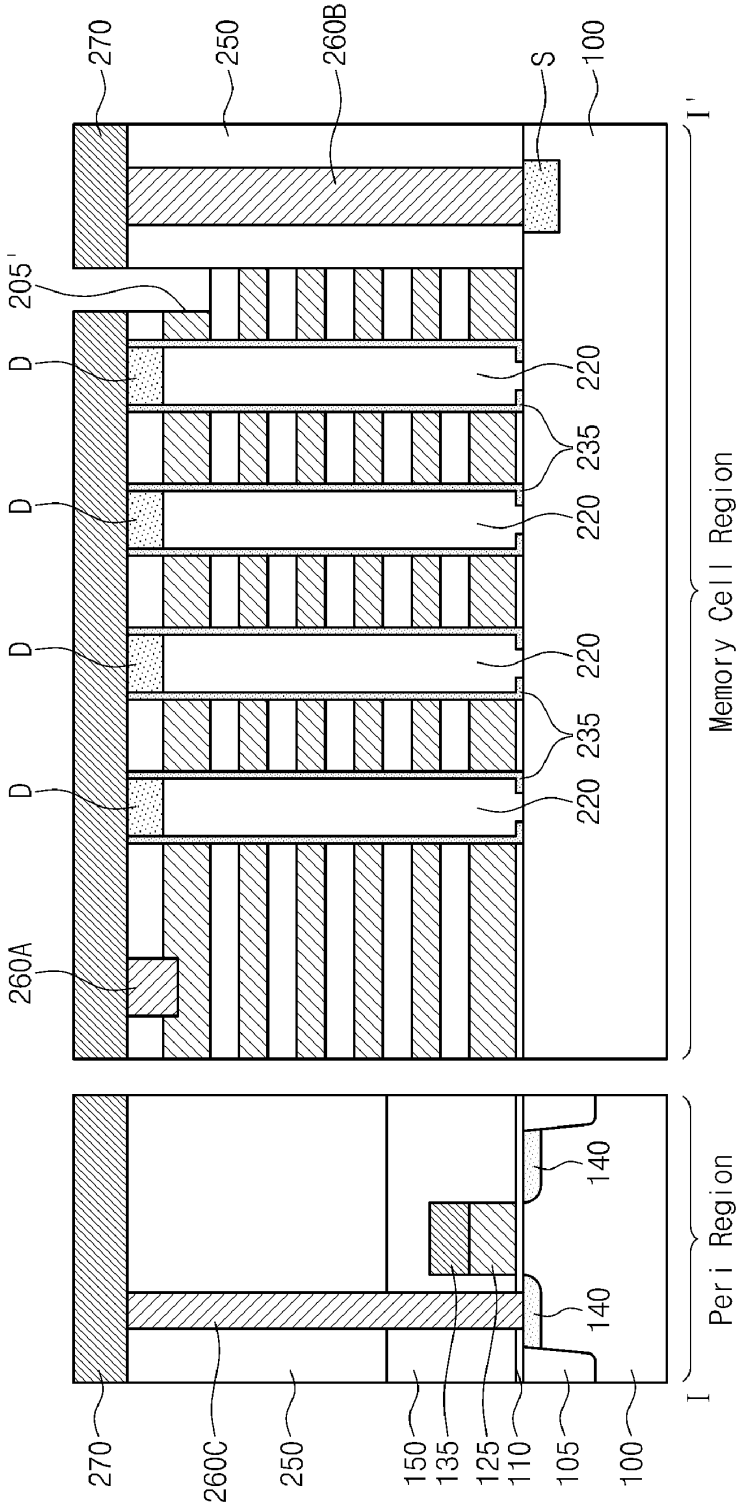

270
250
260B
S
100
I'
205'
D
D
D
D
220
235
220
220
235
220
260A
Memory Cell Region
140
140
Peri Region
I
270
260C
250
150
135
125
110
105
100

Fig. 20B

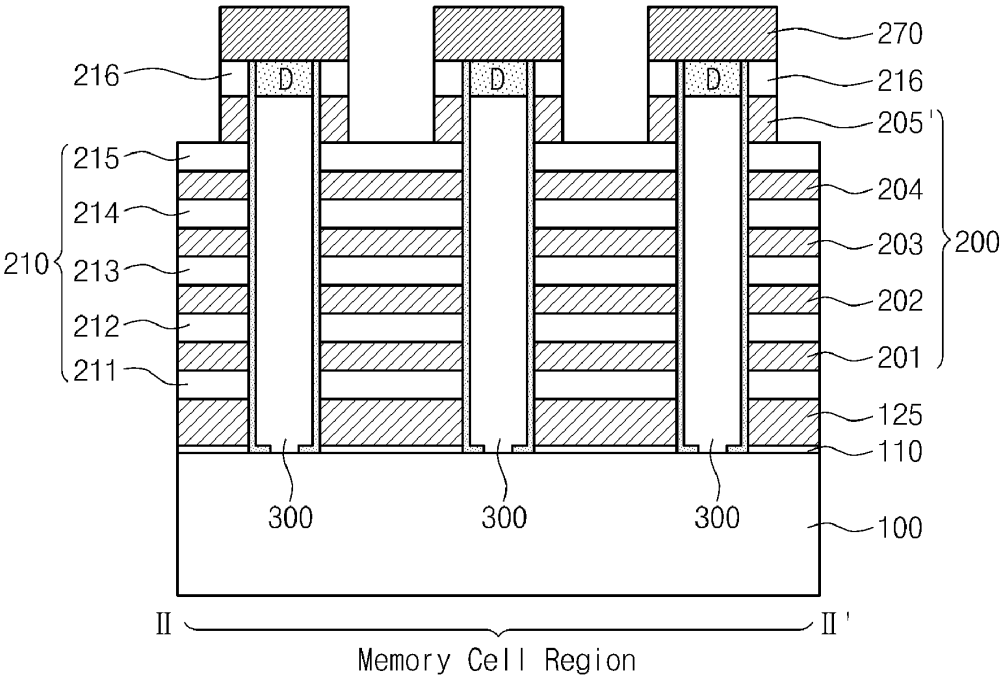

270
216
D
D
D
216
205'
215
204
214
203
200
210
213
202
212
201
211
125
110
300
300
300
100
II
II'
Memory Cell Region

Fig. 21A

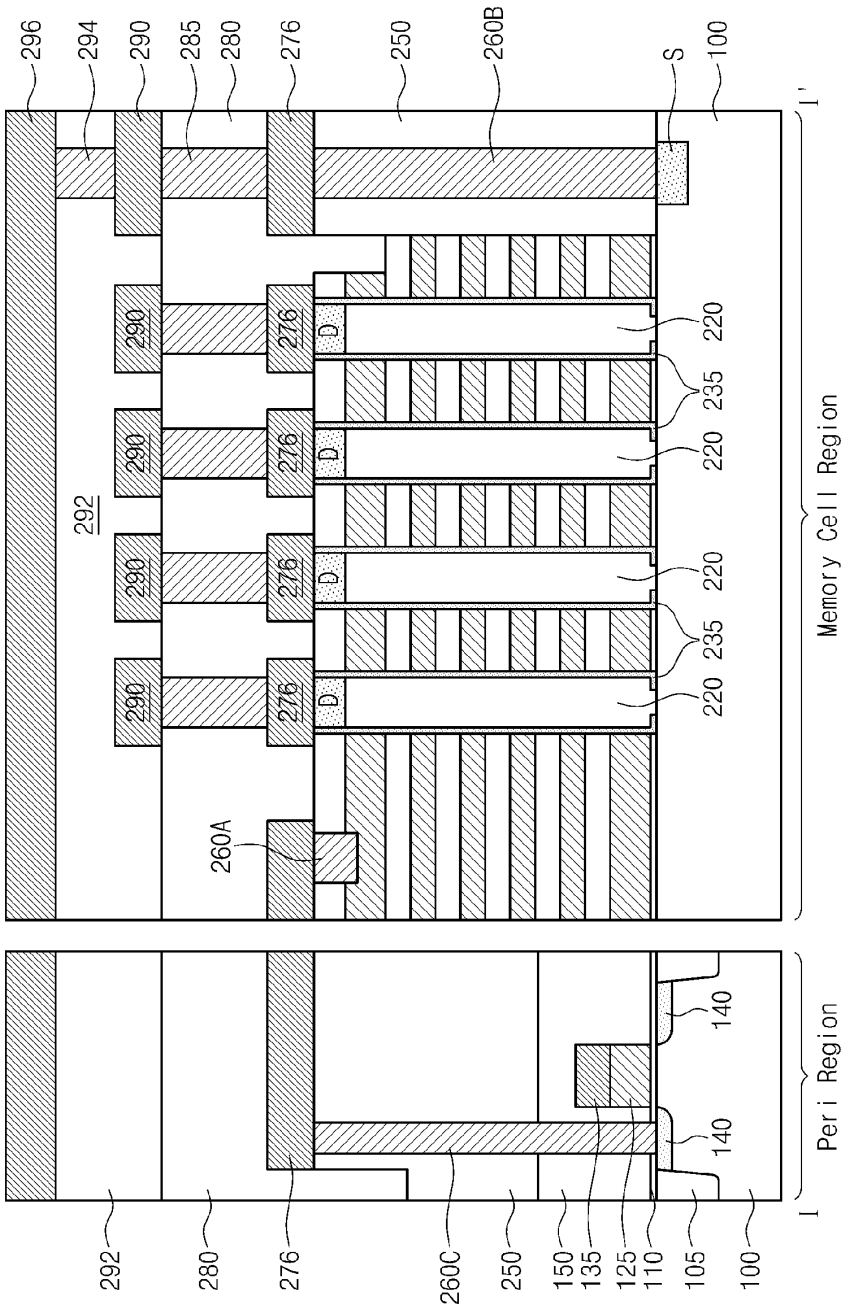

296
294
290
285
280
276
250
260B
S
100
I'
290
276
D
220
235
292
260A
Memory Cell Region
140
Peri Region
I
292
280
276
260C
250
150
135
125
110
105
100

Fig. 21B

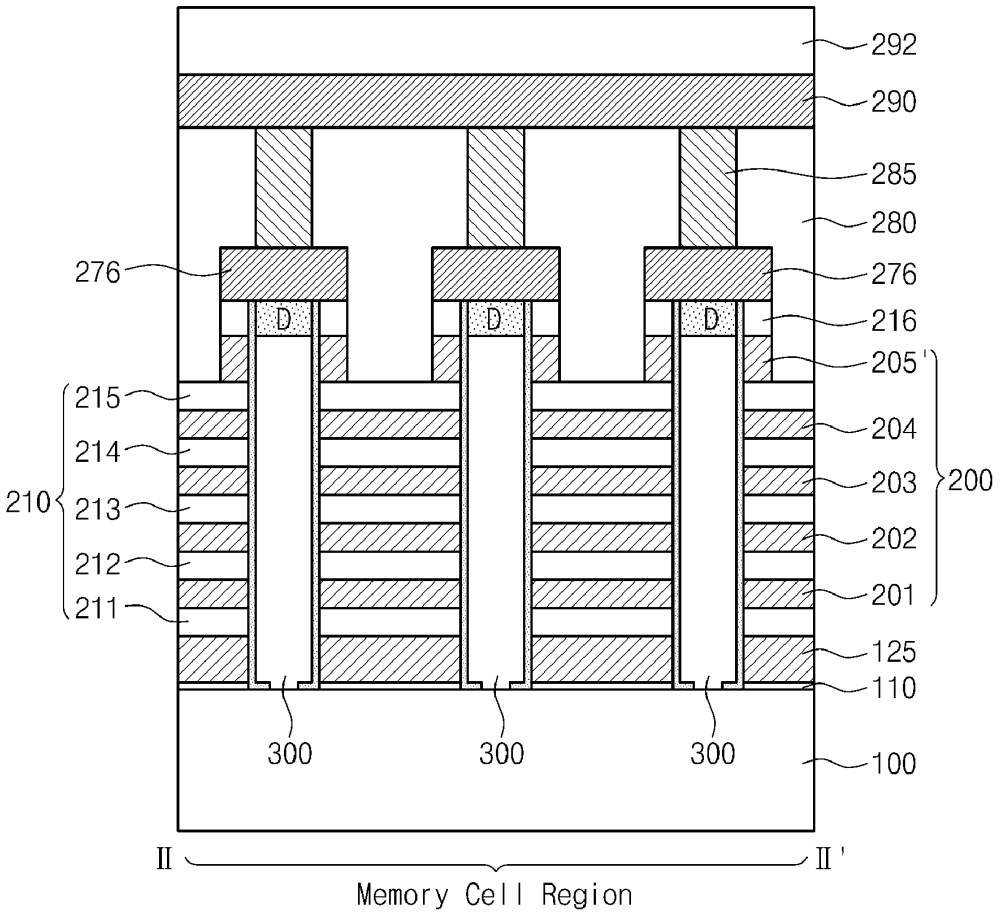

292
290
285
280
276
276
D
D
D
216
205'
215
214
210
213
212
211
204
203
200
202
201
125
110
300
300
300
100
II
II'
Memory Cell Region

Fig. 22

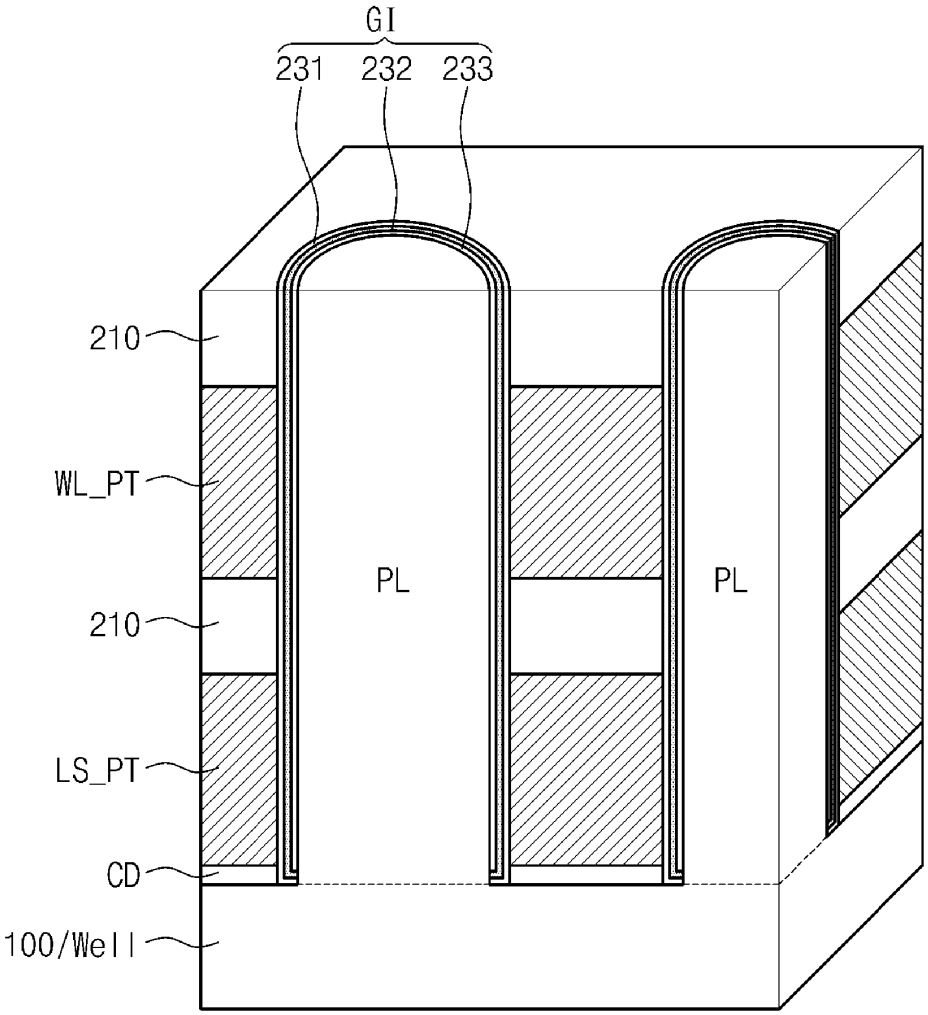


Fig. 23

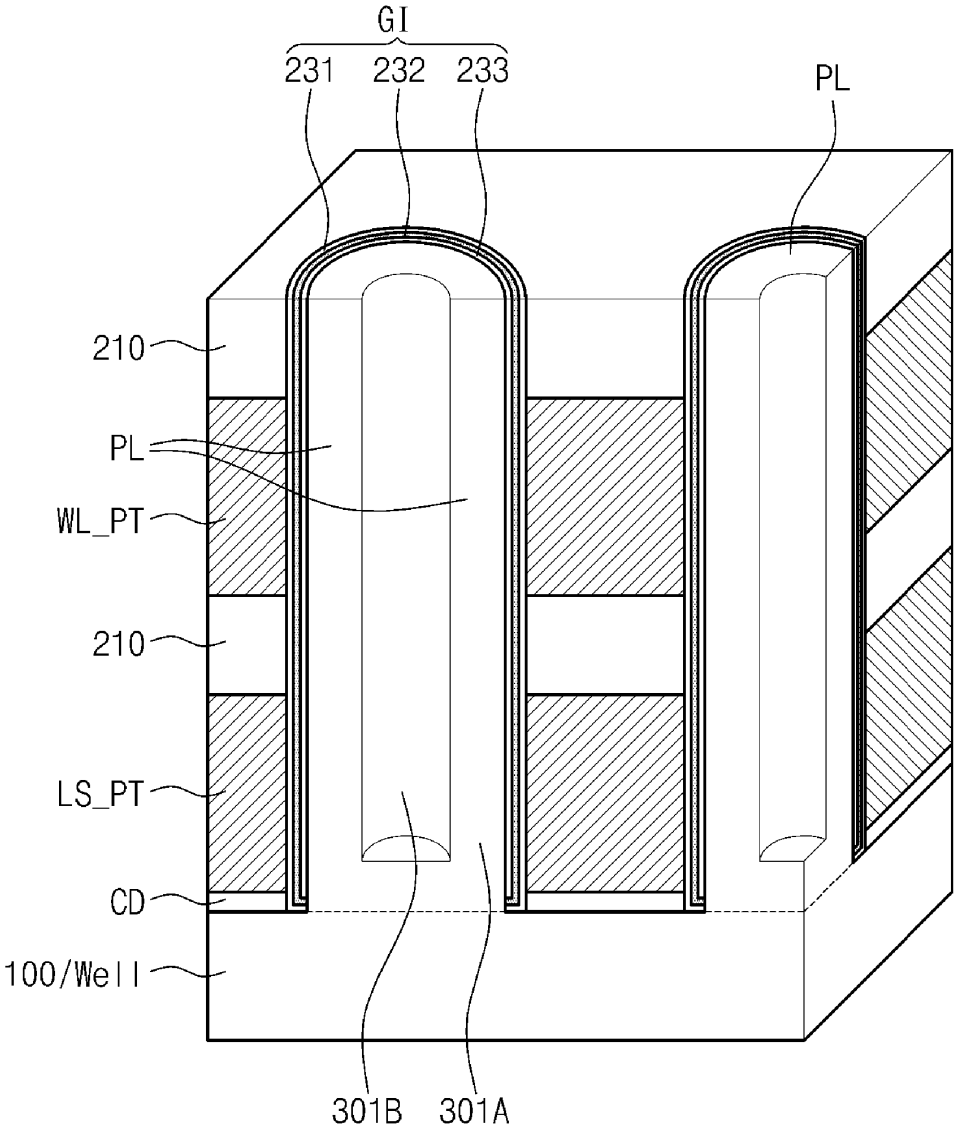


Fig. 24

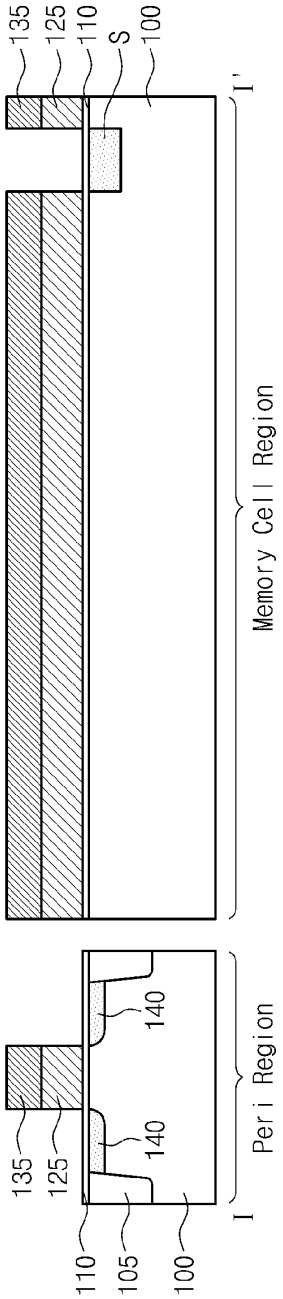

135
125
110
S
100
I'
Memory Cell Region
135
125
140
140
110
105
100
I
Peri Region

Fig. 25

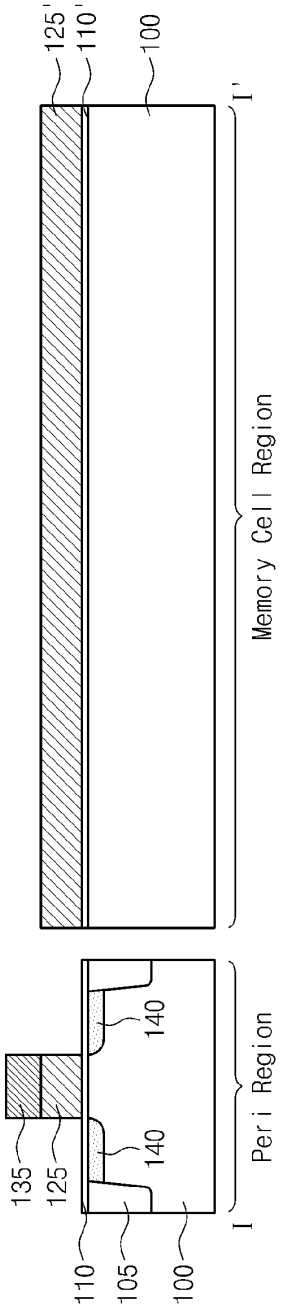

125'
110'
100
I'
Memory Cell Region
135
125
140
140
110
105
100
I
Peri Region

Fig. 26

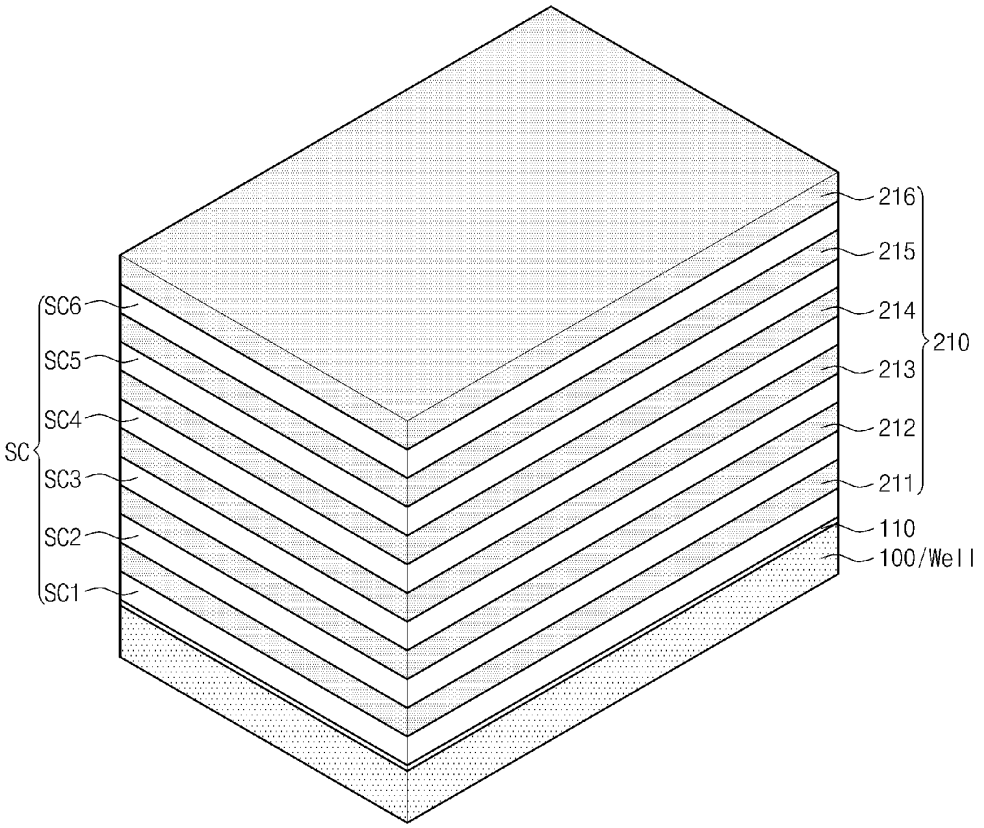

216
215
214
213
212
211
210
110
100/Well
SC6
SC5
SC4
SC3
SC2
SC1
SC

Fig. 27

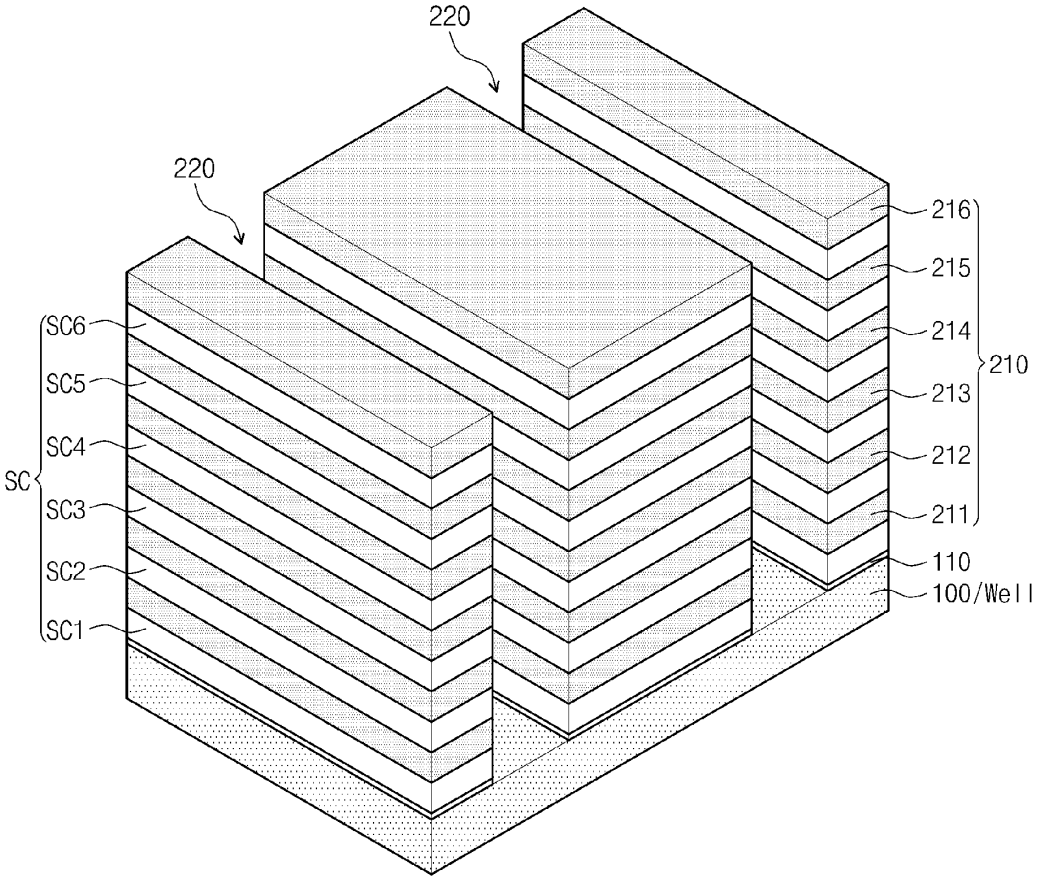

220
220
SC6
SC5
SC4
SC3
SC2
SC1
SC
216
215
214
213
212
211
210
110
100/Well

Fig. 28

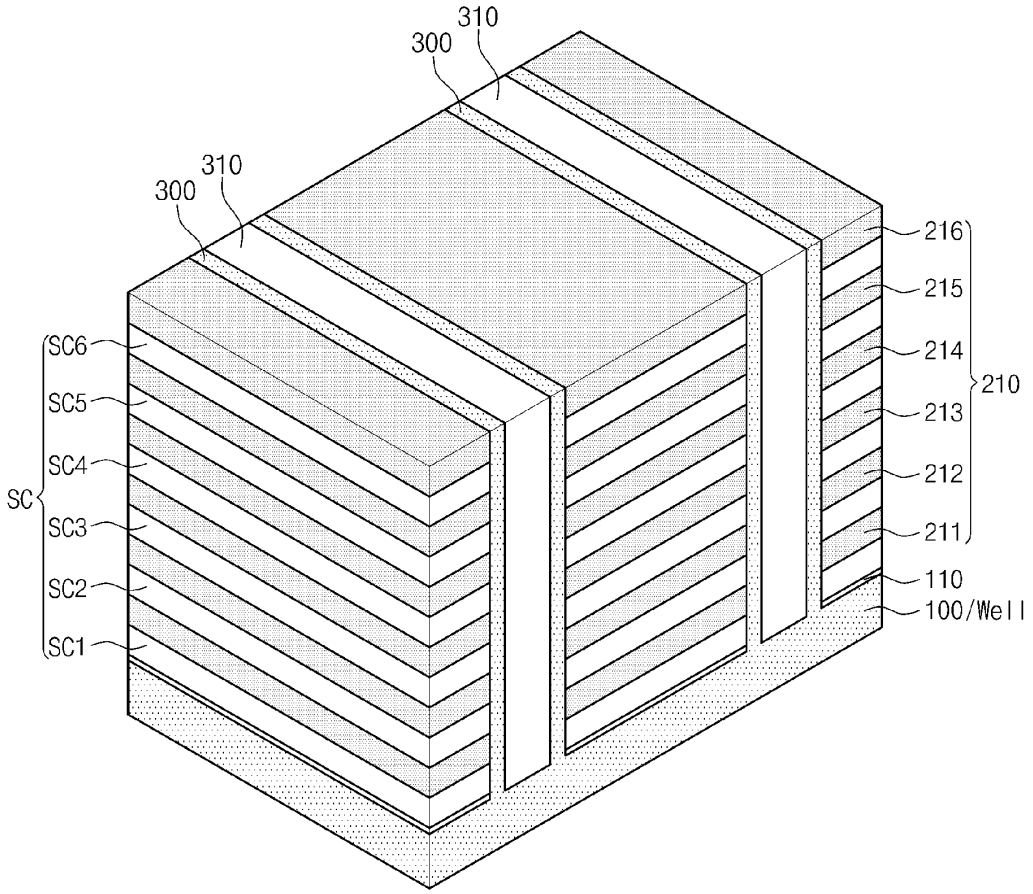

310
300
310
300
SC6
SC5
SC4
SC
SC3
SC2
SC1
216
215
214
210
213
212
211
110
100/Well

Fig. 29

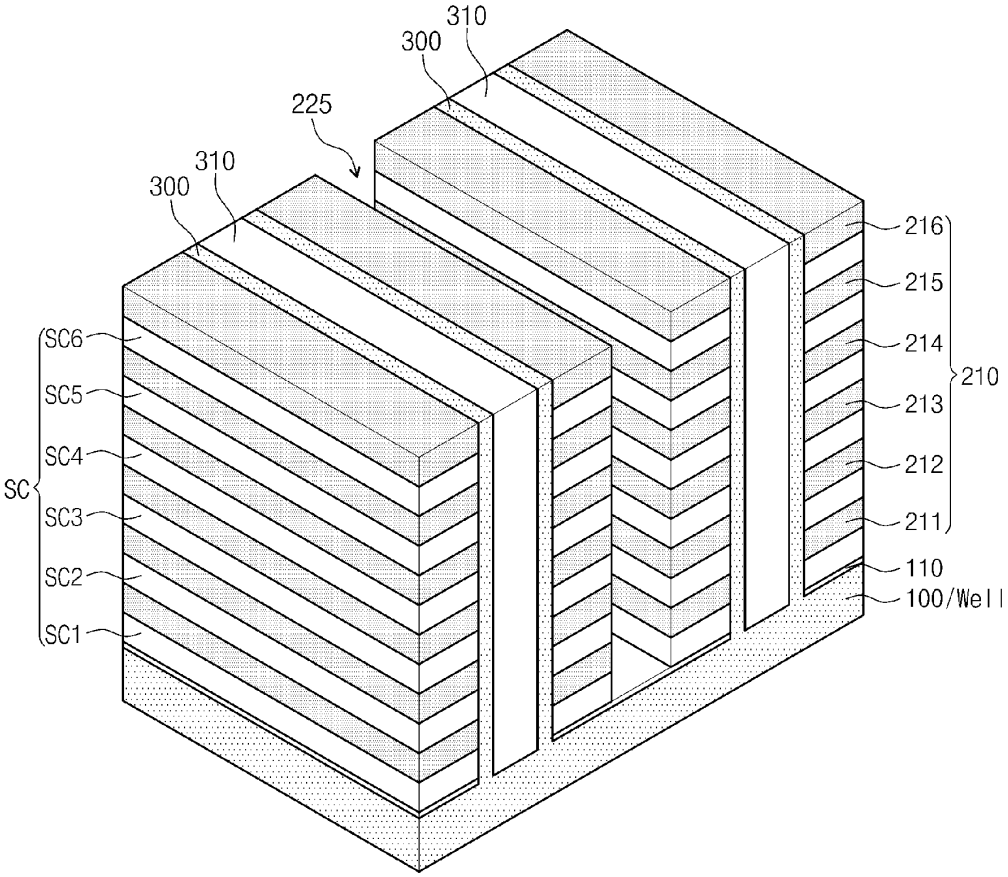

310
300
225
310
300
216
215
214
210
213
212
211
110
100/Well
SC6
SC5
SC4
SC
SC3
SC2
SC1

Fig. 30

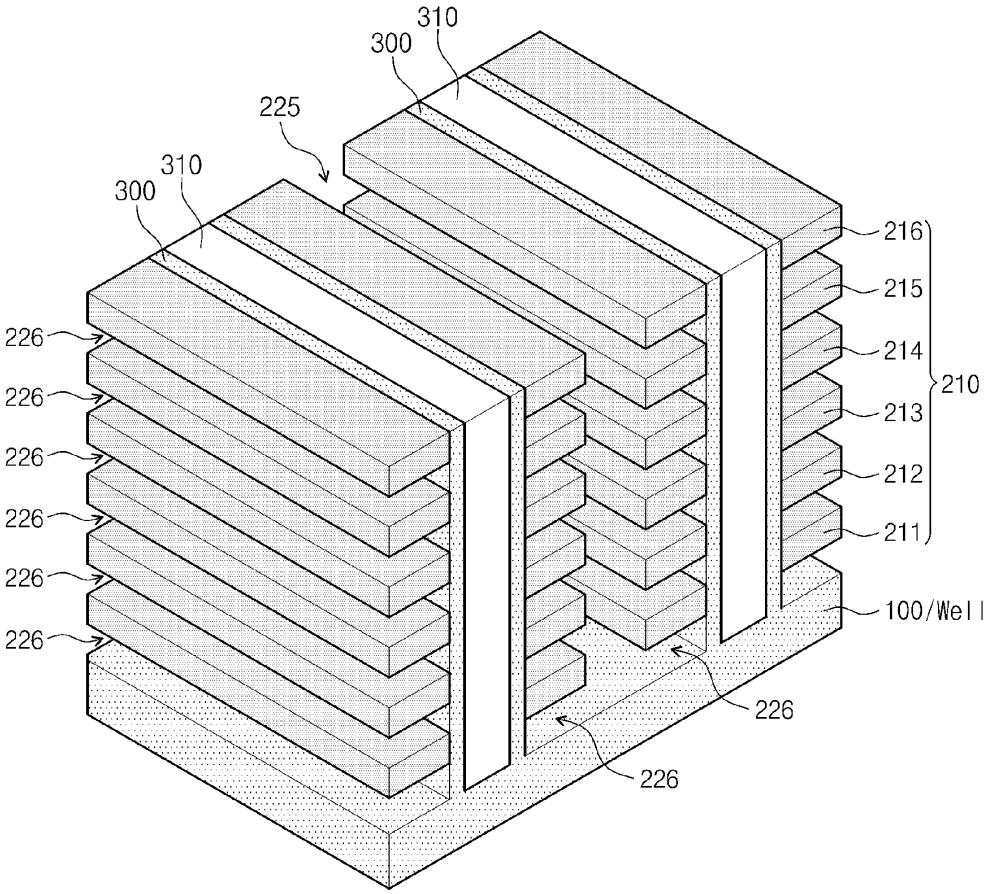

310
300
225
310
300
216
215
214
213
212
211
210
226
226
226
226
226
226
100/Well
226
226

Fig. 31

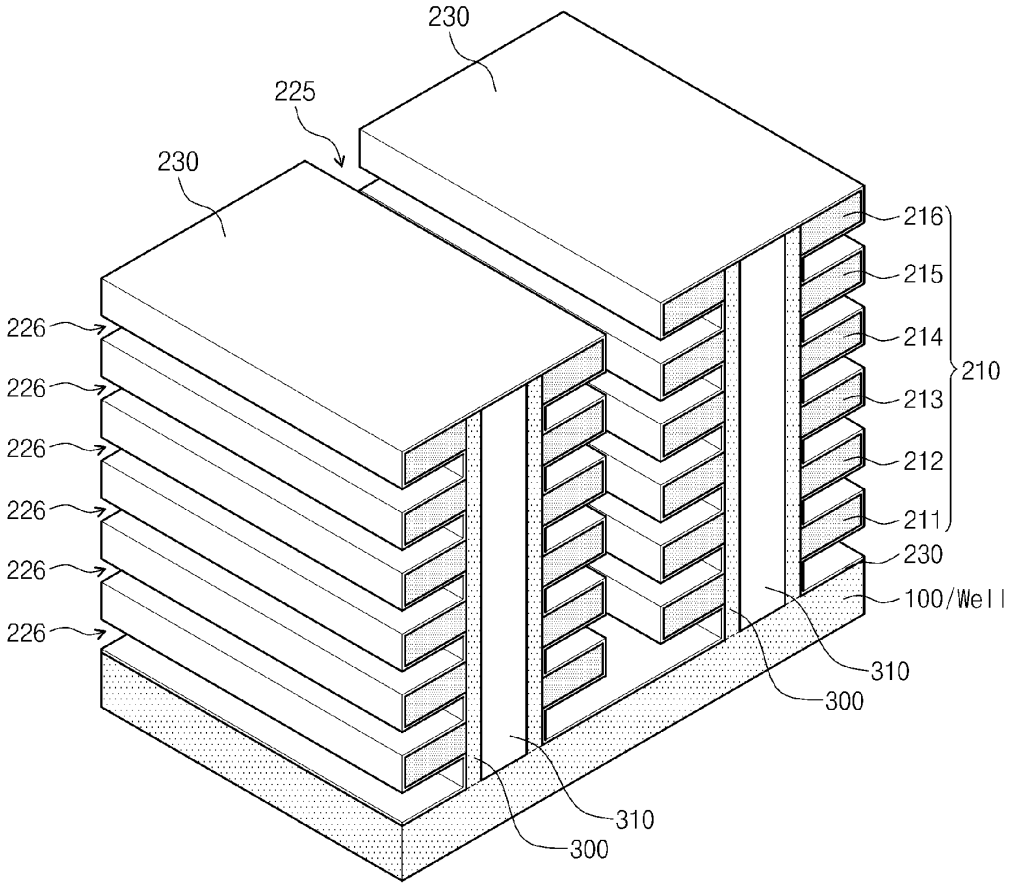

230
225
230
216
215
214
213
212
211
210
230
100/Well
226
226
226
226
226
226
310
300
310
300

Fig. 32

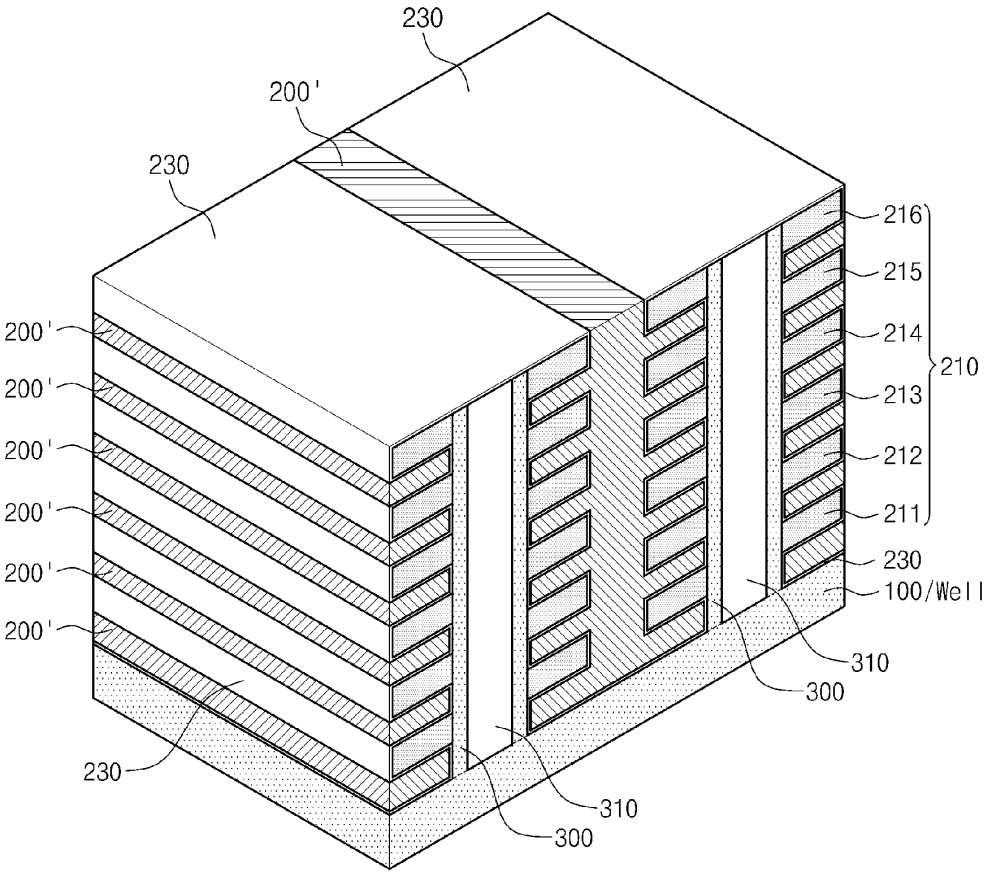

230
200'
230
216
215
214
210
213
212
211
200'
200'
200'
200'
200'
200'
230
100/Well
310
300
230
310
300

Fig. 33

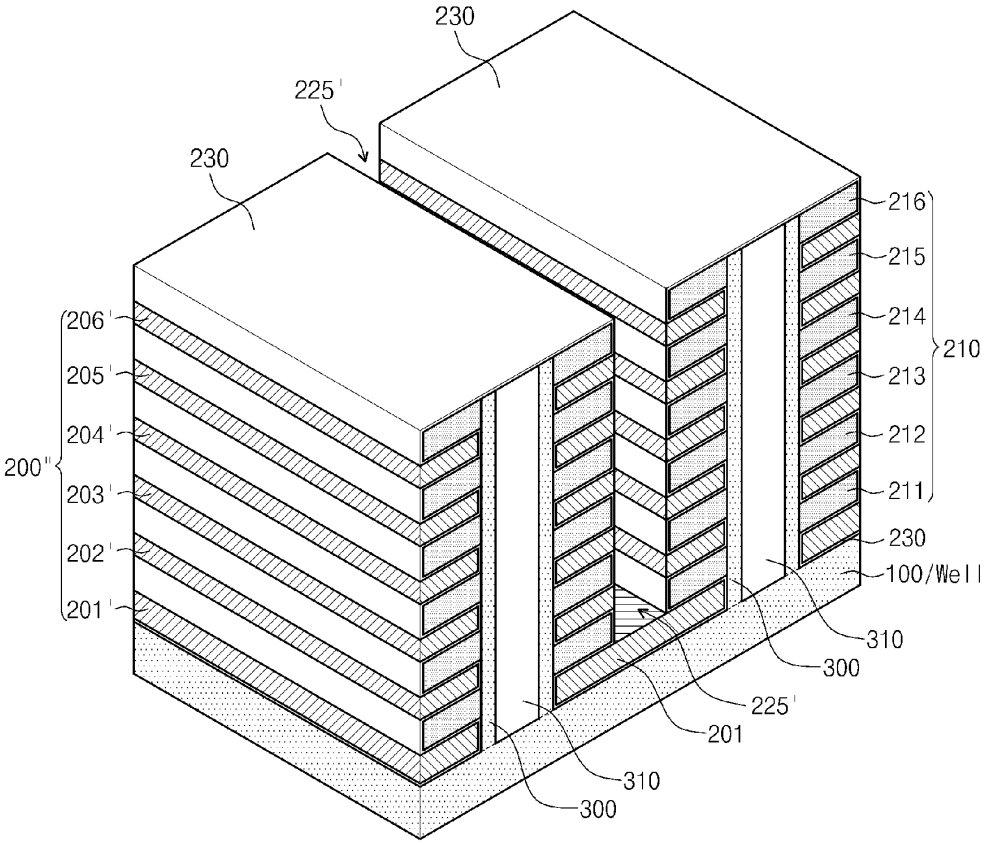

230
225'
230
216
215
214
210
213
212
211
230
100/Well
310
300
225'
201
310
300
206'
205'
204'
200"
203'
202'
201'

Fig. 34

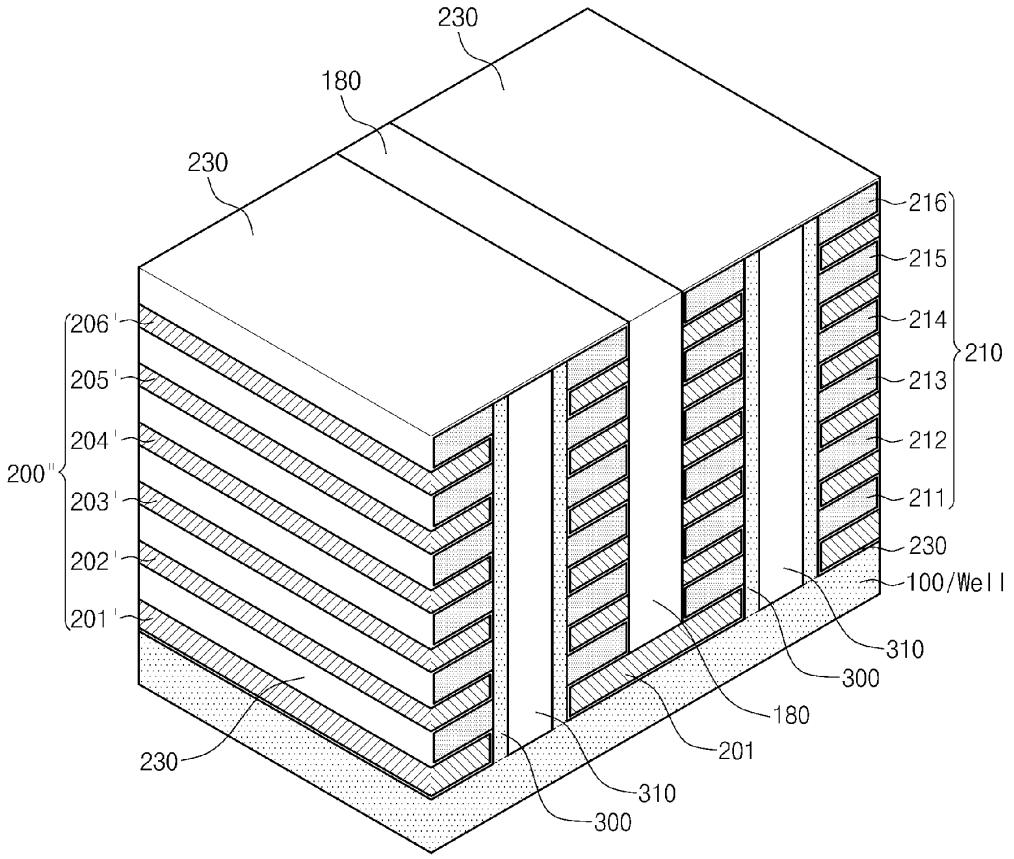

230
180
230
216
215
214
210
213
212
211
230
100/Well
206'
205'
204'
200''
203'
202'
201'
310
300
180
201
230
310
300

Fig. 35

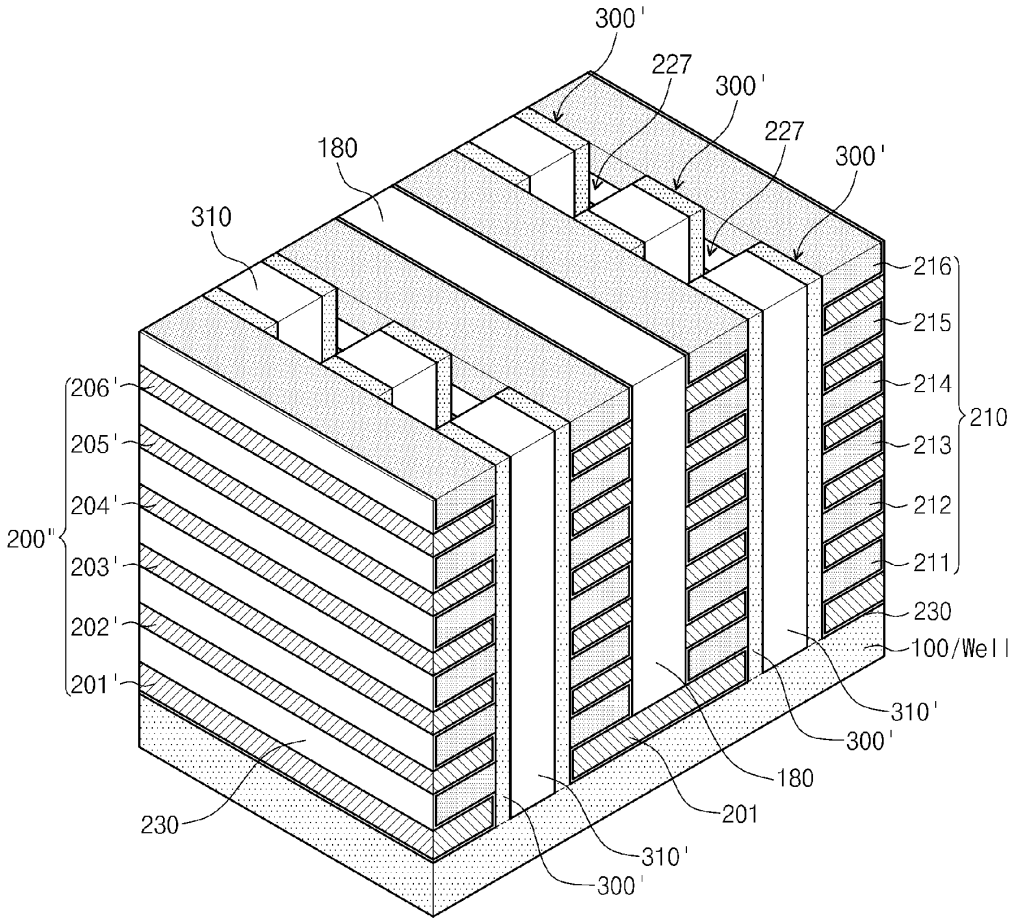

300'
227
300'
227
300'
180
310
216
215
214
210
213
212
211
230
100/Well
206'
205'
204'
200"
203'
202'
201'
310'
300'
180
201
310'
300'
230

Fig. 36

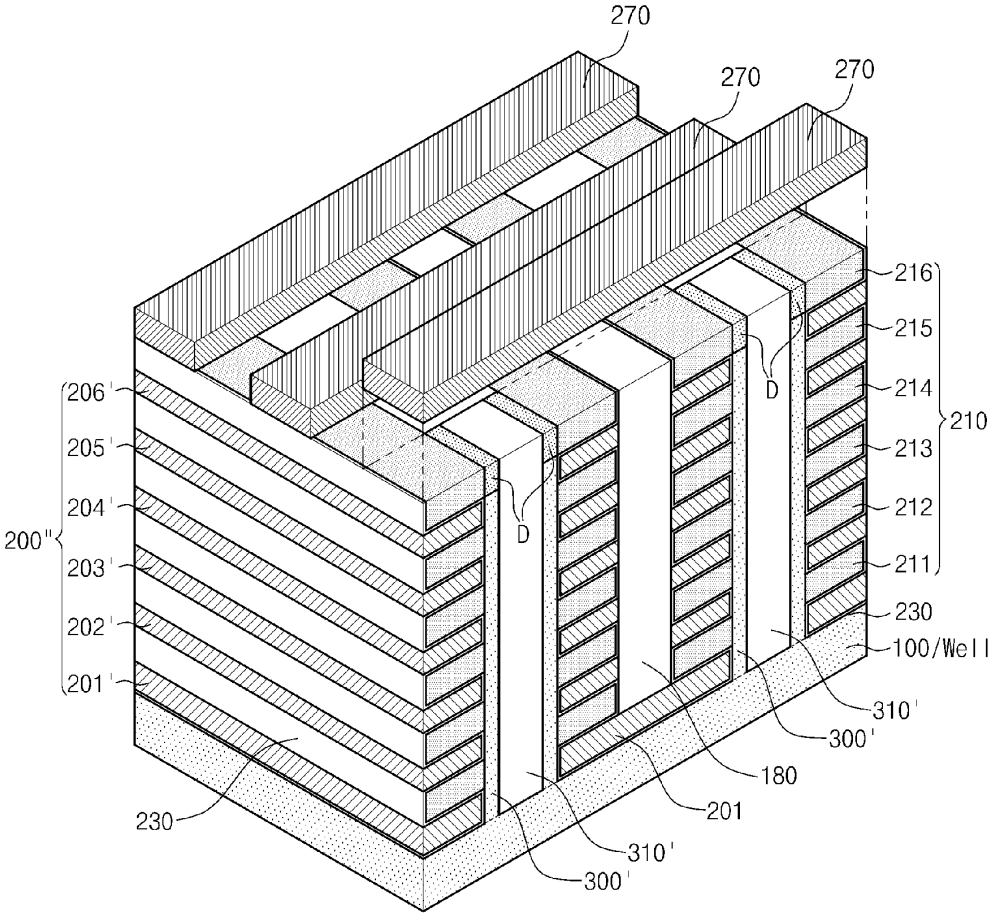

270
270
270
216
215
214
213
212
211
210
206'
205'
204'
203'
202'
201'
200''
D
D
230
100/Well
310'
300'
180
201
230
310'
300'

Fig. 37

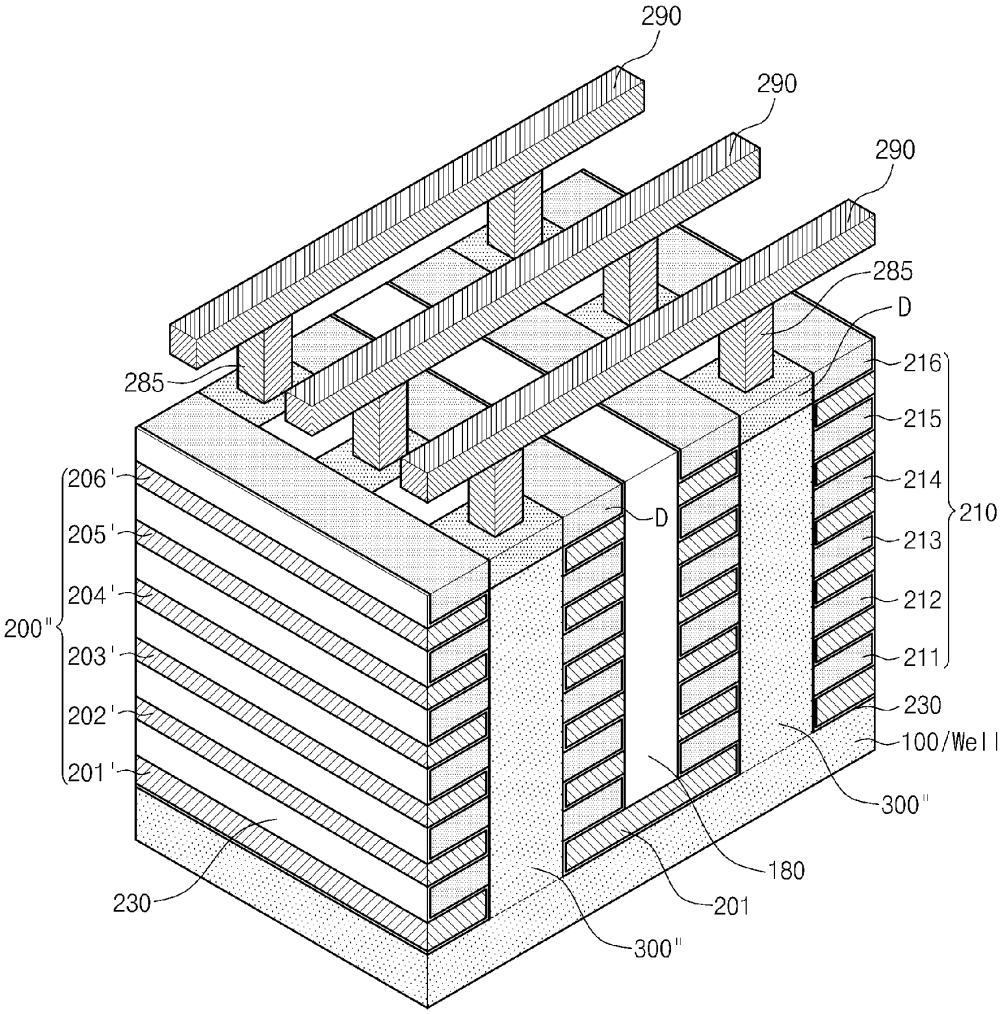

290
290
290
285
D
285
216
215
214
210
213
212
211
230
100/Well
300"
180
201
300"
D
206'
205'
204'
200"
203'
202'
201'
230

Fig. 38

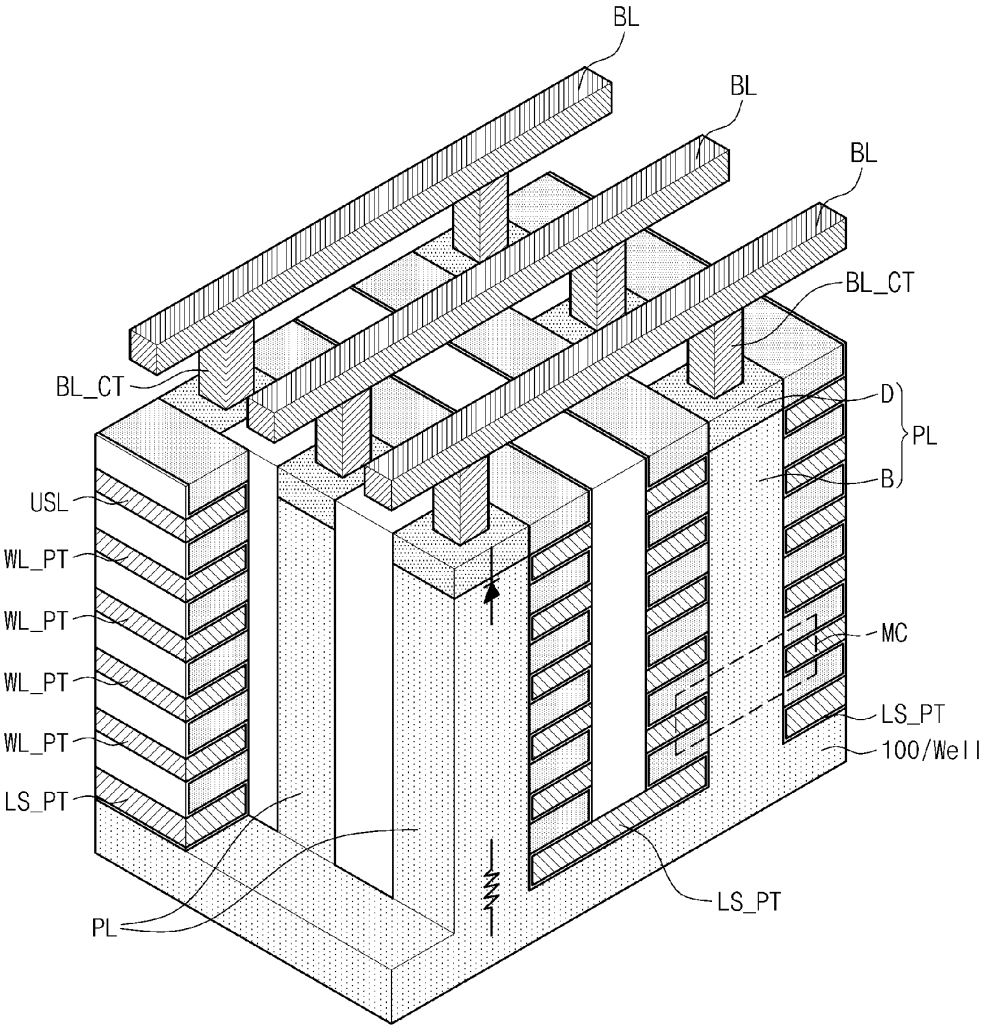

BL
BL
BL
BL_CT
BL_CT
D
PL
B
USL
WL_PT
WL_PT
WL_PT
WL_PT
LS_PT
MC
LS_PT
100/Well
LS_PT
PL

Fig. 39

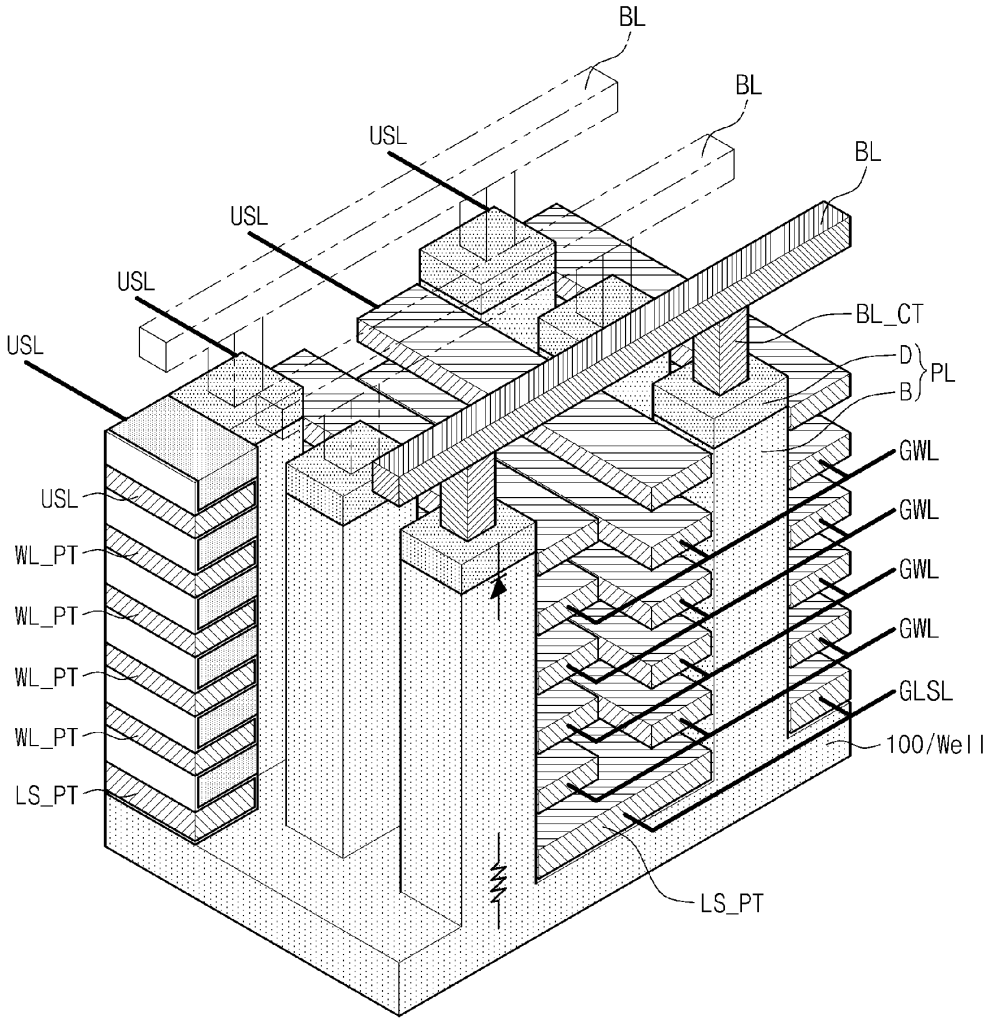

BL
BL
BL
USL
USL
USL
USL
USL
BL_CT
D
B
PL
GWL
GWL
GWL
GWL
GLSL
100/Well
WL_PT
WL_PT
WL_PT
WL_PT
LS_PT
LS_PT

Fig. 40A

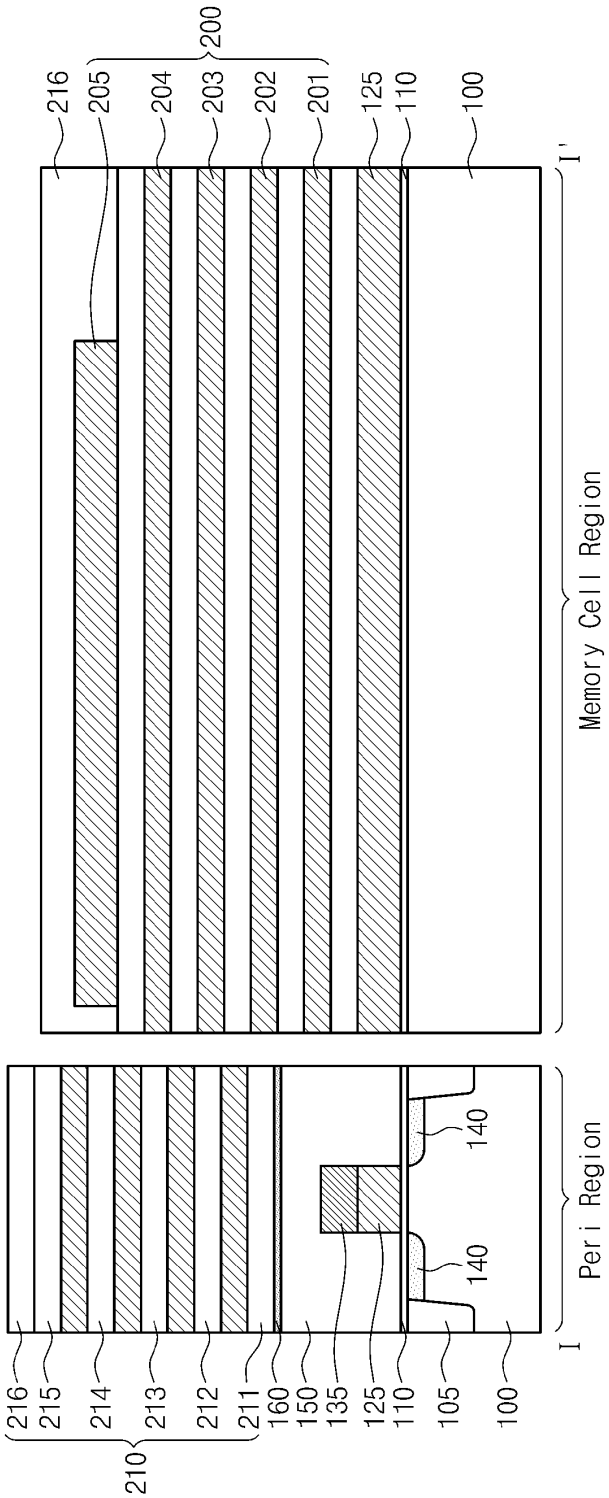

200
216
205
204
203
202
201
125
110
100
I'
Memory Cell Region
140
140
Peri Region
I
216
215
214
213
212
211
160
150
135
125
110
105
100
210

Fig. 40B

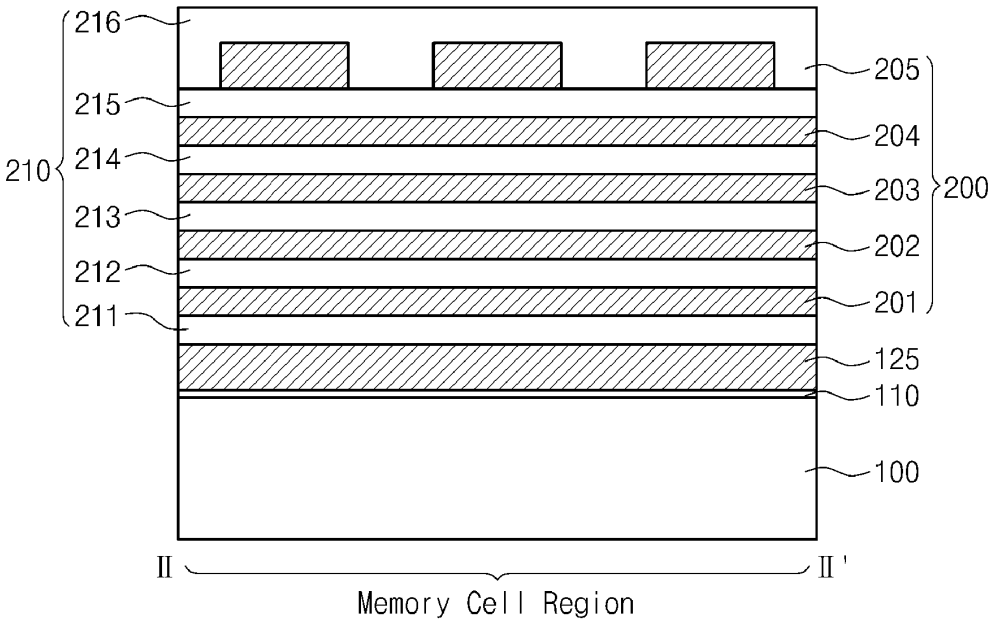

216
215
214
213
212
211
210
205
204
203
202
201
200
125
110
100
II
II'
Memory Cell Region

Fig. 41A

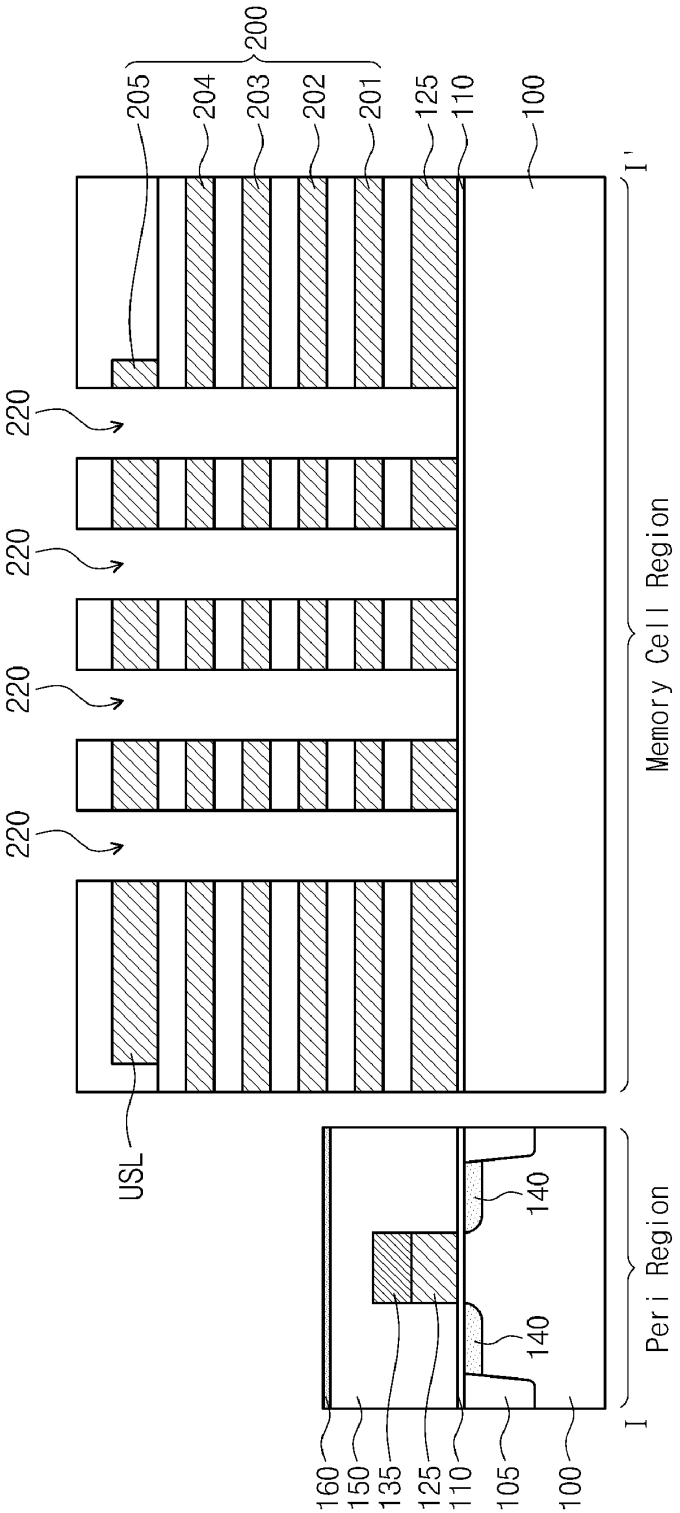

200
205
204
203
202
201
125
110
100
I'
220
220
220
220
Memory Cell Region
USL
140
140
Peri Region
I
160
150
135
125
110
105
100

Fig. 41B

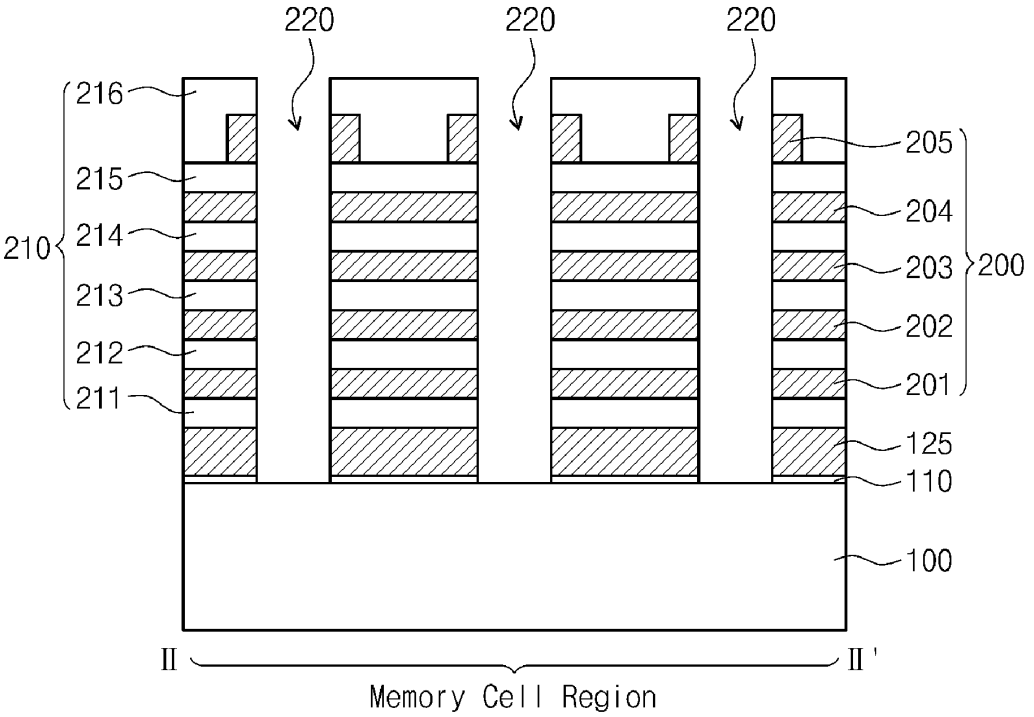

220
220
220
216
215
214
213
212
211
210
205
204
203
202
201
200
125
110
100
II
II'
Memory Cell Region

Fig. 42A

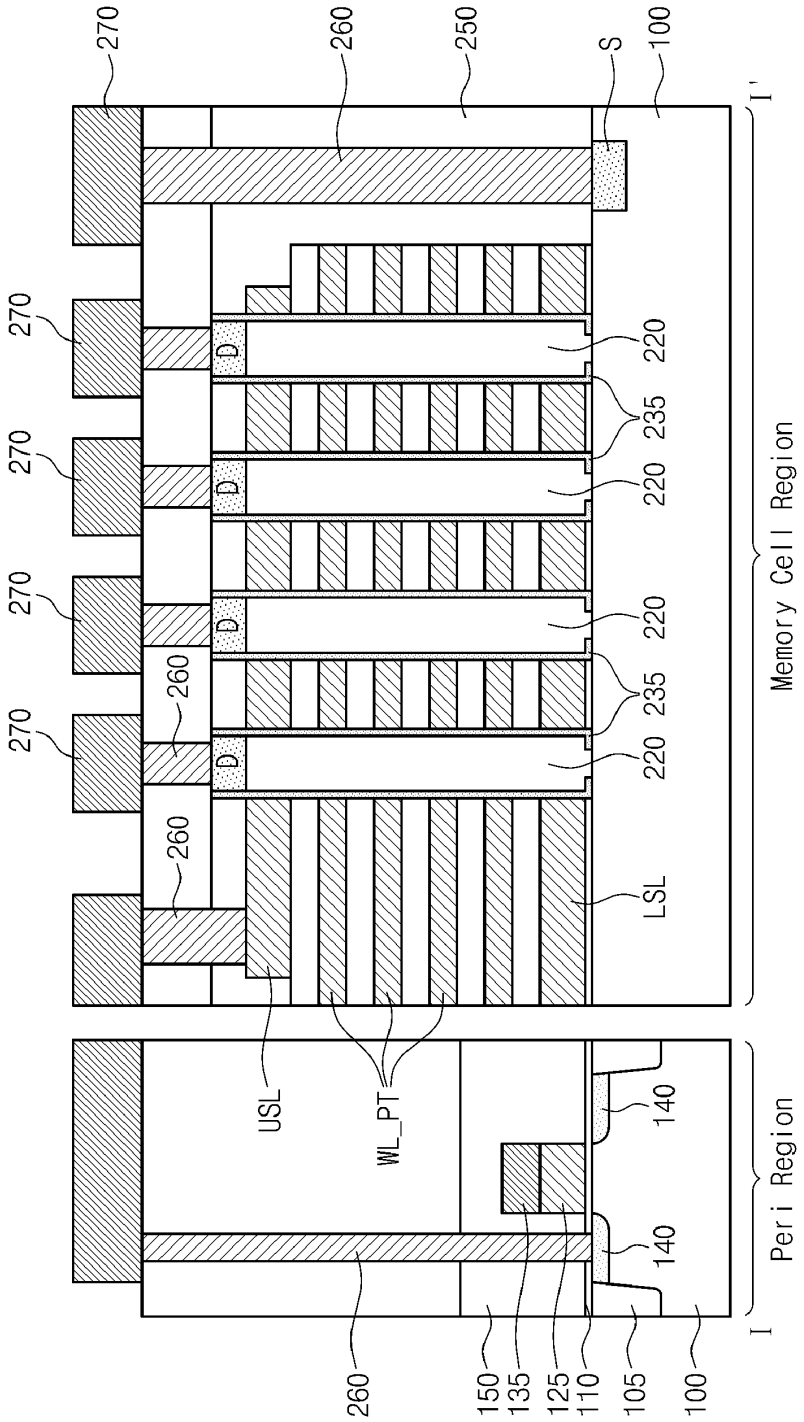

270
260
250
S
100
I'
270
D
220
235
270
D
220
270
D
220
260
235
270
D
220
260
LSL
Memory Cell Region
USL
WL_PT
140
140
Peri Region
I
260
150
135
125
110
105
100

Fig. 42B

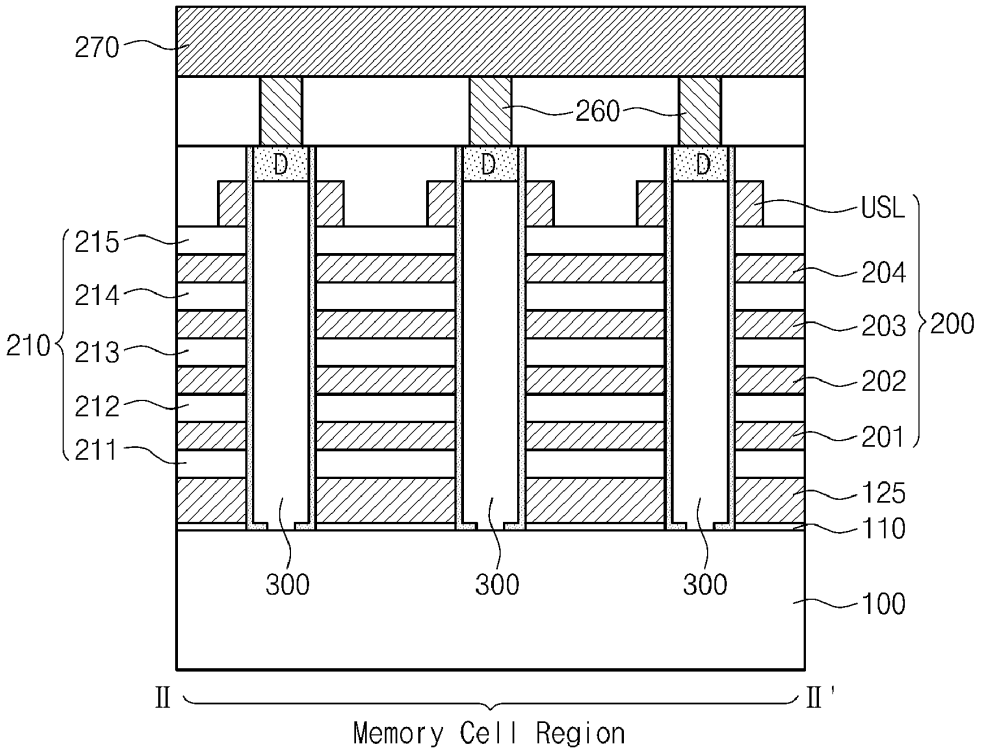

270
260
D
D
D
USL
215
214
213
212
211
210
204
203
202
201
200
125
110
300
300
300
100
II
II'
Memory Cell Region

Fig. 43

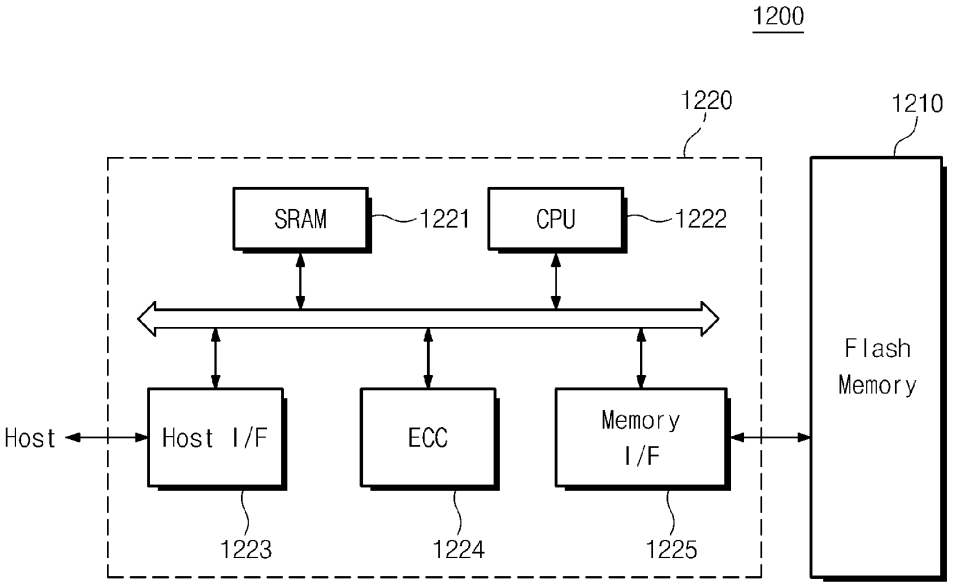
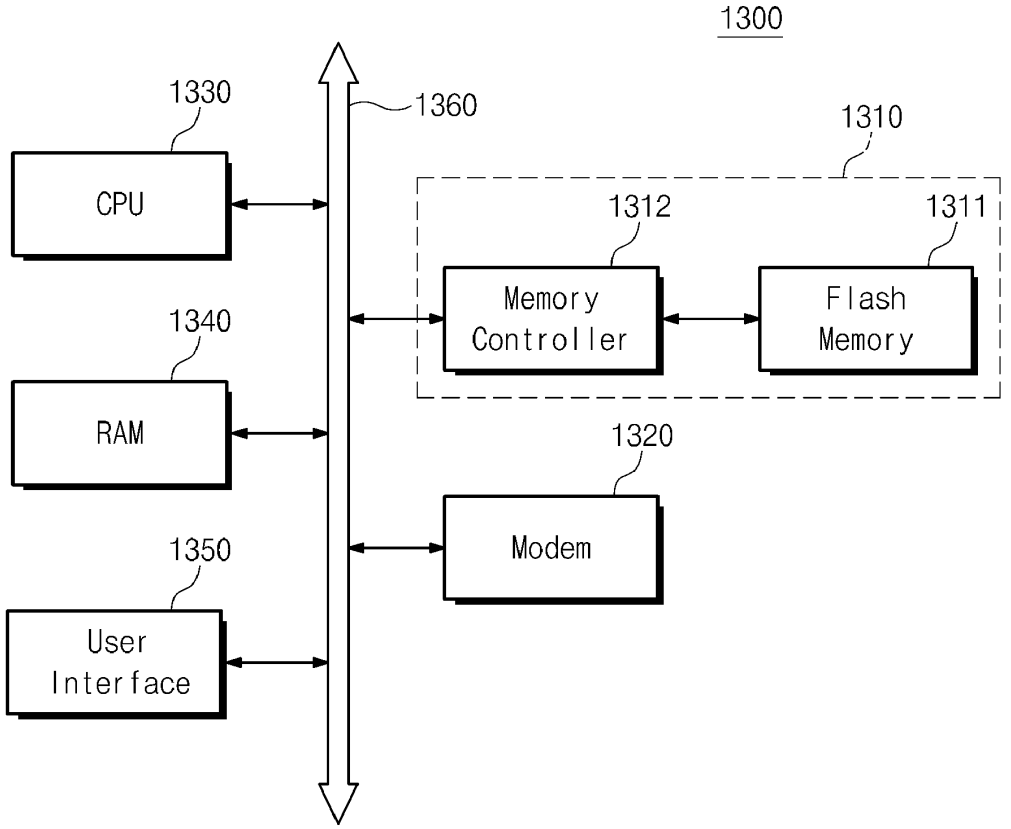

1200
1220
1210
SRAM
1221
CPU
1222
Flash
Memory
Host
Host I/F
ECC
Memory
I/F
1223
1224
1225

Fig. 44


1300
1330
CPU
1360
1310
1312
1311
Memory Controller
Flash Memory
1340
RAM
1320
Modem
1350
User Interface

MEMORY DEVICES INCLUDING VERTICAL PILLARS AND METHODS OF MANUFACTURING AND OPERATING THE SAME

RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. 119 to Korean Patent Application No.10-2008-0054707, filed on Jun. 11, 2008, the content of which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] With the continued emphasis on highly integrated electronic devices, there is an ongoing need for semiconductor memory devices that operate at higher speeds and lower power and that have increased device density. To accomplish this, devices with aggressive scaling and multiple-layered devices with transistor cells arranged in horizontal and vertical arrays have been under development.

[0003] In one approach, planar memory cells, for example NAND memory cells, are formed in a conventional horizontal array. Multiple horizontal arrays are then stacked in a vertical direction. Limitations associated with this approach include poor reliability in the resulting device, since critical lithography steps are required for each layer in achieving the minimum feature size. In addition, in this configuration, the size of the driver transistors for driving the control gates is a function of the number of layers; therefore, the driver transistors are scaled as a multiple of the number of layers. This can lead to integration issues and heat removal concerns.

[0004] In another approach, multiple-layered memory devices with vertically oriented channels have been under development. In one configuration, a plurality of gate layers are formed on a substrate, and a vertical channel penetrates the plurality of gate layers. In each vertical channel, a lower gate layer is configured to operate as a lower select gate, a plurality of middle gate layers are configured to operate as control gates, and an upper gate layer is configured to operate as an upper select gate. The control gates can include charge storage layers adjacent the vertical channel, so the devices can operate as non-volatile memory devices. Upper select gates neighboring each other in a first horizontal direction are connected to operate as row select lines for the device. Vertical channels neighboring each other are connected in a second horizontal direction to operate as bit lines for the device.

[0005] Others attempting the vertically oriented channel approach have met with limited success. In one configuration, a bottom portion of the vertical channel is connected to a common source diffusion layer that is formed in the substrate. The common source diffusion layer is doped to have an n+ doping, and the underlying substrate has a p type doping. Accordingly, a p-n junction is formed between the common source diffusion layer and the underlying substrate. The vertical channel is isolated by the n+ region in the substrate; Therefore, it is difficult to control the potential of the vertical channel through any electrode and it is necessary to apply a negative voltage level on the control gates to erase the memory cells. Such a negative voltage level can require a more complicated device power supply circuit, increasing device cost. Further, application of a negative voltage level is inconsistent with the power arrangement of conventional NAND memory devices, hindering straightforward replacement of conventional NAND devices by the vertically oriented channel memory devices. Furthermore, when an erase operation takes place, the erase operation requiring the injection of holes into the charge storage layers of the control gates adjacent the vertical channel, any holes in the vertical channel are depleted by the injection into the charge storage layers. With the depletion of holes, the potential of the vertical channel is reduced, which makes the erase operation less effective in time.

[0006] In order to prevent hole depletion in the vertical channels, hole injection by a gate-induced-drain-leakage (GIDL) operation has been proposed, in order to maintain the potential of the vertical channels at a suitable level. However, vertical channel potential control through GIDL effect is not straightforward or can be unstable compared with direct body biasing, because it can be affected easily by the junction profiles, which can result in the erased Vth distribution degradation. In addition, the GIDL effect is likely to incorporate hot hole injection into the lower select transistor or edge cell in the vertical channel strings, which can deteriorate endurance reliability characteristics of the resulting device.

SUMMARY

[0007] Embodiments of the present invention are directed to vertical-type semiconductor memory devices and methods of forming the same. In particular, in certain embodiments, a bottom portion of a semiconductor vertical channel is directly connected to the underlying substrate at a contact region that comprises a semiconducting material. In certain embodiments, an inversion layer is formed in the contact region to cause the contact region to be conductive by applying a suitable voltage to a lower-most gate of the vertical channel. The inversion layer in turn operates as a common source line for the resulting device. In the absence of a diffusion region between the vertical channel and the substrate, a positive erase voltage can be used in the resulting device to perform an erase operation, eliminating the need for additional power circuitry for generating negative voltages. Also, since positive erase voltages can be used for an erase operation, the resulting devices are consistent with conventional horizontally configured NAND memory devices; allowing for more straightforward replacement of such conventional devices by the devices of the present invention.

[0008] In one aspect, a semiconductor device comprises: a substrate of semiconductor material extending in a horizontal direction; a plurality of interlayer dielectric layers on the substrate; a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; and a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconducting region.

[0009] In one embodiment, the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

[0010] In another embodiment, the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region.

[0011] In another embodiment, the semiconductor device comprises a semiconductor memory device and wherein: an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor; a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; and further comprises: a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness, wherein the first thickness is less than the second thickness; and wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

[0012] In another embodiment, the semiconductor material of the vertical channel is selected from the group consisting of a single-crystal semiconductor material and a polycrystalline semiconductor material.

[0013] In another embodiment, the semiconductor material of the substrate is selected from the group consisting of a single-crystal semiconductor material and a polycrystalline semiconductor material.

[0014] In another embodiment, the gate insulating layer includes a charge storage layer and wherein the semiconductor device comprises a non-volatile memory device.

[0015] In another embodiment: an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor; a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; control gates of memory cell transistors sharing a same layer of the device arranged in a horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device; memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel; upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors; upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device; and the semiconductor device comprises a semiconductor memory device.

[0016] In another aspect, a memory system comprises: a memory controller that generates command and address signals; and a memory module comprising a plurality of memory devices, the memory module receiving the command and address signals and in response storing and retrieving data to and from at least one of the memory devices. Each memory device comprises: a substrate of semiconductor material extending in a horizontal direction; a plurality of interlayer dielectric layers on the substrate; a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; and a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconducting region.

[0017] In one embodiment, the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region

[0018] In another embodiment, the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region.

[0019] In another embodiment: an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor; a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; and the system further comprises: a gate insulating layer between the lower select gate and the substrate, the gate insulating layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness, wherein the first thickness is less than the second thickness; and wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

[0020] In another embodiment, the gate insulating layer includes a charge storage layer and wherein the memory device comprises a non-volatile memory device.

[0021] In another embodiment: an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor; a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; control gates of memory cell transistors sharing a same layer of the device arranged in a horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device; memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel; upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors; and upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device.

[0022] In another aspect, a method of fabricating a semiconductor device comprises: providing a substrate of semiconductor material extending in a horizontal direction; providing a plurality of interlayer dielectric layers on the substrate; providing a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; providing a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns; and providing a gate insulating layer between each gate pattern and

the vertical channel that insulates the gate pattern from the vertical channel, wherein the vertical channel is in contact with the substrate at a contact region that comprises a semiconducting region.

[0023] In one embodiment, the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

[0024] In another embodiment, the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region.

[0025] In another embodiment, the semiconductor device comprises a semiconductor memory device and wherein: an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor; a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; and the method further comprises: providing a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness, wherein the first thickness is less than the second thickness; and wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

[0026] In another embodiment, the gate insulating layer includes a charge storage layer and wherein the semiconductor device comprises a non-volatile memory device.

[0027] In another aspect, a method of performing an erase operation on a semiconductor memory device is provided, the semiconductor memory device comprising: a substrate of semiconductor material extending in a horizontal direction; a plurality of interlayer dielectric layers on the substrate; a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; and a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconductor material, wherein: an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor; a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; control gates of memory cell transistors sharing a same layer of the device arranged in a horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device; memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel; upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors; and upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device. The erase operation comprises: placing the lower select gate and the upper select gate of the common string in a floating state; applying a ground or positive voltage to the word lines; and applying a positive erase voltage to the semiconductor substrate.

[0028] In one embodiment, the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

[0029] In another embodiment, the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region.

[0030] In another embodiment, the method further comprises: providing a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness, wherein the first thickness is less than the second thickness; and wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

[0031] In another aspect, a method of performing a read operation on a semiconductor memory device is provided, the semiconductor memory device comprising: a substrate of semiconductor material extending in a horizontal direction; a plurality of interlayer dielectric layers on the substrate; a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconducting region; wherein: an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor; a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; control gates of memory cell transistors sharing a same layer of the device arranged in a horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device; memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel; upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors; and upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device. The read operation comprises: applying a ground voltage to the semiconductor substrate; applying a read voltage to control gates of unse-

lected memory cell transistors of the common string; applying a read voltage to gates of selected upper select transistors of the common string; applying a criterion voltage to control gates of selected memory cell transistors of the common string; and applying a read voltage to the lower select gate of the lower select transistor of the common string and of neighboring strings to thereby create an conductive inversion layer at an upper region of the semiconductor substrate and at a lower region of at least sidewalls of the vertical channel in the contact region, the inversion layer operating as a conductive common source line for the semiconductor memory device during the read operation.

[0032] In one embodiment, the contact region comprises the upper region of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

[0033] In another embodiment, the method further comprises: providing a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness, wherein the first thickness is less than the second thickness; and wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

BRIEF DESCRIPTION OF THE DRAWINGS

[0034] The foregoing and other objects, features and advantages of the embodiments of the invention will be apparent from the more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. In the drawings:

[0035] FIG. **1** is a perspective schematic view of a vertical-channel memory device, in accordance with an embodiment of the present invention.

[0036] FIG. **2** is top layout view of a vertical-channel memory device, in accordance with an embodiment of the present invention.

[0037] FIG. **3** is a cross-sectional perspective view of a vertical channel memory device, in accordance with an embodiment of the present invention.

[0038] FIGS. **4** and **5** are cross-sectional views of the vertical channel memory device of FIG. **3**, taken along section line I-I' of FIG. **2**, in accordance with an embodiment of the present invention.

[0039] FIG. **6** is a perspective schematic view of a vertical-channel memory device, in accordance with another embodiment of the present invention.

[0040] FIG. **7**A is top layout view of the vertical-channel memory device of FIG. **6**. FIG. **7**B is a cross-sectional perspective view of the vertical channel memory device of FIG. **6**.

[0041] FIG. **8** is a perspective schematic view of a vertical-channel memory device, illustrating the accessing of an individual memory cell, in accordance with an embodiment of the present invention.

[0042] FIG. **9** is a perspective view of a vertical-channel memory device, illustrating access of an individual memory cell during a programming operation, in accordance with an embodiment of the present invention.

[0043] FIG. **10** is a perspective view of a vertical-channel memory device, illustrating an erase operation, in accordance with an embodiment of the present invention.

[0044] FIG. **11** is a perspective view of a vertical-channel memory device, illustrating access of an individual memory cell during a read operation, in accordance with an embodiment of the present invention.

[0045] FIGS. **12**A-**21**A are cross-sectional views taken along section line I-I' of FIG. **2**, and FIGS. **12**B-**21**B are cross-sectional views taken along section line II-II' of FIG. **2**, of a method of forming a vertical-channel memory device, in accordance with an embodiment of the present invention.

[0046] FIGS. **22** and **23** are close-up perspective views of embodiments of the gate insulating layer and pillar in the vertical openings, in accordance with embodiments of the present invention.

[0047] FIGS. **24** and **25** are cross-sectional views of a method of forming a vertical-channel memory device, in accordance with another embodiment of the present invention.

[0048] FIGS. **26**-**39** are perspective views of a method of forming a vertical-channel memory device, in accordance with another embodiment of the present invention.

[0049] FIGS. **40**A-**42**A are cross-sectional views taken along section line I-I' of FIG. **2**, and FIGS. **40**B-**42**B are cross-sectional views taken along section line II-II' of FIG. **2**, of a method of forming a vertical-channel memory device, in accordance with another embodiment of the present invention.

[0050] FIG. **43** is a block diagram of a memory card that includes a semiconductor device in accordance with the embodiments of the present invention.

[0051] FIG. **44** is a block diagram of a memory system that employs a memory module, for example, of the type described herein, in accordance with the embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS

[0052] Embodiments of the present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Like numbers refer to like elements throughout the specification.

[0053] It will be understood that, although the terms first, second, etc. are used herein to describe various elements, these elements should not be limited by these terms. These terms are used to distinguish one element from another. For example, a first element could be termed a second element, and, similarly, a second element could be termed a first element, without departing from the scope of the present invention. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0054] It will be understood that when an element is referred to as being "on" or "connected" or "coupled" to another element, it can be directly on or connected or coupled to the other element or intervening elements can be present. In contrast, when an element is referred to as being "directly on" or "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other words used to describe the relationship between elements should be

interpreted in a like fashion (e.g., "between" versus "directly between," "adjacent" versus "directly adjacent," etc.). When an element is referred to herein as being "over" another element, it can be over or under the other element, and either directly coupled to the other element, or intervening elements may be present, or the elements may be spaced apart by a void or gap.

[0055] The terminology used herein is for the purpose of describing particular embodiments and is not intended to be limiting of the invention. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes" and/or "including," when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0056] FIG. **1** is a perspective schematic view of a vertical-channel memory device, in accordance with an embodiment of the present invention.

[0057] Referring to FIG. **1**, in this example, a three-dimensional memory device **1000** includes a plurality of vertical channels, or pillars, represented by dashed lines PL. The pillars PL extend in a vertical direction, and transistors formed along a common pillar PL combine to form a cell string CSTR. An upper-most transistor of a cell string CSTR is referred to as an upper select transistor and a lower-most select transistor of a cell string is referred to as a lower select transistor. Transistors between the upper select transistor and the lower select transistor of a cell string CSTR comprise memory cell MC transistors of the cell string CSTR.

[0058] The tops of the pillars PL arranged in a first horizontal direction are connected to each other along bit lines BL. The bottoms of the pillars PL are connected to each other along a common source line CSL. The bottoms of the pillars are also directly connected to the substrate well Well.

[0059] Gates of the upper select transistors arranged along a second horizontal direction are connected to each other along upper select lines USL. Gates of the lower select transistors are connected to each other along a lower select plate LS_PT to provide a lower global select line GLSL. Gates of the memory cell transistors MC sharing a common vertical row are connected to each other along word line plates WL_PT to provide global word lines GWL. Global word lines GWL of different rows are independent.

[0060] FIG. **2** is top layout view of a vertical-channel memory device, in accordance with an embodiment of the present invention. In this view, it can be seen that gate insulator films GI can be provided to surround the vertical pillars PL along their vertical length, to insulate the vertical pillars PL from the upper select lines USL, the word line plates WL_PT and the lower select plate LS_PT. It can also be seen in this view that the bit lines BL are accessed via bit line contacts BL_CT, the word line plates WL_PT are accessed via word line contacts WL_CT, the upper select lines USL are accessed via upper select line contacts USL_CT, and the common source line CSL which is also coupled to the well **100**/Well at source region S, is accessed via a source contact S_CT.

[0061] FIG. **3** is a cross-sectional perspective view of a vertical channel memory device, in accordance with an embodiment of the present invention. Referring to FIG. **3**, in this embodiment, a substrate **100** of semiconductor material is provided. In various embodiments, the substrate **100** can comprise polycrystalline or single-crystal semiconductor material, in a bulk or SOI configuration. The substrate **100** extends in a horizontal direction. A lower gate insulator layer **110** is on the substrate **100**. A plurality of interlayer dielectric layers **210** (see FIG. **4**) are provided on the lower gate insulator layer **110**. The word line plates WL_PT and the upper select lines USL are provided, each being between a neighboring lower interlayer dielectric layer **211**, **212**, **213**, **214**, **215**, . . . and a neighboring upper interlayer dielectric layer **211**, **212**, **213**, **214**, **215**, ... The lower select plate LS_PT is provided between the lower-most interlayer dielectric layer **211** and the lower gate insulator **110**.

[0062] Vertical pillars PL of semiconductor material extend in a vertical direction through the plurality of interlayer dielectric layers **210** and the lower select plate LS_PT, the word line plates WL_PT, and the upper select lines USL, so that the vertical pillars PL are at least partially surrounded in a horizontal direction by the lower select plate LS_PT, the word line plates WL_PT, and the upper select lines USL. For example, the word line plates WL_PT each surround, or encompass, the perimeter of the walls of the vertical pillars PL. The same holds true for the lower select plates LS_PT and the upper select lines USL. The gate insulator films GI are is provided between each of the lower select plate LS_PT, the word line plates WL_PT, and the upper select lines USL and the vertical pillars PL. It can also be seen in this view that each vertical pillar PL comprises a body region B along most of its length and a drain region D at a top portion thereof, in contact with the corresponding bit line BL.

[0063] FIGS. **4** and **5** are cross-sectional views of the vertical channel memory device of FIG. **3**, taken along section line I-I' of FIG. **2**, in accordance with an embodiment of the present invention. In FIG. **4**, it can be seen that an inversion layer I is created along the walls, or outer surface, of the vertical pillars PL when a suitable word line voltage is applied to the word line plates WL_PT. It can also be seen that the thickness T**1** of the word line plates WL_PT is generally greater than the thickness T**2** of the interlayer dielectric layers **210**. At the same time, it can be seen that the thickness T**2** of the interlayer dielectric layers **210** is greater than the thickness T**3** of the capacitor dielectric layer CD. In order for current to flow in a vertical direction of the pillars PL, the inversion layers I generated in the vertical pillars PL and caused by the neighboring word lines plates WL_PT, should overlap. This overlap, or fringing field, has a maximum width W, or amount of vertical extension in the adjacent vertical pillars PL above a level of the top surface of, or below a level of the bottom surface of, the word line plate WL_PT.

[0064] Referring to FIG. **5**, it can be seen that in each pillar PL, rather than using source/drain diffusion regions for each of the memory cell transistors, a diffusion region effect can be generated by a fringing field FF that is originated by the lower select plate LS PT, the word line plates WL_PT, or the upper select lines USL. The generation and operation of a fringing field as applied to a conventional planar NAND memory device is disclosed in United States Patent Application Publication Number 2007/0205445, incorporated herein by reference in its entirety. Formation of source/drain regions in the vertical channel of a vertically oriented memory device is challenging. In view of this, the fringing field configuration can be readily applied to the methods and configurations of the embodiments of the present invention.

[0065] FIG. **6** is a perspective schematic view of a vertical-channel memory device, in accordance with another embodiment of the present invention. FIG. **7**A is top layout view of the vertical-channel memory device of FIG. **6**. FIG. **7**B is a cross-sectional perspective view of the vertical channel memory device of FIG. **6**. In this embodiment, it can be seen that the source contact plug S_CT can be formed of a material that has a different dopant type than that of the substrate well **100**. For example, in the embodiment shown, the well **100** and vertical pillars PL are formed of a semiconducting material having a first p-dopant type p-Si, while the source contact plug S_CT is formed of a semiconducting material having a second, n-dopant type n+.

[0066] FIG. **8** is a perspective schematic view of a vertical-channel memory device, illustrating the accessing of an individual memory cell, in accordance with an embodiment of the present invention. In this embodiment, it can be seen that an individual memory cell MC**1** in the three-dimensional array can be accessed for programming and read operations by applying appropriate voltage levels to a selected word line WL, a selected bit line BL a lower select line LSL and a selected upper select line USL.

[0067] FIG. **9** is a perspective view of a vertical-channel memory device, illustrating access of an individual memory cell during a programming operation, in accordance with an embodiment of the present invention. Referring to FIG. **9** and Table 1 below, during a programming operation, a programming voltage V_{PGM} is applied to selected word line plates Sel.WL_PT and a pass voltage V_{PASS} is applied to unselected word line plates Unsel.WL_PT. A ground voltage GND is applied to selected bit lines Sel(BL) and a Vcc voltage is applied to unselected bit lines Unsel(BL). A Vcc voltage is applied to selected upper select lines USL and a GND voltage is applied to unselected upper select lines USL. In addition, a GND voltage is applied to the lower select line LSL, a voltage (−) is applied to the common source line CSL and a GND voltage is applied to the well **100**. This operation causes electrons to congregate in the channel of the thus-selected memory cell MC**1**, which operates to program the selected cell MC**1**. The operation of self-boosting technology, as described for example in U.S. Pat. No. 5,473,563, incorporated herein by reference, can be employed to inhibit programming of unselected pillars. The self-boosting operation prevents current from flowing to unselected pillars.

TABLE 1

		PRG	ERS	READ
WL	Sel.	V_{PGM}	GND	0 V
	Unsel.	V_{pass}	GND	Vread
BL	Sel.	GND	F	Vpchg
	Unsel.	Vcc	F	—
USL	Sel.	Vcc	F	Vread
	Unsel.	GND/Floating	F	GND
LSL	—	GND/Floating	F	Vread
CSL	—	—	F	GND
Well	—	GND/Floating	Positive V_{ERS}	GND

[0068] FIG. **10** is a perspective view of a vertical-channel memory device, illustrating an erase operation, in accordance with an embodiment of the present invention. Referring to FIG. **10** and Table 1 above, during an erase operation, a GND voltage is applied to all word line plates WL_PT within the selected block, and a Floating voltage F is applied to all bit lines BL and all upper select lines USL. In addition, a Floating voltage is applied to the lower select line LSL, and the common source line CSL. A positive erase voltage V_{ERS} is applied to the well **100**. This operation causes all electrons to be removed from the channel regions of all memory cells in the array, which operates to erase the memory cells of the array. In this case, since the positive erase voltage V_{ERS} is delivered directly to the vertical pillars PL during the erase operation, it is possible to erase the memory cells by applying a ground voltage GND to the word lines WL. Also, since a positive erase voltage can be used, and since a GND voltage can be applied to the word lines WL, there is no need to generate a negative voltage for the erase operation. This simplifies the power supply circuitry required for the device, and makes the resulting device compatible with the power supply configuration of conventional horizontally configured planar NAND memory devices; allowing for easier replacement of such conventional devices by the devices configured in accordance with embodiments of the present invention.

[0069] FIG. **11** is a perspective view of a vertical-channel memory device, illustrating access of an individual memory cell during a read operation, in accordance with an embodiment of the present invention. Referring to FIG. **11** and Table 1 above, during a read operation, a criterion voltage to discriminate '1' and '0', for example ground voltage GND, or 0 V, is applied to selected word line plates Sel.WL_PT and a read voltage V_{READ} is applied to unselected word line plates Unsel.WL_PT. A precharge voltage Vpchg is applied to selected bit lines Sel(BL) to discriminate '1' and '0' and GND voltage is applied to unselected bit lines Unsel(BL). A read voltage V_{READ} is applied to selected upper select lines USL and a GND voltage is applied to unselected upper select lines USL. In addition, a read voltage is applied to the lower select line LSL, a GND voltage is applied to the common source line CSL and a GND voltage is applied to the well **100**.

[0070] Application of the read voltage V_{READ} to the lower select line LSL causes vertical inversion regions **504**B to be formed along the outer walls of lower portions of the vertical pillars PL formed of semiconducting material. Also, since the lower gate insulator **110** between the lower select line and the well **100** is relatively thin, horizontal inversion regions **504**A are likewise formed along the top portions of the well formed of semiconducting material, below the lower gate insulator **110**. As a result of the presence of the horizontal and vertical inversion regions **504**A, **504**B formed in the semiconducting material along the upper portion of the well **100** and along the lower and upper side portions of the vertical pillars PL, the source region S and the vertical pillars PL are made to be electrically connected. In this manner, the horizontal and vertical inversion regions **504**A, **504**B operate to provide a common source line CSL to all the pillars in the array during the read operation.

[0071] In FIG. **1** above, the horizontal dashed lines connected to the source S indicate the operation of the horizontal inversion region **504**A at the upper portion of the well as a result of the application of the read voltage V_{READ} at the lower select plate LS_PT, and the vertical dashed lines along the pillars PL indicate the operation of the vertical inversion region **504**B at sidewalls of the vertical pillars PL as a result of the application of the read voltage V_{READ} at the lower select plate LS_PT, the word line plates WL_PT and the upper select lines USL.

[0072] In FIG. **6** above, the operation of the inversion layer is expressed as a plurality of MOS transistors. By comparison, the lower select plate LS_PT provide the function of a

gate, the lower gate insulator layer **110** provides the function of an oxide, and the substrate **100** provides the function of a semiconductor region. In this manner, the formation of the inversion layer in FIG. **6** is expressed as a plurality of MOS transistors, the gates of which are coupled to the lower select plate LS_PT. Thus, when the read voltage V_{READ} is applied to the lower select plate LS_PT, the horizontal inversion region **504**A is activated.

[0073] Since the voltages that are applied to the various elements during the programming, erase and read operations according to the embodiments of the present invention, are similar to the voltages that are applied for those same operations for conventional, horizontally disposed planar NAND-based memory devices, the devices of the embodiments of the invention are compatible with the power supplies of conventional NAND-based memory devices, and can therefore more readily serve as replacement devices for systems employing the conventional devices. The configuration and operation of the embodiments of the present specification are in contrast with other configurations recently proposed, including those proposed in the disclosure of United States Patent Application Serial No. 2007/0252201; in the disclosure of H. Tanaka et al., "Bit Cost Scalable Technology with Punch and Plug Process for Ultra High Density Flash Memory, Symposium on VLSI Technology Digest of Technical Papers, pp. 14-15 (2007); and in the disclosure of Fukuzumi et al., "Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory, IEDM Technical Digest, pp. 449-452 (2007), the contents of each being incorporated herein by reference. In each of these examples, a common source line is provided in a diffusion layer formed in an upper region of the substrate, as a doped region of the substrate. For this reason, a p-n junction is formed between the common source diffusion layer and the underlying substrate. Therefore, it is difficult to control the potential of the vertical channel through any electrode and it is necessary to apply the negative voltage level on the control gates to erase the memory cells. Such a negative voltage level can require a more complicated device power supply circuit, increasing device cost. Further, application of a negative voltage level is inconsistent with the power arrangement of conventional NAND memory devices, hindering straightforward replacement of conventional NAND devices by the vertically oriented channel memory devices. As described above, to prevent the problems associated with hole depletion in the vertical channels, which are isolated from the common source line, hole injection by a gate-induced-drain-leakage (GIDL) operation has been proposed, in order to maintain the potential of the vertical channels at a suitable level. However, vertical channel potential control through GIDL effect is not straightforward or can be unstable, as compared with direct body biasing, because it can be affected easily by the junction profiles, which can result in the erased Vth distribution degradation. In addition, the GIDL effect is likely to incorporate hot hole injection into the lower select transistor or edge cell in the vertical channel strings, which can deteriorate endurance reliability characteristics of the resulting device.

[0074] FIGS. **12**A-**21**A are cross-sectional views taken along section line I-I' of FIG. **2**, and FIGS. **12**B-**21**B are cross-sectional views taken along section line II-II' of FIG. **2**, of a method of forming a vertical-channel memory device, in accordance with an embodiment of the present invention.

[0075] Referring to FIGS. **12**A and **12**B, a substrate **100** is prepared. In one embodiment, the substrate **100** comprises a single-crystal semiconductor material substrate that provides a seed layer for later formation of single-crystal vertical pillars PL. In other embodiments, the substrate **100** can comprise a polycrystalline semiconductor material. Isolation regions **105** are formed at predetermined regions of the substrate, according to conventional techniques. A lower-most interlayer dielectric layer **110**, also referred to herein as a lower gate insulator **110**, is provided on the substrate. A first lower gate layer **120** is formed on the lower-most interlayer dielectric layer **110**, and a second lower gate layer **130** is formed on the first lower gate layer **120**. The lower gate layer **120**, **130** may optionally be formed as a single gate layer or as multiple gate layers as shown. In a case where the lower gate layer **110** comprises multiple gate layers, the first lower gate layer **120** can comprise a polysilicon layer and the second lower gate layer **130** can comprise a metal layer. In certain embodiments of the present invention, the lower-most interlayer dielectric layer **110** is sufficiently thin so that an inversion layer **504**A, **504**B (see FIG. **11**, above) can be created in the underlying semiconductor material of the substrate **100** when a suitable voltage is applied to the gate layer **120**, **130**.

[0076] Referring to FIGS. **13**A and **13**B, the first and second lower gate layers **120**, **130** are patterned in the peripheral region to form a lower gate pattern **125**, **135**. Source and drain regions **140** can be formed in the peripheral region using the lower gate pattern **125**, **135** as an ion implantation mask, according to conventional fabrication techniques.

[0077] Referring to FIGS. **14**A and **14**B, and interlayer dielectric layer **150** and etch stop layer **160** are sequentially formed in the peripheral region. The second lower gate pattern **135** is then removed in the memory cell region using the etch stop layer **160** as an etch mask.

[0078] Referring to FIGS. **15**A and **15**B, multiple alternating interlayer dielectric layers **210**, including in this example, layers **211**, **212**, **213**, **214**, **215**, and **216** and conductive gate layers **200**, including in this example, layers **201**, **202**, **203**, **204**, and **205** are formed on the first lower gate pattern **125** on the resulting structure. In various embodiments, the interlayer dielectric layers **210** can comprise a material selected from the group consisting of oxide, HDP oxide, CVD oxide, PVD oxide, BPSG, SOG, mixtures thereof, and other suitable materials. The gate layers **200** can comprise a material selected from the group consisting of poly-Silicon, W, TaN, TiN, metal silicide, mixtures thereof, and other suitable materials.

[0079] Referring to FIGS. **16**A and **16**B, the interlayer dielectric layers **210** and the conductive gate layers **200** are patterned to form vertical openings **220** in the memory cell region. In the peripheral region, the interlayer dielectric layers **210** and the conductive gate layers **200** are removed. The lower-most interlayer dielectric layer **110** is also removed at a bottom of the vertical openings **220**, exposing a top portion of the substrate **100** in each opening **220**.

[0080] Referring to FIGS. **17**A and **17**B, a gate insulating layer **230** is provided on the resulting structure. The gate insulating layer **230** covers a bottom and interior sidewalls of the vertical openings **220**, and a top of the uppermost interlayer dielectric layer **216** in the memory cell region, and optionally covers the etch stop layer **160** in the peripheral region.

[0081] FIGS. **22** and **23** are close-up perspective views of embodiments of the gate insulating layer and pillar in the vertical openings **230**. In one embodiment, the gate insulating layer **230** comprises a charge storage layer so that the device

can operate as a non-volatile memory device. In the example of FIGS. **22** and **23**, the gate insulating layer **230** comprises a sequentially formed blocking insulating layer **231**, a charge storage layer **232**, and a tunnel insulating layer **233**. Gate insulating layers **230** formed according to this configuration are described in U.S. Pat. Nos. 6,858,906 and 7,253,467 and in United States Patent Application Publication No. 2006/0180851, the contents of each being incorporated herein by reference. In certain embodiments, the charge storage layer **230** can comprise a charge trapping layer. In various embodiment, the charge trapping layer can comprise SiN. Other suitable materials for the charge trapping layer can be employed, for example, Al_2O_3, HfAlOx, HfAlON, HfSiOx, HfSiON and multiple layers thereof. In another embodiment, the charge storage layer **230** can comprise a floating gate layer, comprising a conducting or semiconducting material

[0082] Returning to FIGS. **17**A and **17**B, a spacer layer **240** is formed in the vertical openings **220**, on the gate insulating layer **230**. The spacer layer **240** is anisotropically etched to expose a middle portion of the underlying gate insulating layer **230** at the bottom of the openings **220**. The spacer layer **240** operates to protect the gate insulating layer **230** along the sidewalls of the openings **220** during subsequent exposure of the underlying substrate **100** during pillar formation, allowing for direct contact between the pillar PL and the substrate **100**. The spacer layer **240** is preferably formed of semiconductor material such as poly-silicon, amorphous silicon, or single-crystal silicon, so that the material is consistent with the subsequently formed pillar PL. In this manner, the spacer layer **240** does not need to be removed prior to formation of the pillar PL, but rather can remain to form a portion of the body of the pillar PL.

[0083] Referring to FIGS. **18**A and **18**B, the exposed middle portion of the underlying gate insulating layer **230** at the bottom of the openings **220** is removed using the spacer layer **240** as an etch mask, exposing the underlying substrate **100**. Pillars **300** are then formed in the openings **220**. The pillars **300** can be formed of a semiconductor material such as poly-silicon, amorphous silicon, or single-crystal silicon.

[0084] In one embodiment for forming the pillars **300**, a poly-silicon layer or first amorphous silicon layer is formed in the openings **220**, in contact with the exposed upper portions of the substrate **100**. In one embodiment, the poly-silicon layer or amorphous silicon layer can be formed by a chemical-vapor deposition (CVD) process; however, other suitable processes for forming the poly-silicon layer or amorphous silicon layer may be applied. In one embodiment, the poly-silicon layer or amorphous silicon layer can be doped with impurities at this stage, for example, doped with n-type impurities, so that the resulting pillar **300** has a suitable doping characteristic. A heat treatment can then be applied to the poly-silicon layer or amorphous silicon layer to convert the layer to a single-crystal silicon material. In one example embodiment, the heat-treatment can take the form of a laser-induced epitaxial growth (LEG) process to obtain the single-crystal silicon material, as is known in the art. In an alternative embodiment, single-crystal silicon pillars **300** can be grown in the openings **220** from the exposed upper surface of the substrate **100** using a selective epitaxial growth (SEG) process.

[0085] In one embodiment, the material used for forming the pillars **300** can be a same material as that used for forming the spacer layers **240**. In other embodiments, the spacer layers **240** can be removed prior to formation of the pillars **300**. In addition, the pillars **300** may be of a same dopant type as that of the substrate **100**.

[0086] Referring again to FIGS. **22** and **23**, the pillars PL may be formed to completely fill the openings **220** so that the pillars PL are solid, as shown in the embodiment of FIG. **22**. Alternatively, the pillars PL may be formed as "macaroni-type" pillars, whereby the pillars are hollow in shape, as shown in the embodiment of FIG. **23**, having a bottom and sidewalls **301**A, with a hollow central region **301**B, or, alternatively, a central region **301**B that is formed of an insulative material. The sidewalls can be cylindrical or rectangular in shape, and can fully surround the central region **301**B, or can be spaced apart and lie at opposed sides of the central region **301**B.

[0087] The resulting pillars **220** formed of a semiconducting material are in direct contact with the underlying substrate/well region **100** in a region of contact. The contact region includes a lower portion of the pillar **220** and an upper portion of the substrate **100**. Since they are in direct contact, a diode-type junction is not formed between the pillar **220** and the substrate **100**. This allows for the horizontal and vertical inversion regions **504**A, **504**B to be present during a read operation, as shown in FIG. **11** above, so that individual memory cells can be accessed.

[0088] Referring to FIGS. **19**A and **19**B, additional patterning is performed to so that the conductive gate layers **200**, including gate layers **201**, **202**, **203**, **204**, and **205** are patterned to form first through fourth word line plates WL_PT and the upper select line USL. The gate layers **200** are patterned in a stair-type pattern as shown in FIG. **3**, to provide vertical access to the plurality of gate layers **200**. The upper select line USL patterns **205** are each accessed by a contact plug **260**A. Also, in this embodiment, at an edge region of the device, a vertical opening is formed to expose the underlying substrate **100** by removing portions of the upper select line plate USL, the word line plates WL_PT and the lower select line plate LS_PT. A source region S is then formed at the top surface of the exposed substrate, as shown. The contact plug **260**B in connection with the underlying source region S is then formed with conductive material to fill the opening. Contact plugs **260**C are similarly formed in the peripheral region of the device to provide connectivity to source/drain regions **140** of the peripheral transistors. Drain regions D are formed at the tops of the pillars **300** using standard doping techniques. This process results in the formation of the source contact plug S_CT of the type shown in the configuration of FIGS. **2** and **3** above.

[0089] Alternatively, the source contact plug S_CT can be formed at the same time as the vertical pillars, for example, during the steps shown in FIGS. **18**A and **18**B above, which describe formation of pillars **300**. In this alternative embodiment, it is not necessary to remove corner portions of the upper select line plate USL, the word line plates WL_PT and the lower select line plate LS_PT, since the pillar for forming the source contact S_CT is formed through the plates, in the same manner as the vertical pillars **300**. As a result, the source contact plug S_CT of the type shown in the configuration of FIGS. **7**A and **7**B is formed.

[0090] Referring to FIGS. **20**A and **20**B, a first conductive layer **270** is formed on, and in contact with, the drain regions D of the pillars **300**. The first conductive layer **270**, the uppermost interlayer dielectric layer **216** and the uppermost con-

ductive gate layer **205** are then patterned to form upper select line USL patterns **205'** that extend in the second horizontal direction.

[0091] Referring to FIGS. **21**A and **21**B, the first conductive layer **270** is further patterned to provide pads **276** on the drains of the pillars **300**. In this example, contact plug **260**A in the memory cell region is connected to the contact plug **260**C in the peripheral region, to connect the upper select line USL to an associated source/drain region **140** of the peripheral transistor in the peripheral region. A first upper interlayer dielectric layer **280** is then formed on the resulting structure, and contact plugs **285** are formed to make contact with the underlying conductive components, in this case, pads **276** formed of the first conductive layer **270**. A second conductive layer is formed and patterned on the first upper interlayer dielectric layer **280** to form conductive lines **290** and features in contact with the underlying contact plugs **285**. In the memory cell area, conductive lines that connect to the drain regions D of vertical pillars that are arranged in the first horizontal direction provide bit lines BL of the device, as shown in FIG. **3**. A second upper interlayer dielectric layer **292** is then formed on the resulting structure, and contact plugs **294** formed to make contact with the underlying conductive components, in this case, contact with the rightmost feature **290** in turn in contact with the source contact plug **260**B in connection with the underlying source region S. A third conductive layer is formed and patterned on the second upper interlayer dielectric layer **292** to form conductive line **296** in contact with the underlying source contact plug **260**B.

[0092] In the above embodiment, the gate insulator **110** of the transistors in the peripheral region and the gate insulator **110** of the memory cell region are of the same thickness, as they are formed at the same time. Simultaneous formation of the gate insulator **110** provides for a more efficient fabrication process, thereby reducing fabrication costs.

[0093] In the above embodiment, the source/drain region **140** of the peripheral region transistors and the source region S of the memory cell region of the device are formed at different times in the process. For example, the source/drain region **140** of the peripheral region transistors are formed in connection with the process steps illustrated at FIGS. **13**A and **13**B, while the source region of the memory cell region of the device is formed just prior to the time of the formation of the source contact plug **260**B, in connection with the process steps illustrated at FIGS. **19**A and **19**B.

[0094] Referring to FIG. **24**, in another embodiment, the common source region S of the memory cell region of the device can be formed at the same time as the source/drain region **140** of the peripheral region transistors. For example at the time of patterning the gate pattern **125**, **135** of the peripheral transistor, the gate layers can also be patterned in the source region of the memory cell region, so that a source region S can be formed in the memory cell region using the lower gate pattern **125**, **135** in the memory cell region as an ion implantation mask, according to conventional fabrication techniques.

[0095] Also in the above embodiment, the thickness of the lower-most interlayer dielectric layer **110** in the memory cell region, that is the dielectric layer between the lowermost gate pattern **125** forming the lower select plate LS_PT and the substrate, and the thickness of the lower gate insulator **110** in the peripheral region, that is the insulative layer between the gate pattern **125**, **135** and the substrate **100** in the peripheral region, are the same, since the layer **110** is initially formed to cover the substrate **100** in both the peripheral and memory cell regions of the device.

[0096] Referring to FIG. **25**, in another embodiment, the thickness of the lower-most interlayer dielectric layer **110'** in the memory cell region, that is the dielectric layer between the lowermost gate pattern **125** forming the lower select plate LS_PT and the substrate, and the thickness of the lower gate insulator **110** in the peripheral region, that is the insulative layer between the gate pattern **125**, **135** and the substrate **100** in the peripheral region, can be different. In this case, the layers **110'**, **110** can be formed at different times, prior to formation of the first and second lower gate layer patterns **125**, **125** and **125'**. Also, where desired, the layers **110'**, **110** can be formed of different materials.

[0097] FIGS. **26-39** are perspective views of a method of forming a vertical-channel memory device, in accordance with another embodiment of the present invention.

[0098] Referring to FIG. **26**, a substrate **100** is prepared. In one embodiment, the substrate **100** comprises a single-crystal semiconductor material substrate that provides a seed layer for later formation of the single-crystal vertical pillars PL. In other embodiments the substrate comprises a polycrystalline semiconductor material. A lower-most interlayer dielectric layer **110** is provided on the substrate. In certain embodiments of the present invention, the lower-most interlayer dielectric layer **110** is sufficiently thin so that an inversion layer can be created in the underlying semiconductor material of the substrate **100** when a suitable voltage is applied to a resulting lowermost gate layer LS_PT (see FIG. **39**, below). Multiple alternating interlayer dielectric layers **210**, including in this example, layers **211**, **212**, **213**, **214**, **215**, and **216** and multiple sacrificial layers SC, including in this case, layers SC**1**, SC**2**, SC**3**, SC**4**, SC**5**, and SC**6** are formed on the lower-most interlayer dielectric layer **110**. In one embodiment, the interlayer dielectric layers **210** and the sacrificial layers SC have etch selectivity with respect to each other. For example, the interlayer dielectric layers **210** can comprise silicon nitride and the sacrificial layers SC can comprise silicon oxide. In one embodiment, the sacrificial layers SC are formed of a material that can readily be removed by a wet etching process.

[0099] Referring to FIG. **27**, first line-type openings **220** are formed through the interlayer dielectric layers **210**, the sacrificial layers SC, and the lower-most interlayer dielectric layer **110** in a vertical direction, and spaced apart in a horizontal direction, as shown. The first openings **220** expose upper portions of the underlying substrate **100** and extend in a first direction of horizontal extension.

[0100] Referring to FIG. **28**, a semiconductor liner layer **300** is formed on sidewalls and on a bottom of the first openings **220**. An insulating layer **310** is then provided to fill the remainder of the first openings **220**. The semiconductor liner layer will form the vertical pillars PL for the resulting device, and can be formed, for example, in the manner described above in connection with FIGS. **18**A and **18**B. In the present example, a "macaroni"-type pillar is shown. Referring to the close-up view of FIG. **23** described above, the "macaroni"-type pillar PL includes a cylindrical shell or walls of semiconductor material **301**A surrounding an insulative, or hollow, core **301**B

[0101] Referring to FIG. **29**, a plurality of second openings **225** extending in the first horizontal direction are formed between neighboring semiconductor liners **300**. In one

embodiment, the second openings **120** expose the lower-most interlayer dielectric layer **110**. This procedure permits access to a region where the control gates and floating gates of the resulting gate insulating layer **230** (see FIG. **31** below) of the memory device will be formed along sidewalls of the resulting semiconductor liner layers **300**, eventually comprising the vertical pillars of the device.

[0102] Referring to FIG. **30**, the sacrificial layer patterns SC including, for example, SC**1**, SC**2**, SC**3**, SC**4**, SC**5**, and SC**6** are removed by a wet etching process. In a case where the lower-most interlayer dielectric layer **110** is formed of a same material as the sacrificial layer patterns SC, exposed portions of the lower-most interlayer dielectric layer **110** are likewise removed. In an example where the sacrificial layer patterns SC are formed of silicon nitride, the etchant of the wet etching process can comprise an HF solution. Resulting concave openings **226** extend from the second opening **225** in the second horizontal direction of extension and lie adjacent the walls of the silicon semiconductor liners **300** to expose outer sidewalls thereof.

[0103] Referring to FIG. **31**, a gate insulating layer **230** is provided on the resulting structure. The gate insulating layer **230** covers interior walls of the concave openings **226**, including covering the exposed outer sidewalls of the semiconductor liners **300**. As described above in connection with FIG. **17** and FIGS. **22** and **23**, in certain embodiments, the gate insulating layer **230** can comprise a charge storage layer so that the device can operate as a non-volatile memory device. In some embodiments, the gate insulating layer **230** comprises a tunnel oxide layer **231**, a charge trapping layer **232** and a blocking insulating layer **233** that are sequentially formed in the second opening **225** and on lower, side, and upper walls of the concave openings **226**. In one embodiment, the tunnel oxide layer **231** can be formed using a thermal oxidation process, which makes it more resistant to degradation over time, leading to improved device reliability and endurance.

[0104] In various embodiments, the charge trapping layer **232** can be a floating-gate structure, for example, comprising a poly-silicon material, or can comprise an ONO (oxide-nitride-oxide) structure. A floating-gate charge trapping layer **232** is possible in accordance with the present embodiment, since access is gained at the concave openings **226**. The blocking oxide layer **233** can comprise, for example, silicon oxide, or other suitable high-k oxide layer.

[0105] Referring to FIG. **32**, a gate conductive layer **200'** formed of a conductive material is provided to fill the second openings **225**, including the concave openings **226**. In one embodiment, the conductive material comprises tungsten silicide.

[0106] Referring to FIG. **33**, the central portions of the gate conductive layer **200'** are etched, forming third openings **225'** that separate portions of the gate conductive layer **200'** into gate patterns **200"**, including gate patterns **201'**, **202'**, **203'**, **204'**, **205'** and **206'**. Lower-most gate pattern **201'** will become a lower select plate LS_PT for the device, while gate patterns **202'**, **203'**, **204'**, and **205'** will become word line plates WL_PT for the device. The upper-most gate pattern **206'** will become an upper select gate for the device. As a result of this processing step, lower-most gate pattern **201'** can remain intact, or partially etched, as shown, in a case where the lower select plate LS_PT operates as a select plate for all vertical pillars in the array. In an embodiment where the gate insulating layer **230** includes a charge trapping layer, this processing step also operates to separate the charge trapping layer into individual charge trapping layer patterns.

[0107] Referring to FIG. **34**, the third openings **225'** are filled with an insulative material to form an insulation pattern **180**.

[0108] Referring to FIG. **35**, the semiconductor liners **300** and associated insulating layers **310** are pattered and etched to form fourth openings **227** that separate the liners **300** in the first horizontal direction into independent vertical pillars **300'**. The fourth openings **227** are then filled with an insulating material to electrically insulate the vertical pillars **300'** in the first horizontal direction.

[0109] Referring to FIG. **36**, drain regions D are formed at the tops of the pillars **300'** using standard doping techniques. First conductive patterns **270** can then be formed and patterned to make electrical contact with the drain regions D of the tops of pillars **300'** arranged in a second horizontal direction of extension of the device.

[0110] Referring to FIG. **37**, an alternative embodiment is shown. In this embodiment, the pillars **300"** are solid semiconductor pillars PL, rather than the shell-type macaroni pillars **300'** of FIG. **36**. Also, in this embodiment, vertical contact plugs **285** make contact, in a vertical direction, with drain regions D at the tops of the pillars **300"**. The vertical contact plugs **285** are formed through an interlayer dielectric layer (not shown). First conductive patterns **290** are then formed and patterned to make electrical contact with the drain regions D of the tops of pillars **300'** arranged in the second horizontal direction of extension of the device.

[0111] Referring to FIGS. **38** and **39**, it can be seen that lower-most gate pattern **201'** provides a lower select plate LS_PT for the resulting device, while gate patterns **202'**, **203'**, **204'**, and **205'** provide word line plates WL_PT that are connected to global word lines GWL for the device. The word line plates WL_PT extend in the first direction of horizontal extension of the device. The upper-most gate patterns **206'** provide a plurality of upper select gates each select gate being connected to an independent upper select line USL for the device. The conductive patterns **270**, **290** extending in the second direction of horizontal extension of the device provide bit lines BL for the resulting device, each bit line connected to the drain regions of corresponding vertical pillars PL by bit line contacts BL_CT.

[0112] In the view of FIG. **39** it can be seen that the vertical pillars PL each include a body region B along most of its length and a drain region D at the top portion. The junction between the semiconducting body region B and the doped drain region D behaves as a diode junction. It can also be seen in this view that bottom portions of the pillars PL are directly connected to the underlying substrate or well **100**. Therefore, the bottom portions of the pillars PL at their intersection with the substrate do not behave as a diode junction, but rather as a direct, resistive, contact. Memory cells MC are positioned along the vertical pillars, each memory cell MC being accessed by an associated word lines plate WL_PT coupled to an associated global word line WL and associated bit line BL.

[0113] FIGS. **40**A-**42**A are cross-sectional views taken along section line I-I' of FIG. **2**, and FIGS. **40**B-**42**B are cross-sectional views taken along section line II-II' of FIG. **2**, of a method of forming a vertical-channel memory device, in accordance with another embodiment of the present invention.

[0114] Referring to FIGS. **40**A and **40**B, in the present embodiment, the upper select line USL, rather than being

initially formed as a continuous plate (see, for example, uppermost gate layer **205** of FIGS. **15**A and **15**B) that is later patterned during the processing steps shown and described in connection with FIGS. **20**A and **20**B, can instead be initially patterned to form individual lines **205** that extend in the second horizontal direction of extension, as shown in FIGS. **40**A and **40**B.

[0115] Referring to FIGS. **41**A and **41**B, the vertical openings **220** can then formed as shown to pass through the central portions of the lines **205**, according to the processing steps described above in connection with FIGS. **16**A and **16**B.

[0116] Referring to FIGS. **42**A and **42**B, processing steps can be performed to complete the resulting device, for example, according to the manner described above in connection with FIGS. **17**A, B-**21**A, B.

[0117] FIG. **43** is a block diagram of a memory card that includes a semiconductor device in accordance with the embodiments of the present invention. The memory card **1200** includes a memory controller **1220** that generates command and address signals C/A and a memory module **1210** for example, flash memory **1210** that includes one or a plurality of flash memory devices. The memory controller **1220** includes a host interface **1223** that transmits and receives command and address signals to and from a host, a controller **1224**, and a memory interface **1225** that in turn transmits and receives the command and address signals to and from the memory module **1210**. The host interface **1223**, the controller **1224** and memory interface **1225** communicate with controller memory **1221** and processor **1222** via a common bus.

[0118] The memory module **1210** receives the command and address signals C/A from the memory controller **1220**, and, in response, stores and retrieves data DATA I/O to and from at least one of the memory devices on the memory module **1210**. Each memory device includes a plurality of addressable memory cells and a decoder that receives the receives the command and address signals, and that generates a row signal and a column signal for accessing at least one of the addressable memory cells during programming and read operations.

[0119] Each of the components of the memory card **1200**, including the memory controller **1220**, electronics **1221**, **1222**, **1223**, **1224**, and **1225** included on the memory controller **1220** and the memory module **1210** can employ vertically oriented memory devices of the type disclosed herein.

[0120] FIG. **44** is a block diagram of a memory system **1300** that employs a memory module **1310**, for example, of the type described herein. The memory system **1300** includes a processor **1330**, random access memory **1340**, user interface **1350** and modem **1320** that communicate via a common bus **1360**. The devices on the bus **1360** transmit signals to and receive signals from the memory card **1310** via the bus **1360**. Each of the components of the memory system **1300**, including the processor **1330**, random access memory **1340**, user interface **1350** and modem **1320** along with the memory card **1310** can employ vertically oriented memory devices of the type disclosed herein. The memory system **1300** can find application in any of a number of electronic applications, for example, those found in consumer electronic devices such as solid state disks (SSD), camera image sensors (CIS) and computer application chip sets.

[0121] The memory systems and devices disclosed herein can be packaged in any of a number of device package types, including, but not limited to, ball grid arrays (BGA), chip scale packages (CSP), plastic leaded chip carrier (PLCC) plastic dual in-line package (PDIP), multi-chip package (MCP), wafer-level fabricated package (WFP), and wafer-level processed stock package (WSP).

[0122] Although the above examples illustrate only four memory cell transistors MC in each vertical channel for purposes of clear illustration of the embodiments of the present invention, embodiments of the present invention are not thus limited, and can include as few as one memory cell transistor in each vertical channel, and as many memory cell transistors in vertical channel as desired for the application, for example, two, four, eight, sixteen, or thirty-two memory cell transistors in each vertical channel.

[0123] While embodiments of the invention have been particularly shown and described with references to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A semiconductor device comprising:

a substrate of semiconductor material extending in a horizontal direction;

a plurality of interlayer dielectric layers on the substrate;

a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; and

a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconducting region.

2. The semiconductor device of claim **1** wherein the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

3. The semiconductor device of claim **1** wherein the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region

4. The semiconductor device of claim **1** wherein the semiconductor device comprises a semiconductor memory device and wherein:

an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor;

a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor;

remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device; and further comprising:

a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness,

wherein the first thickness is less than the second thickness; and

wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

5. The semiconductor device of claim **1** wherein the semiconductor material of the vertical channel is selected from the group consisting of a single-crystal semiconductor material and a polycrystalline semiconductor material.

6. The semiconductor device of claim **1** wherein the semiconductor material of the substrate is selected from the group consisting of a single-crystal semiconductor material and a polycrystalline semiconductor material.

7. The semiconductor device of claim **1** wherein the gate insulating layer includes a charge storage layer and wherein the semiconductor device comprises a non-volatile memory device.

8. The semiconductor device of claim **1** wherein:

an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor;

a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor;

remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device;

control gates of memory cell transistors sharing a same layer of the device arranged in horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device;

memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel;

upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors;

upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device; and

the semiconductor device comprises a semiconductor memory device.

9. A memory system comprising:

a memory controller that generates command and address signals; and

a memory module comprising a plurality of memory devices, the memory module receiving the command and address signals and in response storing and retrieving data to and from at least one of the memory devices,

wherein each memory device comprises:

a substrate of semiconductor material extending in a horizontal direction;

a plurality of interlayer dielectric layers on the substrate;

a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; and

a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconducting region.

10. The memory system of claim **9** wherein the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region

11. The memory system of claim **9** wherein the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region

12. The memory system of claim **9** wherein:

an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor;

a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor; and

remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device;

and further comprising:

a gate insulating layer between the lower select gate and the substrate, the gate insulating layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness,

wherein the first thickness is less than the second thickness; and

wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

13. The memory system of claim **9** wherein the gate insulating layer includes a charge storage layer and wherein the memory device comprises a non-volatile memory device.

14. The memory system of claim **9** wherein:

an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor;

a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor;

remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device;

control gates of memory cell transistors sharing a same layer of the device arranged in horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device;

memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel;

upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors; and

upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device.

15. A method of fabricating a semiconductor device comprising:

providing a substrate of semiconductor material extending in a horizontal direction;

providing a plurality of interlayer dielectric layers on the substrate;

providing a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer;

providing a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns; and

providing a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel,

wherein the vertical channel is in contact with the substrate at a contact region that comprises a semiconducting region.

16. The method of claim **15** wherein the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

17. The method of claim **15** wherein the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region.

18. The method of claim **15** wherein the semiconductor device comprises a semiconductor memory device and wherein:

an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor;

a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor;

remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device;

and further comprising:

providing a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness,

wherein the first thickness is less than the second thickness; and

wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

19. The method of claim **15** wherein the gate insulating layer includes a charge storage layer and wherein the semiconductor device comprises a non-volatile memory device.

20. A method of performing an erase operation on a semiconductor memory device,

the semiconductor memory device comprising:

a substrate of semiconductor material extending in a horizontal direction;

a plurality of interlayer dielectric layers on the substrate;

a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer; and

a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconductor material,

wherein:

an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor;

a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor;

remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device;

control gates of memory cell transistors sharing a same layer of the device arranged in horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device;

memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel;

upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors; and

upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device;

the erase operation comprising:

placing the lower select gate and the upper select gate of the common string in a floating state;

applying a ground or positive voltage to the word lines; and

applying a positive erase voltage to the semiconductor substrate.

21. The method of claim **20** wherein the contact region comprises an upper surface of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

22. The method of claim **20** wherein the contact region is conductive upon the application of a voltage that creates an inversion region in the contact region.

23. The method of claim **20** further comprising:

providing a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness,

wherein the first thickness is less than the second thickness; and

wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

24. A method of performing a read operation on a semiconductor memory device,

the semiconductor memory device comprising:

a substrate of semiconductor material extending in a horizontal direction;

a plurality of interlayer dielectric layers on the substrate;

a plurality of gate patterns, each gate pattern between a neighboring lower interlayer dielectric layer and a neighboring upper interlayer dielectric layer;

a vertical channel of semiconductor material extending in a vertical direction through the plurality of interlayer dielectric layers and the plurality of gate patterns, a gate insulating layer between each gate pattern and the vertical channel that insulates the gate pattern from the vertical channel, the vertical channel being in contact with the substrate at a contact region that comprises a semiconducting region;

wherein:

an upper-most gate pattern of the plurality of gate patterns comprises an upper select gate of an upper select transistor;

a lower-most gate pattern of the plurality of gate patterns comprises a lower select gate of a lower select transistor;

remaining gate patterns of the plurality of gate patterns between the upper select gate and the lower select gate comprise control gates of memory cell transistors of a common string of the semiconductor device;

control gates of memory cell transistors sharing a same layer of the device arranged in horizontal direction of the semiconductor device are connected to provide word lines of the semiconductor device;

memory cell transistors of a common string of the semiconductor device are coupled together in series by the vertical channel;

upper-most gate patterns sharing a same layer of the device arranged in a first horizontal direction of the semiconductor device are connected to provide upper select gates of upper select transistors; and

upper portions of vertical channels arranged in a second horizontal direction of the semiconductor device are connected to provide bit lines of the semiconductor device;

the read operation comprising:

applying a ground voltage to the semiconductor substrate;

applying a read voltage to control gates of unselected memory cell transistors of the common string;

applying a read voltage to gates of selected upper select transistors of the common string;

applying a criterion voltage to control gates of selected memory cell transistors of the common string; and

applying a read voltage to the lower select gate of the lower select transistor of the common string and of neighboring strings to thereby create an conductive inversion layer at an upper region of the semiconductor substrate and at a lower region of at least sidewalls of the vertical channel in the contact region, the inversion layer operating as a conductive common source line for the semiconductor memory device during the read operation.

25. The method of claim **24** wherein the contact region comprises the upper region of the substrate and a lower portion of the vertical channel, and wherein the upper surface of the substrate and at least sidewalls of the lower portion of the vertical channel comprise a semiconducting region.

26. The method of claim **24** further comprising:

providing a lower-most interlayer dielectric layer of the plurality of interlayer dielectric layers between the lower select gate and the substrate, the lower-most interlayer dielectric layer being of a first thickness and wherein the interlayer dielectric layers between the control gates are of a second thickness,

wherein the first thickness is less than the second thickness; and

wherein the first thickness is selected so that a voltage applied to the lower select gate creates an inversion layer in the contact region that causes the contact region to conduct.

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