

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.
Petitioner

v.

MICRON TECHNOLOGY, INC.
Patent Owner

IPR2025-00499
U.S. Patent No. 8,803,214

**DECLARATION OF DR. KELIN J. KUHN IN SUPPORT OF PETITION
FOR *INTER PARTES REVIEW* OF U.S. PATENT 8,803,214**

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I, Kelin Kuhn of Winthrop, Washington, declare that:

I. Introduction

1. My name is Dr. Kelin J. Kuhn, and I am an adjunct professor in the Materials Science and Engineering Department at Cornell University. I have been retained on behalf of Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Petitioner”), to provide my opinions on certain issues related to U.S. Patent No. 8,803,214 (“the ’214 patent”) in connection with the above-captioned *inter partes* review (IPR) proceeding. In particular, I have been asked to provide my insights, analysis, and opinions regarding whether claims 8, 13, and 21 of the ’214 patent (“challenged claims”) are anticipated by and/or obvious over the prior art references identified below.

2. I understand that the ’214 patent is titled “Three Dimensional Memory and Methods of Forming the Same,” names inventors Sanh D. Tang and John K. Zahurak, and is currently owned by Micron Technology, Inc. (“Micron” or “Patent Owner”). I have considered the ’214 patent. I understand that the ’214 patent has been provided as EX1001.

3. I understand that the file history of the ’214 patent has been provided as EX1002. I have considered this file history, and I will refer to it as “the ’214 file history.”

4. I understand that the ’214 patent is issued from U.S. Patent Application

No. 12/825,211, with a filing date of June 28, 2010. The '214 patent does not claim any priority date before June 28, 2010. I have been asked to assume that June 28, 2010 filing date as the purported invention date for purposes of rendering my opinions in this declaration.

5. My analysis and conclusions set forth in this declaration are based on my educational background and experiences in the field (see Section II). Before June 28, 2010, my level of skill in the art was at least that of a person of ordinary skill in the art ("POSITA"). I am qualified to opine concerning what a POSITA would have known and understood at the time of the '214 patent's purported invention. My analysis and conclusions herein are from the perspective of a POSITA as of June 28, 2010.

6. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were commonly known to persons of ordinary skill in this art during the time before the earliest claimed priority date for the '214 patent; my own knowledge and experiences gained from my work experience in the field of the '214 patent and related disciplines; and my experience in working with others involved in this field and related disciplines.

7. I am being compensated by YMTC at my standard hourly consulting rate of \$600 for my time on this matter. My compensation is not dependent on the

outcome of this proceeding or any other proceeding between the parties.

8. As set forth herein, I have concluded that each of the challenged claims is anticipated and/or rendered obvious by the prior art based on the references described below and as described herein. In forming my opinions, I relied on the documents cited in this declaration, which are identified in Section IV. These documents include patents, file histories, printed publications, and other related documents. As discussed below, each document is a type that experts in my field would have reasonably relied upon when forming their opinions. Further, experts in my field would have had access to each document either through the applicable patent offices and/or well-known libraries, conferences, or publications in the field. My opinions are also based upon my personal and professional experience.

II. Background and Qualifications

9. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

10. I am qualified by education and experience to testify as an expert in the field of nonvolatile memory devices. Additionally, the following overview of my background pertains to my qualifications for providing expert testimony in this matter. I am over the age of 18 and am competent to write this declaration. I have personal knowledge, or have developed knowledge, of these technologies based

upon education, training, or experience of the matters set forth herein.

11. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

12. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

13. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

14. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam epitaxy and optoelectronics, and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

15. In 1997, I joined Intel Corporation ("Intel") at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel

0.35 μ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

16. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

17. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel's 90 nm communications process technology. Over a three-year period, my team developed a derivative analog/RF technology (including a SiGe bipolar junction transistor ("BJT")) on top of Intel's premium 90 nm microprocessor process.

18. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel's 45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

19. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement

within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel's FinFET device). I received a second Intel achievement award in 2008 for my work on Intel's FinFET device.

20. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten year time frame.

21. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond: Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper "Considerations for Ultimate CMOS Scaling" (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

22. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course,

protected by client confidentiality, these projects include FinFETs, vertical power transistors, solar cells, conventional (planar) MOS, and flash.

23. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

24. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

25. A few representative book chapters include, “The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications,” Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).

26. I am an inventor of approximately 80 granted U.S. patents in the field of semiconductor technology.

27. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.

28. As specifically relevant to this project, I want to highlight the 3’D gate-last vertical gate-all-around (GAA) devices and the 3’D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight recent proprietary and confidential work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

29. Attached as Appendix A to this report is a current copy of my curriculum vitae, which outlines my academic, professional and experiential qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

III. Level of Ordinary Skill in the Art

30. In rendering the opinions set forth in this declaration, I was asked to

consider the patent claims and the prior art through the eyes of a POSITA at the time of the alleged invention. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field, the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art including the art cited below.

31. Upon consideration of the relevant factors listed above, in my opinion, a POSITA at the time of the claimed invention, would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa.

32. Well before June 28, 2010, my level of skill in the art was at least that of a person having ordinary skill. I am qualified to opine concerning what a POSITA would have known and understood at the time of the '214 patent's purported invention. My analysis and conclusions herein are from the perspective of a POSITA as of June 28, 2010. A different invention date would not change my opinions as long as the identified prior art were still prior art.

IV. Materials Considered and Relied Upon

33. In reaching the conclusions described in this declaration, I have relied on the documents and materials cited herein as well as those identified in this Declaration, including but not limited to, the '214 patent, the prosecution history of the '214 patent, and prior art references cited herein. These materials include patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions.

34. In the cited references, all emphasis is added unless otherwise noted.

35. I have also relied on my education, training, research, knowledge, and personal and professional experience in the relevant technologies that were already in use prior to the claimed invention.

- EX1001: U.S. Patent No. 8,803,214 to Tang *et al.* (“the '214 patent”).
- EX1002: Prosecution History of the '214 patent (“the '214 file history”).
- EX1004: U.S. Patent Application Publication No. 2011/0286283 in the name of Lung *et al.* (“Lung”).
- EX1005: U.S. Patent Application Publication No. 2010/0120214 in the name of Park *et al.* (“Park”).

- EX1006: U.S. Patent Application Publication No. 2008/0242028 in the name of Mokhlesi *et al.* (“Mokhlesi”).
- EX1007: U.S. Patent Application Publication No. 2009/0146190 in the name of Fukuzumi *et al.* (“Fukuzumi”).
- EX1008: Joint Claim Construction and Prehearing Statement and Appendices (Patent Local Rule 4-3), Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC., No. 3:23-cv-05792-RFL, D.I. 105 (N.D. Cal. August 19, 2024) (“Claim Construction”).
- EX1009: S. Zhang *et al.*, “Metal Silicides in CMOS Technology: Past, Present, and Future Trends,” Critical Reviews in Solid State and Materials Sciences, vol. 28, no. 1, pp. 1-129, March 2003 (“Zhang”).
- EX1010: J. Jang *et al.*, “Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193 (“Jang”).
- EX1012: R. Katsumata *et al.*, “Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Operation for Ultra High Density Storage Devices,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 136-137 (“Katsumata”).

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- EX1013: T. Maeda *et al.*, “Multi-Stacked 1G Cell/Layer Pipe-Shaped BiCS Flash Memory,” 2009 Symposium on VLSI Circuits, Kyoto, Japan, 2009, pp. 22-23 (“Maeda”).
 - EX1014: J. Trattles *et al.*, “Three-dimensional Finite-Element Investigation of Current Crowding and Peak Temperatures in VLSI Multilevel Interconnections,” IEEE Transactions on Electron Devices, vol. 40, no. 7, pp. 1344-1347, July 1993 (“Trattles”).
 - EX1015: D. Hisamoto *et al.*, “Sub-10-ps Gate Delay by Reducing the Current Crowding Effect at An Extension,” International Electron Devices Meeting. IEDM Technical Digest, Washington, DC, USA, 1997, pp. 239-242 (“Hisamoto”).
 - EX1019: H. Wong *et al.*, “On the Reliability Issues of RF CMOS Devices,” 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings, Shanghai, China, 2006, pp. 1105-1108 (“Wong”).
 - EX1017: U.S. Patent Application Publication No. 2009/0310425 in the name of Sim *et al.* (“Sim”).

V. Legal Standards

36. I am not an attorney and offer no legal opinions, but in the course of

my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

37. In formulating my opinions, I have been informed of certain legal understandings relevant to my opinions. In formulating my opinions, I have relied on the legal understandings I have been provided with as set forth in this declaration.

38. I have been informed that in *inter partes review* proceedings, invalidity must be shown under a preponderance of the evidence standard.

A. My Understanding of Claim Construction

39. I have been informed that patent claims are construed from the viewpoint of a POSITA of the patent at the time of the invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a POSITA in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification, and the prosecution history (i.e., the intrinsic record).

40. I have further been informed that a POSITA must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is

a record of the proceedings before the U.S. Patent and Trademark Office and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner's rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or clearly and unambiguously disavowing claim coverage.

41. In interpreting the meaning of the claim language, I understand that a POSITA may also consider “extrinsic” evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. For example, this can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

B. My Understanding of Anticipation

42. I understand that a patent claim is invalid as “anticipated” if all the limitations of the claim are present, either expressly or inherently, in a single prior

art publication or patent.

43. I also understand that a prior art reference can disclose a claimed feature because the feature is expressly described or because the feature is inherent in the disclosure. I understand that something is inherent in a prior art reference if the missing descriptive matter must necessarily be present, not merely probably or possibly present, and it would be so recognized by a POSITA as of the priority date of the patent. I understand that it is acceptable to examine evidence outside of the prior art reference (i.e., extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it.

44. I have further been informed that where a reference discloses multiple embodiments, the reference should not be limited to a preferred embodiment. Instead, each disclosed embodiment may anticipate.

45. Moreover, I have been informed that as part of an anticipation analysis, it is proper to take into account not only specific teachings of the reference, but also the inferences that one skilled in the art would reasonably be expected to draw therefrom. A reference can anticipate a claim even if it does not expressly spell out all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would at once envisage the claimed arrangement or combination.

C. My Understanding of Obviousness

46. I understand that a claim may be invalid if the subject matter described by the claim as a whole would have been obvious to a hypothetical POSITA in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a hypothetical POSITA and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

47. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it

deals, logically would have commended itself to a patentee's attention in considering their problem.

48. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

49. I have also been advised that in considering whether a claimed invention would have been obvious over a combination of prior art references, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a POSITA. I understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if POSITA can implement a predictable variation, the variation is likely obvious;

- If a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls whether the claim is obvious;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;
- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
- "Common sense" teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a POSITA will be able to fit the teachings of multiple patents together like pieces of a puzzle;
- A POSITA is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was "obvious to try," particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such

that a POSITA would have had good reason to pursue the known options within his or her technical grasp; and

- One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

50. I further understand that, in making a determination as to whether the claimed invention would have been obvious to a POSITA, the Board may consider certain objective factors if they are present, such as: commercial success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence, and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with predictable results) that is sufficiently strong.

VI. Technology Background

51. Three-dimensional (3D)—or vertical—NAND flash memory is a type of nonvolatile memory in which the memory cells are stacked vertically in multiple layers/levels to increase storage density, compared with traditional two-

dimensional (2D)—or planar—NAND flash memory, where the memory cells are arranged in a simple 2D matrix.

52. A typical 3D NAND memory device includes memory cells and their gate lines (e.g., word lines) are arranged at different vertical levels in 3D. One example of 3D NAND memory device back in 2009 is shown in FIG. A of my Declaration below (FIG. 1 of Jang), which shows a perspective view of a 3D memory structure. EX1010, FIG. 1.

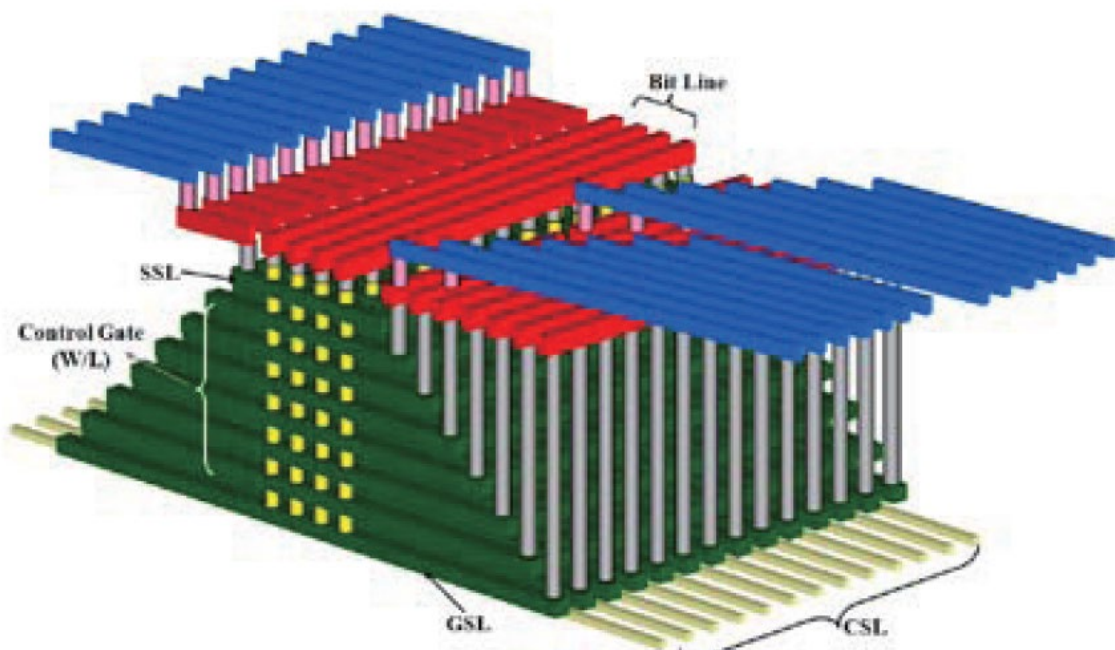


FIG. A – FIG. 1 of Jang

53. As shown in FIG. A above, the 3D memory device includes bit lines (in red), multiple levels of gate lines (in dark green), such as control gates/word lines W/L and select lines SSL/GSL. A common source line CSL (in light yellow) is formed on a substrate (not shown). EX1010, p. 192, Architecture and Key Features

of TCAT Flash.

54. A vertical structural component of Jang's memory device is the semiconductor pillars (in yellow), which penetrate the select lines SSL/GSL and word lines W/L to electrically connect the bit lines with the common source line CSL at opposite ends. These semiconductor pillars correspond to NAND cell strings, where each string includes multiple memory cells connected in series between a drain-side select transistor and a source-side select transistor. Memory cells are formed at the cross-points between the control gates/word lines W/L and the semiconductor pillars. Each memory cell has a "SONOS" type cell structure, which refers to "silicon-oxide-nitride-oxide-silicon," where the middle silicon nitride layer "N" is used as the charge storage memory element. EX1010, p. 192, Architecture and Key Features of TCAT Flash.

VII. Overview of the '214 Patent

A. Subject Matter Overview

55. The '214 patent was issued on August 12, 2014, from U.S. Patent Application No. 12/825,211 ("the '211 application"), filed on June 28, 2010. EX1001, (10), (21), (22).

56. The '214 patent is directed to nonvolatile memory devices and addresses fabrication challenges associated with three-dimensional (3D) memory structures. EX1001, 1:6-8; 2:63-67. The '214 patent states that "[s]ince 3D memory

devices are relatively new, manufacturing these devices can pose fabrication process challenges,” and thus, seeks to mitigate through novel device structures and fabrication methods. EX1001, 1:20-22, 12:30-31.

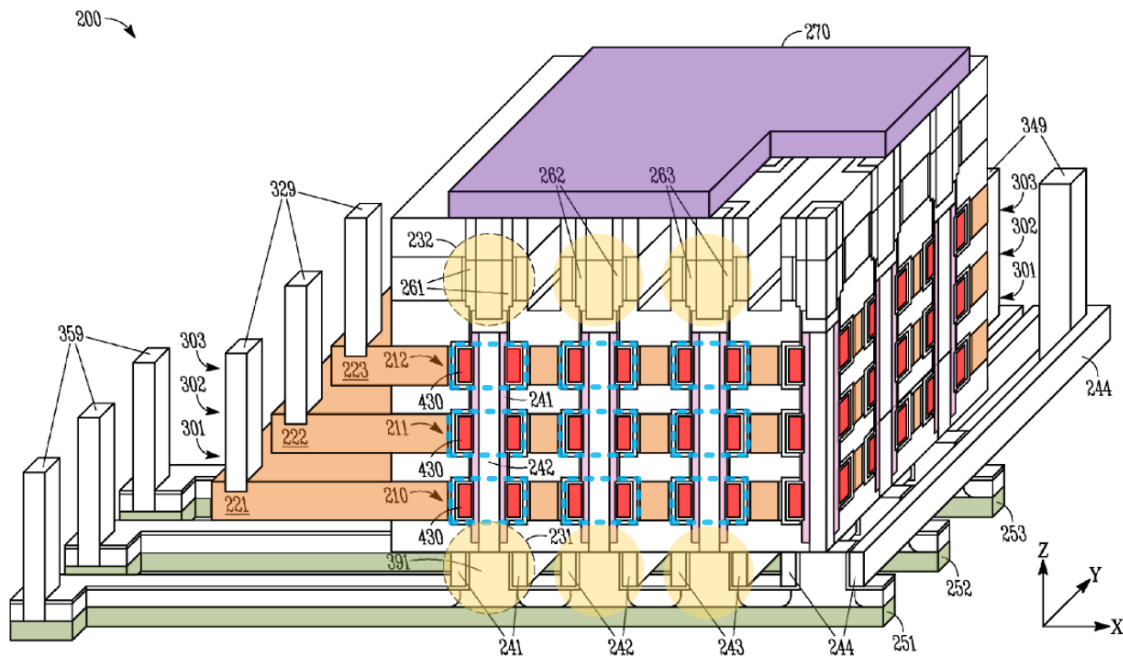


FIG. 3

FIG. B – FIG. 3 of the '214 patent (annotated)

57. The disclosed memory devices include multiple groups of memory cells arranged at different device levels. EX1001, 12:32-41. One such embodiment related to the challenged claims is depicted in FIG. 3 of the '214 patent (FIG. B of my Declaration with annotations) above, illustrating a memory device 200, which includes a string of memory cells 210-212 arranged in the Z-direction, with channel 241 (in pink) extending in the Z-direction through ring-shaped memory elements 430 (in red) of memory cells 210-212. EX1001, 3:65-4:33.

58. Memory elements 430, which are formed within cavities (enclosed within blue dashed boxes) of control gates 221-223 (in orange), function to store charge. EX1001, 4:34-5:3, 7:43-8:38.

59. Additionally, the memory device includes a common source 270 (in purple) positioned above memory cells 210-212. This common source is coupled to channels 241 through upper select transistors 232 (in yellow). Meanwhile, data lines 251-253 (in green) are located below memory cells 210-212 and are coupled to channels 241 through lower select transistors 231 (in yellow). EX1001, 4:9-33, 5:7-11, 5:39-51, 9:56-64.

60. Furthermore, the '214 patent discloses "a substrate underneath data lines 251, 252, and 253," even though it is not explicitly shown in FIG. 3. EX1001, 4:9-14.

B. File History of the '214 Patent

61. I have reviewed the file history of the '214 patent. Upon the issuance of the Non-Final Office Action dated June 7, 2012, claims 1-34 were pending in the application, wherein claims 22-34 were withdrawn, claims 1-6 and 9-21 were rejected under Pre-AIA 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2009/0230454 in the name of Pekny ("Pekny"), and claims 7 and 8 were rejected under Pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Pekny in view of U.S. Patent Application Publication No.

2007/0057310 in the name of Matsui *et al.* (“Matsui”). EX1002, 206-215.

62. In the Response to the Non-Final Office Action dated September 7, 2012, applicant of the ’214 patent amended the claims and argued that Pekny failed to disclose that the first memory cells/first control gate/first conductive material and the second memory cells/second control gate/second conductive material are formed in different device levels (claims 1 and 15), and that the memory elements have a ring shape (claim 9). EX1002, 149-159.

63. Following these amendments, the Examiner maintained the rejection of claims 9-14 over Pekny while allowing claims 1-8 and 15-21 in the Final Office Action dated February 1, 2013. EX1002, 138-141. The allowable subject matter related to the claimed “a plurality of second memory cells” in claim 1, the claimed “a common source,” “data lines,” and the relative positions between “the first and second memory cells,” “the common source,” and “the substrate” in claim 4 (issued as independent claim 8), and the claimed “a second conductive material” in claims 15 and 20 (issued as independent claim 21). EX1002, 141-142.

64. In the Response to the Final Office Action dated April 30, 2013, the applicant of the ’214 patent further amended claim 9 to specify that the first and second memory elements are in different device levels. EX1002, 122-128.

65. Finally, the Examiner allowed all claims in two Notices of Allowance, dated May 28, 2013 and March 31, 2014, stating that the prior art on record did not

teach certain claim limitations, including the claimed “a second control gate” and “data lines” in then-claims 1, 4, 9, and 20, as well as “a second dielectric” and “a conductive channel” in claim 15. EX1002, 40-41, 102-103.

C. Interpretation of the ’214 Patent Challenged Claims

66. I have been instructed that the challenged claims of the ’214 patent are to be given their ordinary and customary meaning as understood by a POSITA at the time of the alleged invention in light of the specification and the prosecution history pertaining to the patent, except as provided below. I have followed these principles in my analysis set forth in this document. I reserve the right to supplement my opinions in this declaration to the extent that any parties later propose claim constructions for any claim terms in the ’214 patent.

67. I understand that the term “cavity” recited in challenged claims 8 and 21 is also recited in claims 1 and 17 of U.S. Patent No. 10,872,903 (“the ’903 patent”), which is one of the continuations of the ’214 patent and is asserted in a pending district court litigation between YMTC and Micron (“YMTC Litigation”).

68. I understand that in the YMTC Litigation, Petitioner proposes that “a [first-fourth] cavity of [first/second] control gate” should be construed as “a [first-fourth] hole with a larger diameter than holes in the layers immediately above and below the [first/second] control gate.” (“Petitioner’s Construction”). EX. 1008, 17-18. I also understand that Patent Owner asserts that those terms should be given their

plain and ordinary meaning, without specifying what it believes the plain and ordinary meaning is (“PO’s Construction”). EX. 1008, 17-18. As I explain below with respect to Grounds 1-4, the challenged claims are anticipated and/or rendered obvious by the prior art under either party’s construction.

VIII. Overview of the Cited References

69. General descriptions provided for the following references and combinations thereof are incorporated into each subsection and mapping of the claims that include citations to these references.

A. Lung (EX1004)

70. Lung relates to 3D memory devices comprising multiple planes of memory cells. EX1004, [0002]. Lung acknowledges that “the need for higher and higher memory capacity in integrated circuit memory devices continues to increase” and that “[3D] stacking is an efficient way to reduce the cost per bit for semiconductor memory.” EX1004, [0007], [0110].

71. Lung thus provides 3D memory devices featuring “a large number of stackable layers of cells, resulting in a high-density NAND architecture flash memory device which overcomes the prior art limitation on the number of stackable layers of cells imposed by the impedance of a vertical string of cells of a single NAND string.” EX1004, [0009].

72. In Lung’s main embodiment, as depicted in FIG. 4 (FIG. C of my

Declaration with annotations) below, 3D memory device 100 comprises bit lines 134-136 (in green) positioned over a substrate (not shown), select lines 137-139 (in yellow) for the bottom set of pillar select transistors 106 (shown in FIG. 1) located over bit lines 134-136, word lines 410-418 (in orange) arranged at various levels above select lines 137-139, and a common source plane 147 (in purple) positioned above word lines 410-418. EX1004, [0054], [0057].

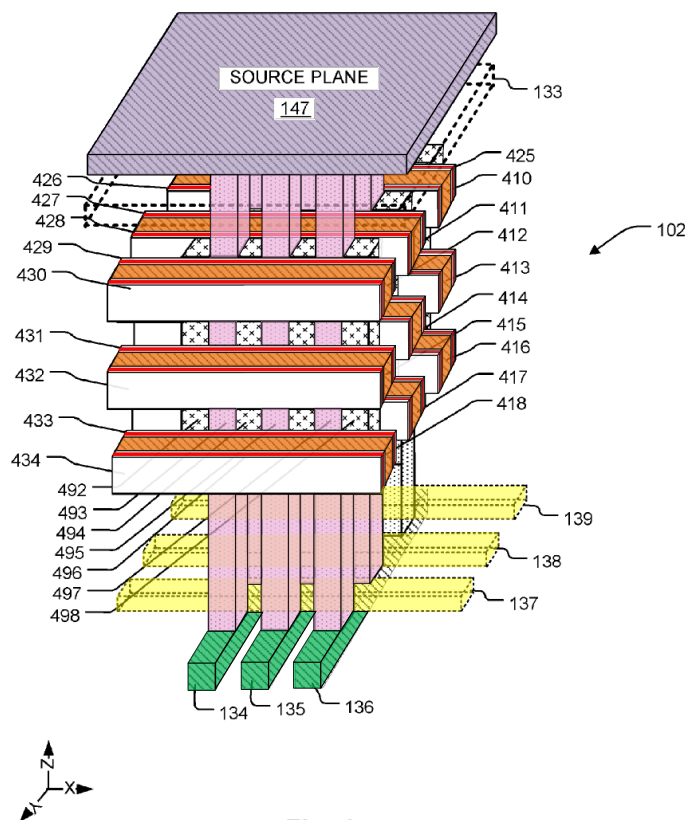


Fig. 4

FIG. C – FIG. 4 of Lung

73. Additionally, 3D memory device 100 includes an array of semiconductor pillars 493, 495, and 497 (in pink), which vertically extend between common source plane 147 and bit lines 134-136. Charge storage structures 425-434

(in red) are located on opposing sides of word lines 410-418. EX1004, [0054], [0057]. Multiple levels of memory cells are formed at the cross-points of semiconductor pillars 493, 495, and 497 and charge storage structures 425-434 above bit lines 134-136. EX1004, [0057].

74. FIG. 5 of Lung (FIG. D of my Declaration with annotations) below illustrates memory cells 500-L/R, 502-L/R, and 504-L/R positioned at three different levels in the Z-direction. EX1004, [0058]-[0062].

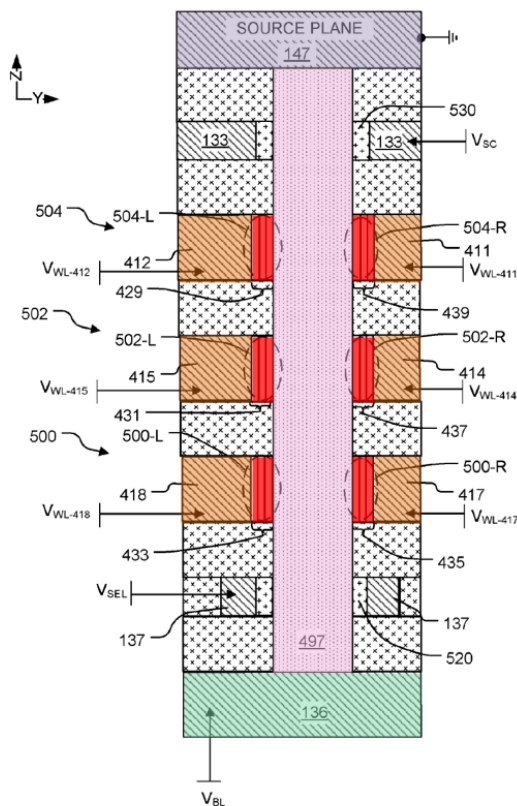


Fig. 5

FIG. D – FIG. 5 of Lung

75. Each memory cell 500-L/R, 502-L/R, or 504-L/R includes a portion of a respective word line 418, 417, 415, 414, 412, or 411 (in orange) serving as the

gate, along with a respective charge storage structure 433, 435, 431, 437, 429, or 439 (in red) acting as the charge storage element. EX1004, [0059]-[0061]. Each charge storage structure 429, 431, 433, 435, 437, or 439 is positioned between the respective word line 412, 415, 418, 417, 414, or 411 and semiconductor pillar 497 (in pink). EX1004, [0058].

76. Lung further discloses that the charge storage structure has an “ONO” structure, comprising “a tunneling layer in contact with the word line, a charge trapping layer over the tunneling layer, and a blocking layer over the charge trapping layer.” EX1004, [0011], [0052].

B. Park (EX1005)

77. Park is directed to a “nonvolatile memory device having a three-dimensional structure” and the manufacturing method thereof. EX1005, [0002]. Park aims to “improv[e] reliability” of the 3D memory devices. EX1005, [0002].

78. One exemplary 3D NAND memory device in Park’s first embodiment in connection with FIGs. 2-10 is shown in FIGs. 2 and 3 of Park (FIG. E of my Declaration with annotations) below, which shows a perspective view and a cross-sectional view of the 3D memory structure. EX1016, [0020]-[0022].

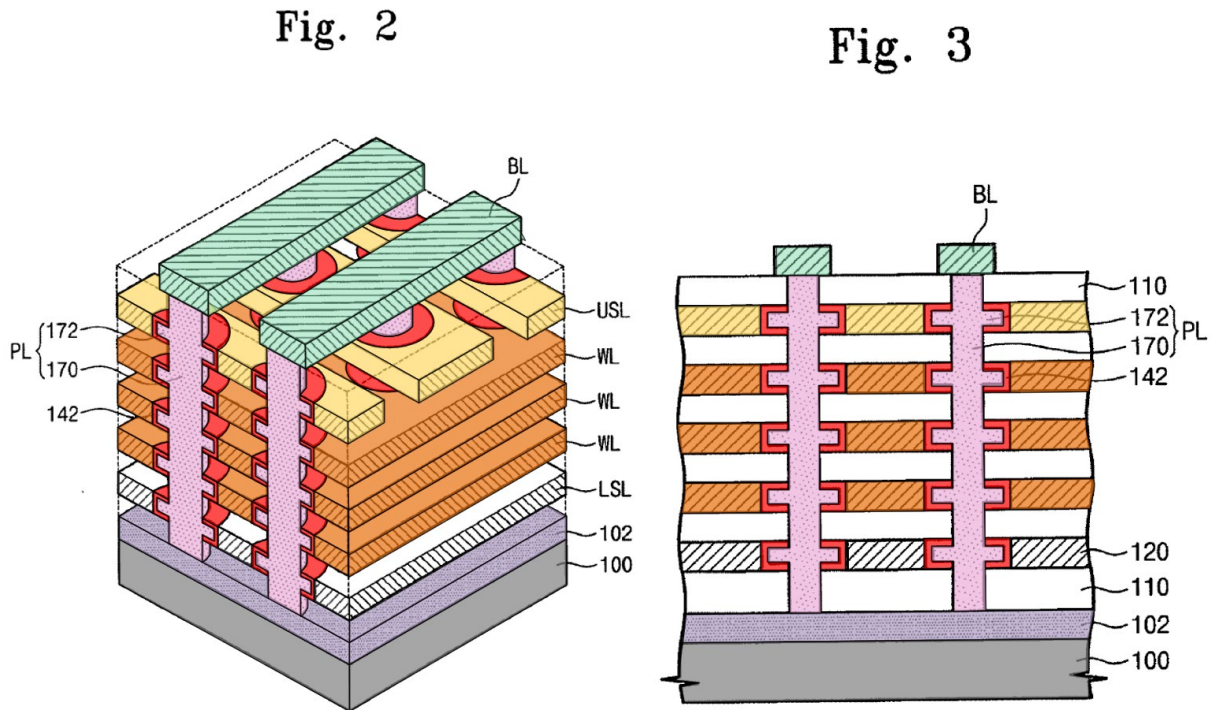


FIG. E – FIGs. 2 and 3 of Park

79. The 3D memory device comprises bit lines BL (in green) positioned above upper select lines USL (in yellow), multiple levels of word lines WL (in orange), and lower select lines LSL (white hatched). A common source line CSL is formed by an impurity region 102 (in purple) on a semiconductor substrate 100 (in gray). EX1016, [0039], [0047]. Bit lines BL (in green) are formed above impurity region 102, and impurity region 102 is disposed vertically between word lines WL and semiconductor substrate 100. EX1005, [0047], [0056].

80. A vertical structural component of Park's memory device is the active pillars PL (in pink), which penetrate the upper select lines USL, word lines WL, and lower select lines LSL to electrically connect the bit lines BL with the common

source line CSL at opposite ends. These active pillars PL correspond to strings of memory cells, where each string includes multiple memory cells connected in series between an upper select transistor UST and a lower select transistor LST. EX1016, [0050]-[0051], [0056].

81. Additionally, Park discloses charge storage layer patterns 142 (in red) between the active pillar protrusions 172 and the conductive layers USL, WL, LSL. EX1016, [0054]. charge storage layer 140 (of which charge storage layer pattern 142 is a portion) comprises a charge blocking layer, a charge trapping layer, and a charge tunneling layer, forming an ONO (oxide-nitride-oxide) structure. EX1016, [0064], [0067]. Charge storage layer pattern 142 and charge storage layer 140 have the same ONO structure because charge storage layer pattern 142 is a portion of charge storage layer 140 remained in the nonvolatile memory device after manufacturing. EX1005, [0067].

82. Park also discloses that the nonvolatile memory device includes a cell array arranged in a 3D structure and having a plurality of strings STR. EX1005, [0040]. Each string STR includes “a plurality of memory cells (MC) serially connected to each other between an upper transistor (UST) and a lower transistor (LST).” EX1005, [0040]. Active pillars PL correspond to the strings STR of the nonvolatile memory device, respectively. EX1005, [0050].

83. By structuring the memory cell array in a 3D configuration and

incorporating these design elements, Park provides a foundation for advancing the reliability of nonvolatile memory devices. EX1016, [0002].

C. Mokhlesi (EX1006)

84. Mokhlesi is directed to “three-dimensional NAND strings and other three-dimensional devices.” EX1006, [0002]. Like Park, Mokhlesi discloses 3D memory devices that include “an array of vertical NAND strings, [which] are vertically oriented, such that at least one memory cell is located over another memory cell.” EX1006, [0013]. Mokhlesi explains that “[t]he array allows vertical scaling of NAND devices to provide a higher density of memory cells per unit area of silicon or other semiconductor material.” EX1006, [0013].

85. Similar to Park, the memory array of Mokhlesi has “two or more memory cell levels,” and “the select transistors for each NAND string[] may also be monolithically integrated into each NAND string above and/or below the memory cells.” EX1006, [0013]. The nonvolatile memory devices of Mokhlesi include memory cells having an ONO structure. EX1006, [0013], [0059].

86. Specifically, Mokhlesi teaches that “source lines may be formed on top and the bit lines may be formed on the bottom. This allows formation of metal and/or silicide rather than semiconductor source lines, which leads to a decreased current crowding due to the lower resistivity source line material.” EX1006, [0092]. Mokhlesi also explains that “source lines may be replaced by a common source

region extending in both dimensions of the plane of the substrate and providing higher current sinking capability.” EX1006, [0017], [0094].

D. Fukuzumi (EX1007)

87. Fukuzumi discloses a nonvolatile semiconductor memory device designed to address challenges associated with transitioning semiconductor memory devices from 2D to 3D structures. EX1007, [0002], [0003], [0040].

88. FIG. 2 of Fukuzumi illustrates a perspective view of the nonvolatile semiconductor memory device 100 in the first embodiment. EX1007, [0078]. FIG. F below, with my annotations, including an inset to the left showing an expanded view of the memory string MS, shows FIG. 2 of Fukuzumi.

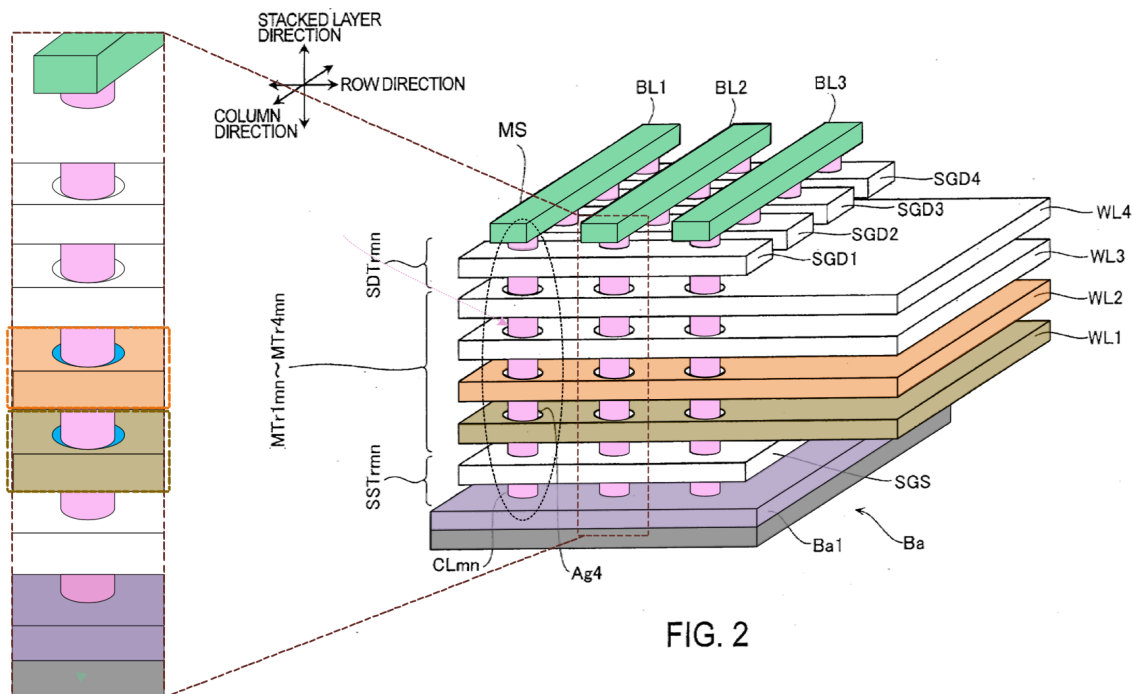


FIG. F – FIG. 2 of Fukuzumi (annotated)

89. As depicted in FIG. F above, the nonvolatile semiconductor memory device 100 of Fukuzumi includes a matrix of memory strings MS, each containing memory cells labeled $MTr1mn$ through $MTr4mn$, where the indices m and n represent the X- and Y-coordinates of the memory cells. EX1007, [0079]. Each memory string MS includes a columnar semiconductor $CLmn$ (in pink), which extends along the stacked layer direction (i.e., vertically) through source-side selection gate lines SGS, word lines WL (in brown and orange), and drain-side selection gate lines SGD. EX1007, [0079]-[0082]. Columnar semiconductors $CLmn$ connect bit lines BL (in green) at the top and a p-well region Ba1 (in purple) at the bottom of the nonvolatile semiconductor memory device 100. EX1007, [0086].

90. Memory cells $MTr1mn$ - $MTr4mn$ (e.g., enclosed in brown and orange dashed boxes) include portions of word lines WL connected to each gate of the memory cells and the charge storage layer formed on the sidewalls of word lines WL in the memory holes (in blue). EX1007, [0080], [0085], [0087].

91. Fukuzumi discloses that “[e]ach of the memory strings MS includes columnar semiconductors $CLmn$ on a p-well region Ba1 formed in an n^+ region of a semiconductor substrate Ba,” and “source means the n^+ -region formed in the p-well region Ba1 of the semiconductor substrate Ba.” EX1007, [0081], [0086]. Thus, p-well region Ba1 is a semiconductor common source of multiple memory strings MS.

92. Fukuzumi also presents a second embodiment, shown in FIG. 28, which differs from the first embodiment primarily in “a configuration of a memory layer 30b as compare[d] with the memory layer 30 in the first embodiment,” while “the same or similar reference numerals in the second embodiment are applied to the same or similar parts and elements throughout the drawings as the first embodiment.” EX1007, [0146]-[0147]. Thus, it is clear to me that although Fukuzumi describes nonvolatile semiconductor memory device 100 and its accompanying figures, including FIG. 2, in the context of the first embodiment, unless otherwise specified (e.g., with respect to memory layer 30 and word line conduction layers 36), the disclosures regarding nonvolatile semiconductor memory device 100 are equally applicable to the second embodiment as well.

93. Both embodiments of Fukuzumi’s nonvolatile semiconductor memory devices provide “an effect of higher integration and lower cost on the nonvolatile semiconductor memory device.” EX1007, [0144], [0150].

IX. Grounds 1 and 2: Lung Anticipates or Otherwise Renders Obvious Claims 8 and 21

A. Independent Claim 8

94. Claim 8 is reproduced below. For ease of discussion, I have included a label for each claim element.

[8.P] An apparatus comprising:

[8.a] a plurality of first memory cells located in a first device level of a memory device;

[8.b] a plurality of second memory cells located in a second device level of the memory device;

[8.c] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;

[8.d.1] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate,

[8.d.2] wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction;

[8.e] a common source; and

[8.f.1] data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions,

[8.f.2] wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

[8.P] An apparatus comprising

95. As shown in FIG. 18 of Lung (FIG. H of my Declaration) reproduced below, Lung discloses an integrated circuit 1875 including 3D NAND flash memory array cubes with a source plane 1860. EX1004, [0108]. The integrated circuit 1875 qualifies as the claimed “apparatus.” Thus, Lung discloses element [8.P].

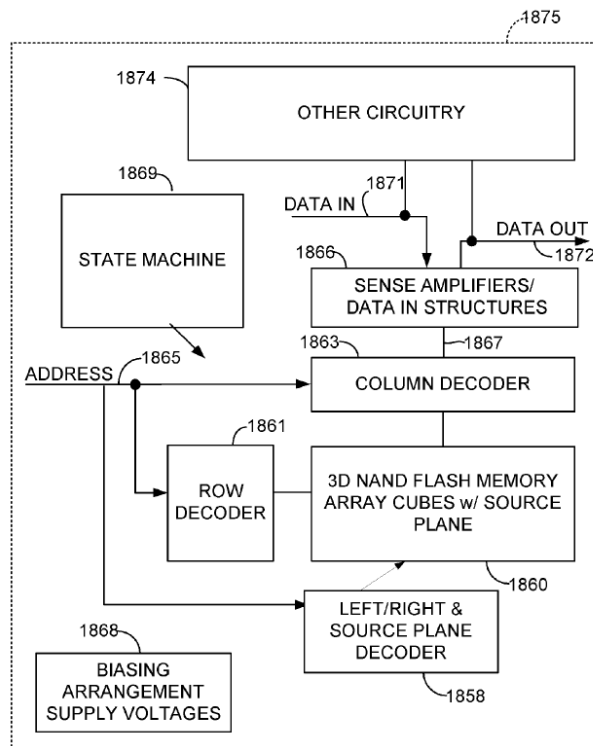


Fig. 18

FIG. H – FIG. 18 of Lung

[8.a] a plurality of first memory cells located in a first device level of a memory device&
[8.b] a plurality of second memory cells located in a second device level of the memory device

96. As illustrated in FIGs. 4 and 5 of Lung (FIG. I of my Declaration with annotations, below), Lung discloses that integrated circuit 1875 includes a first group of memory cells (enclosed in the brown dashed box in FIG. 4), including memory cell 500-R (enclosed by the brown dashed box in FIG. 5), which corresponds to the claimed “a plurality of first memory cells” that are located in a “bottom level” of 3D memory device 100, satisfying “being in “a first device level of a memory device.” Additionally, Lung discloses a second group of memory cells (enclosed in the orange dashed box in FIG. 4), including memory cell 502-R (enclosed in the orange dashed box in FIG. 5), which corresponds to the claimed “a plurality of second memory cells” that are located in a “next lower level” of 3D memory device 100, thereby satisfying being in “a second device level of the memory device.” EX1004, [0054], [0058]-[0060].

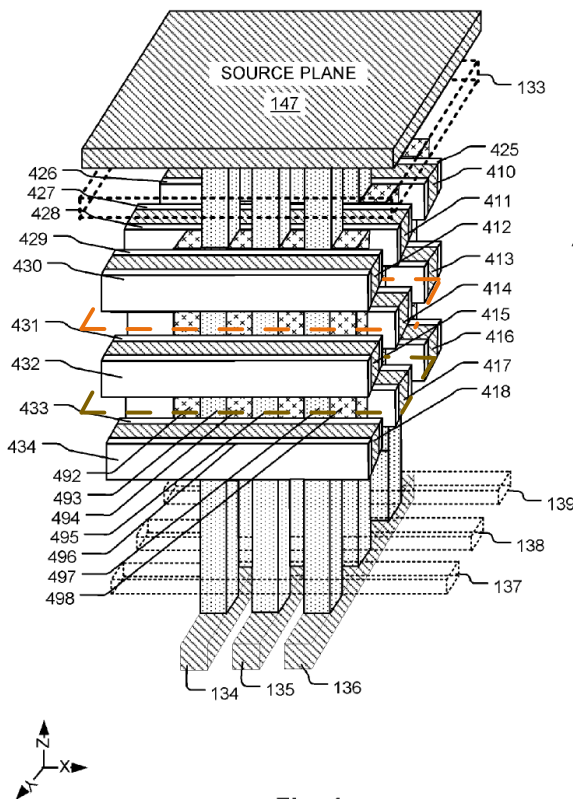


Fig. 4

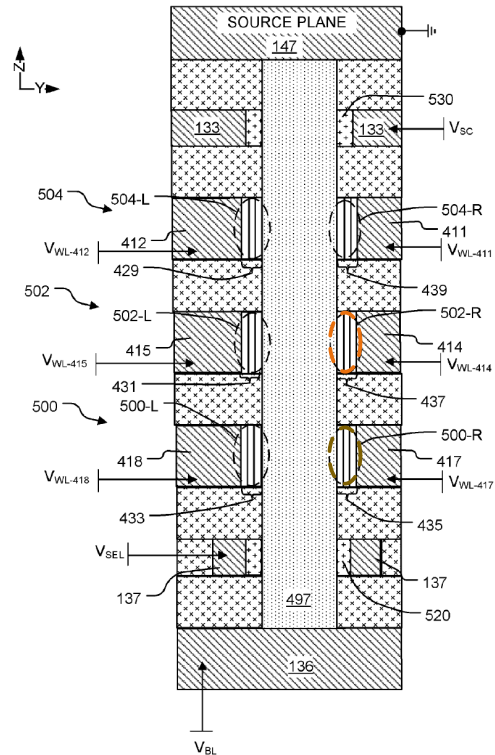


Fig. 5

FIG. I – FIGs. 4 and 5 of Lung (annotated)

97. Based on the above disclosure, I conclude that Lung explicitly discloses elements [8.a] and [8.b].

[8.c] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate

[8.d.1] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate

[8.d.2] wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction

98. Lung discloses that “a next lower level includes word lines 413, 414

and 415, and a bottom level includes word lines 416, 417 and 418.” EX1004, [0054]. Lung also discloses “each cell including a charge trapping element and a gate,” for example, “right cell 500-[R] includes word line 417 as the gate” and “right cell 502-[R] includes word line 414 as the gate.” EX1004, [0051], [0059]-[0060].

99. As illustrated in FIGs. 4 and 5 (FIG. J of my Declaration with annotations, below), 3D memory device 100 includes a first word line 417 (in brown) formed in the same bottom level as the first group of memory cells (enclosed in the brown dashed box), including 500-R, thereby satisfying the “first control gate formed in the first device level, the first control gate to control access to the first memory cells” in element [8.c].

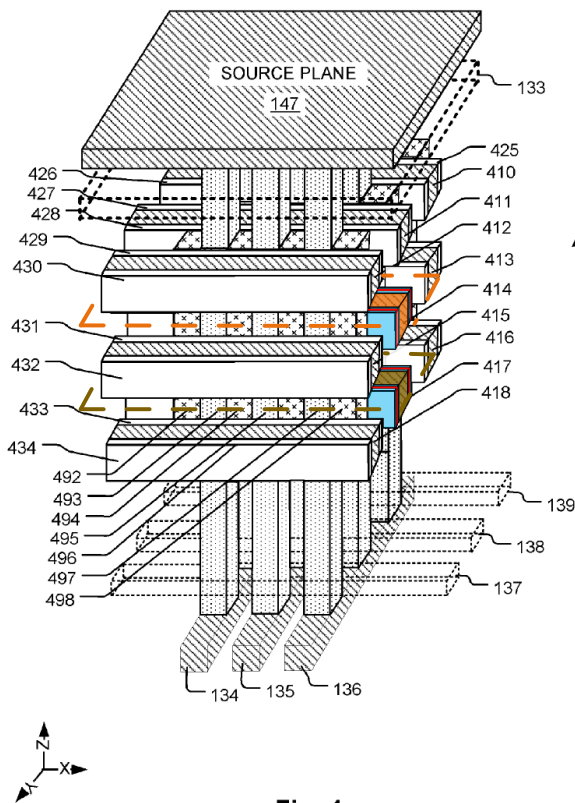


Fig. 4

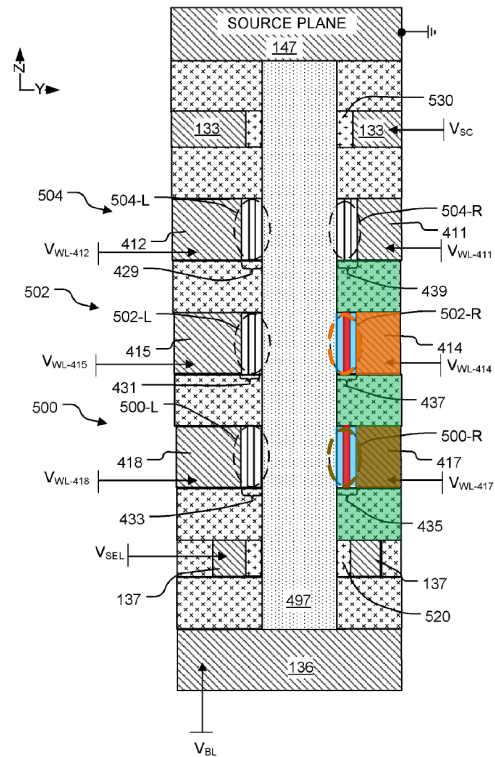


Fig. 5

FIG. J – FIGs. 4 and 5 of Lung (annotated)

100. Likewise, 3D memory device 100 includes a second word line 414 (in orange) formed in the same next lower level as the second group of memory cells (in the orange dashed box), including 502-R, thereby satisfying the “second control gate formed in the second device level, the second control gate to control access to the second memory cells” in element [8.d.1].

101. Lung further discloses applying bias voltages to word lines 410-418, including first and second word lines 417 and 414, when operating the first and second groups of memory cells, including first and second memory cells 500-R and 502-R. EX1004, [0064]-[0067]. A POSITA would have understood that first word

line 417 controls access to the first group of memory cells, including 500-R, thereby satisfying “the first control gate to control access to the first memory cells” in element [8.c]. Similarly, a POSITA would have understood that that second word line 414 controls access to the second group of memory cells, including 502-R, thereby satisfying “the second control gate to control access to the second memory cells” in element [8.d.1].

102. Lung also discloses “each cell including a charge trapping element and a gate,” for example, “right cell 500-[R] includes ... charge storage structure 435 as the charge storage element” and “right cell 502-[R] includes ... charge storage structure 437 as the charge storage element.” EX1004, [0051], [0059]-[0060]. Specifically, Lung discloses that the charge storage structure includes a silicon nitride layer as a charge trapping layer. EX1004, [0052]. Therefore, a POSITA would have understood that the silicon nitride charge trapping layer in charge storage structures 435 and 437 constitutes the claimed “memory element” in elements [8.c] and [8.d.1].

103. Since Lung further discloses that “memory cells [are] formed at the cross points of the semiconductor pillars 493, 495, 497 and the charge storage structures 425-430 on the opposing sides of the word lines (e.g., 410-412),” a POSITA would have understood that each word line has openings where the corresponding charge storage structures are formed. EX1004, [0057]. That is, each

charge storage structure creates an opening in the corresponding word line that controls access to the respective memory cell.

104. This is further illustrated in annotated FIG. J (which I repeat below), where charge trapping layers (in red) in the charge storage structures, including 435 and 437, of the first and second groups of memory cells, including 500-R and 502-R, are formed in the openings (in blue) of first and second word lines 417 and 414 (in brown and orange), respectively.

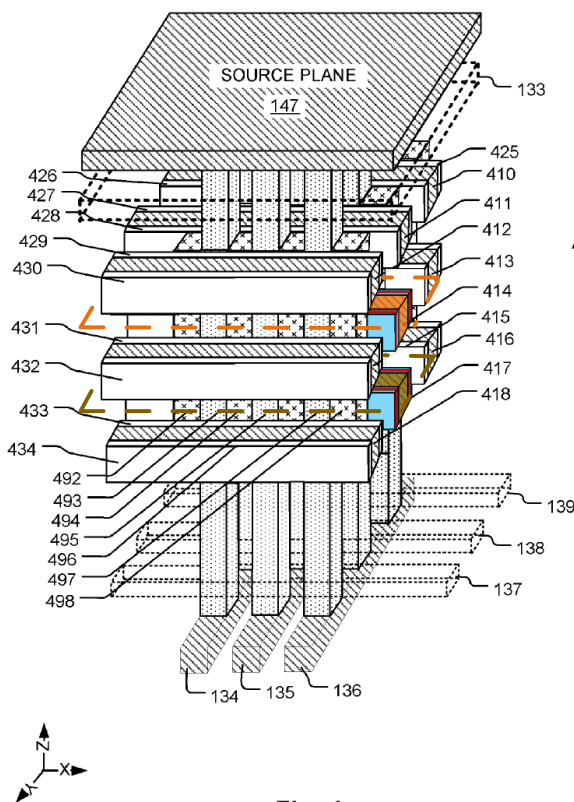


Fig. 4

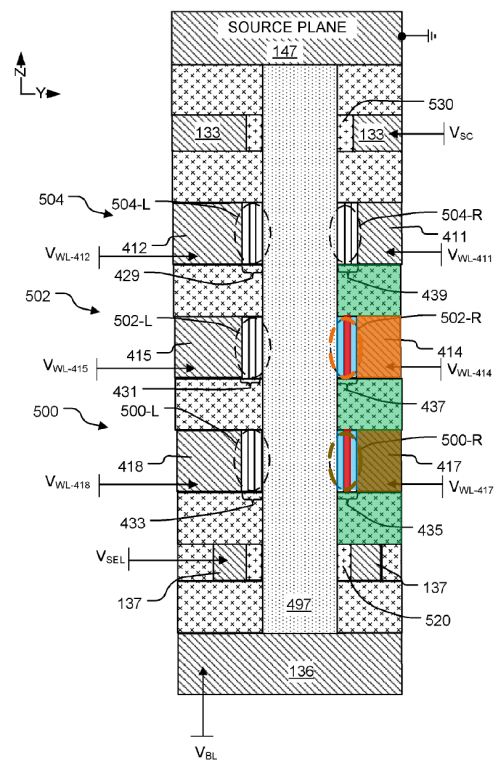


Fig. 5

FIG. J – FIGs. 4 and 5 of Lung (annotated)

105. As shown in annotated FIG. 5 above, each opening (in blue) forms a recess within first or second word line 417 or 414 (in brown or orange) in a control gate layer, relative to the insulation material layers (in green) above and below the control gate layer. EX1004, [0062]. Therefore, the above disclosure of Lung meets the claim requirement that “each of the first memory cells includes a memory element formed in a cavity of the first control gate” in element [8.c], and “each of the second memory cells includes a memory element formed in a cavity of the second control gate” in element [8.d.1].

106. As further illustrated in annotated FIG. 4 above, each of the first and second groups of memory cells (enclosed in the brown and orange dashed boxes) includes a plurality of memory cells along the X-direction, corresponding to the claimed “first direction,” as well as two memory cells along the Y-direction, corresponding to the claimed “second direction.” EX1004, [0057].

107. A POSITA would have understood, as shown in annotated FIG. 5 above, that the two memory cells of the first memory group in the Y-direction include, for example, 500-R (enclosed in the brown dashed box) and another memory cell (not shown) on the opposite end of first word line 417 (in brown) in the Y-direction. Similarly, the two memory cells of the second memory group in the Y-direction include, for example, 502-R (enclosed in the orange dashed box) and another memory cell (not shown) on the opposite end of second word line 414 (in orange)

in the Y-direction. Therefore, Lung explicitly discloses that “the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction” in element [8.d.2].

108. Based on the above analysis, it is my opinion that Lung discloses or at least suggests elements [8.c], [8.d.1], and [8.d.2].

[8.e] a common source

109. As illustrated in FIG. 4 below (FIG. K of my Declaration with annotations), Lung discloses a source plane 147 (in purple). EX1004, [0027], [0034], [0054], [0057]. Specifically, Lung describes that source plane 147 is coupled to an array of semiconductor pillars, e.g., 493, 495, and 497 (in pink), which correspond to an array of NAND memory strings. EX1004, [0045]-[0046], [0056]-[0057].

110. Therefore, a POSITA would have understood that source plane 147 in FIG. 4 is “common” to multiple NAND strings of memory cells, for example, for sourcing current, thereby constituting the claimed “common source.”

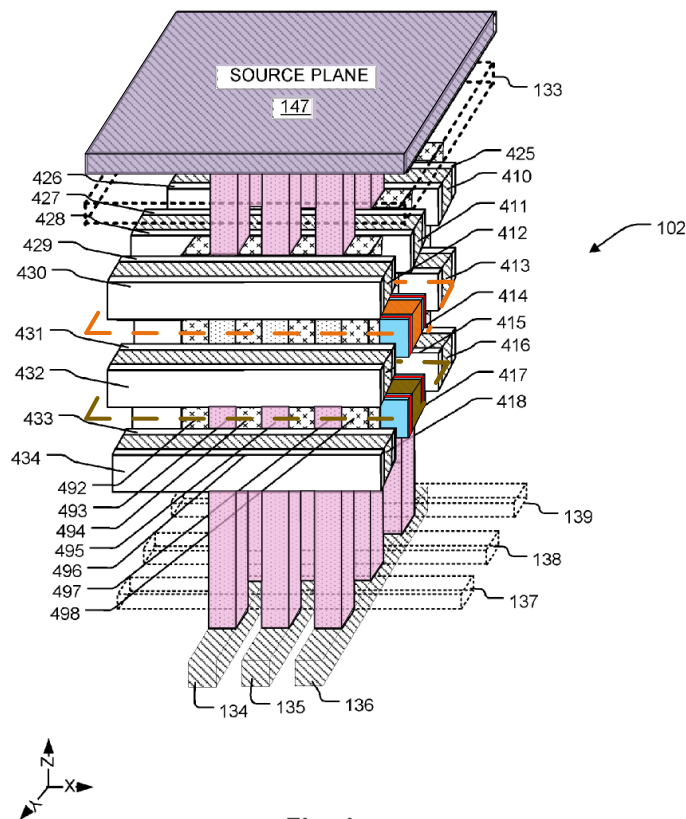


Fig. 4

FIG. K – FIG. 4 of Lung (annotated)

[8.f.1] data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions

[8.f.2] wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate

111. As illustrated in FIGs. 4 and 5 of Lung below (FIG. L of my Declaration with annotations), Lung further discloses bit lines 134-136 (in green) electrically connected to common source plane 147 (in purple) and the first and second groups of memory cells in the bottom and next lower levels (enclosed in brown and orange

dashed boxes) through semiconductor pillars 493, 495, and 497 (in pink). EX1004, [0039], [0045], [0055]-[0057].

112. It is clear to me that bit lines 134-136 qualify as the claimed “data lines” at least because the ’214 patent describes that “[d]ata lines 251, 252, and 253 sometimes correspond to bit lines or sense lines of a non-volatile memory device.” EX1001, 3:29-31.

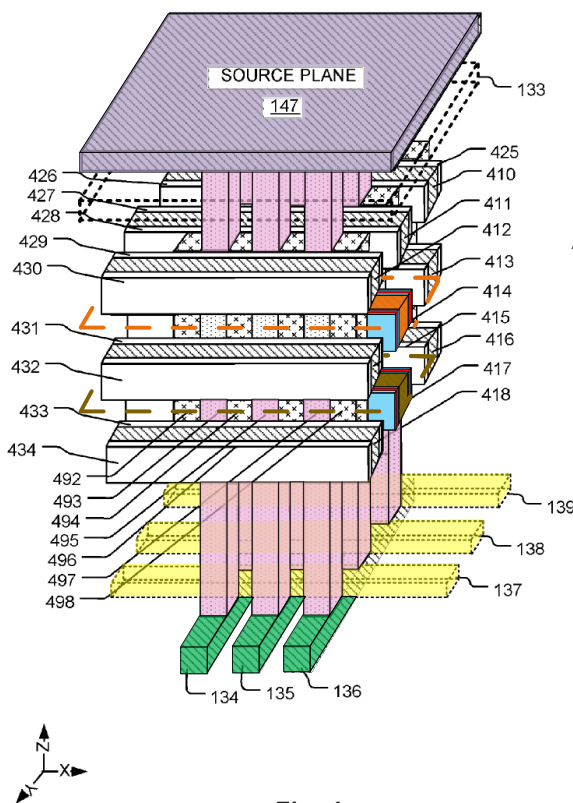


Fig. 4

FIG. L – FIGs. 4 and 5 of Lung (annotated)

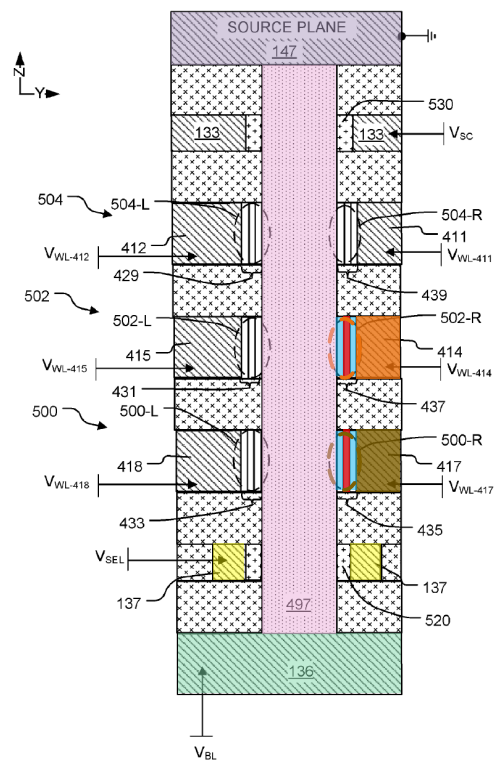


Fig. 5

113. Lung discloses a bottom set of pillar select transistors 106 (shown in FIG. 1) coupled to bit lines 134-136 (in green in FIG. L above) and select lines 137-139 (in yellow in FIG. L above) that “selectively couple a Z-direction column of

the two-cell unit structures 120-128 to a corresponding bit line in a plurality of bit lines 134, 135, 136 extending in the Y-direction,” such that “bit lines 134, 135, 136 are coupled to a column decoder.” EX1004, [0010], [0031]-[0032], [0054]. A POSITA would have understood that the electrical connection between bit lines 134-136 and semiconductor pillars 493, 495, and 497 is controlled by the bottom set of pillar select transistors 106, and that the column decoder selects/deselects each NAND string of memory cells along a respective semiconductor pillar 493, 495, or 497 by turning the bottom set of pillar select transistors 106 on or off to control the connections between bit lines 134-136 and semiconductor pillars 493, 495, and 497, through select lines 137-139.

114. Thus, Lung discloses that bit lines 134-136 are configured to be “selectively” coupled to common source plane 147 and the first and second groups of memory cells through semiconductor pillars 493, 495, and 497. That is, Lung discloses the claimed feature of “data lines configured to be selectively coupled to the common source and the first and second memory cells” in element [8.f.1].

115. Lung discloses that semiconductor pillars 493, 495, and 497 are formed of “doped semiconductor material,” such as “p-type polysilicon.” EX1004, [0073], claim 12. Likewise, the '214 patent also describes that “a **conductive material** 2001 has been formed by, for example, depositing **undoped or lightly doped polysilicon** to place channels 1841 **in electrical communication** with pillars 705.” EX1001,

8:64-67. Therefore, it is clear to me that Lung's semiconductor pillars 493, 495, and 497 having p-type polysilicon material include the claimed "conductive material," which also encompasses "undoped or lightly doped polysilicon in electrical communication with pillars 705." EX1001, 8:64-67.

116. Moreover, since Lung discloses semiconductor pillar 497 is in a Z-direction column, and the memory cells are formed along semiconductor pillars (e.g., 493, 495, and 497), Lung likewise discloses "conductive material" of the semiconductor pillars extending through the first and second groups of memory cells in the Z-direction perpendicular to the X- and Y-directions. EX1004, [0057]-[0058], FIGs. 4-5. Therefore, Lung explicitly discloses that "the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions" in element [8.f.1].

117. Regarding the claimed relative vertical position features of the "common source," "substrate," and "memory cells" in element [8.f.2], FIGs. 4 and 5 of Lung clearly show that common source plane 147 is formed over the stack of memory cells, which are in turn formed over the substrate (not shown). Specifically, Lung explicitly discloses that "FIG. 4 shows a memory device that comprises a plurality of bit lines 134, 135, 136 over a substrate," "memory cells ... lie[] over the plurality of bit lines," and "source plane 147 is over the plurality of memory

cells.” EX1004, [0008], [0057], FIGs. 4-5.

118. Therefore, it is my opinion that Lung discloses or at least renders obvious elements [8.f.1] and [8.f.2].

119. From the foregoing, I conclude that Lung anticipates or otherwise renders obvious claim 8.

B. Independent Claim 21

120. Claim 21 is reproduced below. For ease of discussion, I have included a label for each claim element.

[21.P] An apparatus comprising:

[21.a] a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

[21.b] a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

[21.c] a first dielectric formed on the first sidewall and the second sidewall;

[21.d] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

[21.e] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

[21.f] a second dielectric formed on a side of the first memory element and on a side of the second memory element;

[21.g] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric;

[21.h] a substrate; and

[21.i] a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

[21.P] An apparatus comprising

121. As I discussed in Section IX.A([8.P]), Lung discloses “[a]n apparatus.”

[21.a] a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall

[21.b] a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall

122. As I discussed in Section IX.A([8.c], [8.d.1], [8.d.2]), Lung discloses or otherwise renders obvious “a first/second control gate formed in the first/second device level, ..., wherein each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.”

123. Lung further discloses forming “layers 722, 724, 726, and 728 of word

line materials, such as n⁺-polysilicon,” as part of the process of manufacturing 3D memory device 100. EX1004, [0069]. Thus, a POSITA would have understood that word lines 410-418 are patterned from layers 722, 724, 726, and 728, such that first and second word lines 417 and 414, which correspond to the claimed “first/second control gate,” are made of word line materials, such as n-type polysilicon, i.e., conductive materials. EX1004, [0070].

124. Regarding the claim feature about “first/second conductive material located in a first/second device level, ... including a first/second cavity” recited in elements [21.a] and [21.b], I have noticed that the specification of the ’214 patent describes that “[m]aterials 1002, 1004, and 1006 can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon),” and “[f]orming cavities 1120 in materials 1002, 1004, and 1006 also form control gates 1221, 1222, and 1223, which can correspond to control gates 221, 222, and 223 of FIG. 2.” EX1001, 7:3-5, 39-42.

125. Thus, a POSITA would have understood that, as shown in FIGs. 4 and 5 of Lung (FIG. M of my Declaration with annotations), first word line 417 (in brown) made of n-type polysilicon is “a first conductive material,” consistent with the ’214 patent. EX1001, 7:3-5, 39-42. Similarly, second word line 414 (in orange) made of n-type polysilicon is “a second conductive material.” Accordingly, Lung discloses “a first conductive material located in a first device

level of a memory device” in element [21.a] and “a second conductive material located in a second device level of the memory device” in element [21.b].

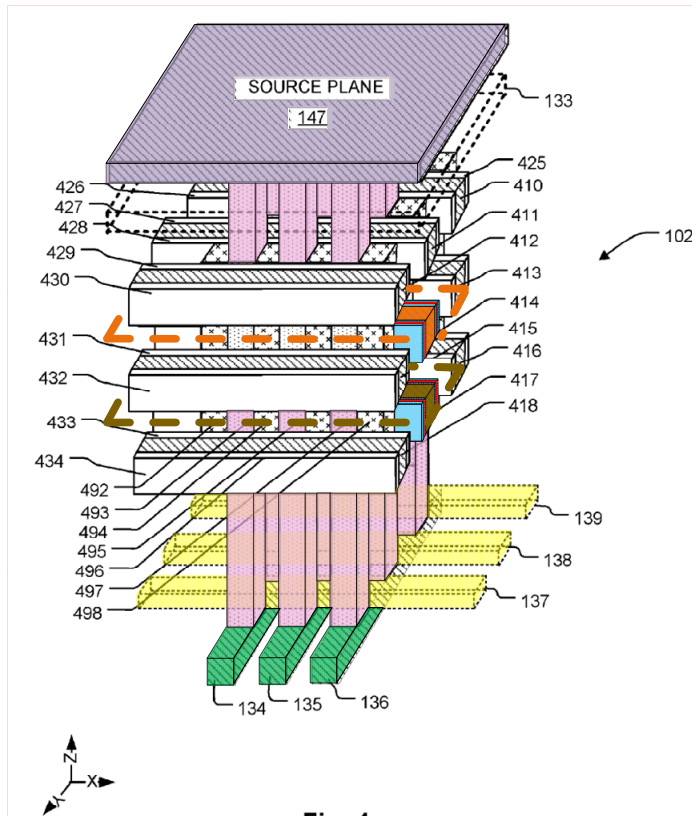


Fig. 4

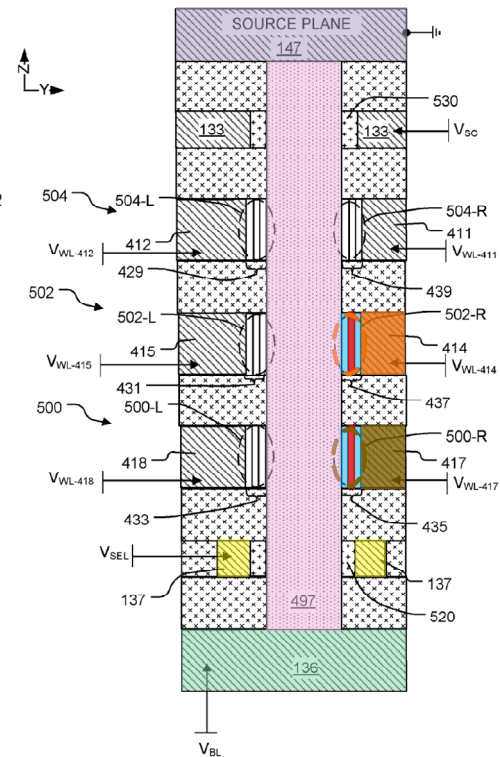


Fig. 5

FIG. M – FIGs. 4 and 5 of Lung (annotated)

126. Lung further discloses “trenches having sidewalls 830-833 on which the layers of word line materials are exposed at each level of the structure,” and “charge trapping structures (940-943) over and on the sidewalls of the trenches (845-848) contacting the layers of word line material.” EX1004, [0070]-[0071].

127. As further shown in FIG. M above, a POSITA would also have understood, or at least found it obvious, that the opening (in blue) in first word line 417 (in brown) has a respective sidewall (e.g., 830-833) on which charge storage

structures, e.g., 435, are formed, thus constitutes the claimed “first cavity having a first sidewall” in element [21.a]. Likewise, the opening (in blue) in second word line 414 (in orange) has a respective sidewall (e.g., 830-833) on which charge storage structures, e.g., 437, are formed, thus constitutes the claimed “second cavity having a first sidewall” in element [21.b].

128. Accordingly, it is my opinion that Lung discloses or otherwise renders obvious elements [21.a] and [21.b].

[21.c] a first dielectric formed on the first sidewall and the second sidewall

[21.d] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric

[21.e] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric

[21.f] a second dielectric formed on a side of the first memory element and on a side of the second memory element

129. As I discussed in Section X.A([8.c]) above, Lung discloses that “each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.”

130. Lung further discloses that the charge storage structure includes an “ONO” structure, having “a tunneling layer in contact with the word line material, the charge trapping layer over the tunneling layer, and a blocking layer over the charge trapping layer, such as used in typical charge trapping memory

devices.” EX1004, [0052].

131. Thus, as shown in FIG. 5 of Lung (FIG. N of my Declaration with annotations, below), a POSITA would have understood that 3D memory device 100 further includes a tunneling layer (in green and located to the right side of the dashed blue boxes in FIG. N below) of charge storage structures, e.g., 435 and 437, corresponding to the claimed “first dielectric,” which is formed on the sidewalls of the openings (enclosed in blue dashed box) in first and second word lines 417 and 414 (in brown and orange), thus satisfying “formed on the first sidewall and the second sidewall,” as claimed in element [21.c].

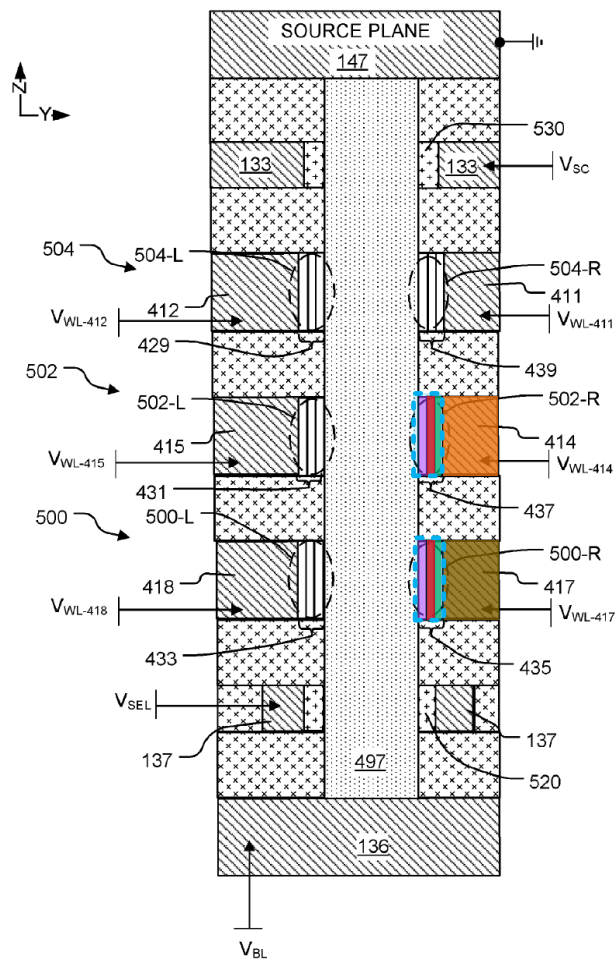


Fig. 5

FIG. N – FIG. 5 of Lung (annotated)

132. A POSITA would further have understood that 3D memory device 100 further includes a blocking layer (in purple, and located to the left side of the dashed blue boxes in FIG. N above) of charge storage structures, e.g., 435 and 437, corresponding to the claimed “second dielectric,” which is formed on the sides of the corresponding charge trapping layers (in red), thus satisfying “formed on a side of the first memory element and on a side of the second memory element,” as recited

in element [21.f].

133. Lung specifically discloses that the tunneling layer may be “a layer of silicon dioxide or silicon oxide nitride” and “in contact with the word line material,” and that the charge trapping layer is “over the tunneling layer.” EX1004, [0052].

134. As shown in FIG. N above (annotated FIG. 5 of Lung), a POSITA would have understood that the charge trapping layer (in red and located in the center of the dashed blue boxes in FIG. N above), corresponding to the claimed “first/second memory element,” is electrically isolated from the respective first or second word line 417 or 414 (in brown or orange) corresponding to the claimed “first/second conductive material,” by a respective portion of the tunneling layer (in green and located to the right side of the dashed blue boxes in FIG. N above), corresponding to the claimed “first dielectric.” That is, Lung discloses or at least renders obvious the claimed “first memory element ... electrically isolated from the first conductive material by a first portion of the first dielectric” in [21.d], and “second memory element ... electrically isolated from the second conductive material by a second portion of the first dielectric” in element [21.e].

135. Based on my above analysis, it is my opinion that Lung discloses elements [21.c]-[21.f].

[21.g] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric

136. Lung discloses that “memory cells [are] formed at the cross points of the semiconductor pillars 493, 495, 497 and the charge storage structures 425-430... at least one memory cell of the plurality of memory cells is over another one memory cell of the plurality of memory cells, such as by being on the same semiconductor pillar as a lower cell.” EX1004, [0057].

137. Lung also discloses that in a read operation, “a current path is established between the bit line 134 and the source plane 147 via the particular NAND string to which the selected memory cell belongs.” EX1004, [0045].

138. Thus, a POSITA would have understood that during certain operations of Lung’s memory device, a channel of a NAND string of memory cells forms in the vertical outermost layer of the semiconductor pillar (e.g., 493, 495, or 497) and does not extend throughout the entire semiconductor pillar. Thus, Lung discloses the claimed “conductive channel.”

139. This understanding is well established in the art. For example, Sim discloses that “[a]pplication of the read voltage VREAD to the lower select line LSL causes vertical inversion regions 504B to be formed **along the outer walls** of lower portions of the vertical pillars PL formed of semiconducting material,” and “it can

where the first and second groups of memory cells are located, respectively.

EX1004, [0057]-[0058], FIGs. 4-5. Thus, Lung discloses the claimed “conductive channel extending from the first device level to the second device level,” as recited in element [21.g].

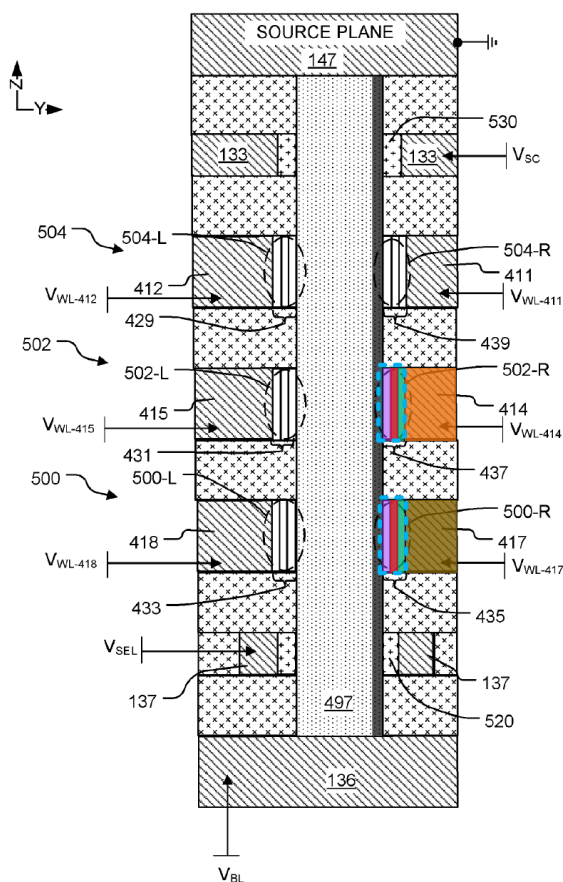


Fig. 5

FIG. P – FIG. 5 of Lung (annotated)

141. As discussed in Section IX.B above and shown in FIG. 5 (FIG. P of my Declaration with annotations) above, Lung further discloses that the “blocking layer [is] between the dielectric charge trapping layer and the given semiconductor pillar,”

and that “the blocking layer may comprise a layer of silicon dioxide or a high-k material typical in SONOS-type memory devices.” EX1004, [0052], claim 5. Thus, a POSITA would have understood that the vertical outermost layer of semiconductive pillar 497 (in black), corresponding to the claimed “conductive channel,” faces the charge trapping layers (in red), corresponding to the claimed “first and second memory elements,” and is electrically isolated from the charge trapping layers by a respective portion of the blocking layer (in purple), corresponding to the claimed “a first/second portion of the second dielectric.”

142. Accordingly, it is my opinion that Lung discloses the subject matter of element [21.g].

***[21.h] a substrate
[21.i] a data line configured to be selectively coupled to the
conductive channel, wherein the data line is located between
the second conductive material and the substrate***

143. As shown in FIG. 5 below (FIG. Q of my Declaration with annotations), a POSITA would have understood, or at least found it obvious, Lung discloses that bit line 136 (in green) is coupled to semiconductor pillar 497, including its vertical outermost layer (in black), thereby satisfying “a data line configured to be ... coupled to the conductive channel” in element [21.i]. EX1004, [0055], FIGs. 4-5.

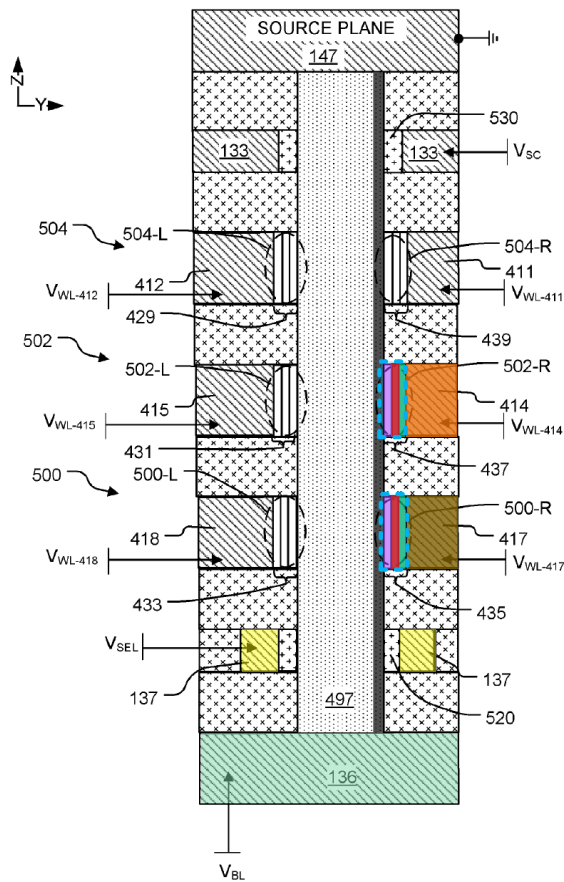


Fig. 5

FIG. Q – FIG. 5 of Lung (annotated)

144. Lung further discloses a bottom set of pillar select transistors 106 (shown in FIG. 1) coupled to select line 137 (in yellow), which “selectively couple a Z-direction column of the two-cell unit structures 120-128 to a corresponding bit line in a plurality of bit lines 134, 135, 136 extending in the Y-direction,” such that “bit lines 134, 135, 136 are coupled to a column decoder.” EX1004, [0010], [0031]-[0032], [0054].

145. Thus, a POSITA would have understood that the electrical connection

between bit line 136 and semiconductor pillar 497 is controlled by the bottom set of pillar select transistors 106 through select line 137. Therefore, Lung discloses that bit line 136 is configured to be “selectively” coupled to the vertical outermost layer of semiconductor pillar 497, thus satisfying “a data line configured to be selectively coupled to the conductive channel,” as recited in element [21.i].

146. Regarding the claimed “substrate” in element [21.h] and the claimed location of “data line” element in [21.i], Lung further discloses a “memory device that comprises a plurality of bit lines 134, 135, 136 over a substrate,” and that “[a] plurality of memory cells ... lies over the plurality of bit line.” EX1004, [0057]. As shown in FIG. Q (annotated FIG. 5 of Lung) above, second word line 414 (in orange) is formed over bit line 136, such that bit line 136 (in green) is located vertically between second word line 414 and the substrate (not shown) underneath bit line 136, thus satisfying the claimed relative location feature that “the data line is located between the second conductive material and the substrate” in element [21.i].

147. Accordingly, Lung discloses elements [21.h] and [21.i].

X. Ground 3: Park In View of Mokhlesi Renders Obvious Claims 8, 13 and 21

A. Reasons to Combine Park and Mokhlesi

148. In my opinion, a POSITA would have found it obvious to modify Park’s 3D memory device and fabrication method thereof in view of Mokhlesi’s teaching

of forming a common source at the top and bit lines at the bottom of a 3D memory device. I will discuss various reasons in detail below.

1. Teaching, suggestion, or motivation in the prior art

149. As I discussed in Section VIII.B, Park's objectives include improving the reliability of 3D NAND memory devices. EX1005, [0002]. Park discloses using impurity region 102 as a common source, which is formed of a semiconductor material. EX1005, [0040], [0047].

150. However, the use of semiconductor material for common sources introduces significant electrical performance limitations, with current crowding being a particularly critical concern. Current crowding occurs when the flow of electrical current is not evenly distributed, leading to localized areas of high current density. This uneven distribution can result in serious reliability issues, including localized overheating and thermal hotspots, which degrade device performance and longevity. Furthermore, increased electromigration effects—where high current density causes the gradual movement of metal atoms—can lead to the formation of voids and eventual circuit failure. EX1014, 1344; EX1015, 239, 242; EX1016, 1, 4.

151. These challenges are further exacerbated in a 3D memory architecture, where the common source and bit lines are vertically stacked. The confined geometry of 3D NAND and similar memory structures limits heat dissipation and increases current density, making current crowding effects even more severe.

152. As I discussed in Section VIII.C, Mokhlesi directly addresses this problem by teaching that source lines should be placed at the top of a 3D NAND memory device and made of metal or silicide rather than semiconductor material. Mokhlesi explains that this approach “allow[s] formation of metal and/or silicide rather than semiconductor source lines, which leads to a decreased current crowding due to the lower resistivity source line material.” EX1006, [0092].

153. Given that Park’s common source is also made of semiconductor material, it suffers from the exact same current crowding problem identified by Mokhlesi. Thus, a POSITA would have naturally been motivated to adopt Mokhlesi’s solution—“source lines may be formed on top and the bit lines may be formed on the bottom” and “formation of metal and/or silicide rather than semiconductor source lines”—to address the same current crowding issue in Park’s 3D memory device. Adopting this solution in Park’s structure would, therefore, be an obvious design choice for enhancing the electrical performance and durability of the memory device. As Mokhlesi explains, “formation of metal and/or silicide rather than semiconductor source lines... leads to decreased current crowding due to the lower resistivity source line material.” EX1006, [0092].

154. By replacing Park’s semiconductor common source with a metal and/or silicide common source at the top of the 3D memory device, the modification would significantly enhance current distribution and minimize localized heating and

electromigration effects. This improvement would be particularly beneficial in high-density 3D NAND architectures, where current crowding effects are more pronounced due to vertical stacking. Ultimately, this modification would directly advance Park's goal of improving device reliability and ensuring stable long-term operation.

155. Furthermore, Mokhlesi's teaching regarding source lines is directly applicable to a common source region. Mokhlesi explicitly states that "[i]n another alternative embodiment, the source lines 239 are be replaced by a common source region (source plane) extending in both dimensions of the plane of the substrate 1 (in the x-y plane)." EX1006, [0094].

156. Additionally or alternatively, a POSITA would have found it obvious to apply Mokhlesi's teaching regarding source lines to Park's common source (impurity region 102). Mokhlesi explicitly states that a "common source plate provides a higher current sinking capability at the expense of losing the ability to select individual source line voltage." EX1006, [0017], [0094]. This suggests that replacing individual source lines with a common source plate can enhance current distribution efficiency, thereby mitigating current crowding and related reliability issues. This principle directly aligns with Park's 3D memory architecture, where individual source line selection is unnecessary since all memory string sources are commonly connected to impurity region 102. EX1005, [0039]-[0040], [0047], FIG.

2.

157. Therefore, given Mokhlesi's well-documented benefits of such a structure in mitigating reliability concerns, a POSITA would have been naturally motivated to apply Mokhlesi's teachings to optimize Park's common source configuration.

2. Applying known techniques to a known device ready for improvement

158. Furthermore, the industry-wide recognition of the benefits of using metal or silicide for common sources reinforces the obviousness of applying Mokhlesi's teachings to Park's 3D memory device. It was well understood that high resistivity in semiconductor materials leads to increased voltage drops and power losses, negatively impacting device efficiency and reliability. By contrast, metals and silicides offer superior conductivity, reducing resistive losses and enabling more efficient current distribution, particularly in high-density memory architectures like 3D NAND. EX1009, 11.

159. Additionally, memory manufacturers had already begun implementing alternative source placement strategies to address these resistivity challenges. Prior industry literature proposed positioning the common source at the top of the memory stack, as opposed to the bottom, specifically to facilitate the use of low-resistivity materials such as metals or silicides. EX1012, 136-137; EX1013, 22-23.

These established solutions demonstrated that transitioning from a semiconductor common source to a metal or silicide common source was a predictable design choice that offered clear advantages in minimizing resistance, reducing power consumption, and enhancing overall device performance.

160. Given this industry knowledge, a POSITA would have recognized the clear benefits of adopting Mokhlesi's approach in Park's device. The combination would yield a more reliable and efficient 3D NAND structure while maintaining compatibility with existing fabrication techniques, making it an obvious and advantageous modification.

161. A POSITA would have understood that implementing Mokhlesi's modification in Park's structure would lead to a predictable reduction in current crowding, thereby enhancing the reliability and efficiency of the 3D memory device.

3. Reasonable expectation of success

162. A POSITA would have had a reasonable expectation of success in modifying Park's 3D memory device by incorporating Mokhlesi's metal/silicide common source at the top. Both Park and Mokhlesi describe 3D NAND memory devices with similar structural features, including vertically stacked memory cells, NAND memory strings, charge storage elements utilizing an "ONO" structure, and selection transistors positioned above and/or below the memory cells. See Sections VIII.B, VIII.C.

163. Mokhlesi explicitly describes repositioning the common source to the top of the 3D memory structure. EX1006, [0094]. This reconfiguration does not alter the fundamental function of the common source; rather, it enhances its efficiency by reducing resistance. The well-documented electrical benefits of metal and silicide materials further support a POSITA's expectation of success in making this modification.

164. Moreover, fabricating a metal/silicide common source at the top of Park's memory device would have been well within a POSITA's skillset. The semiconductor industry has already developed standard manufacturing techniques for depositing and patterning metal and silicide layers. A POSITA would have recognized that these techniques could be seamlessly integrated into Park's process without introducing undue complexity. The proposed modification does not introduce any unpredictable results or undue complexities in the fabrication process. Instead, it aligns with well-established design improvements in the field and follows the logical progression of memory device optimization.

165. For example, as illustrated in the modified and annotated FIG. 3 of Park (FIG. R of my Declaration below), the proposed configuration involves forming modified bit lines BL' (in green) over the semiconductor substrate 100 (in gray), placing drain-side selection transistors and lines (in yellow) above the bit lines BL', positioning word lines (in orange) and charge storage layer patterns 142 (in red)

above the drain-side selection transistors and lines, situating source-side selection transistors and lines (in blue) over the word lines, and finally forming a metal/silicide common source 102' (in purple) at the top.

Fig. 3

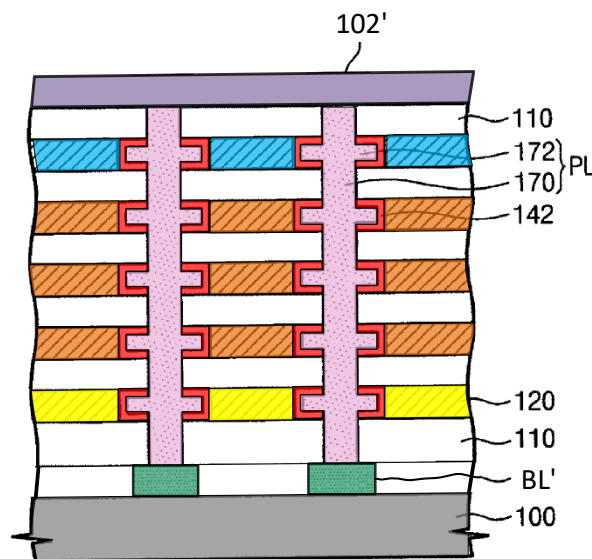


FIG. R – FIG. 3 of Park (annotated and modified)

166. This reconfiguration is straightforward to a POSITA and would neither impair the functionality of Park's 3D memory device nor introduce any manufacturing hurdles. Instead, it improves performance by reducing resistivity and minimizing current crowding. Accordingly, a POSITA would have had a reasonable expectation of success in implementing this modification.

167. Particularly, a POSITA would have understood that the rearrangement of bit lines BL and common source in Park's 3D memory device in view of

Mokhlesi would not affect Park's disclosures of other features related to the challenged claims of the '214 patent, such as memory cells MC, word lines WL, active pillars PL, etc., which would remain unchanged in the modified structure (e.g., the example shown in FIG. R above).

B. Independent Claim 8

[8.P] An apparatus comprising

168. As shown in FIG. 25 of Park (FIG. S of my Declaration) reproduced below, Park discloses a memory system 1100 including a memory 1130. EX1005, [0106], [0108]. The memory system 1100 qualifies as the claimed "apparatus." It is noted that, unless otherwise specified, Park's disclosures are applicable to the combination of Park and Mokhlesi in my Declaration used for mapping in Ground 3. Thus, Park discloses element [8.P].

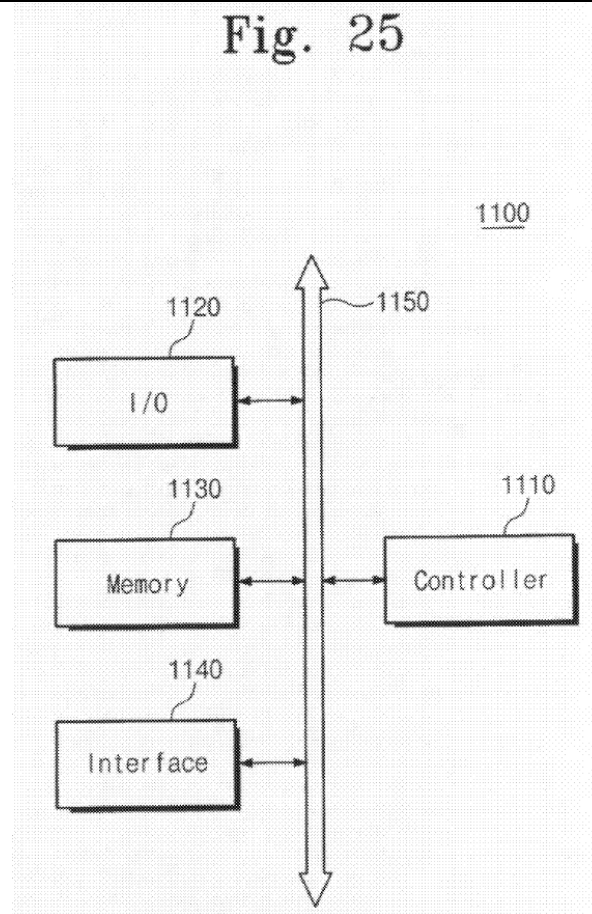


FIG. S – FIG. 25 of Park

[8.a] a plurality of first memory cells located in a first device level of a memory device

[8.b] a plurality of second memory cells located in a second device level of the memory device

169. Park discloses that memory 1130 includes a nonvolatile memory device having a 3D structure, where “each xy plane includes m memory cells and the xy plane including m memory cells may be stacked to have n layers.” EX1005, [0043].

170. Regarding its first embodiment, as shown in annotated FIGs. 2 and 3 below (FIG. T of my Declaration with annotations), Park discloses the first memory

cells (enclosed in brown dashed box) in a first layer of the nonvolatile memory device, which constitutes “a plurality of first memory cells located in a first device level of a memory device,” as recited in element [8.a]. EX1005, [0043].

Fig. 2

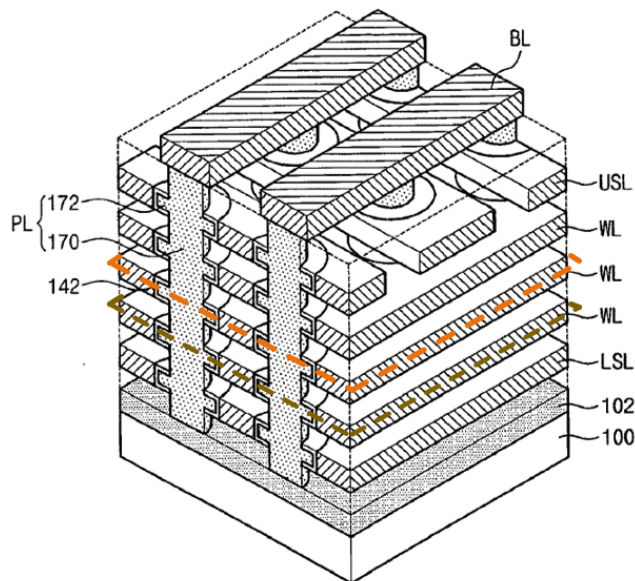


Fig. 3

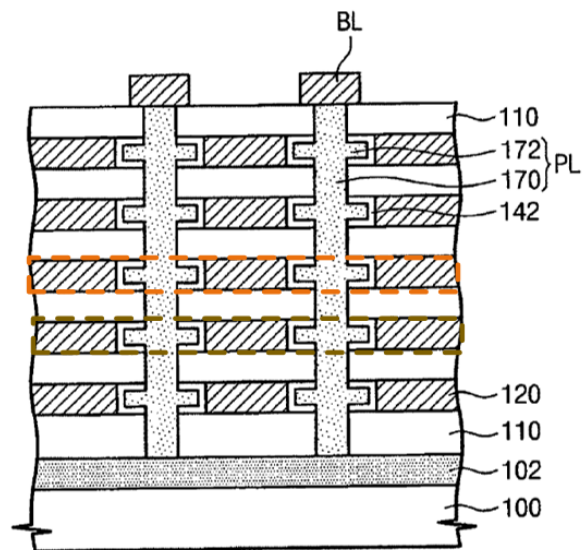


FIG. T – FIGs. 4 and 5 of Park (annotated)

171. Similarly, Park further discloses the second memory cells (enclosed in the orange dashed box in FIG. T above) in a second layer of the nonvolatile memory device, which constitutes “a plurality of second memory cells located in a second device level of a memory device,” as recited in element [8.b]. EX1005, [0048].

172. Thus, Park explicitly discloses claim elements [8.a] and [8.b].

[8.c] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate

[8.d.1] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate

[8.d.2] wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction

173. Park discloses that “[s]ince the word line of each layer is formed to have a plate shape, the same voltage may be applied to word lines of the memory cells formed on the same layer.” EX1005, [0048].

174. As shown in annotated FIGs. 2 and 3 below (FIG. U of my Declaration with annotations), the nonvolatile memory device of Park includes a first conductive layer 120 (in brown) formed in the first layer and used as a first word line WL to control access to the first memory cells in the first layer, which satisfies the claimed “a first control gate formed in the first device level, the first control gate to control access to the first memory cells” in element [8.c]. EX1005, [0041], [0048]. For instance, Park discloses that “[s]ince the word line of each layer is formed to have a plate shape, the same voltage may be applied to word lines of the memory cells formed on the same layer.” EX1005, [0048].

thus have understood that a silicon nitride charge trapping layer constitutes the claimed “memory element” for storing charge.

177. Park further discloses that “active pillars (PL) may penetrate the conductive layers (USL, WL, LSL),” and that “charge storage layer pattern 142 is disposed between the protrusion 172 of the active pillar (PL) and a sidewall of each of the conductive layers (USL, WL, LSL).” EX1005, [0050], [0054].

178. As shown in FIG. U above, a POSITA would have understood that active pillar PL (in pink) and charge storage patterns 142 (in red) create a respective hole (in blue, see also 136 and 134 in FIG. 5) through each of the first and second conductive layers WL 120. The holes are occupied by active pillar PL and charge storage patterns 142. Therefore, a POSITA would have understood that each hole (in blue) is the claimed “cavity of the first/second control gate” in elements [8.c] and [8.d.1], and the active pillar PL and corresponding charge storage pattern 142 occupying each hole is the claimed “memory element.”

179. To the extent that the claimed “cavity” requires a hole in the control gate layer to have a larger diameter than the holes in the layers above and below the control gate layer, Park’s FIGs. 3 and 5 still disclose the “cavity.” As shown in the repeated FIG. U below (annotated FIG. 3 of Park), a POSITA would have understood that the holes (in blue) in first and second conductive layers WL 120 (in brown and orange) have a larger diameter than the holes (in yellow) in interlayer

insulating layers 110 (in green) above and below conductive layer WL 120. EX1005, [0052]. Specifically, Park discloses that “a diameter of a hole formed in the conductive layer 120 may be greater than a diameter of a hole formed in the interlayer insulating layer 110.” EX1005, [0063]. Thus, Park discloses the claimed “memory element formed in a cavity of the first/second control gate” in [8.c] and [8.d.1], under either party’s construction. See Section VII.C.

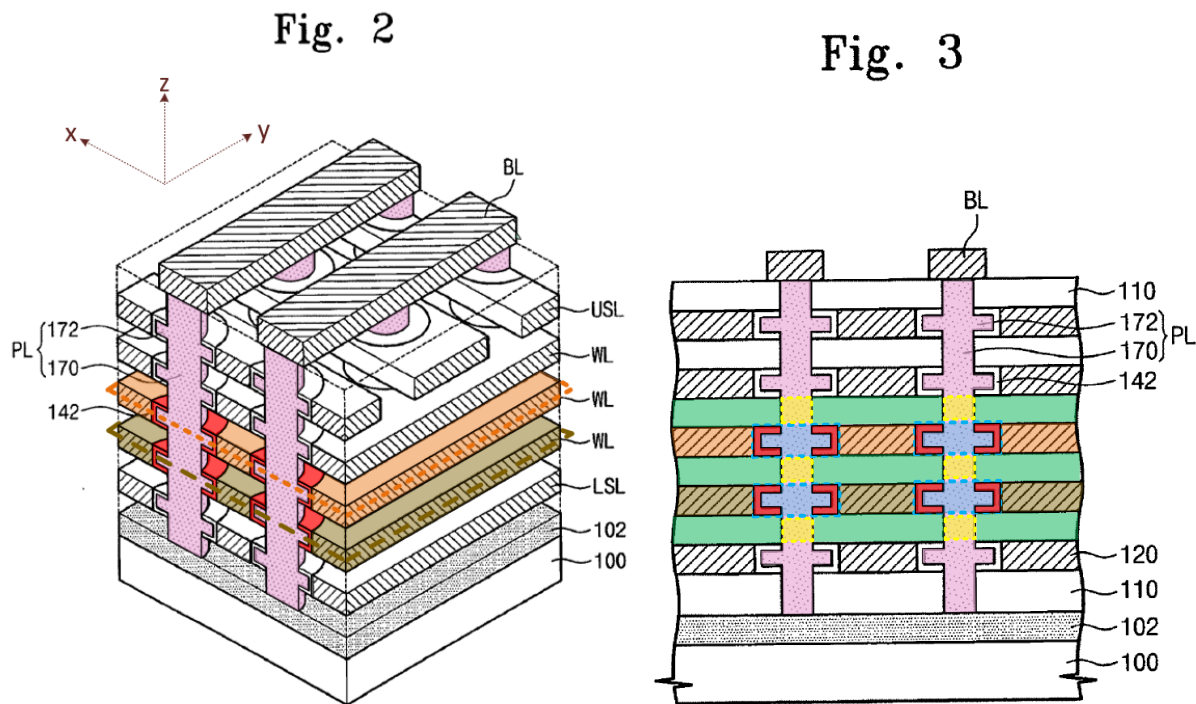


FIG. U – FIGs. 2 and 3 of Park (annotated)

180. Additionally, Park discloses that the memory cells in each xy plane/layer are arranged in an array form including multiple cells along the x-direction and y-direction, respectively, as shown in annotated FIG. 2 above. Therefore, Park discloses that “the first and second memory cells include multiple

memory cells arranged in a first direction and multiple memory cells arranged in a second direction.” EX1005, [0039], [0042]-[0043], FIG. 2.

181. Based on the above analysis, it is my opinion that Park discloses elements [8.c], [8.d.1], and [8.d.2].

[8.e] a common source

182. As shown in FIGs. 2 and 3 below (FIG. V of my Declaration with annotations), Park further discloses “an impurity region 102[(in purple)] (or a well) provided as a common source line” “to which the sources of the lower select transistors (LST) are commonly connected.” EX1005, [0040], [0047]. A POSITA would have understood that impurity region 102 is a semiconductor common source, as it is “formed in the semiconductor substrate 100” and connected to multiple active pillars PL/strings of memory cells. EX1005, [0047].

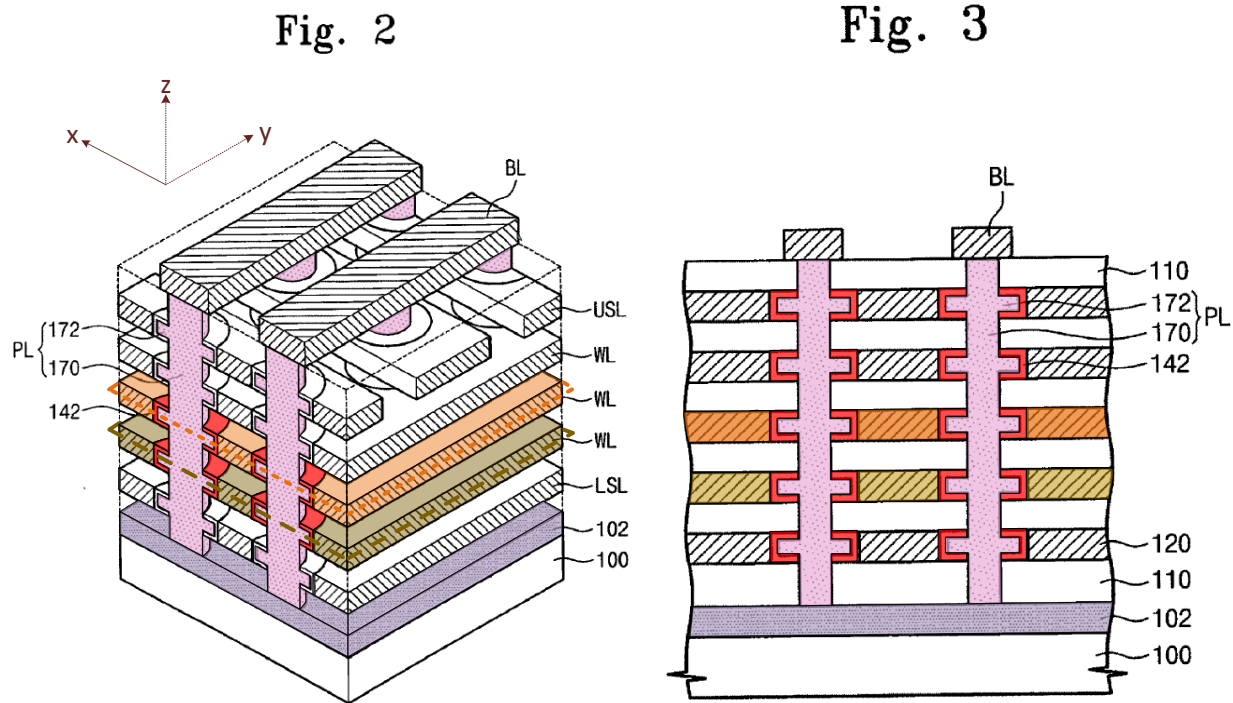


FIG. V – FIGs. 2 and 3 of Park (annotated)

183. A POSTIA would have understood that impurity region 102 serves as a shared source line for the memory strings, allowing a common electrical potential to be applied across multiple memory cells. EX1005, [0047]. Given that impurity region 102 is explicitly formed within a semiconductor substrate, a POSITA would recognize that it is composed of a doped semiconductor material, such as doped silicon. EX1005, [0047]. This is consistent with conventional 3D NAND architecture, where a common source region is often implemented using a doped region in the semiconductor substrate.

184. Accordingly, Park discloses a semiconductor common source.

[8.f.1] data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions

[8.f.2] wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate

185. As shown in annotated FIGs. 2 and 3 below (FIG. W of my Declaration with annotations), Park discloses bit lines BL (in green) that are electrically connected to impurity region 102 (in purple) and the first and second memory cells in the first and second layers (in brown and orange) through active pillars PL (in pink). EX1005, [0047], [0050]-[0052], [0056].

Fig. 2

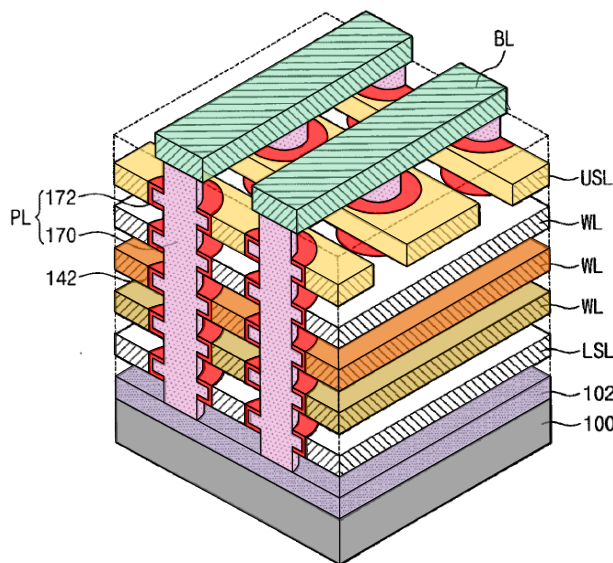


Fig. 3

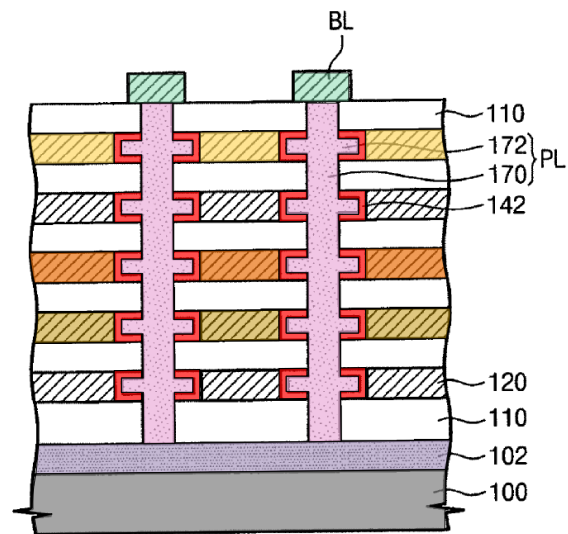


FIG. W – FIGs. 2 and 3 of Park (annotated)

186. Park also describes that “[e]ach string (STR) includes a plurality of memory cells (MC) serially connected to each other between an upper transistor (UST) and a lower transistor (LST). Drains of the upper select transistors (UST) are connected to the bit lines (BL1~BL3) and sources of the lower select transistors (LST) are connected to the common source line (CSL),” “upper select transistors (UST) are connected to the upper select lines (USL1~USL3) and the lower select transistors (LST) are connected to the lower select line (LSL),” and “bit lines (BL) cross the upper select lines (USL) and may be electrically connected to the active pillars (PL).” EX1005, [0040]-[0041], [0056].

187. As illustrated in FIG. W above, a POSITA would have understood that the electrical connections between bit lines BL (in green) and active pillars PL (in pink) are controlled by select transistors UST/LST. This selective coupling ensures that each string STR of memory cells along a respective active pillar PL can be selected or deselected by turning the select transistors UST/LST on or off via select lines USL/LST (in yellow/white hatched).

188. Accordingly, Park explicitly discloses that bit lines BL are configured to be “selectively” coupled to impurity region 102 and the first and second memory cells in the first and second layers through active pillars PL.

189. Thus, Park discloses the claimed “data lines configured to be selectively coupled to the common source and the first and second memory cells” in element

[8.f.1].

190. Park further discloses that active pillar PL is formed of “a polycrystalline semiconductor or a single crystalline semiconductor.” EX1005, [0050], [0071]. Likewise, the '214 patent also describes that “a **conductive material** 2001 has been formed by, for example, depositing **undoped or lightly doped polysilicon** to place channels 1841 **in electrical communication** with pillars 705.” EX1001, 8:64-67. Therefore, it is clear to me that Park’s active pillar PL having a polycrystalline semiconductor, such as polysilicon, includes the claimed “conductive material,” which also encompasses “undoped or lightly doped polysilicon in electrical communication with pillars 705.” EX1001, 8:64-67.

191. Furthermore, Park discloses that active pillar PL extends vertically through the conductive layers, including the first and second conductive layers WL 120. EX1005, [0042], [0052]. As a result, a POSITA would have understood that active pillar PL, including the claimed “conductive material,” also extends through the first and second memory cells in the first and second layers in the z-direction. This z-directional extension is perpendicular to the xy plane, where the first and second memory cells are arranged.

192. Thus, Park alone discloses or at least renders obvious “data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending

through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions,” as recited in element [8.f.1].

193. Regarding [8.f.2], as I discussed above in Section X.A, a POSITA would have found it obvious to modify Park’s nonvolatile memory device in view of Mokhlesi to form a metal/silicide common source at the top of its memory device.

194. For instance, in the example modified nonvolatile memory device of Park in view of Mokhlesi, as shown in FIG. X of my Declaration below, a metal/silicide common source 102’ (in purple) is formed over semiconductor substrate 100 (in gray). I have noticed that, according to the ’214 patent, “the term ‘on’ used with respect to two or more materials, one ‘on’ the other, means at least some contact between the materials, while ‘over’ ... could refer to either a material being ‘on’ another material or where there is one or more additional intervening materials between the materials (e.g., contact is not necessarily required).” EX1001, 5:30-38. Thus, a POSITA would have understood that metal/silicide common source 102’ is positioned “over” semiconductor substrate 100, with intervening layers in between, according to the ’214 patent.

Fig. 3

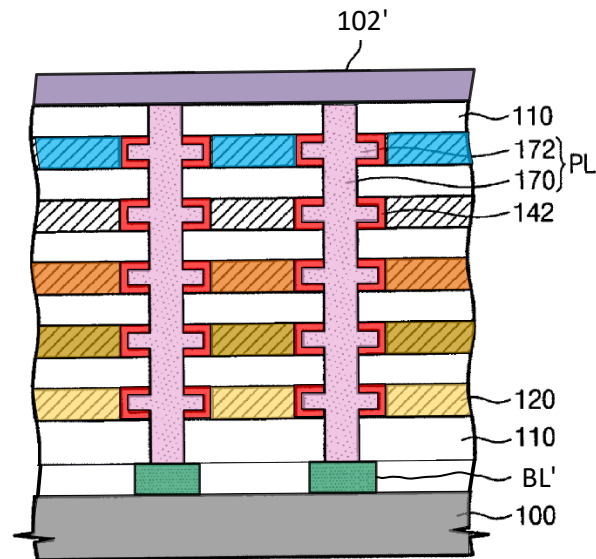


FIG. X – FIG. 3 of Park (modified and annotated)

195. In this modified structure, the first and second memory cells in the first and second layers, the same as first and second conductive layers 120 (in brown and orange), are positioned vertically between metal/silicide common source 102' (in purple) and semiconductor substrate 100 (in gray).

196. Therefore, Park in view of Mokhlesi renders obvious element [8.f.2].

C. Dependent Claim 13

197. Claim 13 depends on independent claim 9 and thus includes all claim elements of claim 9.

198. Claim 9 is reproduced below. For ease of discussion, I have included a label for each claim element.

[9.P] An apparatus comprising:

[9.a] a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device;

[9.b] a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level;

[9.c] a conductive material extending through the first and second memory elements; and

[9.d] a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material.

Claim 13 further requires that “the data line is located between the substrate and the first memory cell.”

Firstly, it is my opinion that Park alone discloses or otherwise renders obvious each element of independent claim 9, as discussed below in detail.

[9.P] An apparatus comprising

[9.a] a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device

[9.b] a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level

199. As I discussed in Section X.B([8.P]-[8.d.2]), Park discloses

“an apparatus comprising” a “plurality of first/second memory cells located in a first/second device level of a memory device,” where “each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.”

200. A POSITA would have recognized that the first and second memory cells, located in the first and second layers are part of a **nonvolatile** memory device. EX1005, [0045]. Accordingly, Park also discloses a “first **non-volatile** memory cell” corresponding to the first memory cells and a “second **non-volatile** memory cell” corresponding to the second memory cells.

201. Additionally, Park describes the formation of charge storage layer 140, which is **conformally** deposited along the surface of second hole 136. Specifically, Park discloses that the charge storage layer is formed by “sequentially depositing a charge blocking layer, a charge trapping layer, and a charge tunneling layer.” EX1005, [0064]; see also FIGs. 5-6. Given this process, a POSITA would have understood that charge storage layer pattern 142 (in red) includes a charge trapping layer that conforms to the surface of second hole 136. Since the charge storage layer follows the perimeter of the hole in which it is deposited, it inherently forms a “ring shape,” satisfying the claimed features in elements [9.a] and [9.b]

202. Furthermore, annotated FIG. 2 below (FIG. Y of my Declaration with annotations), clearly depicts the “ring shape” of each charge storage layer pattern

142 (in red). A POSITA would have understood that the charge trapping layer in charge storage layer pattern 142 also has the same “ring shape” as charge storage layer pattern 142 since the charge trapping layer is formed in a conformal manner around the active pillars. EX1005, [0064], FIGs. 5-6.

Fig. 2

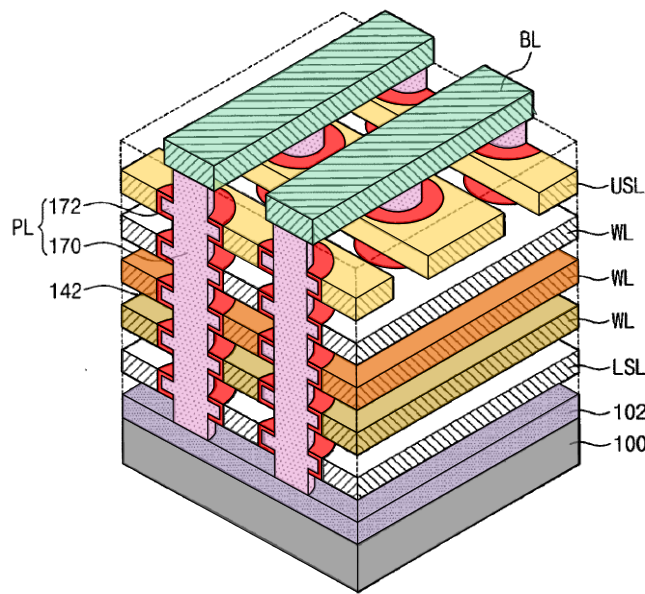


FIG. Y – FIG. 3 of Park (annotated)

203. Thus, Park discloses or at least suggests the presence of a ring-shaped memory element in the first and second non-volatile memory cells, satisfying the elements [9.a] and [9.b]

[9.c] a conductive material extending through the first and second memory elements

[9.d] a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material

204. As I discussed above in Section X.B ([8.e]-[8.f.2]), Park discloses “a common source” and “data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.”

205. Thus, Park discloses elements [9.c] and [9.d].

[13] The apparatus of claim 9, wherein the data line is located between the substrate and the first memory cell.

206. As I discussed above in Sections X.A and X.B([8.f.2]), a POSITA would have found it obvious to modify Park’s nonvolatile memory device in view of Mokhlesi to form a metal/silicide common source at the top of the 3D memory device and relocate the bit lines BL to the bottom.

207. For instance, in the example modified nonvolatile memory device of Park in view of Mokhlesi, as shown in FIG. Z of my Declaration below, the modified bit line BL’ (in green), corresponding to the claimed “data line,” is positioned vertically between semiconductor substrate 100 (in gray) and the first

memory cell in the same first layer as first conductive layer 120 (first word line WL, in brown). By positioning the bit lines below the memory array while placing the metal/silicide common source at the top, the modified architecture optimizes the electrical routing and enhances performance by reducing resistive losses and improving signal integrity.

Fig. 3

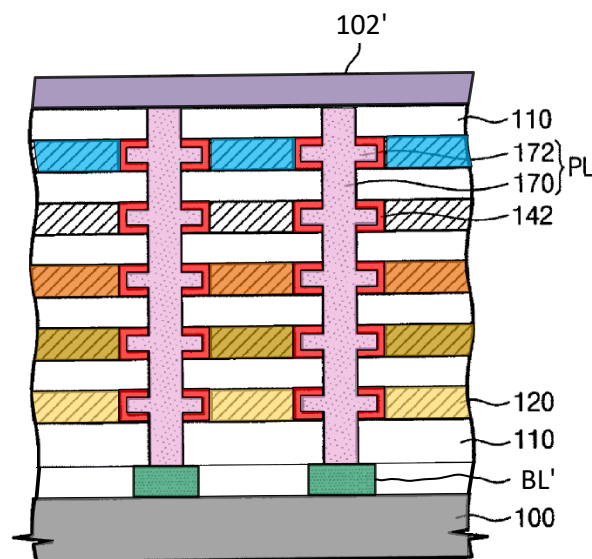


FIG. Z – FIG. 3 of Park (modified and annotated)

208. Accordingly, it is my opinion that Park in view of Mokhlesi renders obvious claim 13.

D. Independent Claim 21

[21.P] An apparatus comprising

209. As I discussed in Section X.B([8.P]), Park discloses “[a]n apparatus.”

[21.a] a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall
[21.b] a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall

210. As I discussed in Section X.B([8.c]-[8.d.1]), Park discloses “a first/second control gate formed in the first/second device level, ..., wherein each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.”

211. Regarding the claim feature about “first/second conductive material located in a first/second device level, ... including a first/second cavity” recited in elements [21.a] and [21.b], I have noticed that the specification of the ’214 patent describes that “[m]aterials 1002, 1004, and 1006 can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon),” and “[f]orming cavities 1120 in materials 1002, 1004, and 1006 also form control gates 1221, 1222, and 1223, which can correspond to control gates 221, 222, and 223 of FIG. 2.” EX1001, 7:3-5, 39-42.

212. Likewise, Park explicitly discloses that “conductive layer 120 may be formed of a polysilicon layer or a metal layer.” EX1005, [0060]. Based on this disclosure, a POSITA would have understood that the first and second conductive layers WL 120 may be composed of either metal or polysilicon, which is consistent

with the '214 patent. Accordingly, Park's disclosure directly meets elements [21.a] and [21.b] requiring first and second conductive materials.

213. Furthermore, Park discloses that “charge storage layer pattern 142 [is] in contact with sidewalls of the conductive layers (USL, WL, LSL),” and that “charge storage layer 140 may be formed on ... sidewalls of the conductive layers 120 ... exposed by the second hole 136.” EX1005, [0054], [0064]. These statements indicate that the charge storage layer is in contact with the sidewalls of the conductive layers. A POSITA would have recognized that this is describing the presence of “first/second cavities” within the first and second conductive layers, where each cavity has a corresponding sidewall formed by the exposed surface of the respective conductive layer.

214. Given that charge storage layer 140 is explicitly described as conformally forming along the exposed surfaces of the conductive layers, a POSITA would have further understood that the first and second cavities (i.e., holes within the first and second conductive layers WL 120) are defined by the sidewalls of these conductive layers. Thus, Park discloses, or at least renders obvious, elements [21.a] and [21.b] requiring a first and second conductive material having a corresponding first and second sidewall.

215. Accordingly, it is my opinion that Park discloses elements [21.a] and [21.b].

[21.c] a first dielectric formed on the first sidewall and the second sidewall

[21.d] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric

[21.e] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric

[21.f] a second dielectric formed on a side of the first memory element and on a side of the second memory element

216. As I discussed in Section X.B ([8.c]-[8.d.1]) above, Park discloses that “each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.”

217. Park further explicitly discloses that charge storage layer pattern 142/charge storage layer 140 has an “ONO” structure, stating that “charge storage layer 140 may be formed by **sequentially** depositing a charge blocking layer, a charge trapping layer, and a charge tunneling layer.” EX1005, [0064]. Additionally, Park further specifies that “[a]n oxide layer, a nitride layer, and an oxide layer may be **sequentially** formed on a surface of the second hole 136.” EX1005, [0064].

218. A POSITA would recognize this description as referring to the ONO (oxide-nitride-oxide) structure commonly used in charge storage memory devices, where the charge blocking and charge tunneling layers are composed of silicon oxide.

219. Furthermore, Park states that “charge storage layer pattern 142 is disposed between the protrusion 172 of the active pillar (PL) and a sidewall of each of the conductive layers (USL, WL, LSL).” EX1005, [0054]. This disclosure confirms that the charge storage layer pattern 142 is in contact with the sidewalls of the cavities formed within the conductive layers.

220. Given this, a POSITA would have understood, or at least found it obvious, that the nonvolatile memory device includes a silicon oxide charge blocking layer, satisfying the claimed “first dielectric”, as part of charge storage layer pattern 142, which is formed on the sidewalls of holes 136. EX1005, FIGs. 3, 5. Thus, Park discloses element [21.c].

221. A POSITA would have also understood, or at least found it obvious, that the nonvolatile memory device includes a silicon oxide charge tunneling layer, satisfying the claimed “second dielectric,” located within charge storage layer pattern 142. This charge tunneling layer is formed on the sides of the corresponding charge trapping layers, corresponding to the claimed “first/second memory elements.” Thus, Park discloses element [21.f].

222. Given that the ONO structure provides electrical isolation between the charge trapping layer and the surrounding conductive materials, a POSITA would have further recognized that the respective charge trapping layer, corresponding to the claimed “first/second memory element,” is electrically isolated from the

corresponding first or second conductive layer WL 120, corresponding to the claimed “first/second conductive material,” by a respective portion of the silicon oxide charge blocking layer formed on the sidewalls.

223. Thus, Park’s disclosure supports, or at least renders obvious, the presence of the first and second dielectric layers and their respective roles in electrically isolating the charge storage elements within the nonvolatile memory device. Thus, Park discloses or at least renders obvious elements [21.d] and [21.e].

[21.g] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric

224. Park explicitly describes that “through the active pillars (PL), a channel of string select transistors and memory cell transistors may be electrically connected,” and further clarifies that “a channel can be formed in the protrusion 172 when the nonvolatile memory device operates.” EX1005, [0042], [0050], [0052]. This disclosure indicates that the active pillars PL serve as the conductive paths for charge carriers, effectively acting as channels for the memory cells and select transistors. A POSITA would have understood, or at least found it obvious, that protrusions 172 of active pillar PL function as the claimed “conductive channel” of a string STR of memory cells.

225. Park also explicitly discloses that “channels of the select transistors

(UST, LST) and the memory cell transistors (MC) may be formed to be perpendicular to an xy plane,” and that “active pillars (PL) may penetrate the conductive layers (USL, WL, LSL).” EX1005, [0042], [0050]-[0052].

226. A POSITA would have recognized that these statements indicate that the conductive channels extend vertically through the memory structure. Specifically, the channel of active pillar PL extends from the first layer to the second layer where the first and second conductive layers WL 120 are formed, respectively. This vertical channel architecture is consistent with the structure of 3D NAND memory, where memory cells are arranged in a stacked fashion, and a continuous channel extends through multiple device levels.

227. Therefore, Park discloses the claimed “conductive channel extending from the first device level to the second device level” in element [21.g].

228. As I further discussed above, Park discloses that “[a]n oxide layer, a nitride layer, and an oxide layer may be sequentially formed on a surface of the second hole 136,” and that “charge storage layer pattern 142 is disposed between the protrusion 172 of the active pillar (PL) and a sidewall of each of the conductive layers (USL, WL, LSL).” EX1005, [0054], [0064]. A POSITA would have understood that these layers correspond to an ONO (oxide-nitride-oxide) charge storage structure, where the nitride layer serves as the charge-trapping layer, constituting the claimed “first and second memory elements.”

229. Since Park discloses that charge storage layer patterns 142 are positioned between the conductive layers 120 and active pillar PL, a POSITA would have further understood, or at least found it obvious, that protrusions 172 of active pillar PL, corresponding to the claimed “conductive channel,” face the silicon nitride charge trapping layers, corresponding to the claimed “first and second memory elements.”

230. In addition, Park also describes the presence of a silicon oxide charge tunneling layer between the charge trapping layer and the conductive channel. A POSITA would have recognized that this tunneling layer serves as an electrical barrier, preventing direct electrical conduction between the charge trapping layer and protrusions 172 of active pillar PL. Specifically, a respective portion of the silicon oxide charge tunneling layer, corresponding to the claimed “first/second portion of the second dielectric,” ensures that the charge stored in the memory elements remains electrically isolated while allowing controlled charge transfer during programming and erasing operations.

231. Accordingly, it is my opinion that Park discloses or at least suggests element [21.g].

[21.h] a substrate

232. Park discloses a semiconductor substrate 100. EX1005, [0047]. Thus, Park discloses element [21.h].

[21.i] a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate

233. As discussed in Section X.B ([8.f.1]-[8.f.2]), Park discloses that electrical connections between bit lines BL and active pillars PL are controlled by select transistors UST/LST. These select transistors act as switching elements that determine whether a given memory string STR is active or inactive. Specifically, each string of memory cells along an active pillar PL can be selectively coupled or decoupled from bit line BL by turning select transistors UST/LST on or off through select lines USL/LST. A POSITA would have understood that this configuration allows for controlled access to memory cells, ensuring proper read/write operations.

234. Thus, Park discloses a structure in which bit line BL, satisfying the claimed “data line,” is configured to “selectively” coupled to active pillar PL, including protrusions 172, through select transistors UST/LST. This selective coupling mechanism is essential for reliable memory operation, as it ensures that only the desired memory cells are accessed at any given time while preventing unintended interference from other memory strings.

235. Further, as I discussed in Section X.A, a POSITA would have found it obvious to modify Park’s nonvolatile memory device (as shown in FIGs. 2 and 3) in view of Mokhlesi to form a metal/silicide common source at the top of the 3D memory device and bit lines BL at the bottom.

236. For example, as depicted below in FIG. AA of my Declaration, the modified nonvolatile memory device of Park in view of Mokhlesi features a modified bit line configuration. In this structure, modified bit line BL' (in green) is positioned vertically between the second conductive layer WL 120 (in orange) and semiconductor substrate 100 (in gray). That is, the modified structure satisfies the claimed relative position feature that “the data line is located between the second conductive material and the substrate” in element [21.i].

Fig. 3

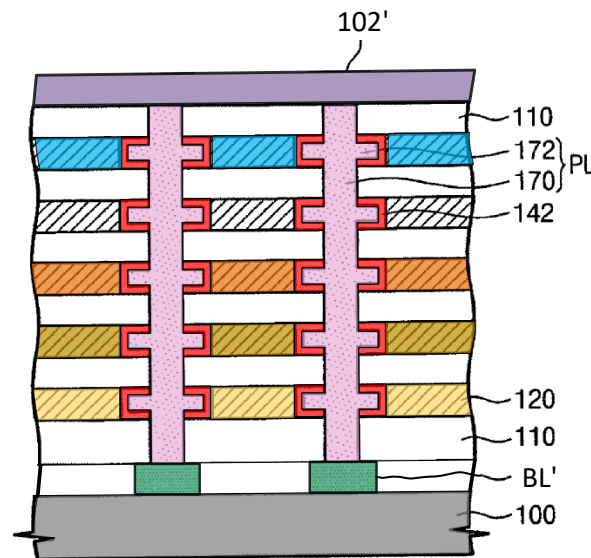


FIG. AA – FIG. 3 of Park (modified and annotated)

237. From the foregoing, it is my opinion that Park in view of Mokhlesi renders obvious claim 21.

XI. Ground 4: Fukuzumi In View of Mokhlesi Renders Obvious Claims 8 And 21

A. Reasons to Combine Fukuzumi and Mokhlesi

238. In my opinion, a POSITA would have found it obvious to modify Fukuzumi's 3D memory device and fabrication method thereof in view of Mokhlesi's teaching of forming a common source at the top and bit lines at the bottom of a 3D memory device. I will discuss various reasons in detail below.

1. Teaching, suggestion, or motivation in the prior art

239. As I discussed in Section VIII.D, Fukuzumi aims to address challenges associated with transitioning semiconductor memory devices from 2D to 3D structures. EX1007, [0003], [0040]. Specifically, Fukuzumi discloses the use of a p-well region Ba1, which is formed within an n+ region of a semiconductor substrate Ba, as the common source. Fukuzumi's common source is made of semiconductor material. EX1007, [0081], [0086].

240. However, the use of semiconductor material for common sources introduces significant electrical performance limitations, with current crowding being a particularly critical concern. Current crowding occurs when the flow of electrical current is not evenly distributed, leading to localized areas of high current density. This uneven distribution can result in serious reliability issues, including localized overheating and thermal hotspots, which degrade device performance and

longevity. Furthermore, increased electromigration effects—where high current density causes the gradual movement of metal atoms—can lead to the formation of voids and eventual circuit failure. EX1014, 1344; EX1015, 239, 242; EX1016, 1, 4.

241. These challenges are further exacerbated in a 3D memory architecture, where the common source and bit lines are vertically stacked. The confined geometry of 3D NAND and similar memory structures limits heat dissipation and increases current density, making current crowding effects even more severe.

242. As I discussed in Section VIII.C, Mokhlesi directly addresses this problem by teaching that source lines should be placed at the top of a 3D NAND memory device and made of metal or silicide rather than semiconductor material. Mokhlesi explains that this approach “allow[s] formation of metal and/or silicide rather than semiconductor source lines, which leads to a decreased current crowding due to the lower resistivity source line material.” EX1006, [0092].

243. Given that Fukuzumi’s common source is also made of semiconductor material, it suffers from the exact same current crowding problem identified by Mokhlesi. Thus, a POSITA would have naturally been motivated to adopt Mokhlesi’s solution—“source lines may be formed on top and the bit lines may be formed on the bottom” and “formation of metal and/or silicide rather than semiconductor source lines”—to address the same current crowding issue in Fukuzumi’s 3D memory device. Adopting this solution in Fukuzumi’s structure

would, therefore, be an obvious design choice for enhancing the electrical performance and durability of the memory device. As Mokhlesi explains, “formation of metal and/or silicide rather than semiconductor source lines... leads to decreased current crowding due to the lower resistivity source line material.” EX1006, [0092].

244. By replacing Fukuzumi’s semiconductor common source with a metal and/or silicide common source at the top of the 3D memory device, the modification would significantly enhance current distribution and minimize localized heating and electromigration effects. This improvement would be particularly beneficial in high-density 3D NAND architectures, where current crowding effects are more pronounced due to vertical stacking. Ultimately, this modification would directly advance Fukuzumi’s goal of addressing challenges associated with transitioning semiconductor memory devices from 2D to 3D structures.

245. Furthermore, Mokhlesi’s teaching regarding source lines is directly applicable to a common source region. Mokhlesi explicitly states that “[i]n another alternative embodiment, the source lines 239 are be replaced by a common source region (source plane) extending in both dimensions of the plane of the substrate 1 (in the x-y plane).” EX1006, [0094].

246. Additionally or alternatively, a POSITA would have found it obvious to apply Mokhlesi’s teaching regarding source lines to Fukuzumi’s common source

(p-well region Ba1). Mokhlesi explicitly states that a “common source plate provides a higher current sinking capability at the expense of losing the ability to select individual source line voltage.” EX1006, [0017], [0094]. This suggests that replacing individual source lines with a common source plate can enhance current distribution efficiency, thereby mitigating current crowding and related reliability issues. This principle directly aligns with Fukuzumi’s 3D memory architecture, which does not require the ability to select individual source line voltages, since the sources of each memory string (MS) are commonly connected to the p-well region Ba1. EX1007, [0081].

247. Therefore, given Mokhlesi’s well-documented benefits of such a structure in mitigating reliability concerns, a POSITA would have been naturally motivated to apply Mokhlesi’s teachings to optimize Fukuzumi’s common source configuration.

2. Applying known techniques to a known device ready for improvement

248. Furthermore, the industry-wide recognition of the benefits of using metal or silicide for common sources reinforces the obviousness of applying Mokhlesi’s teachings to Fukuzumi’s 3D memory device. It was well understood that high resistivity in semiconductor materials leads to increased voltage drops and power losses, negatively impacting device efficiency and reliability. By contrast,

metals and silicides offer superior conductivity, reducing resistive losses and enabling more efficient current distribution, particularly in high-density memory architectures like 3D NAND. EX1009, 11.

249. Additionally, memory manufacturers had already begun implementing alternative source placement strategies to address these resistivity challenges. Prior industry literature proposed positioning the common source at the top of the memory stack, as opposed to the bottom, specifically to facilitate the use of low-resistivity materials such as metals or silicides. EX1012, 136-137; EX1013, 22-23. These established solutions demonstrated that transitioning from a semiconductor common source to a metal or silicide common source was a predictable design choice that offered clear advantages in minimizing resistance, reducing power consumption, and enhancing overall device performance.

250. Given this industry knowledge, a POSITA would have recognized the clear benefits of adopting Mokhlesi's approach in Fukuzumi's device. The combination would yield a more reliable and efficient 3D NAND structure while maintaining compatibility with existing fabrication techniques, making it an obvious and advantageous modification.

251. A POSITA would have understood that implementing Mokhlesi's modification in Fukuzumi's structure would lead to a predictable reduction in current crowding, thereby enhancing the reliability and efficiency of the 3D

memory device.

3. *A POSITA Would Have Had a Reasonable Expectation of Success in Implementing the Modification*

252. A POSITA would have had a reasonable expectation of success in modifying Fukuzumi's 3D memory device by incorporating Mokhlesi's metal/silicide common source at the top. Both Fukuzumi and Mokhlesi describe 3D NAND memory devices with similar structural features, including vertically stacked memory cells, NAND memory strings, charge storage elements utilizing an "ONO" structure, and selection transistors positioned above and/or below the memory cells. See Sections VIII.C, VIII.D.

253. Mokhlesi explicitly describes repositioning the common source to the top of the 3D memory structure. EX1006, [0094]. This reconfiguration does not alter the fundamental function of the common source; rather, it enhances its efficiency by reducing resistance. The well-documented electrical benefits of metal and silicide materials further support a POSITA's expectation of success in making this modification.

254. Moreover, fabricating a metal/silicide common source at the top of Fukuzumi's memory device would have been well within a POSITA's skillset. The semiconductor industry has already developed standard manufacturing techniques for depositing and patterning metal and silicide layers. A POSITA would

have recognized that these techniques could be seamlessly integrated into Fukuzumi's process without introducing undue complexity. The proposed modification does not introduce any unpredictable results or undue complexities in the fabrication process. Instead, it aligns with well-established design improvements in the field and follows the logical progression of memory device optimization.

255. For example, as illustrated in the modified and annotated FIG. 2 of Fukuzumi (FIG. AB of my Declaration below), the proposed configuration involves forming modified bit lines BL' over the semiconductor substrate Ba, placing drain-side selection transistors SDTrmn and drain-side selection lines SGD above the bit lines, positioning word lines WL above the drain-side selection transistors, situating source-side selection transistors SStrmn and source-side selection lines SGS over the word lines WL, and finally forming a metal/silicide common source Ba1' at the top.

B. Independent Claim 8

[8.P] An apparatus comprising

258. Fukuzumi discloses a nonvolatile semiconductor memory device, which qualifies as the claimed “apparatus.” EX1007, [0073]. It is noted that, unless otherwise specified, Fukuzumi’s disclosures are applicable to the combination of Fukuzumi and Mokhlesi used in my Declaration for mapping in Ground 4. Therefore, Fukuzumi discloses [8.P].

[8.a] a plurality of first memory cells located in a first device level of a memory device

[8.b] a plurality of second memory cells located in a second device level of the memory device

259. Fukuzumi discloses that nonvolatile semiconductor memory device 100 includes memory cell strings MS, each of which includes memory cells MTr1 mn -MTr4 mn that are vertically and serially connected to each other. EX1007, [0079]-[0080], [0085]. I have noticed that, although Fukuzumi describes nonvolatile semiconductor memory device 100 and its accompanying figures, including FIG. 2 cited in Ground 4, in the context of the first embodiment, unless otherwise specified (e.g., with respect to memory layer 30 and word line conduction layers 36) in my Declaration, the disclosures regarding nonvolatile semiconductor memory device 100 are equally applicable to the second embodiment as well. EX1007, [0146]-[0148].

260. As illustrated in FIG. 2 of Fukuzumi (FIG. AC of my Declaration with annotations, below), first memory cells $MTr1mn$ (enclosed within brown dashed box and corresponding to WL1) are located in a first device level of nonvolatile semiconductor memory device 100 over semiconductor substrate Ba (in gray), while second memory cells $MTr2mn$ (enclosed within orange dashed box and corresponding to WL2) are located in a second device level of nonvolatile semiconductor memory device 100 over both the first device level and semiconductor substrate Ba. EX1007, [0077], [0081].

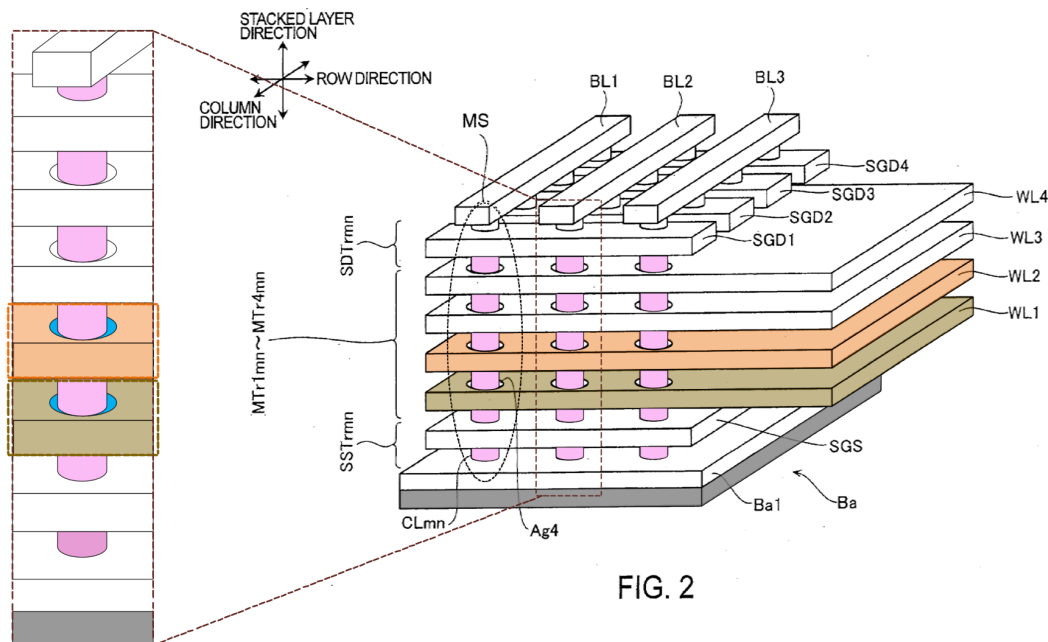


FIG. AC – FIG. 2 of Fukuzumi (annotated)

261. Based on the above disclosure, Fukuzumi discloses claim elements [8.a] and [8.b].

[8.c] a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate

[8.d.1] a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate

[8.d.2] wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction

262. Fukuzumi discloses that nonvolatile semiconductor memory device 100 includes vertically stacked word lines WL1–WL4, such as first–fourth word line conduction layers 36a–36d in the first embodiment or 361a–361d in the second embodiment. EX1007, [0101], [0148]. Each word line WL has a planar structure extending two-dimensionally and is connected to the gate of a corresponding layer of memory cells MTr1mn–MTr4mn within each memory string MS, with its end portions functioning as the control gates of the respective memory cells. EX1007, [0077], [0080], [0087], [0101], [0148].

263. Fukuzumi further discloses that “word line driving circuit 13 controls voltage applied to a word line WL” and has “a function as control circuits controlling the memory strings MS.” EX1007, [0076], [0090].

264. Therefore, as shown in annotated FIGs. 2 and 28 below (FIGs. AD and AE of my Declarations, respectively, with annotations), Fukuzumi discloses a first word line WL1 (in brown, e.g., first word line conduction layer 361a) in the first

device level to control access to first memory cells $MTr1mn$ (enclosed in the brown dashed box in FIG. 2) in the first device level, and a second word line $WL2$ (in orange, e.g., second word line conduction layer 361b) in the second device level to control access to second memory cells $MTr2mn$ (enclosed in the orange dashed box in FIG. 2) in the second device level.

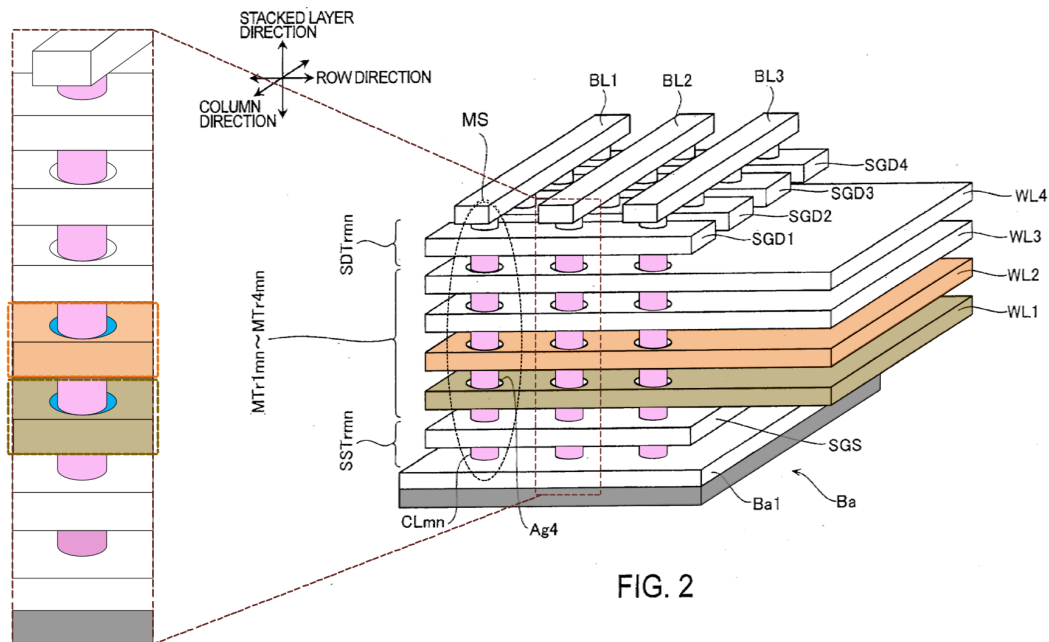


FIG. AD – FIG. 2 of Fukuzumi (annotated)

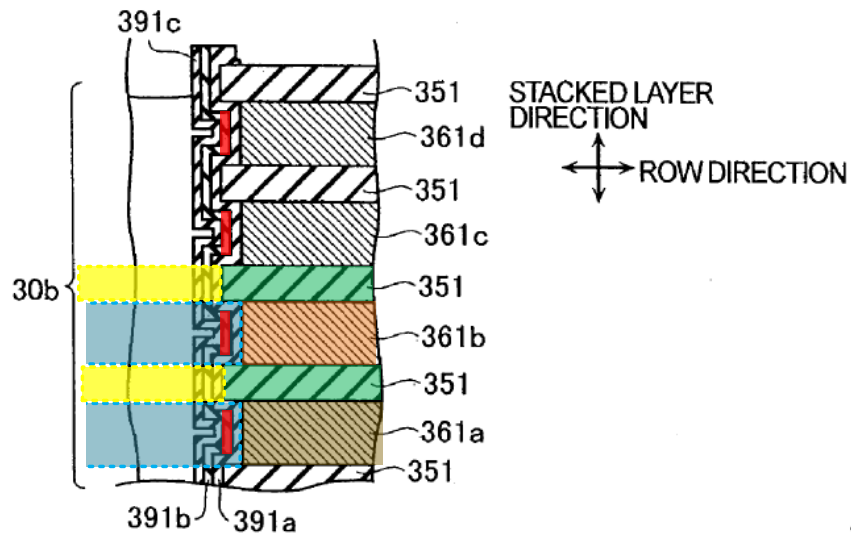


FIG. 28

FIG. AE – FIG. 28 of Fukuzumi (annotated)

265. Furthermore, Fukuzumi describes that each memory cell $MTr1mn$ or $MTr2mn$ contains a charge storage layer 39b/391b, composed of silicon nitride to facilitate data writing and reading. EX1007, [0114], [0148], [0151]. While Fukuzumi explicitly details the material composition and function of charge storage layer 39b in the first embodiment, a POSITA would have recognized that the same disclosures apply to charge storage layer 391b in the second embodiment. EX1007, [0146]. Consequently, a POSITA would have understood that charge storage layer 391b qualifies as the claimed “memory element.”

266. Additionally, Fukuzumi discloses that charge storage layer 39b/391b is formed within memory hole 37, which extends through word line conduction layers

36a/361a-36d/361d, as depicted in FIG. AE above. A POSITA would have therefore recognized that charge storage layer 391b (in red) resides inside memory hole 37 (in blue). EX1007, [0103]-[0104], [0148], FIG. 4.

267. As I discussed in Section VII.C, if the claim term “cavity” is construed to require that a hole in the control gate has a larger diameter than the holes in the layers above and below, memory hole 37 still satisfies the “cavity” construction. Fukuzumi explicitly states that charge storage layers 391b “are formed as the concavo-convex shape accompanying with the first-fourth word line conduction layer 361a-361d” and that “sidewalls of first-fourth word line conduction layers 361a-361d facing the fourth space Ag4 are formed as recesses corresponding to a side wall of an interlayer insulator 351.” EX1007, [0148], [0151]. A POSITA would have thus understood, as illustrated in FIG. AE above, memory hole 37 (in blue) within word line conduction layers 361a and 361b possesses a greater diameter than memory hole 37 (in yellow) within the interlayer insulators 351 (in green) located above and below each respective word line conduction layer 361a or 361b.

268. Accordingly, in my opinion, Fukuzumi discloses the claimed “cavity” limitation under either party’s construction.

269. Therefore, in my opinion, Fukuzumi discloses the claimed subject matter of elements [8.c] and [8.d.1]

270. In relation to element [8.d.2], Fukuzumi further describes that

“memory strings MS are also displaced like a matrix in a plane perpendicular to the columnar semiconductors CL_{mn} ,” as stated in EX1007, [0081] and illustrated in FIG. 2. Since Fukuzumi also discloses that “memory strings MS are constituted with memory cells $MTr1_{mn}$ - $MTr4_{mn}$,” it logically follows that memory cells $MTr1_{mn}$ - $MTr4_{mn}$ are arranged in a matrix pattern, meaning they are aligned in both row direction and column direction, which correspond to the claimed “first direction” and “second direction,” respectively.

271. Therefore, Fukuzumi discloses the claimed feature that “the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction” in element [8.d.2].

[8.e] a common source

272. Fukuzumi discloses that “[e]ach of the memory strings MS includes columnar semiconductors CL_{mn} on a p-well region Ba1 formed in an n⁺ region of a semiconductor substrate Ba,” and that “source means the n⁺-region formed in the p-well region Ba1 of the semiconductor substrate Ba.” EX1007, [0081], [0086]. Based on this disclosure, it is clear to me that the p-well region Ba1 functions as a “common source” shared by multiple memory strings MS.

273. The structural arrangement described in Fukuzumi ensures that the source region is not isolated to a single memory string but is instead a shared feature across multiple strings, allowing for efficient charge distribution and proper

operation of the memory arrays.

274. Therefore, Fukuzumi explicitly discloses the claimed “common source” in element [8.e].

[8.f.1] data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions

[8.f.2] wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate

275. As shown in FIG. 2 (FIG. AF of my Declaration with annotations, below), Fukuzumi discloses that bit lines BL (in green) are electrically connected to the p-well region Ba1 (in purple) and to memory cells MTrmn via columnar semiconductors CLmn (in pink). EX1007, [0081], [0109]. It is clear to me that bit lines BL qualify as the claimed “data lines” at least because the ’214 patent describes that “[d]ata lines 251, 252, and 253 sometimes correspond to bit lines or sense lines of a non-volatile memory device.” EX1001, 3:29-31.

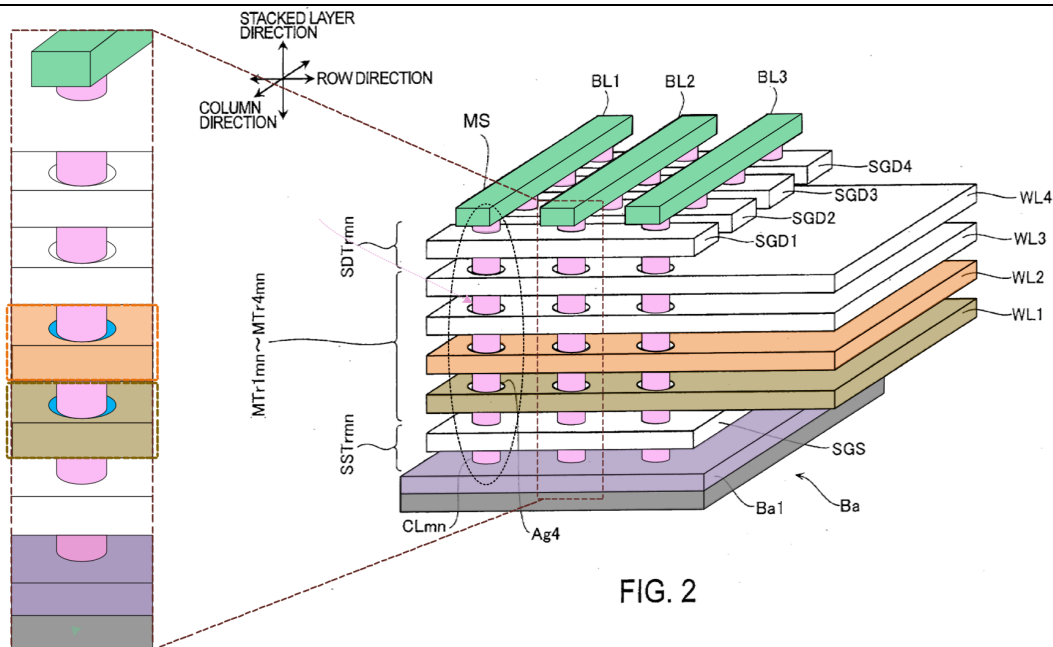


FIG. 2

FIG. AF – FIG. 2 of Fukuzumi (annotated)

276. Additionally, Fukuzumi discloses that bit lines BL are electrically connected to columnar semiconductor CLmn through selection transistors STrmn/SSTrmn, which are controlled by selection gate lines SGD/SGS. These selection gate lines are driven by the selection gate line SGD/SGS driving circuit 14/15. EX1007, [0076], [0082]-[0083], [0085], [0088]-[0089]. A POSITA would have understood that bit lines BL interact with memory cells MTrmn and p-well region Ba1 through selection transistor STrmn/SSTrmn, and that the selection gate line SGD/SGS driving circuit 14/15 enables or disables each memory string MS by toggling selection transistor STrmn/SSTrmn on or off. This, in turn, controls the connection between bit lines BL and memory cells MTrmn via selection gate lines SGD/SGS. EX1007, [0076]. Accordingly, Fukuzumi demonstrates that bit lines BL

are configured to be “selectively” coupled to memory cells MTr_{mn} and p-well region $Ba1$ through columnar semiconductor CL_{mn} .

277. Furthermore, Fukuzumi states that memory 38, which is part of columnar semiconductor CL_{mn} in both the first and second embodiments, is formed of silicon. EX1007, [0103]. Likewise, the '214 patent also describes that “a **conductive material** 2001 has been formed by, for example, depositing **undoped or lightly doped polysilicon** to place channels 1841 in electrical communication with pillars 705.” EX1001, 8:64-67. Therefore, it is clear to me that Fukuzumi’s columnar semiconductor CL_{mn} , which contains silicon, includes the claimed “conductive material,” consistent with the disclosure of the '214 patent.

278. Furthermore, Fukuzumi explains that columnar semiconductor CL_{mn} extends vertically along a stacked layer direction through word lines $WL1$ – $WL4$, including first and second word lines $WL1$ and $WL2$ positioned at different device levels. As a result, columnar semiconductor CL_{mn} , including the claimed “conductive material,” also extends vertically through the first and second memory cells $MTr1_{mn}$ and $MTr2_{mn}$ at the corresponding device levels. The stacked layer direction shown in FIG. AF above (annotated version of FIG. 2 of Fukuzumi) is perpendicular to the matrix plane defined by the row direction and the column direction, thereby aligning with the claimed “third direction.” EX1007, [0081], FIG.

2.

279. Thus, Fukuzumi discloses the claimed “data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material,” and “conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions,” as recited in element [8.f.1].

280. Regarding [8.f.2], as I discussed above in Section XI.A, a POSITA would have found it obvious to modify Fukuzumi’s nonvolatile memory device in view of Mokhlesi to form a metal/silicide common source at the top of its memory device.

281. For example, as illustrated in FIG. AG of my Declaration below, modifying Fukuzumi’s memory device in view of Mokhlesi results in a metal/silicide common source Ba1’ (in purple) positioned over semiconductor substrate Ba (in gray).

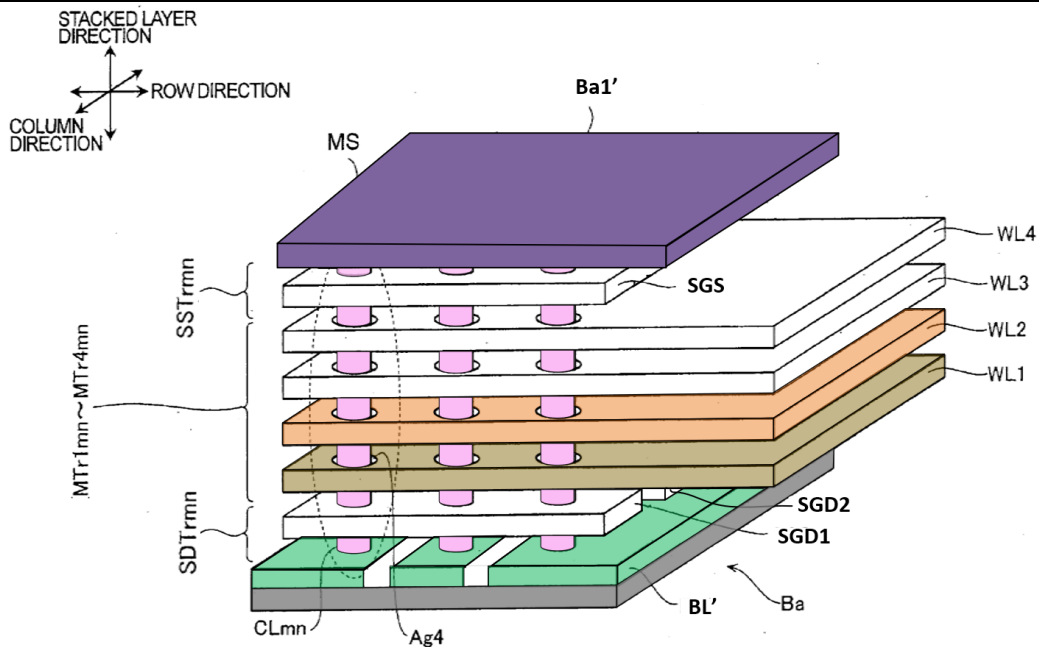


FIG. 2

FIG. AG – FIG. 2 of Fukuzumi (modified and annotated)

282. I have noticed that, according to the '214 patent, “the term ‘on’ used with respect to two or more materials, one ‘on’ the other, means at least some contact between the materials, while ‘over’ ... could refer to either a material being ‘on’ another material or where there is one or more additional intervening materials between the materials (e.g., contact is not necessarily required).” EX1001, 5:30-38. Thus, a POSITA would have understood that metal/silicide common source Ba1’ is positioned “over” semiconductor substrate Ba, with intervening layers in between, according to the '214 patent.

283. Under this configuration, first and second memory cells MTr1mn and MTr2mn are vertically positioned between the metal/silicide common source Ba1’

and semiconductor substrate Ba.

284. Therefore, it is my opinion that Fukuzumi in view Mokhlesi renders obvious element [8.f.2].

C. Independent Claim 21

[21.P] An apparatus comprising

285. As I discussed in Section XI.B([8.P]), Fukuzumi discloses “[a]n apparatus.”

[21.a] a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall

[21.b] a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall

286. As I discussed in Section X.B([8.c]-[8.d.1]), Fukuzumi discloses “a first/second control gate formed in the first/second device level,” and “a cavity of the first/second control gate.”

287. Fukuzumi further explicitly states that “[e]ach of the word lines WL1-WL4 is connected to each gate of the memory cells MTr1 mn -MTr4 mn in each of the memory strings MS and each of the word lines WL1-WL4 are formed of the same conductive layer and are common in plane each other.” EX1007, [0080]. This disclosure establishes that word lines WL1-WL4 serve as control gates and share a common conductive layer.

288. I notice that the '214 patent describes “conductive materials” in the context of word lines and control gate structures, which aligns with Fukuzumi’s disclosure. EX1001, 7:3-5, 39-42. From this, it follows that first and second word line conduction layers 361a and 361b of Fukuzumi —examples of word lines WL1-WL4—constitute the claimed “first/second conductive materials” in elements [21.a] and [21.b].

289. As shown in annotated FIGs. 2 and 28 below (FIGs. AH and AI of my Declarations, respectively, with annotations), a POSITA would have understood that each portion of memory hole 37 (in blue), in which charge storage layer 311b (in red) is formed, has a respective sidewall on first or second conductive layer 361a or 361b (in brown or orange) under either party’s interpretation of “cavity,” as I discussed in Section XI.B([8.c]-[8.d.1]).

290. Therefore, Fukuzumi explicitly discloses elements [21.a] and [21.b].

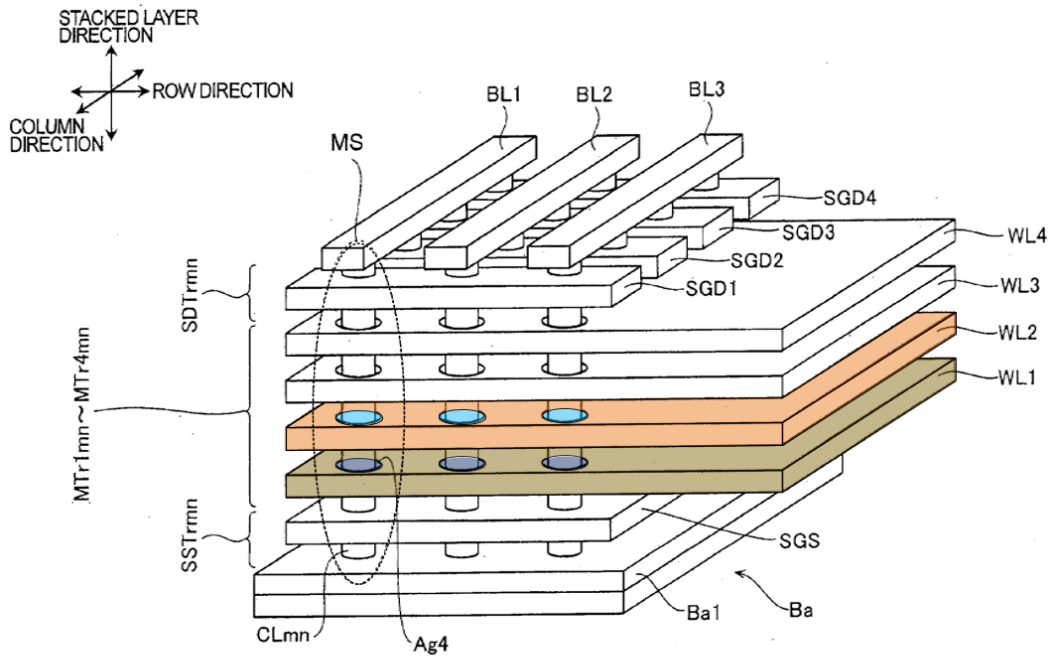


FIG. 2

FIG. AH – FIG. 2 of Fukuzumi (annotated)

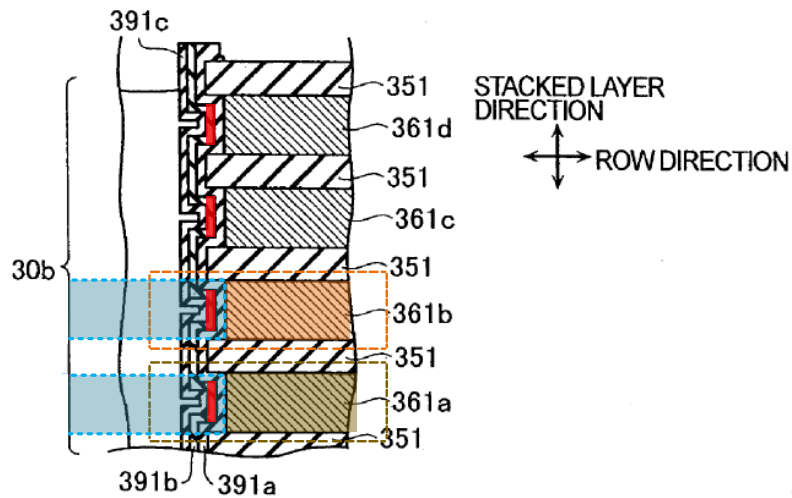


FIG. 28

FIG. AI – FIG. 28 of Fukuzumi (annotated)

[21.c] a first dielectric formed on the first sidewall and the second sidewall

[21.d] a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric

[21.e] a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric

[21.f] a second dielectric formed on a side of the first memory element and on a side of the second memory element

291. As I discussed in Section XI.B([8.c]-[8.d.1]) above, Fukuzumi discloses that “each of the first/second memory cells includes a memory element formed in a cavity of the first/second control gate.”

292. Fukuzumi further states that “[e]ach of the memory cells M_{trmn} includes the columnar semiconductor CL_{mn} , the insulation layer surrounding the columnar semiconductor CL_{mn} via the space Ag_4 as shown in FIG. 2, a charge storage layer (not illustrated in FIGs. 2-3) and the word line WL surrounding the insulation layer and the charge storage layer.” EX1007, [0087]. Additionally, as examples of the insulation layer and charge storage layer surrounding columnar semiconductor CL_{mn} and surrounded by word line WL, Fukuzumi specifically describes that “surfaces of a block insulation layer 391a, a charge storage layer 391b and a tunnel insulation layer 391c faced to the fourth space Ag_4 .” EX1007, [0148].

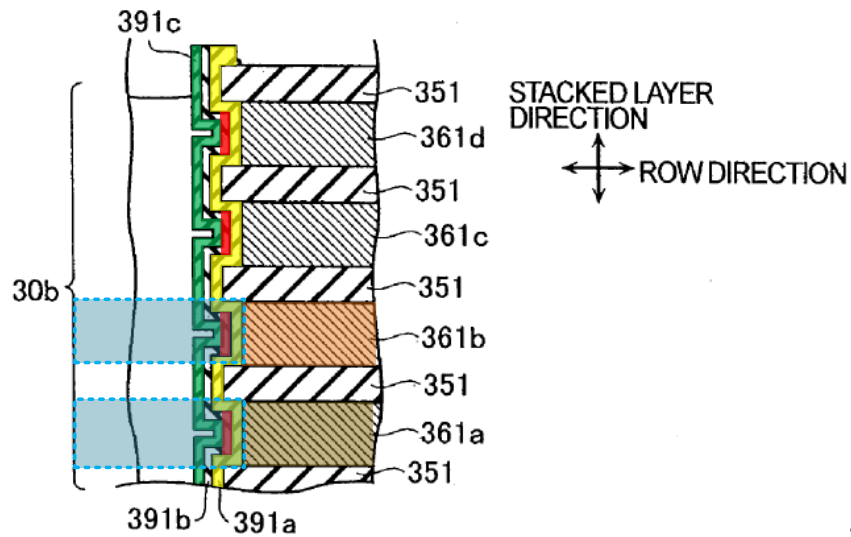


FIG. 28

FIG. AJ – FIG. 28 of Fukuzumi (annotated)

293. As illustrated in annotated FIG. 28 above (FIG. AJ of my Declaration with annotations), Fukuzumi discloses that block insulation layer 391a (in yellow) is formed on the sidewalls of memory hole 37 (in blue), while tunnel insulation layer 391c (in green) is formed on the sides of charge storage layers 391b (in red).

294. A POSITA would have understood, or at least found it obvious, that charge storage layer 391b (in red) is electrically isolated from the respective first or second word line conduction layer 361a or 361b (in brown and orange) by a respective portion of block insulation layer 391a (in yellow).

295. Based on my above analysis, it is my opinion that Fukuzumi discloses or otherwise renders obvious elements [21.c]-[21.f].

[21.g] a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric

296. Fukuzumi discloses that each memory string MS includes columnar semiconductor CL_{mn}, with the source and drain of memory string MS formed within columnar semiconductor CL_{mn}. EX1007, [0081], [0085], [0087]. Regarding memory 38, which is part of columnar semiconductor CL_{mn} in the first and second embodiments, Fukuzumi states that “when the fourth word line conduction layer 36d is applied to voltage, the memory 38 is performed to write in data into the approached portion of the charge storage layer 39b and read out data from the approached portion of the charge storage layer 39b.” EX1007, [0114].

297. Thus, A POSITA would have understood that, during certain operations of Fukuzumi’s memory device, a channel of memory string MS forms in the vertical outermost layer of columnar semiconductor CL_{mn} and does not extend throughout the entire columnar semiconductor CL_{mn}. Accordingly, Fukuzumi discloses the claimed “conductive channel.”

298. This understanding is well established in the art. For example, Sim discloses that “[a]pplication of the read voltage VREAD to the lower select line LSL causes vertical inversion regions 504B to be formed **along the outer walls** of lower portions of the vertical pillars PL formed of semiconducting material,” and “it can

be seen that an inversion layer I is created **along the walls, or outer surface**, of the vertical pillars PL when a suitable word line voltage is applied to the word line plates WL_PT.” EX1017, [0063], [0070], FIG. 11; see Section IX.B([21.g]).

299. Further, Fukuzumi discloses that columnar semiconductor CL_{mn} extends vertically through word lines, including first and second word lines WL in the first and second device levels. EX1007, [0081], FIG. 2. Thus, Fukuzumi discloses that columnar semiconductor CL_{mn} , including its vertical outermost layer, extends from the first device level to the second device level.

300. As illustrated in annotated FIG. 28 below (FIG. AK of my Declaration with annotations), a POSITA would have further understood, or at least found it obvious, that tunneling insulation layer 391c (in green) is formed laterally between charge storage layers 391b (in red) and the vertical outermost layer of columnar semiconductor CL_{mn} (in black), such that the vertical outermost layer of columnar semiconductor CL_{mn} faces charge storage layers 391b but is electrically isolated from charge storage layers 391b by tunneling insulation layer 391c (in green).

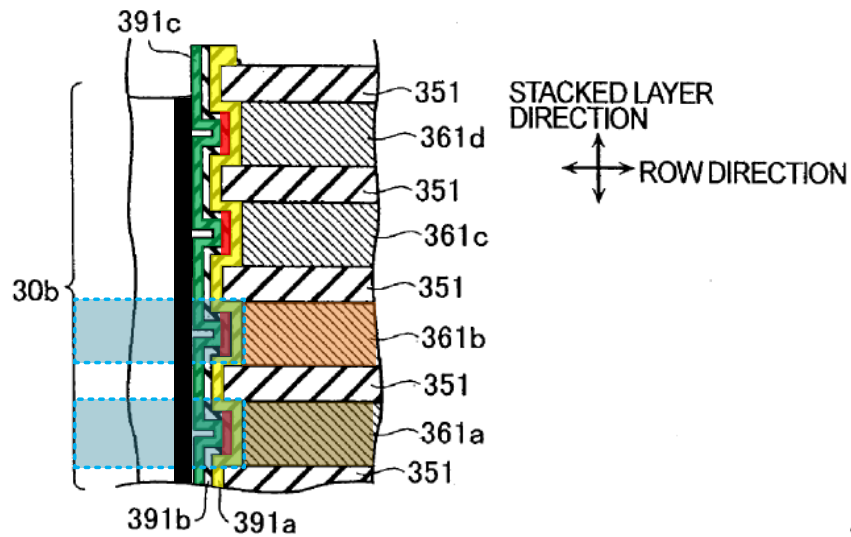


FIG. 28

FIG. AK – FIG. 28 of Fukuzumi (annotated)

301. Accordingly, it is my opinion that Fukuzumi discloses element [21.g].

[21.h] a substrate

302. Fukuzumi discloses a semiconductor substrate Ba, which corresponds to the claimed “substrate.” EX1007, [0081].

[21.i] a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate

303. As I discussed in Section XI.B([8.f.1]), a POSITA would have understood that the electrical connections between bit lines BL and columnar semiconductors CL_{mn} are controlled by selection transistors SDTr_{mn}/SSTr_{mn},

allowing each memory string MS to be selectively coupled or decoupled by turning selection transistors $SDTrmn/SSTrmn$ on or off through selection gate lines SGD/SGS.

304. Consequently, Fukuzumi discloses that bit line BL, which corresponds to the claimed “data line,” is configured to be “selectively” coupled to columnar semiconductor $CLmn$ including its vertical outermost layer that forms the conductive channel, which corresponds to the claimed “conductive channel.”

305. Further, as I discussed in Section XI.A, a POSITA would have found it obvious to modify Fukuzumi’s nonvolatile memory device as shown in FIG. 2 in view of Mokhlesi to incorporate a metal/silicide common source at the top and relocate the bit lines BL to the bottom of the device.

306. For example, as shown in FIG. AL of my Declaration below, in the modified nonvolatile memory device based on Fukuzumi’s structure in view of Mokhlesi, the repositioned bit line BL’ (in green), corresponding to the claimed “data line,” is located vertically between the second word line WL2 (in orange), corresponding to the claimed “second conductive material,” and the semiconductor substrate Ba (in gray). This modification, as understood by a POSITA, renders obvious the claimed relative position feature in element [21.i].

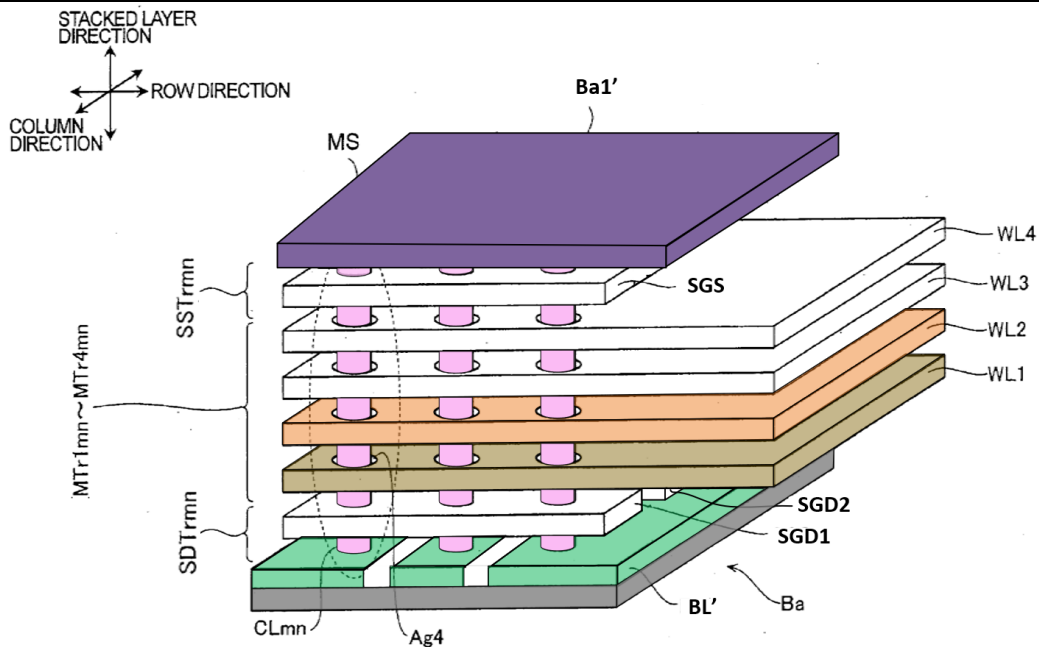


FIG. 2

FIG. AL – FIG. 2 of Fukuzumi (modified and annotated)

307. Therefore, Fukuzumi in view of Mokhlesi renders obvious element [21.i].

XII. Secondary Considerations

308. I have seen no evidence in the '214 patent's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any of the challenged claims. See generally EX1002. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the '214 patent were already well known. To the extent Patent Owner asserts the existence of any secondary considerations in its responses, I reserve my right to address any such evidence.

XIII. Additional Remarks

309. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

310. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

311. I have reviewed the accompanying Petition for *Inter Partes* Review of the '214 patent and, given the information set forth in this declaration, I agree with the reasoning and conclusions of the grounds of challenge in the petition. Based on my own analysis, I agree that: (1) Lung anticipates or otherwise renders obvious claims 8 and 21; (2) Park in view of Mokhlesi also renders obvious claims 8, 13, and 21; and (3) Fukuzumi in view of Mokhlesi further renders obvious claims 8 and 21.

* * *

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this proceeding.

Dated: 2/14/2025

By: Kelin Z. Kuhn
Dr. Kelin Kuhn
Winthrop, Washington

APPENDIX A

CURRICULUM VITAE
Dr. Kelin J. Kuhn

CONTACT INFORMATION:

Kelin J. Kuhn
P.O. Box 609
Winthrop, WA 98862
kjkuhn@confluence-tech.com

EDUCATION:

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980
(magna cum laude)

PRESENT ROLE:

**Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com);
present role**

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

**Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu)
2014 to date**

Position: Adjunct Professor
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:

Bayes PLLC: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *Inter Partes Review of U.S. Patent Nos. 8,803,214 And 10,475,737*.

Pillsbury Winthrop Shaw Pittman LLP: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

Ropes and Gray: Initiated 2023 and on-going. Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792*.

Heim, Payne & Chorush: Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc.* with regards to a dispute with *Taiwan Semiconductor Manufacturing Company*.

Smith Baluch LLP: Initiated 2022 and on-going. Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

Carter Arnett: Initiated 2022 and ongoing. Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S. 2 LLC*.

Mintz: Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

Heim, Payne & Chorush: Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

Quinn Emanuel Urquhart & Sullivan: Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

Ropes and Gray: Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Lawrence and Phillips: Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes reviews* (IPRs) filed by Samsung.

Wolf Greenfield: Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.* with regards to *inter partes reviews* (IPRs) filed by Micron.

Hueston Henningan: Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

Skadden Arps: Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

PARADIM: Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn

is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

Quinn Emanuel Urquhart & Sullivan: Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Susman Godfrey: Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

Womble Bond Dickinson: Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* (“EPR”) proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

Womble Bond Dickinson: Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al.* Dr. Kuhn supported this litigation for the plaintiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

Lathrop Gage: Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

Ropes & Gray: Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

GlaserWeil: Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314*. Dr. Kuhn supported this litigation for the plaintiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

yoR Labs Inc.: Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

Oregon State University, Department of Electrical Engineering and Computer Science: Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn’s role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

FORMER ROLES (2014 and PRIOR)

Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)

Grade level: 12 (Fellow)

Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59, No: 7, 2012, pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008

Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)

Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

Intel, Portland, OR, (90nm communication process manager) 2001-2004+

Grade level: 9/10 (Sr. Engineer / Principal engineer)

Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

Other Intel experience:

Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001

Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998

Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

Other relevant experience:

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Professor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

Highlights include:

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

BOOKS

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

BOOK CHAPTERS

“The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

AWARDS:

Elected to the National Academy of Engineering (2023)
IEEE Frederik Philips Award (2016)
IEEE Paul Rappaport Award (2013)
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)

Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)

Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996

University of Washington, Distinguished Teaching Award, 1995

College of Engineering, Outstanding Faculty Achievement Award, 1994

NSF Presidential Young Investigator award, 1991-6

NSF Research Initiation Award, 1989-91

IBM Graduate Fellowship, 1983-5

Hertz Graduate Fellowship, 1982-3

National Merit Scholar, 1976-80

JOURNAL PUBLICATIONS:

49. "First principles modeling of defects in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, J. Appl. Phys., Vol. 121, No. 7, Jan. 2017.

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46. "Adhesion Limits and Design Criteria for Nanorelays", Kevin L. Lin, Graham L. W. Cross, Peter Gleeson, Johann P. de Silva, Alejandro Levander, Jorge A. Muñoz, Chytra Pawashe, Alexis Potie, Patrick Theofanis, John J. Boland, and Dr. Kuhn J. Kuhn, IEEE Trans. on Elec. Dev., Vol. 63, No. 1, Jan. 2016, 465-470.

45. Distributive Quasi-Ballistic Drift Diffusion Model Including Effects of Stress and High Driving Field, Roza Kotlyar,, Rafael Rios, Cory E. Weber, Thomas D. Linton, Mark Armstrong and Dr. Kuhn Kuhn, IEEE Trans. on Elec. Dev., Vol. 62, No. 3, March 2015. Pp. 743-750.

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43. Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions, Monaghan, S. O'Connor, E., Rios, R., Ferdousi, F., Floyd, L., Ryan, E., Cherhaoui, K., Povey, I.M., Kuhn, K.J., Hurley, P.K. IEEE Transactions on Electron Devices, Vol. 61, No. 12, pp. 4176-85, Dec. 2014.

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41. Scaling Limits of Electrostatic Nanorelays, Pawashe, C., Lin, K., Kuhn, K.J., IEEE Transactions on Electron Devices, Vol. 60, No. 9, pp. 2936-42, Sept. 2013,
40. Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors, Kotlyar, R.; Avci, U.E.; Cea, S.; Rios, R.; Linton, T.D.; Kuhn, K.J.; Young, I.A., Applied Physics Letters, v 102, n 11, March 18, 2013.
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38. Considerations for Ultimate CMOS Scaling, Dr. Kuhn J. Kuhn, invited review paper, IEEE Trans. on Elec. Dev., Vol: 59 , No: 7, 2012 , pp. 1813 – 1828 (won the Paul Rappaport Award)
37. Does the low hole transport mass in <110> and <111> Si nanowires lead to mobility enhancements at high field and stress: a self-consistent tight-binding study, R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, Michael Povolotskyi, Tillmann Kubis, and Gerhard Klimeck, Vol: 111 , No: 12, 2012, pp 123718 - 123718-11
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27. Elevated temperature performance of pseudomorphic AlGaAs/InGaAs MODFETs. Zurek, S.J.; Darling, R.B.; Kuhn, K.J.; Foisy, M.C. IEEE Transactions on Electron Devices, vol.45, no.1, Jan. 1998. p. 2-8
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CONFERENCE PUBLICATIONS

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51. Understanding the feasibility of scaled III-V TFET for logic by bridging atomistic simulations and experimental results, Avci, U.E. ; Hasan, S. ; Nikonov, D.E. ; Rios, R. ; Kuhn, K. ; Young, I.A., Symposium on VLSI Technology (VLSIT), 2012, pp: 183 – 184.
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49. Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation, K. Kuhn, INFOS 2011 (June 22, 2011, France)
48. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET, Avci, U.E.; Rios, R.; Kuhn, K.J.; Young, I.A., IEEE Conference on Nanotechnology (IEEE-NANO), 2011 11th, pp. 869 – 872
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46. CMOS scaling for the 22nm node and beyond: Device physics and technology, Kuhn, K.J., 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2011 , pp. 1 – 2
45. Past, Present and Future: SiGe and CMOS Transistor Scaling. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, ECS 2010, Oct. 10, Las Vegas, CA, USA.
44. Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, K. J. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.
43. CMOS transistor scaling past 32nm and implications on variation, K. Kuhn, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA, pp. 241-246.
42. Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, K. Kuhn, Nikkei Electronics Symposium, June 29th, 2010.
41. Technology options for 22nm and beyond, K. Kuhn, Technology, Kuhn, K.J.; Liu, M.Y.; Kennel, H.; 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.
40. CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California
39. Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.
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PATENTS

	PAT. NO.	Title
1	11,302,777	Integration methods to fabricate internal spacers for nanowire devices
2	11,195,919	Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer
3	11,139,400	Non-planar semiconductor device having hybrid geometry-based active region
4	11,024,714	Nanowire transistor fabrication with hardmask layers
5	10,991,799	Silicon and silicon germanium nanowire structures
6	10,825,752	Integrated thermoelectric cooling
7	10,804,357	Integration methods to fabricate internal spacers for nanowire devices
8	10,636,871	Silicon and silicon germanium nanowire structures
9	10,593,804	Non-planar semiconductor device having hybrid geometry-based active region
10	10,586,868	Non-planar semiconductor device having hybrid geometry-based active region
11	10,580,899	Nanowire structures having non-discrete source and drain regions
12	10,580,860	Integration methods to fabricate internal spacers for nanowire devices
13	10,535,770	Scaled TFET transistor formed using nanowire with surface termination
14	10,424,580	Semiconductor devices having modulated nanowire counts
15	10,283,589	Integration methods to fabricate internal spacers for nanowire devices
16	10,121,861	Nanowire transistor fabrication with hardmask layers
17	10,121,856	Integration methods to fabricate internal spacers for nanowire devices
18	10,115,822	Methods of forming low band gap source and drain structures in microelectronic devices
19	10,109,711	CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel
20	10,074,573	CMOS nanowire structure
21	10,074,357	Integrated acoustic phase array
22	10,026,829	Semiconductor device with isolated body portion
23	9,978,636	Isolated and bulk semiconductor devices formed on a same bulk substrate
24	9,947,805	Nanowire-based mechanical switching device
25	9,935,205	Internal spacers for nanowire transistors and method of fabrication thereof
26	9,935,107	CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same
27	9,926,193	Magnetic nanomechanical devices for stiction compensation

28	9,911,835	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
29	9,893,167	Integration methods to fabricate internal spacers for nanowire devices
30	9,882,053	Molded dielectric fin-based nanostructure
31	9,859,368	Integration methods to fabricate internal spacers for nanowire devices
32	9,825,130	Leakage reduction structures for nanowire transistors
33	9,812,524	Nanowire transistor devices and forming techniques
34	9,691,843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
35	9,680,013	Non-planar device having uniaxially strained semiconductor body and method of making same
36	9,673,302	Conversion of strain-inducing buffer to electrical insulator
37	9,614,060	Nanowire transistor with underlayer etch stops
38	9,608,059	Semiconductor device with isolated body portion
39	9,595,581	Silicon and silicon germanium nanowire structures
40	9,583,602	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
41	9,583,491	CMOS nanowire structure
42	9,564,522	Nanowire structures having non-discrete source and drain regions
43	9,559,160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
44	9,508,796	Internal spacers for nanowire transistors and method of fabrication thereof
45	9,484,447	Integration methods to fabricate internal spacers for nanowire devices
46	9,472,613	Conversion of strain-inducing buffer to electrical insulator
47	9,425,212	Isolated and bulk semiconductor devices formed on a same bulk substrate
48	9,412,872	N-type and P-type tunneling field effect transistors (TFETs)
49	9,385,221	Nanowire transistor with underlayer etch stops
50	9,362,074	Nanowire-based mechanical switching device
51	9,355,242	Method and apparatus for managing and accessing personal data
52	9,343,559	Nanowire transistor devices and forming techniques
53	9,287,576	Self-powered internal medical device
54	9,258,114	Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)
55	9,224,810	CMOS nanowire structure
56	9,183,829	Integrated acoustic phase array

57	9,129,829	Silicon and silicon germanium nanowire structures
58	9,129,827	Conversion of strain-inducing buffer to electrical insulator
59	9,105,344	Shut-off mechanism in an integrated circuit device
60	9,087,863	Nanowire structures having non-discrete source and drain regions
61	9,064,944	Nanowire transistor with underlayer etch stops
62	9,029,221	Semiconductor devices having three-dimensional bodies with modulated heights
63	9,012,284	Nanowire transistor devices and forming techniques
64	8,890,120	Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs
65	8,853,741	Junctionless accumulation-mode devices on decoupled prominent architectures
66	8,766,372	Copper-filled trench contact for transistor performance improvement
67	8,753,942	Silicon and silicon germanium nanowire structures
68	8,558,279	Non-planar device having uniaxially strained semiconductor body and method of making same
69	8,507,948	Junctionless accumulation-mode devices on prominent architectures, and methods of making same
70	8,487,348	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
71	8,269,283	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
72	8,258,057	Copper-filled trench contact for transistor performance improvement
73	7,999,607	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
74	7,888,710	CMOS fabrication process utilizing special transistor orientation
75	7,737,770	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
76	7,312,485	CMOS fabrication process utilizing special transistor orientation
77	6,627,506	Thin tensile layers in shallow trench isolation and method of making same
78	6,368,931	Thin tensile layers in shallow trench isolation and method of making same
79	4,617,669	Method and apparatus for pumping laser slabs
80	4,563,763	Method and apparatus for cooling a slab laser

INVITED TECHNICAL PRESENTATIONS/SEMINARS :

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures ...and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17th, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California

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Invited – International Electron Device meeting – short course.
http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf

Invited seminar - "45nm High-k + Metal Gate Logic Technology," K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.