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| APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/900,188 | 11/12/2019 | 10475737 | MI22-6502 | 1775 |

128753 7590 10/23/2019

Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

# ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Sanh D. Tang, Boise, ID;
Micron Technology, Inc., Boise, ID;
Roger W. Lindsay, Boise, ID;
Krishna K. Parat, Palo Alto, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
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# "FEE ADDRESS" INDICATION FORM

**Address to:**
**Mail Stop M Correspondence**
**Commissioner for Patents**
**P.O. Box 1450**
**Alexandria, VA 22313-1450**

**- OR -**

**Fax to:**
**571-273-6500**

**INSTRUCTIONS:** The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 26809

*OR*

☐ The attached Request for Customer Number (PTO/SB/125) form.

| PATENT NUMBER (if known) | APPLICATION NUMBER |
|---|---|
| | 15/900,188 |

Completed by (check one):

☐ Applicant/Inventor

/Mark S. Matkin/
Signature

☑ Attorney or Agent of record 32,268 (Reg. No.)

Mark S. Matkin
Typed or printed name

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

(509) 624-4276
Requester's telephone number

☐ Assignee recorded at Reel _____ Frame_____

October 8, 2019
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ * Total of _____forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
**SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

## Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

| Electronic Patent Application Fee Transmittal | | | | | |
|---|---|---|---|---|---|
| **Application Number:** | 15900188 | | | | |
| **Filing Date:** | 20-Feb-2018 | | | | |
| **Title of Invention:** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | | | | |
| **First Named Inventor/Applicant Name:** | Sanh D. Tang | | | | |
| **Filer:** | Mark S. Matkin/Bridget Wiseman | | | | |
| **Attorney Docket Number:** | MI22-6502 | | | | |
| Filed as Large Entity | | | | | |
| **Filing Fees for Utility under 35 USC 111(a)** | | | | | |
| **Description** | | **Fee Code** | **Quantity** | **Amount** | **Sub-Total in USD($)** |
| **Basic Filing:** | | | | | |
| **Pages:** | | | | | |
| **Claims:** | | | | | |
| **Miscellaneous-Filing:** | | | | | |
| **Petition:** | | | | | |
| **Patent-Appeals-and-Interference:** | | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | | |
| UTILITY APPL ISSUE FEE | | 1501 | 1 | 1000 | 1000 |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Extension-of-Time:** | | | | |
| **Miscellaneous:** | | | | |
| | | | **Total in USD ($)** | **1000** |

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 37399681 |
| **Application Number:** | 15900188 |
| **International Application Number:** | |
| **Confirmation Number:** | 1775 |
| **Title of Invention:** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells |
| **First Named Inventor/Applicant Name:** | Sanh D. Tang |
| **Customer Number:** | 128753 |
| **Filer:** | Mark S. Matkin/Bridget Wiseman |
| **Filer Authorized By:** | Mark S. Matkin |
| **Attorney Docket Number:** | MI22-6502 |
| **Receipt Date:** | 08-OCT-2019 |
| **Filing Date:** | 20-FEB-2018 |
| **Time Stamp:** | 16:53:21 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
|---|---|
| Submitted with Payment | yes |
| Payment Type | CARD |
| Payment was successfully received in RAM | $1000 |
| RAM confirmation Number | E201908G53577560 |
| Deposit Account | 230925 |
| Authorized User | Bridget Wiseman |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:<br>37 CFR 1.16 (National application filing, search, and examination fees)<br>37 CFR 1.17 (Patent application and reexamination processing fees) | |

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | Issue Fee Payment (PTO-85B) | 6502_Fee_Transmittal.pdf | 329982<br>63e584954a268d891ad4eb7c3b5805ce6ab0773d | no | 1 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Miscellaneous Incoming Letter | 6502_Fee_Address.pdf | 120299<br>b9aae4379d0a1b71acea60b0a69eda2d82435cdd | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 3 | Fee Worksheet (SB06) | fee-info.pdf | 30703<br>0c367ea789fae55ea56b9830f2cc091adb71156b | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 480984 | | |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

## PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

128753 7590 07/09/2019

Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)

(Signature)

(Date)

| APPLICATION NO | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/900,188 | 02/20/2018 | Sanh D. Tang | MI22-6502 | 1775 |

TITLE OF INVENTION: Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1000 | $0.00 | $0.00 | $1000 | 10/09/2019 |

| EXAMINER | ART UNIT | CLASS-SUBCLASS |
|---|---|---|
| NGUYEN, CUONG QUANG | 2811 | 438-216000 |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47, Rev 03-09 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Wells St. John P.S.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Micron Technology, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Boise, ID

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 230925

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Mark S. Matkin/ Date October 8, 2019

Typed or printed name Mark S. Matkin Registration No. 32,268



PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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www.uspto.gov

# NOTICE OF ALLOWANCE AND FEE(S) DUE

128753 7590 07/09/2019

Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

| EXAMINER | |
|---|---|
| NGUYEN, CUONG QUANG | |
| ART UNIT | PAPER NUMBER |
| 2811 | |

DATE MAILED: 07/09/2019

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/900,188 | 02/20/2018 | Sanh D. Tang | MI22-6502 | 1775 |

TITLE OF INVENTION: Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

| APPLN. TYPE | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE |
|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1000 | $0.00 | $0.00 | $1000 | 10/09/2019 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

**HOW TO REPLY TO THIS NOTICE:**

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.**



PTOL-85 (Rev. 02/11)

## PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

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**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

| (Typed or printed name) |
|---|
| (Signature) |
| (Date) |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
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|---|---|---|---|---|---|---|
| nonprovisional | UNDISCOUNTED | $1000 | $0.00 | $0.00 | $1000 | 10/09/2019 |

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|---|---|---|
| NGUYEN, CUONG QUANG | 2811 | 438-216000 |

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❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

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❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

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NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



**YMTC EXHIBIT 1002**
**Page 10 of 186**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/900,188 | 02/20/2018 | Sanh D. Tang | MI22-6502 | 1775 |

128753 7590 07/09/2019

Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

| EXAMINER | |
|---|---|
| NGUYEN, CUONG QUANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |

DATE MAILED: 07/09/2019

**Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)**
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.



PTOL-85 (Rev. 02/11)

## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

## Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

| *Notice of Allowability* | **Application No.** 15/900,188 | **Applicant(s)** Tang et al. | |
|---|---|---|---|
| | **Examiner** CUONG Q NGUYEN | **Art Unit** 2811 | **AIA (FITF) Status** No |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 04/18/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 39-40 and 42-61 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   **Certified copies:**

   a) ☐ All  b) ☐ Some  *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CUONG Q NGUYEN/
Primary Examiner, Art Unit 2811

| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15/900,188 | Tang et al. |
| | Examiner | Art Unit |
| | CUONG Q NGUYEN | 2811 |

| CPC - Searched* | | |
|---|---|---|
| Symbol | Date | Examiner |
| H01L27/10, 101, 11556, 1157, 11582, 249, 29/66825, 788 | 04/13/2019 | CN |
| Updated search | 07/05/2019 | CN |

| CPC Combination Sets - Searched* | | |
|---|---|---|
| Symbol | Date | Examiner |
| | | |

| US Classification - Searched* | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| | | | |

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

| Search Notes | | |
|---|---|---|
| Search Notes | Date | Examiner |
| EAST, EPO, JPO, DERWENT, IBM, inventor name | 04/13/2019 | CN |
| Updated search | 07/05/2019 | CN |

| Interference Search | | | |
|---|---|---|---|
| US Class/CPC Symbol | US Subclass/CPC Group | Date | Examiner |
| See search note | | 07/05/2019 | CN |



YMTC EXHIBIT 1002
Page 14 of 186

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15/900,188 | Tang et al. |
| | **Examiner** | **Art Unit** |
| | CUONG Q NGUYEN | 2811 |

| CPC | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | | | | | | | | **Type** | **Version** |
| H01L | / | 23 | / | 52 | | | | F | 2013-01-01 |
| H01L | / | 27 | / | 101 | | | | I | 2013-01-01 |
| H01L | / | 27 | / | 10 | | | | I | 2013-01-01 |
| G11C | / | 13 | / | 0007 | | | | I | 2013-01-01 |
| H01L | / | 23 | / | 528 | | | | I | 2013-01-01 |
| H01L | / | 27 | / | 11556 | | | | I | 2013-01-01 |
| H01L | / | 27 | / | 11582 | | | | I | 2013-01-01 |
| H01L | / | 27 | / | 249 | | | | I | 2013-01-01 |
| H01L | / | 45 | / | 142 | | | | I | 2013-01-01 |
| H01L | / | 45 | / | 143 | | | | I | 2013-01-01 |
| H01L | / | 45 | / | 144 | | | | I | 2013-01-01 |
| H01L | / | 45 | / | 146 | | | | I | 2013-01-01 |
| H01L | / | 45 | / | 147 | | | | I | 2013-01-01 |
| H01L | / | 27 | / | 1157 | | | | I | 2013-01-01 |
| H01L | / | 2924 | / | 0002 | | | | A | 2013-01-01 |
| G11C | / | 2213 | / | 11 | | | | A | 2013-01-01 |
| G11C | / | 2213 | / | 31 | | | | A | 2013-01-01 |
| G11C | / | 2213 | / | 32 | | | | A | 2013-01-01 |
| G11C | / | 2213 | / | 71 | | | | A | 2013-01-01 |
| G11C | / | 2213 | / | 75 | | | | A | 2013-01-01 |
| H01L | / | 27 | / | 11524 | | | | A | 2013-01-01 |
| H01L | / | 45 | / | 141 | | | | A | 2013-01-01 |
| H01L | / | 45 | / | 145 | | | | A | 2013-01-01 |

| CPC Combination Sets | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | | | | | | | **Type** | **Set** | **Ranking** | **Version** |
| H01L | / | 2924 | / | 0002 | | | A | 1 | 1 | 2013-01-01 |
| H01L | / | 2924 | / | 00 | | | A | 1 | 2 | 2013-01-01 |

| NONE | | **Total Claims Allowed:** | |
|---|---|---|---|
| (Assistant Examiner) | (Date) | 22 | |
| /CUONG Q NGUYEN/<br>Primary Examiner, Art Unit 2811 | 05 July 2019 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 39 | 7 |

U.S. Patent and Trademark Office — Part of Paper No.: 20190705



YMTC EXHIBIT 1002
Page 15 of 186

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15/900,188 | Tang et al. |
| | Examiner | Art Unit |
| | CUONG Q NGUYEN | 2811 |

| INTERNATIONAL CLASSIFICATION | | | | |
|---|---|---|---|---|
| CLAIMED | | | | |
| H01L | / | 27 | / | 1157 |

| NON-CLAIMED | | | | |
|---|---|---|---|---|
| | / | | / | |

| US ORIGINAL CLASSIFICATION | |
|---|---|
| CLASS | SUBCLASS |
| | |

| CROSS REFERENCES(S) | | | | | | |
|---|---|---|---|---|---|---|
| CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) | | | | | |
| | | | | | | |

| NONE | | Total Claims Allowed: | |
|---|---|---|---|
| (Assistant Examiner) | (Date) | 22 | |
| /CUONG Q NGUYEN/<br>Primary Examiner, Art Unit 2811 | 05 July 2019 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 39 | 7 |

U.S. Patent and Trademark Office — Part of Paper No.: 20190705

| Issue Classification | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15/900,188 | Tang et al. |
| | Examiner | Art Unit |
| | CUONG Q NGUYEN | 2811 |

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

| Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
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| | | | | | | | | | | | | | | | |

| NONE | | Total Claims Allowed: | |
|---|---|---|---|
| (Assistant Examiner) | (Date) | 22 | |
| /CUONG Q NGUYEN/<br>Primary Examiner, Art Unit 2811 | 05 July 2019 | O.G. Print Claim(s) | O.G. Print Figure |
| (Primary Examiner) | (Date) | 39 | 7 |

U.S. Patent and Trademark Office — Part of Paper No.: 20190705

**EAST Search History**

**EAST Search History (Interference)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 0 | ((conductive adj transistor adj gate adj line) and (primary adj portion) and (operation adj structure) and (end adj portion) and (dummy adj structure) and (vertically adj2 transistor)).clm. | US-PGPUB; USPAT | OR | ON | 2019/07/05 11:53 |

**7/5/2019 11:53:49 AM**

**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 0 | (vetical$5 near5 (transistor or gate)) and semiconductor and dummy and memory and (@pd<="20110412" or @ad<="20110412" or @rlad<="20110412") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2019/07/05 10:22 |
| L2 | 2311 | (vertical$5 near5 (transistor or gate)) and semiconductor and dummy and memory and (@pd<="20110412" or @ad<="20110412" or @rlad<="20110412") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2019/07/05 10:24 |
| L3 | 2079 | (vertical$5 near5 (transistor or gate)) and semiconductor and (h01l27/101.cpc. or h01l27/11556.cpc. or h01l27/1157.cpc. or h01l27/11582.cpc. or h01l27/249.cpc. or h01l29/66825.cpc. or h01l29/788.cpc.) and memory and (@pd<="20110412" or @ad<="20110412" or @rlad<="20110412") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2019/07/05 10:34 |
| L4 | 2273 | (vertical$5 near5 (transistor or gate)) and semiconductor and (micron adj technology) and memory and (@pd<="20110412" or @ad<="20110412" or @rlad<="20110412") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2019/07/05 10:42 |

**7/5/2019 10:51:54 AM**

| *Application Number* * 15/900,188 * | Application/Control No. 15/900,188 | Applicant(s)/Patent under Reexamination Tang et al. | |
|---|---|---|---|
| | Examiner NGUYEN, CUONG QUANG | Art Unit 2811 | |

| Document Code - DISQ | Internal Document - DO NOT MAIL |
|---|---|

| TERMINAL DISCLAIMER | ☑ APPROVED | ☐ DISAPPROVED |
|---|---|---|
| Date Filed: 18 April 2019 | This patent is subject to a Terminal Disclaimer | |

| Approved/Disapproved by: |
|---|
| /CRYSTAL QUEEN/<br>**Technology Center: PLRC**<br>**Telephone:** |

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>15/900,188 | Filing Date<br>02/20/2018 | ☐ To be Mailed |
|---|---|---|---|

**ENTITY:** ☑ LARGE ☐ SMALL ☐ MICRO

## APPLICATION AS FILED - PART I

| FOR | (Column 1)<br>NUMBER FILED | (Column 2)<br>NUMBER EXTRA | | RATE ($) | FEE ($) |
|---|---|---|---|---|---|
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | | x $100 = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | | x $460 = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | | TOTAL | |

## APPLICATION AS AMENDED - PART II

| AMENDMENT | 04/18/2019 | (Column 1)<br>CLAIMS REMAINING AFTER AMENDMENT | | (Column 2)<br>HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3)<br>PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * 22 | Minus | ** 22 | = 0 | | x $100 = | 0 |
| | Independent (37 CFR 1.16(h)) | * 5 | Minus | *** 5 | = 0 | | x $460 = | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | 0 |

| AMENDMENT | | (Column 1)<br>CLAIMS REMAINING AFTER AMENDMENT | | (Column 2)<br>HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3)<br>PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | | x $0 = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | | x $0 = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | |

| | |
|---|---|
| * If the entry in column 1 is less than the entry in column 2, write "0" in column 3. | LIE |
| ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". | /TERESA J JACKSON WOODRUFF/ |
| *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". | |
| The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1. | |

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

PTO/AIA/26 (04-14)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT | Docket Number (Optional) MI22-6502 |
|---|---|

In re Application of: Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat, Inventors

Application No.: 15/900,188

Filed: February 20, 2018

For: Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

The applicant, Micron Technology, Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9,929,175 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 32,268

/Mark S. Matkin/ — Signature
April 18, 2019 — Date

Mark S. Matkin — Typed or printed name

Patent Practitioner — Title
509-624-4276 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

This collection of information is required by 37 CFR 1.321. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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| Electronic Patent Application Fee Transmittal | | | | | |
|---|---|---|---|---|---|
| **Application Number:** | 15900188 | | | | |
| **Filing Date:** | 20-Feb-2018 | | | | |
| **Title of Invention:** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | | | | |
| **First Named Inventor/Applicant Name:** | Sanh D. Tang | | | | |
| **Filer:** | Mark S. Matkin/Bridget Wiseman | | | | |
| **Attorney Docket Number:** | MI22-6502 | | | | |
| Filed as Large Entity | | | | | |
| **Filing Fees for Utility under 35 USC 111(a)** | | | | | |
| **Description** | | **Fee Code** | **Quantity** | **Amount** | **Sub-Total in USD($)** |
| **Basic Filing:** | | | | | |
| **Pages:** | | | | | |
| **Claims:** | | | | | |
| **Miscellaneous-Filing:** | | | | | |
| **Petition:** | | | | | |
| **Patent-Appeals-and-Interference:** | | | | | |
| **Post-Allowance-and-Post-Issuance:** | | | | | |
| **Extension-of-Time:** | | | | | |

| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
|---|---|---|---|---|
| **Miscellaneous:** | | | | |
| STATUTORY OR TERMINAL DISCLAIMER | 1814 | 1 | 160 | 160 |
| | | **Total in USD ($)** | | **160** |

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 35769045 |
| **Application Number:** | 15900188 |
| **International Application Number:** | |
| **Confirmation Number:** | 1775 |
| **Title of Invention:** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells |
| **First Named Inventor/Applicant Name:** | Sanh D. Tang |
| **Customer Number:** | 128753 |
| **Filer:** | Mark S. Matkin/Bridget Wiseman |
| **Filer Authorized By:** | Mark S. Matkin |
| **Attorney Docket Number:** | MI22-6502 |
| **Receipt Date:** | 18-APR-2019 |
| **Filing Date:** | 20-FEB-2018 |
| **Time Stamp:** | 16:14:48 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| | |
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| Submitted with Payment | yes |
| Payment Type | CARD |
| Payment was successfully received in RAM | $160 |
| RAM confirmation Number | 041919INTEFSW16152200 |
| Deposit Account | 230925 |
| Authorized User | Bridget Wiseman |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:<br>37 CFR 1.16 (National application filing, search, and examination fees)<br>37 CFR 1.17 (Patent application and reexamination processing fees) | |

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | | 6502_M03.pdf | 30650<br>342b4b3f97c6235e43025b8fbe0a54be4199dbf3 | yes | 7 |
| | **Multipart Description/PDF files in .zip description** | | | | |
| | **Document Description** | | **Start** | **End** | |
| | Amendment/Req. Reconsideration-After Non-Final Reject | | 1 | 1 | |
| | Claims | | 2 | 6 | |
| | Applicant Arguments/Remarks Made in an Amendment | | 7 | 7 | |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | Terminal Disclaimer Filed | 6502_Terminal_Disclaimer.pdf | 105211<br>7244f3b5c87e46bf6ab53c1b154dfb049e9d250f | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 3 | Fee Worksheet (SB06) | fee-info.pdf | 30978<br>d9e5c93a09f64f69541bc0b93534be8fd0767d8d | no | 2 |
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| | | **Total Files Size (in bytes):** | 166839 | | |

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**New Applications Under 35 U.S.C. 111**

**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .....15/900,188
Filing Date .....February 20, 2018
Confirmation No. ..... 1775
Inventor.....Sanh D. Tang
Assignee .....Micron Technology, Inc.
Group Art Unit ..... 2811
Examiner .....Cuong Quang Nguyen
Attorney's Docket No. ..... MI22-6502
Title:....Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

**RESPONSE TO THE OFFICE ACTION MAILED APRIL 15, 2019**

To: Mail Stop Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. Main Avenue, Suite 600
Spokane, WA 99201-0613

**AMENDMENTS**

Responsive to the Office Action dated April 15, 2019, Applicant amends and remarks as follows:

**Amendments To The Claims:**

Claims 1-38 (Cancelled).

39. (Previously Presented): Integrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines, the integrated circuitry comprising:

a primary portion and an end portion, at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the gate lines in the primary portion, the operative structures comprising semiconductive material, the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines; and

dummy structures extending vertically through the gate lines in the end portion.

40. (Previously Presented): The stack of claim 39 further comprising contacts in the end portion that individual extend to the individual gate lines.

Claim 41 (Cancelled).

42. (Previously Presented): The integrated circuitry of claim 39 wherein the vertically oriented transistors are charge storage transistors of individual memory cells.

43. (Previously Presented): The integrated circuitry of claim 42 wherein the memory cells comprise a portion of NAND architecture.

44. (Previously Presented): The integrated circuitry of claim 39 wherein the operative and dummy structures comprise the same material.

45. (Previously Presented): The integrated circuitry of claim 44 wherein the operative and dummy structures comprise a plurality of the same materials.

46. (Previously Presented): The integrated circuitry of claim 45 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

47. (Previously Presented): The integrated circuitry of claim 44 wherein the operative and dummy structures consist essentially of the same material.

48. (Previously Presented): The integrated circuitry of claim 39 wherein the dummy structures comprise semiconductor material.

49. (Previously Presented): The integrated circuitry of claim 39 wherein the dummy structures comprise the semiconductive material.

50. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion, the dummy structures individually comprising a cylinder of semiconductive material.

51. (Previously Presented): The stack of claim 50 comprising solid material filling radially internal regions of individual of the cylinders of semiconductive material.

52. (Previously Presented): The stack of claim 50 wherein individual of the cylinders of semiconductive material define a radially-outermost horizontal periphery of individual of the dummy structures.

53. (Previously Presented): The stack of claim 50 wherein the operative structures individually comprise a cylinder of semiconductor material.

54. (Previously Presented): The stack of claim 50 further comprising vertical contacts in the end portion connecting with conductive material of individual of the features.

55. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string; and

dummy structures extending vertically through the features in the end portion, some of the dummy structures horizontally overlapping the primary portion and the end portion.

56. (Previously Presented): The stack of claim 55 wherein the dummy structures comprise a cylinder of semiconductive material.

57. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion; and

vertical contacts in the end portion connecting with individual of the control gate lines, the contacts and dummy structures having different horizontal cross-sections relative one another.

58. (Previously Presented): The stack of claim 57 wherein the different horizontal cross-sections are of the same shape and of different sizes relative one another.

59. (Previously Presented): The stack of claim 57 wherein the different horizontal cross-sections have different values of total horizontal area relative one another.



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60. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, the at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion, some of the dummy structures being longitudinally spaced alone a horizontal line; and

vertical contacts in the end portion connecting with individual of the control gate lines, at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line.

61. (Previously Presented): The stack of claim 60 wherein the horizontal line is linearly straight.

## REMARKS

Claims 39, 40, and 42-61 remain the claims in the application for consideration.

A Terminal Disclaimer is filed herewith as respects U.S. Patent No. 9,929,175, thereby obviating the Examiner's obviousness-type double patenting rejection. Therefore, each of Applicant's claims 39, 40, and 42-61 should be formally allowed, and action to that end is requested.

This application is believed to be in immediate condition for allowance, and action to that end is requested.

Respectfully submitted,

Dated: April 18, 2019

By: /Mark S. Matkin/
Mark S. Matkin
Reg. No. 32,268

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/900,188 | 02/20/2018 | Sanh D. Tang | MI22-6502 | 1775 |

128753 7590 04/15/2019

Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

| EXAMINER | |
|---|---|
| NGUYEN, CUONG QUANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |
| **MAIL DATE** | **DELIVERY MODE** |
| 04/15/2019 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| *Office Action Summary* | **Application No.** 15/900,188 | **Applicant(s)** Tang et al. | |
|---|---|---|---|
| | **Examiner** CUONG Q NGUYEN | **Art Unit** 2811 | **AIA (FITF) Status** No |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☑ Responsive to communication(s) filed on 01/22/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims***

5) ☑ Claim(s) 39-40 and 42-61 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☑ Claim(s) 57-61 is/are allowed.

7) ☑ Claim(s) 39-40 and 42-56 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

**Application Papers**

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 01/22/2019, 02/20/2018.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.



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***Notice of Pre-AIA or AIA Status***

1. The present application is being examined under the pre-AIA first to invent provisions.

**DETAILED ACTION**

## Election/Restriction

2. Applicant's election without traverse of Group I (device claims), claims 39-40 and 42-61 is acknowledged.

***Double Patenting***

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 39, 40, 42-50, 52-56 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 10 of U.S. Patent No. US 9,929,175. Although the claims at issue are not identical, they are not patentably distinct from each other because the following reasons:

Regarding claim 39 of the present invention:

39. Integrated circuitry comprising (1) a stack of horizontally extending and vertically overlapping conductive transistor gate lines, the integrated circuitry comprising: (2) a primary portion and (3) an end portion, (4) at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion; (5) operative structures extending vertically through the gate lines in the primary portion, (6) the operative structures comprising semiconductive material, the semiconductive material of the operative structures comprising (7) interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines; and (8) dummy structures extending vertically through the gate lines in the end portion.

Claim 10 0f US 9,929,175:

10. A memory array comprising (1) a stack of memory cells of NAND architecture (which including gate lines extending horizontally and vertically overlapping (stack of memory cells with vertically oriented transistors)): a substrate comprising (2) a primary portion and (3) an end portion; (5) a plurality of NAND strings of vertically oriented transistors (operation structure) in the primary portion; (6, 7) the transistors (operation structure) individually comprising a channel comprising a hollow cylinder of semiconductive material, a tunnel dielectric laterally outward of the channel, a charge trapping material laterally outward of the tunnel dielectric, a dielectric material laterally outward of the charge trapping material, and a control gate laterally outward of the dielectric material; the control gate comprising a portion of one of a plurality of horizontally extending control gate lines, (4) the control gate lines extending horizontally farther in the end portion moving deeper into the stack in the end portion, another

dielectric elevationally between immediately vertically- adjacent control gate lines in the stack, the channels in individual of the NAND strings being interconnected by the hollow cylinder semiconductive material; and (8) dummy structures extending vertically through the control gate lines and the another dielectric in the end portion, (9) the dummy structure comprising a hollow cylinder of semiconductive material of the same composition as the hollow cylinder semiconductive material of the channels.

Regarding claim 40 of the present invention:

40. (Previously Presented): The stack of claim 39 further comprising (9) contacts in the end portion that individual extend to the individual gate lines.

Regarding claim 42 of the present invention:

42. The integrated circuitry of claim 39 wherein (10) the vertically oriented transistors are charge storage transistors of individual memory cells.

Regarding claim 43 of the present invention:

43. The integrated circuitry of claim 42 wherein the memory cells comprise (11) a portion of NAND architecture.

Claim 17 0f US 9,929,175:

17. A memory array comprising (1) a stack of memory cells of NAND architecture (which including gate lines extending horizontally and vertically overlapping (stack of memory cells with vertically oriented transistors)): a substrate comprising (2) a primary portion and (3) an end portion; (5, 11) a plurality of NAND strings of vertically oriented transistors (operation structure) in the primary portion; (6, 7, 10) the transistors (operation structure) individually comprising a channel, a tunnel dielectric laterally outward of the channel, a charge trapping material laterally outward of the tunnel

dielectric, a dielectric material laterally outward of the charge trapping material, and a control gate laterally outward of the dielectric material; the control gate comprising a portion of one of a plurality of horizontally extending control gate lines, (4) the control gate lines extending horizontally farther in the end portion moving deeper into the stack in the end portion, another dielectric elevationally between immediately vertically-adjacent control gate lines in the stack, the channels in individual of the NAND strings being interconnected; (8) dummy structures extending vertically through the control gate lines and the another dielectric in the end portion; and (9) a contact in the end portion between two immediately horizontally- adjacent of the dummy structures to individual of the control gate lines in the end portion.

Regarding claim 44 of the present invention:

44. The integrated circuitry of claim 39 wherein (12) the operative and dummy structures comprise the same material.

Claim 1 0f US 9,929,175:

1. A memory array comprising (1) a stack of memory cells of NAND architecture (which including gate lines extending horizontally and vertically overlapping (stack of memory cells with vertically oriented transistors)): a substrate comprising (2) a primary portion and (3) an end portion; (5, 11) a plurality of NAND strings of vertically oriented transistors (operation structure) in the primary portion; (6, 7, 10) the transistors (operation structure) individually comprising a channel, a tunnel dielectric laterally outward of the channel, a charge trapping material laterally outward of the tunnel dielectric, a dielectric material laterally outward of the charge trapping material, and a control gate laterally outward of the dielectric material; the control gate comprising a

portion of one of a plurality of horizontally extending control gate lines, (4) the control gate lines extending horizontally farther in the end portion moving deeper into the stack in the end portion, another dielectric elevationally between immediately vertically-adjacent control gate lines in the stack, the channels in individual of the NAND strings being interconnected; and (8) dummy structures extending vertically through the control gate lines and the another dielectric in the end portion.

Claim 3 0f US 9,929,175:

3. The memory array of claim 1 wherein the dummy structures comprise (12) at least some of the same material as that of the NAND strings.

Regarding claim 45 of the present invention:

45. The integrated circuitry of claim 44 wherein (13) the operative and dummy structures comprise a plurality of the same materials.

Claim 4 0f US 9,929,175:

4. The memory array of claim 3 wherein (13) the dummy structures comprise a plurality of the same materials as that of the NAND strings.

Regarding claim 46 of the present invention:

46. The inlegrated circuitry of claim 45 wherein (14) the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

Claim 5 0f US 9,929,175:

5. The memory array of claim 4 wherein (14) the same materials are arranged in the same lateral order relative one another in the NAND strings and n the dummy structures.

Claim 47 of the present invention is reject for the same reason of the rejection of claim 44.

Claim 48 and 49 of the present invention are reject for the same reason of the rejection of claim 44 because the NAND strings comprising semiconductor channel (see claim 10 of the US 9,929,175.

Regarding claim 50 of the present invention:

50. (1) A stack of horizontally extending and vertically overlapping features, the stack comprising: (2) a primary portion and (3) an end portion, (4) at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion; (5) operative structures extending vertically through the features in the primary portion; and (6) dummy structures extending vertically through the features in the end portion, (7) the dummy structures individually comprising a cylinder of semiconductive material.

Claim 10 0f US 9,929,175:

10. A memory array comprising (1) a stack of memory cells of NAND architecture (which including gate lines extending horizontally and vertically overlapping (stack of memory cells with vertically oriented transistors)): a substrate comprising (2) a primary portion and (3) an end portion; (5) a plurality of NAND strings of vertically oriented transistors (features) in the primary portion; the transistors (features) individually comprising a channel comprising a hollow cylinder of semiconductive material, a tunnel dielectric laterally outward of the channel, a charge trapping material laterally outward of the tunnel dielectric, a dielectric material laterally outward of the charge trapping material, and a control gate laterally outward of the dielectric material; the control gate

comprising a portion of one of a plurality of horizontally extending control gate lines, (4) the control gate lines (of the features) extending horizontally farther in the end portion moving deeper into the stack in the end portion, another dielectric elevationally between immediately vertically- adjacent control gate lines in the stack, the channels in individual of the NAND strings being interconnected by the hollow cylinder semiconductive material; and (6) dummy structures extending vertically through the control gate lines and the another dielectric in the end portion, (7) the dummy structure comprising a hollow cylinder of semiconductive material of the same composition as the hollow cylinder semiconductive material of the channels.

Regarding claim 52 of the present invention:

52. The stack of claim 50 wherein individual of the cylinders of semiconductive material define a radially- outermost horizontal periphery of individual of the dummy structures.

Claim 10 of US 9,929,175 disclose that " the dummy structure comprising a hollow cylinder of semiconductive material of the same composition as the hollow cylinder semiconductive material of the channels" that means the cylinders of semiconductive material define a radially- outermost horizontal periphery of individual of the dummy structures.

Regarding claim 53 of the present invention:

53. The stack of claim 50 wherein the operative structures individually comprise a cylinder of semiconductor material.

Claim 10 of US 9,929,175 disclose that " the dummy structure comprising a hollow cylinder of semiconductive material of the same composition as the hollow cylinder

semiconductive material of the channels" that means the operative structures (including individually channel) individually comprise a cylinder of semiconductor material.

Regarding claim 54 of the present invention:

54. The stack of claim 50 further comprising vertical contacts in the end portion connecting with conductive material of individual of the features.

Claim 10 of US 9,929,175 disclose that , "the channels in individual of the NAND strings(of the features) being interconnected by the hollow cylinder semiconductive material" that means vertical contacts in the end portion connecting with conductive material of individual of the features.

Regarding claim 55 of the present invention:

55. (1) A stack of horizontally extending and vertically overlapping features, the stack comprising: (2) a primary portion and (3) an end portion, (4) at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion; (5) operative structures extending vertically through the features in the primary portion, (6) the operative structures comprising portions of memory cells, (7) the memory cells comprising a portion of NAND architecture,(7) the operative structures comprising interconnected channel regions of a NAND string; and (8) dummy structures extending vertically through the features in the end portion, (9) some of the dummy structures horizontally overlapping the primary portion and the end portion.

Claim 56 of the present invention:

56. The stack of claim 55 (10) wherein the dummy structures comprise a cylinder of semiconductive material.

Claim 10 0f US 9,929,175:

10. A memory array comprising (1) a stack of memory cells of NAND architecture (which including gate lines extending horizontally and vertically overlapping (stack of memory cells with vertically oriented transistors)): a substrate comprising (2) a primary portion and (3) an end portion; (4) a plurality of NAND strings of vertically oriented transistors (features) in the primary portion; (6, 7) the transistors (of the features) individually comprising a channel comprising a hollow cylinder of semiconductive material, a tunnel dielectric laterally outward of the channel, a charge trapping material laterally outward of the tunnel dielectric, a dielectric material laterally outward of the charge trapping material, and a control gate laterally outward of the dielectric material; the control gate comprising a portion of one of a plurality of horizontally extending control gate lines, (5) the control gate lines extending horizontally farther in the end portion moving deeper into the stack in the end portion, another dielectric elevationally between immediately vertically- adjacent control gate lines in the stack, the channels in individual of the NAND strings being interconnected by the hollow cylinder semiconductive material; and (8) dummy structures extending vertically through the control gate lines and the another dielectric in the end portion, (9, 10) the dummy structure comprising a hollow cylinder of semiconductive material of the same composition as the hollow cylinder semiconductive material of the channels.

Claim 10 of US 9,929,175 includes all the limitations of claims 55 and 56 of the present invention.

Claim 51 is rejected on the ground of nonstatutory double patenting as being unpatentable over claim 10 of U.S. Patent No. 9,929,175 in view of Fukuzumi et al. (US 2010/0244119).

Claim 10 of US 9,929,175 does not explicitly teach that the stack comprising solid material filling radially internal regions of individual of the cylinders of semiconductive material.

Fukuzumi et al. teaches that the stack comprising a solid material (68) filling radially internal regions of individual of the cylinders of semiconductive material (SP).

Claim 10 of US 9,929,175 and Fukuzumi et al. are both analogous art because both are directed to a vertical memory devices and one of ordinary skill in the art would have had a reasonable expectation of success to modify teaching of Fukuzumi et al. into Claim 10 of US 9,929,175 because they are from the same field of endeavor.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the stack comprising solid material filling radially internal regions of individual of the cylinders of semiconductive material as taught by Fukuzumi et al in order to physically support the hollow semiconductive material.

## Allowable Subject Matter

4. Claims 57-61 are allowed.

The following is an examiner's statement of reasons for allowance: above references appear to be the closest prior art reference. However, these reference fail to teach the following: "vertical contacts in the end portion connecting with individual of the

control gate lines, the contacts and dummy structures having different horizontal cross-sections relative one another" (claim 57) and "vertical contacts in the end portion connecting with individual of the control gate lines, at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line" (claim 60).

## Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong Nguyen whose telephone number is (571) 272-1661. The examiner can normally be reached on 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/CUONG Q NGUYEN/
Primary Examiner, Art Unit 2811

| Notice of References Cited | Application/Control No. 15/900,188 | Applicant(s)/Patent Under Reexamination Tang et al. | |
|---|---|---|---|
| | Examiner CUONG Q NGUYEN | Art Unit 2811 | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * | | Document Number Country Code-Number-Kind Code | Date MM-YYYY | Name | CPC Classification | US Classification |
|---|---|---|---|---|---|---|
| * | A | US-9929175-B2 | 03-2018 | Tang; Sanh D. | H01L27/101 | 1/1 |
| * | B | US-20100244119-A1 | 09-2010 | Fukuzumi; Yoshiaki | H01L27/11582 | 257/324 |
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**FOREIGN PATENT DOCUMENTS**

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| Search Notes | Application/Control No. | Applicant(s)/Patent Under Reexamination |
|---|---|---|
| | 15/900,188 | Tang et al. |
| | Examiner | Art Unit |
| | CUONG Q NGUYEN | 2811 |

| CPC - Searched* | | |
|---|---|---|
| Symbol | Date | Examiner |
| H01L27/10, 101, 11556, 1157, 11582, 249, 29/66825, 788 | 04/13/2019 | CN |

| CPC Combination Sets - Searched* | | |
|---|---|---|
| Symbol | Date | Examiner |
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| US Classification - Searched* | | | |
|---|---|---|---|
| Class | Subclass | Date | Examiner |
| | | | |

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

| Search Notes | | |
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| Search Notes | Date | Examiner |
| EAST, EPO, JPO, DERWENT, IBM, inventor name | 04/13/2019 | CN |

| Interference Search | | | |
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**CONFIRMATION NO. 1775**

| SERIAL NUMBER | FILING or 371(c) DATE<br>RULE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET NO. |
|---|---|---|---|---|
| 15/900,188 | 02/20/2018 | 438 | 2811 | MI22-6502 |

**APPLICANTS**
Micron Technology, Inc., Boise, ID;

**INVENTORS**
Sanh D. Tang, Boise, ID;
Roger W. Lindsay, Boise, ID;
Krishna K. Parat, Palo Alto, CA;

**** CONTINUING DATA ***************************
This application is a CON of 15/397,919 01/04/2017 PAT 9929175
which is a CON of 15/095,208 04/11/2016 PAT 9564471
which is a DIV of 14/602,559 01/22/2015 PAT 9318430
which is a DIV of 13/085,083 04/12/2011 PAT 8945996

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
03/14/2018

| Foreign Priority claimed | ❑ Yes ☑ No | ❑ Met after Allowance | STATE OR COUNTRY | SHEETS DRAWINGS | TOTAL CLAIMS | INDEPENDENT CLAIMS |
|---|---|---|---|---|---|---|
| 35 USC 119(a-d) conditions met | ❑ Yes ☑ No | | | | | |
| Verified and Acknowledged | /CUONG QUANG NGUYEN/ Examiner's Signature | /CN/ Initials | ID | 18 | 22 | 5 |

**ADDRESS**
Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201
UNITED STATES

**TITLE**
Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

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**EAST Search History**

**EAST Search History (Prior Art)**

| Ref # | Hits | Search Query | DBs | Default Operator | Plurals | Time Stamp |
|---|---|---|---|---|---|---|
| L1 | 2300 | (vertical$5 near5 (transistor or gate)) and semiconductor and dummy and memory and (@pd<="20110412" or @ad<="20110412" or @rlad<="20110412") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2019/04/08 11:50 |
| L2 | 2089 | (vertical$5 near5 (transistor or gate)) and semiconductor and (h01l27/10.cpc. or h01l27/101.cpc. or h01l27/11556.cpc. or h01l27/1157.cpc. or h01l27/11582.cpc. or h01l27/249.cpc. or h01l29/66825.cpc. or h01l29/788.cpc.) and memory and (@pd<="20110412" or @ad<="20110412" or @rlad<="20110412") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2019/04/08 12:05 |
| L3 | 222 | (vertical$5 near5 (transistor or gate)) and semiconductor and (micron adj technology) and dummy and memory and (@pd<="20110412" or @ad<="20110412" or @rlad<="20110412") | US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB | OR | ON | 2019/04/08 12:13 |

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**EAST Search History**

**EAST Search History (Prior Art)**

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Sheet 1 of 1

| *Complete if Known* | |
|---|---|
| **Application Number** | 15/900,188 |
| **Filing Date** | February 20, 2018 |
| **First Named Inventor** | Sanh D. Tang |
| Art Unit | 2811 |
| Examiner Name | Cuong Quang Nguyen |
| Attorney Docket Number | MI22-6502 |

## U.S. PATENT DOCUMENTS

| Examiner initial * | Cite No. | Document Number<br>Number - Kind Code [2] (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
| | 1 | US-2011/0156132 | 06-30-2011 | Kiyotoshi | |
| | 2 | US-8,426,908 | 04-23-2013 | Higashi | |
| | 3 | US-8,581,323 | 11-12-2013 | Uenaka et al. | |
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## FOREIGN PATENT DOCUMENTS

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|---|---|
| **Application Number** | Filed Herewith |
| **Filing Date** | February 20, 2018 |
| **First Named Inventor** | Sanh D. Tang |
| Art Unit | Unknown |
| Examiner Name | Unknown |
| Attorney Docket Number | MI22-6502 |

## U.S. PATENT DOCUMENTS

| Examiner initial * | Cite No. | Document Number: Number - Kind Code [2] (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
| | 1 | US-2006/0148171 | 07-06-2006 | Lee | |
| | 2 | US-2009/0309152 | 12-17-2009 | Knoefler et al. | |
| | 3 | US-2011/0199804 | 08-18-2011 | Son | |
| | 4 | US-2012/0003831 | 01-05-2012 | Kang et al. | |
| | 5 | US-2012/0052674 | 03-01-2012 | Lee et al. | |
| | 6 | US-2014/0106569 | 04-17-2014 | Oh et al. | |
| | 7 | US-2014/0162420 | 06-12-2014 | Oh et al. | |
| | 8 | US-2014/0179068 | 06-26-2014 | Samachisa | |
| | 9 | US-5,414,285 | 05-09-1995 | Nishihara | |
| | 10 | US-6,023,099 | 02-08-2000 | Komuro | |
| | 11 | US-6,472,735 | 10-29-2002 | Isaak | |
| | 12 | US-7,446,038 | 11-04-2008 | Jeng | |
| | 13 | US-9,034,710 | 05-19-2015 | Sills | |
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## FOREIGN PATENT DOCUMENTS

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| Sheet | 2 | of | 2 |
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| **Application Number** | Filed Herewith |
| **Filing Date** | February 20, 2018 |
| **First Named Inventor** | Sanh D. Tang |
| Art Unit | Unknown |
| Examiner Name | Unknown |
| Attorney Docket Number | MI22-6502 |

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|---|---|---|---|
| | 14 | Katsumata et al., "Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Coperation for Ultra High Density Storage Devices", Toshiba Corporation, 2009 Symposium on VLSI Technology Digest of Technical Papers, pp. 136-137. | |
| | 15 | Komori et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device", Center for Semiconductor Research & Development, Toshiba Coporation, IEEE, 2008, pp. 851-854. | |
| | 16 | Niklaus et al., "Wafer-Level 3D Integration Technology Platforms for ICs and MEMS", Research Paper, Center for Integrated Institute, Rennsselaer Polytechnic Institute (RPI); 1/2005; 8pp. | |
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| Examiner Signature | /CUONG Q NGUYEN/ | Date Considered | 04/13/2019 |
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| PATENT APPLICATION FEE DETERMINATION RECORD<br>Substitute for Form PTO-875 | Application or Docket Number<br>15/900,188 | Filing Date<br>02/20/2018 | ☐ To be Mailed |
|---|---|---|---|

**ENTITY:** ☑ LARGE ☐ SMALL ☐ MICRO

## APPLICATION AS FILED - PART I

| FOR | (Column 1)<br>NUMBER FILED | (Column 2)<br>NUMBER EXTRA | | RATE ($) | FEE ($) |
|---|---|---|---|---|---|
| ☐ BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | | N/A | |
| ☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | | N/A | |
| ☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | | N/A | |
| TOTAL CLAIMS (37 CFR 1.16(i)) | minus 20 = | * | | x $100 = | |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | minus 3 = | * | | x $460 = | |
| ☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | |
| ☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | | TOTAL | |

## APPLICATION AS AMENDED - PART II

| AMENDMENT | 01/22/2019 | (Column 1)<br>CLAIMS REMAINING AFTER AMENDMENT | | (Column 2)<br>HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3)<br>PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * 20 | Minus | ** 22 | = 0 | | x $100 = | 0 |
| | Independent (37 CFR 1.16(h)) | * 4 | Minus | *** 5 | = 0 | | x $460 = | 0 |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | 0 |

| AMENDMENT | | (Column 1)<br>CLAIMS REMAINING AFTER AMENDMENT | | (Column 2)<br>HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3)<br>PRESENT EXTRA | | RATE ($) | ADDITIONAL FEE ($) |
|---|---|---|---|---|---|---|---|---|
| | Total (37 CFR 1.16(i)) | * | Minus | ** | = | | x $0 = | |
| | Independent (37 CFR 1.16(h)) | * | Minus | *** | = | | x $0 = | |
| | ☐ Application Size Fee (37 CFR 1.16(s)) | | | | | | | |
| | ☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | |
| | | | | | | | TOTAL ADD'L FEE | |

| | |
|---|---|
| * If the entry in column 1 is less than the entry in column 2, write "0" in column 3. | SLIE |
| ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". | /VONDA A GALE/ |
| *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". | |
| The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1. | |

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

PTO/SB/08a (07-09)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

Sheet 1 of 1

| *Complete if Known* | |
|---|---|
| **Application Number** | 15/900,188 |
| **Filing Date** | February 20, 2018 |
| **First Named Inventor** | Sanh D. Tang |
| Art Unit | 2811 |
| Examiner Name | Cuong Quang Nguyen |
| Attorney Docket Number | MI22-6502 |

## U.S. PATENT DOCUMENTS

| Examiner Initial * | Cite No. | Document Number<br>Number - Kind Code[2] (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
| | 1 | US-2011/0156132 | 06-30-2011 | Kiyotoshi | |
| | 2 | US-8,426,908 | 04-23-2013 | Higashi | |
| | 3 | US-8,581,323 | 11-12-2013 | Uenaka et al. | |
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## FOREIGN PATENT DOCUMENTS

| Examiner Initial * | Cite No. 1 | Foreign Patent Document<br>Country[3] Code Number[4] Kind Code (if known)[5] | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear | T |
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| Examiner Signature | | Date Considered | |
|---|---|---|---|

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not Considered. Include copy of this form with next communication to applicant. 1. Applicant's unique citation design number (optional). 2 See Kinds Codes of USPTO patent Documents. at www.uspto.gov or MPEP 901.04. 3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

**SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786.9199) and select option 2.*

| Electronic Acknowledgement Receipt | |
|---|---|
| **EFS ID:** | 34921095 |
| **Application Number:** | 15900188 |
| **International Application Number:** | |
| **Confirmation Number:** | 1775 |
| **Title of Invention:** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells |
| **First Named Inventor/Applicant Name:** | Sanh D. Tang |
| **Customer Number:** | 128753 |
| **Filer:** | Mark S. Matkin/Bridget Wiseman |
| **Filer Authorized By:** | Mark S. Matkin |
| **Attorney Docket Number:** | MI22-6502 |
| **Receipt Date:** | 22-JAN-2019 |
| **Filing Date:** | 20-FEB-2018 |
| **Time Stamp:** | 14:37:44 |
| **Application Type:** | Utility under 35 USC 111(a) |

## Payment information:

| Submitted with Payment | no |
|---|---|

## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
|---|---|---|---|---|---|
| 1 | | 6502_M02.pdf | 31348<br>71a245d56837ab2010d321f0b0b64bbefb6e4549 | yes | 7 |

| | Multipart Description/PDF files in .zip description | | |
|---|---|---|---|
| | **Document Description** | **Start** | **End** |
| | Response to Election / Restriction Filed | 1 | 1 |
| | Claims | 2 | 6 |
| | Applicant Arguments/Remarks Made in an Amendment | 7 | 7 |

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|---|---|---|---|---|---|
| **Warnings:** | | | | | |
| **Information:** | | | | | |
| 2 | | 6502_SIDS_1-17-19.pdf | 130350<br>269c6dc0b8fccfac03ab2c900753cd6ee8e42b37 | yes | 2 |

| | Multipart Description/PDF files in .zip description | | |
|---|---|---|---|
| | **Document Description** | **Start** | **End** |
| | Transmittal Letter | 1 | 1 |
| | Information Disclosure Statement (IDS) Form (SB08) | 2 | 2 |

| | |
|---|---|
| **Warnings:** | |
| **Information:** | |
| **Total Files Size (in bytes):** | 161698 |

**This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.**

**New Applications Under 35 U.S.C. 111**
**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**
**National Stage of an International Application under 35 U.S.C. 371**
**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**
**New International Application Filed with the USPTO as a Receiving Office**
**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .....15/900,188
Filing Date .....February 20, 2018
Confirmation No. ..... 1775
Inventor.....Sanh D. Tang
Assignee .....Micron Technology, Inc.
Group Art Unit ..... 2811
Examiner .....Cuong Quang Nguyen
Attorney's Docket No. ..... MI22-6502
Title:....Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

**RESPONSE TO THE ELECTION/RESTRICTION MAILED DECEMBER 27, 2018**

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. Main Avenue, Suite 600
Spokane, WA 99201-0613

**AMENDMENTS**

Responsive to the Office Action dated December 27, 2018, Applicant amends and remarks as follows:

**Amendments to the Claims:**

Claims 1-38 (Cancelled).

39. (Previously Presented): Integrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines, the integrated circuitry comprising:

a primary portion and an end portion, at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the gate lines in the primary portion, the operative structures comprising semiconductive material, the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines; and

dummy structures extending vertically through the gate lines in the end portion.

40. (Previously Presented): The stack of claim 39 further comprising contacts in the end portion that individual extend to the individual gate lines.

Claim 41 (Cancelled).

42. (Previously Presented): The integrated circuitry of claim 39 wherein the vertically oriented transistors are charge storage transistors of individual memory cells.

43. (Previously Presented): The integrated circuitry of claim 42 wherein the memory cells comprise a portion of NAND architecture.

44. (Previously Presented): The integrated circuitry of claim 39 wherein the operative and dummy structures comprise the same material.

45. (Previously Presented): The integrated circuitry of claim 44 wherein the operative and dummy structures comprise a plurality of the same materials.

46. (Previously Presented): The integrated circuitry of claim 45 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

47. (Previously Presented): The integrated circuitry of claim 44 wherein the operative and dummy structures consist essentially of the same material.

48. (Previously Presented): The integrated circuitry of claim 39 wherein the dummy structures comprise semiconductor material.

49. (Previously Presented): The integrated circuitry of claim 39 wherein the dummy structures comprise the semiconductive material.

50. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion, the dummy structures individually comprising a cylinder of semiconductive material.

51. (Previously Presented): The stack of claim 50 comprising solid material filling radially internal regions of individual of the cylinders of semiconductive material.

52. (Previously Presented): The stack of claim 50 wherein individual of the cylinders of semiconductive material define a radially-outermost horizontal periphery of individual of the dummy structures.

53. (Previously Presented): The stack of claim 50 wherein the operative structures individually comprise a cylinder of semiconductor material.

54. (Previously Presented): The stack of claim 50 further comprising vertical contacts in the end portion connecting with conductive material of individual of the features.

55. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string; and

dummy structures extending vertically through the features in the end portion, some of the dummy structures horizontally overlapping the primary portion and the end portion.

56. (Previously Presented): The stack of claim 55 wherein the dummy structures comprise a cylinder of semiconductive material

57. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion; and

vertical contacts in the end portion connecting with individual of the control gate lines, the contacts and dummy structures having different horizontal cross-sections relative one another.

58. (Previously Presented): The stack of claim 57 wherein the different horizontal cross-sections are of the same shape and of different sizes relative one another.

59. (Previously Presented): The stack of claim 57 wherein the different horizontal cross-sections have different values of total horizontal area relative one another.

60. (Previously Presented): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, the at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion, some of the dummy structures being longitudinally spaced alone a horizontal line; and

vertical contacts in the end portion connecting with individual of the control gate lines, at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line.

61. (Previously Presented): The stack of claim 60 wherein the horizontal line is linearly straight.

## REMARKS

Claims 39, 40, and 42-61 are in the application.

The Examiner has required restriction under 35 U.S.C. §121 between, claims 1-3 and 14-21 (Invention I), drawn to a semiconductor device, allegedly classified in class 257, subclass 292, and claims 28-31 (Invention II), drawn to a method of making a semiconductor device, allegedly classified in class 438, subclass 100+.

The Examiner's restriction is with respect to claims that are not in the application and is thereby in fundamental error. To any extent that the Examiner is restricting between method and device subject matter and claims, Applicant hereby elects device, with each of claims 39, 40, and 42-61 being readable thereon.

Examination on the merits is requested.

Respectfully submitted,

Dated: January 18, 2019

By: /Mark S. Matkin/
Mark S. Matkin
Reg. No. 32,268

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .....15/900,188
Filing Date .....February 20, 2018
Confirmation No. ..... 1775
Inventor.....Sanh D. Tang
Assignee .....Micron Technology, Inc.
Group Art Unit ..... 2811
Examiner .....Cuong Quang Nguyen
Attorney's Docket No. ..... MI22-6502
Title:....Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References - - See attached Form PTO/SB/08A-B

The attached Form PTO/SB/08 is submitted in compliance with 37 CFR §§ 1.56, 1.97 and 1.98, and your attention is directed to the references listed on the attached Form PTO/SB/08. No admission is made regarding whether the submitted references are prior art.

This Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing of a first Office Action on the merits, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for this filing, please charge the fee, any underpayment or credit any overpayment specified under 37 CFR § 1.17(p) to Deposit Account No. 23-0925.

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: January 17, 2019 By: /Mark S. Matkin/
Mark S. Matkin
Reg. No. 32,268

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 15/900,188 | 02/20/2018 | Sanh D. Tang | MI22-6502 | 1775 |

128753 7590 12/27/2018

Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

| EXAMINER | |
|---|---|
| NGUYEN, CUONG QUANG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2811 | |
| **MAIL DATE** | **DELIVERY MODE** |
| 12/27/2018 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| *Office Action Summary* | **Application No.** 15/900,188 | **Applicant(s)** Tang et al. | |
|---|---|---|---|
| | **Examiner** CUONG Q NGUYEN | **Art Unit** 2811 | **AIA Status** No |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims***

5) ☑ Claim(s) 1-41 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☐ Claim(s) _____ is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☑ Claim(s) 1-41 are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

**Application Papers**

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

***Notice of Pre-AIA or AIA Status***

The present application is being examined under the pre-AIA first to invent provisions.

**DETAILED ACTION**

***Election/Restrictions***

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-3 and 14-21, drawn to a semiconductor device, classified in class 257, subclass 292.

II. Claims 28-31, drawn to a method of making a semiconductor device, classified in class 438, subclass 100+.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case unpatentability of the group I invention would not necessarily imply unpatentability of the group II invention, since the device of the group I invention could be made by processes materially different from those of group II invention, for example in method claim 1, selectively forming the sacrificial material at desired areas instead of forming the sacrificial material and the remove unwanted portions of the sacrificial material.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cuong Nguyen whose telephone number is (571) 272-1661. The examiner can normally be reached on 8:00 am to 5:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Lynne Gurley who can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-irect.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free).

/CUONG Q NGUYEN/
Primary Examiner, Art Unit 2811

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NUMBER | FILING OR 371(C) DATE | FIRST NAMED APPLICANT | ATTY. DOCKET NO./TITLE |
|---|---|---|---|
| 15/900,188 | 02/20/2018 | Sanh D. Tang | MI22-6502 |

**CONFIRMATION NO. 1775**

**PUBLICATION NOTICE**

128753
Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

*OC000000100460390*

**Title:**Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

**Publication No.**US-2018-0175059-A1
**Publication Date:**06/21/2018

## NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

## PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/900,188

### APPLICATION AS FILED - PART I

| FOR | (Column 1) NUMBER FILED | (Column 2) NUMBER EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY FEE($) |
|---|---|---|---|---|---|---|---|
| BASIC FEE (37 CFR 1.16(a), (b), or (c)) | N/A | N/A | N/A | | | N/A | 300 |
| SEARCH FEE (37 CFR 1.16(k), (i), or (m)) | N/A | N/A | N/A | | | N/A | 660 |
| EXAMINATION FEE (37 CFR 1.16(o), (p), or (q)) | N/A | N/A | N/A | | | N/A | 760 |
| TOTAL CLAIMS (37 CFR 1.16(i)) | 22 minus 20 = | * 2 | | | OR | x 100 = | 200 |
| INDEPENDENT CLAIMS (37 CFR 1.16(h)) | 5 minus 3 = | * 2 | | | | x 460 = | 920 |
| APPLICATION SIZE FEE (37 CFR 1.16(s)) | If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). | | | | | | 0.00 |
| MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j)) | | | | | | | 0.00 |
| * If the difference in column 1 is less than zero, enter "0" in column 2. | | | TOTAL | | | TOTAL | 2840 |

### APPLICATION AS AMENDED - PART II

AMENDMENT A

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | SMALL ENTITY RATE($) | SMALL ENTITY ADDITIONAL FEE($) | OR | OTHER THAN SMALL ENTITY RATE($) | OTHER THAN SMALL ENTITY ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

AMENDMENT B

| | (Column 1) CLAIMS REMAINING AFTER AMENDMENT | | (Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR | (Column 3) PRESENT EXTRA | RATE($) | ADDITIONAL FEE($) | OR | RATE($) | ADDITIONAL FEE($) |
|---|---|---|---|---|---|---|---|---|---|
| Total (37 CFR 1.16(i)) | * | Minus | ** | = | x = | | OR | x = | |
| Independent (37 CFR 1.16(h)) | * | Minus | *** | = | x = | | OR | x = | |
| Application Size Fee (37 CFR 1.16(s)) | | | | | | | | | |
| FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j)) | | | | | | | OR | | |
| | | | | | TOTAL ADD'L FEE | | OR | TOTAL ADD'L FEE | |

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

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| APPLICATION NUMBER | FILING or 371(c) DATE | GRP ART UNIT | FIL FEE REC'D | ATTY.DOCKET.NO | TOT CLAIMS | IND CLAIMS |
|---|---|---|---|---|---|---|
| 15/900,188 | 02/20/2018 | 2811 | 2840 | MI22-6502 | 22 | 5 |

**CONFIRMATION NO. 1775**

**FILING RECEIPT**

128753
Wells St. John, P.S.
601 W. Main Avenue
Suite 600
Spokane, WA 99201

OC000000098089577

Date Mailed: 03/15/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

**Inventor(s)**

Sanh D. Tang, Boise, ID;
Roger W. Lindsay, Boise, ID;
Krishna K. Parat, Palo Alto, CA;

**Applicant(s)**

Micron Technology, Inc., Boise, ID;

**Assignment For Published Patent Application**

Micron Technology, Inc., Boise, ID

**Power of Attorney:** The patent practitioners associated with Customer Number 128753

**Domestic Priority data as claimed by applicant**

This application is a CON of 15/397,919 01/04/2017 PAT 9929175
which is a CON of 15/095,208 04/11/2016 PAT 9564471
which is a DIV of 14/602,559 01/22/2015 PAT 9318430
which is a DIV of 13/085,083 04/12/2011 PAT 8945996

**Foreign Applications** for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
*Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.*

**Permission to Access Application via Priority Document Exchange:** Yes

**Permission to Access Search Results:** Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

**If Required, Foreign Filing License Granted:** 03/14/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/900,188**

**Projected Publication Date:** 06/21/2018

**Non-Publication Request:** No

**Early Publication Request:** No

**Title**

Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

**Preliminary Class**

257

**Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:** No

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## Title 37, Code of Federal Regulations, 5.11 & 5.15

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .....Filed Herewith
Filing Date .....Filed Herewith
Confirmation No. .....Unknown
Inventor.....Sanh D. Tang
Assignee .....Micron Technology, Inc.
Group Art Unit .....Unknown
Examiner .....Unknown
Attorney's Docket No. ..... MI22-6502
Title:....Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

## PRELIMINARY AMENDMENT

To: Mail Stop Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Mark S. Matkin (Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. Main Avenue, Suite 600
Spokane, WA 99201-0613

## AMENDMENTS

Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

**Amendments To The Specification:**

At page 1 before the "Technical Field" section, insert the following:

**RELATED PATENT DATA**

**[0001]** This patent resulted from a continuation application of U.S. Patent Application Serial No.15/397,919, filed January 4, 2017, entitled "Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells", naming Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat as inventors, which was a continuation application of U.S. Patent Application Serial No. 15/095,208, filed April 11, 2016, now US Patent No. 9,564,471, entitled "Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells", naming Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat as inventors, which is a divisional application of U.S. Patent Application Serial No. 14/602,559, filed January 22, 2015, now U.S. Patent No. 9,318,430, which is a divisional application of U.S. Patent Application Serial No. 13/085,083, filed April 12, 2011, now U.S. Patent No. 8,945,996, entitled "Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells", naming Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat as inventors, the disclosures of which are incorporated by reference.

**Amendments To The Claims:**

Claims 1-38 (Cancelled).

39. (Currently Amended) ~~A stack~~ Integrated circuitry comprising a stack of horizontally extending and vertically overlapping ~~features~~ conductive transistor gate lines, the ~~stack comprising~~ integrated circuitry comprising:

a primary portion and an end portion, at least some of the ~~features~~ gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the ~~features~~ gate lines in the primary portion, the operative structures comprising semiconductive material, the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines; and

dummy structures extending vertically through the ~~features~~ gate lines in the end portion.

40. (Currently Amended) The stack of claim 39 further comprising contacts in the end portion that individual extend to the individual gate lines.

Claim 41 (Cancelled).

42. (New): The integrated circuitry of claim 39 wherein the vertically oriented transistors are charge storage transistors of individual memory cells.

43. (New): The integrated circuitry of claim 42 wherein the memory cells comprise a portion of NAND architecture.

44. (New): The integrated circuitry of claim 39 wherein the operative and dummy structures comprise the same material.

45. (New): The integrated circuitry of claim 44 wherein the operative and dummy structures comprise a plurality of the same materials.

46. (New): The integrated circuitry of claim 45 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

47. (New): The integrated circuitry of claim 44 wherein the operative and dummy structures consist essentially of the same material.

48. (New): The integrated circuitry of claim 39 wherein the dummy structures comprise semiconductor material.

49. (New): The integrated circuitry of claim 39 wherein the dummy structures comprise the semiconductive material.

50. (New): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion, the dummy structures individually comprising a cylinder of semiconductive material.

51. (New): The stack of claim 50 comprising solid material filling radially internal regions of individual of the cylinders of semiconductive material.

52. (New): The stack of claim 50 wherein individual of the cylinders of semiconductive material define a radially-outermost horizontal periphery of individual of the dummy structures.

53. (New): The stack of claim 50 wherein the operative structures individually comprise a cylinder of semiconductor material.

54. (New): The stack of claim 50 further comprising vertical contacts in the end portion connecting with conductive material of individual of the features.

55. (New): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string; and

dummy structures extending vertically through the features in the end portion, some of the dummy structures horizontally overlapping the primary portion and the end portion.

56. (New): The stack of claim 55 wherein the dummy structures comprise a cylinder of semiconductive material

57. (New): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion; and

vertical contacts in the end portion connecting with individual of the control gate lines, the contacts and dummy structures having different horizontal cross-sections relative one another.

58. (New): The stack of claim 57 wherein the different horizontal cross-sections are of the same shape and of different sizes relative one another.

59. (New): The stack of claim 57 wherein the different horizontal cross-sections have different values of total horizontal area relative one another.

60. (New): A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, the at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion, some of the dummy structures being longitudinally spaced alone a horizontal line; and

vertical contacts in the end portion connecting with individual of the control gate lines, at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line.

61. (New): The stack of claim 60 wherein the horizontal line is linearly straight.

## REMARKS

This application is a continuation of U.S. Patent Application Serial No. 15/397,919.

Claims 39 and 40 are amended. Claims 1-38 and 41 are cancelled. Claims 42-61 are added. Claims 39, 40, and 42-61 are in the application for consideration.

Examination on the merits is requested.

Respectfully submitted,

Dated: February 18, 2018 By: /Mark S. Matkin/
Mark S. Matkin
Reg. No. 32,268

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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## Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

## Inventor Information:

**Inventor 1** Remove

**Legal Name**

| Prefix | Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|---|
| | Sanh | D. | Tang | |

**Residence Information (Select One)** ◉ US Residency ○ Non US Residency ○ Active US Military Service

| City | Boise | State/Province | ID | Country of Residence | US |
|---|---|---|---|---|---|

**Mailing Address of Inventor:**

| Address 1 | 11587 W. Verde Drive | | |
|---|---|---|---|
| Address 2 | | | |
| City | Boise | State/Province | ID |
| Postal Code | 83709 | Country i | US |

**Inventor 2** Remove

**Legal Name**

| Prefix | Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|---|
| | Roger | W. | Lindsay | |

**Residence Information (Select One)** ◉ US Residency ○ Non US Residency ○ Active US Military Service

| City | Boise | State/Province | ID | Country of Residence | US |
|---|---|---|---|---|---|

**Mailing Address of Inventor:**

| Address 1 | 4376 Falconcrest Way | | |
|---|---|---|---|
| Address 2 | | | |
| City | Boise | State/Province | ID |
| Postal Code | 83716 | Country i | US |

**Inventor 3** Remove

**Legal Name**

| Prefix | Given Name | Middle Name | Family Name | Suffix |
|---|---|---|---|---|
| | Krishna | K. | Parat | |

**Residence Information (Select One)** ◉ US Residency ○ Non US Residency ○ Active US Military Service

PTO/AIA/14 (02-18)
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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

| **City** | Palo Alto | **State/Province** | CA | **Country of Residence** | US |
|---|---|---|---|---|---|

**Mailing Address of Inventor:**

| **Address 1** | 4177 Hubbartt Drive | | |
|---|---|---|---|
| **Address 2** | | | |
| **City** | Palo Alto | **State/Province** | CA |
| **Postal Code** | 94306 | **Country** | US |

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

## Correspondence Information:

**Enter either Customer Number or complete the Correspondence Information section below.**
**For further information see 37 CFR 1.33(a).**

☐ **An Address is being provided for the correspondence Information of this application.**

| **Customer Number** | 128753 | | |
|---|---|---|---|
| **Email Address** | docketing@wellsstjohn.com | Add Email | Remove Email |

## Application Information:

| **Title of the Invention** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | | |
|---|---|---|---|
| **Attorney Docket Number** | MI22-6502 | **Small Entity Status Claimed** | ☐ |
| **Application Type** | Nonprovisional | | |
| **Subject Matter** | Utility | | |
| **Total Number of Drawing Sheets (if any)** | 18 | **Suggested Figure for Publication (if any)** | |

## Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

| Application number of the previously filed application | Filing date (YYYY-MM-DD) | Intellectual Property Authority or Country |
|---|---|---|
| | | |

## Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

## Representative Information:

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| Please Select One: | (●) Customer Number | ( ) US Patent Practitioner | ( ) Limited Recognition (37 CFR 11.9) |
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## Domestic Benefit/National Stage Information:

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When referring to the current application, please leave the "Application Number" field blank.

| Prior Application Status | Pending | | Remove |
|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing or 371(c) Date (YYYY-MM-DD) |
| | Continuation of | 15397919 | 2017-01-04 |

| Prior Application Status | Patented | | | | Remove |
|---|---|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 15397919 | Continuation of | 15095208 | 2016-04-11 | 9564471 | 2017-02-07 |

| Prior Application Status | Patented | | | | Remove |
|---|---|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 15095208 | Division of | 14602559 | 2015-01-22 | 9318430 | 2016-04-19 |

| Prior Application Status | Patented | | | | Remove |
|---|---|---|---|---|---|
| Application Number | Continuity Type | Prior Application Number | Filing Date (YYYY-MM-DD) | Patent Number | Issue Date (YYYY-MM-DD) |
| 14602559 | Division of | 13085083 | 2011-04-12 | 8945996 | 2015-02-03 |

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

## Foreign Priority Information:

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

| Application Number | Country[i] | Filing Date (YYYY-MM-DD) | Access Code[i] (if applicable) |
|---|---|---|---|
| | | | |

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

## Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Approved for use through 11/30/2020. OMB 0651-0032
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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

## Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

**NOTE**: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

**1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)**

**A. Priority Document Exchange (PDX)** - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

**B. Search Results from U.S. Application to EPO** - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

**2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)**

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

**NOTE:** Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (02-18)
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| Application Data Sheet 37 CFR 1.76 | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

## Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

**Applicant 1**

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

| | | |
|---|---|---|
| ◉ Assignee | ○ Legal Representative under 35 U.S.C. 117 | ○ Joint Inventor |
| ○ Person to whom the inventor is obligated to assign. | ○ Person who shows sufficient proprietary interest | |

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

| Organization Name | Micron Technology, Inc. |
|---|---|

**Mailing Address Information For Applicant:**

| | | | |
|---|---|---|---|
| **Address 1** | MS 1-525 | | |
| Address 2 | 8000 South Federal Way | | |
| **City** | Boise | **State/Province** | ID |
| **Country** | US | Postal Code | 83716 |
| Phone Number | 208-368-4505 | Fax Number | 208-368-5606 |
| Email Address | docketing@wellsstjohn.com | | |

Additional Applicant Data may be generated within this form by selecting the Add button.

## Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

**Assignee 1**

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

| Organization Name | Micron Technology, Inc. |
|---|---|

**Mailing Address Information For Assignee including Non-Applicant Assignee:**

| **Address 1** | MS 1-525 | | |
|---|---|---|---|
| Address 2 | 8000 South Federal Way | | |
| **City** | Boise | **State/Province** | ID |
| **Country** i | US | Postal Code | 83716 |
| Phone Number | 208-368-4505 | Fax Number | 208-368-5606 |
| Email Address | docketing@wellsstjohn.com | | |

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

## Signature:

**NOTE:** This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

| **Signature** | /Mark S. Matkin/ | | | Date (YYYY-MM-DD) | 2018-02-20 |
|---|---|---|---|---|---|
| First Name | Mark S. | Last Name | Matkin | Registration Number | 32,268 |

Additional Signature may be generated within this form by selecting the Add button.

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Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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| **Application Data Sheet 37 CFR 1.76** | Attorney Docket Number | MI22-6502 |
|---|---|---|
| | Application Number | |
| Title of Invention | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | |

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

# Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .....Filed Herewith
Filing Date .....Filed Herewith
Confirmation No. .....Unknown
Inventor.....Sanh D. Tang
Assignee .....Micron Technology, Inc.
Group Art Unit .....Unknown
Examiner .....Unknown
Attorney's Docket No. ..... MI22-6502
Title:....Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

**RESCISSION OF ANY PRIOR DISCLAIMERS AND REQUEST TO REVISIT ART**

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Mark S. Matkin
(Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 W. Main Avenue, Suite 600
Spokane, WA 99201-3828

The claims of the present application may be different and may be possibly broader in scope than the claims pursued in one or more related applications. To the extent any prior amendments and/or characterizations of the scope of any previous claim and/or referenced art could be construed as a disclaimer of any claimed subject matter of the present application, Applicant hereby rescinds and retracts any and all such disclaimer(s) to facilitate full prosecution on the merits of the claims of the present application. Accordingly, the references previously considered in the related application(s) may need to be revisited.

No fee is believed due by the filing of this document. Please charge any additional fees to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: February 20, 2018

By: /Mark S. Matkin/
Mark S. Matkin
Reg. No. 32,268

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .....Filed Herewith
Filing Date .....Filed Herewith
Confirmation No. .....Unknown
Inventor.....Sanh D. Tang
Assignee .....Micron Technology, Inc.
Group Art Unit .....Unknown
Examiner .....Unknown
Attorney's Docket No. ..... MI22-6502
Title:....Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

**INFORMATION DISCLOSURE STATEMENT**
**PURSUANT TO 37 CFR §§ 1.56, 1.97 AND 1.98**

In compliance with 37 CFR §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO/SB/08. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a continuation application of co-pending application Serial No. 15/397,919, filed January 4, 2017. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 CFR § 1.98 and MPEP § 609.02. Citation of these references is respectfully requested.

Respectfully submitted,

Dated: February 20, 2018 By: /Mark S. Matkin/
Mark S. Matkin
Reg. No. 32268

PTO/SB/08a (07-09)
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Substitute for form 1449A/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

Sheet 1 of 2

| *Complete if Known* | |
|---|---|
| **Application Number** | Filed Herewith |
| **Filing Date** | February 20, 2018 |
| **First Named Inventor** | Sanh D. Tang |
| Art Unit | Unknown |
| Examiner Name | Unknown |
| Attorney Docket Number | MI22-6502 |

## U.S. PATENT DOCUMENTS

| Examiner initial * | Cite No. | Document Number<br>Number - Kind Code [2] (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
| | 1 | US-2006/0148171 | 07-06-2006 | Lee | |
| | 2 | US-2009/0309152 | 12-17-2009 | Knoefler et al. | |
| | 3 | US-2011/0199804 | 08-18-2011 | Son | |
| | 4 | US-2012/0003831 | 01-05-2012 | Kang et al. | |
| | 5 | US-2012/0052674 | 03-01-2012 | Lee et al. | |
| | 6 | US-2014/0106569 | 04-17-2014 | Oh et al. | |
| | 7 | US-2014/0162420 | 06-12-2014 | Oh et al. | |
| | 8 | US-2014/0179068 | 06-26-2014 | Samachisa | |
| | 9 | US-5,414,285 | 05-09-1995 | Nishihara | |
| | 10 | US-6,023,099 | 02-08-2000 | Komuro | |
| | 11 | US-6,472,735 | 10-29-2002 | Isaak | |
| | 12 | US-7,446,038 | 11-04-2008 | Jeng | |
| | 13 | US-9,034,710 | 05-19-2015 | Sills | |
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## FOREIGN PATENT DOCUMENTS

| Examiner Initial * | Cite No. [1] | Foreign Patent Document<br>Country [3] Code Number [4] Kind Code (if known) [5] | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, columns, Lines, Where Relevant Passages or Relevant Figures Appear | T |
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| Examiner Signature | | Date Considered | |
|---|---|---|---|

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not Considered. Include copy of this form with next communication to applicant. 1. Applicant's unique citation design number (optional). 2 See Kinds Codes of USPTO patent Documents. at www.uspto.gov or MPEP 901.04. 3. Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). 4. For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. 5. Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. 6. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

**SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/SB/08b (07-09)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449B/PTO

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

*(Use as many sheets as necessary)*

Sheet 2 of 2

| *Complete if Known* | |
|---|---|
| **Application Number** | Filed Herewith |
| **Filing Date** | February 20, 2018 |
| **First Named Inventor** | Sanh D. Tang |
| Art Unit | Unknown |
| Examiner Name | Unknown |
| Attorney Docket Number | MI22-6502 |

**NON PATENT LITERATURE DOCUMENTS**

| Examiner initial * | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
| | 14 | Katsumata et al., "Pipe-shaped BiCS Flash Memory with 16 Stacked Layers and Multi-Level-Cell Coperation for Ultra High Density Storage Devices", Toshiba Corporation, 2009 Symposium on VLSI Technology Digest of Technical Papers, pp. 136-137. | |
| | 15 | Komori et al., "Disturbless Flash Memory due to High Boost Efficiency on BiCS Structure and Optimal Memory Film Stack for Ultra High Density Storage Device", Center for Semiconductor Research & Development, Toshiba Coporation, IEEE, 2008, pp. 851-854. | |
| | 16 | Niklaus et al., "Wafer-Level 3D Integration Technology Platforms for ICs and MEMS", Research Paper, Center for Integrated Institute, Rennsselaer Polytechnic Institute (RPI); 1/2005; 8pp. | |
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| | | | |
| | | | |
| | | | |

| Examiner Signature | | Date Considered | |
|---|---|---|---|

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1. Applicants unique citation designation number. (optional) 2. Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Cheif Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.

**SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assisstance in completing the form, call 1-800-PTO-9199 and select option 2.*

| | | |
|---|---|---|
| First Named Inventor | Sanh D. Tang | DECLARATION FOR UTILITY PATENT APPLICATION (37 CFR § 1.63) USING AN APPLICATION DATA SHEET (37 CFR § 1.76) |
| Serial No. | Filed Herewith | |
| Filing Date | Filed Herewith | |
| Group Art Unit | Unknown | |
| Examiner Name | Unknown | |
| Confirmation No. | Unassigned | |
| Attorney Docket No. | MI22-5729 | |
| Title: Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | | |

Micron Ref. No. 2010-0763.01/US
As a below named inventor, I hereby declare that this declaration is directed to the application identified by Attorney Docket No. MI22-5729 filed in the name of the following inventors:

Sanh D. Tang
Roger W. Lindsay
Krishna K. Parat

The above-identified application was made or authorized to be made by me.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Direct all correspondence to the address associated with Customer No. 128753.

Signature: Krishna P. Date: 12/30/2014

Full Name of inventor: Krishna K. Parat
Mailing Address: 4177 Hubbartt Drive
Residence: Palo Alto CA 94306

| | | |
|---|---|---|
| First Named Inventor | Sanh D. Tang | DECLARATION FOR UTILITY PATENT APPLICATION (37 CFR § 1.63) USING AN APPLICATION DATA SHEET (37 CFR § 1.76) |
| Serial No. | Filed Herewith | |
| Filing Date | Filed Herewith | |
| Group Art Unit | Unknown | |
| Examiner Name | Unknown | |
| Confirmation No. | Unassigned | |
| Attorney Docket No. | MI22-5729 | |
| Title: Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | | |

Micron Ref. No. 2010-0763.01/US
As a below named inventor, I hereby declare that this declaration is directed to the application identified by Attorney Docket No. MI22-5729 filed in the name of the following inventors:

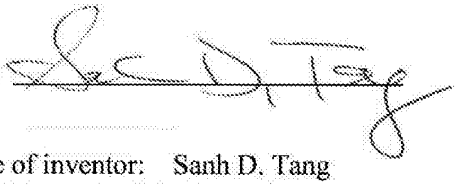
Sanh D. Tang
Roger W Lindsay
Krishna K. Parat

The above-identified application was made or authorized to be made by me.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Direct all correspondence to the address associated with Customer No. 128753.

Signature:  Date: 01-14-2015

Full Name of inventor: Sanh D. Tang
Mailing Address: 11587 W. Verde Drive
Residence: Boise, Idaho 83709

| | | |
|---|---|---|
| First Named Inventor | Sanh D. Tang | DECLARATION FOR UTILITY PATENT APPLICATION (37 CFR § 1.63) USING AN APPLICATION DATA SHEET (37 CFR § 1.76) |
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| Attorney Docket No. | MI22-5729 | |
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Direct all correspondence to the address associated with Customer No. 128753.

Signature: Roger W Lindsay Date: 1-14-15

Full Name of inventor: Roger W Lindsay
Mailing Address: 4376 Falconcrest Way
Residence: Boise, Idaho 83716

| Electronic Patent Application Fee Transmittal | | | | | |
|---|---|---|---|---|---|
| **Application Number:** | | | | | |
| **Filing Date:** | | | | | |
| **Title of Invention:** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells | | | | |
| **First Named Inventor/Applicant Name:** | Sanh D. Tang | | | | |
| **Filer:** | Mark S. Matkin/Bridget Wiseman | | | | |
| **Attorney Docket Number:** | MI22-6502 | | | | |
| Filed as Large Entity | | | | | |
| **Filing Fees for Utility under 35 USC 111(a)** | | | | | |
| **Description** | | **Fee Code** | **Quantity** | **Amount** | **Sub-Total in USD($)** |
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| UTILITY APPLICATION FILING | | 1011 | 1 | 300 | 300 |
| UTILITY SEARCH FEE | | 1111 | 1 | 660 | 660 |
| UTILITY EXAMINATION FEE | | 1311 | 1 | 760 | 760 |
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| **Claims:** | | | | | |
| CLAIMS IN EXCESS OF 20 | | 1202 | 2 | 100 | 200 |
| INDEPENDENT CLAIMS IN EXCESS OF 3 | | 1201 | 2 | 460 | 920 |
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| Description | Fee Code | Quantity | Amount | Sub-Total in USD($) |
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| Petition: | | | | |
| Patent-Appeals-and-Interference: | | | | |
| Post-Allowance-and-Post-Issuance: | | | | |
| Extension-of-Time: | | | | |
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| **Confirmation Number:** | 1775 |
| **Title of Invention:** | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells |
| **First Named Inventor/Applicant Name:** | Sanh D. Tang |
| **Customer Number:** | 128753 |
| **Filer:** | Mark S. Matkin/Bridget Wiseman |
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## File Listing:

| Document Number | Document Description | File Name | File Size(Bytes)/ Message Digest | Multi Part /.zip | Pages (if appl.) |
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| 1 | | ParentSpecification.pdf | 131103<br>86ffcc4e8bf97cc089f0c91a5986a4933db989b3 | yes | 30 |
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| | Specification | | 1 | 20 | |
| | Claims | | 21 | 29 | |
| | Abstract | | 30 | 30 | |
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| | Preliminary Amendment | | 1 | 1 | |
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**If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.**

**National Stage of an International Application under 35 U.S.C. 371**

**If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.**

**New International Application Filed with the USPTO as a Receiving Office**

**If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

# APPLICATION FOR LETTERS PATENT

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Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells

* * * * *

INVENTORS:

Sanh D. Tang
Roger W. Lindsay
Krishna K. Parat

ATTORNEY'S DOCKET NO. MI22-4725

# STACK OF HORIZONTALLY EXTENDING AND VERTICALLY OVERLAPPING FEATURES, METHODS OF FORMING CIRCUITRY COMPONENTS, AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS

## TECHNICAL FIELD

**[0001]** Embodiments disclosed herein pertain to stacks of horizontally extending and vertically overlapping features, and to methods of forming circuitry components and to methods of forming an array of memory cells.

## BACKGROUND

**[0002]** Integrated circuits are often formed on a semiconductor substrate such as a silicon wafer or other semiconductive material. In general, layers of various materials which are semiconductive, conductive, or electrically insulative are utilized to form the integrated circuits. By way of examples, the various materials may be doped, ion implanted, deposited, etched, grown, etc. using various processes. A continuing goal in semiconductive processing is to strive to reduce the size of individual circuitry components, thereby enabling smaller and denser integrated circuitry.

**[0003]** Memory is one type of integrated circuitry, and is used in computer systems for storing data. Such is usually fabricated in one or more arrays of individual memory cells. The memory cells might be volatile, semi-volatile, or nonvolatile. Nonvolatile memory cells can store data for extended periods of time, in many instances including when the computer is turned off. Volatile memory dissipates and therefore requires being refreshed/rewritten, in many instances multiple times per second. Regardless, the smallest unit in each array is termed as a memory cell and is configured to store data as one of at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store data as one of more than two selectable states.

**[0004]** Integrated circuitry fabrication continues to strive to produce smaller and denser integrated circuits. Accordingly, the fewer components an individual circuit device has, the smaller the construction of the finished device can be. A simple memory cell will be comprised of two conductive electrodes having a programmable material there-between. The programmable material is selected or designed to be configured in a selected one of at least two different physical memory states to enable storing of information by an individual memory cell. The reading of the cell comprises determination of which of the states the programmable material is in, and the writing of information to the cell comprises placing the programmable material in a target memory state. Some programmable materials retain a memory state in the absence of refresh, and thus may be incorporated into nonvolatile memory cells.

**[0005]** Some programmable materials may contain mobile charge carriers larger than electrons and holes, for example ions in some example applications. Regardless, the programmable materials may be converted from one memory state to another by moving the mobile charge carriers to alter a distribution of charge density within the programmable materials. Some example memory devices that utilize ions as mobile charge carriers are resistive RAM (RRAM) cells, which can include classes of memory cells containing multivalent oxides, and which can include memristors in some specific applications. Other example memory devices that utilize ions as charge carriers are programmable metallization cells (PMCs); which may be alternatively referred to as a conductive bridging RAM (CBRAM), nanobridge memory, or electrolyte memory.

**[0006]** The RRAM cells may contain programmable material sandwiched between a pair of electrodes. The programming of the RRAM cells may comprise transitioning the programmable material between first a memory state in which charge density is relatively uniformly dispersed throughout the material and a second memory state in which the charge density is concentrated in a specific region of the material (for instance, a region closer to one electrode than the other).

**[0007]** A PMC may similarly have programmable material sandwiched between a pair of current conductive electrodes. The PMC programmable material comprises ion conductive material, for example a suitable chalcogenide or any of various suitable oxides. A suitable voltage applied across the electrodes generates current conductive super-ionic clusters or filaments. Such result from ion transport through the ion conductive material which grows the clusters/filaments from one of the electrodes (the cathode), through the ion conductive material, and toward the other electrode (the anode). The clusters or filaments create current conductive paths between the electrodes. An opposite voltage applied across the electrodes essentially reverses the process and thus removes the current conductive paths. A PMC thus comprises a high resistance state (corresponding to the state lacking a current conductive filament or clusters between the electrodes) and a low resistance state (corresponding to the state having a current conductive filament or clusters between the electrodes), with such states being reversibly interchangeable with one another.

**[0008]** Another type of nonvolatile memory is known as flash memory, a type of EEPROM (electrically-erasable programmable read-only memory) that may be erased and reprogrammed in groups. A typical flash memory array includes a large number of nonvolatile memory cells usually grouped into blocks. Each of the cells within a block may be electrically programmed by charging its programmable gate material. The charge may be removed from the programmable gate material by a block erase operation. NAND is a basic architecture of flash memory. A NAND architecture comprises at least one select gate coupled in series to a serial combination of memory cells (with the serial combination being commonly referred to as a NAND string).

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]** Fig. 1 is a diagrammatic oblique view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

**[0010]** Fig. 2 is a view of the Fig. 1 substrate at a processing step subsequent to that shown by Fig. 1.

**[0011]** Fig. 3 is a view of the Fig. 2 substrate at a processing step subsequent to that shown by Fig. 2.

**[0012]** Fig. 4 is a view of the Fig. 3 substrate at a processing step subsequent to that shown by Fig. 3.

**[0013]** Fig. 5 is a view of the Fig. 4 substrate at a processing step subsequent to that shown by Fig. 4.

**[0014]** Fig. 6 is an end view of Fig. 5 relative to line 6-6 in Fig. 5.

**[0015]** Fig. 7 is a view of the Fig. 5 substrate wherein certain material in Fig. 5 is not shown in Fig. 7 solely for clarity.

**[0016]** Fig. 8 is an end view of Fig. 7 relative to line 8-8 in Fig. 7.

**[0017]** Fig. 9 is a view of the Fig. 7 substrate at a processing step subsequent to that shown by Fig. 7.

**[0018]** Figs. 10 is a view of the Fig. 9 substrate wherein certain material in Fig. 9 is not shown in Fig. 10 solely for clarity.

**[0019]** Fig. 11 is a view of the Fig. 9 substrate at a processing step subsequent to that shown by Fig. 9.

**[0020]** Fig. 11A is an enlarged view of a portion of Fig. 11.

**[0021]** Fig. 12 is view of the Fig. 11 substrate wherein certain material in Fig. 11 is not shown in Fig. 12 solely for clarity.

**[0022]** Fig. 13 is a view of the Fig. 12 substrate at a processing step subsequent to that shown by Fig. 12.

**[0023]** Fig. 14 is a diagrammatic perspective view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

**[0024]** Fig. 15 is a view of the Fig. 14 substrate at a processing step subsequent to that shown by Fig. 14.

**[0025]** Fig. 16 is a view of the Fig. 15 substrate at a processing step subsequent to that shown by Fig. 15.

**[0026]** Fig. 17 is a view of the Fig. 16 substrate at a processing step subsequent to that shown by Fig. 16.



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## DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

**[0027]** Example embodiments in accordance with the invention of methods of forming circuitry components are initially described with reference to Figs. 1-10. In some embodiments, an array of memory cells may be fabricated, for example as described with reference to Figs. 1-13 and with reference to Figs. 14-17. In one embodiment, such may comprise cross-point memory cells (e.g., as shown in Fig. 17), and in one embodiment may comprise NAND circuitry (e.g., as shown in Figs. 11, 11A, 12, and 13).

**[0028]** Referring to Fig. 1, a substrate fragment 10 comprises a suitable base substrate 13 over which various materials have been provided. Base substrate 13 may be homogenous or non-homogenous, for example comprising multiple different composition materials and/or layers. As examples, such may comprise bulk monocrystalline silicon and/or a semiconductor-on-insulator substrate. As an additional example, such may comprise dielectric material having contacts (e.g., conductive vias) formed therein which extend vertically or otherwise into communicative contact (e.g., current conductive electrical connection) with device components, regions, or material that is elevationally inward of the dielectric material. In this document, vertical is a direction generally orthogonal to a primary surface relative to which the substrate is processed during fabrication and which may be considered to define a generally horizontal direction. Further, "vertical" and "horizontal" as used herein are generally perpendicular directions relative one another independent of orientation of the substrate in three-dimensional space. Further in this document, "elevational" and "elevationally" are with reference to the vertical direction from a base substrate upon which the circuitry is fabricated.

**[0029]** The base substrate may or may not be a semiconductor substrate. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in

assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

**[0030]** In one embodiment, substrate 10 comprises a stack of alternating sacrificial material 12 and dielectric material 14 formed over base substrate 13. Each material 12 and 14 may be homogenous or non-homogenous. In one embodiment, the respective sacrificial materials 12 are of the same composition relative one another. In one embodiment, the respective dielectric materials 14 are of the same composition relative one another. Regardless, sacrificial material 12 may be selectively etchable, in one embodiment highly selectively etchable, relative to dielectric material 14. In the context of this document, a “selective” etch requires removal of the stated one material relative to another at a rate of at least 1.5:1, and a highly selective etch at a rate of at least about 10:1. Sacrificial material 12 may be any one or more of conductive (e.g., current conductive), dielectric, or semiconductive. By way of an example only, dielectric material 14 may comprise silicon dioxide (whether doped or un-doped), and an example sacrificial material is a conductive or insulative nitride, for example titanium nitride or silicon nitride, respectively. A dielectric material 16 and a hardmask 18 have been provided outwardly of alternating materials 12, 14. Each material 16 and 18 may be homogenous or non-homogenous. Dielectric material 16 may be of the same composition as dielectric material 14, and hardmask material 18 may be of the same composition as sacrificial material 12. Fig. 1 depicts vertical tiers of three sacrificial materials 12 with two alternating dielectric materials 14. Additional alternating pairs of sacrificial and dielectric materials may be provided elevationally inward of innermost sacrificial material 12 or elevationally outward of outermost sacrificial material 12.

**[0031]** Stack of alternating materials 12, 14 may be considered as comprising a primary portion 18 and an end portion 20. The end portion in the depicted embodiment has been patterned to form a stair step-like construction. Such may be formed to provide horizontal area for later forming contacts to components,

regions, or material in end portion 20 as will be apparent in the continuing discussion. In one embodiment and as shown, end portion 20 comprises individual stairs 21 which at least include sacrificial material 12.

**[0032]** In one embodiment, materials 12 and 14 may be features (e.g., plates), such as plates or features that are plate-like, whether continuously and/or discontinuously formed. In one embodiment, a method of forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping plates at least some of which increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Either of collective materials 12 or 14 may be considered in such example embodiment as comprising such plates, or materials 12 and 14 in combination in the depicted embodiment may be considered as such plates. In one embodiment, the horizontally extending and vertically overlapping plates are dielectric, for example plates 14 regardless of the composition of sacrificial material 12. In one embodiment, all of the plates increase in horizontal extent in the vertical inward direction in the end portion of the stack. For example in the embodiment of Fig. 1, either of collective plates 12 or collective plates 14 may be considered as plates all of which increase in horizontal extent progressing vertically inward in the end portion of the stack. Alternately, a composite of each immediately adjacent plate pairs 12, 14 may be considered as respective plates which increase in horizontal extent in the vertical inward direction in end portion 20 of the stack.

**[0033]** In one embodiment, primary portion 18 and end portion 20 comprise a portion of an array area 22 within which a plurality of memory cells will be fabricated. Logic circuitry (not shown) may be fabricated outside of the array area. Control and/or other peripheral circuitry (not shown) for operating the memory array may or may not fully or partially be within the array area, with an example array area as a minimum encompassing all of the memory cells of the given array/sub-array. Further, multiple sub-arrays might also be fabricated and operated

independently, in tandem, or otherwise relative one another. As used in this document, a "sub-array" may also be considered as an array.

**[0034]** Referring to Fig. 2, dielectric material has been formed over substrate 10 and planarized at least to the outermost surface of hardmask 18. The dielectric material may be homogenous or non-homogenous and, in one embodiment, may be of the same composition as that of material 14 and is so shown and designated in the figures.

**[0035]** Referring to Fig. 3, first openings 25 have been formed into primary portion 18 of the stack and second openings 27 have been formed into end portion 20 of the stack. Any openings which overlap the primary and end portions may be such first or second openings (i.e., as primary portion openings or end portion openings), with example such openings being shown in Fig. 3 and designated as second openings 27. Openings 25, 27 may be formed through each plate 12, 14. An example technique for forming openings 25, 27 is by photolithographic patterning followed by subtractive anisotropic etching. First openings 25 need not be of the same shape and/or density relative one another. Second openings 27 need not be of the same shape and/or density relative one another, or relative to any one or more of first openings 25. As examples, openings 25 and 27 may be formed to have the same horizontal and vertical cross sections (not shown). Alternately, openings 25 and 27 may be formed to have at least one of different horizontal cross sections (as shown) or different vertical cross sections (as shown). Further and regardless, openings 25 and 27 may be formed at the same time or at different times, and/or may use the same masking step or different masking steps where, for example, photolithographic or other masking is used. In one embodiment and as shown, at least some of openings 27 in end portion 20 are formed to horizontally overlap ends of individual plates 12 and/or 14.

**[0036]** At least one of conductive material, semiconductive material, and programmable material is/are deposited into the openings. In one embodiment where conductive material is deposited into the openings, such may comprise

current conductive material. In the context of this document, current conductive material can include a composition where electric current flow may inherently occur therein predominantly by movement of subatomic positive and/or negative charges when such are generated as opposed to predominantly by movement of ions. Example current conductive materials are elemental metals, alloys of elemental metals, current conductive metal compounds, and conductively doped semiconductive material, including any combinations thereof.

**[0037]** In one embodiment, the depositing of the conductive material, semiconductive material and/or programmable material occurs simultaneously into all of the openings in the primary portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in the end portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in both of the primary and end portions. Operative structures (e.g., circuit components, such as local vertical extensions) are formed therewith within the openings in the primary portion, and dummy structures (e.g. dummy vertical extensions) are formed therewith within the openings in the end portion. In the context of this document, a "dummy" structure is a structure which is used to mimic a physical property of another structure (e.g., load carrying ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive). Openings in which dummy structures are formed may be considered as "dummy openings".

**[0038]** For example referring to Fig. 4, a material 30 has been deposited within openings 25, 27, and then planarized back through hardmask material 18 (not shown). An example thickness for material 30 is from about 100 to about 150 Angstroms. Material 30 may be homogenous or non-homogenous, and may comprise one or more of conductive material (e.g., current conductive material), semiconductive material, and programmable material. In one embodiment, material 30 comprises semiconductive material. Further in such embodiment, the semiconductive material may comprise interconnected channels of a plurality of

vertically oriented transistors, and in one embodiment comprises interconnected channels of vertically oriented charge storage transistors as will be apparent from the continuing discussion. Regardless, in one embodiment, material 30 may form operative structures 31 (e.g., operative circuit components 31) within primary portion openings 25 and form dummy structures 32 (e.g., dummy circuit components) within end portion openings 27. In one embodiment and as shown, such operative structures 31 and dummy structures 32 are in the form of hollow cylinders. Alternately by way of example, such may be in the form of laterally solid pillars (not shown in Fig. 4). Regardless, the above processing describes but examples of forming operative structures 31 vertically through plates 12 and/or 14 in primary portion 18 and forming dummy structures 32 vertically through plates 12 and/or 14 in end portion 20. In one embodiment, the operative and dummy structures may comprise the same material (as shown). In one embodiment, the operative and dummy structures may comprise a plurality of the same materials (not shown in Fig. 4), and in one such embodiment be arranged in the same lateral order relative one another in the operative and dummy structures. In one embodiment, the operative and dummy structures may consist essentially of the same material.

**[0039]** Referring to Figs. 5-8, horizontally elongated openings 34 (e.g., trenches) have been formed through plates 12 and/or 14, and laterally between material 30, to form horizontally elongated and vertically overlapping lines 36 from material of the plates. Lines 36 individually extend from primary portion 18 into end portion 20 and individually laterally about sides of vertically extending portions of both operative structures 31 and dummy structures 32. Figs. 7 and 8 are views of Figs. 5 and 6, respectively, wherein dielectric material 14 added in Fig. 2 is removed solely for clarity in such drawings. Where either of operative structures 31 or dummy structures 32 are upwardly open (e.g., as shown), such may be partially or wholly filled (not shown) with dielectric and/or other material prior to the forming of horizontally elongated openings 34.

**[0040]** Referring to Figs. 9 and 10, at least some of sacrificial material 12 that is elevationally between lines 36 within primary portion 18 and end portion 20 has been removed from being laterally between horizontally elongated openings 34. Such thereby, in one embodiment, forms void spaces 29 elevationally between vertically spaced horizontal dielectric lines 36. An example technique includes etching, for example isotropic dry and/or wet etching. Etching may be conducted selectively (ideally, highly selectively) relative to lines 36, operative structures 31, and dummy structures 32. Fig. 10 is a view of the Fig. 9 substrate wherein dielectric material 14 added in Fig. 2 is removed solely for clarity in such drawing.

**[0041]** The above processing discloses but example embodiments of forming circuitry components in accordance with some aspects of the invention. In one embodiment, a method of forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping features. By way of example only, such features may comprise plates, with the example depicted structure of plates 14 comprising but one example of such plates. Regardless, in such embodiment, the stack comprises a primary portion and an end portion wherein at least some of the features increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Operative structures 31 (e.g., circuit components) are formed vertically through the features in the primary portion and dummy structures 32 (e.g., dummy circuit components) are formed vertically through the features in the end portion. The processing depicted through Fig. 4, or through Figs. 5-8, are examples. The operative and dummy structures may comprise the same material, and in one embodiment may consist essentially of the same material. The dummy structures may support material of the features from vertical movement in the end portion while at least some of sacrificial material that is elevationally between the material of the features in the primary and end portions is removed. The processing depicted in going from that of Figs. 5-8 to that of Figs. 9 and 10 is but one such example processing. With respect to a prior art problem, dummy structures heretofore have not been provided in a stair-like end portion of an array.

Accordingly, the floors/ceilings that are vertically between the respective void spaces 29 in Figs. 9 and 10 may be sagged, bent, or broken during processing due to lack of support. In accordance with one embodiment of the invention, dummy structures in the end portion support the features (e.g., the respective ceilings and floors, or plates) from vertical movement, for example by laterally engaging side portions of such floors/ceilings that were created where such dummy structures extend there-through. Regardless, other attributes as described may be employed.

**[0042]** Additional processing may occur in fabricating integrated circuitry, for example in fabricating an array of memory cells as next described with reference to Figs. 11-13. Referring to Figs. 11 and 11A, material 40 has been isotropically deposited within horizontally elongated openings 34, former void spaces 29 (not shown in Figs. 11, 11A), and any remaining volume of openings 25, 27. Material 40 has subsequently been removed from horizontally elongated openings 34 to form vertically spaced horizontal conductive lines 42 within the void spaces elevationally between horizontal lines 36 of dielectric material 14. In one embodiment, conductive lines 42 collectively cross a row of the operative and dummy structures at different respective elevations. In one embodiment, individual structures 31, 32 cross different conductive lines at different respective elevations. In the depicted example, conductive lines 42 extend longitudinally straight linear. Alternately by way of example, some or all of lines 42 may not be straight linear, for example being longitudinally curvilinear (not shown). Material 40 may also be removed from the remaining internal volume of openings 25, 27 as shown. Fig. 12 depicts the circuitry of Fig. 11 wherein the dielectric material that is shown as being deposited in Fig. 2 is removed solely for clarity.

**[0043]** Figs. 11, 11A, and 12 depict but one example embodiment comprising NAND circuitry wherein operative structures 31 comprise interconnected channel regions of a NAND string. In such example embodiment, material 40 comprises a composite of a suitable tunnel dielectric 49 (Fig. 11A), floating gate/charge trapping material 48, dielectric 50, and conductive control gate material 52.

Thereby, conductive material 52 provides but an example conductive portion of conductive lines 42 that is within the void spaces between the horizontal lines of dielectric material, and which collectively cross a row of the operative and dummy structures at different respective elevations. Individual ones of the memory cells of the example circuitry of Figs. 11 and 11A comprise an intersection of an individual horizontal conductive line and an individual operative structure (e.g., in the form of a string of channels of NAND), and some of which are indicated with reference numeral 55.

**[0044]** In one embodiment, a respective contact may be formed to a stair extension of individual ones of horizontal conductive lines 42 in end portion 20 for making communicative connection to circuitry. One such example is diagrammatically shown in Fig. 13. The dielectric material 14 of Fig. 2 is again showed removed solely for clarity in depicting certain components. Specifically, Fig. 13 shows example individual contacts 60 (e.g, current conductive contacts) which may be formed through the dielectric material 14 (not shown) of Fig. 2 for making communicative connection to circuitry, such as that elevationally outward of that depicted by Fig. 13 with respect to each conductive line 42.

**[0045]** Circuitry components other than or in addition to components of memory cells may be fabricated in accordance with embodiments of the invention.

**[0046]** An example embodiment of a method of forming an array of cross-point memory cells is next described with reference to Figs. 14-17. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a" or with different numerals. Fig. 14 depicts an alternate embodiment substrate fragment 10a to that depicted by Fig. 4. In Fig. 14, openings 25, 27 have been lined with a first material 62. In one embodiment, such material is dielectric (i.e., a 15 to 30 Angstroms thick layer of undoped silicon dioxide). Thereafter, a programmable material 30 was deposited to line over first material 62 within openings 25, 27. Then, remaining volume of openings 25, 27 has been filled with conductive material 64, and materials 62, 30, and 64 planarized back to materials 14 and 16.

Horizontally elongated openings (not shown in Fig. 14) may then be formed analogous to the processing depicted by Figs. 5-8.

**[0047]** Programmable material 30 may be solid, gel, amorphous, crystalline, or any other suitable phase. Any existing or yet-to-be developed programmable material may be used, with only some examples being provided below.

**[0048]** One example programmable material is ion conductive material. Example suitable such materials comprise chalcogenide-type (for instance, materials comprising one or more of germanium, selenium, antimony, tellurium, sulfur, copper, etc.; with example chalcogenide-type materials being $Ge_2Sb_2Te_5$, $GeS_2$, $GeSe_2$, $CuS_2$, and CuTe) and/or oxides such as zirconium oxide, hafnium oxide, tungsten oxide, copper oxide, niobium oxide, iron oxide, silicon oxide (specifically, silicon dioxide), gadolinium oxide, etc. capable of inherently (or with additive) supporting electrolyte behavior. Such may have silver, copper, cobalt, and/or nickel ions, and/or other suitable ions, diffused therein for ionic conduction, analogously to structures disclosed in U.S. Patent No. 7,405,967 and U.S. Patent Publication Number 2010/0193758.

**[0049]** Additional example programmable materials include multi-resistive state metal oxide-comprising material. Such may comprise, for example, at least two different layers or regions generally regarded as or understood to be active or passive regions, although not necessarily. Alternately, such may only comprise active material. Example active cell region compositions which comprise metal oxide and can be configured in multi-resistive states include one or a combination of $Sr_xRu_yO_z$, $Ru_xO_y$, and $In_xSn_yO_z$. Other examples include MgO, $Ta_2O_5$, $SrTiO_3$, $SrZrO_3$, $BaTiO_3$, $Ba_{(1-x)}Sr_xTiO_3$, $ZrO_x$ (perhaps doped with La), and $CaMnO_3$ (doped with one or more of Pr, La, Sr, or Sm). Example passive cell region compositions include one or a combination of $Al_2O_3$, $TiO_2$, and $HfO_2$. Regardless, a programmable material composite might comprise additional metal oxide or other materials not comprising metal oxide. Example materials and constructions for a multi-resistive state region comprising one or more layers including a programmable metal oxide-comprising material are described and disclosed in U.S.

Patent Nos. 6,753,561; 7,149,108; 7,067,862; and 7,187,201, as well as in U.S. Patent Application Publication Nos. 2006/0171200 and 2007/0173019. Further as is conventional, multi-resistive state metal oxide-comprising materials encompass filament-type metal oxides, ferroelectric metal oxides and others, and whether existing or yet-to-be developed, as long as resistance of the metal oxide-comprising material can be selectively changed.

**[0050]** The programmable material may comprise memristive material. As an example, such material may be statically programmable semiconductive material which comprises mobile dopants that are received within a dielectric such that the material is statically programmable between at least two different resistance states. At least one of the states includes localization or gathering of the mobile dopants such that a dielectric region is formed and thereby provides a higher resistance state. Further, more than two programmable resistance states may be used. In the context of this document, a "mobile dopant" is a component (other than a free electron) of the semiconductive material that is movable to different locations within said dielectric during normal device operation of repeatedly programming the device between at least two different static states by application of voltage differential to the pair of electrodes. Examples include atom vacancies in an otherwise stoichiometric material, and atom interstitials. Specific example mobile dopants include oxygen atom vacancies in amorphous or crystalline oxides or other oxygen-containing material, nitrogen atom vacancies in amorphous or crystalline nitrides or other nitrogen-containing material, fluorine atom vacancies in amorphous or crystalline fluorides or other fluorine-containing material, and interstitial metal atoms in amorphous or crystalline oxides. More than one type of mobile dopant may be used. Example dielectrics in which the mobile dopants are received include suitable oxides, nitrides, and/or fluorides that are capable of localized electrical conductivity based upon sufficiently high quantity and concentration of the mobile dopants. The dielectric within which the mobile dopants are received may or may not be homogenous independent of consideration of the mobile dopants. Specific example dielectrics include $TiO_2$, AlN, and/or $MgF_2$. Example programmable materials that comprise oxygen vacancies as mobile

dopants may comprise a combination of $TiO_2$ and $TiO_{2-x}$ in at least one programmed resistance state depending on location of the oxygen vacancies and the quantity of the oxygen vacancies in the locations where such are received. An example programmable material that comprises nitrogen vacancies as mobile dopants is a combination of AlN and $AlN_{1-x}$ in at least one programmed state depending on location of the nitrogen vacancies and the quantity of the nitrogen vacancies in the locations where such are received. An example programmable material that comprises fluorine vacancies as mobile dopants may is a combination of $MgF_2$ and $MgF_{2-x}$ in at least one programmed resistance state depending on location of the fluorine vacancies and the quantity of the fluorine vacancies in the locations where such are received. As another example, the mobile dopants may comprise aluminum atom interstitials in a nitrogen-containing material.

**[0051]** Still other example programmable materials include polymer materials such as Bengala Rose, $AlQ_3Ag$, Cu-TCNQ, DDQ, TAPA, and fluorescine-based polymers.

**[0052]** Referring to Fig. 15, such corresponds in processing sequence to that of Fig. 9 of the above-described embodiments. Sacrificial material 12 (not shown) has been at least partially removed (e.g., by etching) between dielectric lines 36 in primary portion 18 and end portion 20 laterally between horizontally elongated openings 34. Material 12 may be etched selectively (ideally, highly selectively) relative to dielectric lines 36, first material lining 62, and conductive material 64 in openings 25, 27. Figs. 14 and 15 depict an example embodiment wherein the operative and dummy structures comprise a plurality of the same materials, and in such embodiment arranged in the same lateral order relative one another in the operative and dummy structures. Regardless, in one embodiment, first material lining 62 may serve as a protecting barrier from adverse exposure of programmable material 30 to the etching chemistry which etches the sacrificial material.

**[0053]** Referring to Fig. 16, at least a portion of first material 62 has been removed elevationally between dielectric lines 36 to expose laterally outer sidewalls of programmable material 30 that is elevationally between dielectric

lines 36. An example technique for doing so where material 62 comprises silicon dioxide includes etching with a dilute HF solution.

**[0054]** Referring to Fig. 17, at least a portion of sacrificial material 12 (not shown) of Fig. 14 has been replaced with conductor material 52 (e.g., current conductive material) that is in electrical connection with the laterally outer sidewalls of programmable material 30 and to comprise vertically spaced horizontal conductive lines 42a. Materials 64 and 52 may be of the same composition or of different compositions. Further and regardless, conductive material 64 within remaining volumes of openings 25, 27 alternately may be provided subsequent to the etching depicted by Fig. 15. Regardless, Fig. 17 also depicts conductor material 52 as having been at least partially removed from horizontally elongated openings 34 to form such vertically spaced horizontal conductive lines 42a.

**[0055]** Individual ones of the cross-point memory cells comprise crossing ones of the horizontal conductive lines in the primary portion and conductive material in the openings in the primary portion having the programmable material there-between, with some of such example memory cells being indicated with reference numeral 55 in the Fig. 17 example embodiment.

**[0056]** An embodiment of the invention includes a stack of horizontally extending and vertically overlapping features. The stack comprises a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures extend vertically through the features in the primary portion. Dummy structures extend vertically through the features in the end portion. In one embodiment, the features may be horizontally extending lines, for example formed of any one or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s). In one embodiment, the features comprise a combination of horizontally extending conductive and dielectric lines (e.g., overlapping and alternating such lines). In one embodiment, contacts may be in the end portion, for example extending vertically to the lines.

Any other attribute as described above may be used, for example as shown and described with respect to Figs. 1-13 and with respect to Figs. 14-17.

**[0057]** In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.



**YMTC EXHIBIT 1002**
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**CLAIMS:**

1. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and

removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.

2. The method of claim 1 wherein the operative and dummy structures comprise the same material.

3. The method of claim 2 wherein the operative and dummy structres comprise a plurality of the same materials.

4. The method of claim 3 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

5. The method of claim 2 wherein the operative and dummy structures consist essentially of the same material.

6. The method of claim 1 wherein the features comprise plates.

7. The method of claim 1 wherein the operative and dummy structures comprise programmable material.

8. The method of claim 1 wherein the operative and dummy structures comprise semiconductive material.

9. The method of claim 8 wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

10. The method of claim 9 wherein interconnected channels are of vertically oriented charge storage transistors.

11. The method of claim 1 wherein the operative and dummy structures comprise conductive material.



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12. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;

forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and

removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.

13. The method of claim 12 wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.

14. The method of claim 12 wherein the operative and dummy structures comprise hollow cylinders.

15. The method of claim 12 wherein the operative and dummy structures comprise laterally solid pillars.

16. The method of claim 12 wherein the features comprise plates.

17. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;

forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;

forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and

removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

18. The method of claim 17 comprising forming the primary portion openings and the end portion openings at the same time.

19. The method of claim 17 comprising forming the primary portion openings and the end portion openings at different times.

20. The method of claim 17 comprising forming at least some of the end portion openings horizontally overlap ends of individual ones of the features.

21. The method of claim 17 comprising forming the primary portion openings and the end portion openings to have the same horizontal and vertical cross sections.

22. The method of claim 17 comprising forming the primary portion openings and the end portion openings to have at least one of different horizontal cross sections or different vertical cross sections.

23. The method of claim 17 wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.

24. The method of claim 17 wherein the features comprise plates.



**YMTC EXHIBIT 1002**
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25. A method of forming an array of memory cells, comprising:

forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs;

forming a plurality of first openings into the primary portion of the stack;

forming a plurality of second openings into the end portion of the stack;

simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;

forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;

removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;

after the removing, forming conductive material into the horizontally elongated openings and the void spaces;

removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and

forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.

26. The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.

27. The method of claim 25 wherein the memory cells comprise cross-point memory cells and the at least one formed material comprises programmable material.

28. The method of claim 25 comprising forming the first and second openings using the same masking step.

29. The method of claim 25 comprising forming the first and second openings using different masking steps.

30. The method of claim 25 wherein the sacrificial material is dielectric.

31. The method of claim 25 wherein the sacrificial material is at least one of semiconductive and conductive.

32. The method of claim 25 wherein the features comprise plates.

33. A method of forming an array of cross-point memory cells, comprising:

forming a stack of horizontally extending and vertically overlapping dielectric features, the stack comprising a primary portion and an end portion, at least some of the dielectric features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming openings through the dielectric features in the primary portion and in the end portion;

lining the openings with first material;

lining the first material-lined openings with programmable material;

filling remaining volume of the first and programmable material-lined openings with conductive material;

forming horizontally elongated trenches through the dielectric features to form horizontally elongated and vertically overlapping dielectric lines from dielectric material of the dielectric features, the dielectric lines individually extending from the primary portion into the end portion and individually laterally about sides of both the openings in the primary and end portions;

removing at least some of sacrificial material that is elevationally between the dielectric lines in the primary and end portions laterally between the trenches selectively relative to the dielectric lines and the first material lining in the openings;

after removing at least a portion of the sacrificial material, removing at least a portion of the first material that is elevationally between the dielectric lines to expose laterally outer sidewalls of the programmable material that is elevationally between the dielectric lines; and

replacing at least a portion of the sacrificial material with conductor material that is in electrical connection with the laterally outers sidewalls of the programmable material and to comprise vertically spaced horizontal conductive lines; individual ones of the cross-point memory cells comprising crossing ones of the horizontal conductive lines in the primary portion and conductive material in

the openings in the primary portion having the programmable material therebetween.

34. The method of claim 33 comprising forming the trenches after the filling.

35. The method of claim 33 wherein the conductive material and the conductor material are of the same composition.

36. The method of claim 33 wherein the conductive material and the conductor material are of different compositions.

37. The method of claim 33 wherein the first material is dielectric.

38. The method of claim 33 wherein the features comprise plates.

39. A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion.

40. The stack of claim 39 further comprising contacts in the end portion.

41. The stack of claim 39 wherein the features comprise horizontally extending conductive lines.

## ABSTRACT OF THE DISCLOSURE

A method of forming circuitry components includes forming a stack of horizontally extending and vertically overlapping features. The stack has a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures are formed vertically through the features in the primary portion and dummy structures are formed vertically through the features in the end portion. Horizontally elongated openings are formed through the features to form horizontally elongated and vertically overlapping lines from material of the features. The lines individually extend from the primary portion into the end portion, and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures. Sacrificial material that is elevationally between the lines is at least partially removed in the primary and end portions laterally between the horizontally elongated openings. Other aspects and implementations are disclosed.

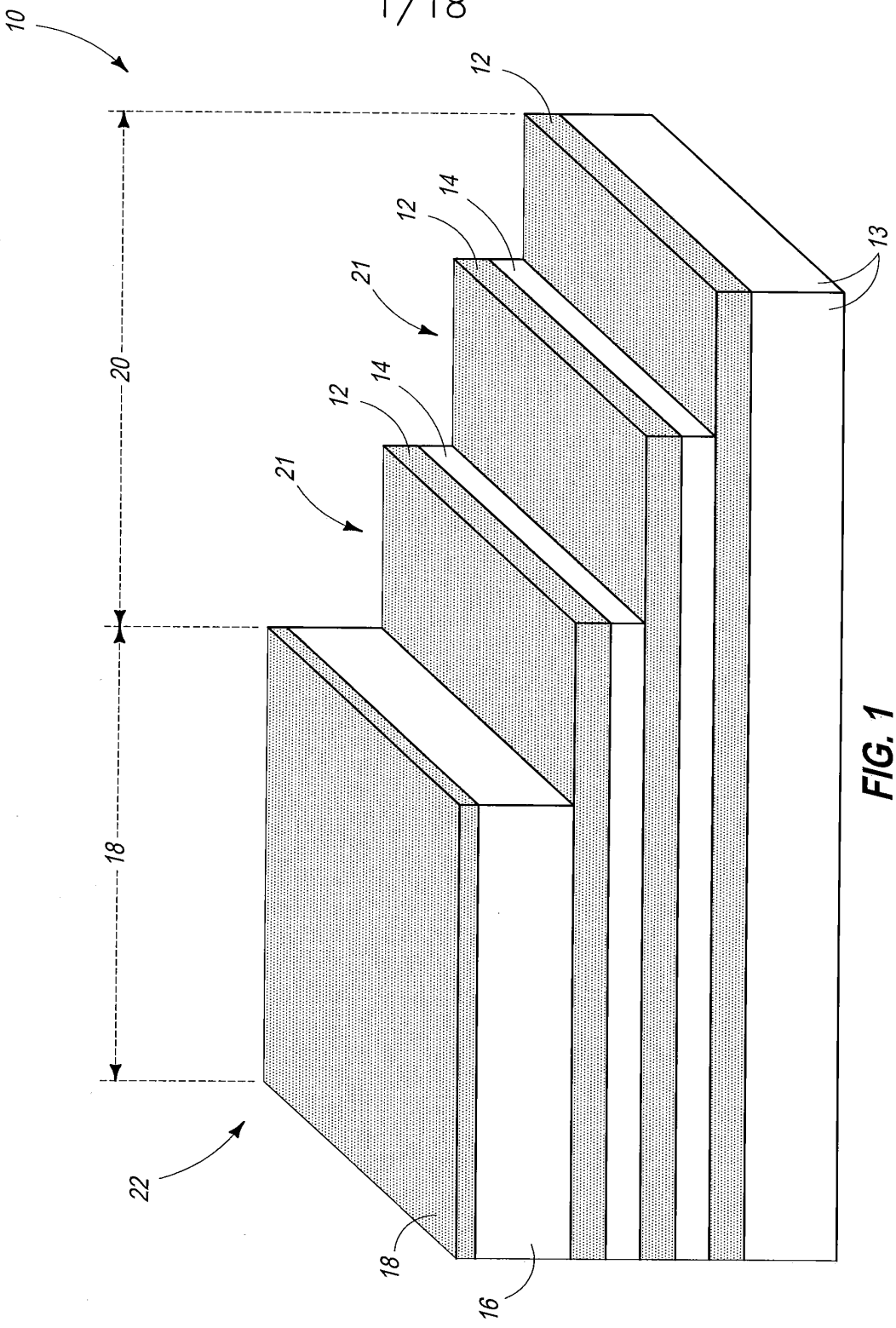



FIG. 1

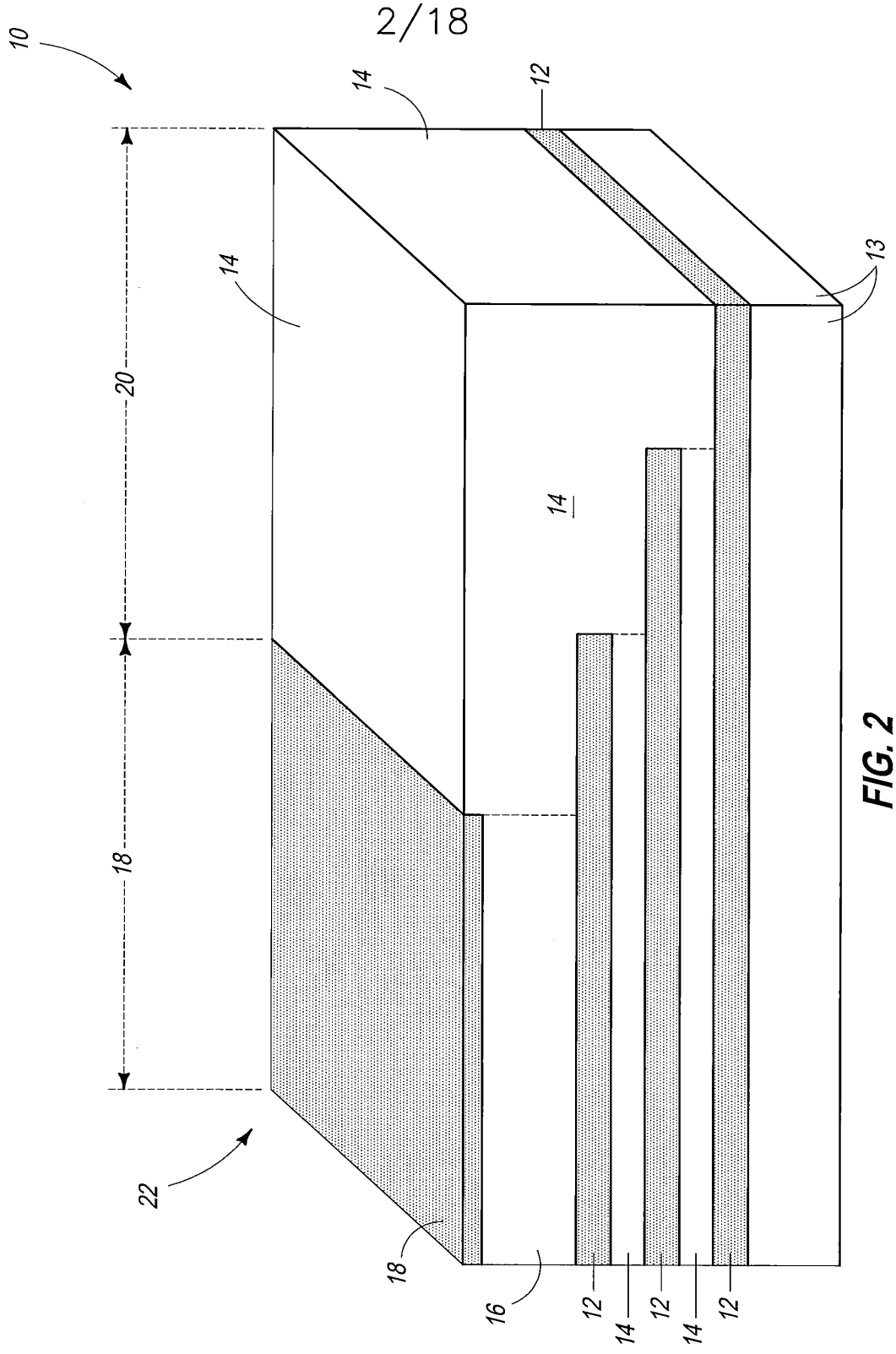
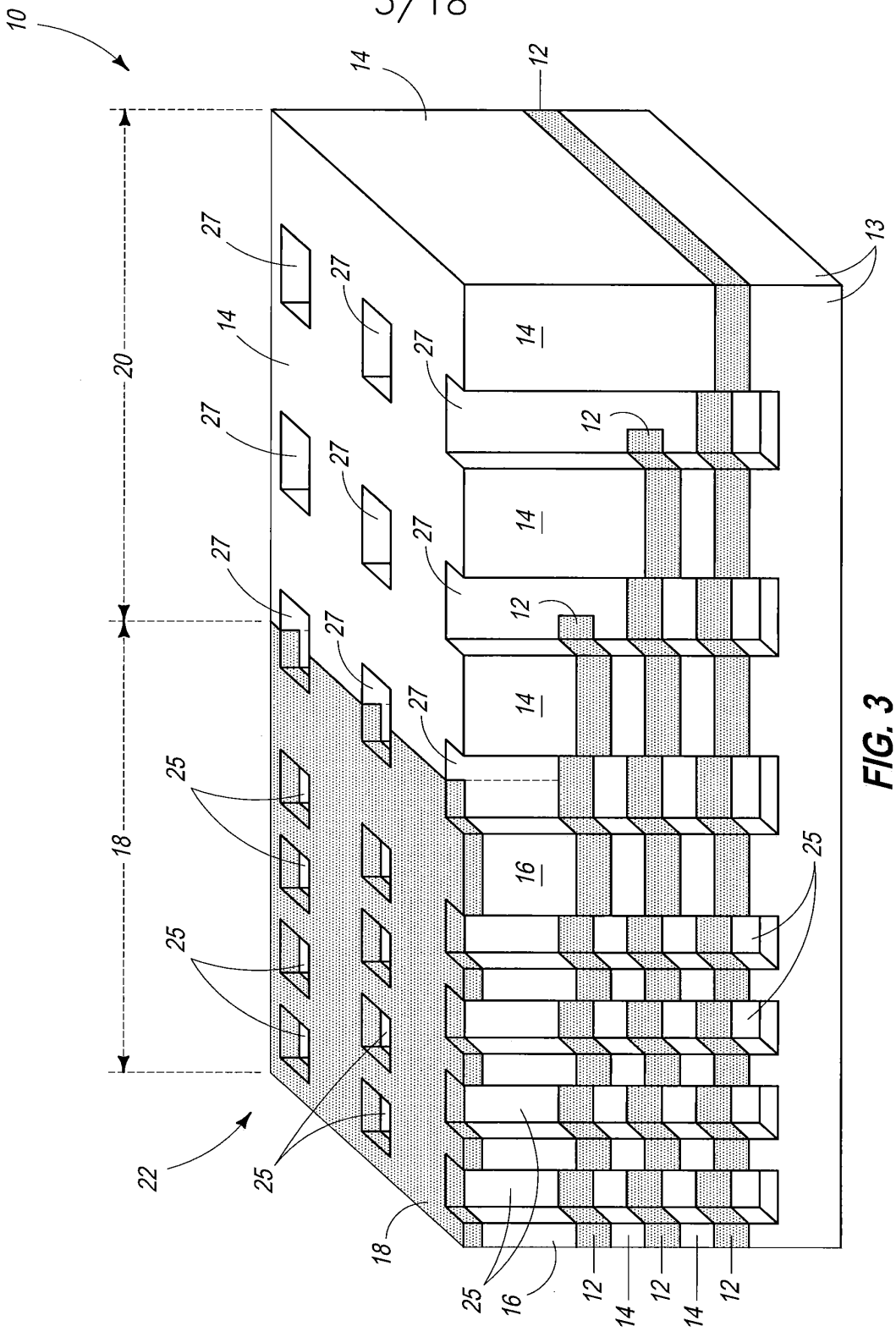



FIG. 2


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FIG. 3

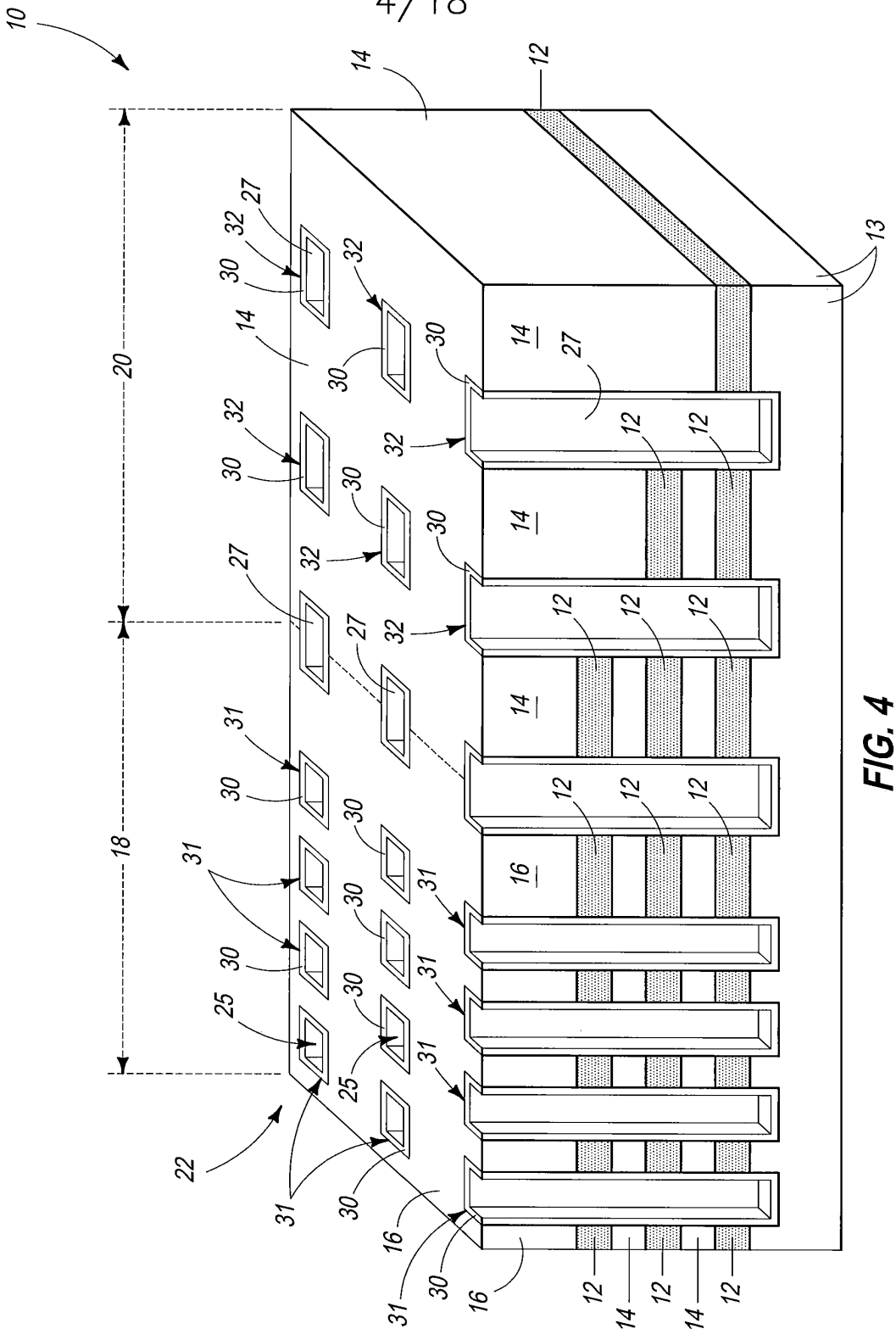



FIG. 4

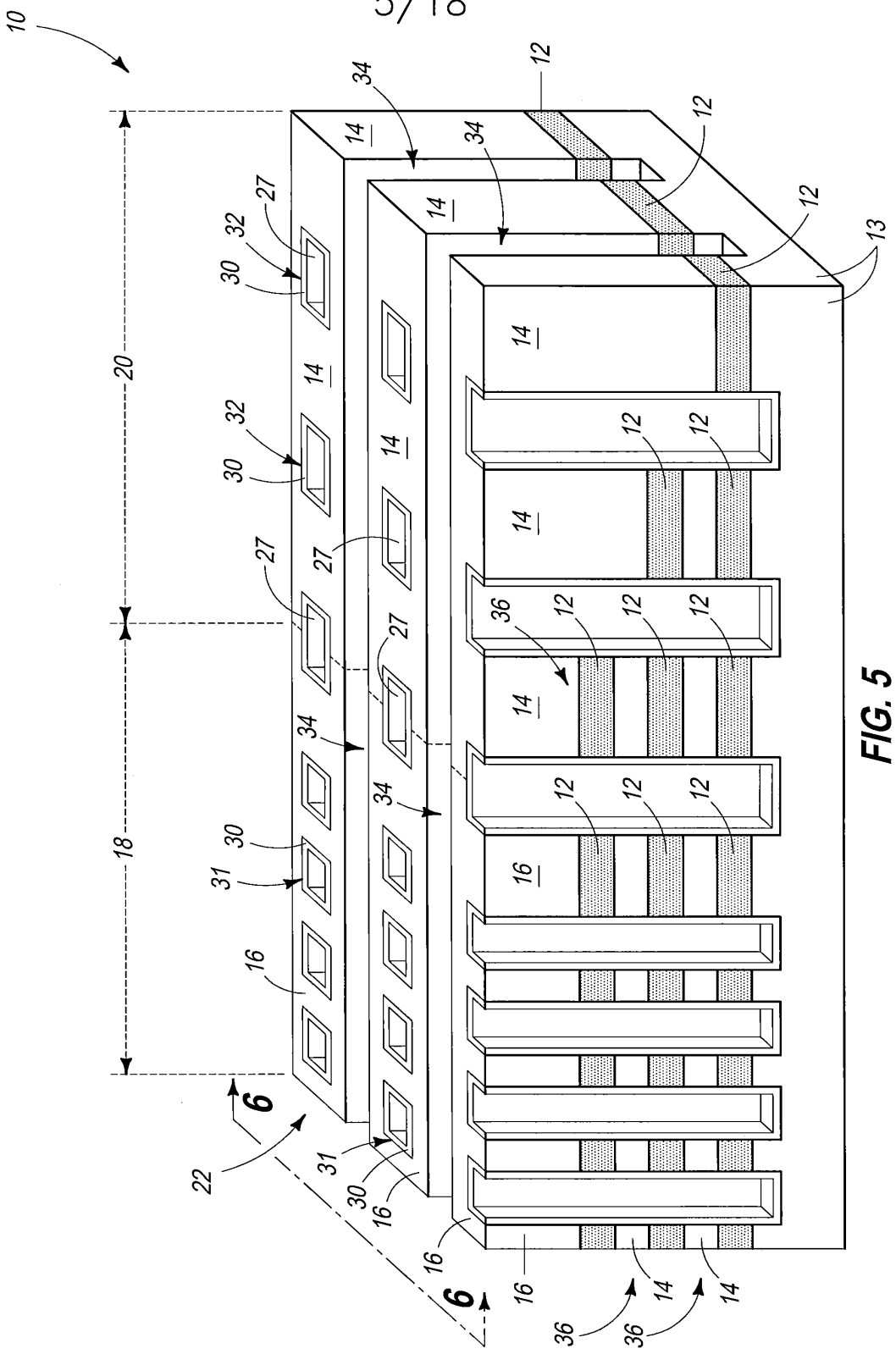



FIG. 5

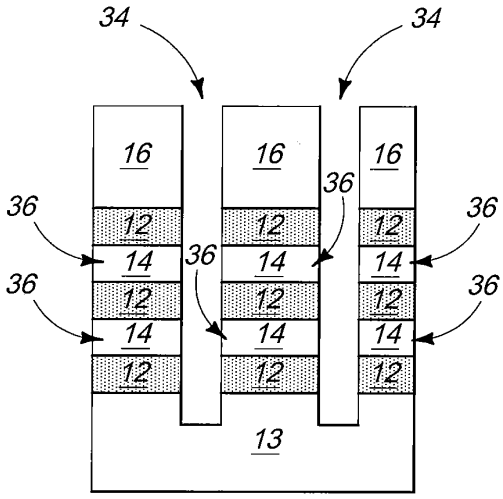

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*FIG. 6*

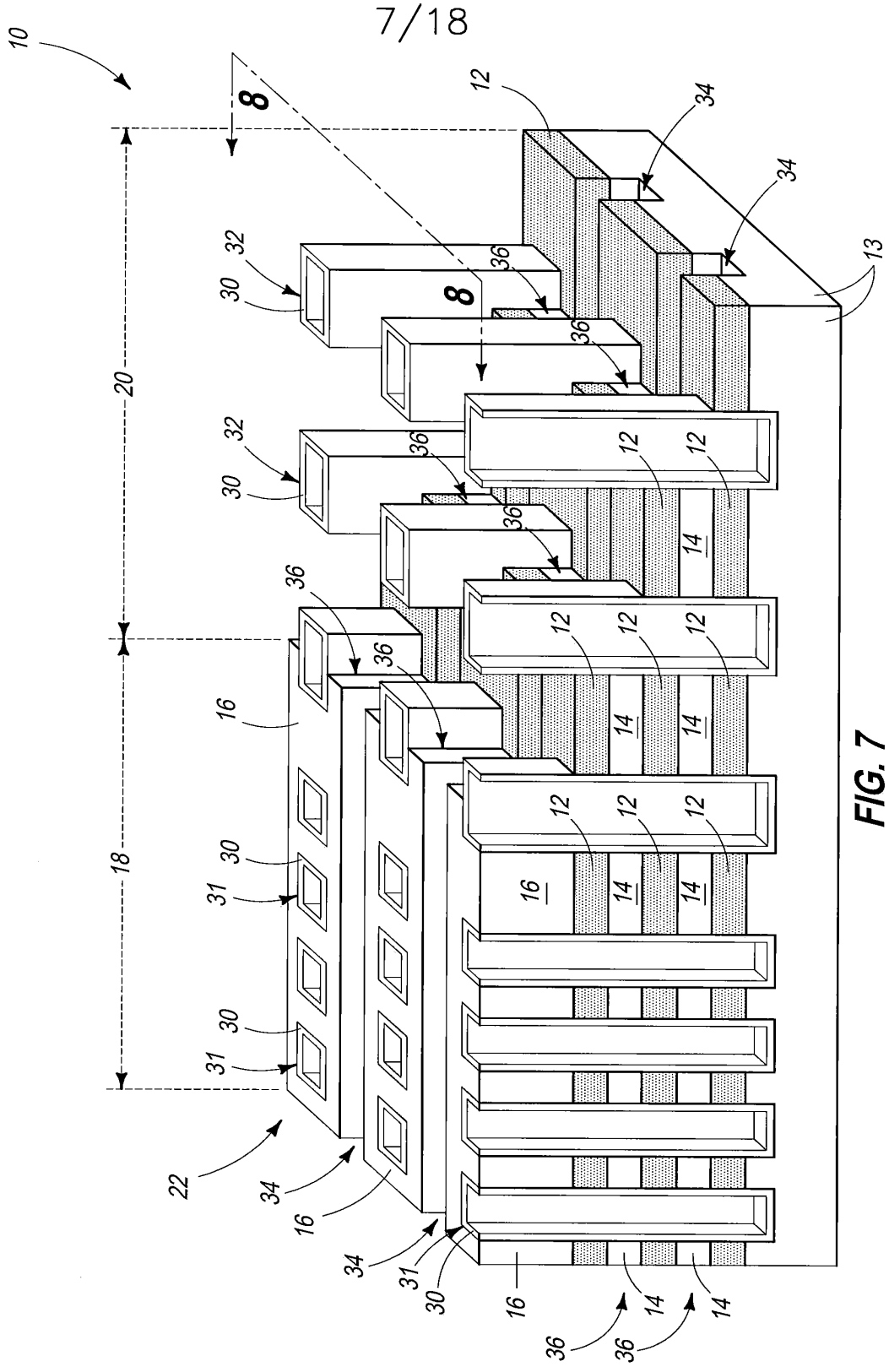

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FIG. 7

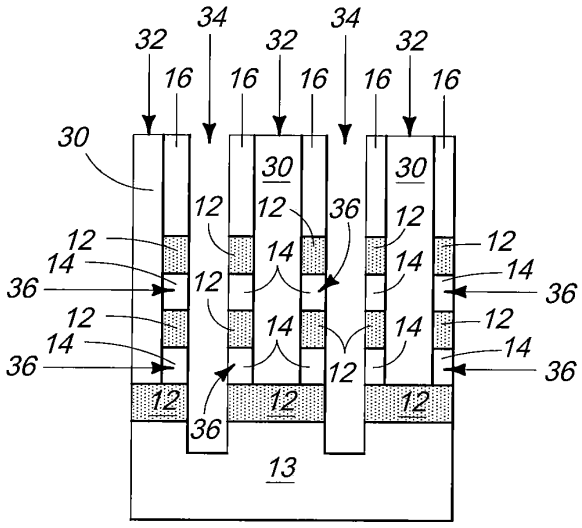

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*FIG. 8*

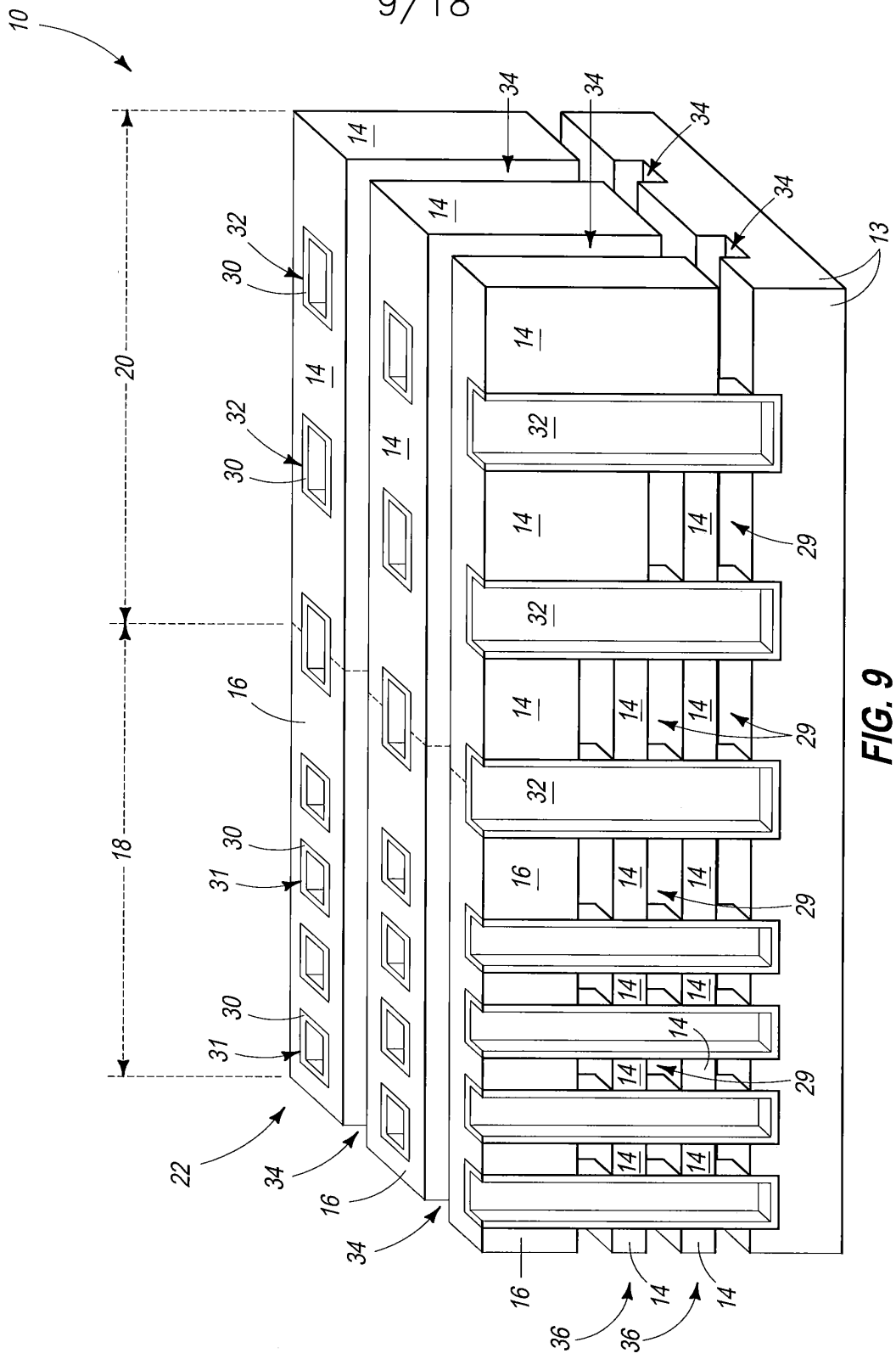



FIG. 9

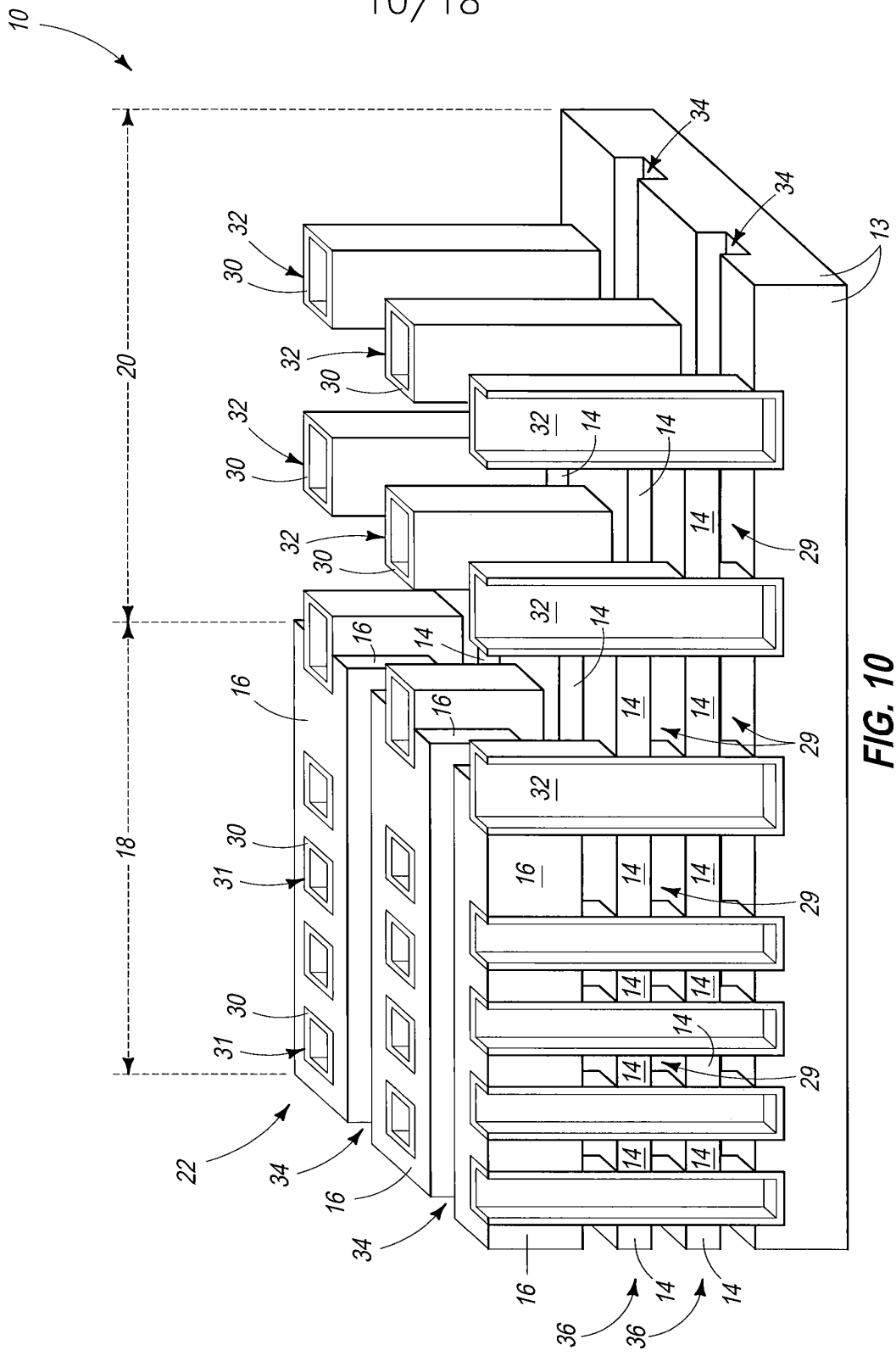



FIG. 10

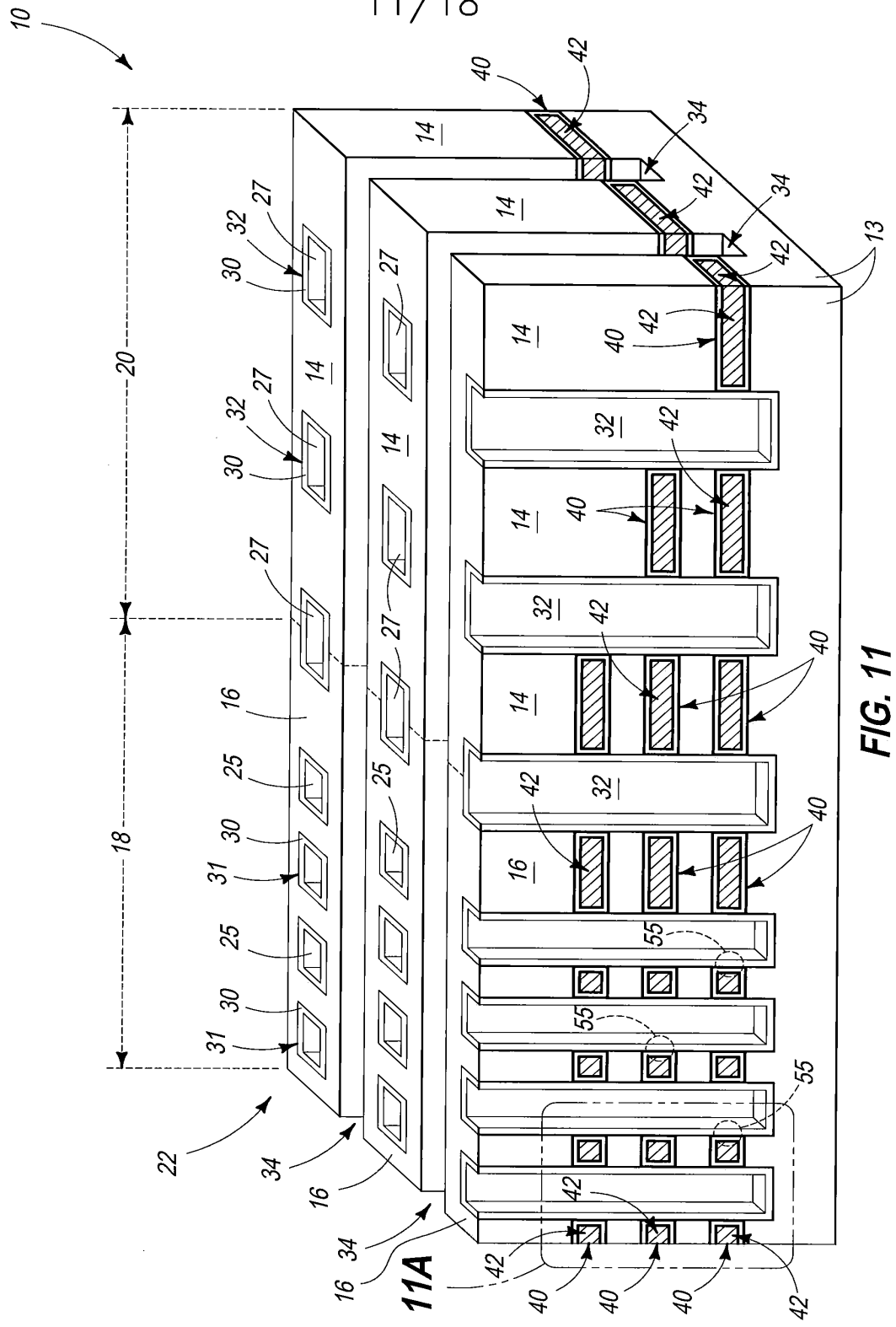



FIG. 11

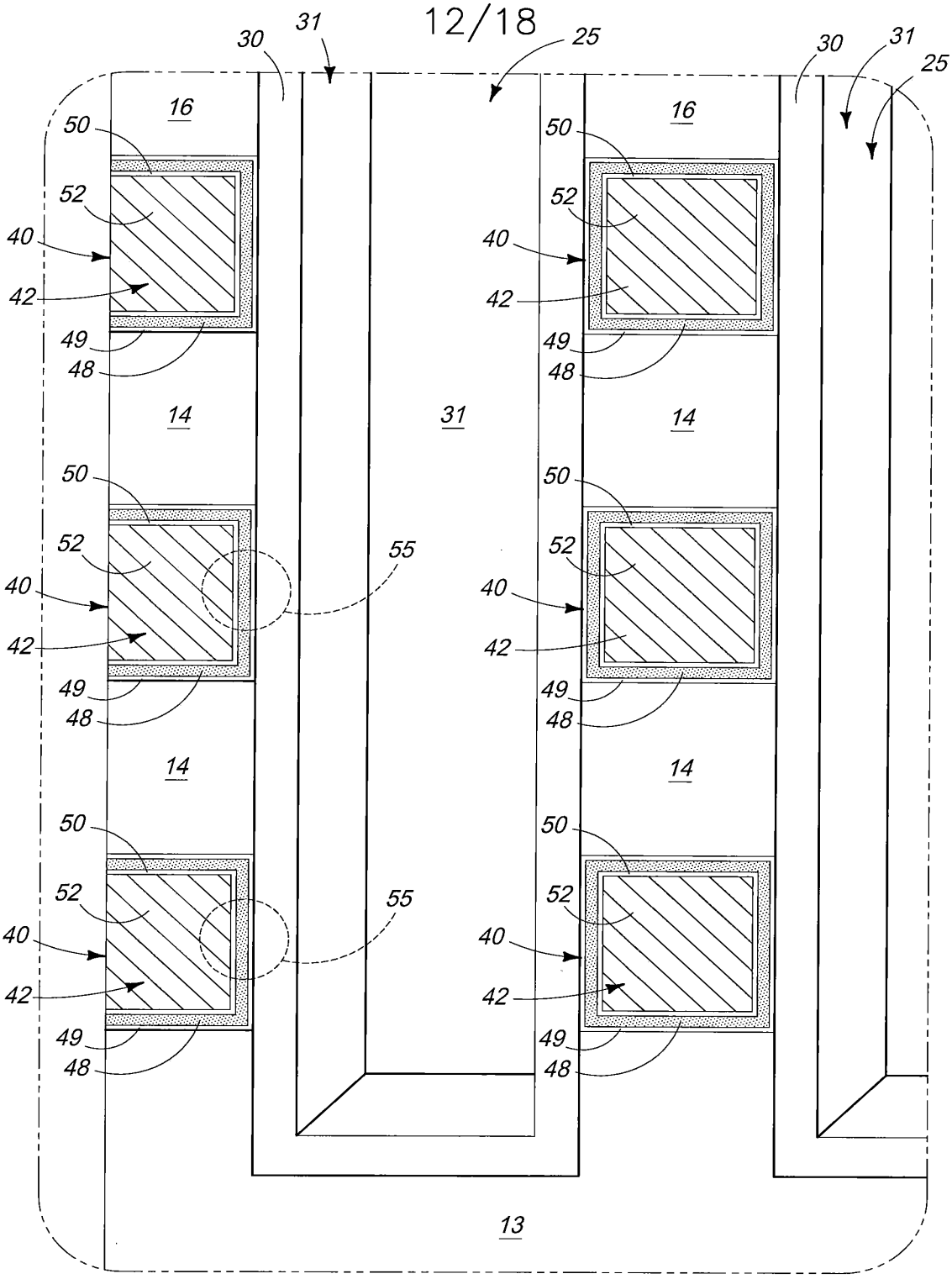



FIG. 11A

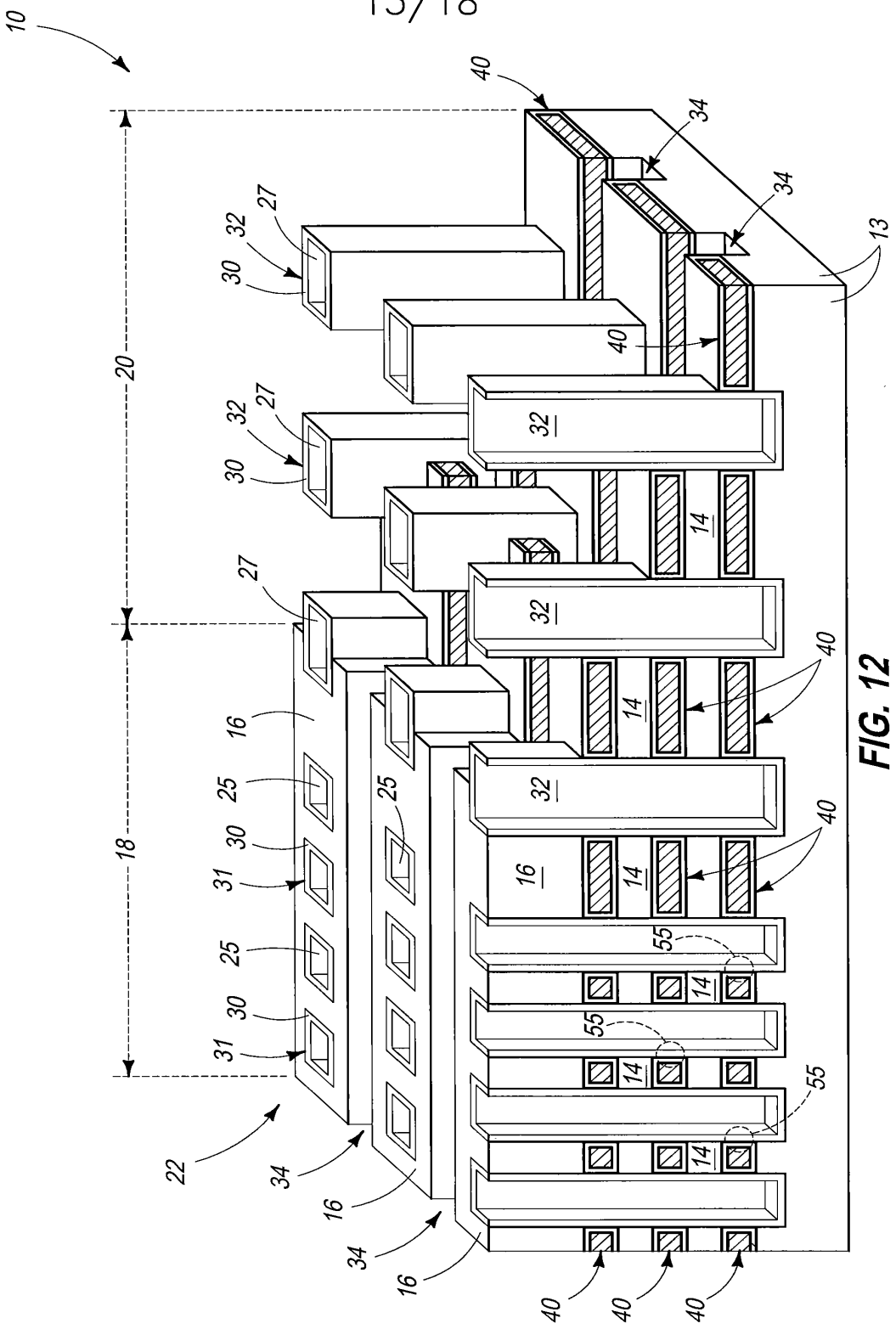



FIG. 12

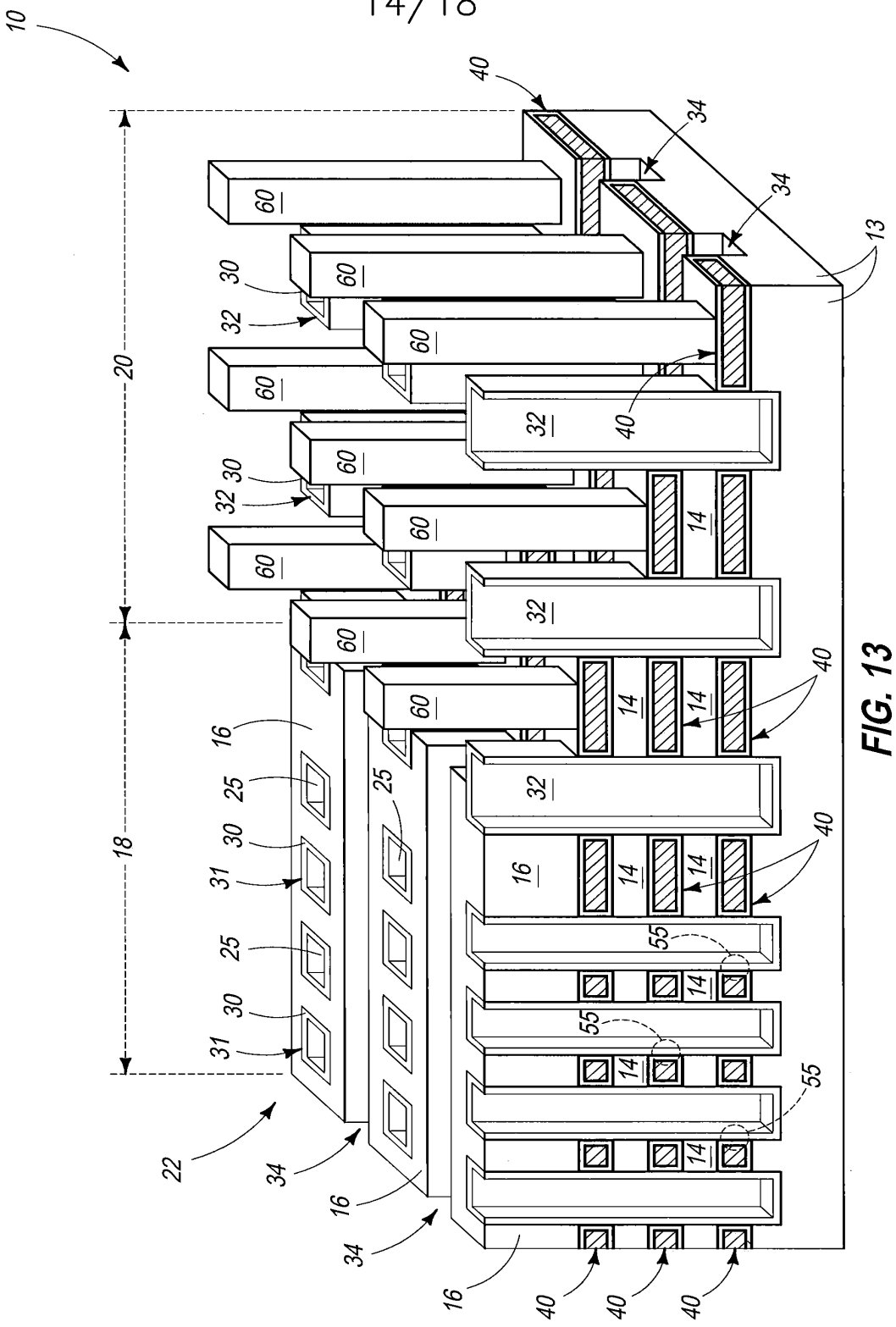



FIG. 13

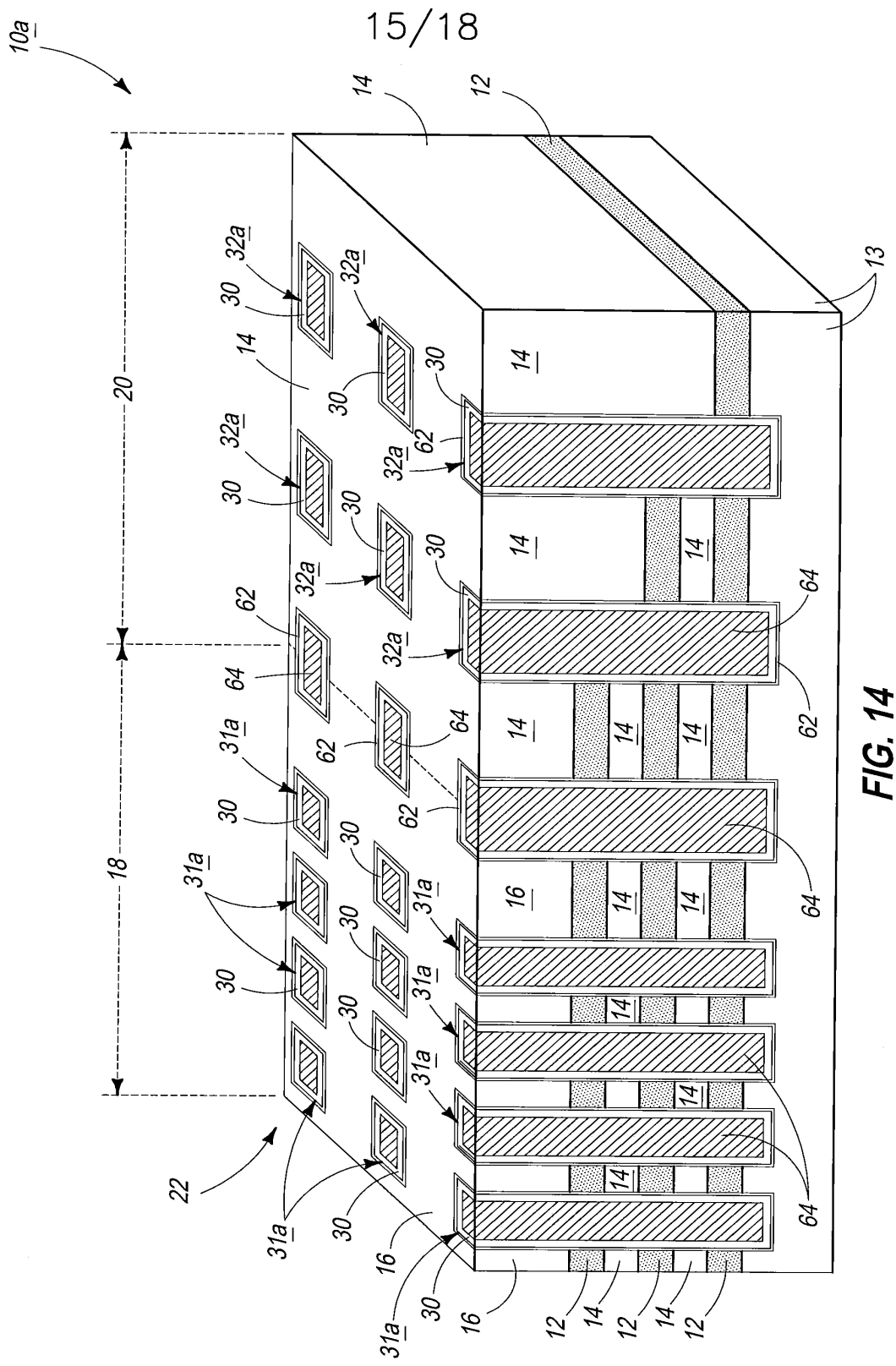



FIG. 14

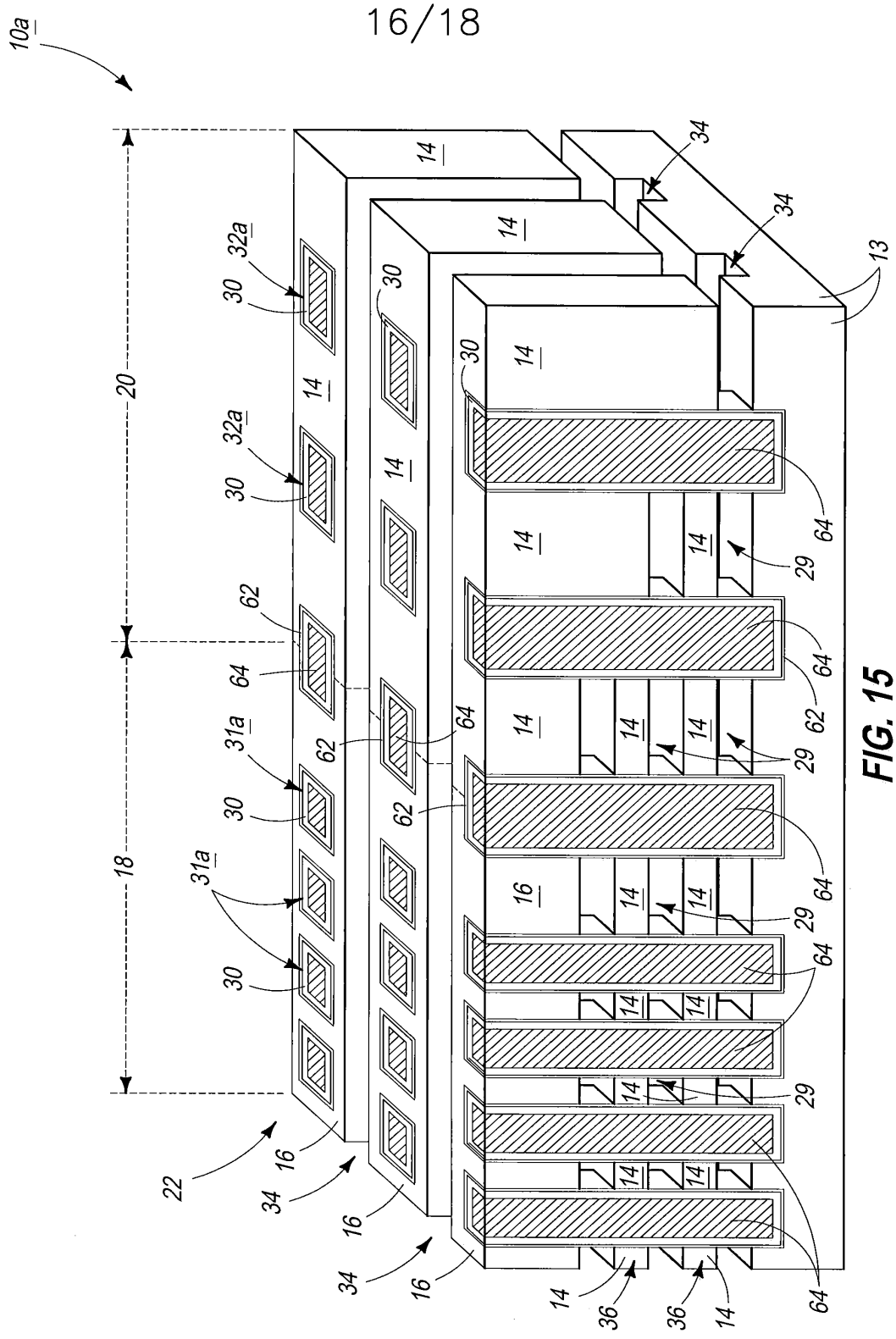



FIG. 15

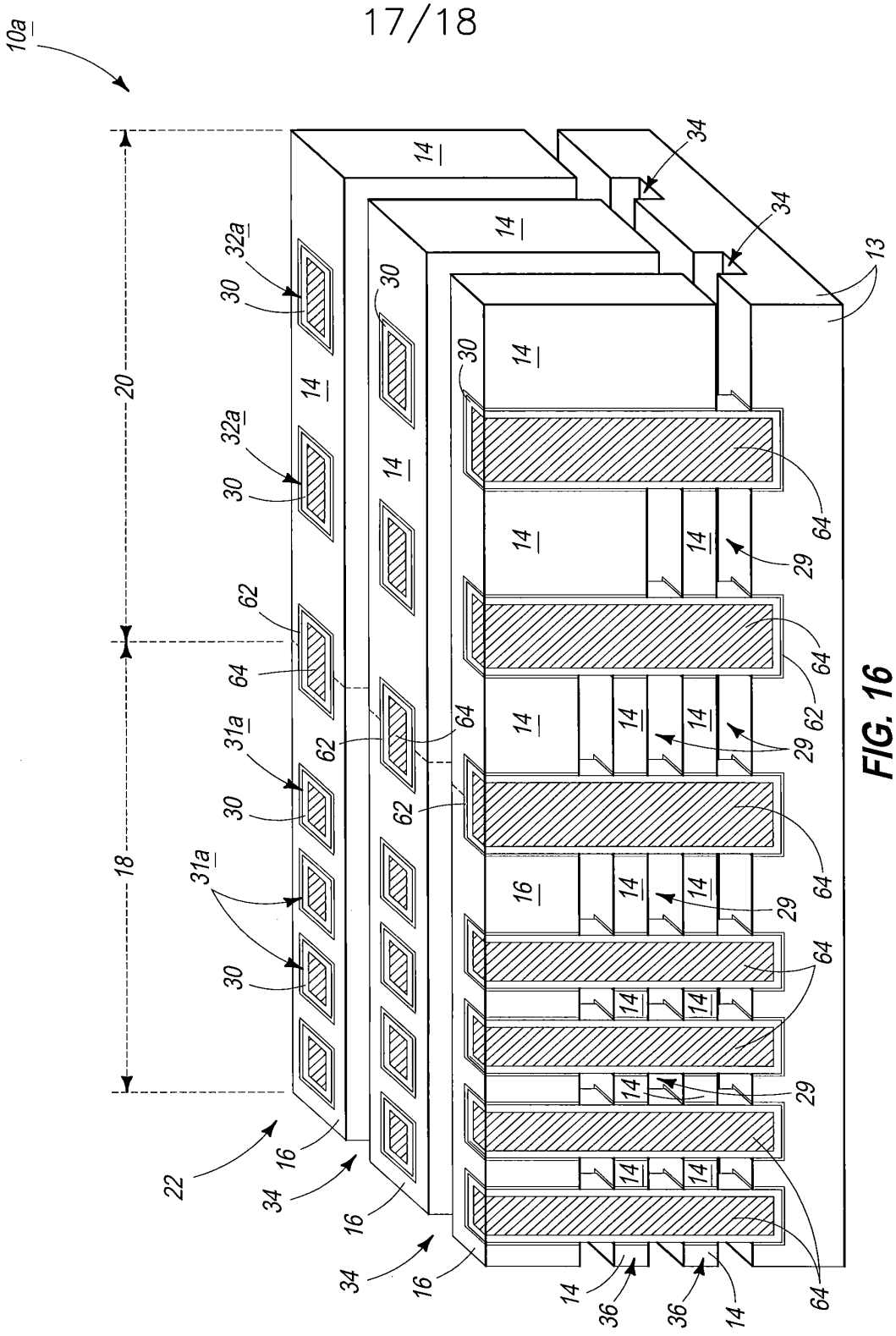



FIG. 16

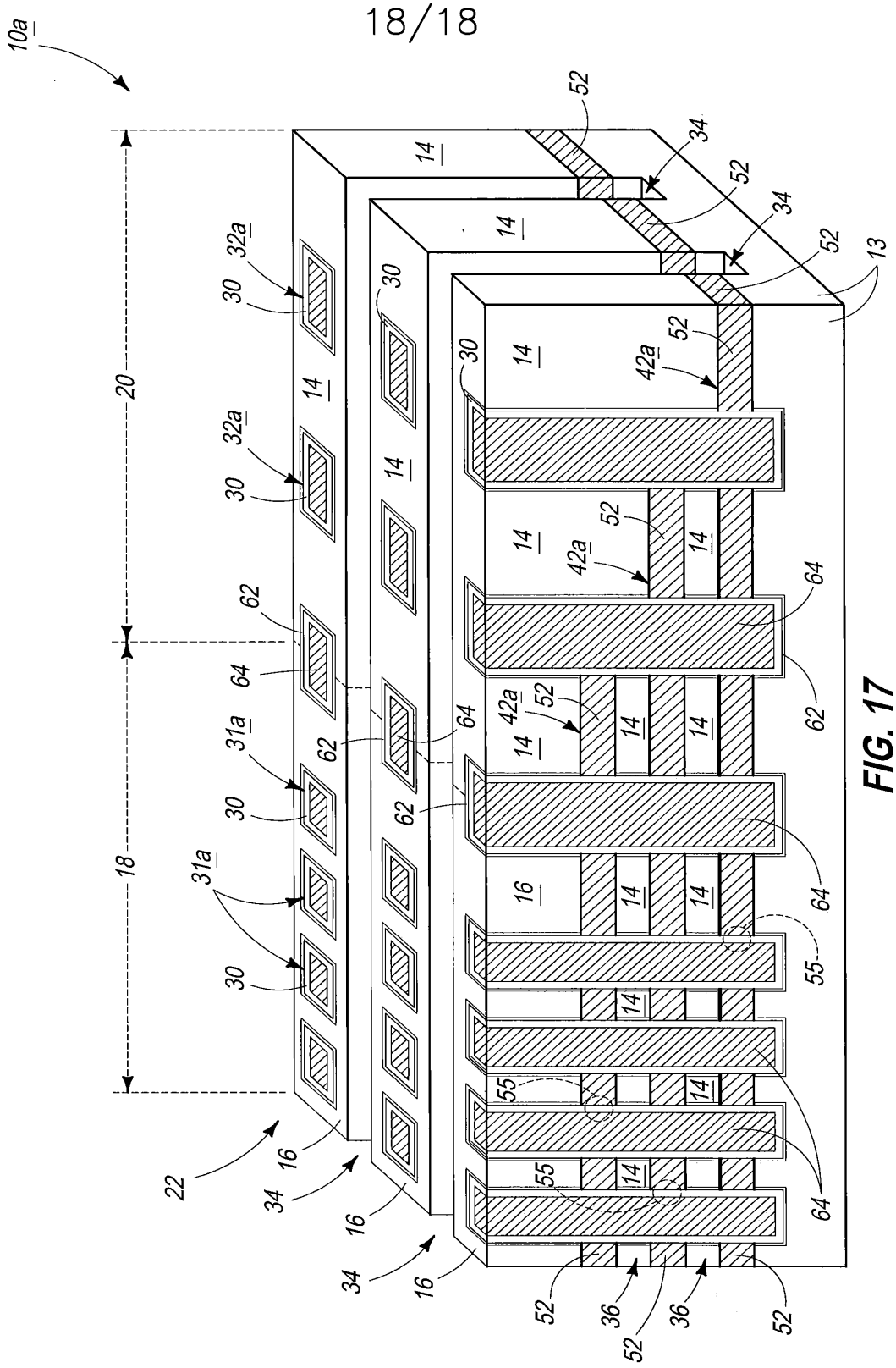



FIG. 17

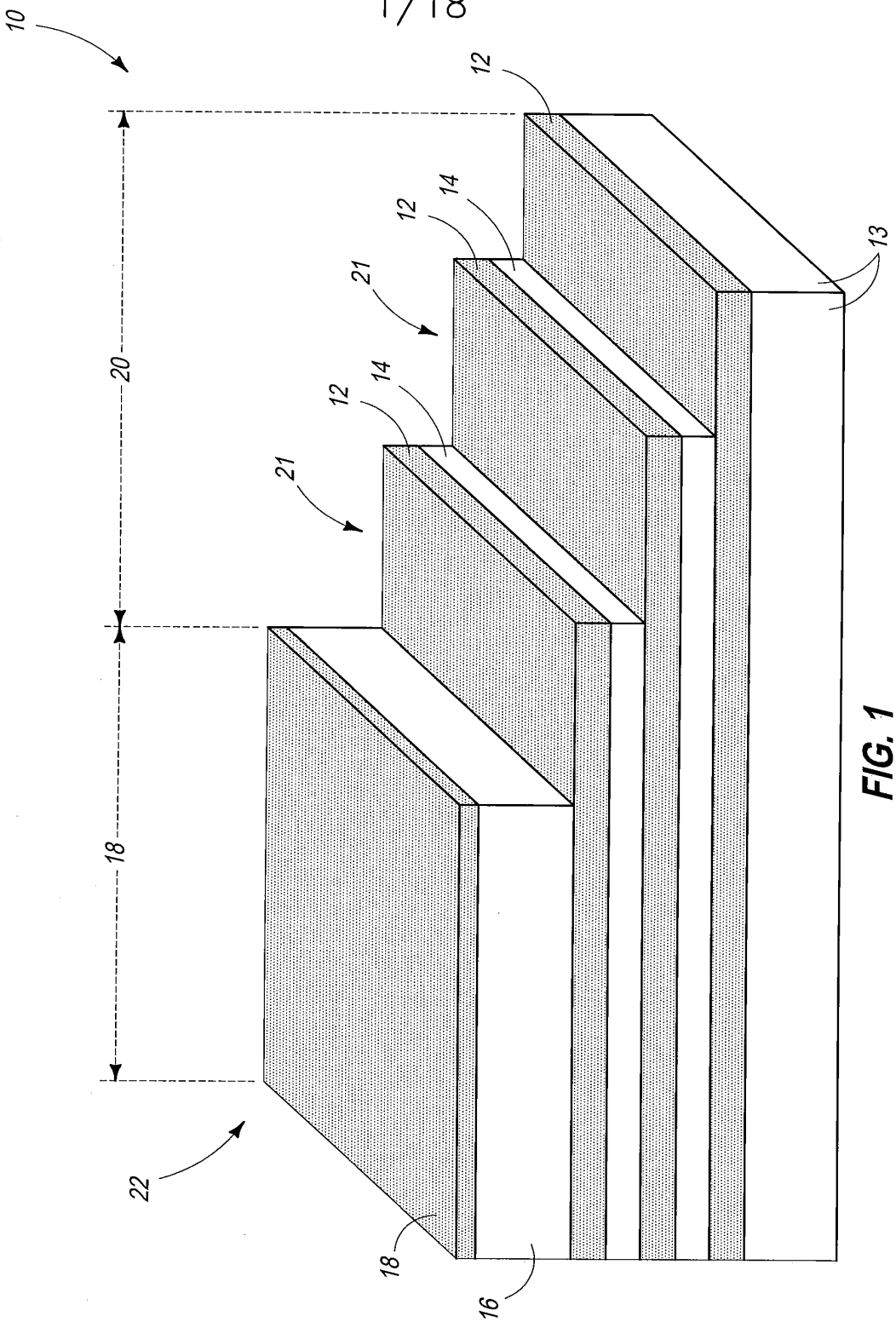



FIG. 1

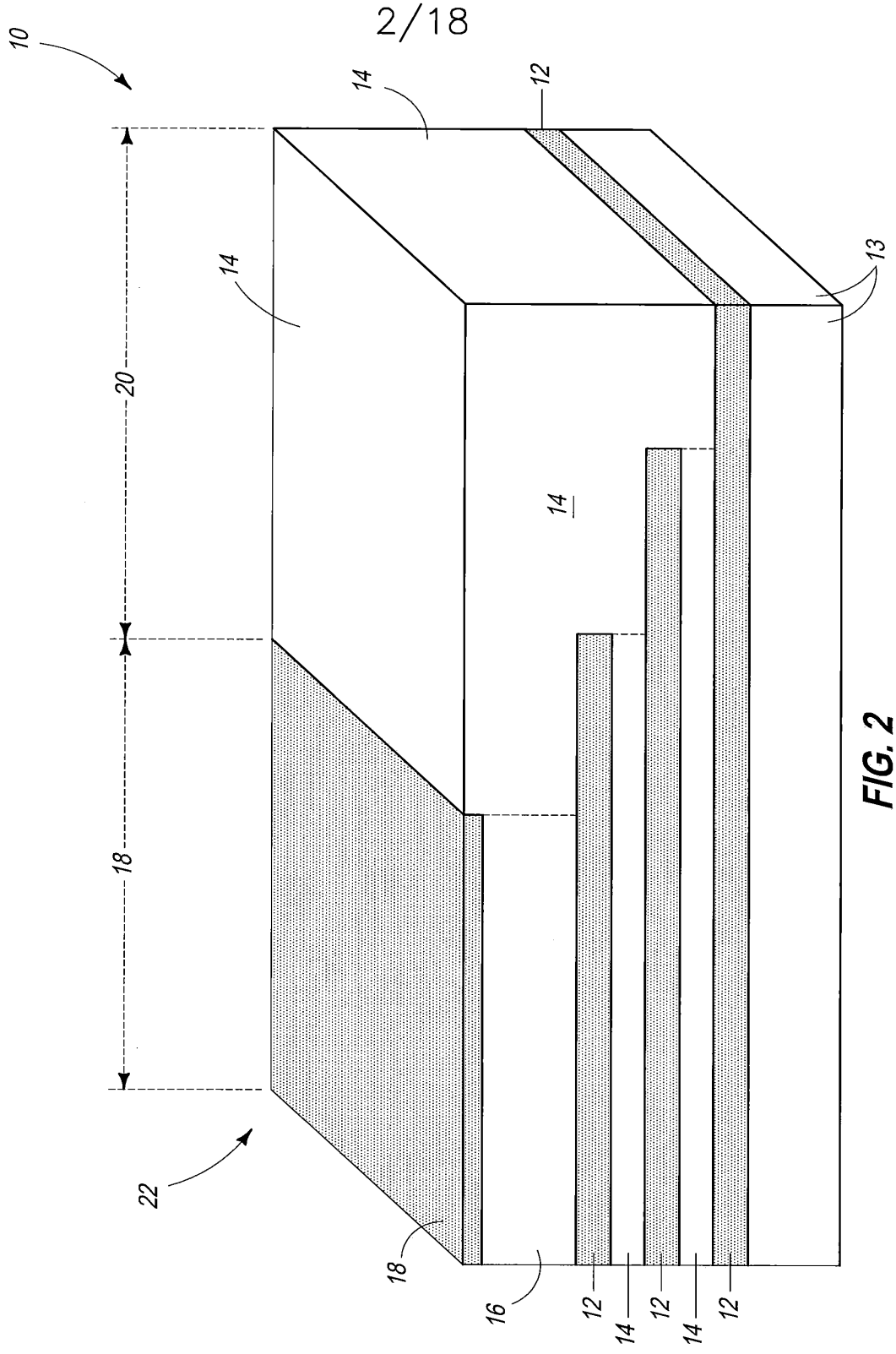



FIG. 2

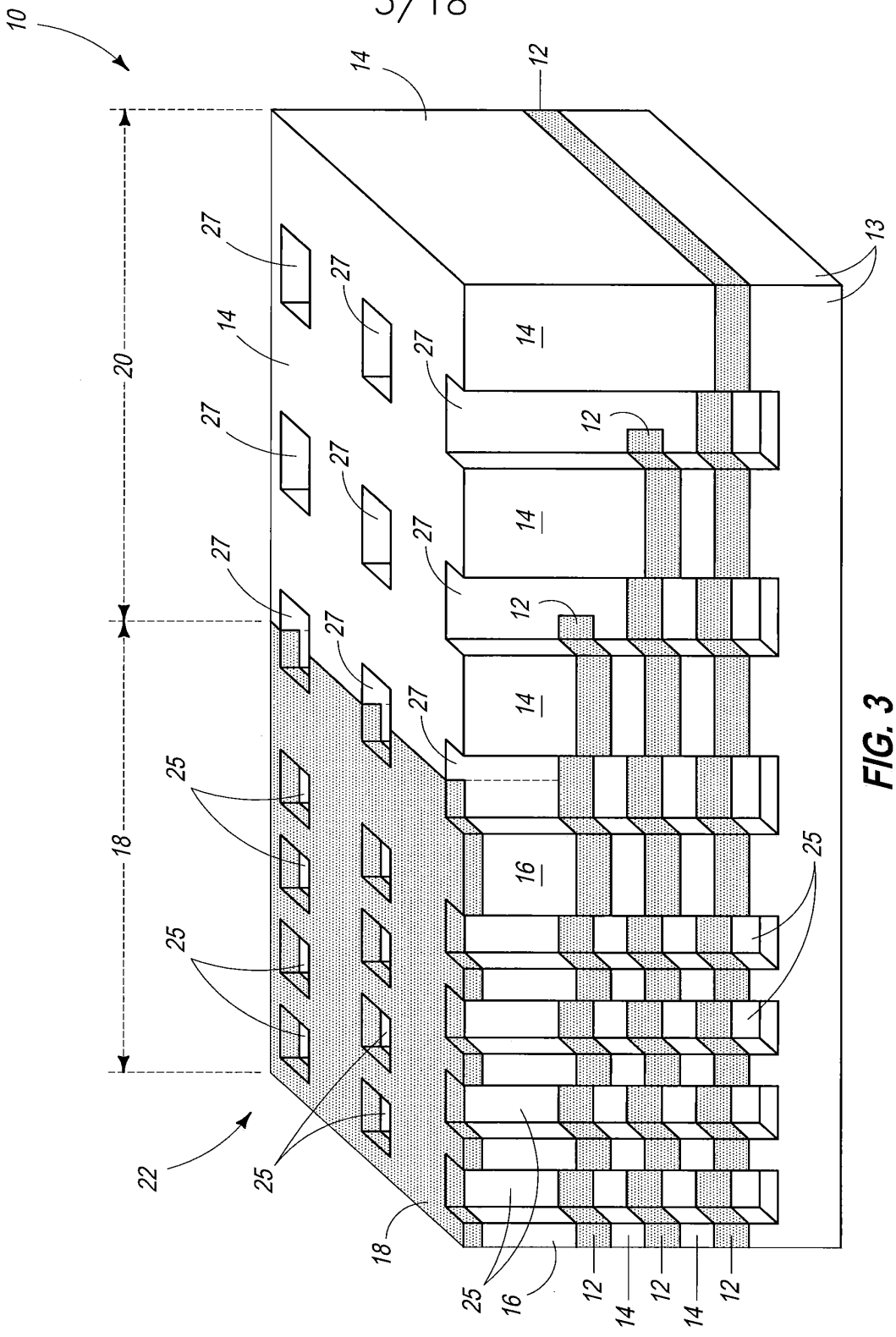



FIG. 3

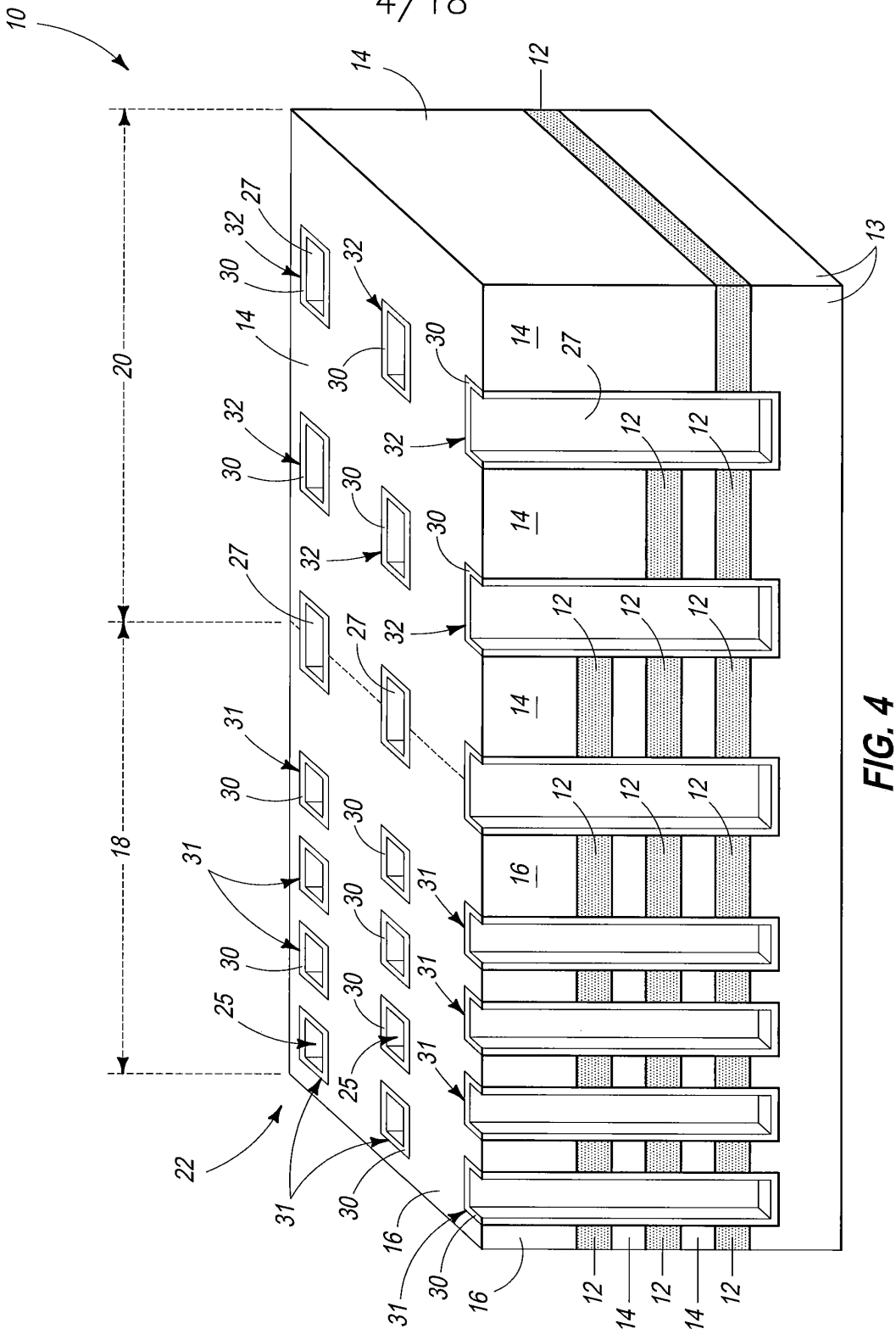



FIG. 4

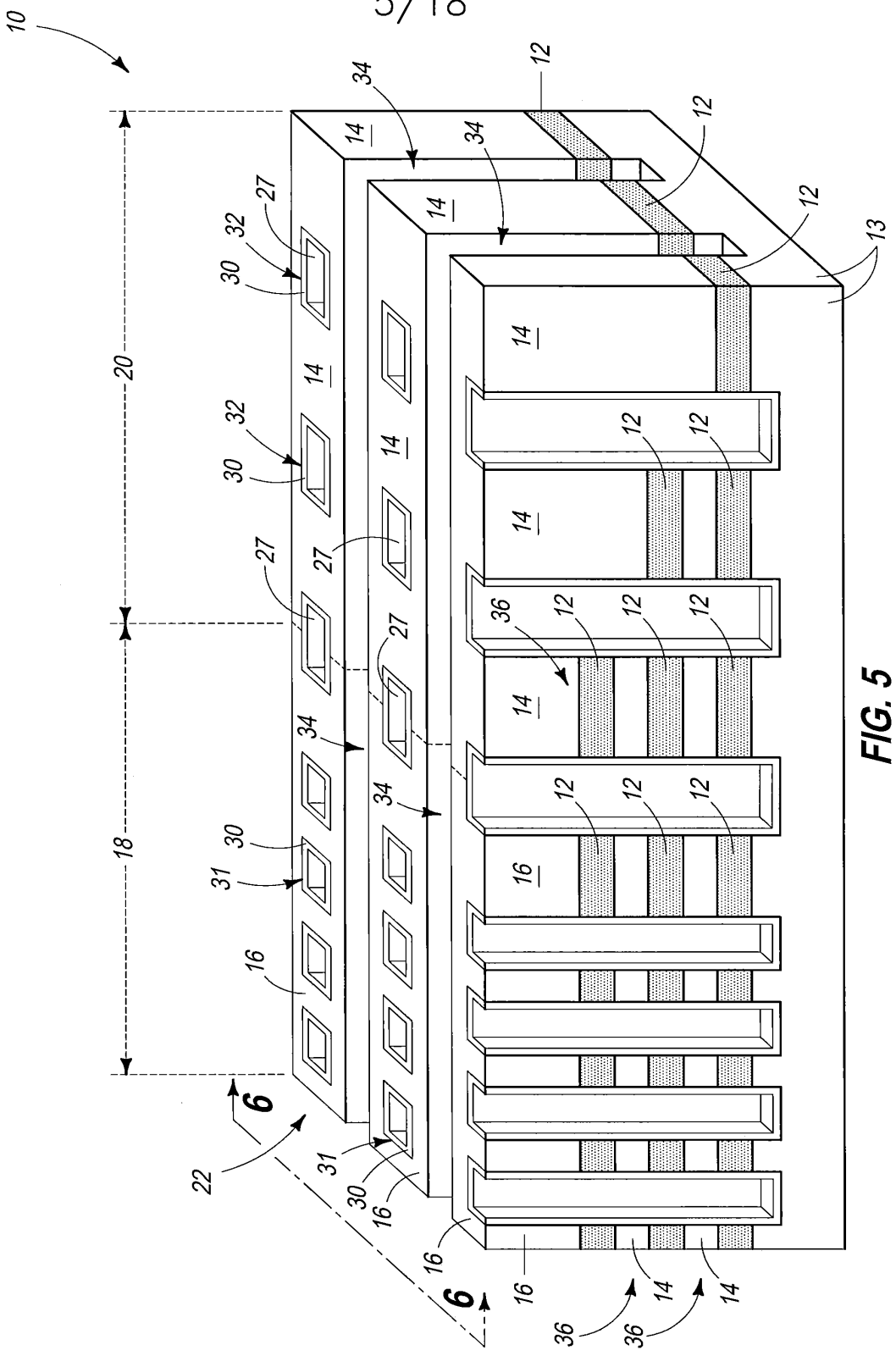



FIG. 5

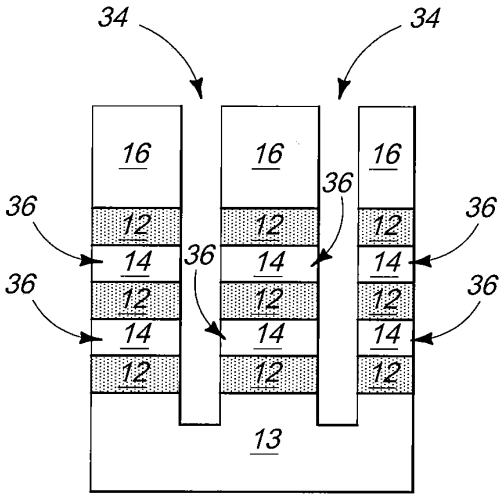

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*FIG. 6*

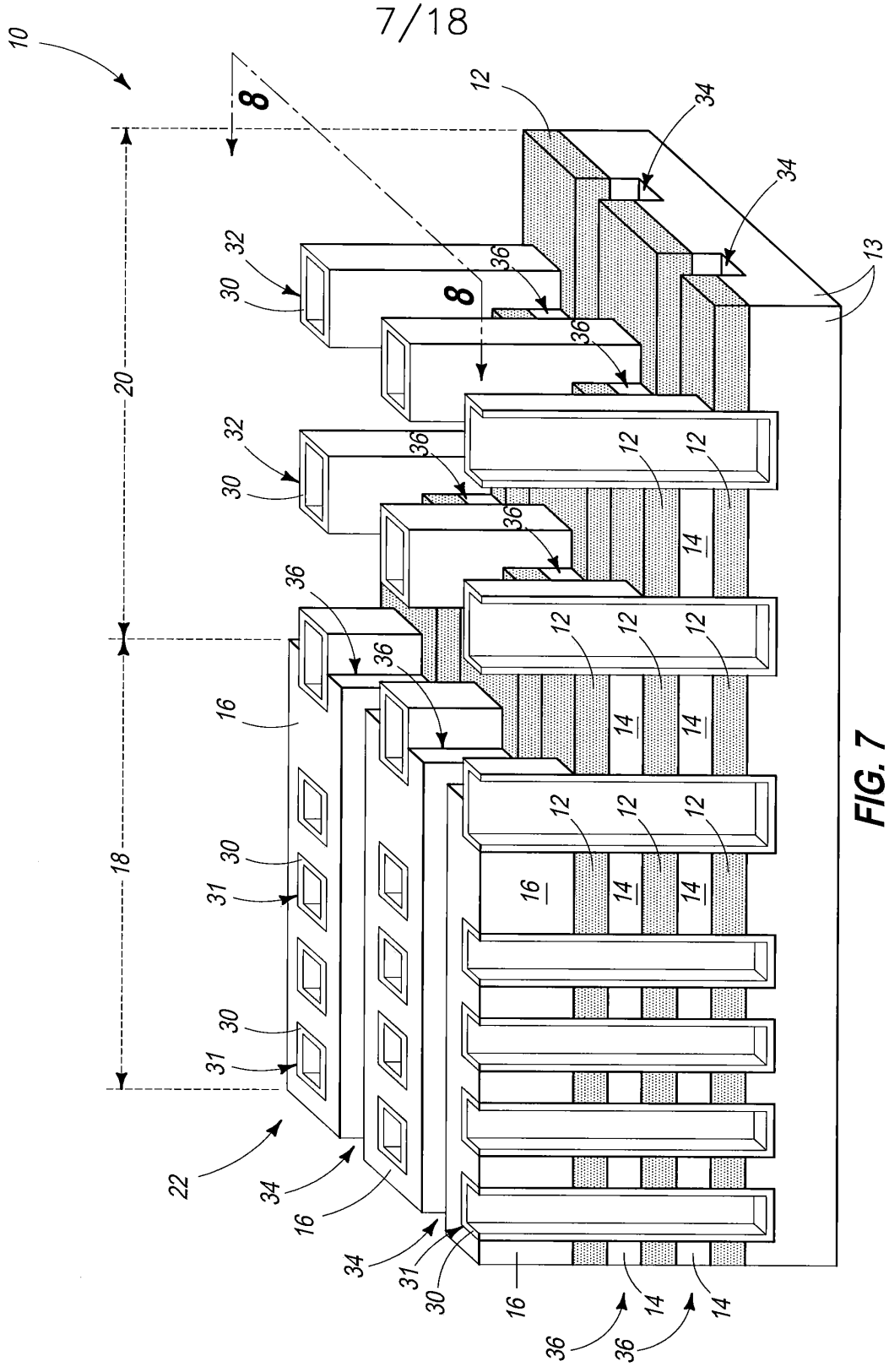

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FIG. 7

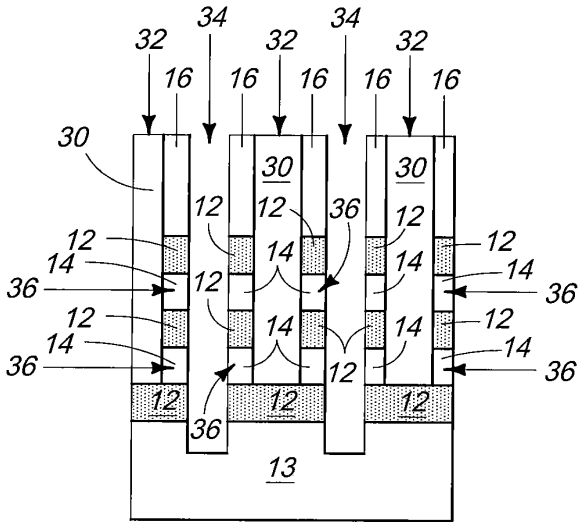

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*FIG. 8*

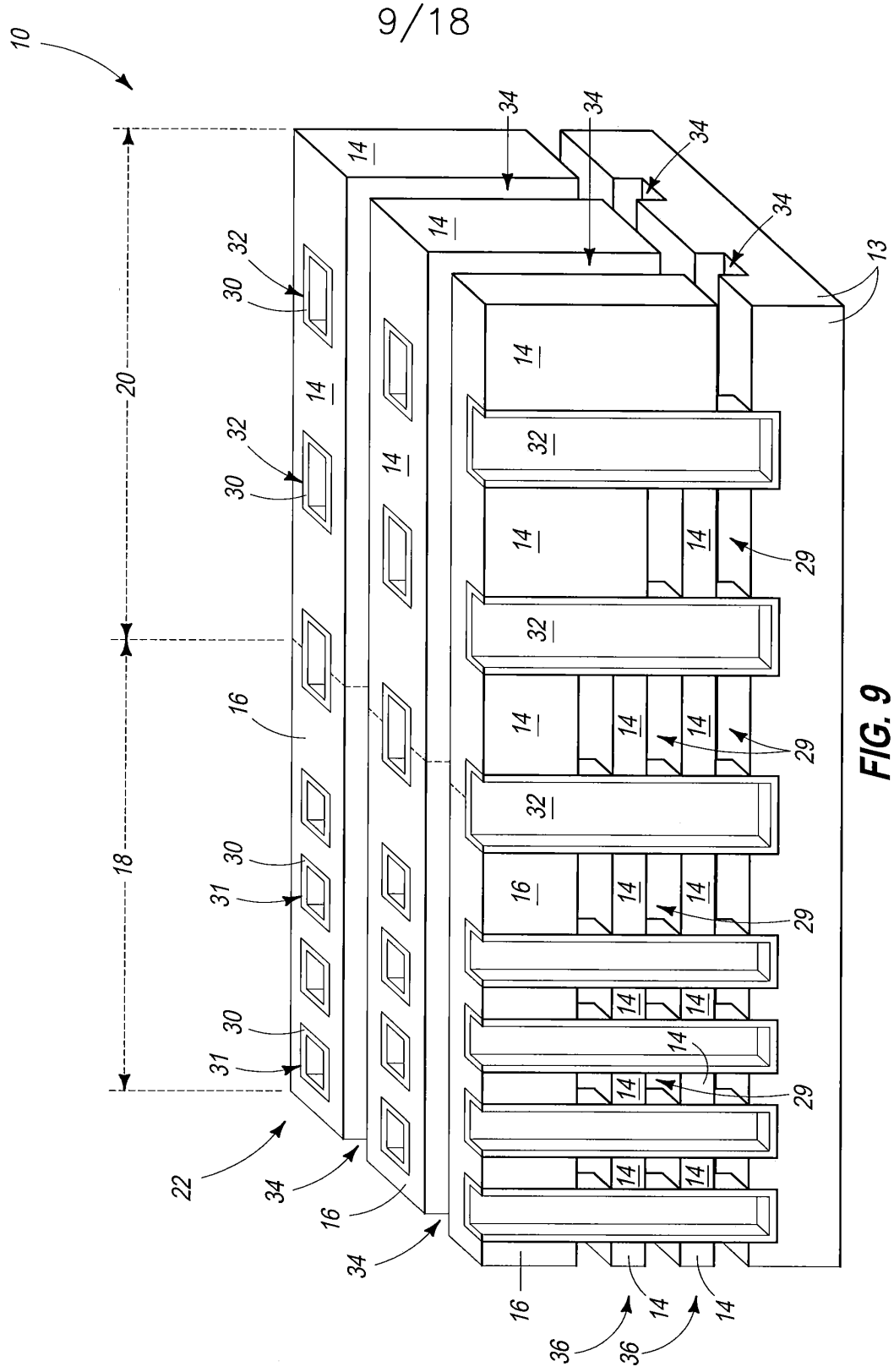



FIG. 9

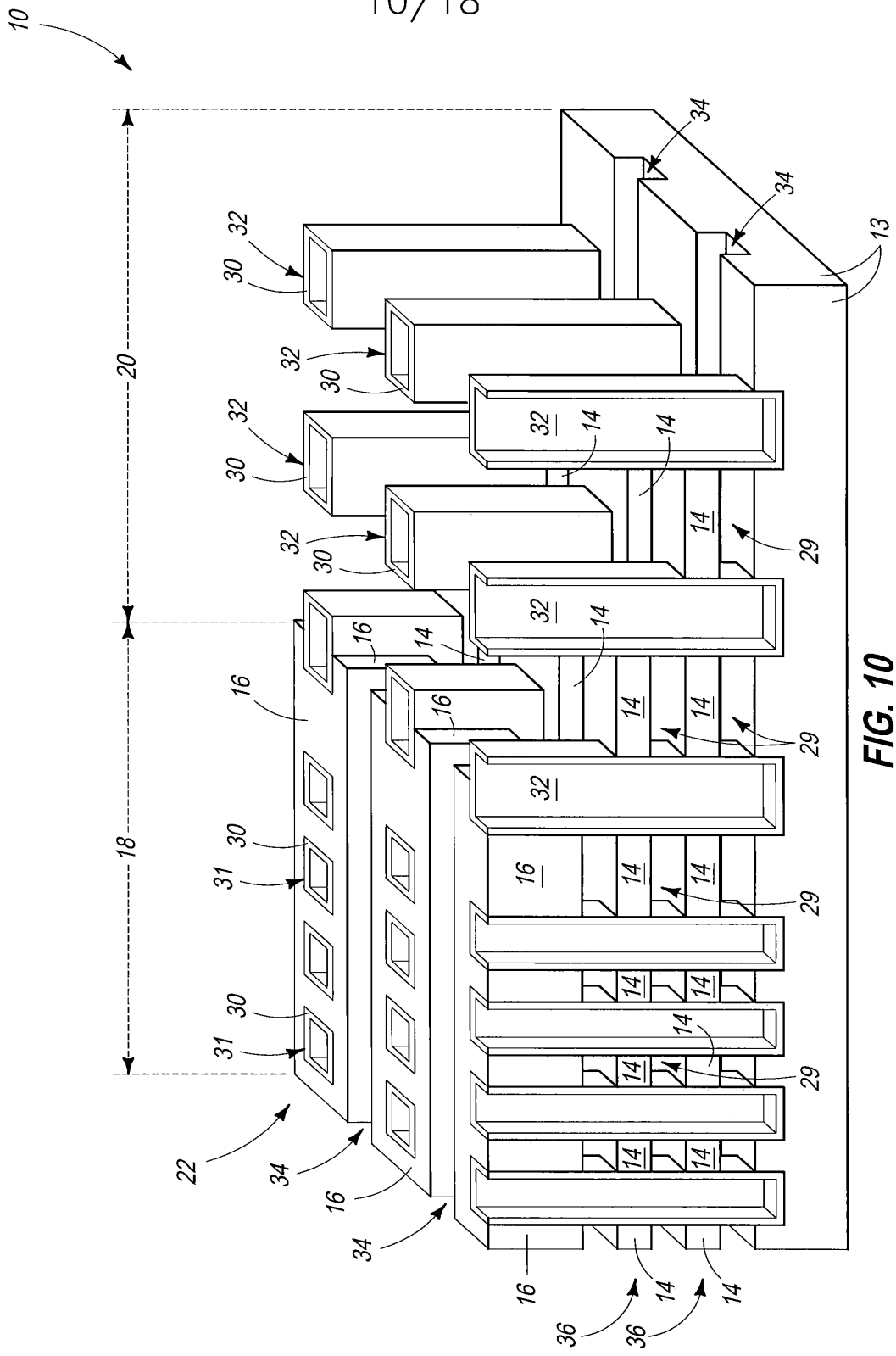



FIG. 10

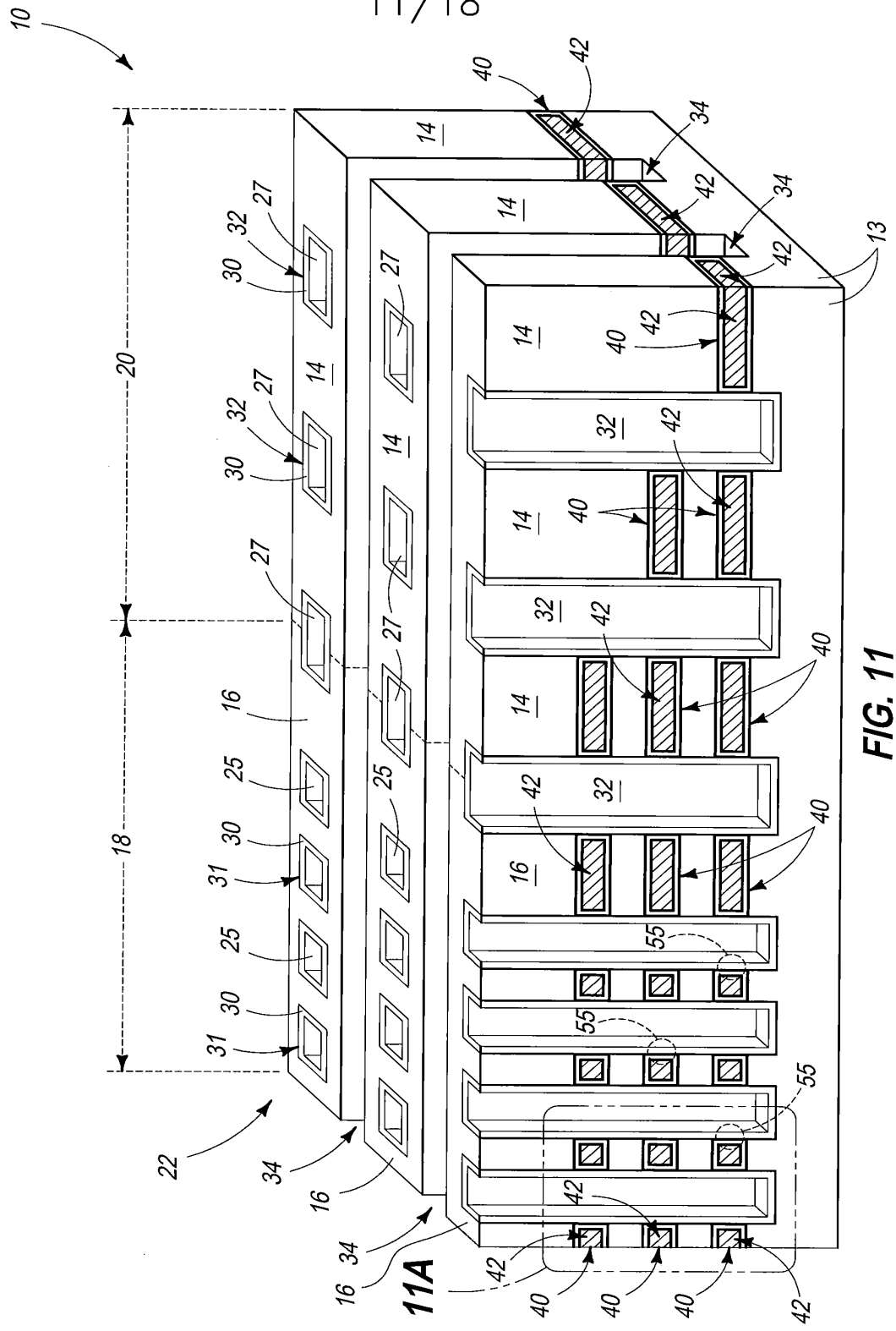



FIG. 11

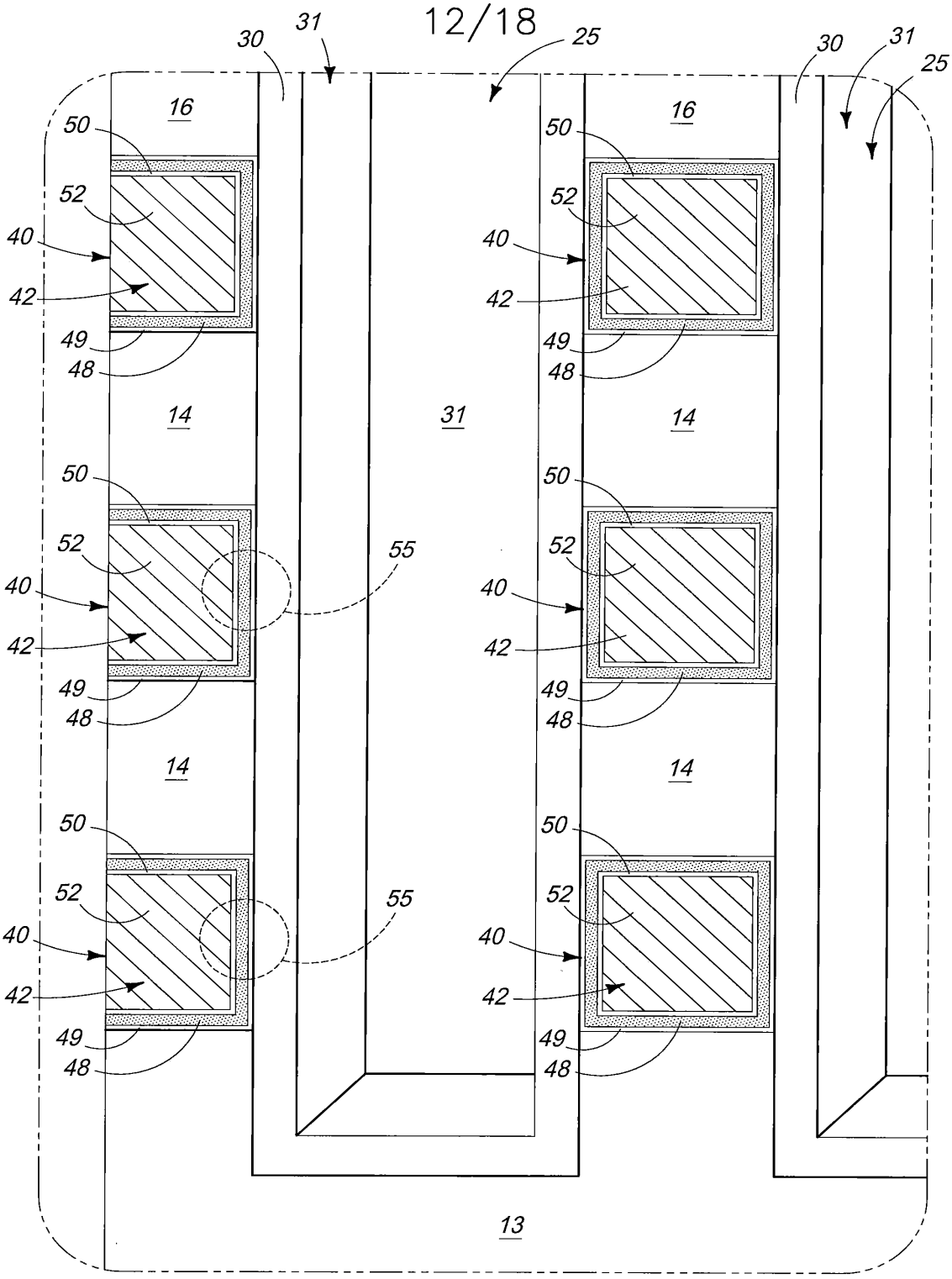



FIG. 11A

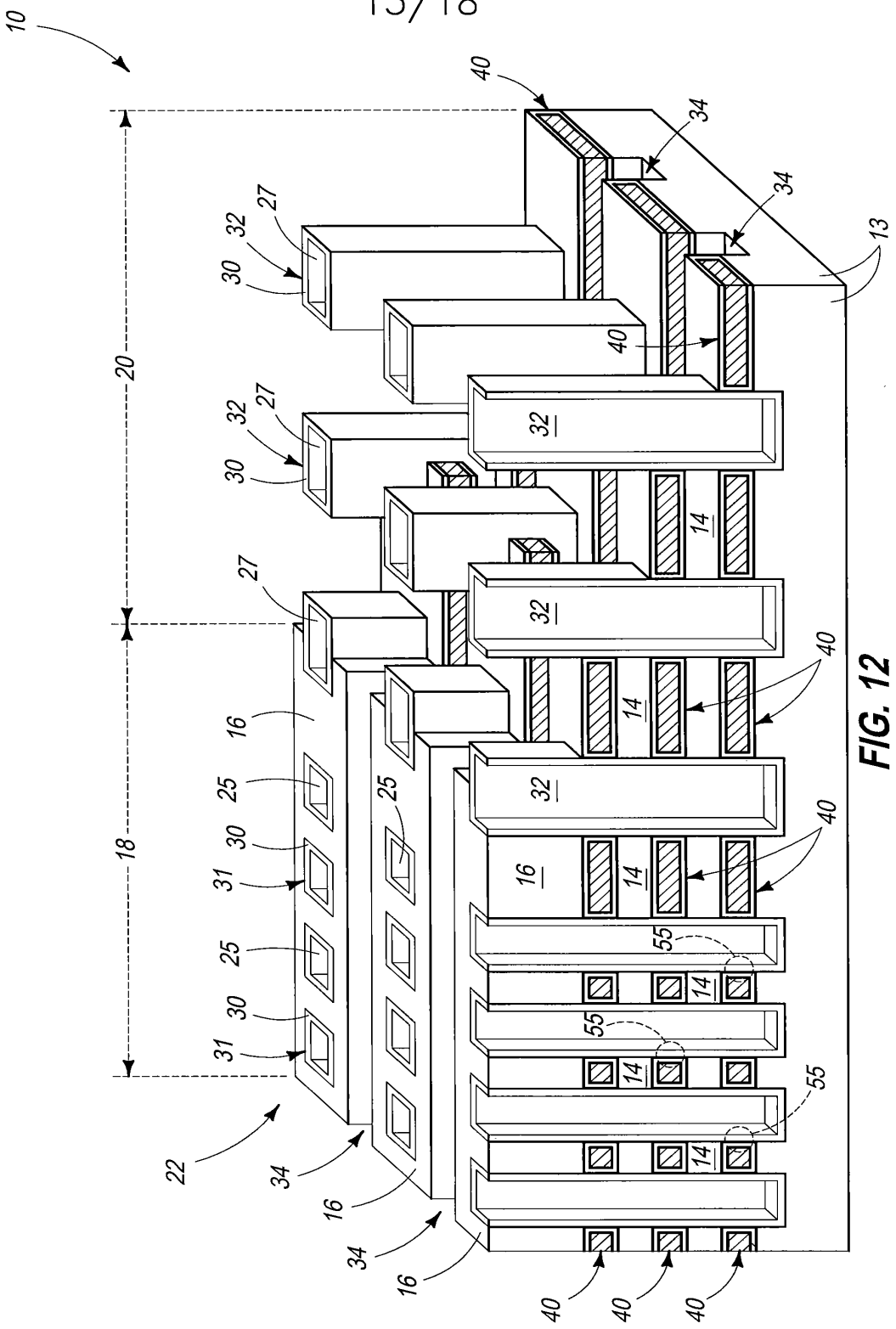



FIG. 12

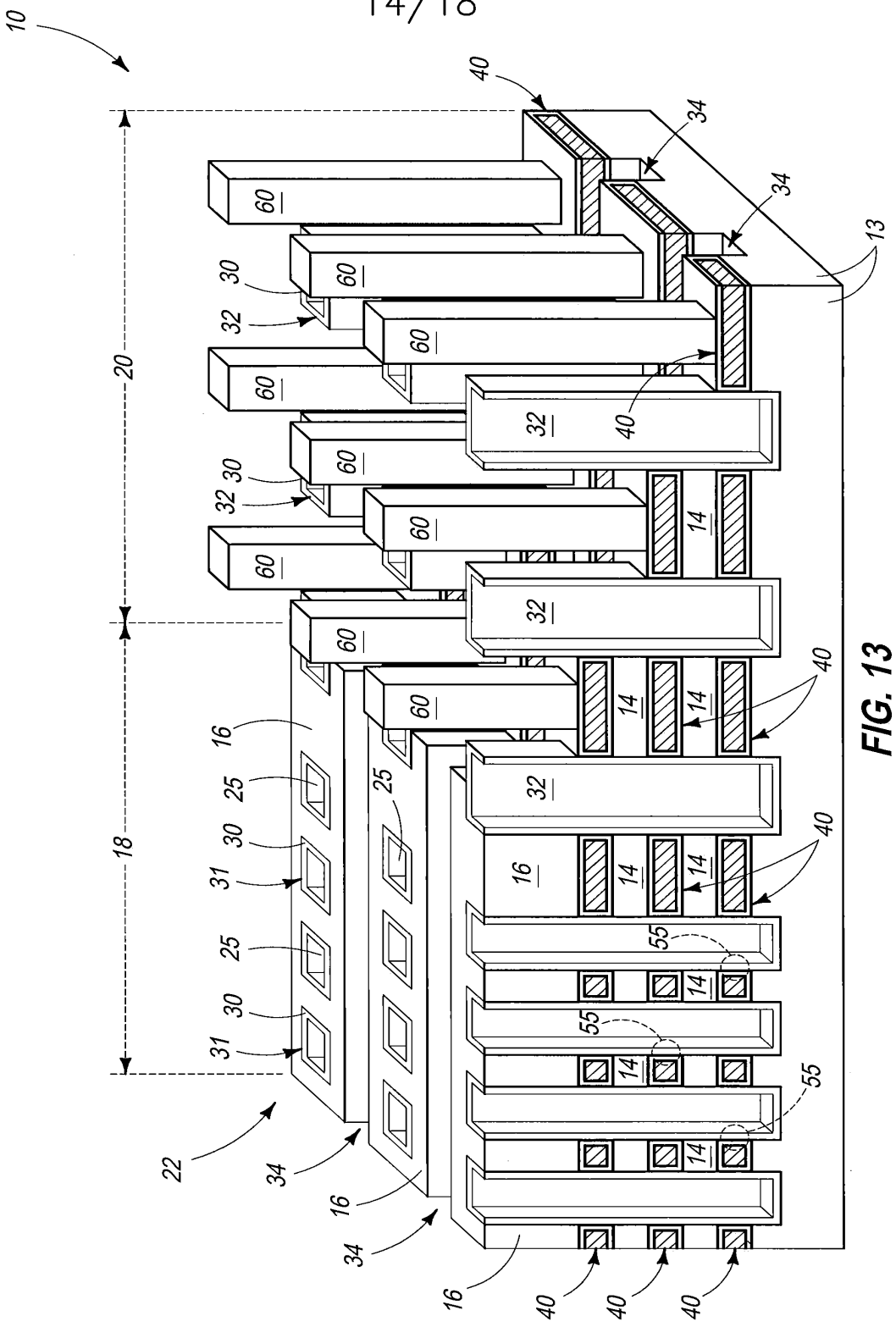



FIG. 13

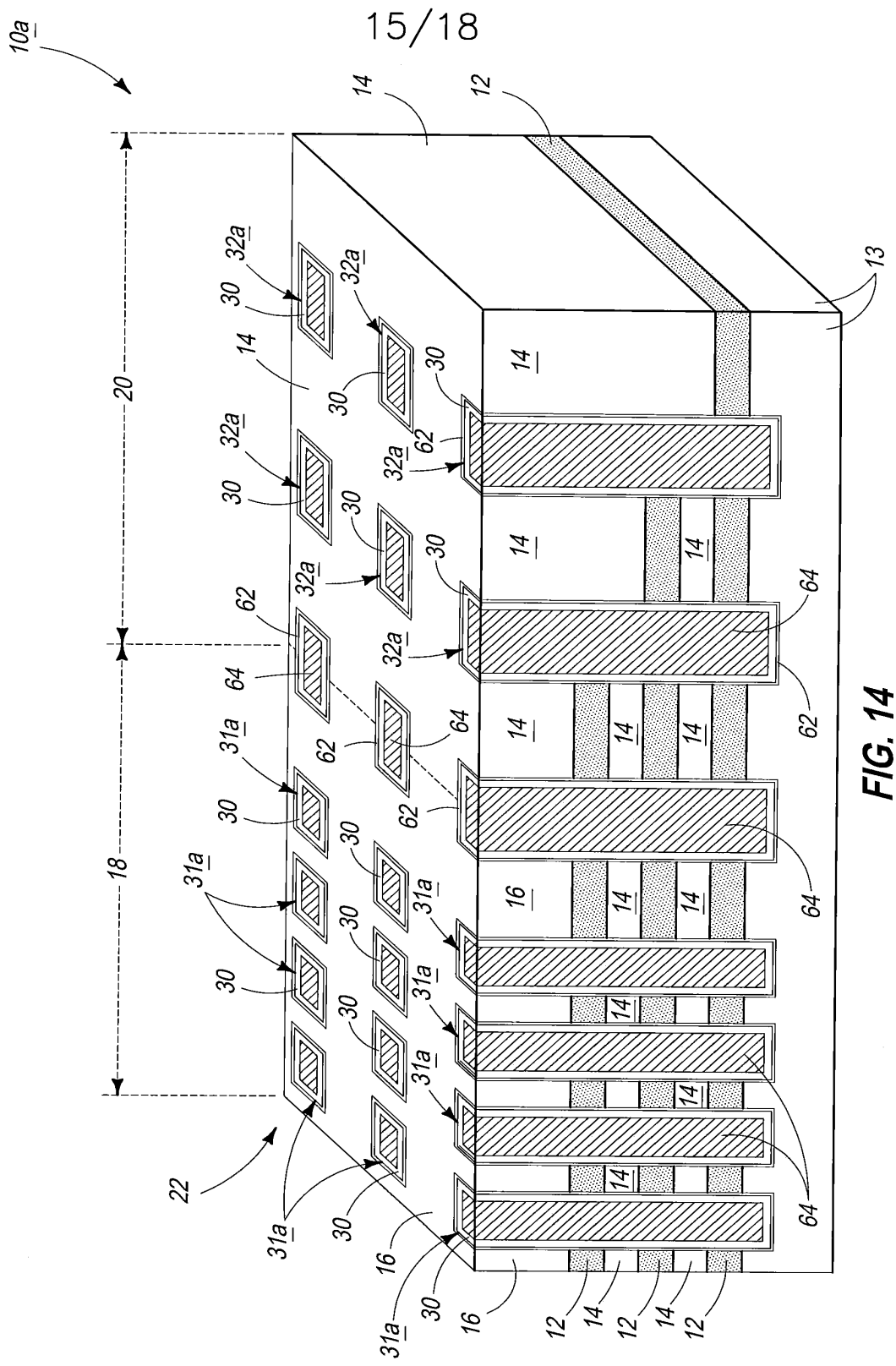



FIG. 14

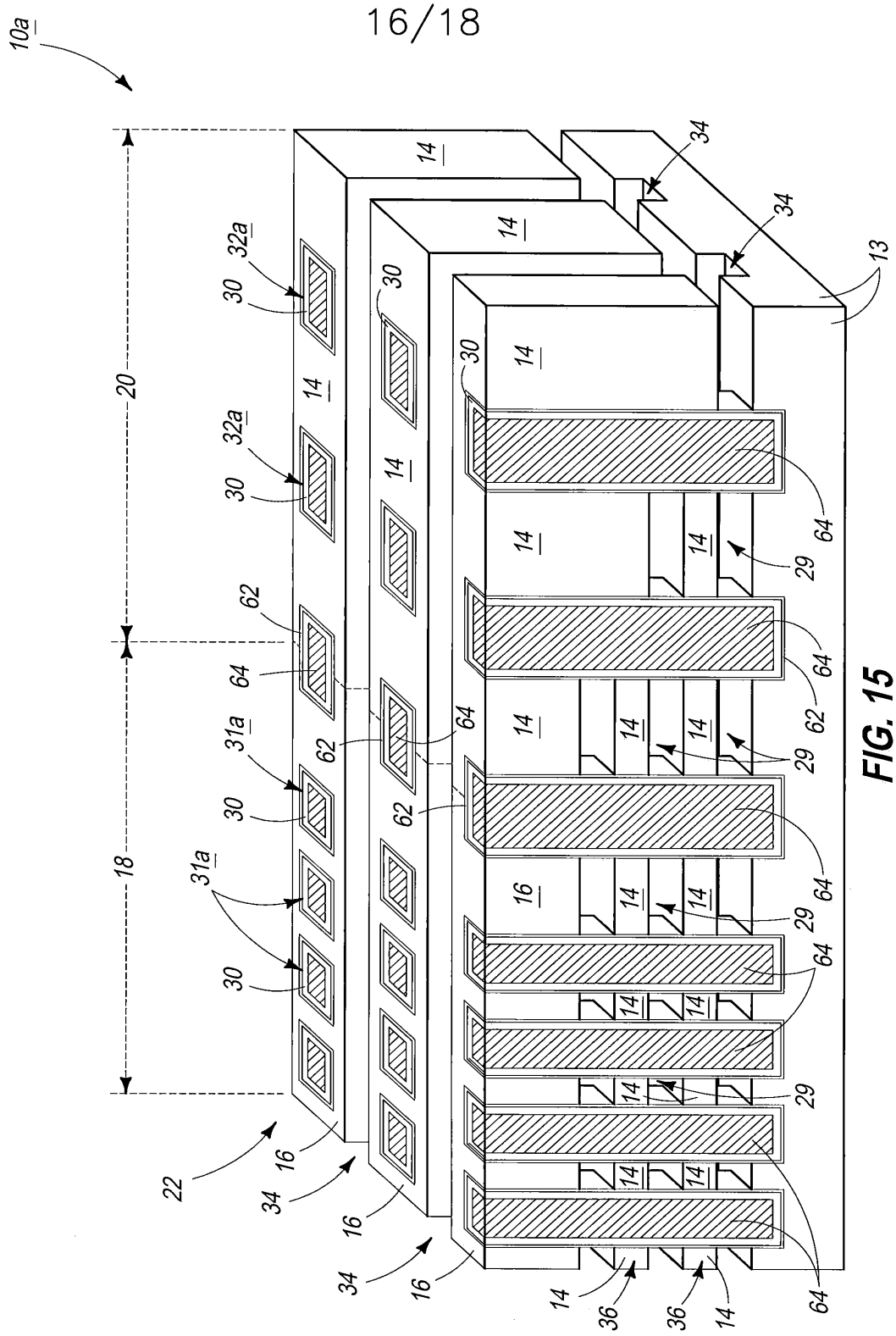



FIG. 15

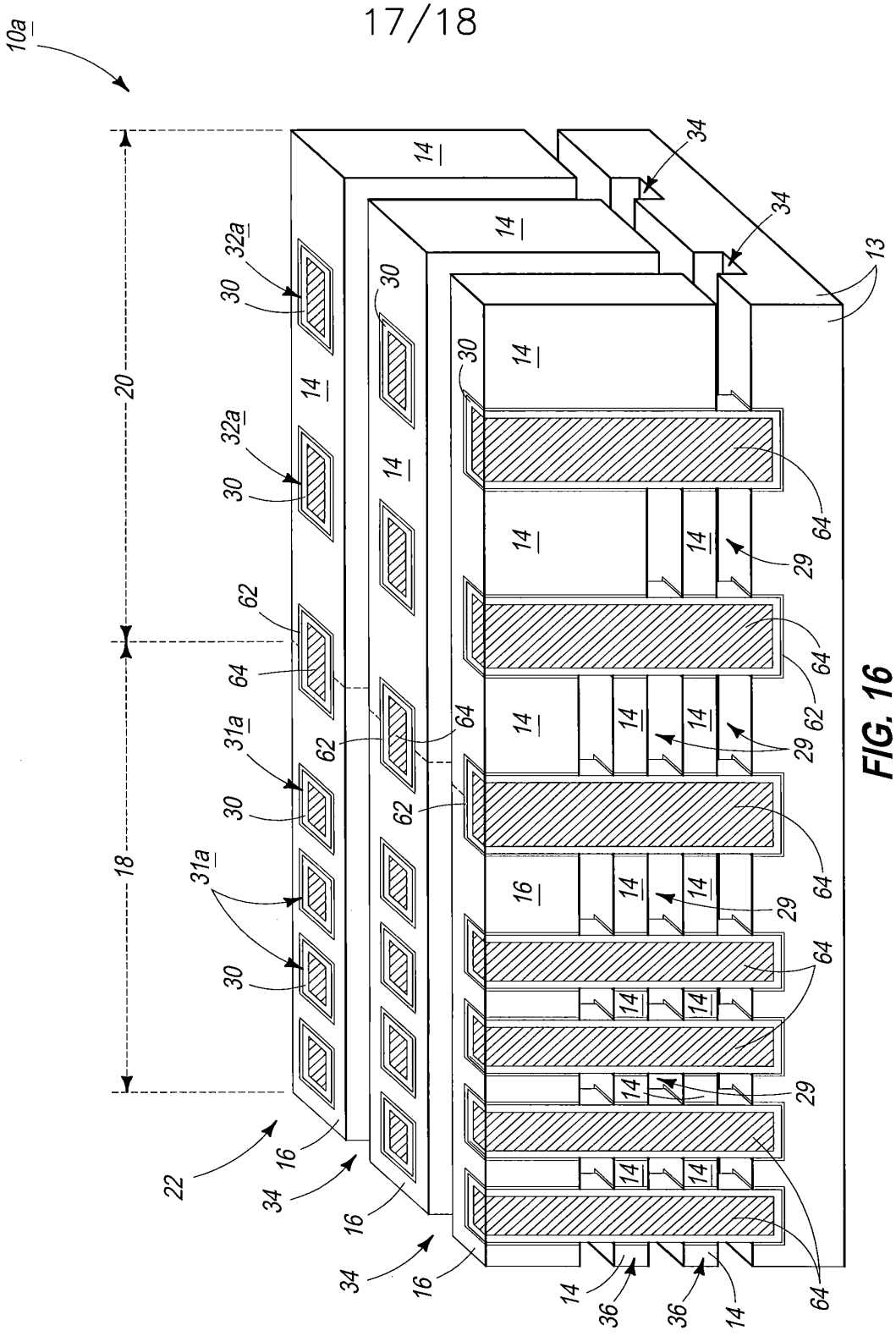



FIG. 16

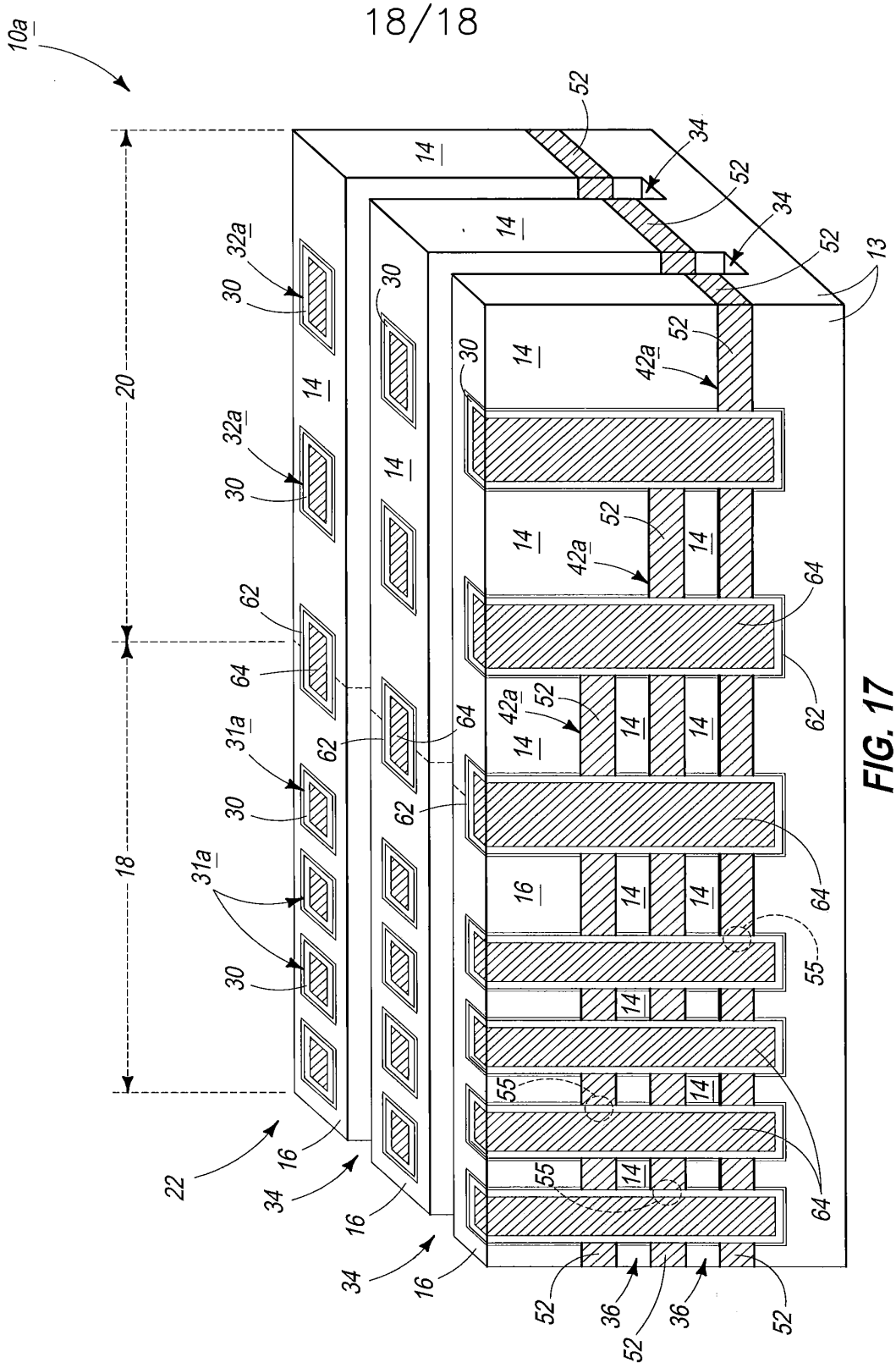



FIG. 17

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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# TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

| | |
|---|---|
| Application Number | Filed Herewith |
| Filing Date | Filed Herewith |
| First Named Inventor | Sanh D. Tang |
| Title | Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells |
| Art Unit | Unknown |
| Examiner Name | Unknown |
| Attorney Docket Number | MI22-6502 |

**SIGNATURE of Applicant or Patent Practitioner**

| | | | |
|---|---|---|---|
| Signature | /Mark S. Matkin/ | Date (Optional) | February 20, 2018 |
| Name | Mark S. Matkin | Registration Number | 32,268 |
| Title (if Applicant is a juristic entity) | Patent Practitioner | | |
| Applicant Name (if Applicant is a juristic entity) | Micron Technology, Inc. | | |

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

# POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

| Application Number | Filing Date |
|---|---|
| | |

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 128753

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

**Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:**

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

| | | | | | |
|---|---|---|---|---|---|
| Firm or Individual Name | | | | | |
| Address | | | | | |
| City | | State | | Zip | |
| Country | | | | | |
| Telephone | | Email | | | |

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Micron Technology, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

**SIGNATURE of Applicant for Patent**

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

| | | | |
|---|---|---|---|
| Signature | /Joel L. Poppen/ | Date (Optional) | |
| Name | Joel L. Poppen | | |
| Title | V.P. of Legal Affairs, General Counsel, and Corporate Secretary | | |

SNO

**NOTE:** Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

# ASSIGNMENT

## PARTIES TO THE ASSIGNMENT:

INVENTORS:

Sanh D. Tang
1273 N. Jullion Ave.
Boise, ID 83704
United States

Roger W. Lindsay
4376 Falconcrest Way
Boise, ID 83716
United States

Krishna K. Parat
4177 Hubbartt Drive
Palo Alto,CA 94306
United States

ASSIGNEE:

Micron Technology, Inc.
MS 1-525
8000 South Federal Way
Boise, ID 83716
United States

## BACKGROUND OF THIS ASSIGNMENT:

Inventors have conceived certain new and useful inventions disclosed in a United States patent application titled Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells.

Micron Technology, Inc. (hereinafter referred to as "ASSIGNEE") desires to acquire the entire right, title and interest in said inventions and with respect to any Letters Patent that may be granted with respect to the inventions in both the United States and in all foreign countries.

**THE PARTIES AGREE AS FOLLOWS:**

In consideration of good and valuable consideration, the receipt, sufficiency and adequacy of which is hereby acknowledged, INVENTORS have sold, assigned and transferred, and by these present do hereby sell, assign and transfer to ASSIGNEE the entire right, title and interest in the above-identified inventions and application and to any reissues, renewals, divisions or continuations of the application thereof, and hereby authorizes the Commissioner of Patents and Trademarks to issue such Letters Patent to ASSIGNEE for the sole use of ASSIGNEE, its successors or assigns.

INVENTORS further agree to execute, at the request and expense of ASSIGNEE, such other formal documents as may be required to fully convey the interest transferred herein and will similarly execute any patent application papers (foreign or domestic) required for the filing of any divisional, continuation, renewal or reissue of the patent application or resulting Letters Patent; and will generally do everything necessary or desirable to obtain and enforce proper protection for the inventions assigned hereby.

INVENTORS further assign to ASSIGNEE the whole right, title and interest in the inventions disclosed in the application throughout all

countries foreign to the United States. ASSIGNEE is hereby authorized to apply for patents relating to the inventions in its own name in countries where such procedure is proper; to claim the benefit of the International Convention; to file and prosecute International Applications relating to the inventions under the Patent Cooperation Treaty; and to file and prosecute applications relating to the inventions under the European Patent Convention. INVENTORS agree to execute applications relating to the inventions in those countries and under those conventions where it is necessary that the same be executed by the inventor, and to execute assignments of such applications and the resulting Letters Patent to ASSIGNEE as well as all other necessary papers in relation to such applications and Letters Patent. INVENTORS hereby consent that a copy of this assignment shall be deemed a full legal and formal equivalent of any document which may be required in any country as proof of the right of ASSIGNEE to apply for patent and other form of protection for said inventions and to claim the aforesaid benefit of the right of priority.

To be binding on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignee.

Dated: 04-08-11 Signature: Sanh D. Tang
Sanh D. Tang

State of Idaho )
) ss.
County of Ada )

On this 8th day of April, 2011, before me, Art Tyczka – Patent Asst (name and title of Notary Official), personally appeared Sanh D. Tang, known or identified to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed within the Assignment, and acknowledged to me that he/she executed the Assignment in his/her authorized capacity, and that by his/her signature on the Assignment, the person executed the Assignment.

ARTHUR TYCZKA NOTARY SEAL PUBLIC STATE OF IDAHO

My Commission Expires: 3-15-12

Dated: 4-11-2011 Signature: Roger W. Lindsay
Roger W. Lindsay

State of Idaho )
) ss.
County of Ada )

On this 11th day of April, 2011, before me, Art Tyczka – Patent Asst (name and title of Notary Official), personally appeared Roger W. Lindsay, known or identified to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed within the Assignment, and acknowledged to me that he/she executed the Assignment in his/her authorized capacity, and that by his/her signature on the Assignment, the person executed the Assignment.

ARTHUR TYCZKA NOTARY SEAL PUBLIC STATE OF IDAHO

My Commission Expires: 3-15-12

Dated: 4/5/2011 Signature: Krishna K. Parat
Krishna K. Parat

State of Idaho )
) ss.
County of Ada )

On this 5th day of April, 2011, before me, Art Tyczka - Notary Asst (name and title of Notary Official), personally appeared Krishna K. Parat, known or identified to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed within the Assignment, and acknowledged to me that he/she executed the Assignment in his/her authorized capacity, and that by his/her signature on the Assignment, the person executed the Assignment.

SEAL

ARTHUR TYCZKA NOTARY PUBLIC STATE OF IDAHO

My Commission Expires: 5-15-12