

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.
Petitioner

v.

MICRON TECHNOLOGY, INC.
Patent Owner

IPR2025-00500
U.S. Patent No. 10,475,737

**DECLARATION OF DR. KELIN J. KUHN IN SUPPORT OF PETITION
FOR *INTER PARTES REVIEW* OF U.S. PATENT 10,475,737**

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I, Kelin Kuhn of Winthrop, Washington, declare that:

I. Introduction

1. My name is Dr. Kelin J. Kuhn, and I am an adjunct professor in the Materials Science and Engineering Department at Cornell University. I have been retained on behalf of Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Petitioner”), to provide my opinions on certain issues related to U.S. Patent No. 10,475,737 (“the ’737 patent”) in connection with the above-captioned *inter partes* review (IPR) proceeding. In particular, I have been asked to provide my insights, analysis, and opinions regarding whether claims 1-12, 14, 15, 18, and 20-22 of the ’737 patent (“challenged claims”) are anticipated by and/or obvious over the prior art references identified below.

2. I understand that the ’737 patent is titled “Stack of horizontally extending and vertically overlapping features, methods of forming circuitry components, and methods of forming an array of memory cells,” names as inventors Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat, and is currently owned by Micron Technology, Inc (“Micron” or “Patent Owner”). I have considered the ’737 patent. I understand that the ’737 patent has been provided as EX1001.

3. I understand that the file history of the ’737 patent has been provided as EX1002. I have considered this file history, and I will refer to it as “the ’737 file history.”

4. I understand that the '737 patent is a continuation of a series of earlier-filed parent applications, the earliest of which was filed on April 12, 2011, as U.S. Patent Application No. 13/085,083 ("the '083 application"). For claims 18 and 20 of the '737 patent, I have opined whether they satisfy the written description requirement, and my opinion supports that claims 18 and 20 are not entitled to priority dates of any of its earlier-filed parent applications in Section VII.C. As to the rest of the challenged claims, I have been asked to assume the April 12, 2011 priority date for purposes of rendering my opinions in this Declaration.

5. My analysis and conclusions set forth in this Declaration are based on my educational background and experiences in the field. Before April 12, 2011, my level of skill in the art was at least that of a person of ordinary skill in the art (POSITA). I am qualified to opine concerning what a POSITA would have known and understood at the time of the '737 patent's purported invention. My analysis and conclusions herein are from the perspective of a POSITA as of April 12, 2011. My analysis and conclusions with respect to claims 18 and 20 remain the same from the perspective of a POSITA as of February 20, 2018, the filing date of the '737 patent, should the Board agree that claims 18 and 20 are not entitled to any priority dates before February 20, 2018.

6. As part of my independent analysis for this declaration, I have considered the following: the background knowledge/technologies that were

commonly known to persons of ordinary skill in this art during the time before the earliest claimed priority date for the '737 patent; my own knowledge and experiences gained from my work experience in the field of the '737 patent and related disciplines; and my experience in working with others involved in this field and related disciplines.

7. I am being compensated by YMTC at my standard hourly consulting rate of \$600 for my time on this matter. My compensation is not dependent on the outcome of this proceeding or any other proceeding between the parties.

8. As set forth herein, I have concluded that each of the challenged claims is anticipated and/or rendered obvious by the prior art based on the references described below and as described herein. In forming my opinions, I relied on the documents cited in this Declaration, which are identified in Section IV. These documents include patents, file histories, printed publications, and other related documents. As discussed below, each document is a type that experts in my field would have reasonably relied upon when forming their opinions. Further, experts in my field would have had access to each document either through the applicable patent offices and/or well-known libraries, conferences, or publications in the field. My opinions are also based upon my personal and professional experience.

II. Background and Qualifications

9. My qualifications including cases in which I was an expert are stated

more fully in my curriculum vitae, which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

10. I am qualified by education and experience to testify as an expert in the field of nonvolatile memory devices. Additionally, the following overview of my background pertains to my qualifications for providing expert testimony in this matter. I am over the age of 18 and am competent to write this Declaration. I have personal knowledge, or have developed knowledge, of these technologies based upon education, training, or experience of the matters set forth herein.

11. I received my B.S., magna cum laude, in Electrical Engineering from the University of Washington, Seattle in 1980, and received an M.S. and a Ph.D. in Electrical Engineering from Stanford University in 1985. I undertook post-doctoral work at Stanford from 1985 to 1987.

12. I am presently retired from industry. However, I still periodically engage in engineering projects for select clients and have a small business (Confluence Technology Services) to support that activity.

13. I am also currently an adjunct professor of Materials Science and Engineering at Cornell University, where my research interests are in the areas of quantum materials, post-CMOS technology, and spintronics.

14. For nearly a decade, beginning in 1987, I held faculty positions at the University of Washington, Seattle, beginning as a Research Assistant Professor in

Material Science and Engineering, then as Assistant Professor in Electrical and Computer Engineering, and finally as a tenured Associate Professor of Electrical and Computer Engineering. During this period, I worked in III-V molecular beam epitaxy and optoelectronics, and was awarded the University's highest accolade for a faculty member, the Distinguished Teaching Award, in 1995.

15. In 1997, I joined Intel Corporation ("Intel") at the Aloha Campus in Oregon as a Senior Process Engineer. I focused on front-end integration on the Intel 0.35 μ m process technology. In this role, I was responsible for the silicide section of the process flow, interaction with the reliability community, and integration on the CMOS camera chip project.

16. In 1999, I was transferred to Portland Technology Development at Ronler Acres, Oregon, as a Senior Process Engineer. I worked on front-end integration on the 130 nm CMOS generation. In this role, I was responsible for the isolation section of the process flow as well as integration of Optical Proximity Correction technologies into 130 nm.

17. In 2001, I advanced to the title of Principal Engineer. In 2002, I was promoted to the role of Process Program Manager for Intel's 90 nm communications process technology. Over a three-year period, my team developed a derivative analog/RF technology (including a SiGe bipolar junction transistor ("BJT")) on top of Intel's premium 90 nm microprocessor process.

18. In 2004, I advanced to the title of Senior Principal Engineer and was promoted to the role of Device Technology Manager of the pathfinding team at Intel that was responsible for the high-k metal-gate transistor architecture of Intel's 45 nm microprocessor processor technology. I received an Intel Achievement Award in 2006 for my work on the high-k metal gate.

19. In 2007, I achieved the title of Intel Fellow and became Director of Advanced Device Technology. Fellow is the highest level of technical achievement within Intel, with approximately 50 Fellows among approximately 100,000 total employees. My work evolved to a strategic role in overseeing the transition of advanced device technologies from research into development. In this role, I played an active part in the transfer of transistor technology for the 32 nm node, 22 nm node, and 14 nm node (the last two nodes involving Intel's FinFET device). I received a second Intel achievement award in 2008 for my work on Intel's FinFET device.

20. In 2009, my title remained the same, but my role transitioned from development (in Portland Technology Development, at Ronler Acres) to research (in the Components Research Group, still at Ronler Acres). From 2009 until my retirement from Intel in 2014, I researched advanced device architectures for Intel processes in the five-to-ten year time frame.

21. While much of my later work at Intel still remains confidential, certain aspects of my work during this period are featured in my book CMOS And Beyond:

Logic Switches for Terascale Integrated Circuits (Co-Editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015), as well as in my paper “Considerations for Ultimate CMOS Scaling” (IEEE Trans. on Elec. Dev., Vol. 59, No. 7, 2012), winner of the 2013 Paul Rappaport Award.

22. Since my retirement in 2014, my consulting work has included a variety of semiconductor related projects. While the detailed technical content is, of course, protected by client confidentiality, these projects include FinFETs, vertical power transistors, solar cells, conventional (planar) MOS, and flash.

23. I am the author of more than 100 technical papers in electronics and photonics. I am currently the Associate Editor in Chief (AEiC) of IEEE Electron Device Letters, having served as an editor since 2015, and as AEiC since 2024.

24. A few of my other representative journal publications include: “Understanding the feasibility of scaled III–V TFET for logic by bridging atomistic simulations and experimental results,” (Symposium on VLSI Technology, 2012); “Process Technology Variation,” (IEEE Transactions on Electron Devices, Vol. 58, No. 8, 2011); “A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging,” (2007 IEEE International Electron Devices Meeting); and “Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm,” (IEEE Electron Device Letters, Vol. 32, No. 9, 2011).

25. A few representative book chapters include “The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8. Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications,” Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616).

26. I am an inventor of approximately 80 granted U.S. patents in the field of semiconductor technology.

27. A few of my other relevant honors include being a Fellow at the Institute of Electrical and Electronics Engineers (“IEEE”), a recipient of the IEEE Frederik Philips Award (2016), a recipient of the IEEE Paul Rappaport Award (2013), the recipient of eleven Intel Divisional Awards, and election to the National Academy of Engineering (2023). Earlier in my career, I received the NSF Presidential Young Investigator Award.

28. As specifically relevant to this project, I want to highlight the 3D gate-last vertical gate-all-around (GAA) devices and the 3D vertical GAA arrays that are discussed at some length in “Considerations for Ultimate CMOS Scaling” (see Fig. 15 in particular). I also want to highlight on-going proprietary and confidential work, in the matter of Silicon Storage Technology, Inc. vs. Taiwan Semiconductor Manufacturing Company involving flash.

29. Attached as Appendix A to this report is a current copy of my curriculum vitae, which outlines my academic, professional, and experiential qualifications in the semiconductor and integrated circuit industries, as well as a list of publications I have authored and co-authored and presentations I have given.

III. Level of Ordinary Skill in the Art

30. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a POSITA at the time of the alleged invention. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field, the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art including the art cited below.

31. In general, my analyses and conclusions herein are from the perspective of a POSITA as of April 12, 2011. However, as discussed in Section VII.C, I have opined whether claims 18 and 20 of the '737 patent satisfy the written description requirement, and my opinion supports that claims 18 and 20 are not entitled to priority dates of any of its earlier-filed parent applications. In this regard, my

analyses and conclusions with respect to claims 18 and 20 (using the perspective of a POSITA as of April 12, 2011) remain the same from the perspective of a POSITA as of February 20, 2018, the filing date of the '737 patent, should the Board agree that claims 18 and 20 are not entitled to any priority dates before February 20, 2018. I have been asked to assume that the rest of the challenged claims are entitled to the April 12, 2011 filing date of the '083 application, for the purposes of this Declaration only.

32. Upon consideration of the relevant factors listed above, in my opinion, a POSITA at the time of the claimed invention would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa.

33. Well before April 12, 2011, my level of skill in the art was at least that of a person having ordinary skill. I am qualified to opine concerning what a POSITA would have known and understood at the time of the '737 patent's purported invention. My analysis and conclusions herein are from the perspective of a POSITA as of April 12, 2011. A different priority date would not change my opinions as long as the identified prior art were still prior art.

IV. Materials Considered and Relied Upon

34. In reaching the conclusions described in this declaration, I have relied

on the documents and materials cited herein as well as those identified in this Declaration, including but not limited to, the '737 patent, the prosecution history of the '737 patent, and prior art references cited herein. These materials include patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions.

35. In the cited references, all emphasis is added unless otherwise noted.

36. I have also relied on my education, training, research, knowledge, and personal and professional experience in the relevant technologies that were already in use prior to the claimed invention.

- EX1001: U.S. Patent No. 10,475,737 to Tang et al. (“the '737 patent”).
- EX1002: Prosecution History of the '737 patent (“the '737 file history”).
- EX1004: U.S. Patent Application Publication No. 2010/0133598 in the name of Chae et al. (“Chae”).
- EX1005: U.S. Patent Application Publication No. 2011/0156132 in the name of Kiyotoshi et al. (“Kiyotoshi”).
- EX1006: U.S. Patent Application Publication No. 2017/0352674 in the name of Jeong et al. (“Jeong”).
- EX1007: U.S. Patent Application Publication No. 2011/0151667 in the name of Hwang et al. (“Hwang”).
- EX1008: U.S. Patent No. 9,929,175 to Tang et al. (“the '175 patent”).
- EX1009: U.S. Patent No. 9,564,471 to Tang et al. (“the '471 patent”).

- EX1010: U.S. Patent No. 9,318,430 to Tang et al. (“the ’430 patent”).
- EX1011: U.S. Patent No. 8,945,996 to Tang et al. (“the ’996 patent”).
- EX1012: Joint Claim Construction and Prehearing Statement (Patent Local Rule 4-3), Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC., No. 3:23-cv-05792-RFL, D.I. 105 (N.D. Cal. August 19, 2024) (“Claim Construction”).
- EX1013: “Solid” – Merriam-Webster Online Dictionary 2010, Retrieved February 20, 2010, from <https://web.archive.org/web/20100218235823/http://www.merriam-webster.com/dictionary/solid> (“MW”).
- EX1014: Bill Arnold, “Shrinking Possibilities,” IEEE Spectrum, vol. 46, no. 4, April 2009, pp. 26-28, 50-56 (“Arnold”).
- EX1015: U.S. Patent Application Publication No. 2007/0066004 in the name of Nakagawa (“Nakagawa”).
- EX1016: Y. Fukuzumi et al., “Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory,” Proceedings of the 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, December 10-12, 2007, pp. 449–452 (“Fukuzumi”).
- EX1017: S. Bangsaruntip et al., “Universality of Short-Channel Effects in Undoped-Body Silicon Nanowire MOSFETs,” IEEE Electron Device Letters, vol. 31, no. 9, Sept. 2010, pp. 903-905 (“Bangsaruntip”).
- EX1018: U.S. Patent Application Publication No. 2010/0327252 in the name of Lee (“Lee”).
- EX1019: Prosecution History of the ’175 patent (“the ’175 file history”).

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- EX1020: J. Jang et al., “Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193 (“Jang”).
 - EX1021: K. Joo et al., “Novel Transition Layer Engineered Si Nanocrystal Flash Memory with MHSOS Structure Featuring Large V_{th} Window and Fast P/E Speed,” IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest., Washington, DC, USA, 2005, pp. 865-868 (“Joo”).
 - EX1022: S. Park et al., “A New Operating Scheme by Switching the Polarity of Program/Erase Bias for Partially Oxidized Amorphous-Si-Based Charge-Trap Memory,” IEEE Transactions on Electron Devices, vol. 53, no. 11, Nov. 2006, pp. 2847-2849 (“Park”).
 - EX1023: M. Rosmeulen et al., “Silicon Rich Oxides as an Alternative Charge Trapping Medium in Fowler-Nordheim and Hot Carrier Type Non-Volatile-Memory Cells,” Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 189-192 (“Rosmeulen”).

V. Legal Standards

37. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

38. In formulating my opinions, I have been informed of certain legal understandings relevant to my opinions. In formulating my opinions, I have relied on the legal understandings I have been provided with as set forth in this declaration.

39. I have been informed that in *inter partes review* proceedings, invalidity must be shown under a preponderance of the evidence standard.

A. My Understanding of Claim Construction

40. I have been informed that patent claims are construed from the viewpoint of a POSITA of the patent at the time of the invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a POSITA in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification, and the prosecution history (i.e., the intrinsic record).

41. I have further been informed that a POSITA must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner’s rejection, by clearly and unambiguously arguing

to overcome or distinguish a prior art reference, or clearly and unambiguously disavowing claim coverage.

42. In interpreting the meaning of the claim language, I understand that a POSITA may also consider “extrinsic” evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. For example, this can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

B. Legal Standard for Priority Date

43. I understand that to obtain the priority benefit of an earlier-filed application, the claims must meet the written description requirement of 35 U.S.C. §112.

44. I also understand that to satisfy the written description requirement, a patent specification must describe the claimed invention in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. An applicant shows that the inventor was in possession of the

claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. I was informed that a prior application itself must describe an invention, and do so in sufficient detail that one skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought.

C. My Understanding of Anticipation

45. I understand that a patent claim is invalid as “anticipated” if all the limitations of the claim are present, either expressly or inherently, in a single prior art publication or patent.

46. I also understand that a prior art reference can disclose a claimed feature because the feature is expressly described or because the feature is inherent in the disclosure. I understand that something is inherent in a prior art reference if the missing descriptive matter must necessarily be present, not merely probably or possibly present, and it would be so recognized by a POSITA as of the priority date of the patent. I understand that it is acceptable to examine evidence outside of the prior art reference (i.e., extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it.

47. I have further been informed that where a reference discloses multiple embodiments, the reference should not be limited to a preferred embodiment.

Instead, each disclosed embodiment may anticipate.

48. Moreover, I have been informed that as part of an anticipation analysis, it is proper to take into account not only specific teachings of the reference, but also the inferences that one skilled in the art would reasonably be expected to draw therefrom. A reference can anticipate a claim even if it does not expressly spell out all the limitations arranged or combined as in the claim, if a POSITA, reading the reference, would at once envisage the claimed arrangement or combination.

D. My Understanding of Obviousness

49. I understand that a claim may be invalid if the subject matter described by the claim as a whole would have been obvious to a hypothetical POSITA in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a hypothetical POSITA and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

50. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the

reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering their problem.

51. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

52. I have also been advised that in considering whether a claimed invention would have been obvious over a combination of prior art references, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the marketplace, and/or the background knowledge possessed by a POSITA. I

understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a POSITA can implement a predictable variation, the variation is likely obvious;
- If a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls whether the claim is obvious;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;

-
- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
 - “Common sense” teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a POSITA will be able to fit the teachings of multiple patents together like pieces of a puzzle;
 - A POSITA is also a person of ordinary creativity, and is not an automaton;
 - A patent claim can be proved obvious by showing that the claimed combination of elements was “obvious to try,” particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a POSITA would have had good reason to pursue the known options within his or her technical grasp; and
 - One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

53. I further understand that, in making a determination as to whether the claimed invention would have been obvious to a POSITA, the Board may consider certain objective factors if they are present, such as: commercial success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be

relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence, and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with predictable results) that is sufficiently strong.

VI. Technology Background

54. Three-dimensional (3D)—or vertical—NAND flash memory is a type of nonvolatile memory in which the memory cells are stacked vertically in multiple layers/levels to increase storage density, compared with traditional two-dimensional (2D)—or planar—NAND flash memory, where all the memory cells are arranged in a simple two-dimensional matrix.

55. Since memory cells and their gate lines (e.g., word lines) are arranged at different vertical levels in 3D NAND, a stair-like structure (a.k.a., staircase structure) is used to allow gate line contact structures to land on the contact regions at each stair step of the stair-like structure at the end of the memory stack, enabling interconnections of the gate lines of the memory cells at different levels, respectively. One of such stair-like structures back to 2009 is shown in FIG. A below (FIG. 6 of Jang, EX1020), which is a cross-sectional scanning electron microscopy (SEM) image at cell array edge showing stair-like shaped word-line pad structure. EX1020,

pp. 192-193, Architecture and Key Features of TCAT Flash, ¶1, FIG. 6. As shown in the stair-like structure in FIG. A, the farther a gate line extends horizontally toward the end of the stack, the lower its position within the stack.

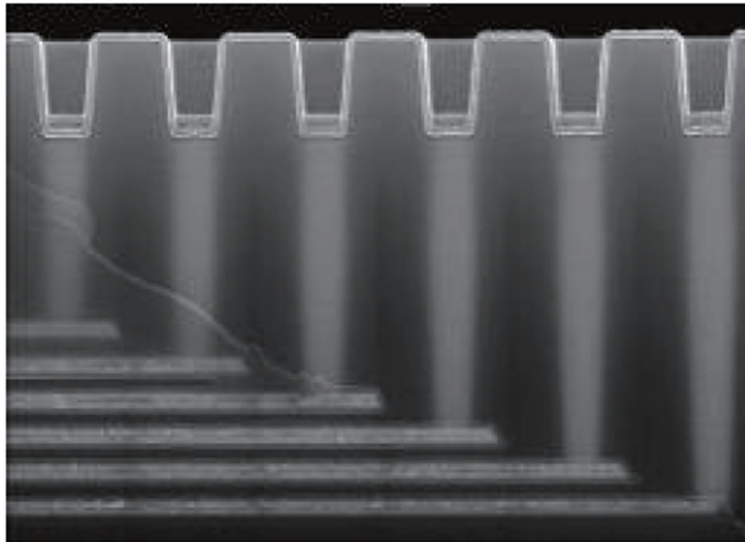


FIG. A – FIG. 6 of Jang

56. Another important concept for modern 3D NAND flash memory devices is the so-called “gate replacement” process for forming the gate lines (“gate replacement” technology is not unique to NAND flash, but was originally developed in the mid-2000s for manufacturing implementation of planar HiK-metal gate logic CMOS technologies). As illustrated in FIG. B below: an alternating stack of silicon oxide layer (in gray) and silicon nitride layer (in yellow, used as “sacrificial layers”) is deposited, and polysilicon channel structures (in light green), as well as word line (W/L)-cuts, are formed vertically through the stack in the cell array region (FIG. 4(a)); the silicon nitride sacrificial layers are then selectively removed using wet

etching from the word line cuts (FIG. 4(b)); gate dielectric (in orange) and conductor (in dark green, e.g., tungsten, W) are deposited to fill the recesses from the word line cuts (FIG. 4(c)); the gate lines are separated by removing the conductor from the word line cuts (FIG. 4(d)). EX1020, pp. 192-193, Architecture and Key Features of TCAT Flash, ¶1, FIG. 4.

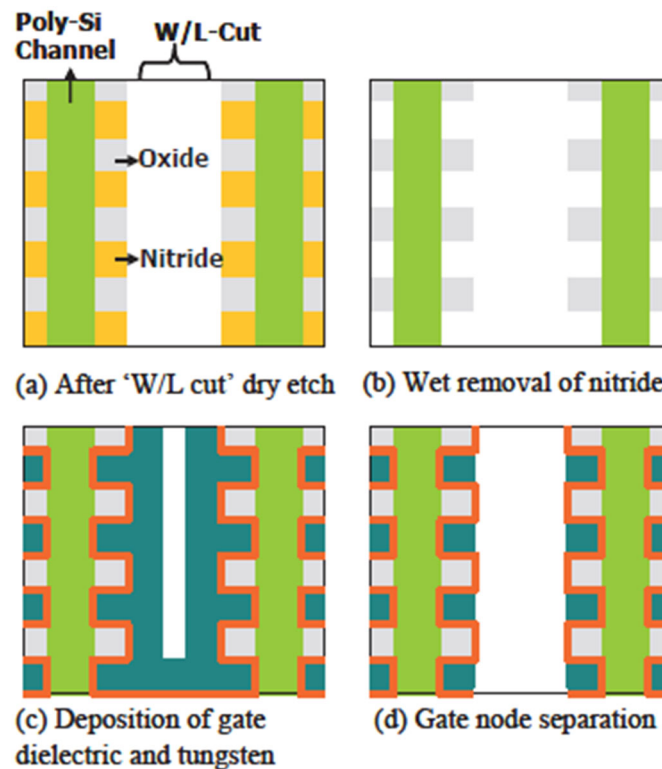


FIG. B – FIG. 4 of Jang

57. After the removal of the silicon nitride sacrificial layers and prior to the deposition of gate dielectric and conductor materials, the recesses between silicon oxide layers are supported in the cell array region by the channel structures, but not supported in the end region where the stair-like structure is formed because channel structures are not formed in the end region. Therefore, the silicon oxide layers may

bend or even collapse in the end region of the stack during the gate replacement process when fabricating a 3D NAND flash memory device.

VII. Overview of the '737 Patent

A. Subject Matter Overview

58. The '737 patent was issued on November 12, 2019 from U.S. Patent Application No. 15/900,188 (“the '188 application”), filed on February 20, 2018, and is a continuation of the '175 patent, filed on January 4, 2017, which is a continuation of the '471 patent, filed on April 11, 2016, which is a divisional of the '430 patent,” filed on January 22, 2015, which is a divisional of the '996 patent, filed on April 12, 2011. EX1001, (10), (21), (22), (45), (60).

59. The '737 patent relates to stacks of horizontally extending and vertically overlapping features, and methods of forming circuitry components and an array of memory cells. EX1001, 1:36-39. The '737 patent warns that, when forming the stacks, the features in the end portion “may be sagged, bent, or broken due to lack of support” when the sacrificial material between the features is removed. EX1001, 7:58-64. As discussed above in Section VI, this problem during the gate replacement process was widely recognized in the industry before the '737 patent. The '737 patent proposes forming “dummy structures” vertically through the features in the end portion to support them from vertical movement, purportedly solving this issue. EX1001, 7:52-58, 7:64-8:2.

60. A substrate fragment 10 described in FIG. 13 of the '737 patent, which is related to the challenged claims, is reproduced below as FIG. C with my annotations.

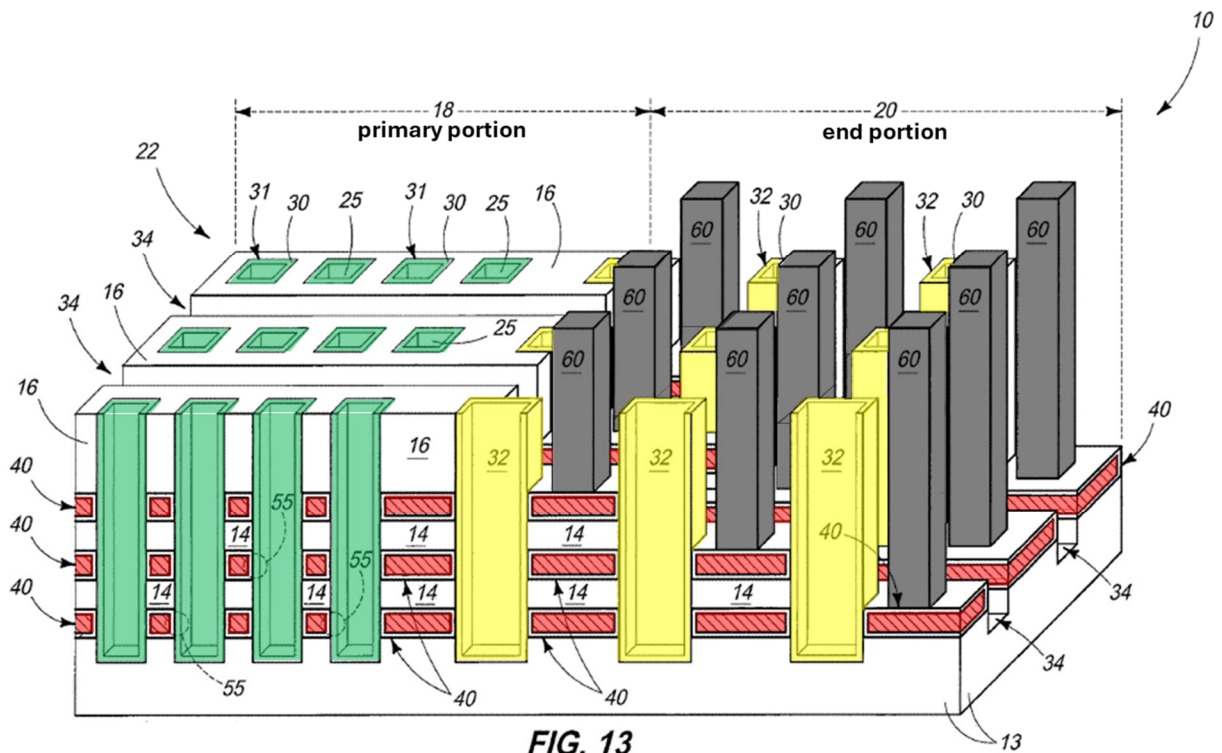


FIG. 13
FIG. C – FIG. 13 of the '737 patent (annotated)

61. FIG. 13 of the '737 patent depicts a stack of vertically overlapping materials 40 that extend horizontally across a primary portion 18 and an end portion 20 of the stack in a substrate fragment 10. End portion 20 has a “stair step-like construction” in which materials 40 extend farther in the horizontal direction, moving deeper into the stack. EX1001, 4:57-59; 5:1-7. This “stair step-like construction” is merely one example of the well-known stair-like structure discussed in Section VI above, similar to the one illustrated in FIG. A of this Declaration.

62. Material 40 includes a horizontal extending conductive line 42 (in red). EX1001, 8:31-39. Although the numerical label “42” for the conductive lines does not appear in FIG. 13, it is shown in FIGs. 11 and 11A, referring to the same structures. EX1001, FIGs. 11 and 11A. The ’737 patent explains that “the features may be horizontally extending lines, for example formed of any one or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s).” EX1001, 11:28-31. Thus, the horizontal extending conductive lines 42 (in red) are “features,” according to the ’737 patent.

63. As shown in FIG. 13 of the ’737 patent, operative structures 31 (in green) and dummy structures 32 (in yellow) are formed vertically through conductive lines 42 of materials 40 in primary portion 18 and end portion 20, respectively. EX1001, 8:17-20. Additionally, contacts 60 (in black) in end portion 20 are connected to the respective conductive line 42 of materials 40. EX1001, 8:45-48, 51-56.

64. Regarding operative structures 31 (in green) and dummy structures 32 (in yellow), the ’737 patent explains the following:

Operative structures (e.g., **circuit components**, such as local vertical extensions) are formed therewith within the openings in the primary portion, and dummy structures (e.g. dummy vertical extensions) are formed therewith within the openings in the end portion. In the context of this document, a “dummy” structure is **a structure which is used to mimic a physical property of another structure (e.g., load carrying ability of an operative structure) and which may comprise a circuit**

inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive).
EX1001, 6:22-32.

B. File History of the '737 Patent

65. I have reviewed the file history of the '737 patent. Upon the issuance of the first non-final Office Action dated April 15, 2019, claims 39, 40, 42-50, and 52-56 (now issued claims 1-11 and 13-17) were pending in the application and were rejected on the ground of nonstatutory double patenting over the '175 patent. EX1002, pp. 38-48. Claim 51 (now issued claim 12) was rejected over the parent '175 patent in view of U.S. Patent Application Publication No. 2010/0244119 in the name of Fukuzumi et al. ("Fukuzumi"). EX1002, p. 48.

66. The Office Action also allowed claims 57-61 (now issued claims 18-22) because the prior art on the record did not teach "vertical contacts in the end portion connecting with individual of the control gate lines, the contacts and dummy structures having different horizontal cross-sections relative one another" in claim 57, and "vertical contacts in the end portion connecting with individual of the control gate lines, at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line" in claim 60. EX1002, pp. 48-49.

67. In the Response to the Office Action filed on April 18, 2019, Applicant of the '737 patent filed a Terminal Disclaimer with respect to the '175 patent without

making additional substantive arguments. EX1002, pp. 22, 35.

68. The Examiner subsequently issued the Notice of Allowance on July 9, 2019. EX1002, at 9.

C. Written Description Requirement for Claims 18 and 20

69. On its face, the '737 patent is a continuation of a series of earlier-filed parent applications, which were issued as the '175 patent, '471 patent, '430 patent, and '996 patent ("parent patents"). EX1001, (60).

70. I have been asked to analyze whether the specifications of each of the parent patents describe the claimed invention of claims 18 and 20 in sufficient detail that one skilled in the art can reasonably conclude that the inventor had possession of the claimed invention. My opinion is that a POSITA cannot reasonably conclude that the inventor of the parent patents had possession of the claimed invention, in particular, the features related to "the contacts and dummy structures having different horizontal cross-sections relative one another" recited in independent claim 18 and "different horizontal cross-sections have different values of total horizontal area relative one another" in dependent claim 20, because none of the parent patents describe these features with reasonable clarity, let alone in sufficient detail.

71. Specifically, none of the specifications of any parent patents disclose the horizontal cross-section of **contacts** at all, much less provide a comparison between the horizontal cross-section of contacts and the horizontal cross-section of

dummy structures. The only place that mentions a “cross section” in the specifications is about openings 25 and 27, where operative structures 31 (instead of contacts) and dummy structures 32 are formed, respectively. EX1008, 5:53-58, 6:45-49; EX1009, 5:45-50, 6:37-41; EX1010, 5:39-44, 6:30-35; EX1011, 5:27-32, 6:18-23. It is clear that openings 25 (and operative structures 31 formed therein) do not correspond to the claimed “contacts” (e.g., contacts 60 in the specifications and drawings), and the horizontal cross-section of openings 25 (operative structures 31) is not even associated with the horizontal cross-section of the contacts.

72. I also noted that FIG. 13 of the parent patents (which are identical among all the parent patents) is the only drawing that illustrates contacts (e.g., contacts 60). However, FIG. 13 still does not convey with reasonable clarity to a POSITA that the inventor was in possession of the claimed subject matters related to the horizontal cross-section of contacts and dummy structures at least because FIG. 13 does not depict, nor does the associated text describes, a complete horizontal cross-section of any dummy structure 32 with sufficient detail for a POSITA to compare the horizontal cross-sections between dummy structures 32 and contacts 60. Moreover, since the parent patents clearly state that contacts 60 are “**diagrammatically** shown in FIG. 13,” any comparison result about the dimensions or shapes of contacts 60 based on FIG.13 is unreasonable as FIG.13 is not to scale or intended to convey the dimensions or shapes of contacts 60. EX1008, 8:42-46;

EX1009, 8:34-38; EX1010, 8:22-26; EX1011, 8:10-14.

D. Interpretation of the '737 Patent Challenged Claims

73. I have been instructed that the challenged claims 1-12, 14, 15, 18, and 20-22 of the '737 patent are to be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of the alleged invention in light of the specification and the prosecution history pertaining to the patent; except that for the term “dummy structure,” I have been asked to assume it means “electrically inoperable structure that mimics a physical property of an operative structure.” I have followed these principles in my analysis set forth in this Declaration. I reserve the right to supplement my opinions in this Declaration to the extent that any parties later propose claim constructions for any claim terms in the '737 patent.

VIII. Overview of the Cited References

74. General descriptions provided for the following references and combinations thereof are incorporated into each subsection and mapping of the claims that include citations to these references.

A. Chae (EX1004)

75. Chae is directed to nonvolatile memory devices and their fabricating methods. EX1004, [0002]. Chae's goals include “reducing the resistance of gate electrodes,” “preventing process defects,” and improving the “operation speed of the

blue)] that are connected in series between the upper and lower select transistors UST and LST.” EX1004, [0041]-[0043], see also [0005]-[0006]. Chae also discloses that “upper select transistors UST are connected to the upper select lines USL1~USL3, and the lower select transistors LST are connected respectively to the lower select lines LSL. The memory cells MC are connected respectively to the word lines WL1~WL4.” EX1004, [0044].

79. FIGs. E and F below, with my annotations, show the plan view and cross-sectional view of the fifth embodiment of Chae, respectively. I noted that FIG. 15E refers to the same fifth embodiment as FIG. 10, and is taken along the line II-II’ of FIG. 10. EX1004, [0122]. Chae, in its fifth embodiment, discloses a nonvolatile memory device having a stack of conductive line-shaped gate electrodes 250 (in red) extending horizontally and overlapping vertically, which include upper and lower select lines USL and LSL and word lines WL. EX1004, [0078], [0130]. Chae also discloses that the stack includes a memory cell region MR (labeled as “primary portion”) and a contact region CR (labeled as “end portion”) “formed in a stair shape.” EX1004, [0078], [0132].

Fig. 10

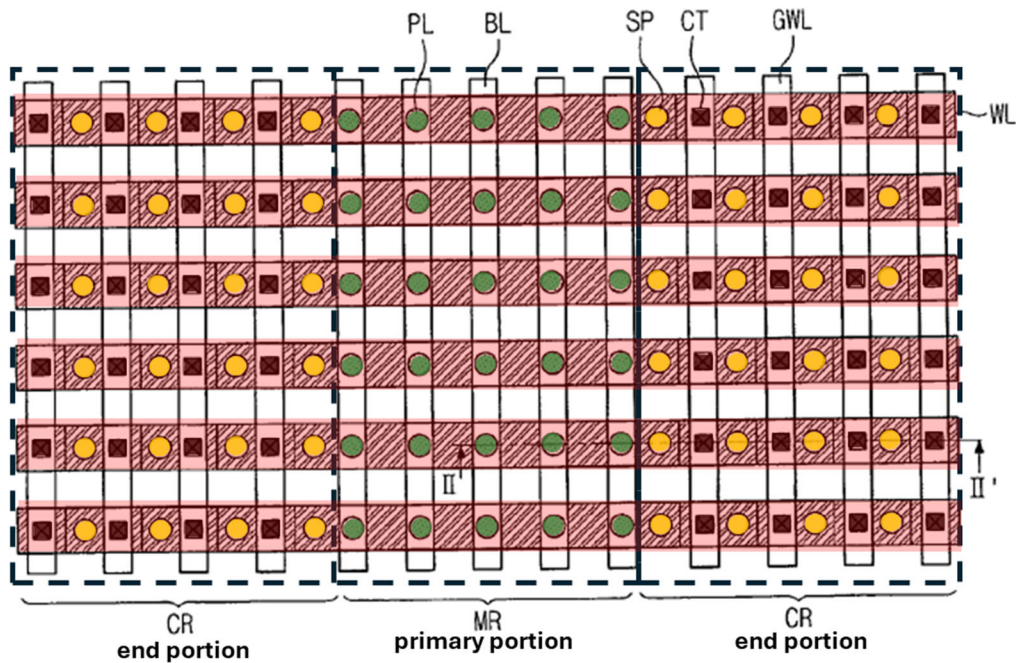


FIG. E – FIG. 10 of Chae (annotated)

Fig. 15E

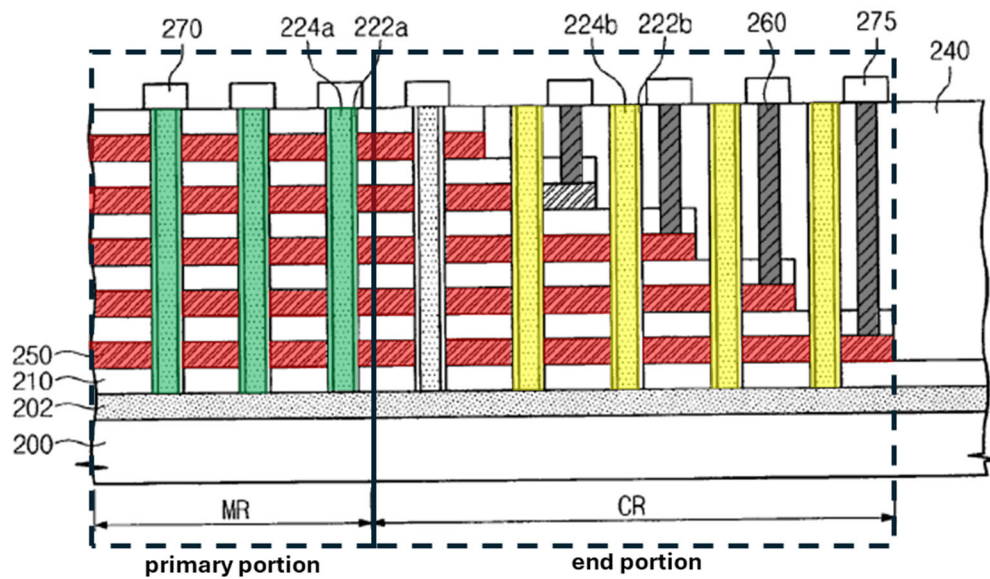


FIG. F – FIG. 15E of Chae (annotated)

80. As shown in FIGs. E and F above, the nonvolatile memory device also includes active pillars PL 224a with charge storage layers 222a (collectively in green) extending vertically through gate electrodes 250 (in red) in memory cell region MR, as well as supporters SP 224b with charge storage layers 222b (collectively in yellow) extending vertically through gate electrodes 250 (in red) in contact region CR. EX1004, [0078], [0126], [0128]. The nonvolatile memory device further includes contact plugs CT 260 (in black), each of which extends and connects to a respective gate electrode 250 (in red) in contact region CR. EX1004, [0131].

81. Specifically, for supporter 224b with charge storage layers 222b, Chae discloses, or at least suggests, that they are formed in the same process with the same structures and materials as active pillars 224a with charge storage layers 222a:

Thereafter, charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b. That is, charge storage layers 222a and 222b may be formed around the supporters 224b of the contact region CR and the active pillars 224a of the memory cell region MR. Also, the active pillars 224a and the supporters 224b may be formed to the same length. EX1004, [0128].

Throughout the specification, like reference numerals refer to like elements. EX1004, [0037].

82. Chae also discloses that supporters 224b are used to prevent dielectric layers from collapsing during the gate replacement process in contact region CR,

similar to the role of active pillars 224a in memory cell region MR:

Thereafter, an etchant having a high etch selectivity with respect to the first dielectric layer 210 are supplied between the line-shaped stack structures to remove the second dielectric layers 215. Accordingly, an empty space is formed between the first dielectric layers 210 that are perpendicular to the semiconductor substrate 200 and are spaced apart from each other. The first dielectric layers 210 spaced apart from each other may be supported by the active pillars 224a of the memory cell region MR, which are perpendicular to the semiconductor substrate 200, and the supporters 224b of the contact region CR. That is, the second dielectric layers 215¹ can be prevented from collapsing or getting near to each other during the removing of the second dielectric layers 215 through a wet etch process.
EX1004, [0129].

83. Chae further discloses that supporters SP 224b are electrically inoperable:

In this embodiment, because the supporters SP of the contact region CR are not connected to the bit lines BL, they do not affect the operation of the nonvolatile memory device.
EX1004, [0081].

Because a conductive pattern such as the global word line 275 or the bit line 270 is not formed on the supporters 224b, it does not affect the operation of the nonvolatile memory device according to the exemplary embodiment of the inventive concept.
EX1004, [0134].

B. Kiyotoshi (EX1005)

84. Kiyotoshi relates to nonvolatile semiconductor memory devices.

¹ A POSITA would have recognized that the “second dielectric layers 215” is a typographical error and should instead be “first dielectric layers 210” based on the context.

EX1005, [0003]. Kiyotoshi recognizes the same issue of dielectric layers collapsing during the gate replacement process as Chae and the '737 patent, and proposes the same method to solve the problem: forming dummy semiconductor films 131 to provide support in a word-line contact region 20. EX1005, [0127].

85. Kiyotoshi distinguishes the hollow cylindrical semiconductor films 131 formed in word-line contact region 20 from those formed in a memory cell region 11: the hollow cylindrical semiconductor films 131 in memory cell region 11 form “memory strings MS,” whereas the hollow cylindrical semiconductor films 131 in word-line contact region 20 “do not form the memory strings MS and are **dummy** semiconductor films 131.” EX1005, [0116].

86. As shown in the following FIG. G with my annotations made to the sectional view of the memory cell region in FIG. 29C and the two sectional views of the word-line contact region in FIGs. 29E and 29D, Kiyotoshi, in its fourth embodiment, discloses the following:

- i. A stack of horizontally extending and vertically overlapping gate electrode films 134 (in red).
- ii. Semiconductor films 131 with dielectric films 132 (collectively in green), each extending vertically through gate electrode films 134 (in red) in memory cell region 11 (labeled as “primary portion”).
- iii. Dummy semiconductor films 131 with dielectric films 132

(collectively in yellow), each extending vertically through gate electrode films 134 (in red) in word-line contact region 20 (labeled as “end portion”).

- iv. Contacts 145 (in black) in word-line contact region 20 and each connecting with a respective one of gate electrode films 134 (in red).

EX1005, [0114], [0116]-[0117].

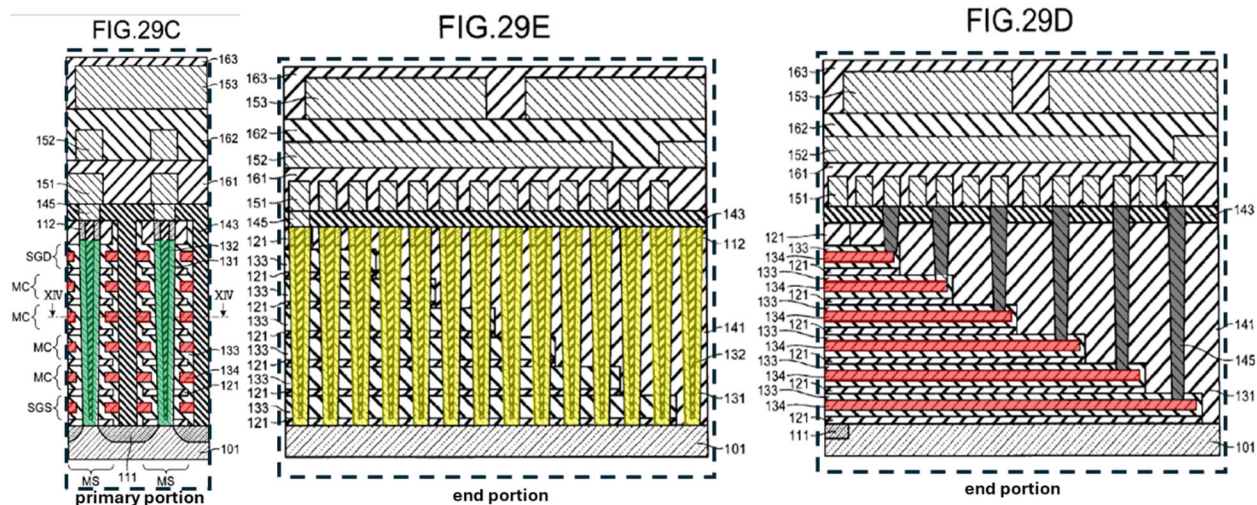


FIG. G – FIGs. 29C-29E of Kiyotoshi (annotated)

87. FIG. H below, with my annotations, depicts the manufacturing process of semiconductor films 131 and dielectric films 132 with respect to the sectional view of the memory cell region in FIG. 33A and the sectional view of the word-line contact region in FIG. 33F. EX1005, [0118]. This process simultaneously forms the semiconductor films 131 with dielectric films 132 in the memory cell region (collectively in green, FIG. 33A) and dummy semiconductor films 131 with dielectric films 132 (collectively in yellow, FIG. 33F) in the word-line contact region

using the same film-forming methods, such as chemical vapor deposition (CVD) followed by atomic layer deposition (ALD). EX1005, [0124]-[0125]. Consequently, the same materials, for example, polysilicon and silicon oxide, are arranged in the same lateral order in both structures.

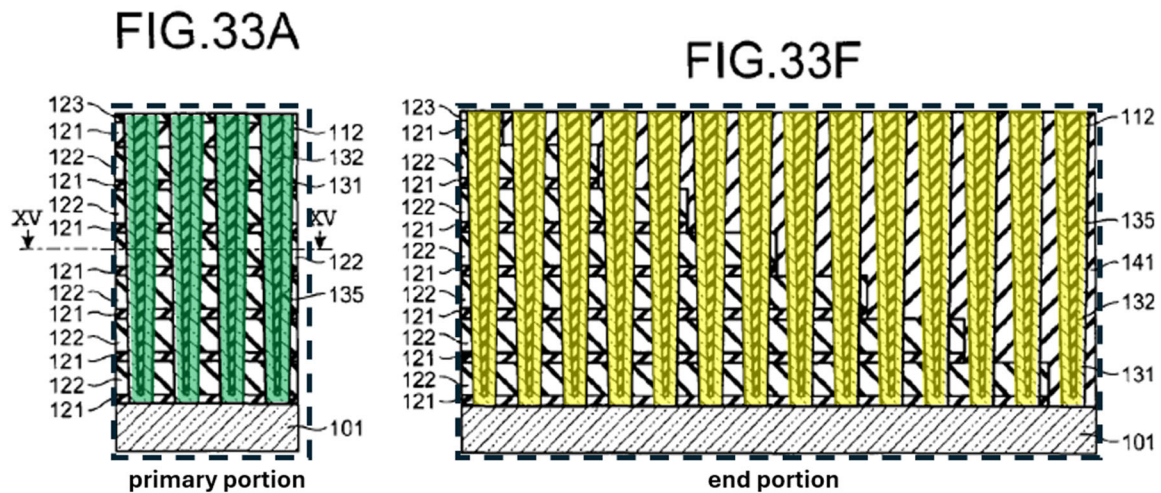


FIG. H – FIGs. 33A and 33F of Kiyotoshi (annotated)

88. Specifically, Kiyotoshi discloses the following:

Subsequently, as shown in FIGS. 33A to 33F, the semiconductor films 131 functioning as the channels are formed by a film forming method such as the LPCVD method. The semiconductor films 131 are deposited in the through-holes 135 and formed such that the lower ends thereof are connected to the semiconductor substrate 101. As the semiconductor films 131, for example, a B-doped polysilicon film can be used.

EX1005, [0124].

Further, the dielectric films 132 formed of a silicon oxide film or the like are formed to fill the inside of the hollow cylindrical semiconductor films 131 by the ALD method.

EX1005, [0125].

C. Jeong (EX1006)

89. Jeong is directed to 3D semiconductor devices. EX1006, [0003]. Like Chae, Kiyotoshi, as well as the '737 patent, Jeong identifies the same issue of dielectric layer collapsing during the gate replacement process and proposes the same solution to it by disclosing that “formation of the dummy pillars DP1 and DP2 through the insulating layers 110 in the second region R2 supports the insulating layers 110 during removal of the sacrificial layers 120, thereby minimizing or preventing the above problems, e.g., misalignment and/or breaking of the insulating layers 110.” EX1006, [0110], see also [0074], [0109].

90. FIGs. I and J, with my annotations below, illustrate the plan view of FIG. 1 and the cross-sectional view of FIG. 3 of Jeong, respectively. FIG. 3 refers to the same embodiment as FIG. 1 since FIG. 3 is taken along the lines I-I', II-II', III-III', and IV-IV' of FIG. 1. EX1006, [0052]. Jeong, in this embodiment, discloses a 3D semiconductor device having electrode structures ES, each including a stack of horizontally extending and vertically overlapping ground selection electrodes 130, cell electrodes 135, and string selection electrodes 138 (in red). EX1006, [0055]-[0056]. Jeong also discloses that the electrode structure ES includes a first region R1 (labeled as “primary portion”), which “may be a cell region, in which memory cells are three-dimensionally arranged,” and a second region R2 (labeled as “end portion”), which “may be a connection region,” in which “a stepped structure” of

electrodes 130, 135, and 138 is formed. EX1006, [0053], [0055].

FIG. 1

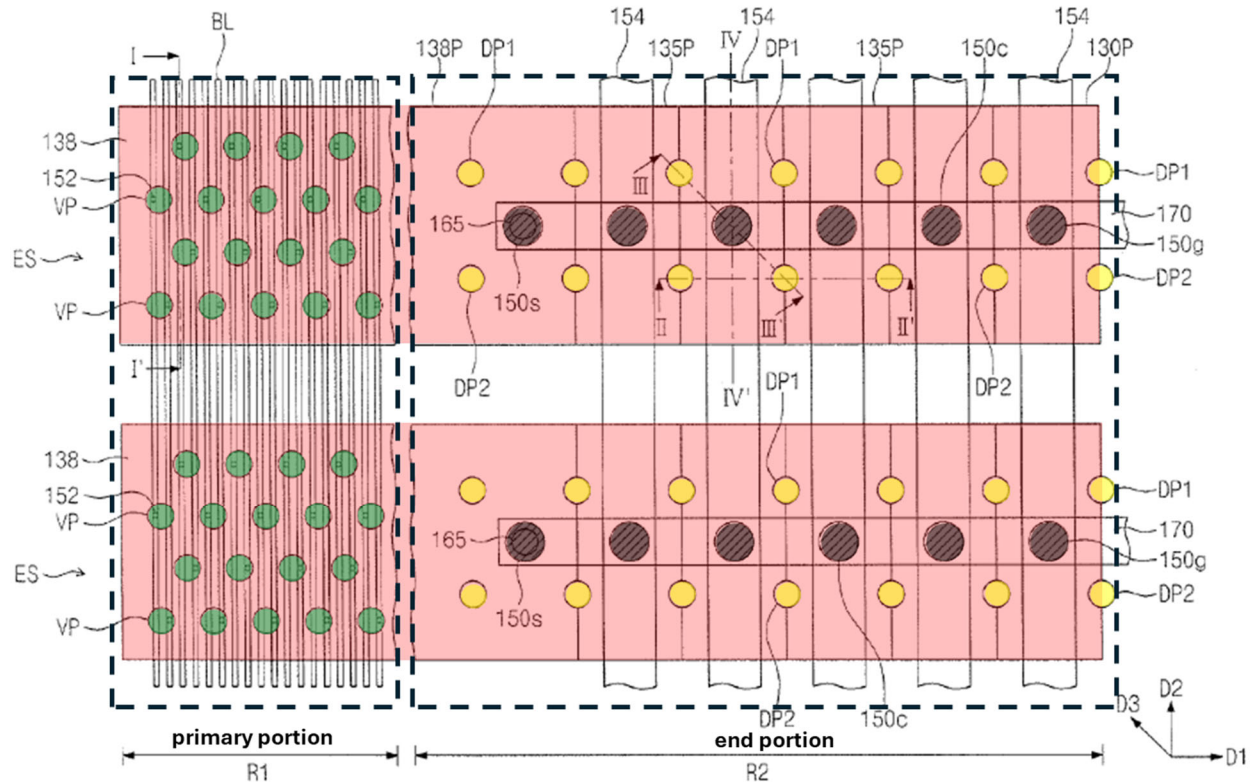


FIG. I – FIG. 1 of Jeong (annotated)

FIG. 3

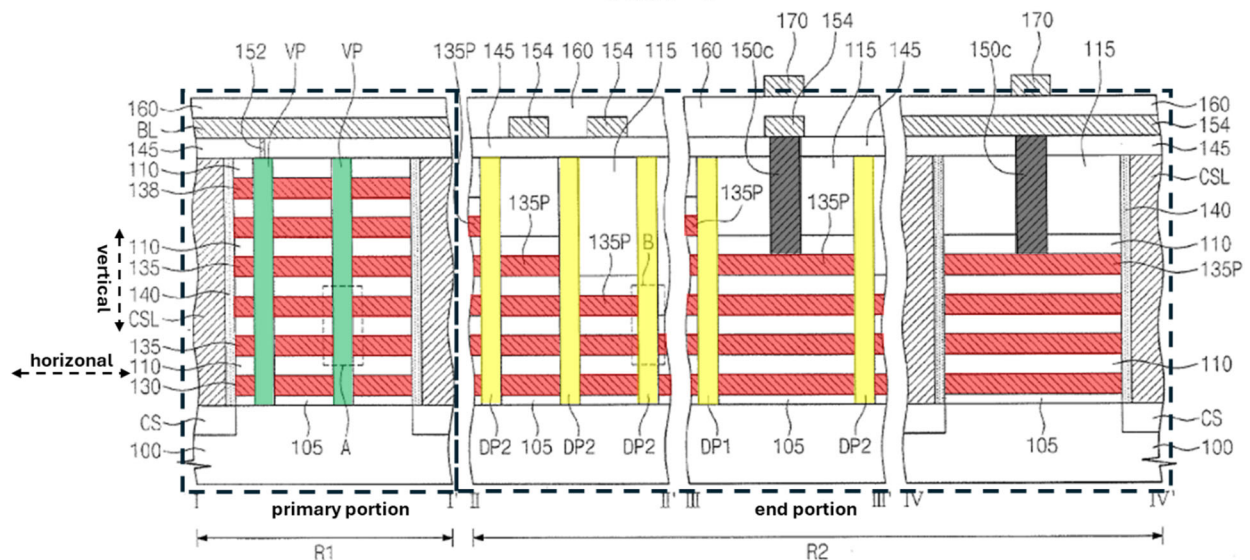


FIG. J – FIG. 3 of Jeong (annotated)

91. Jeong also discloses that the 3D semiconductor device includes vertical patterns VP (in green), each penetrating electrodes 130, 135, and 138 in first region R1, as well as dummy pillars DP1 and DP2 (in yellow), each penetrating electrodes 130, 135, and 138 in second region R2. EX1006, [0058], [0060]. Jeong further discloses contact plugs 150 (in black) connecting with electrodes 130, 135, and 138, respectively, in second region R2. EX1006, [0066].

92. Specifically, for dummy pillars DP1 and DP2, Jeong discloses that they are formed in the same process with the same structure and material as vertical patterns VP:

The dummy pillar DP2 may include the same material as the vertical pattern VP. According to the present embodiment, like the vertical pattern VP, the dummy pillar DP2 may include the blocking insulating layer BIL, the charge storage layer CL, the tunnel insulating layer TL, the vertical semiconductor pattern SP, and the vertical insulating pattern VI. The first dummy pillar DP1 may have the same structure as the second dummy pillar DP2. EX1006, [0080].

The vertical patterns VP may be formed in the vertical holes H1, respectively, and the dummy pillars DP1 and DP2 may be formed in the dummy holes H2, respectively. The vertical patterns VP and the dummy pillars DP1 and DP2 may be formed at the same time. EX1006, [0105].

93. Jeong also discloses that dummy pillars DP1 and DP2 are used to prevent dielectric layers from collapsing during the gate replacement process in second region R2, just like what vertical patterns VP do in first region R1:

In addition, the minimum of the dummy pillars DP1 and DP2 may support a mold stack structure used during a replacement process of forming the electrode structure ES, and thus, shape variation of the pads 130P, 135P, and 138P may be minimized using the minimum of the dummy pillars DP1 and DP2. As a result, it is possible to minimize or prevent deterioration of the electrode structure ES.
EX1006, [0074].

When the sacrificial layers 120 are removed, the dummy pillars DP1 and DP2 support the insulating layers 110 and the capping layer 115 in the second region R2, and the vertical patterns VP may support the insulating layers 110 in the first region R1. Thus, it is possible to minimize or prevent problems which may be caused by the removal of the sacrificial layers 120.
EX1006, [0109], see also [0110].

94. As shown in FIG. J above, dummy pillars DP1 and DP2 (in yellow) are electrically inoperable because dummy pillars DP1 and DP2 are covered by first insulating layer 145, as opposed to conductive contacts or interconnect layers, such as bit line contact plugs 152.

D. Hwang (EX1007)

95. Hwang is related to 3D semiconductor devices and manufacturing methods thereof. EX1007, [0002]. Similar to Chae, Kiyotoshi, Jeong, as well as the '737 patent, Hwang recognizes the same problem of dielectric layer collapsing during the gate replacement process and proposes the same solution to it—disclosing that “supporting members 175 may prevent and/or reduce collapse of the lower inter-layer insulating layers 120 and the lower insulating layers 160 in the subsequent process of removing the lower sacrificial layers 130.” EX1007, [0120], see also

[0118], [0122].

96. FIG. K below with annotations to FIG. 8 of Hwang relates to the modified first embodiment in connection with FIGs. 8 and 9. Because FIGs. 8 and 9, along with their accompanying disclosures, relate to a “modified example of the first embodiments of inventive concepts,” it is clear to me that the disclosures of the first embodiments with respect to FIGs. 1-7 are also applicable to the modified first embodiment of FIGs. 8 and 9. EX1007, [0031], [0117], [0118].

Fig. 8

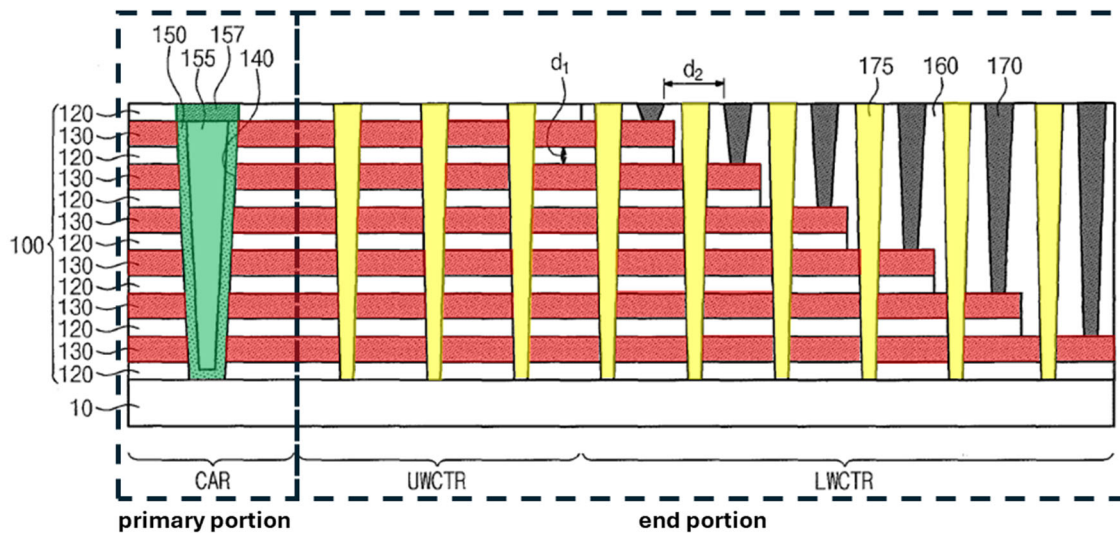


FIG.

K – FIG. 8 of Hwang (annotated)

97. As shown in FIG. K above, in Hwang’s modified first embodiment, a 3D semiconductor device having a lower thin film structure 100 includes a stack of horizontally extending and vertically overlapping lower sacrificial layers 130 (in red). EX1007, [0033], [0119]. Hwang explains that lower sacrificial layers 130 are

first removed to form lower recess regions 351 (see FIGs. 4A-4C) and eventually replaced with lower conductive patterns 430 (see FIGs. 6A-6C). EX1007, [0080], [0091], [0093]. Thus, Hwang discloses a stack of lower conductive patterns 430 horizontally extending and vertically overlapping, like lower sacrificial layers 130 shown in FIG. K.

98. FIG. K above also illustrates that lower thin film structure 100 includes a cell array region CAR (labeled as “primary portion”) where “[m]emory cells with a three-dimensional structure are formed,” and also a lower word line contact region LWCTR (labeled as “end portion”) “with a terraced shape.” EX1007, [0032], [0036].

99. The 3D semiconductor device shown in FIG. K also includes lower semiconductor patterns 150 with buried patterns 155 (collectively in green) penetrating lower sacrificial layers 130/lower conductive patterns 430 in cell array region CAR, as well as supporting members 175 (in yellow) penetrating lower sacrificial layers 130/lower conductive patterns 430 in lower word line contact region LWCTR. EX1007, [0044], [0050], [0109], [0119].

100. Specifically, for supporting members 175, Hwang discloses that they are formed together with lower semiconductor patterns 150 with the same semiconductor material:

The supporting members 175 may be formed together with the lower semiconductor patterns 150 so as to be formed of a semiconductor material.

EX1007, [0119].

101. Hwang also discloses that supporting members 175 are used to prevent dielectric layers from collapsing during the gate replacement process in lower word line contact region LWCTR, similar to what lower semiconductor patterns 150 do in cell array region CAR:

Referring to FIG. 8, supporting members 175 may be formed in the lower word line contact region LWCTR to support the lower thin film structure 100, before or after the lower sacrificial contact patterns 170 are formed in first embodiments of inventive concepts.
EX1007, [0118].

The supporting members 175 may be formed between the lower sacrificial contact patterns 170 to penetrate the lower thin film structure 100. The supporting members 175 may prevent and/or reduce collapse of the lower inter-layer insulating layers 120 and the lower insulating layers 160 in the subsequent process of removing the lower sacrificial layers 130.
EX1007, [0120].

That is, when the recess regions 351 to 353 are formed, the supporting members 175 may penetrate the recess regions 351. The supporting members 175 may maintain distance between the lower inter-layer insulating layers 120. That is, the supporting members 175 may prevent and/or reduce collapse of the lower thin film structure 100, the upper thin film structure 200, the lower insulating layer 160, and the upper insulating layer 26.
EX1007, [0122].

102. As shown in FIG. 9 of Hwang, supporting members 175 are electrically inoperable because supporting members 175 are covered by upper insulating layer 260, instead of conductive wirings, such as global word lines or bit lines.

103. FIG. K above also illustrates lower sacrificial contact patterns 170 (in black) in lower word line contact region LWCTR, each connecting with a respective one of lower sacrificial layers 130 (in red). EX1007, [0120]-[0121]. Hwang explains that lower sacrificial contact patterns 170 are first removed to form contact recess regions 353 (see FIGs. 4A and 4C), and finally replaced with buried contact plugs 450 (see FIGs. 6A and 6C). EX1007, [0080], [0091], [0093]. Specifically, Hwang discloses that “buried contact plugs 450 are locally formed in the contact recess region 353 to be connected to the lower conductive patterns 430, respectively.” EX1007, [0093]. Thus, each of buried contact plugs 450 in lower word line contact region LWCTR, is connected with a respective one of lower conductive patterns 430, just like lower sacrificial contact patterns 170 and lower sacrificial layers 130 shown in FIG. K.

104. Regarding buried contact plugs 450, Hwang further discloses that buried contact plugs 450 have a “horizontal cross-section of a substantially rectangular shape.” EX1007, [0114], FIG. 7, see also [0093].

IX. Grounds 1 and 2: Chae Anticipates or Otherwise Renders Obvious Claims 1-12, 14, 15, 21, and 22

A. Independent Claim 1

105. Claim 1 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[1.P] Integrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines:

[1.a.1] a primary portion and an end portion, **[1.a.2]** at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

[1.b.1] operative structures extending vertically through the gate lines in the primary portion, **[1.b.2]** the operative structures comprising semiconductive material, **[1.b.3]** the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines; and;

[1.c] dummy structures extending vertically through the gate lines in the end portion.

[1.P] Integrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines

106. Chae discloses “[i]ntegrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines.”

107. Chae discloses that a nonvolatile memory device (i.e., “[i]ntegrated circuitry”) includes a stack of conductive line-shaped gate electrodes 250. EX1004, [0122], [0130]. As shown in FIG. L with my annotations below, the stack of gate electrodes 250 (in red) extend horizontally and overlap vertically. According to Chae, gate electrodes 250 function as select lines USL and LSL and word lines WL, which control the operations of select transistors UST and LST and memory cell

transistors MC connected thereto, respectively. EX1004, [0043]-[0044], [0078], FIG.

1. Therefore, gate electrodes 250 qualify as the claimed “transistor gate lines.”

Fig. 15E

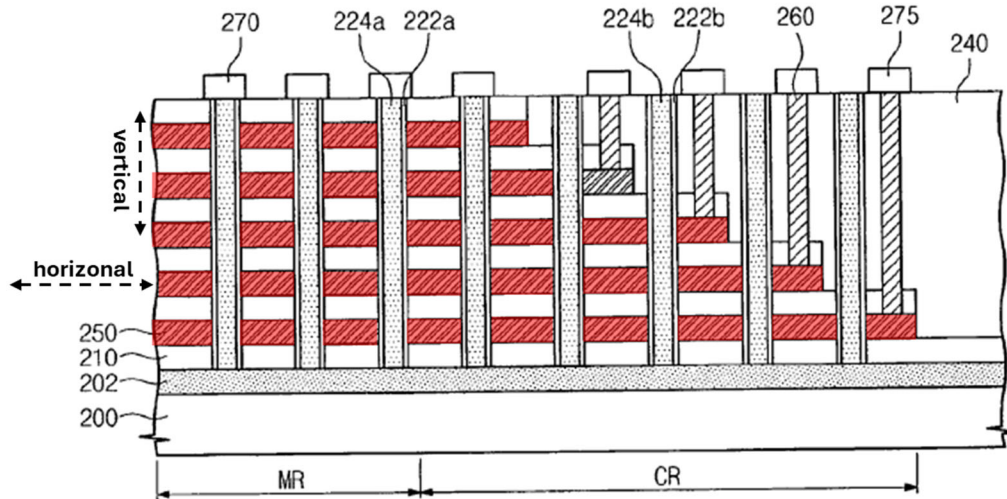


FIG. L – FIG. 15E of Chae (annotated)

[1.a.1] a primary portion and an end portion

108. Chae discloses “a primary portion and an end portion.”

109. FIGs. M and L below, with my annotations, show the plan view of FIG. 10 and the cross-sectional view of FIG. 15E, respectively, which is along the line II-II’ of FIG. 10. EX1004, [0122]. As shown in FIGs. M and N, the nonvolatile memory device includes a memory cell region MR (labeled as “primary portion”) and a contact region CR (labeled as “end portion”). EX1004, [0078].

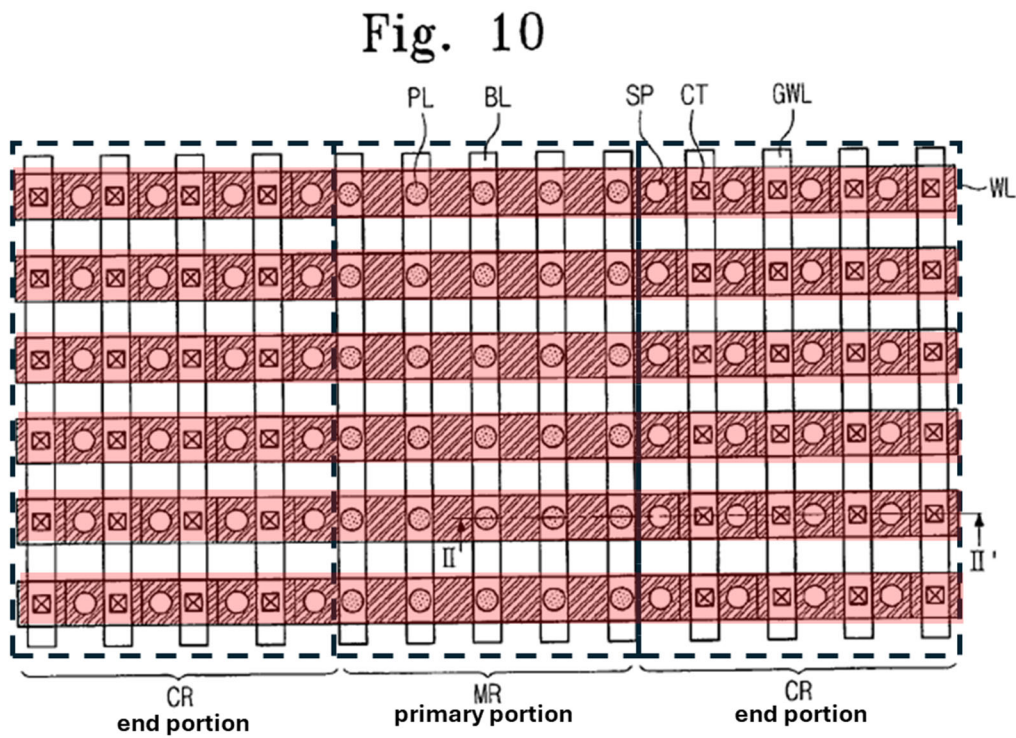


FIG. M – FIG. 10 of Chae (annotated)

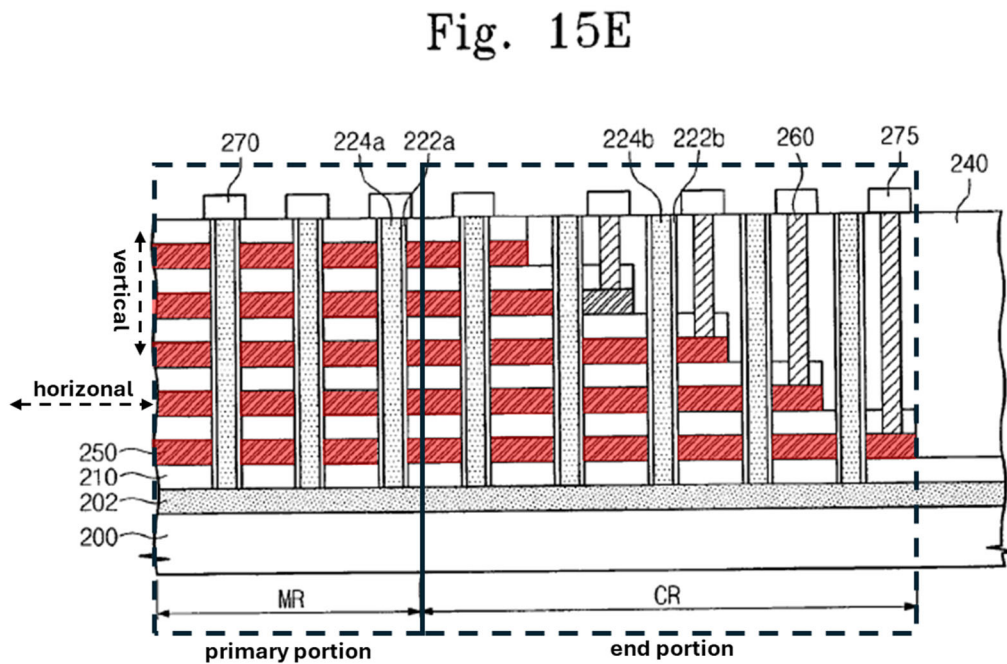


FIG. L – FIG. 15E of Chae (annotated)

110. Because memory cell region MR refers to the region where the memory

cells are formed, which is the primary portion of a memory device, memory cell region MR is the claimed “primary portion.” Because contact region CR is at the end/edge of the stack, as shown in FIGs. M and N above, it is the claimed “end portion.” EX1004, [0078], [0162].

[1.a.2] at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion

111. Chae discloses “at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion,” which merely recites the well-known stair-like structure in a 3D NAND memory device, as discussed above in Section VI. See, e.g., EX1020, FIG. 6.

112. Chae also discloses this well-known structure—“gate electrodes 250 of the contact region CR are formed in **a stair shape**.” EX1004, [0132], see also [0124], [0130]. For instance, FIG. L below clearly shows that, in contact region CR, gate electrode 250 (in red) at a lower level in the vertical direction of the stack, i.e., moving deeper into the stack, extends farther in the horizontal direction.

Fig. 15E

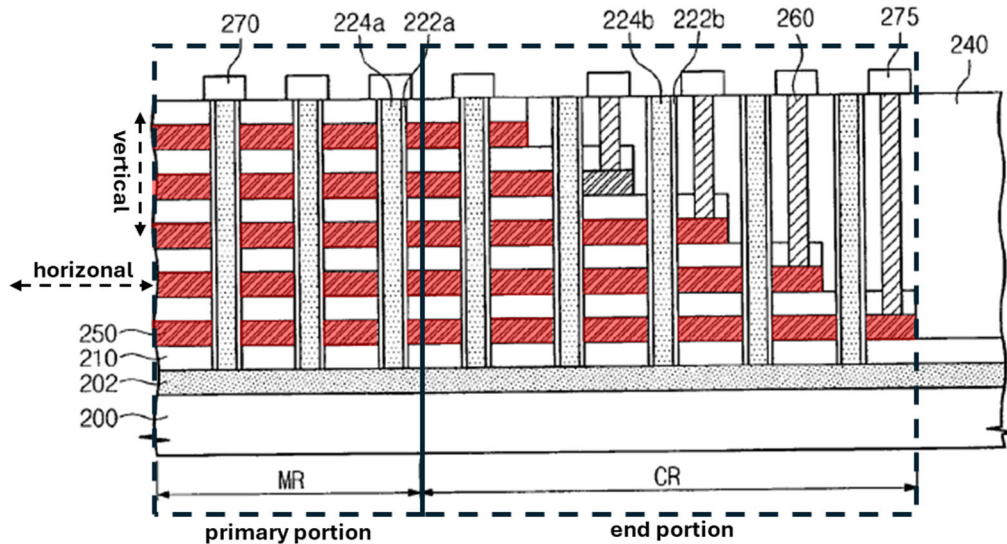


FIG. L – FIG. 15E of Chae (annotated)

[1.b.1] operative structures extending vertically through the gate lines in the primary portion

113. Chae further discloses “operative structures extending vertically through the gate lines in the primary portion.”

114. As illustrated in FIG. N with my annotations below, FIG. 15E of Chae shows that in memory cell region MR (labeled as “primary portion”), active pillars 224a with charge storage layers 222a (collectively in green) each extends vertically through gate electrodes 250 (in red). EX1004, [0126], [0128].

Fig. 15E

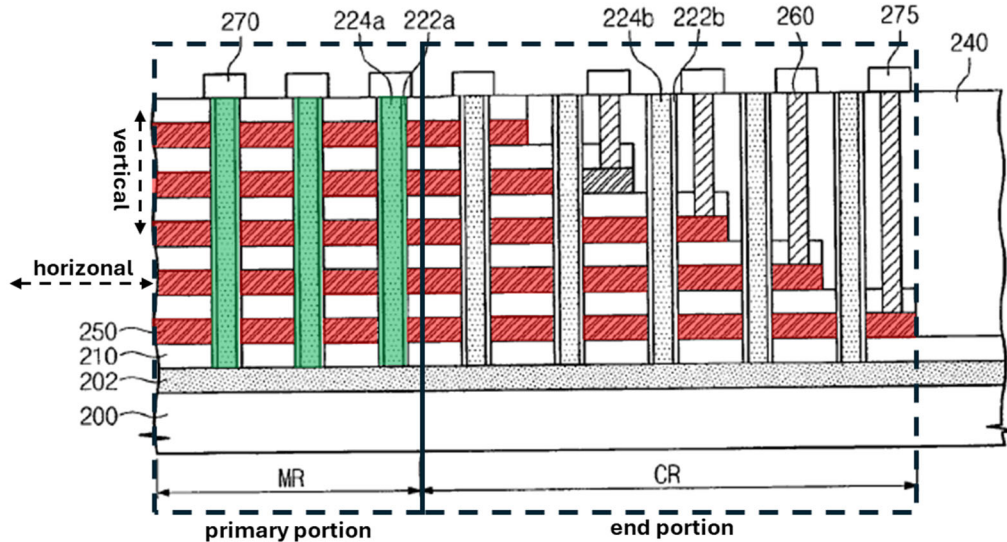


FIG. N – FIG. 15E of Chae (annotated)

115. Chae specifically explains the following with respect to active pillars

PL and charge storage layers CS:

The active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept. That is, the channels of memory cell transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.

EX1004, [0054].

Also, in the memory cell region MR, a charge storage layer CS is formed to surround each of the active pillars PL. That is, the charge storage layer CS is disposed between the active pillar PL and the gate electrodes LSL, WL and USL.

EX1004, [0055].

Although the quotations cited above are provided in the context of FIG. 1 related to the first embodiment, it is clear to me, based on Chae's explanations, that

descriptions of the “active pillars PL” and “charge storage layer CS” in paragraphs [0054] and [0055] equally apply to active pillars 224a and charge storage layer 222a in the “fifth exemplary embodiment of the inventive concept,” upon which my mappings of Chae are based. EX1004, [0121].

116. Furthermore, the '737 patent describes that the claimed “operative structures” may be “circuit components.” EX1001, 6:22-25. As shown in FIG. D below, active pillar PL 224a, along with charge storage layer 222a, are parts of a string STR (in purple), including select transistors UST and LST (in brown) and memory cells MC (in blue), which are also “circuit components” of the nonvolatile memory device. Thus, active pillars PL 224a with charge storage layers 222a qualify as the claimed “operative structures.”

Fig. 1

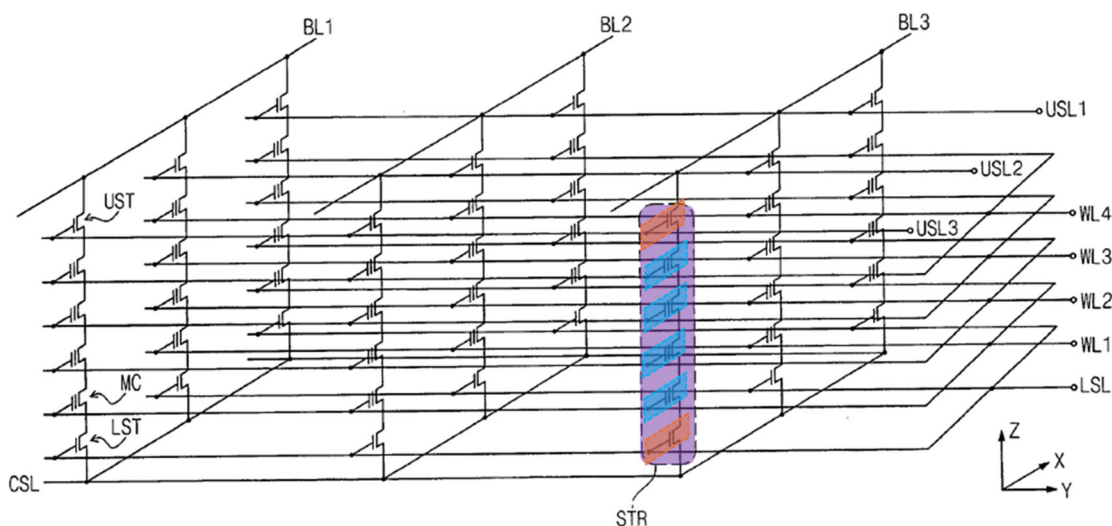


FIG. D – FIG. 1 of Chae (annotated)

[1.b.2] the operative structures comprising semiconductive material

117. Chae discloses “the operative structures comprising semiconductive material.” Specifically, Chae discloses “charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.” EX1004, [0128]. Chae further discloses “[t]he semiconductor material may be monocrystalline or polycrystalline semiconductor material.” EX1004, [0109]. Thus, Chae discloses that active pillars 224a include “semiconductor material.”

[1.b.3] the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines

118. Chae discloses or otherwise renders obvious “the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines.”

119. Specifically, Chae discloses that “[e]ach string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST,” “the strings STR are configured in such a way that the memory cells MC are

connected in series in a Z-axis direction perpendicular to an XY plane parallel to the top surface of a semiconductor substrate,” “the channel of the memory cell transistors MC and the select transistors UST and LST may be formed perpendicular to the XY plane,” “active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept,” and that “channels of memory cell transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.” EX1004, [0043], [0045], [0054].

120. In view of these disclosures of Chae and as further shown in FIG. D below, a POSITA would have understood, or at least found it obvious, that memory cell transistors MC (in blue) are vertically oriented transistors connected in a string STR (in purple), each memory cell transistor MC includes a channel, and that the channels of memory cell transistors MC in a string STR are vertically interconnected and provided in a respective active pillar PL 224a.

Fig. 1

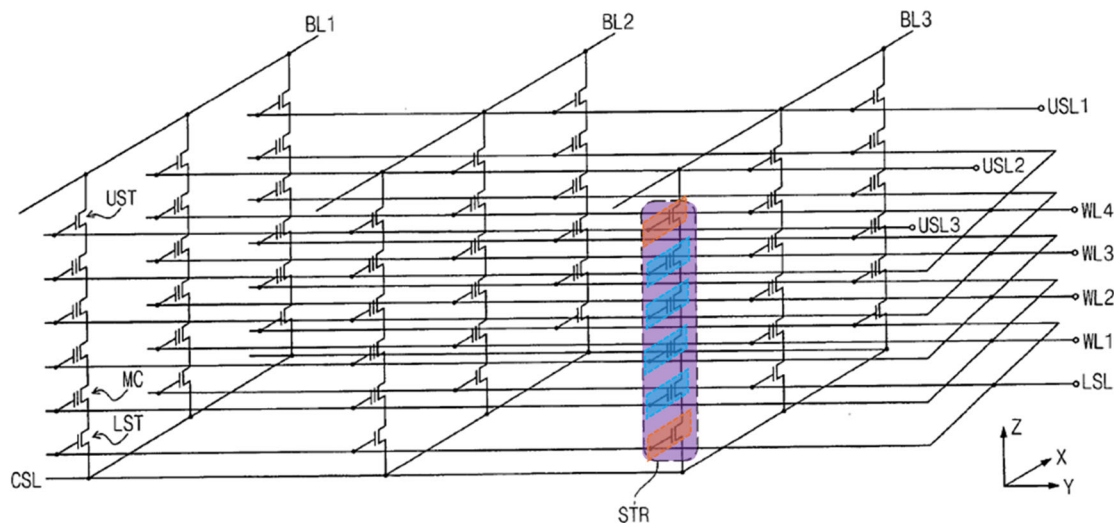


FIG. D – FIG. 1 of Chae (annotated)

121. Chae further discloses that “memory cells MC are connected respectively to the word lines WL1~WL4” and that “the charge storage layer CS is disposed between the active pillar PL and the gate electrodes LSL, WL and USL.” EX1004, [0044], [0055]. Based on these disclosures and as further illustrated in FIG. D above, a POSITA would have understood, or at least found it obvious, that each memory cell transistor MC also includes a respective gate electrode 250, e.g., a word line WL.

[1.c] dummy structures extending vertically through the gate lines in the end portion

122. Chae further discloses “dummy structures extending vertically through the gate lines in the end portion.”

123. As shown in FIG. O with my annotations below, FIG. 15E of Chae illustrates that in contact region CR (labeled as “end portion”), supporters 224b with charge storage layers 222b (collectively in yellow) each extends vertically through gate electrodes 250 (in red). EX1004, [0126], [0128].

Fig. 15E

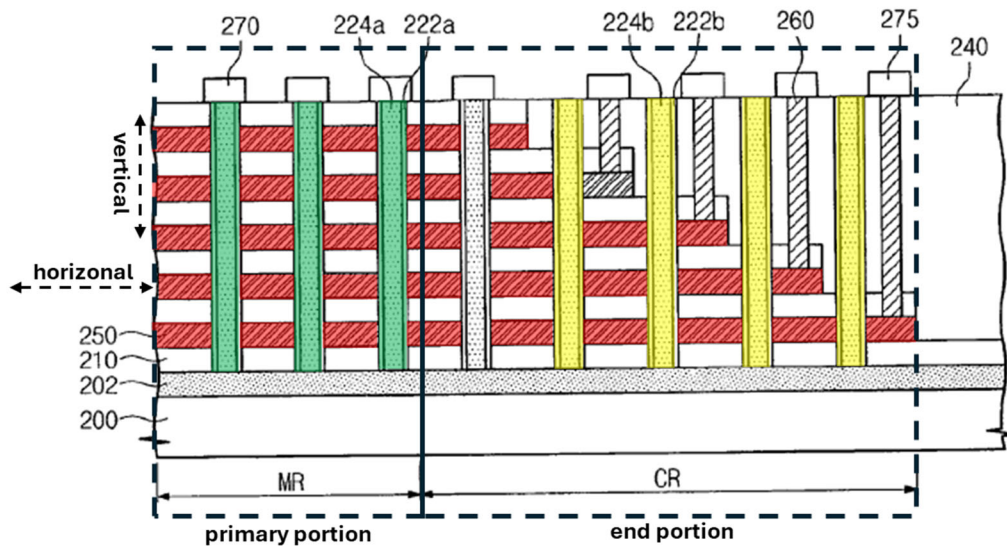


FIG. O – FIG. 15E of Chae (annotated)

124. Specifically, Chae discloses that “first dielectric layers 210 spaced apart from each other may be supported by the active pillars 224a of the memory cell region MR, which are perpendicular to the semiconductor substrate 200, and the supporters 224b of the contact region CR,” and that “second dielectric layers 215 can be prevented from collapsing or getting near to each other during the removing of the second dielectric layers 215 through a wet etch process.” EX1004, [0129]. As discussed above in detail in Section VIII.A, Chae also discloses that supporters 224b

with charge storage layers 222b, and active pillars 224a with charge storage layers 222a, are formed of the same materials in the same process with the same structure. See Section VIII.A. Based on these disclosures, a POSITA would have understood that supporters 224b with charge storage layers 222b mimic a physical property of active pillars 224a with charge storage layers 222a.

125. As I also discussed above in Section VIII.A, Chae further discloses that “[b]ecause a conductive pattern such as the global word line 275 or the bit line 270 is not formed on the supporters 224b, it does not affect the operation of the nonvolatile memory device according to the exemplary embodiment of the inventive concept.” EX1004, [0134]; see Section VIII.A. Thus, a POSITA would have understood that supporter 224b with charge storage layer 222b is an electrically inoperable structure.

126. Therefore, supporters 224b with charge storage layers 222b are the claimed “dummy structures” under the construction of “electrically inoperable structure that mimics a physical property of an operative structure.” See Section VII.D.

B. Dependent Claim 2: The stack of claim 1 further comprising contacts in the end portion that individual extend to the individual gate lines.

127. Chae further discloses “contacts in the end portion that individual extend to the individual gate lines.”

128. As illustrated in FIG. P with my annotations below, FIG. 15E of Chae also illustrates that in contact region CR (labeled as “end portion”), contact plugs 260 (in black) each extends to and connects with a respective gate electrode 250 (in red). EX1004, [0131].

Fig. 15E

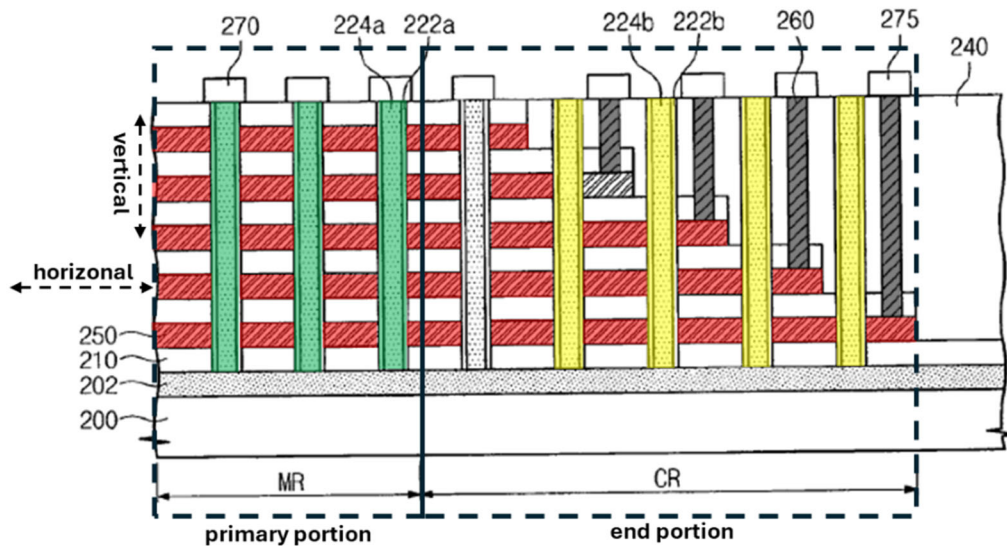


FIG. P – FIG. 15E of Chae (annotated)

C. Dependent Claim 3: The integrated circuitry of claim 1 wherein the vertically oriented transistors are charge storage transistors of individual memory cells.

129. Chae discloses or otherwise renders obvious “the vertically oriented transistors are charge storage transistors of individual memory cells.” Specifically, Chae discloses, or at least suggests, that memory cell transistors MC include charge storage layers CS 222a. EX1004, [0054]-[0055], [0128].

130. It is well known in the art that charge storage layer 222a surrounding active pillars PL 224a includes materials, such as silicon nitride in charge trapping memory, or polysilicon in floating gate memory. EX1021, Table 1; EX1022, 2847, § I. Charge stored in charge storage layer 222a changes the threshold voltage required at the corresponding gate electrode 250 to enable current flow through surrounded semiconductor material of active pillars PL 224a, such that these varying threshold voltages of the memory cell transistors MC can be measured to determine the storage of information. EX1023, 189. Thus, a POSITA would readily appreciate that a memory cell transistor MC having charge storage layer 222a qualifies as the claimed “charge storage transistors of individual memory cells.”

D. Dependent Claim 4: The integrated circuitry of claim 3 wherein the memory cells comprise a portion of NAND architecture.

131. Chae discloses “the memory cells comprise a portion of NAND architecture.”

132. I noted that the '737 patent, in its Background section, states that “NAND is a basic architecture of flash memory. A NAND architecture comprises at least one select gate coupled in series to a serial combination of memory cells (with the serial combination being commonly referred to as a NAND string).” EX1001, 3:1-5. NAND architecture is indeed well known in the memory industry as a basic architecture of flash memory before the '737 patent.

133. Nevertheless, Chae discloses that “the NAND-type nonvolatile memory device is advantageous for high integration because it includes a cell string structure having a plurality of memory cell transistors connected in series.” EX1004, [0005]. Chae also discloses that “[e]ach string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST.” EX1004, [0043].

134. FIG. D below depicts that memory cell transistors MC (in blue) connected in series in a string STR (in purple) are parts of the NAND architecture in the nonvolatile memory device, which is consistent with the NAND architecture described in the '737 patent, as well as known in the art. EX1001, 3:1-5.

Fig. 1

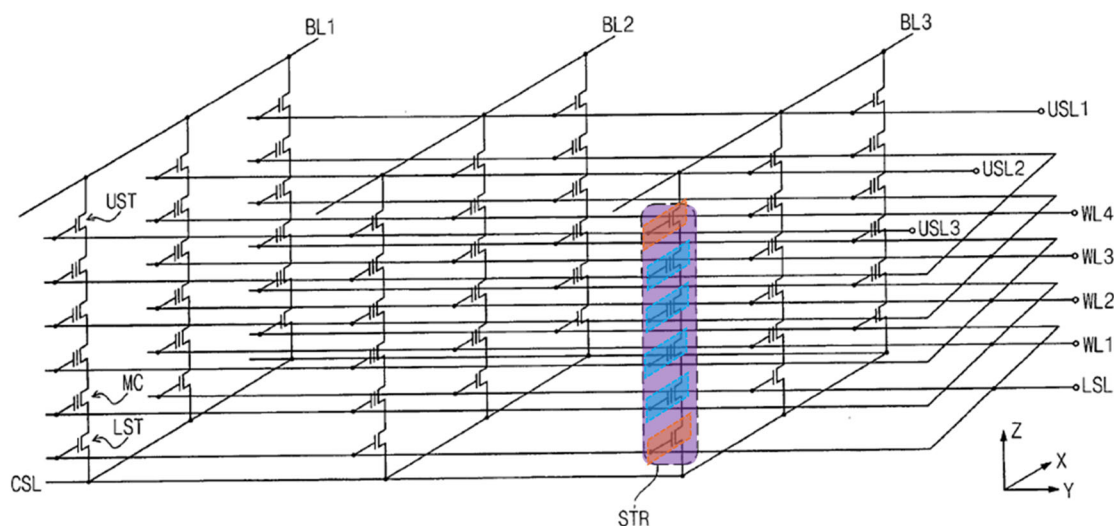


FIG. D – FIG. 1 of Chae (annotated)

E. Dependent Claim 5: The integrated circuitry of claim 1 wherein the operative and dummy structures comprise the same material. Dependent Claim 6: The integrated circuitry of claim 5 wherein the operative and dummy structures comprise a plurality of the same materials.

135. Chae discloses or otherwise renders obvious “the operative and dummy structures comprise the same material” and “the operative and dummy structures comprise a plurality of the same materials.”

136. Specifically, Chae discloses “the supporters SP may have the same structure as the active pillars PL. That is, the supporters SP of the contact region CR may also be formed of semiconductor material, and the charge storage layer CS surrounding the supporters SP may be formed between the supporters SP and the gate electrodes LSL, WL and US.” EX1004, [0081]. Chae also discloses that “charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are **filled with semiconductor material** to form active pillars 224a and supporters 224b.” EX1004, [0128]. Chae explicitly explains that “[t]hroughout the specification, like reference numerals refer to like elements.” EX1004, [0037].

137. Accordingly, a POSITA would have understood that active pillars 224a and supporters 224b are both made of the semiconductor material. Similarly, a POSITA would also have understood that charge storage layers 222a and charge storage layers 222b are both made of a charge storage material, such as silicon nitride

or polysilicon. EX1021, Table 1; EX1022, 2847, § I. Collectively, both active pillars 224a with charge storage layers 222a and supporters 224b with charge storage layers 222b have a semiconductor material and a charge storage material.

138. To the extent that Chae's above-quoted disclosures do not expressly state that the semiconductor materials forming active pillars 224a and supporters 224b are the same, and/or that the charge storage materials forming charge storage layers 222a and 222b are the same, a POSITA would have found these obvious. Because the same processes are used, the respective structures are obvious to be formed of the same materials. Specifically, a POSITA would have found it obvious to use the same materials to fill both the dummy holes and channel holes to form active pillars 224a with charge storage layers 222a and supporters 224b with charge storage layers 222b, respectively.

139. This is because implementing this approach would simplify the fabrication process and advantageously reduce the number of processing steps. Minimizing the number of steps in semiconductor manufacturing is highly beneficial, as it directly decreases the risk of defects, shortens overall manufacturing time, and improves fabrication yield. EX1014, 54; EX1015, [0004], [0108], [0190]. For example, in the context of deposition processes used in semiconductor manufacturing, it was well-recognized that each additional processing step introduced potential sources of defects, including particle contamination, variations

in film thickness, and interface inconsistencies. These defects could negatively impact device performance, reliability, and yield. By streamlining the process and reducing unnecessary steps, manufacturers could enhance process control, improve uniformity, and maintain higher production efficiency.

140. Moreover, filling both the dummy holes and channel holes using the same materials is a common practice in semiconductor manufacturing, which can be achieved, for example, by using various well-established deposition processes, such as CVD and/or ALD, such as detailed in Kiyotoshi. EX1005, [0124]-[0125]. Therefore, such a process would predictably work and yield the expected resulting structures—both active pillars 224a with charge storage layers 222a and supporters 224b with charge storage layers 222b have the same semiconductor material and the same charge storage material.

F. Dependent Claim 7: The integrated circuitry of claim 6 wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

141. Chae discloses or otherwise renders obvious “the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.”

142. As illustrated in FIG. P below, in both active pillars 224a with charge storage layers 222a (collectively in green) and supporters 224b with charge storage layers 222b (collectively in yellow), the same charge storage material (e.g., silicon

nitride or polysilicon), which form charge storage layers 222a and 222b, is formed on the side, and the same semiconductor material (e.g., silicon), which form active pillars 224a and supporters 224b, is formed in the center. That is, Chae discloses that the same charge storage material and the same semiconductor material are arranged in the same centripetal direction inward towards the centers of active pillars 224a and supports 224b.

Fig. 15E

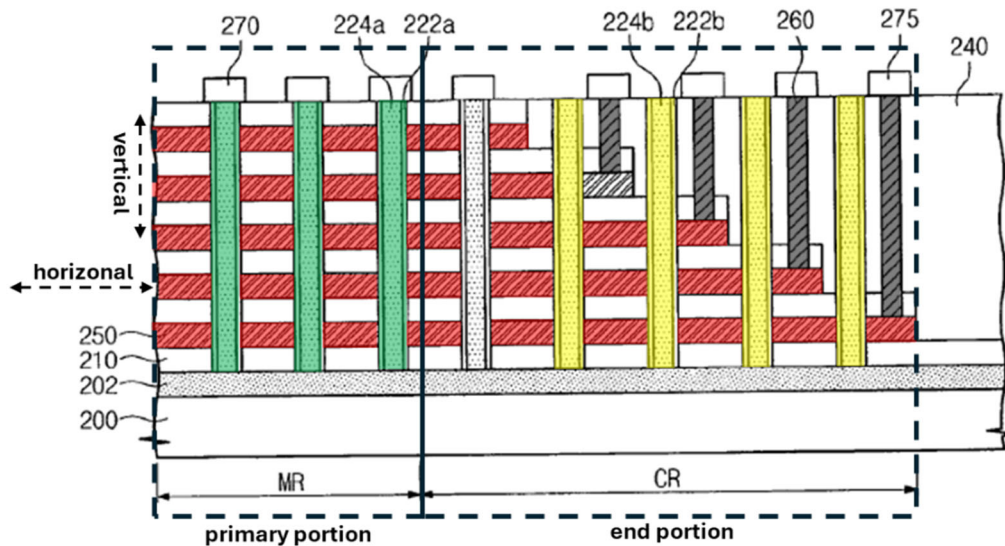


FIG. P – FIG. 15E of Chae (annotated)

143. This is further supported by Chae’s express disclosure in paragraph [0128] that “charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.” EX1004, [0128].

G. Dependent Claim 8: The integrated circuitry of claim 5 wherein the operative and dummy structures consist essentially of the same material.

144. Chae discloses or otherwise renders obvious “the operative and dummy structures consist essentially of the same material,” which merely replaces the term “comprises” in claim 5 with “consist essentially of.”

145. Since the specification of the ’737 patent reiterates the same language of claim 8 without providing further explanation—such as what qualifies as “essentially” or how it differs from the requirement in claim 5—I assume that claims 5 and 8 effectively have the same scope. Accordingly, I reached the same conclusion as claim 8 for the reasons for claim 5.

H. Dependent Claim 9: The integrated circuitry of claim 1 wherein the dummy structures comprise semiconductor material.

146. Chae discloses “the dummy structures comprise semiconductor material.” Specifically, Chae discloses “the supporters SP of the contact region CR may also be formed of semiconductor material” and “the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b” EX1004, [0081], [0128]. See also Section IX.E.

I. Dependent Claim 10: The integrated circuitry of claim 1 wherein the dummy structures comprise the semiconductive material.

147. Chae discloses “the dummy structures comprise the semiconductive material.” As I discussed in Sections IX.A([1.b.2]) and IX.E, active pillars 224a and

supporters 224b are made of the same semiconductor material. Thus, supporters 224b include the same semiconductive material as active pillars 224a. See Sections IX.A, IX.E.

J. Independent Claim 11

148. Claim 11 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[11.P] A stack of horizontally extending and vertically overlapping features, the stack comprising:

[11.a] a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

[11.b] operative structures extending vertically through the features in the primary portion;

[11.c.1] dummy structures extending vertically through the features in the end portion, **[11.c.2]** the dummy structures individually comprising a cylinder of semiconductive material.

[11.P] A stack of horizontally extending and vertically overlapping features, the stack comprising

149. Chae discloses a “stack of horizontally extending and vertically overlapping features.”

150. As I discussed in Section IX.A([1.P]), Chae discloses a stack of horizontally extending and vertically overlapping conductive line-shaped gate

electrodes 250. See Section IX.A.

151. Element [11.P] requires “features” instead of “conductive transistor gate lines” in element [1.P]. Regarding the term “features,” the ’737 patent explains the following:

In one embodiment, the features may be horizontally extending lines, for example formed of any one or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s). In one embodiment, the features comprise a combination of horizontally extending conductive and dielectric lines (e.g., overlapping and alternating such lines).
EX1001, 11:28-34.

That is, the claimed “features” may be horizontally extending lines, such as horizontally extending conductive lines. I also noted that claim 15, which depends on claim 11, further requires that “vertical contacts in the end portion connecting with **conductive material** of individual of the features.” Thus, it is clear to me that conductive line-shaped gate electrodes 250 of Chae qualify as the claimed “features,” consistent with the ’737 patent.

152. Even if the term “features” is narrowly interpreted to require a combination of horizontally extending conductive lines and dielectric lines—which I disagree with—each pair of gate electrode 250 and first dielectric layer 210 in Chae would still collectively qualify as one of the “features.” Moreover, this alternative interpretation and mapping would not affect my analysis of Chae with respect to any claim limitations related to the “features” in my Declaration.

[11.a] a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion

153. I incorporate the discussion provided above with respect to elements [1.a.1] and [1.a.2] in Grounds 1 and 2. Chae discloses element [11.a].

[11.b] operative structures extending vertically through the features in the primary portion

154. I incorporate the discussion provided above with respect to element [1.b.1] in Grounds 1 and 2. Chae discloses element [11.b].

[11.c.1] dummy structures extending vertically through the features in the end portion

155. I incorporate the discussion provided above with respect to element [1.c] in Grounds 1 and 2. Chae discloses element [11.c.1].

[11.c.2] the dummy structures individually comprising a cylinder of semiconductive material

156. Chae discloses or otherwise renders obvious “the dummy structures individually comprising a cylinder of semiconductive material.”

157. As I discussed in Sections IX.E, IX.H, and IX.I, Chae discloses that supporters SP 224b with charge storage layers 222b individually include a semiconductor material. See Sections IX.E, IX.H-IX.I.

158. Chae discloses various shapes of supporters SP both in the specifications and in the accompanying drawings. For instance, Chae expressly

discloses “the shape of a cylindrical pillar,” which matches the shape of supporters SP shown in FIG. 2A, as well as “circular pillars,” which match the shape of supporters SP shown in FIG. 6. EX1004, [0058], [0071], FIGs. 2A, 6. Conversely, Chae explicitly discloses “line-shaped supporters SP’,” which matches the shape of supporters SP’ shown in FIG. 2B, as well as “line patterns that are connected to each other and extend in different directions on the plane,” which match the shape of supporters SP’ shown in FIG. 2C. EX1004, [0059]-[0060], FIGs. 2B-2C. Accordingly, a POSITA would have understood that the plan view drawings of Chae (*e.g.*, FIGs. 2A, 2B, 2C, and 6) reflect the intended shapes of supporters SP.

159. Similarly, FIG. 10—a plan view of the fifth embodiment of Chae—depicts the shape of supporters SP in this embodiment, which also takes the shape of a cylindrical pillar, consistent with those shown in FIGs. 2A and 6. EX1004, [0058].

160. FIGs. Q and R below are annotated versions of FIGs. 10 and 15E of Chae, respectively. FIG. 15E is the sectional view along the line II-II’ of FIG. 10. EX1004, [0122]. In view of the discussion above, and as further shown in FIGs. Q and R, a POSITA would have understood, or at least found it obvious, that each supporter SP 224b with charge storage layer 222b (collectively in yellow) has a semiconductor material in the shape of a cylinder.

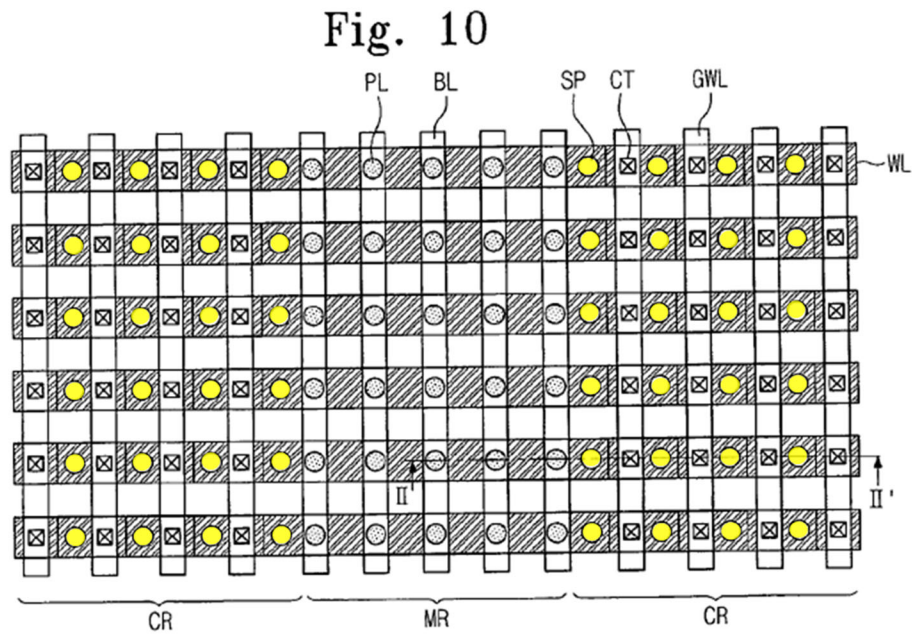


FIG. Q – FIG. 10 of Chae (annotated)

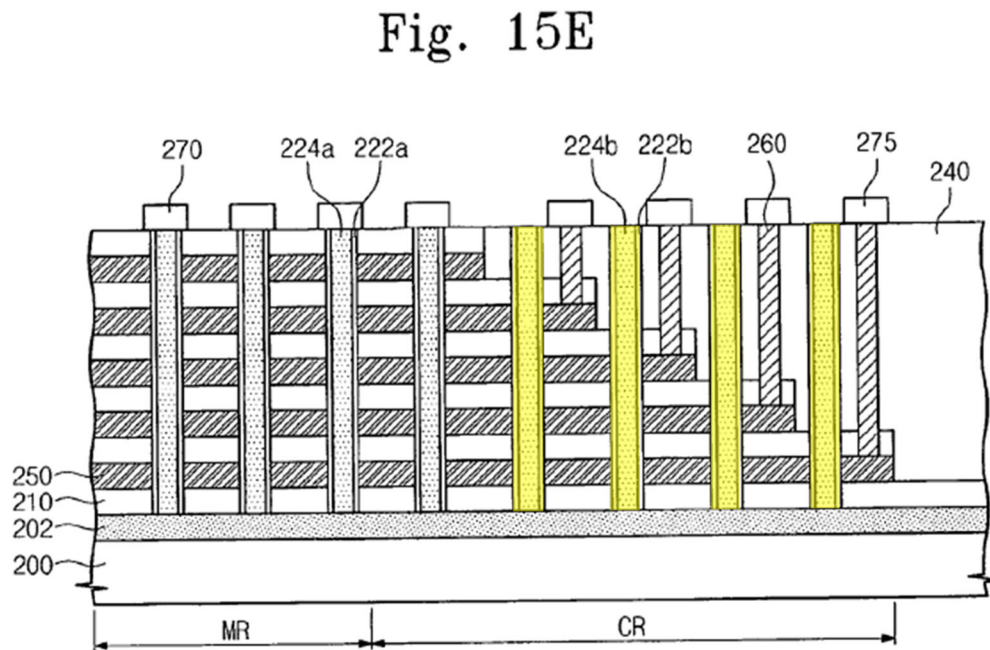


FIG. R – FIG. 15E of Chae (annotated)

K. Dependent Claim 12: The stack of claim 11 comprising solid material filling radially internal regions of individual of the cylinders of semiconductive material.

161. Chae discloses or otherwise renders obvious “solid material filling radially internal regions of individual of the cylinders of semiconductive material.”

162. I do not see any indication in the '737 patent or its file history that the phrase “solid material” shall depart from its plain and ordinary meaning, which is a material “without an internal cavity.” EX1013, 1a. In fact, the specification of the '737 patent does not mention the same phrase “solid material” at all. The closest description is about operative structures 31 and dummy structures 32 being “in the form of laterally solid pillars,” which is consistent with my understanding of the plain and ordinary meaning of the claimed “solid material.” EX1001, 6:55-57.

163. Chae discloses that “the dummy holes and the channel holes are **filled** with semiconductor material to form active pillars 224a and supporters 224b.” EX1004, [0128]. From this disclosure, in particular, the usage of the term “filled,” which means being occupied the whole of, it is clear to me that the radially internal region of each supporter 224b is fully occupied by the semiconductor material without an internal cavity.

164. Therefore, a POSITA would have understood, or at least found it obvious, that the semiconductor material disclosed by Chae is the claimed “solid material,” which occupies the whole of the radially internal region of each supporter

224b, which is in the shape of a cylinder. See also Sections IX.H, IX.J([11.c.2]).

L. Dependent Claim 14: The stack of claim 11 wherein the operative structures individually comprise a cylinder of semiconductor material.

165. Chae discloses or otherwise renders obvious “the operative structures individually comprise a cylinder of semiconductor material.”

166. As I discussed above in Section IX.E, Chae discloses that active pillar PL 224a includes a semiconductor material.

167. Similar to supporters SP, Chae discloses various shapes of active pillars PL both in the specifications and in the accompanying drawings. For example, Chae expressly discloses “a cylindrical shape,” which matches the shape of active pillars PL shown in FIGs. 2A, 2B, 2C, and 4 in the first and second embodiments. EX1004, [0070], FIGs. 2A-2C, 4. Conversely, Chae discloses active pillars PL’ in a line shape, as shown in FIG. 6 of the third embodiment. EX1004, [070], FIG. 6. Accordingly, a POSITA would have understood that the plan view drawings of Chae (*e.g.*, FIGs. 2A, 2B, 2C, 4, and 6) reflect the intended shapes of active pillars PL.

168. Similarly, FIG. 10—a plan view of the fifth embodiment of Chae—depicts the shape of active pillars PL in this embodiment, which also takes the shape of a cylindrical pillar, consistent with those shown in FIGs. 2A, 2B, 2C, and 4. EX1004, [0070].

169. FIGs. S and T below are annotated versions of FIGs. 10 and 15E of

Chae, respectively. FIG. 15E is the sectional view along the line II-II' of FIG. 10. EX1004, [0122]. In view of the discussion above, and as further shown in FIGs. S and T, a POSITA would have understood, or at least found it obvious, that each active pillar PL 224a with charge storage layer 222a (collectively in green) has a semiconductor material in the shape of a cylinder.

Fig. 10

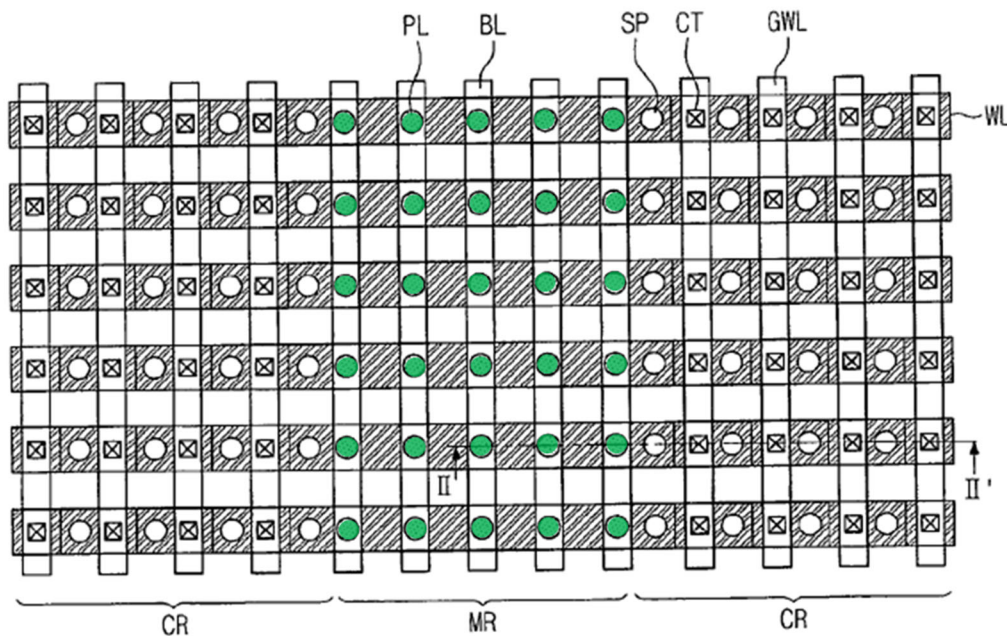


FIG. S – FIG. 10 of Chae (annotated)

Fig. 15E

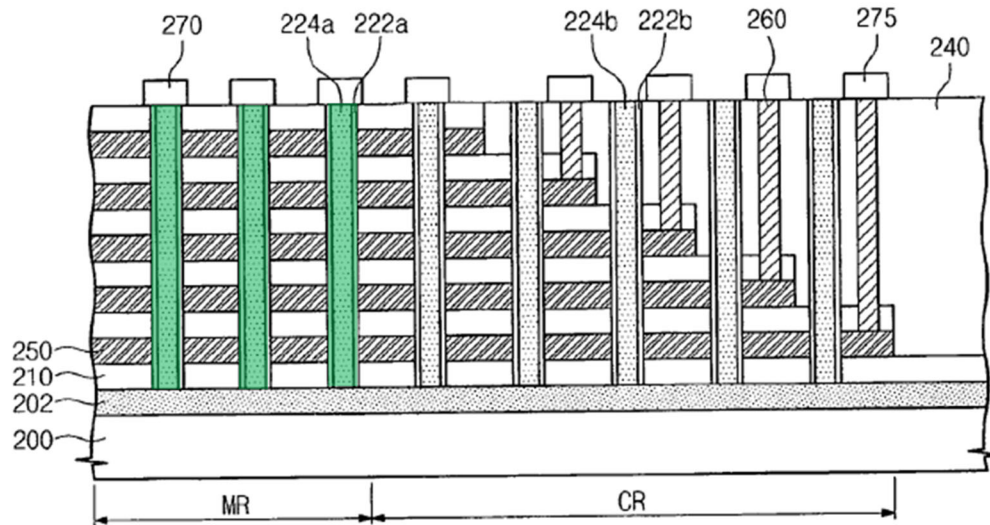


FIG. T – FIG. 15E of Chae (annotated)

M. Dependent Claim 15: The stack of claim 11 further comprising vertical contacts in the end portion connecting with conductive material of individual of the features.

170. Chae discloses “vertical contacts in the end portion connecting with conductive material of individual of the features.”

171. As I discussed above in Section IX.B, Chae discloses that “contact plugs 260, connected respectively to the gate electrodes 250 of each layer, are formed in the contact region CR of the gate electrodes 250.” EX1004, [0131].

172. FIG. P below illustrates that each contact plug 260 (in black) extends vertically to connect a respective global word line 275, which is “formed on the contact plugs 260,” and also to connect a respective gate electrode 250 (in red), which is underneath contact plugs 260. EX1004, [0119]-[0120]. Contact plugs 260

are arranged vertically and thus, qualify as the claimed “vertical contacts.”

Fig. 15E

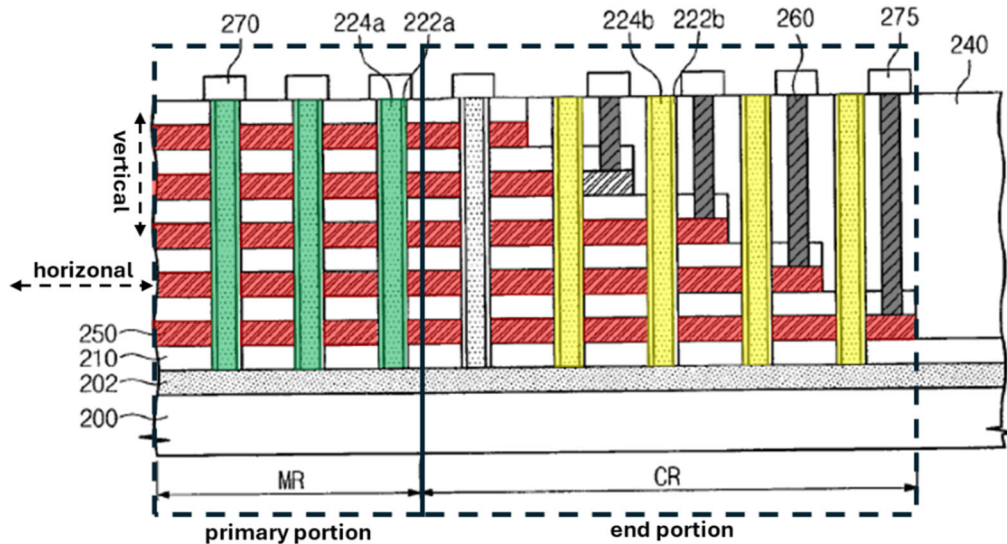


FIG. P – FIG. 15E of Chae (annotated)

173. Moreover, Chae discloses that each gate electrode 250 is formed of “a conductive material,” such as “polysilicon or metal material.” EX1004, [0130]-[0131]. Thus, contact plugs 260 connect with the conductive material of each gate electrode 250.

N. Independent Claim 21

174. Claim 21 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[21.P] A stack of horizontally extending and vertically overlapping features, the stack comprising:

[21.a] a primary portion and an end portion, at least some of the features

extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

[21.b.1] operative structures extending vertically through the features in the primary portion, [21.b.2] the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, [21.b.3] the at least some of the features comprising control gate lines;

[21.c.1] dummy structures extending vertically through the control gate lines in the end portion, [21.c.2] some of the dummy structures being longitudinally spaced along a horizontal line; and

[21.d.1] vertical contacts in the end portion connecting with individual of the control gate lines, [21.d.2] at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line.

[21.P] A stack of horizontally extending and vertically overlapping features, the stack comprising

175. I incorporate the discussion provided above with respect to element [11.P] in Grounds 1 and 2. Chae discloses element [21.P].

[21.a] a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion

176. I incorporate the discussion provided above with respect to element [11.a] in Grounds 1 and 2. Chae discloses element [21.a].

[21.b.1] operative structures extending vertically through the features in the primary portion

177. I incorporate the discussion provided above with respect to element [11.b] in Grounds 1 and 2. Chae discloses element [21.b.1].

[21.b.2] the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string

178. Chae discloses or otherwise renders obvious “the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string.”

179. Specifically, Chae discloses that “[e]ach string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST,” “the strings STR are configured in such a way that the memory cells MC are connected in series in a Z-axis direction perpendicular to an XY plane parallel to the top surface of a semiconductor substrate,” “the channel of the memory cell transistors MC and the select transistors UST and LST may be formed perpendicular to the XY plane,” “active pillars PL are provided for the channels of transistors, which correspond to the strings of the nonvolatile memory device according to the embodiments of the inventive concept,” and that “channels of memory cell

transistors and select transistors (LST, UST and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.” EX1004, [0043], [0045], [0054]. Chae further discloses that “a charge storage layer CS is formed to surround each of the active pillars PL each of the active pillars PL. That is, the charge storage layer CS is disposed between the active pillar PL and the gate electrodes LSL, WL and USL.” EX1004, [0055]. Thus, Chae discloses that active pillars PL with charge storage layers CS include portions of memory cell transistors MC.

180. Regarding the claimed “NAND architecture,” Chae discloses that “the NAND-type nonvolatile memory device is advantageous for high integration because it includes a cell string structure having a plurality of memory cell transistors connected in series,” and that “[e]ach string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series between the upper and lower select transistors UST and LST.” EX1004, [0005], [0043]. These disclosures are consistent with the “basic architecture of flash memory” in the Background section of the ’737 patent, as well as known in the art. EX1001, 3:1-5; see Section IX.D. Thus, Chae discloses memory cell transistors MC include a portion of NAND architecture.

181. In view of these disclosures of Chae and as further shown in FIG. D below, a POSITA would have understood, or at least found it obvious, that memory cell transistors MC (in blue) are vertically oriented transistors connected in a string

STR (in purple) in the NAND architecture (i.e., a NAND string), and that each active pillar PL includes the channels of the memory cell transistors MC, which are vertically interconnected in a respective string STR.

Fig. 1

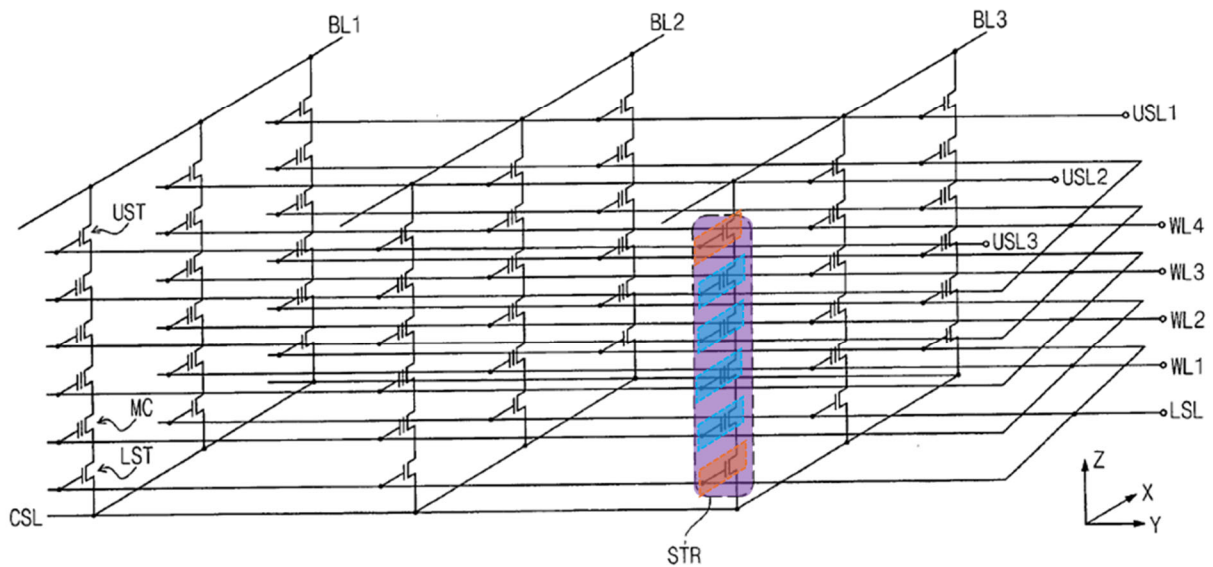


FIG. D – FIG. 1 of Chae (annotated)

[21.b.3] the at least some of the features comprising control gate lines

182. Chae discloses “the at least some of the features comprising control gate lines.”

183. Chae discloses that gate electrodes 250 include select lines and word lines. EX1004, [0078]; see also [0044], [0051], FIG. 1. Gate electrodes 250 function as select lines USL and LSL and word lines WL to control the operations of select transistors UST and LST and memory cell transistors MC connected thereto,

respectively. Thus, gate electrodes 250 include the claimed “control gate lines.”

[21.c.1] dummy structures extending vertically through the control gate lines in the end portion

184. I incorporate the discussion provided above with respect to element [11.c.1] in Grounds 1 and 2. Chae discloses element [21.c.1].

[21.c.2] some of the dummy structures being longitudinally spaced along a horizontal line

185. Chae discloses “some of the dummy structures being longitudinally spaced along a horizontal line.”

186. Chae discloses that “the dummy holes on the same line are spaced apart from each other.” EX1004, [0127]. Since Chae also discloses “charge storage layers 222a and 222b are formed at the sidewalls of the dummy holes and the channel holes, and the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b,” Chae discloses that supporters SP 224b with charge storage layers 222b are also formed “on the same line are spaced apart from each other.” EX1004, [0128].

187. FIGs. U and V below are annotated versions of FIGs. 10 and 15E of Chae, respectively. FIG. 15E is the sectional view along the line II-II’ of FIG. 10. EX1004, [0122]. FIGs. U and V further show that supporters SP 224b (in yellow) are longitudinally spaced along the line II-II’.

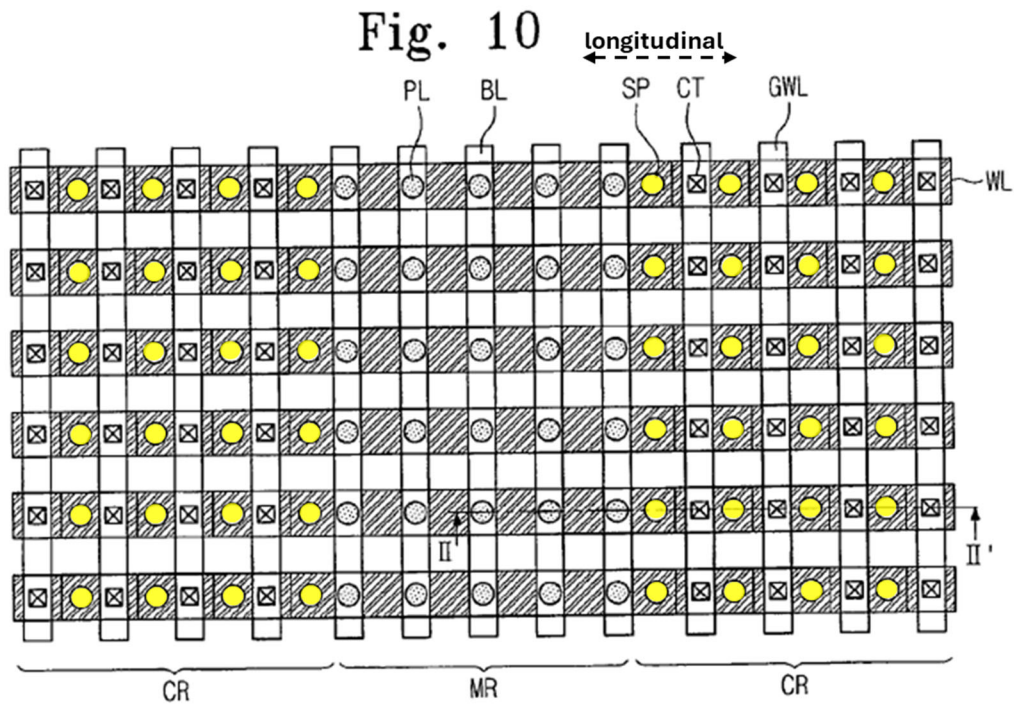


FIG. U – FIG. 10 of Chae (annotated)

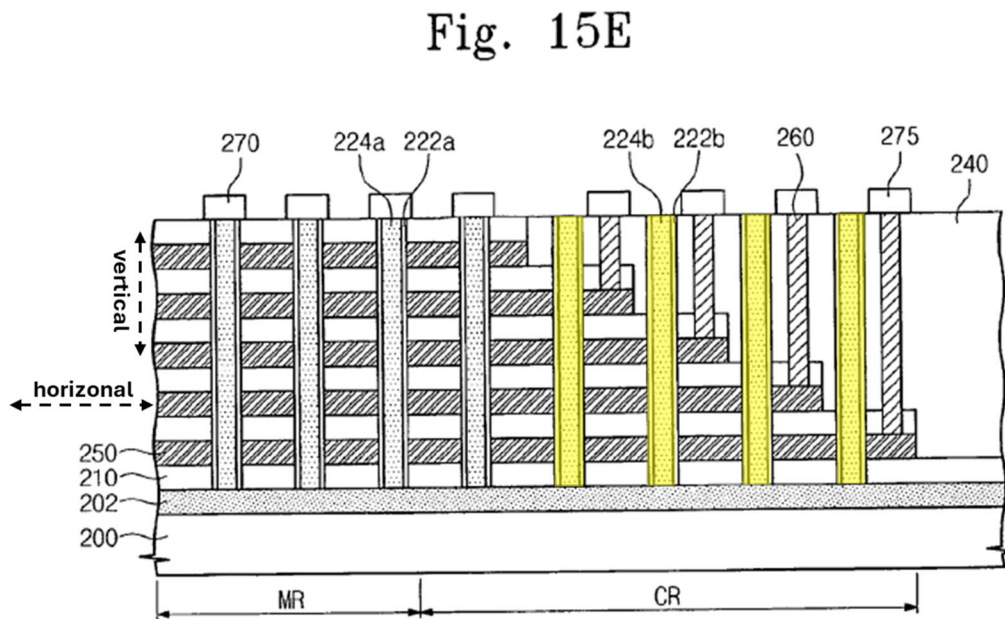


FIG. V – FIG. 15E of Chae (annotated)

[21.d.1] vertical contacts in the end portion connecting with individual of the control gate lines

188. I incorporate the discussion provided above with respect to element [15] in Grounds 1 and 2. Chae discloses element [21.d.1].

[21.d.2] at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line

189. Chae discloses or otherwise renders obvious “at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line.”

190. FIGs. W and X below are annotated versions of FIGs. 10 and 15E of Chae, respectively. FIG. 15E is the sectional view along the line II-II’ of FIG. 10. EX1004, [0122]. FIGs. W and X further show that at least one of contact plugs CT 260 (in black) is longitudinally between two immediately-longitudinally adjacent supporters SP 224b (in yellow) in the line II-II,’ along which supporters SP 224b are longitudinally spaced.

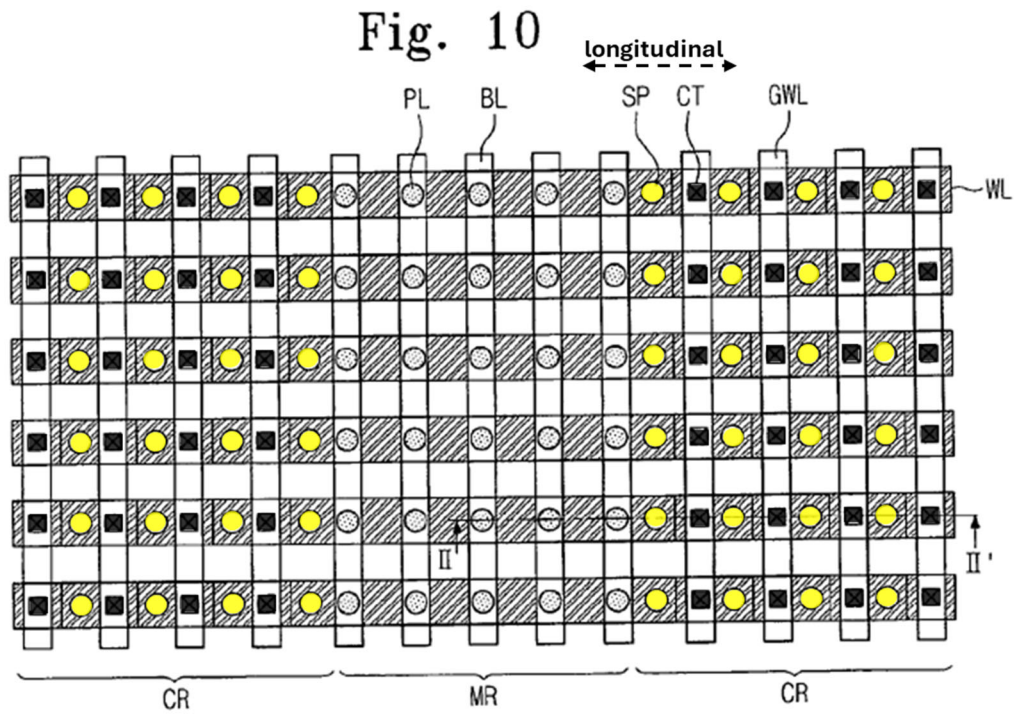


FIG. W – FIG. 10 of Chae (annotated)

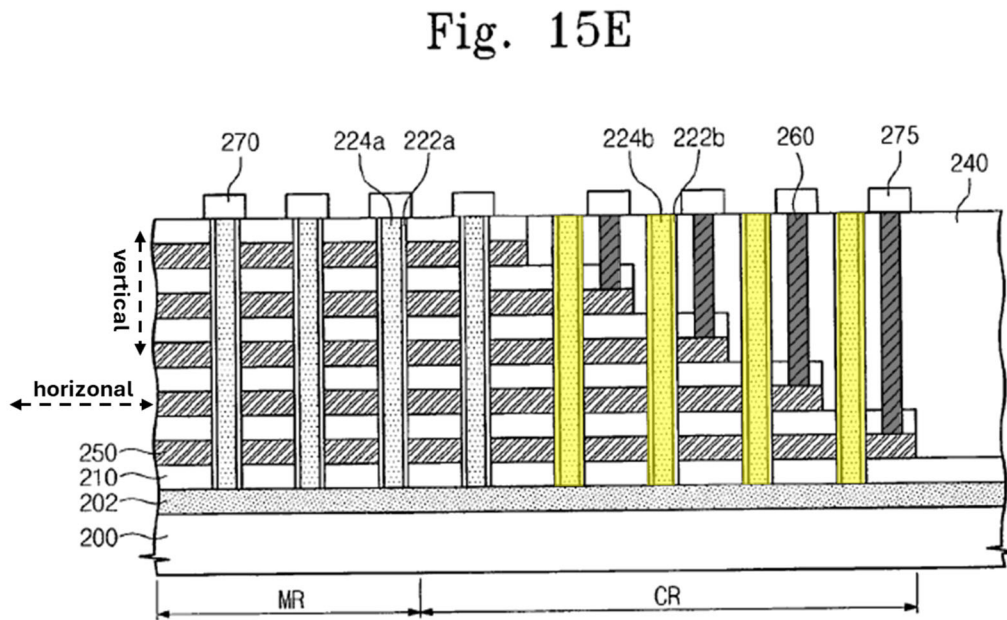


FIG. X – FIG. 15E of Chae (annotated)

O. Dependent Claim 22: The stack of claim 21 wherein the horizontal line is linearly straight.

191. Chae discloses “the horizontal line is linearly straight.” As I discussed above in Section IX.N with respect to element [21.d.2], and in particular, illustrated in FIG. W below, the line II-II’, along which supporters SP (in yellow) are longitudinally spaced, is linearly straight.

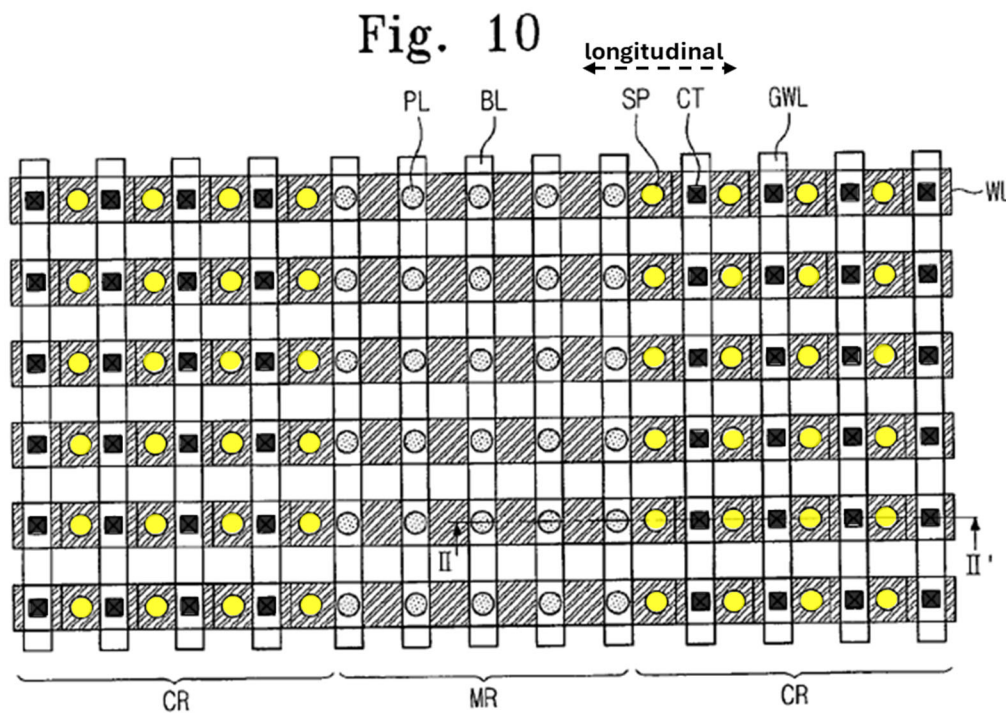


FIG. W – FIG. 10 of Chae (annotated)

X. Ground 3: Chae In View of Kiyotoshi Renders Obvious Claims 5-8, 10-12, 14, and 15

192. As I discussed in Section IX, Chae anticipates or otherwise renders obvious claims 5-8, 10-12, 14, and 15. To the extent further disclosure is required, my opinion is that Chae in view of Kiyotoshi renders these claims obvious.

A. Dependent Claims 5-8 and 10

193. As discussed in Sections IX.E-IX.G and IX.I, a POSITA would have understood, or at least found it obvious, that active pillars 224a with charge storage layers 222a and supporters 224b with charge storage layers 222b are made of the same semiconductor material and charge storage material, which are arranged in the same lateral order. See Sections IX.E-IX.G, IX.I.

194. To the extent that express teaching is required for simultaneous filling of both dummy holes and channel holes using the same materials for claims 5, 6, 8, and 10, and in the same process steps following the same sequence for claim 7, Kiyotoshi supplements the express teaching. As I discussed above in Section VIII.B, Kiyotoshi discloses the following:

Subsequently, as shown in FIGS. 33A to 33F, the semiconductor films 131 functioning as the channels are formed by a film forming method such as the LPCVD method. The semiconductor films 131 are deposited in the through-holes 135 and formed such that the lower ends thereof are connected to the semiconductor substrate 101. As the semiconductor films 131, for example, a B-doped polysilicon film can be used. The concentration of B can be set to, for example, 1×10^{17} to $1 \times 10^{18} \text{ cm}^{-3}$. The semiconductor films 131 are formed to be deposited in a macaroni shape along the inner surfaces of the through-holes 135. EX1005, [0124].

Further, the dielectric films 132 formed of a silicon oxide film or the like are formed to fill the inside of the hollow cylindrical semiconductor films 131 by the ALD method. Thereafter, etch-back is performed by a method such as the RIE method to remove the semiconductor films 131 and the dielectric films 132 above the stopper film 123. Consequently, the hollow cylindrical semiconductor films 131 and the dielectric films

132 remain only in the through-holes 135.
EX1005, [0125].

Based on these disclosures, a POSITA would have understood, or at least found it obvious, that Kiyotoshi discloses forming semiconductor films 131 and dielectric films 132 in through-holes 135, both in memory cell region 11 as the claimed “operative structures” and in word-line contact region 20 as the claimed “dummy structures,” using the same materials (e.g., B-doped polysilicon and silicon oxide) by the same film forming methods (e.g., LPCVD and ALD) following the same sequence (depositing B-doped polysilicon by LPCVD first, followed by depositing silicon oxide by ALD).

195. Chae and Kiyotoshi are analogous art, in the same field as the ’737 patent—nonvolatile memory devices. EX1001, 1:36-39; EX1004, [0002]; EX1005, [0003]. Moreover, Chae and Kiyotoshi are related to the same problem purportedly addressed by the ’737 patent—supporting dielectric layers while replacing sacrificial layers between the dielectric layers with gate layers. EX1001, 7:58-8:2; EX1004, [0129]; EX1005, [0127].

196. Chae discloses that “the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.” EX1004, [0128]. A POSITA would have been motivated to apply Kiyotoshi’s teaching of forming the claimed “operative structures” and “dummy structures”

using the same semiconductor and dielectric materials arranged in the same lateral order to Chae's device and fabrication method thereof to simplify the process and advantageously reduce the number of processing steps.

197. Reducing the number of processing steps in semiconductor fabrication would have been highly advantageous, as it directly correlates with minimizing the likelihood of defects and optimizing manufacturing efficiency. By streamlining the process, manufacturers could achieve shorter production cycles, leading to higher fabrication yields and improved cost-effectiveness. EX1014, 54; EX1015, [0004], [0108], [0190]. For instance, in the context of deposition techniques commonly used in semiconductor fabrication, it was widely recognized that each additional processing step introduced potential sources of defects, such as particle contamination, non-uniform layer formation, or interface inconsistencies. These defects could negatively impact device performance, reliability, and overall production yield. Therefore, eliminating unnecessary steps not only reduced these risks but also enhanced process stability and reproducibility.

198. Moreover, the simultaneous filling of both dummy holes and channel holes using the same materials is a well-established practice in semiconductor manufacturing. This can be achieved through various deposition processes, such as CVD and/or ALD. Specifically, as quoted above, Kiyotoshi provides explicit guidance on this process by detailing suitable deposition materials (e.g., B-doped

polysilicon and silicon oxide), deposition techniques (e.g., CVD followed by ALD), and methods for controlling the shape and thickness of the deposited semiconductor films. EX1005, [0124]-[0125]. Given Kiyotoshi's guidance and the common knowledge in the field, a POSITA would have found it straightforward to apply Kiyotoshi's teachings to Chae's device with a reasonable expectation of success.

199. Although Kiyotoshi teaches a process in which charge storage layers are formed after the holes are filled with semiconductive material (followed by a dielectric material), while Chae teaches a different sequence—forming charge storage layers inside the holes before depositing the semiconductive material—this variation in process order does not alter the fundamental teaching of Kiyotoshi regarding the simultaneous filling of holes with semiconductive and dielectric materials. The underlying benefit of depositing the same materials into multiple holes at the same time remains unchanged, regardless of whether the charge storage material is deposited before or after the semiconductor material. A POSITA would recognize that Kiyotoshi's teaching about simultaneously filling the holes with the same materials is a process optimization that enhances uniformity, reduces process complexity, and improves manufacturing efficiency. Given these advantages, a POSITA would have been motivated to apply this technique to Chae's process, understanding that the order of layer deposition does not diminish the feasibility or benefits of simultaneous hole filling.

200. Therefore, such a process would predictably work and yield the expected resulting structures—both active pillars 224a with charge storage layers 222a and supporters 224b with charge storage layers 222b have the same semiconductor material and the same charge storage material, arranged in the same lateral order.

B. Independent Claim 11 and Dependent Claims 12 and 14

201. I disagree that the “solid material” in claim 12 must be distinct from the “semiconductive material” in element [11.c.2] and claim 12, or that the “cylinder” in element [11.c.2] necessarily requires a “hollow cylinder.” Even under these unduly narrow interpretations, Chae in view of Kiyotoshi still renders claims 11, 12, and 14 obvious, in my opinion.

202. Kiyotoshi teaches that semiconductor film 131 in memory cell region 11 and dummy semiconductor film 131 in word-line contact region 20 are both “**hollow** cylindrical.” EX1005, [0116], [0125]. Kiyotoshi further explicitly explains the following:

The semiconductor films 131 are formed to be deposited in a macaroni shape along the inner surfaces of the through-holes 135. When the semiconductor films 131 are deposited in a macaroni shape, the thickness of the semiconductor films 131 controlled by the gate electrode films 134 is equal among the stacked memory cells MC. Therefore, it is possible to reduce fluctuation in transistor characteristics among the memory cells MC. Interference among the memory cells MC in independently writing electrons in the memory cells MC on both sides of one channel (semiconductor film) less easily

occurs.
EX1005, [0124].

Further, the dielectric films 132 formed of a silicon oxide film or the like are formed to fill the inside of the hollow cylindrical semiconductor films 131 by the ALD method. Thereafter, etch-back is performed by a method such as the RIE method to remove the semiconductor films 131 and the dielectric films 132 above the stopper film 123. Consequently, the hollow cylindrical semiconductor films 131 and the dielectric films 132 remain only in the through-holes 135.
EX1005, [0125].

A POSITA reading Kiyotoshi, in particular the disclosures in paragraphs [0116], [0124], and [0125], would have found it obvious to apply the same macaroni/hollow cylindrical shape with uniform thickness among the stacked memory cells to Chae's string of stack memory cells, provided by active pillars PL 224a. This is because doing so would enhance device performance for various reasons, as detailed below. Additionally, it would have been obvious to a POSITA to fill the remaining space in the channel holes with a different material, such as a dielectric material, as taught by Kiyotoshi, ensuring that the semiconductor material maintains the desired macaroni/hollow cylindrical shape.

1. Teaching, suggestion, or motivation in the prior art

203. First, Kiyotoshi itself provides teaching, suggestions, or motivation for a POSITA to replace Chae's solid cylindrical semiconductor material in active pillars 224a with Kiyotoshi's macaroni/hollow cylindrical semiconductor material filled with a dielectric material. Specifically, Kiyotoshi teaches that "[w]hen the

semiconductor films 131 are deposited in a macaroni shape, the thickness of the semiconductor films 131 controlled by the gate electrode films 134 is equal among the stacked memory cells MC. Therefore, it is possible to reduce fluctuation in transistor characteristics among the memory cells MC. Interference among the memory cells MC in independently writing electrons in the memory cells MC on both sides of one channel (semiconductor film) less easily occurs.” EX1005, [0124].

204. Thus, Kiyotoshi explicitly teaches that adopting a macaroni/hollow cylindrical semiconductor structure enhances characteristic uniformity among memory cells by ensuring consistent channel thickness and reducing variability in transistor performance. Additionally, this structure mitigates interference between adjacent memory cells, which is crucial for maintaining data integrity and reliable memory operations. Given these advantages, a POSITA would have been motivated to incorporate Kiyotoshi’s hollow cylindrical semiconductor design into Chae’s device to achieve improved performance, reduced cell-to-cell interference, and enhanced overall device reliability.

2. *Applying known techniques to a similar device in the same way*

205. Second, implementing this modification or combination simply applies Kiyotoshi’s well-established techniques to improve the performance of a similar nonvolatile memory device in Chae using the same principles. In the semiconductor

industry, it is widely recognized that reducing the thickness of semiconductor bodies in 3D NAND memory cells (or transistors in general) by adopting a macaroni/hollow cylindrical structure enhances short-channel controllability over sub-threshold characteristics. This improvement is achieved by enabling fully depleted device operation, leading to better electrostatic control over the channel. EX1016, 451; EX1017, 903-904.

206. Furthermore, this approach improves threshold voltage stability by reducing the number of grain boundaries, which helps minimize variations in device performance. EX1016, 451. Achieving better control over NAND memory cell transistors is particularly important, as reducing the semiconductor material thickness below the depletion width minimizes material volume and decreases the total number of charge traps, thereby making the threshold voltage less sensitive to fluctuations in trap density. EX1016, 451.

207. Additionally, the hollow center of the semiconductor material can be filled with a dielectric material, which not only enhances electrical isolation but also simplifies process integration in NAND memory device fabrication, leading to greater manufacturing efficiency and improved device reliability. EX1016, 451.

3. *Reasonable expectation of success*

208. Third, a POSITA would have found it routine, straightforward, and highly beneficial to apply Kiyotoshi's teaching of a hollow cylindrical

semiconductor film filled with a dielectric material to Chae's active pillars PL 224a. Kiyotoshi provides clear guidance on the formation of such structures, detailing the process steps necessary to achieve uniform semiconductor film thickness, which improves transistor performance and reduces cell-to-cell interference. EX1005, [0124]-[0125]. Moreover, this modification aligns with well-established principles in semiconductor device engineering, where replacing solid semiconductor pillars with hollow structures enhances electrostatic control and improves short-channel effects. Given the common knowledge in the field and Kiyotoshi's explicit disclosure of these benefits, a POSITA would have readily recognized that this combination would not only meet the claimed limitations but also provide predictable and desirable structural and electrical improvements. Additionally, the straightforward nature of this modification, based on known fabrication techniques, would have given a POSITA a reasonable expectation of success in implementing it without introducing undue complexity or manufacturing challenges.

209. Therefore, Chae in view of Kiyotoshi renders obvious that "the operative structures individually comprise a [hollow] cylinder of semiconductor material" in claim 14.

210. Moreover, as I discussed above in Sections IX.E, IX.F, and X.B, Chae alone discloses or at least suggests, either independently or in view of Kiyotoshi, that the same materials fill both the dummy holes and channel holes in the same

process steps and sequence to form supporters SP 224b and active pillars PL 224a, respectively. See Sections IX.E, IX.F, X.B. Accordingly, in the proposed modification or combination, Chae's supporter 224b would have the same configuration as active pillar 224a—including a hollow cylindrical semiconductor film with a different material, such as a dielectric material, filling its radially internal region.

211. Therefore, Chae in view of Kiyotoshi also renders obvious that “the dummy structures individually comprising a [hollow] cylinder of semiconductive material” in element [11.c.2] and that “solid material filling radially internal regions of individual of the [hollow] cylinders of semiconductive material” in claim 12.

C. Dependent Claim 15

212. I incorporate the discussion provided above with respect to claim 15 in Grounds 1 and 2. At least Chae discloses the additional features recited in claim 15. Thus, Chae in view of Kiyotoshi renders claim 15 obvious.

XI. Grounds 4 and 5: Jeong Anticipates or Otherwise Renders Obvious Claims 18 and 20

A. Independent Claim 18

213. Claim 18 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[18.P] A stack of horizontally extending and vertically overlapping

features, the stack comprising:

[18.a.1] a primary portion and an end portion, [18.a.2] at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

[18.b.1] operative structures extending vertically through the features in the primary portion, [18.b.2] the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, [18.b.3] at least some of the features comprising control gate lines;

[18.c] dummy structures extending vertically through the control gate lines in the end portion; and

[18.d.1] vertical contacts in the end portion connecting with individual of the control gate lines, [18.d.2] the contacts and dummy structures having different horizontal cross-sections relative one another.

[18.P] A stack of horizontally extending and vertically overlapping features, the stack comprising

214. Jeong discloses a “stack of horizontally extending and vertically overlapping features.”

215. Jeong discloses an electrode structure ES including a stack of electrodes 130, 135, and 138, as follows:

Each of the electrode structures ES may include electrodes 130, 135, and 138 sequentially stacked on the substrate 100 of the first region RE and insulating layers 110 disposed between the electrodes 130, 135, and 138. The electrodes 130, 135, and 138 and the insulating layers 110 may be alternately stacked on

the substrate 100.
EX1006, [0055].

216. As further shown in FIG. Y with my annotations below, a stack of electrodes 130, 135, and 138 (in red) in FIG. 3 of Jeong each extends horizontally and overlaps vertically.

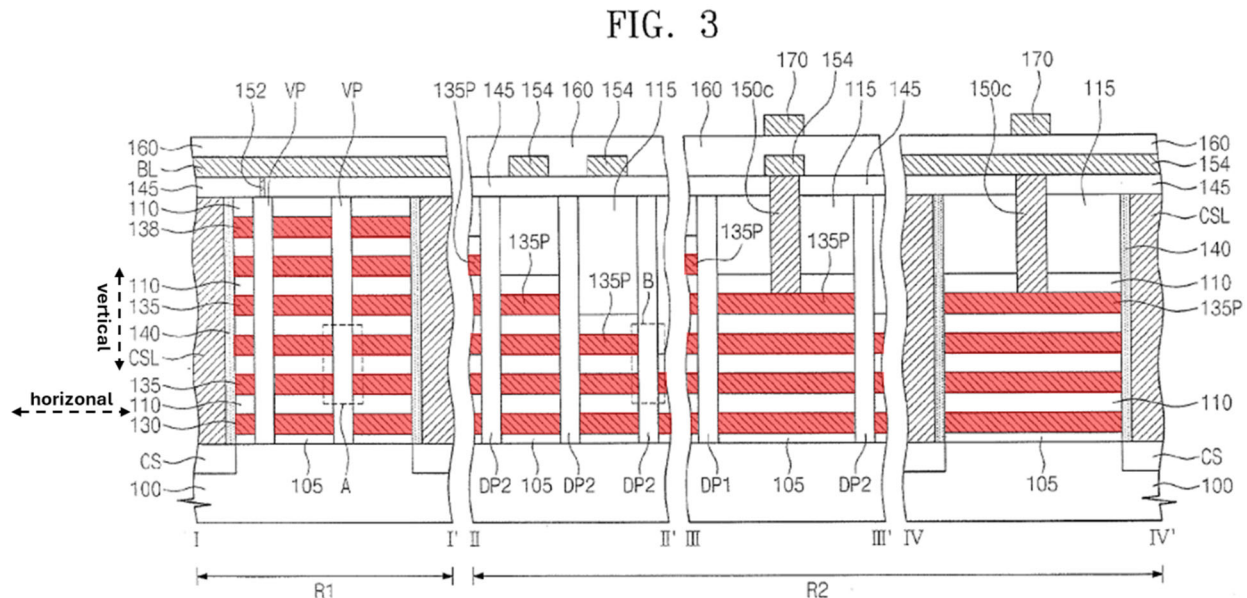


FIG. Y – FIG. 3 of Jeong (annotated)

217. Regarding the term “features,” the ’737 patent explains the following:

In one embodiment, the features may be horizontally extending lines, for example formed of any one or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s). In one embodiment, the features comprise a combination of horizontally extending conductive and dielectric lines (e.g., overlapping and alternating such lines).

EX1001, 11:28-34.

That is, the claimed “features” may be horizontally extending lines, such as horizontally extending conductive lines. See also Section IX.J([11.P].) Jeong

specifically discloses that “cell electrodes 135 may correspond to word lines, the ground selection electrode 130 may correspond to a ground selection line, and the string selection electrode 138 may correspond to a string selection line.” EX1006, [0070]. Thus, it is clear to me that electrodes 130, 135, and 138 (*i.e.*, ground selection lines, word lines, and string selection lines) of Jeong qualify as the claimed “features,” consistent with the ’737 patent.

218. Even if the term “features” is narrowly interpreted to require a combination of horizontally extending conductive lines and dielectric lines—which I disagree with—each pair of electrode 130, 135, or 138 and insulating layer 110 in Jeong would still collectively qualify as one of the “features.” Nonetheless, this alternative interpretation and mapping would not affect my analysis of Jeong with respect to any claim limitations related to the “features” in my Declaration.

[18.a.1] a primary portion and an end portion

219. Jeong discloses “a primary portion and an end portion.”

220. FIGs. Z and AA, with my annotations below, show the plan view of FIG. 1 and the cross-sectional view of FIG. 3, respectively. FIG. 3 is along the lines I-I’, II-II’, III-III’, and IV-IV’ of FIG. 1. EX1006, [0052]. As shown in FIGs. Z and AA, the electrode structure ES includes a first region R1 (labeled as “primary portion”) and a second region R2 (labeled as “end portion”). EX1006, [0053]-[0054].

FIG. 1

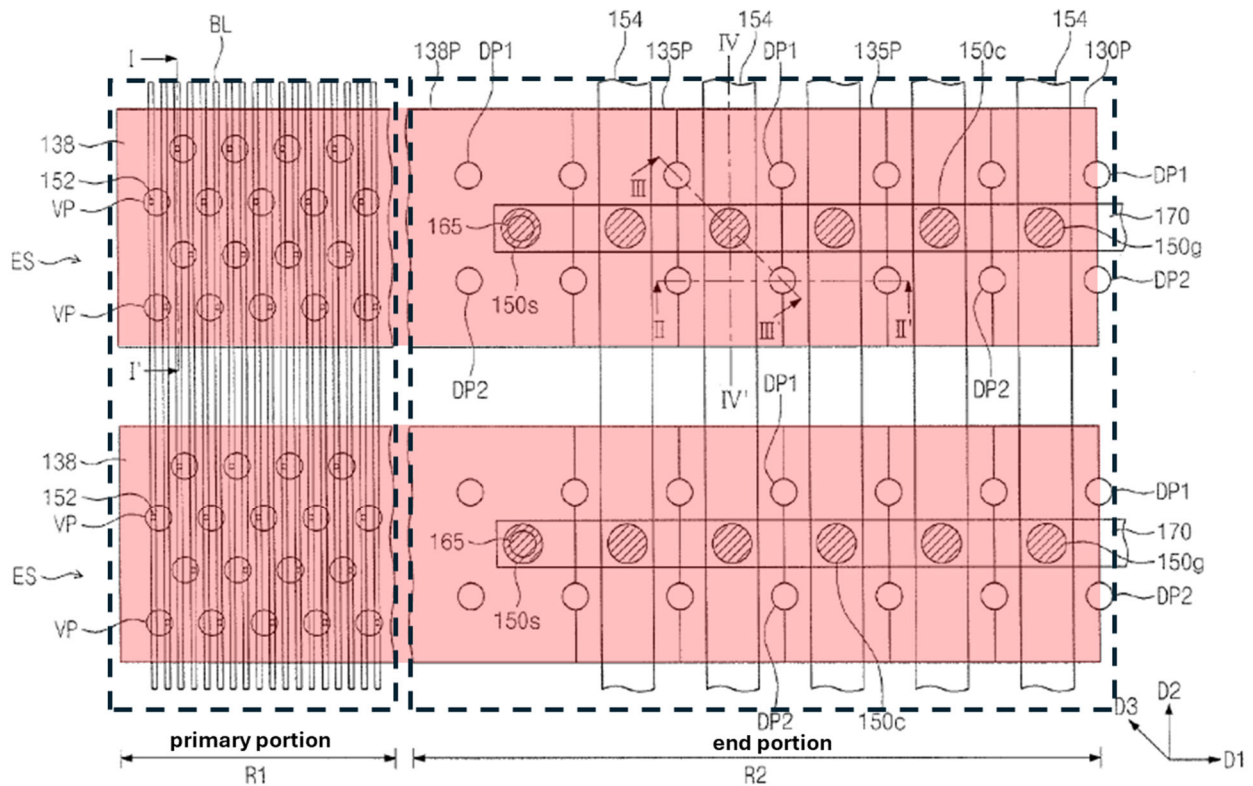


FIG. Z – FIG. 1 of Jeong (annotated)

FIG. 3

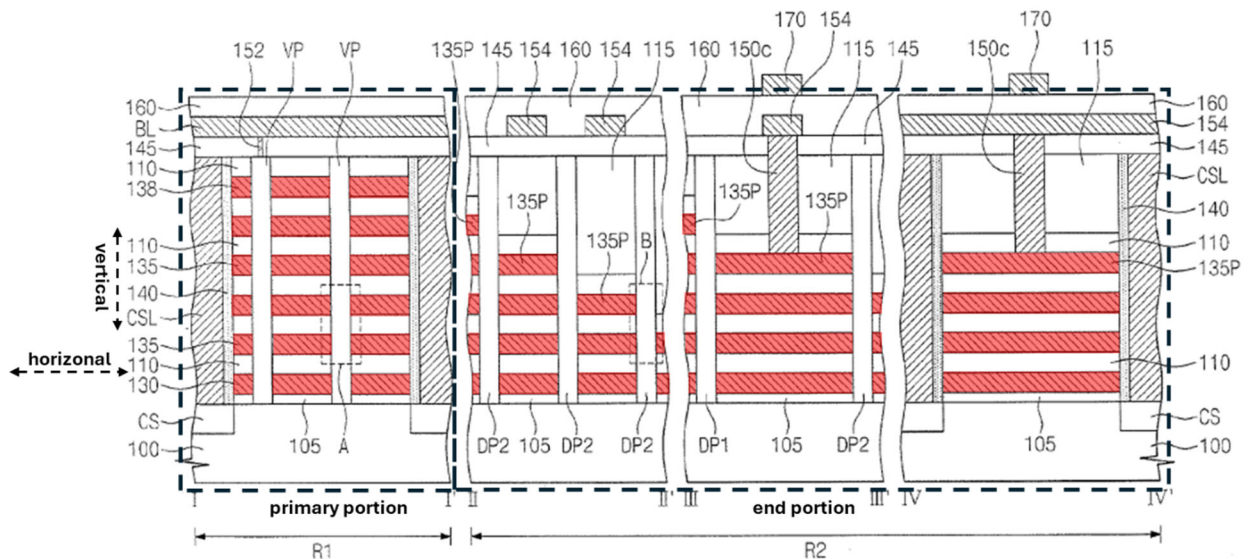


FIG. AA – FIG. 3 of Jeong (annotated)

221. Because first region R1 “may be a cell region, in which memory cells

are three-dimensionally arranged,” which is the primary portion of a memory device, first region R1 is the claimed “primary portion.” EX1006, [0053]. Because second region R2 “may be a connection region, in which pads are provided,” located at the end of the electrode structure ES, as shown in FIGs. Z and AA above, it is the claimed “end portion.” EX1006, [0053].

[18.a.2] at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion

222. Jeong discloses “at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion,” which merely recites the well-known stair-like structure in a 3D NAND memory device, as discussed above in Section VI. See, e.g., EX1020, FIG. 6.

223. Jeong also discloses this well-known structure—“electrodes 130, 135, and 138 may respectively include pads 130P, 135P, and 138P that constitute **a stepped structure** in the second region R2.” EX1006, [0055]. For instance, FIG. AA below clearly shows that, in second region R2, an electrode 130, 135, or 138 (in red) at a lower level in the vertical direction of the stack, i.e., moving deeper into the stack, extends farther in the horizontal direction.

FIG. 3

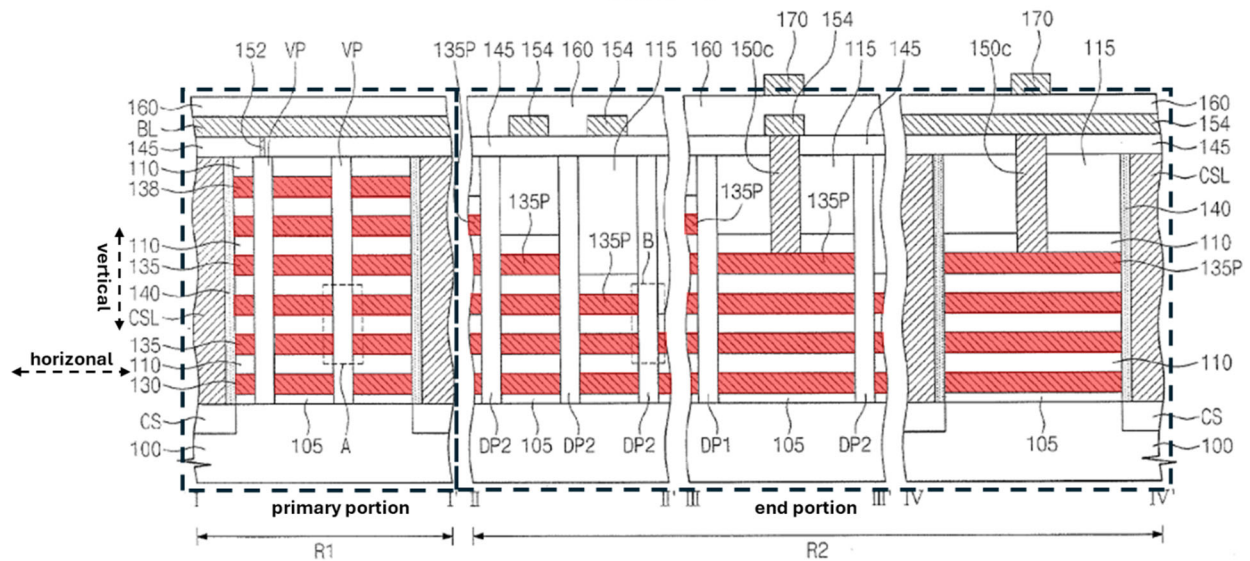


FIG. AA – FIG. 3 of Jeong (annotated)

[18.b.1] operative structures extending vertically through the features in the primary portion

224. Jeong further discloses “operative structures extending vertically through the features in the primary portion.”

225. As illustrated in FIG. AB with my annotations below, FIG. 3 of Jeong shows that in first region R1 (labeled as “primary portion”), vertical patterns VP (in green) each extends vertically through electrodes 130, 135, and 138 (in red). EX1006, [0058].

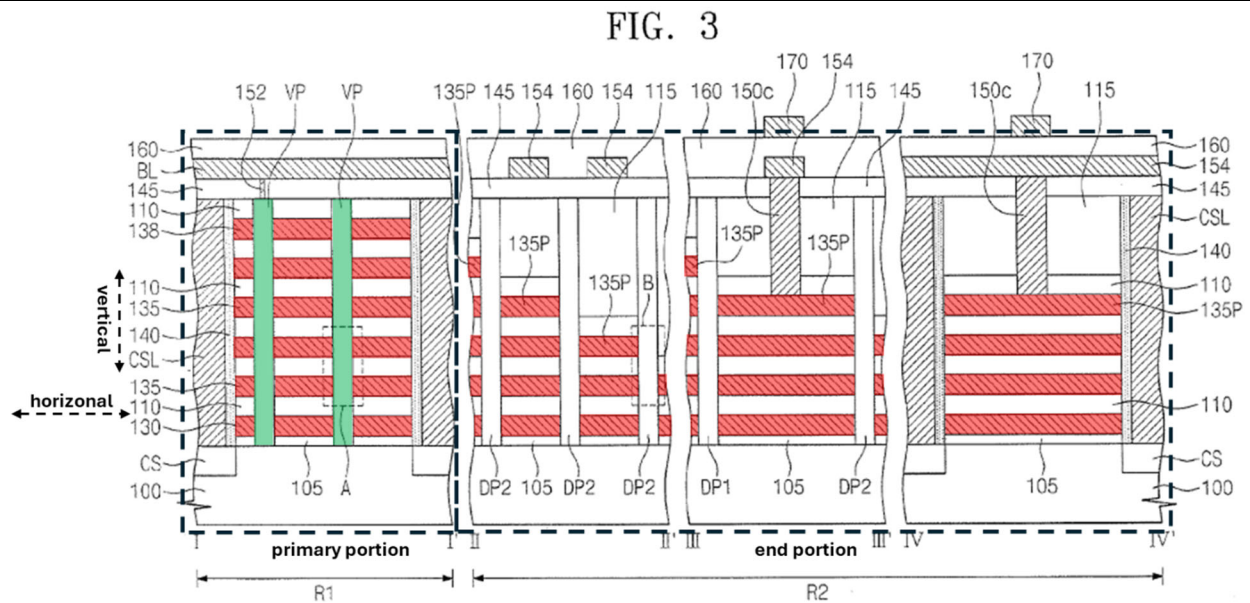


FIG. AB – FIG. 3 of Jeong (annotated)

226. Jeong specifically explains the following with respect to vertical patterns VP:

Referring to FIG. 4A, the vertical pattern VP may include a vertical semiconductor pattern SP extending upward from the substrate 100. The vertical pattern VP may further include a blocking insulating layer BIL, a charge storage layer CL, and a tunnel insulating layer TL which are disposed between the cell electrode 135 and the vertical semiconductor pattern SP.
EX1006, [0078].

227. Jeong also discloses additional details of vertical patterns VP with respect to FIGs. 4A-4D. See also, e.g., EX1006, [0079], [0082], [0085], [0088], FIGs. 4A-4D. For example, as further depicted in annotated FIG. 4A of Jeong (FIG. AC) below, a vertical pattern VP (in green) is part of a NAND memory cell string (in purple dashed box), which includes memory cells (in blue dashed boxes).

FIG. 4A

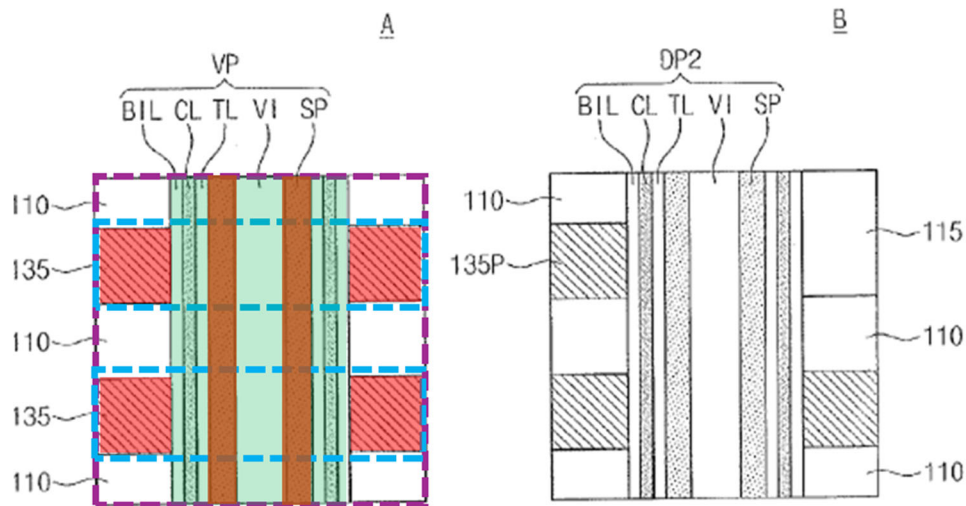


FIG. AC – FIG. 4A of Jeong (annotated)

228. Furthermore, the '737 patent describes that the claimed “operative structures” may be “circuit components.” EX1001, 6:22-25. Thus, vertical patterns VP, which include memory cells—“circuit components”—qualify as the claimed “operative structures.”

[18.b.2] the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string

229. Jeong discloses or otherwise renders obvious “the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string.”

230. Jeong further discloses vertical semiconductor pattern SP, which is part

of vertical pattern VP. EX1006, [0078]-[0079]; see also [0082], [0085], and [0088].

As illustrated in FIG. AC below, a POSITA would have understood, or at least found it obvious, that vertical pattern VP (in green) encompasses vertical semiconductor patterns SP (in brown), forming interconnected channels within the NAND memory cell string (in purple dashed box), along with portions of the memory cells (in blue dashed boxes). Additionally, a POSITA would have understood, or at least found it obvious, that the memory cells (in blue dashed box) are vertically connected in series as part of the NAND memory cell string (in purple dashed box). This configuration aligns with the claimed “NAND architecture,” which is consistent with the “basic architecture of flash memory” described in the Background section of the ’737 patent, and is widely recognized in the art. EX1001, 3:1-5; see also Section IX.D.

FIG. 4A

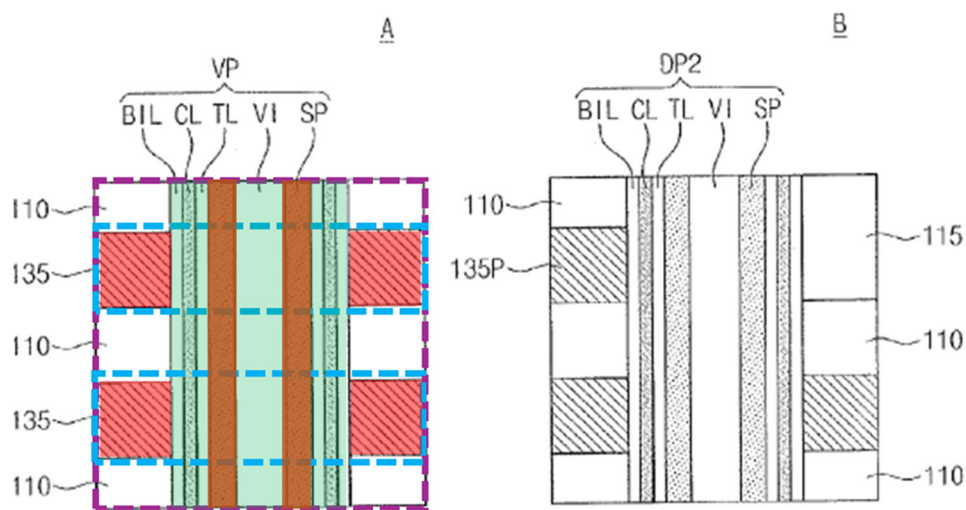


FIG. AC – FIG. 4A of Jeong (annotated)

[18.b.3] at least some of the features comprising control gate lines

231. Jeong discloses “at least some of the features comprising control gate lines.”

232. Specifically, Jeong discloses that “electrodes 130, 135, and 138 of each of the electrode structures ES may include a ground selection electrode 130, a string selection electrode 138, and cell electrodes 135 disposed between the ground selection electrode 130 and the string selection electrode 138,” and that “cell electrodes 135 may correspond to word lines, the ground selection electrode 130 may correspond to a ground selection line, and the string selection electrode 138 may correspond to a string selection line.” EX1006, [0056], [0070].

233. Ground selection electrodes 130, cell electrodes 135, and string selection lines 138 function as ground selection lines, word lines, and string selection lines to control ground selection, string selection, and cell operation, respectively. Thus, electrodes 130, 135, and 138 include the claimed “control gate lines” of element [18.b.3].

[18.c] dummy structures extending vertically through the control gate lines in the end portion

234. Jeong further discloses “dummy structures extending vertically through the control gate lines in the end portion.”

235. As shown in FIG. AD with my annotations below, FIG. 3 of Jeong

illustrates that in second region R2 (labeled as “end portion”), dummy pillars DP1 and DP2 (in yellow) each extends vertically through electrodes 130, 135, and 138 (in red). EX1006, [0060]-[0061].

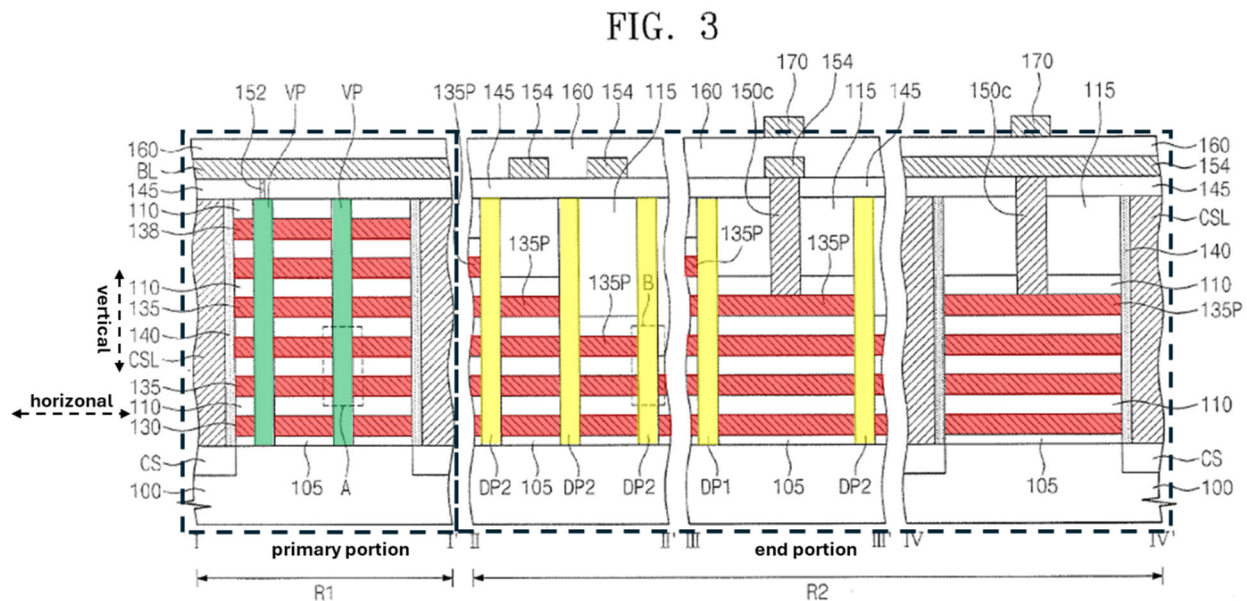


FIG. AD – FIG. 3 of Jeong (annotated)

236. Specifically, Jeong discloses that “[w]hen the sacrificial layers 120 are removed, the dummy pillars DP1 and DP2 support the insulating layers 110 and the capping layer 115 in the second region R2, and the vertical patterns VP may support the insulating layers 110 in the first region R1,” and that “formation of the dummy pillars DP1 and DP2 through the insulating layers 110 in the second region R2 supports the insulating layers 110 during removal of the sacrificial layers 120, thereby minimizing or preventing the above problems, e.g., misalignment and/or breaking of the insulating layers 110.” EX1006, [0109]-[0110], see also [0074]. As discussed above in detail in Section VIII.C, Jeong also discloses that vertical patterns

VP and dummy pillars DP1 and DP2 are formed in the same process with the same structure and materials. See Section VIII.C. Based on those disclosures, a POSITA would have understood that dummy pillars DP1 and DP2 mimic a physical property of vertical patterns VP.

237. As I also discussed above in Section VIII.C, dummy pillars DP1 and DP2 are electrically inoperable because dummy pillars DP1 and DP2 are covered by first insulating layer 145, as opposed to conductive contacts, such as bit line contact plugs 152. EX1006, FIG. 3; see Section VIII.C.

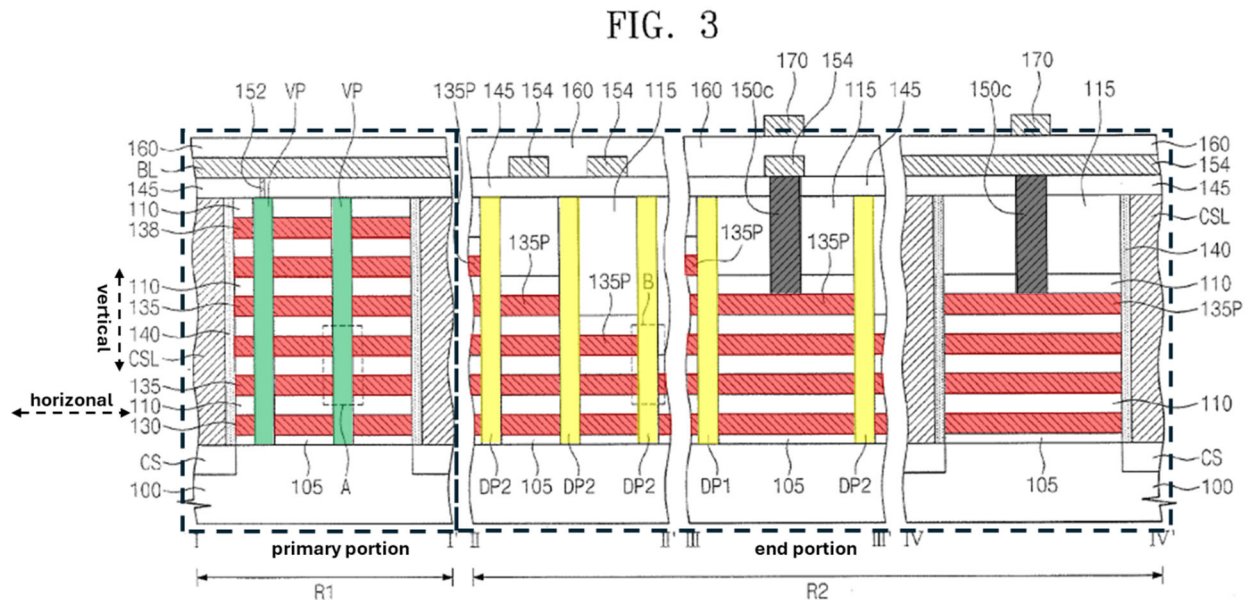
238. Therefore, dummy pillars DP1 and DP2 are the claimed “dummy structures” under the construction of “electrically inoperable structure that mimics a physical property of an operative structure.” See Section VII.D.

[18.d.1] vertical contacts in the end portion connecting with individual of the control gate lines

239. Jeong further discloses “vertical contacts in the end portion connecting with individual of the control gate lines.”

240. As shown in FIG. AE with my annotations below, FIG. 3 of Jeong illustrates that contact plugs 150 (in black) in second region R2 (labeled as “end portion”), each extending to and connecting with a respective electrode 130, 135, or 138 (in red). For example, Jeong discloses that “[c]ell contact plugs 150c may be provided on the substrate 100 of the second region R2 so as to be connected to the

cell pads 135P of each of the electrode structures ES, respectively,” and that “string selection contact plug 150s may be provided on the substrate 100 in the second region R2 so as to be connected to the string selection pad 138P of each of the electrode structures ES. A ground selection contact plug 150g may be provided on the substrate 100 of the second region R2 so as to be connected to the ground selection pad 130P of each of the electrode structures ES.” EX1006, [0066].



[18.d.2] the contacts and dummy structures having different horizontal cross-sections relative one another

241. Jeong further discloses “the contacts and dummy structures having different horizontal cross-sections relative one another.”

242. Specifically, Jeong explicitly teaches that “a size of each of the dummy pillars is smaller than that of each of the contact plugs, when viewed from a plan

view,” and “a diameter of each of the dummy pillars is less than that of the contact plug, when viewed from a plan view.” EX1006, claims 25, 34, 39. That is, Jeong clearly discloses dummy pillars DP1 and DP2 and contact plugs 150 have different sizes, *e.g.*, diameters, from the plan view.

B. Dependent Claim 20: The stack of claim 18 wherein the different horizontal cross-sections have different values of total horizontal area relative one another.

243. Jeong further discloses “the different horizontal cross-sections have different values of total horizontal area relative one another.” Specifically, Jeong discloses that the area in the plan view of each dummy pillar DP1 or DP2 is smaller than that of contact plug 150. EX1006, claims 25, 34, 39; see also Section XI.A([18.d.2].) Thus, dummy pillar DP1 or DP2 and contact plug 150 have different values of total horizontal area.

XII. Ground 6: Chae In View of Hwang Renders Obvious Claims 18 and 20

244. In addition to Grounds 4 and 5 above in which Jeong alone anticipates or otherwise renders obvious claims 18 and 20, Chae in view of Hwang, in Ground 6, also renders obvious claims 18 and 20 regardless of whether claims 18 and 20 are entitled to any of the ’737 patent’s claimed priority dates.

A. Reasons to Combine Chae and Hwang

245. A POSITA would have found it obvious to combine Chae’s stack with Hwang’s buried contact plugs 450, which have a rectangular horizontal cross-section,

as discussed in Section VIII.D, for the reasons detailed below. This proposed modification would result in Chae's contact plugs CT also having a rectangular horizontal cross-section.

1. Simple substitution of one known element for another

246. As one viable example of the proposed combination, I modify and annotate FIG. 10 of Chae by designing Chae's contact plugs CT (in black) to have a rectangular horizontal cross-section, as illustrated in FIG. AF below. This example is not intended to represent the only possible way to combine Chae and Hwang.

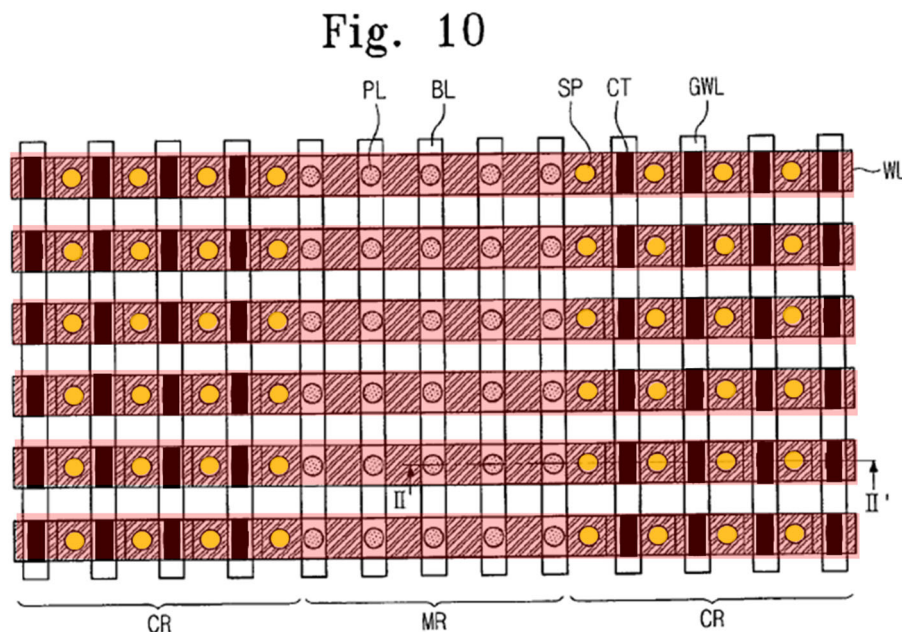


FIG. AF – FIG. 10 of Chae (modified and annotated)

247. For a POSITA, the proposed modification is merely a straightforward substitution of Hwang's rectangular buried contact plugs 450 for Chae's contact plugs CT, resulting in predictable benefits—specifically, increasing the horizontal

area of Chae's contact plugs CT to reduce resistance while maintaining adequate margins and safe distances from adjacent supporters SP.

248. A POSITA would readily recognize the advantages of substituting Hwang's rectangular buried contact plugs 450 (serving as gate line contacts) for Chae's contact plugs CT (also serving as gate line contacts), as shown in FIG. AF above. This substitution increases the horizontal area of Chae's contact plug CT. In particular, a POSITA would understand that increasing the horizontal area of a contact plug, such as contact plug CT, reduces its bulk resistance. EX1018, [0032]. Additionally, a larger horizontal area improves contact interfaces with both the word lines below and the global word lines above, thereby effectively lowering contact resistance. Consequently, this modification enhances the overall electrical performance of the nonvolatile memory device.

249. As illustrated in the modified FIG. 10 of Chae below (shown as FIG. AH of my Declaration), supporters SP and contact plugs CT are arranged alternately in a straight horizontal line (e.g., along the line II-II'). See Section IX.N([21.d.2]). This specific arrangement, while structurally efficient, imposes limitations on the possible horizontal shapes that contact plugs CT can adopt, particularly when attempting to reduce resistance by increasing their size. Since supporters SP have a circular horizontal cross-section (see Section IX.J([11.c.2])), it would be challenging to design the horizontal cross-section of contact plugs CT in a similarly circular

shape while also increasing their size. Enlarging the diameter of a circular contact plug CT to reduce resistance would inherently decrease the spacing between adjacent supporters SP and contact plugs CT. This reduction in spacing could lead to increased risks of process defects, such as misalignment or etching inaccuracies, potentially resulting in electrical shorts or structural instability. Additionally, the decreased spacing could negatively impact overall fabrication yield by making it more difficult to maintain consistent process tolerances, thus complicating large-scale production.

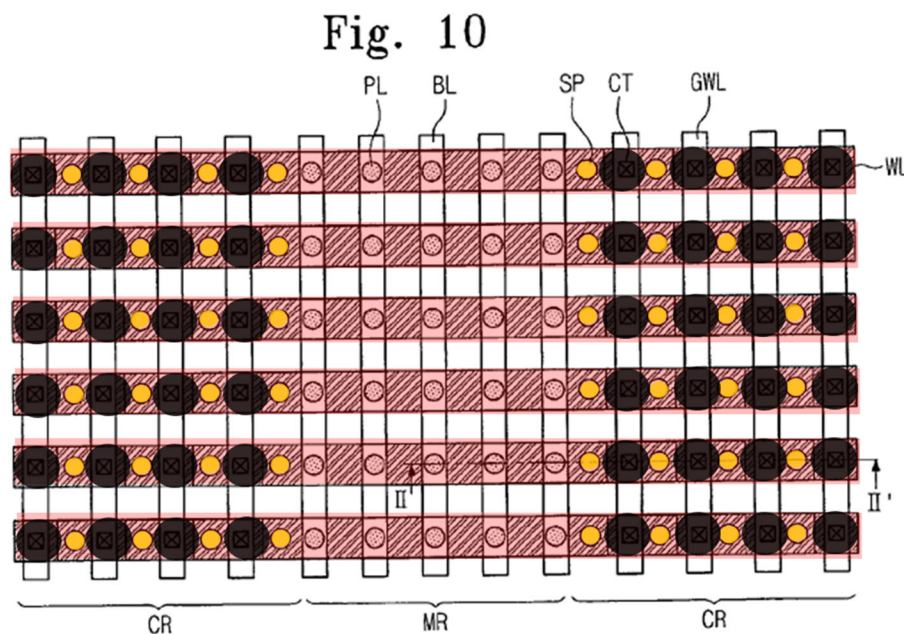


FIG. AH – FIG. 10 of Chae (modified and annotated)

250. Thus, a POSITA would have found it obvious to design contact plugs CT with a **non-circular** horizontal cross-section, such as a rectangular shape, as taught by Hwang and shown in FIG. AF above. This design enables an increase in

the horizontal area of contact plug CT by enlarging only one dimension in the bit line direction (perpendicular to the line II-II'), while maintaining sufficient spacing between adjacent supporters SP and contact plug CT in the word line direction (along the line II-II').

251. Additionally, the need to increase the effective memory cell density (i.e., the number of memory cells per unit device area) drives the reduction of contact region CR size along the word line direction (i.e., line II-II'), as these regions consume valuable device area that could be used for memory cell formation. EX1014, 50. Therefore, designing contact plugs CT with a rectangular horizontal cross-section having a smaller dimension along the word line direction, as taught by Hwang, would be particularly advantageous for increasing memory cell density.

2. *Reasonable expectation of success*

252. A POSITA would also have a reasonable expectation of success in combining Chae and Hwang as the proposed combination would yield predictable results. At the outset, Chae and Hwang are analogous prior art in the same field as the '737 patent, which pertains to nonvolatile memory devices. EX1001, 1:36-39; EX1004, [0002]; EX1007, [0002]. Both references address the same problem as the '737 patent—supporting dielectric layers while removing sacrificial layers between them. EX1001, 7:58-8:2; EX1004, [0129]; EX1007, [0120].

253. Furthermore, Chae and Hwang exhibit significant similarities in their

stacked structures, as required by claim 18. See Sections VIII.A, VIII.D. A comparison of FIG. 15E of Chae with FIG. 8 of Hwang, shown as FIG. AG below, demonstrates that both disclose substantially the same stacked structure, as recited in claim 18. Specifically, as shown in FIG. AG, each of Chae and Hwang's stack structures includes the claimed stack of "gate lines" (in red) with a stair-like structure, the claimed "operative structures" (in green) in the "primary portion," the claimed "dummy structures" (in yellow) and "vertical contacts" (in black) in the "end portion." These similarities establish a foundation for interchangeability between their stacks, enabling the successful substitution of components (e.g., gate line contact plugs) from one reference with their counterparts in the other.

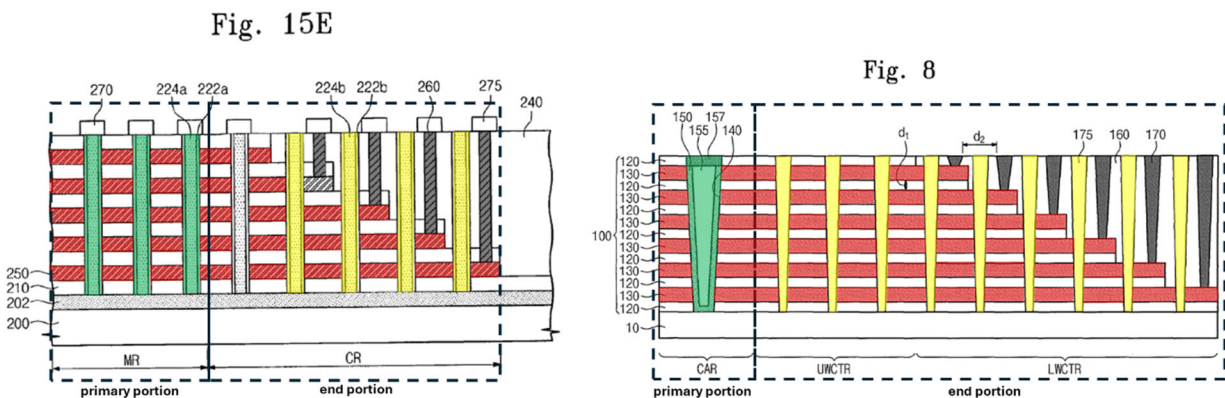


FIG. AG – Comparison of FIG.15E of Chae with FIG. 8 of Hwang (annotated)

254. Specifically, both Hwang's buried contact plugs 450 and Chae's contact plugs CT 260 are arranged in a similar configuration, as shown in FIG. AG above—each extending vertically to and connecting with a respective gate line (in

red) at the stair-like structure in the “end portion” of the stack. Also, both Hwang’s buried contact plugs 450 and Chae’s contact plugs CT 260 serve the same function, i.e., as gate line contacts connecting gate lines to global gate lines.

255. A POSITA would have found it routine, straightforward, and advantageous to substitute Hwang’s rectangular horizontal cross-section design of buried contact plugs 450 in place of Chae’s contact plugs CT 260. A POSITA would have recognized that such a modification, which satisfies the claimed limitations, would predictably function as expected and yield the anticipated resulting structure (e.g., as shown in FIG. AF). Furthermore, this modification would provide the expected technical benefits of reduced resistance and increased cell density without compromising production yield.

3. Teaching, suggestion, or motivation in the prior art

256. Chae aims to enhance the operation speed of its 3D nonvolatile memory device by reducing electrode resistance. EX1004, [0007], [0160]. While Chae proposes various designs to lower the resistance of gate lines, it does not address the design of its contact plugs CT, which, as gate line contacts, directly interface with the gate lines.

257. Given this gap in Chae’s disclosure and its objectives, a POSITA would have been motivated to explore designs that could also reduce the resistance of Chae’s gate line contacts, e.g., contact plugs CT 260, while remaining compatible

with Chae's device.

258. Hwang happens to specifically address gate line contact structures (e.g., word line contacts) and provide detailed teachings on various designs, including buried contact plugs 450. EX1007, [0032], [0196]-[0197]. Notably, Hwang explicitly states:

The buried contact plugs 450 may have a substantial hexahedron shape. That is, the buried contact plugs 450 may have a horizontal cross-section of a substantially rectangular shape. In this case, the length of one of two sides defining the horizontal cross-section of the rectangular shape may substantially be the same as the width of the lower conductive pattern 430. EX1007, [0114].

Thus, Hwang teaches, or at least suggests, maximizing the horizontal cross-section of buried contact plug 450 to match the width of lower conductive patterns 430, which serve as gate lines, such as word lines WL. Accordingly, a POSITA would have been motivated to apply Hwang's design to Chae's contact plugs CT to reduce their resistance by increasing the dimension of contact plugs CT, for example, to also match the width of the gate lines.

259. Additionally, Hwang explains:

According to the modified example, since the sacrificial contact pattern 170 and the supporting member 175 are disposed between the one sidewalls of the lower sacrificial layers 130 vertically adjacent to each other, the distance d2 between the sacrificial contact patterns 170 may be larger than that of first embodiments of inventive concepts. EX1007, [0121], see also FIGs. 2C, 8.

A POSITA would have understood that this disclosure teaches, or at least suggests, that when supporting members 175 are arranged, as shown in FIG. 8, between adjacent buried contact plugs 450 (which eventually replaced sacrificial contact patterns 170), the distance d_2 between adjacent buried contact plugs 450 should be increased compared to FIG. 2C. This would ensure that an adequate space is maintained between adjacent supporting members 175 and buried contact plugs 450, thereby preventing process defects.

260. Therefore, a POSITA would have been motivated to adopt the same rectangular design for Chae's contact plugs CT as Hwang's buried contact plugs 450. As depicted in the example below in FIG. AF, Chae's modified contact plugs CT (in black) would have a rectangular horizontal cross-section, with one side matching the width of word line WL (in red), while the other side would be smaller to maintain a sufficient distance from adjacent supporters SP (in yellow). This modification would enhance electrical performance by reducing resistance, while preserving production yield, thereby advancing Chae's goal of improving device operation speed.

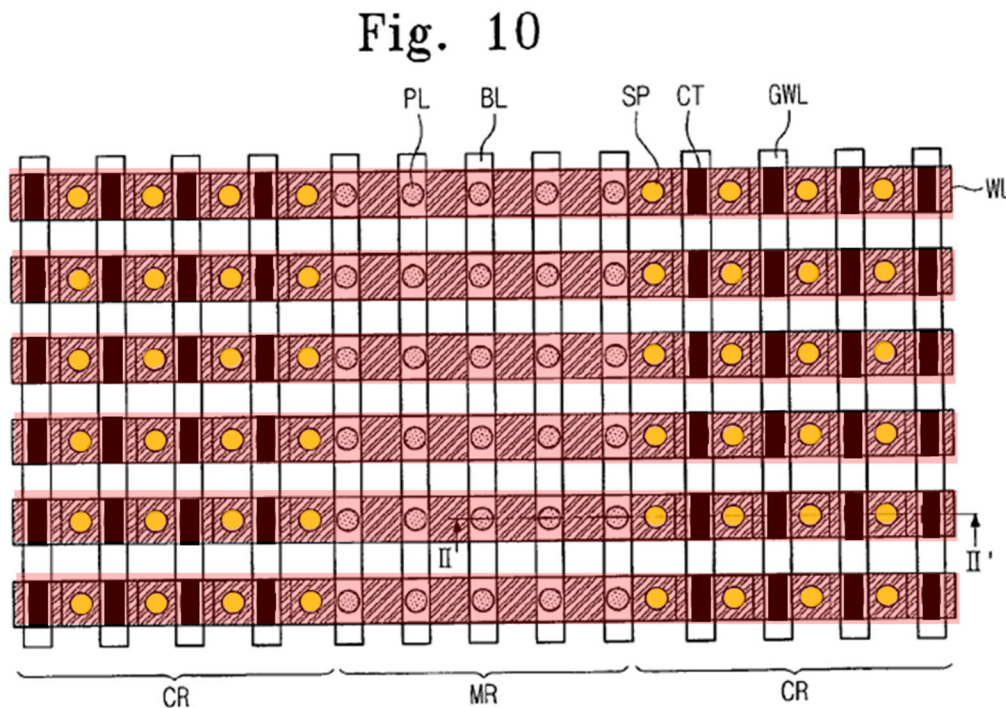


FIG. AF – FIG. 10 of Chae (modified and annotated)

B. Independent Claim 18

261. Because elements [18.P], [18.a], [18.b], [18.c], and [18.d.1] are identical to corresponding elements [21.P], [21.a], [21.b.1]-[21.b.3], [21.c.1], and [21.d.1], I incorporate my discussions provided above with respect to elements [21.P], [21.a], [21.b.1]-[21.b.3], [21.c.1], and [21.d.1] in Grounds 1 and 2. For the same reasons, at least Chae discloses or otherwise renders obvious elements [18.P], [18.a], [18.b], [18.c], and [18.d.1]. See Section IX.N.

262. Hwang also discloses element [18.d.1], which recites “vertical contacts in the end portion connecting with individual of the control gate lines.” Specifically, Hwang discloses that in lower word line contact region LWCTR, “buried contact

plugs 450 are locally formed in the contact recess region 353 to be connected to the lower conductive patterns 430, respectively.” EX1007, [0093]. As shown in FIG. K (annotated FIG. 8 of Hwang) below, lower sacrificial contact patterns 170 (in black) in lower word line contact region LWCTR each connects with a respective lower sacrificial layer 130 (in red). Hwang explains that lower sacrificial contact patterns 170 and lower sacrificial layers 130 are eventually replaced with buried contact plugs 450 and lower conductive patterns 430, respectively. EX1007, [0080], [0091], [0093].

Fig. 8

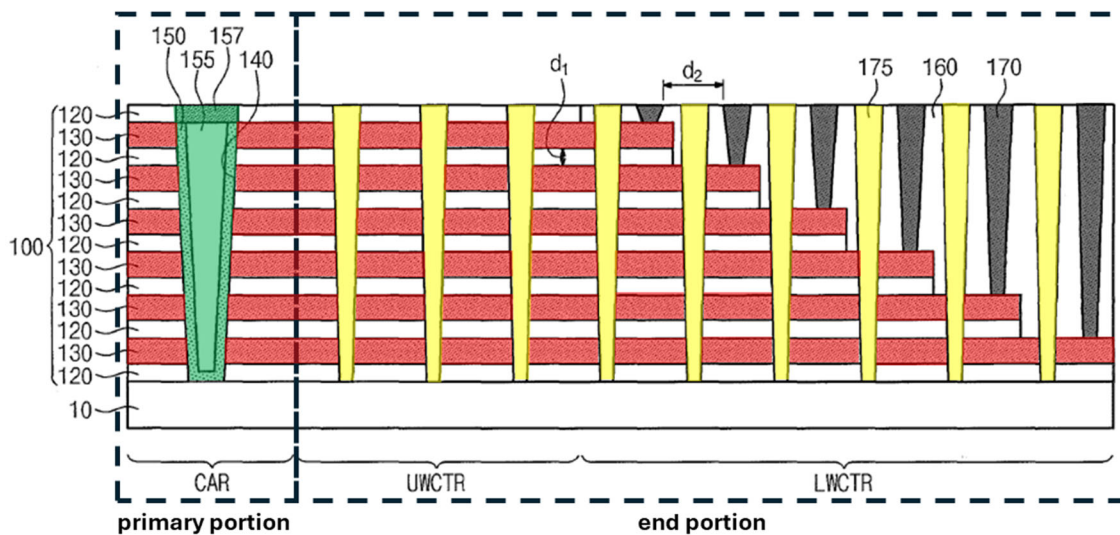


FIG. K – FIG. 8 of Hwang (annotated)

263. As to element [18.d.2], which recites “the contacts and dummy structures having different horizontal cross-sections relative one another,” as discussed in Section IX.J([11.c.2]), Chae discloses, or at least suggests, that in its

fifth embodiment, supporters SP 224b with charge storage layers 222b have a circular horizontal cross-section. Hwang, in its first embodiment, explicitly teaches that buried contact plugs 450 have a “horizontal cross-section of a substantially rectangular shape.” EX1007, [0114], FIG. 7.

264. As I discussed above in Section XII.A, a POSITA would have found it obvious to modify Chae’s device by incorporating Hwang’s rectangular buried contact plugs 450, resulting in a modified device that includes supporters SP 224b with charge storage layers 222b having a **circular** horizontal cross-section, and contact plugs CT 260 having a **rectangular** horizontal cross-section. Thus, Chae in view of Hwang renders obvious that “the contacts and dummy structures having different horizontal cross-sections relative one another.”

C. Dependent Claim 20

265. As I discussed in Section XII.A, a POSITA would have found it obvious that, in the combination of Chae and Hwang, the total horizontal area of the rectangular cross-section of contact plugs CT 260 is larger than that of the circular cross-section of supporters SP 224b with charge storage layers 222b. This would result in contact plugs CT 260 having lower resistance.

266. Conversely, a POSITA would not have been motivated to increase the total horizontal area of supporter 224b with charge storage layer 222b to make it the same as the total horizontal area of the rectangular cross-section of contact plugs

260. This is because doing so would increase the diameter of the circular horizontal cross-section, thereby reducing the margin between adjacent contact plug 260 and supporter 224b, which would increase the likelihood of process defects.

Fig. 15E

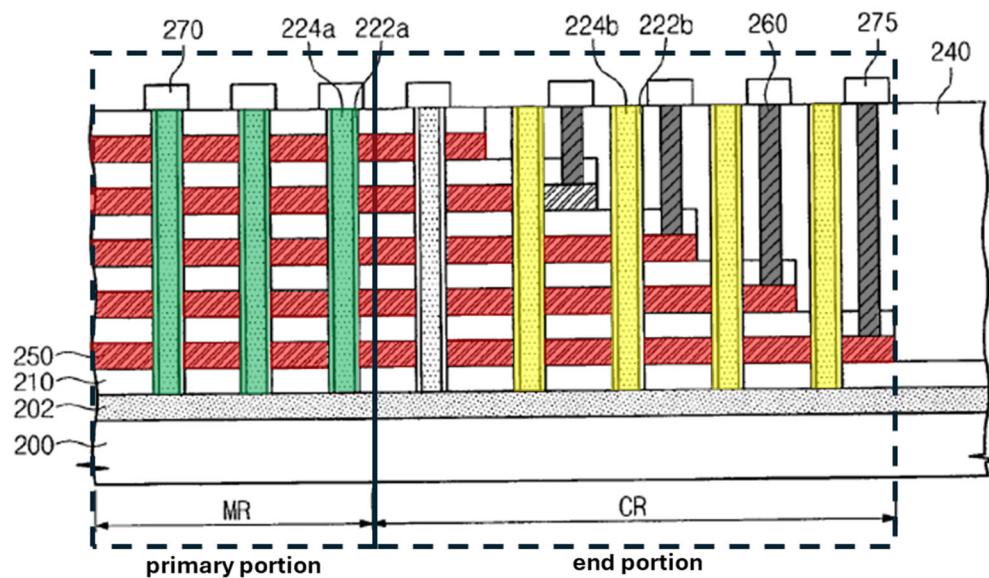


FIG. F – FIG. 15E of Chae (annotated)

267. Furthermore, contact plugs CT 260 and supporters SP 224b with charge storage layers 222b are two distinct structures: (i) they serve different functions—contact plugs CT 260 are gate line contacts, while supporters SP 224b with charge storage layers 222b are dummy structures; (ii) they have different configurations, as shown in FIG. F above (in black and yellow), with distinct structures, depths, and materials; (iii) they are formed through separate fabrication processes, as shown in FIGs. 15B and 15E of Chae, where contact plugs CT 260 are formed (FIG. 15E)

after supporters SP 224b with charge storage layers 222b are formed (FIG. 15B). Therefore, it would not be obvious to a POSITA to design them to have the same total horizontal area in light of their distinctions.

XIII. Secondary Considerations

268. I have seen no evidence in the '737 patent's prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any of the challenged claims. See generally EX1002. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the '737 patent were already well known. To the extent Patent Owner asserts the existence of any secondary considerations in its responses, I reserve my right to address any such evidence.

XIV. Additional Remarks

269. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

270. In signing this declaration, I recognize that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-

examination within the United States during the time allotted for cross-examination.

271. I have reviewed the accompanying Petition for *Inter Partes* Review of the '737 patent and, given the information set forth in this declaration, I agree with the reasoning and conclusions of the grounds of challenge in the petition. Based on my own analysis, I agree that: (1) Chae anticipates or otherwise renders obvious claims 1-12, 14, 15, 21, and 22; (2) Chae in view of Kiyotoshi further renders obvious claims 5-8, 10-12, 14, and 15; (3) Jeong anticipates or otherwise renders obvious claims 18 and 20; (4) Chae in view of Hwang also renders obvious claims 18 and 20.

* * *

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this proceeding.

Dated: 2/12/25

By: Kelin Kuhn
Dr. Kelin Kuhn
Winthrop, Washington

APPENDIX A

CURRICULUM VITAE
Dr. Kelin J. Kuhn

CONTACT INFORMATION:

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EDUCATION:

Ph.D., Electrical Engineering, Stanford University, Stanford, CA. June 1985
M.S., Electrical Engineering, Stanford University, Stanford, CA. June 1985
B.S., Electrical Engineering, University of Washington, Seattle, WA. March 1980
(magna cum laude)

PRESENT ROLE:

**Confluence Technology Services, Winthrop, WA (kjkuhn@confluence-tech.com);
present role**

Dr. Kuhn's business (Confluence Technology Services) supports a variety of engineering services in electronics and photonics, with emphasis on CMOS and beyond-CMOS technologies.

**Cornell University, Ithaca, NY; Materials Science and Engineering (kjk236@cornell.edu)
2014 to date**

Position: Adjunct Professor
Key Collaborator: Darrell Schlom

Prof. Kuhn's role is collaborating with a diverse group of faculty (both at Cornell and elsewhere) for establishment of long-term research programs in the area of valleytronics, inverse-design, quantum materials, post-CMOS technology, and spintronics.

CLIENTS / SIGNIFICANT INTERACTIONS POST-2014:

Bayes PLLC: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *Inter Partes Review of U.S. Patent Nos. 8,803,214 And 10,475,737*.

Pillsbury Winthrop Shaw Pittman LLP: Initiated 2024 and on-going. Technical evaluation and consulting on matters related to *MicroSemi Corporation v. Commissioner of Internal Revenue*.

Ropes and Gray: Initiated 2023 and on-going. Technical evaluation and consulting on the matters related to *Yangtze Memory Technologies Company, LTD. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC, Case No. 5-23-cv-05792*.

Heim, Payne & Chorush: Initiated 2023 and on-going. Technical evaluation and consulting representing *Microchip Corporation* and its subsidiary *Silicon Storage Technology, Inc.* with regards to a dispute with *Taiwan Semiconductor Manufacturing Company*.

Smith Baluch LLP: Initiated 2022 and on-going. Technical evaluation and consultation to advise and assist Smith Baluch LLP matters relating to semiconductor processing.

Carter Arnett: Initiated 2022 and ongoing. Technical evaluation and consultation to advise and assist Carter Arnett PLLC in representing *Katana Silicon Technologies, LLC* in IPR2022-00763 and litigation related to Case No. 6:22-cv-00191 (W.D. Tex), adverse to *GlobalFoundries, Inc., GlobalFoundries, U.S. Inc., and GlobalFoundries U.S. 2 LLC*.

Mintz: Completed 2022-2023. Technical evaluation and consulting representing *Daedalus Prime LLC* with regards to the ITC Case: 337-TA-133, Certain Semiconductor Devices, Mobile Devices Containing Same (Taiwan Semiconductor Manufacturing Company).

Heim, Payne & Chorush: Completed 2021-2023. Technical evaluation and consulting representing *Arigna Technology Limited* with regards to IPR2021-01321 (*Volkswagen*) and IPR2021-01382 (*Infineon*).

Quinn Emanuel Urquhart & Sullivan: Believed complete 2021-2023. Technical evaluation and consulting representing *Hanwha* with regards to ITC Inv. No. 337-TA-1271.

Ropes and Gray: Completed 2021-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Lawrence and Phillips: Completed 2021-2022. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.* with regards to *inter partes reviews* (IPRs) filed by Samsung.

Wolf Greenfield: Completed 2020-2023. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.* with regards to *inter partes reviews* (IPRs) filed by Micron.

Hueston Henningan: Completed 2020-22. Technical evaluation and consulting in the matter of *Acorn Semi, LLC v. Samsung Electronics et al.*

Skadden Arps: Initiated 2020 and on-going. Technical consulting for the *Audit Committee of the Intel Board of Directors* on matters related to Technology Development.

PARADIM: Initiated 2016 and on-going. PARADIM's mission is to create new interface materials with unprecedented properties for the next generation of electronic devices. Dr. Kuhn

is a member of the External Advisory Committee. In this role, Dr. Kuhn provides technical and management support with regards to PARADIM operations.

Quinn Emanuel Urquhart & Sullivan: Completed, 2020-2021. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Micron Technology et al.*

Susman Godfrey: Completed 202-2023. Technical evaluation and consulting with regards to *Arigna Technology Limited* on matters related to CMOS transistor design.

Womble Bond Dickinson: Completed, 2020. Technical consulting for KIPB LLC (formerly KAIST IP US LLC) on an *ex parte reexamination* (“EPR”) proceeding in the United States Patent and Trademark Office with regards to patent 6,885,055.

Womble Bond Dickinson: Completed, 2019-2020. Technical evaluation and consulting in the matter of *KIPB LLC v. Samsung Electronics et al.* Dr. Kuhn supported this litigation for the plaintiff as an expert witness, including completion of the Infringement and Rebuttal Reports, as well as completing a deposition conducted on the contents of the Infringement and Rebuttal Reports. This case was settled out of court in September 2020.

Lathrop Gage: Completed, 2018-2020. Technical evaluation and consulting for KIPB LLC (formerly KAIST IP US LLC) on Korean Patent 10-0458288 (Korean counterpart to US 6,885,055).

Ropes & Gray: Completed, 2018. Technical evaluation and consulting in the matter of *Godo Kaisha IP Bridge 1 v. Qualcomm Inc. et al.*

GlaserWeil: Completed, 2016-2018. Technical evaluation and consulting in the matter of *KAIST IP US LLC v. Samsung Electronics Co., Ltd., Case No. 2:16-cv-01314*. Dr. Kuhn supported this litigation for the plaintiff as an expert witness. This included IPR proceedings (a total of 6 IPRs were presented to the PTO in this case). This also included completion and submission of the Claim Construction Declaration, the Infringement Report, and the Rebuttal Report, as well as depositions conducted on the contents of these Reports. This case went to trial June 11-15, where Dr. Kuhn presented both Direct testimony on infringement (6/12/18) and Rebuttal (6/14/18) testimony on validity.

yoR Labs Inc.: Completed. 2015-2017. yoR Labs is a medical instrumentation start-up, focusing on non-invasive medical imaging instrumentation. Dr. Kuhn served first as a member of the External Advisory Committee and later as a member of the Board of Directors. In this role, Dr. Kuhn provided technical and management support with regards to yoR labs operations.

Oregon State University, Department of Electrical Engineering and Computer Science: Completed. 2015 to 2018: Professor-courtesy. Prof. Kuhn’s role was establishment of long-term research programs in the area advanced CMOS technology and post-CMOS technology.

FORMER ROLES (2014 and PRIOR)

Intel, Portland, OR, (advanced development / research) 2008-2014 (retired in 2014)

Grade level: 12 (Fellow)

Manager: Mike Mayberry, VP

Dr. Kuhn's role was researching advanced device architectures for Intel processes in the 5-10 year time frame. While much of her work as an Intel Fellow remains proprietary, some of the public domain aspects are captured in her book *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits* (Cambridge, 2015) and her paper "Considerations for Ultimate CMOS Scaling," (IEEE Trans. on Elec. Dev., Vol: 59, No: 7, 2012, pp. 1813 – 1828 which won the Paul Rappaport Award). She received an Intel IAA in 2008 for her work on the TriGate transistor.

Intel, Portland, OR, (45nm Device technology manager in pathfinding) 2004-2008

Grade level: 10/11 (Principal Engineer / Sr. Principal Engineer)

Manager: Mark Bohr, Senior Intel Fellow / Kaizad Mistry, VP

Dr. Kuhn's role was as device technology manager of the pathfinding team responsible for the high-k metal-gate transistor architecture for Intel's 45nm microprocessor processor technology. She received an Intel IAA in 2006 for her work on high-k metal-gate.

Intel, Portland, OR, (90nm communication process manager) 2001-2004+

Grade level: 9/10 (Sr. Engineer / Principal engineer)

Manager: Scott Thompson (was Intel Fellow at the time, now a professor at Univ. of Florida).

Dr. Kuhn's role in this time frame was Process Program Manager of the team responsible for Intel's 90nm communications process technology. Over a 4-year period, this team developed a derivative analog/RF technology (including a SiGe BJT) on top of Intel's premium 90nm microprocessor process.

Other Intel experience:

Intel, Portland, OR, (130nm front-end integration engineer) 1998-2001

Intel, Portland, OR, (0.35um front-end integration engineer) 1997-1998

Grade level: 7-9 (Sr. engineering grades)

During the 130nm generation, Dr. Kuhn was an integration engineer responsible for the isolation section of the flow. 130nm was the last of the "classic" CMOS generations, and her work in that generation was updating the isolation process. She had the satisfaction of watching the work she did in the 130nm successfully scale through 90nm, 65nm, 45nm, and 32nm, with little change in the base process.

Dr. Kuhn joined Intel on the 0.35um generation as a sustaining integration engineer in F15. She was responsible for the silicide section of the flow. Additionally, she participated in the DIVD camera chip project (Intel's historical project to build CMOS camera chips).

Other relevant experience:

Univ. of Washington, Seattle, WA (Assoc. Prof., Ass't. Prof., Res. Ass't. Prof.), 1987-1997

Dr. Kuhn held faculty positions at the University of Washington (in Seattle) for roughly a decade in the order of Research Assistant Professor (Materials Science and Engineering), Assistant Professor (Electrical and Computer Engineering), and Associate Professor (Electrical and Computer Engineering). She left the University in 1997 as a tenured Associate Professor of Electrical and Computer Engineering. While at the Univ. of Washington, she achieved distinction in both research and teaching.

Highlights include:

- University of Washington, Distinguished Teaching Award, 1995 (UW's highest level of achievement for a faculty member)
- NSF Presidential Young Investigator award, 1991-6 (The National Science foundation is the most prestigious funding agency for faculty and the NSF PYI award is the most prestigious national level award for junior faculty).
- Single-author on a textbook, Laser Engineering, Prentice-Hall, 1998, ISBN 0-02-366921-7 (this is a mezzanine text discussing the theory and practice of building conventional and diode laser systems).

BOOKS

Laser Engineering, (sole author) Prentice-Hall, 1998, ISBN 0-02-366921-7

CMOS and Beyond: Logic Switches for Terascale Integrated Circuits (Co-editor with Prof. Tsu-Jae King Liu, Cambridge Press, 2015, ISBN 978-1107043183).

BOOK CHAPTERS

“The Magic of MOSFET Manufacturing,” Chapter in the 75th Anniversary of the Transistor, Wiley-IEEE Press, July 2023, ISBN: 978-1-394-20247-8.

Chapter 1, CMOS and Beyond CMOS: Scaling Challenges” (Book title: “High Mobility Materials for CMOS Applications”, Woodhead Publishing Series in Electronic and Optical Materials, Elsevier, June 2018, ISBN 9780081020616) .

AWARDS:

Elected to the National Academy of Engineering (2023)
IEEE Frederik Philips Award (2016)
IEEE Paul Rappaport Award (2013)
IEEE Fellow (2011)

Intel Achievement Awards (Intel's highest technical award): IAA 2006 (for HiK-MG) and IAA 2008 (for key contributions to Intel's 22nm TriGate technology)

Intel Divisional Awards: Turbo operation (2009), RF Vccmin (2007), TCC (2005), SCD 1213.4 SCD/ICG (2004), LAD NW/Ophir A-1 (2003), SiGe BJT (2002), Hitachi etch (2002), 2um2SRAM (2001), Gamma Test chip (2000), Certification P854.6 (1999), F15 ISO 9000 (1998)

Academic Engineer of the Year Award, Puget Sound Engineering Council, 1996

University of Washington, Distinguished Teaching Award, 1995

College of Engineering, Outstanding Faculty Achievement Award, 1994

NSF Presidential Young Investigator award, 1991-6

NSF Research Initiation Award, 1989-91

IBM Graduate Fellowship, 1983-5

Hertz Graduate Fellowship, 1982-3

National Merit Scholar, 1976-80

JOURNAL PUBLICATIONS:

49. "First principles modeling of defects in the $\text{Al}_2\text{O}_3/\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ system", G. Greene-Diniz, K. Kuhn, P. Hurley, and J. Greer, J. Appl. Phys., Vol. 121, No. 7, Jan. 2017.

48. "Doping top-down e-beam fabricated germanium nanowires using molecular monolayers," B. Long, G. Alessio Verni, J. O'Connell, M. Shayesteh, A. Gangnaik, Y.M. Georgiev, P. Carolan, D. O'Connell, K.J. Kuhn, S.B. Clendenning, R. Nagle, R. Duffy, and J.D. Holmes, Materials Science in Semiconductor Processing, Vol. 62, May 2017, pp. 196-200.

47. "Device Physics Modeling of Surfaces and Interfaces from an Induced Gap State Perspective," J. Wager and K. Kuhn, Critical Reviews in Solid State and Materials Science, Oct. 4, 2016.

46. "Adhesion Limits and Design Criteria for Nanorelays", Kevin L. Lin, Graham L. W. Cross, Peter Gleeson, Johann P. de Silva, Alejandro Levander, Jorge A. Muñoz, Chytra Pawashe, Alexis Potie, Patrick Theofanis, John J. Boland, and Dr. Kuhn J. Kuhn, IEEE Trans. on Elec. Dev., Vol. 63, No. 1, Jan. 2016, 465-470.

45. Distributive Quasi-Ballistic Drift Diffusion Model Including Effects of Stress and High Driving Field, Roza Kotlyar,, Rafael Rios, Cory E. Weber, Thomas D. Linton, Mark Armstrong and Dr. Kuhn Kuhn, IEEE Trans. on Elec. Dev., Vol. 62, No. 3, March 2015. Pp. 743-750.

44. Improved MOSFET characterization technique for single channel length, scaled transistors, Ferdousi, F., Rios, R., Kuhn K.J. Solid State Electronics, Vol. 104, pp. 44-6, Feb. 2015

43. Capacitance and Conductance for an MOS System in Inversion, with Oxide Capacitance and Minority Carrier Lifetime Extractions, Monaghan, S. O'Connor, E., Rios, R., Ferdousi, F., Floyd, L., Ryan, E., Cherhaoui, K., Povey, I.M., Kuhn, K.J., Hurley, P.K. IEEE Transactions on Electron Devices, Vol. 61, No. 12, pp. 4176-85, Dec. 2014.

42. First principle-based analysis of single-walled carbon nanotube and silicon nanowire Junctionless transistors, Ansari, L., Feldman, B., Faga, G., Martinez, L.C., Haverty, M.G., Kuhn, K.J., Shankar, S., Greer, J.C., IEEE Transactions on Nanotechnology, Vol. 12, No. 6, pp. 1075-81, Nov. 2013.
41. Scaling Limits of Electrostatic Nanorelays, Pawashe, C., Lin, K., Kuhn, K.J., IEEE Transactions on Electron Devices, Vol. 60, No. 9, pp. 2936-42, Sept. 2013,
40. Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors, Kotlyar, R.; Avci, U.E.; Cea, S.; Rios, R.; Linton, T.D.; Kuhn, K.J.; Young, I.A., Applied Physics Letters, v 102, n 11, March 18, 2013.
39. Effects of alternating current voltage amplitude and oxide capacitance on mid-gap interface state defect density extractions in InGaAs capacitors, Monaghan, Scott ; O'Connor, Eamon ; Povey, Ian M. ; Sheehan, Brendan J. ; Cherkaoui, Karim ; Hutchinson, Barry J. A. ; Hurley, Paul K. ; Ferdousi, Fahmida ; Rios, Rafael ; Kuhn, Dr. Kuhn J. ; Rahman, Anisur, Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, Vol: 31 , No: 1, 2013, pp: 01A119 - 01A119-8.
38. Considerations for Ultimate CMOS Scaling, Dr. Kuhn J. Kuhn, invited review paper, IEEE Trans. on Elec. Dev., Vol: 59 , No: 7, 2012 , pp. 1813 – 1828 (won the Paul Rappaport Award)
37. Does the low hole transport mass in <110> and <111> Si nanowires lead to mobility enhancements at high field and stress: a self-consistent tight-binding study, R. Kotlyar, T. D. Linton, R. Rios, M. D. Giles, S. M. Cea, K. J. Kuhn, Michael Povolotskyi, Tillmann Kubis, and Gerhard Klimeck, Vol: 111 , No: 12, 2012, pp 123718 - 123718-11
36. Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm, Rios, R.; Cappellani, A.; Armstrong, M.; Budrevich, A.; Gomez, H.; Pai, R.; Rahhal-orabi, N.; Kuhn, K., IEEE Electron Device Letters, Vol. 32, No. 9, 2011, pp. 1170 - 1172
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11. Effect of etch treatment prior to Schottky contact fabrication on In/sub 0.05/Ga/sub 0.95/As. Johnson, M.J.; Kuhn, K.J.; Darling, R.B. Applied Physics Letters, vol.58, no.17, 29 April 1991. p. 1893-5
10. An enhanced and linear Stark shift in n-i-n AlGaAs/GaAs symmetric and asymmetric coupled quantum wells. Kuhn, K.J.; Cheng Juang; Darling, R.B. Journal of Applied Physics, vol.69, no.5, 1 March 1991. p. 3135-41
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1. Implementation of Distributed Microprocessor Systems in Custom Heavy Trucks, K.J. Kuhn, 1979-80 IEEE Student Papers, Vol. TT0114 IEEE, pg. 334-342.

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53. Semiconductors Stand Aside, the Age of Metals is Here! K. Kuhn, A. Sanchez, C. George, R. Rios, J. Clarke, J. Greer, Lester Eastman Conference, Cornell, May 2014.
52. The ultimate CMOS device and beyond, Kuhn, K.J. ; Avci, U. ; Cappellani, A. ; Giles, M.D. ; Haverty, M. ; Seiyon Kim ; Kotlyar, R. ; Manipatruni, S. ; Nikonov, D. ; Pawashe, C. ; Radosavljevic, M. ; Rios, R. ; Shankar, S. ; Vedula, R. ; Chau, R. ; Young, I. 2012 IEEE International Electron Devices Meeting (IEDM), pp. 171-174.
51. Understanding the feasibility of scaled III-V TFET for logic by bridging atomistic simulations and experimental results, Avci, U.E. ; Hasan, S. ; Nikonov, D.E. ; Rios, R. ; Kuhn, K. ; Young, I.A., Symposium on VLSI Technology (VLSIT), 2012, pp: 183 – 184.
50. Beyond the Planar Transistor: Progress in Next Generation Switches, K. Kuhn, Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

49. Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation, K. Kuhn, INFOS 2011 (June 22, 2011, France)
48. Comparison of power and performance for the TFET and MOSFET and considerations for P-TFET, Avci, U.E.; Rios, R.; Kuhn, K.J.; Young, I.A., IEEE Conference on Nanotechnology (IEEE-NANO), 2011 11th, pp. 869 – 872
47. Comparison of performance, switching energy and process variations for the TFET and MOSFET in logic, Avci, U.E.; Rios, R.; Kuhn, K.; Young, I.A., 2011 Symposium on VLSI Technology (VLSIT), 2011 , pp. 124 – 125
46. CMOS scaling for the 22nm node and beyond: Device physics and technology, Kuhn, K.J., 2011 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 2011 , pp. 1 – 2
45. Past, Present and Future: SiGe and CMOS Transistor Scaling. K. J. Kuhn, A. Murthy, R. Kotlyar, and M. Kuhn, ECS 2010, Oct. 10, Las Vegas, CA, USA.
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PATENTS

	PAT. NO.	Title
1	11,302,777	Integration methods to fabricate internal spacers for nanowire devices
2	11,195,919	Method of fabricating a semiconductor device with strained SiGe fins and a Si cladding layer
3	11,139,400	Non-planar semiconductor device having hybrid geometry-based active region
4	11,024,714	Nanowire transistor fabrication with hardmask layers
5	10,991,799	Silicon and silicon germanium nanowire structures
6	10,825,752	Integrated thermoelectric cooling
7	10,804,357	Integration methods to fabricate internal spacers for nanowire devices
8	10,636,871	Silicon and silicon germanium nanowire structures
9	10,593,804	Non-planar semiconductor device having hybrid geometry-based active region
10	10,586,868	Non-planar semiconductor device having hybrid geometry-based active region
11	10,580,899	Nanowire structures having non-discrete source and drain regions
12	10,580,860	Integration methods to fabricate internal spacers for nanowire devices
13	10,535,770	Scaled TFET transistor formed using nanowire with surface termination
14	10,424,580	Semiconductor devices having modulated nanowire counts
15	10,283,589	Integration methods to fabricate internal spacers for nanowire devices
16	10,121,861	Nanowire transistor fabrication with hardmask layers
17	10,121,856	Integration methods to fabricate internal spacers for nanowire devices
18	10,115,822	Methods of forming low band gap source and drain structures in microelectronic devices
19	10,109,711	CMOS FinFET device having strained SiGe fins and a strained Si cladding layer on the NMOS channel
20	10,074,573	CMOS nanowire structure
21	10,074,357	Integrated acoustic phase array
22	10,026,829	Semiconductor device with isolated body portion
23	9,978,636	Isolated and bulk semiconductor devices formed on a same bulk substrate
24	9,947,805	Nanowire-based mechanical switching device
25	9,935,205	Internal spacers for nanowire transistors and method of fabrication thereof
26	9,935,107	CMOS FinFET device with dual strained cladding layers on relaxed SiGe fins, and method of fabricating the same
27	9,926,193	Magnetic nanomechanical devices for stiction compensation

28	9,911,835	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
29	9,893,167	Integration methods to fabricate internal spacers for nanowire devices
30	9,882,053	Molded dielectric fin-based nanostructure
31	9,859,368	Integration methods to fabricate internal spacers for nanowire devices
32	9,825,130	Leakage reduction structures for nanowire transistors
33	9,812,524	Nanowire transistor devices and forming techniques
34	9,691,843	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
35	9,680,013	Non-planar device having uniaxially strained semiconductor body and method of making same
36	9,673,302	Conversion of strain-inducing buffer to electrical insulator
37	9,614,060	Nanowire transistor with underlayer etch stops
38	9,608,059	Semiconductor device with isolated body portion
39	9,595,581	Silicon and silicon germanium nanowire structures
40	9,583,602	Tunneling field effect transistors (TFETs) for CMOS architectures and approaches to fabricating N-type and P-type TFETs
41	9,583,491	CMOS nanowire structure
42	9,564,522	Nanowire structures having non-discrete source and drain regions
43	9,559,160	Common-substrate semiconductor devices having nanowires or semiconductor bodies with differing material orientation or composition
44	9,508,796	Internal spacers for nanowire transistors and method of fabrication thereof
45	9,484,447	Integration methods to fabricate internal spacers for nanowire devices
46	9,472,613	Conversion of strain-inducing buffer to electrical insulator
47	9,425,212	Isolated and bulk semiconductor devices formed on a same bulk substrate
48	9,412,872	N-type and P-type tunneling field effect transistors (TFETs)
49	9,385,221	Nanowire transistor with underlayer etch stops
50	9,362,074	Nanowire-based mechanical switching device
51	9,355,242	Method and apparatus for managing and accessing personal data
52	9,343,559	Nanowire transistor devices and forming techniques
53	9,287,576	Self-powered internal medical device
54	9,258,114	Quantum key distribution (QSD) scheme using photonic integrated circuit (PIC)
55	9,224,810	CMOS nanowire structure
56	9,183,829	Integrated acoustic phase array

57	9,129,829	Silicon and silicon germanium nanowire structures
58	9,129,827	Conversion of strain-inducing buffer to electrical insulator
59	9,105,344	Shut-off mechanism in an integrated circuit device
60	9,087,863	Nanowire structures having non-discrete source and drain regions
61	9,064,944	Nanowire transistor with underlayer etch stops
62	9,029,221	Semiconductor devices having three-dimensional bodies with modulated heights
63	9,012,284	Nanowire transistor devices and forming techniques
64	8,890,120	Tunneling field effect transistors (TFETs) for CMOS approaches to fabricating N-type and P-type TFETs
65	8,853,741	Junctionless accumulation-mode devices on decoupled prominent architectures
66	8,766,372	Copper-filled trench contact for transistor performance improvement
67	8,753,942	Silicon and silicon germanium nanowire structures
68	8,558,279	Non-planar device having uniaxially strained semiconductor body and method of making same
69	8,507,948	Junctionless accumulation-mode devices on prominent architectures, and methods of making same
70	8,487,348	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
71	8,269,283	Methods and apparatus to reduce layout based strain variations in non-planar transistor structures
72	8,258,057	Copper-filled trench contact for transistor performance improvement
73	7,999,607	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
74	7,888,710	CMOS fabrication process utilizing special transistor orientation
75	7,737,770	Power switches having positive-channel high dielectric constant insulated gate field effect transistors
76	7,312,485	CMOS fabrication process utilizing special transistor orientation
77	6,627,506	Thin tensile layers in shallow trench isolation and method of making same
78	6,368,931	Thin tensile layers in shallow trench isolation and method of making same
79	4,617,669	Method and apparatus for pumping laser slabs
80	4,563,763	Method and apparatus for cooling a slab laser

INVITED TECHNICAL PRESENTATIONS/SEMINARS :

Invited panel, IEDM, Variation and the End of the World, December, 2013.

Keynote, The End of Scaling?, ICTC, December 2013.

Invited seminar, CMOS and Beyond, Portland State University, October, 2013.

Keynote panel, CMOS and Beyond: Future Device Technology, ENF 2013, Ireland, June 2013.

Invited seminar, CMOS and Beyond: Future Device Technology for the Mobile World, IDF, May 2013.

Invited Workshop, The Future is Already Here: Evolving Concepts in Device and Materials Technology, AMAT, March 2013.

Invited paper, "The Ultimate CMOS Device and Beyond," IEDM 2012, San Francisco.

Invited talk, Beyond Simply Small: Progress in Advanced Transistor Architectures, Cornell, November 2012.

Invited seminar, Demystifying Moore's Law How it Really Works!, IDF, Sept. 2012, San Francisco.

Invited talk, The Ultimate CMOS Device and Beyond, Ireland, April 2012.

Keynote: "MOS scaling for the 22nm node and beyond: Device physics and technology," April 24, 2011, Taiwan, VLSI-TSA

Plenary: "Moore's Crystal Ball: Device Physics and Technology Past the 15nm Generation," INFOS 2011 (June 22, 2011, France)

Keynote: "Beyond the Planar Transistor: Progress in Next Generation Switches," Int'l Symposium on Adv. Gate. Stack Technology, Oct. 19-21, 2011 New York

Invited seminar - "Polishing Moore's Crystal Ball: Advanced Transistor Architectures ...and Beyond," K. Kuhn, March 30th. 2011, MIT, MTL seminar series.

Invited seminar - "Emerging Devices: Moore's Law and Advanced Transistor Architectures," K. Kuhn, Varian Technology Symposium, March 31st. 2011.

Keynote: "Scaling Electronics:Trends and Bottlenecks," K. Kuhn, April 4th. 2011, MIT Microphotonics meeting.

Invited seminar - "Gazing into Moore's Crystal Ball: Transistor Scaling after the 15nm node," K. Kuhn, Feb. 17th, 2010, Berkeley.

IEDM 2010 Short Course chair for 15nm technology, December 2010.

Plenary: Past, Present and Future: SiGe and CMOS Transistor Scaling, ECS 2010, Oct. 10, Las Vegas, CA, USA.

Keynote: Peering into Moore's Crystal Ball, Transistor Scaling beyond the 15nm node, Int'l Symposium on Adv. Gate. Stack Technology, Sept. 29th, 2010; Albany, NY, USA.

Plenary: CMOS transistor scaling past 32nm and implications on variation, 2010 IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC), ASMC'2010, 11-13 July 2010, San Francisco, CA, USA

Keynote: Technology options for 22nm and beyond, K. Kuhn, 2010 International Workshop on Junction Technology (IWJT), IWJT'10, 10-11 May 2010, Shanghai, China, pp. 1-6.

Invited seminar: Next Steps in Moore's Law: Transistor Scaling for the 15nm node and beyond, Nikkei Electronics Symposium / June 29th, 2010.

Plenary - CMOS technology beyond 22nm, K. Kuhn, 12th IEEE International Workshop on Cellular Nanoscale Networks and Applications, CNNA 2010, February 3-5 Berkeley, California

Keynote - Transistor architecture: 45nm and beyond, K. Kuhn, Intel European Research and Innovation Conference, 8-10th September 2009, Leixlip, Co. Kildare.

Plenary - Moore's Law Past 32nm: The Challenges in Physics and Technology Scaling, K. Kuhn, Solid State Devices and Materials Conference (SSDM), September 18, 2009, Sendai, Japan.

Invited talk - CMOS scaling beyond 32 nm: challenges and opportunities, Kuhn, K.J., 2009 46th ACM/IEEE Design Automation Conference (DAC), 26-31 July 2009, San Francisco, CA, USA, Pages: 310-13 Published: 2009

Keynote - Variation in 45nm and Implications for 32nm and Beyond, K. Kuhn, NMI International Conference on CMOS Variability, 12th & 13th May 2009, London, UK.

Invited talk - Moore's law past 32 nm: future challenges in device scaling, Kuhn, K.J., 2009 13th International Workshop on Computational Electronics (IWCE 2009), 27-29 May 2009, Beijing, China, (IWCE 2009) Pages: 6 pp. Published: 2009

Invited – International Electron Device meeting – short course.
http://download.intel.com/pressroom/pdf/kkuhn/Kuhn_22nm_Device.pdf

Invited seminar - “45nm High-k + Metal Gate Logic Technology,” K. Kuhn, May 2008, MIT, MTL laboratory.

Invited talk - Reducing variation in advanced logic technologies: approaches to process and design for manufacturability of nanoscale CMOS, Kuhn, K.J., 2007 IEEE International Electron Devices Meeting - IEDM '07, 10-12 December 2007, Washington, DC, USA, IEDM '07 Pages: 471-4

Invited seminar - "CMOS Transistor Architecture Challenges and Opportunities," K. Kuhn, September 2005, MIT, MTL laboratory.

Keynote - "Nanotechnology Challenges and Opportunities," K. Kuhn, January 2005, MIT, MTL laboratory.

Invited seminar - "Transistor Scaling and its Impact on Analog/RF Device Performance", Dr. Kuhn Kuhn, March 2005, Stanford University, invited seminar.

Invited seminar - "Advanced transistor architecture approaches and their implications for device and circuit performance," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2004.

Invited seminar - "Moore's Law meets Materials Science", Dr. Kuhn Kuhn, September 2004, University of Washington.

Invited seminar - "Centrino, convergence of computing and communications," November 2003, Dr. Kuhn Kuhn, Stanford University, invited seminar.

Invited seminar - "Challenges in the parallel development of the 90nm communications (121x) and microprocessor (1262) process technologies," Dr. Kuhn Kuhn, Intel Fellow's Forum, October 2003.

Invited seminar - "RF/analog integration with 90nm digital CMOS", Dr. Kuhn Kuhn, MIT invited seminar, March 2003

Invited seminar - "Femtosecond pulse laser technology", Dr. Kuhn Kuhn, Oregon State University, March 10, 1997.

Invited talk- "Symbolic Solvers and their impact on engineering education", Dr. Kuhn Kuhn, Fifth annual conference on the teaching of mathematics, Baltimore, Maryland, June 21, 1996.