

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner

v.

MICRON TECHNOLOGY, INC.

Patent Owner

IPR2025-00500

U.S. PATENT 10,475,737

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 10,475,737

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EX1013	“Solid” – Merriam-Webster Online Dictionary 2010, Retrieved February 20, 2010, from https://web.archive.org/web/20100218235823/http://www.merriam-webster.com/dictionary/solid
EX1014	Bill Arnold, “Shrinking Possibilities,” IEEE Spectrum, vol. 46, no. 4, April 2009, pp. 26-28, 50-56
EX1015	U.S. Patent Application Publication No. 2007/0066004 in the Name of Nakagawa
EX1016	Y. Fukuzumi <i>et al.</i> , “Optimal Integration and Characteristics of Vertical Array Devices for Ultra-High Density, Bit-Cost Scalable Flash Memory,” Proceedings of the 2007 IEEE International Electron Devices Meeting, Washington, DC, USA, December 10-12, 2007, pp. 449–452
EX1017	S. Bangsaruntip <i>et al.</i> , “Universality of Short-Channel Effects in Undoped-Body Silicon Nanowire MOSFETs,” IEEE Electron Device

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	Letters, vol. 31, no. 9, Sept. 2010, pp. 903-905
EX1018	U.S. Patent Application Publication No. 2010/0327252 in the Name of Lee
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EX1020	J. Jang <i>et al.</i> , “Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193
EX1021	K. Joo <i>et al.</i> , “Novel Transition Layer Engineered Si Nanocrystal Flash Memory with MHSOS Structure Featuring Large V_{th} Window and Fast P/E Speed,” IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest., Washington, DC, USA, 2005, pp. 865-868
EX1022	S. Park <i>et al.</i> , “A New Operating Scheme by Switching the Polarity of Program/Erase Bias for Partially Oxidized Amorphous-Si-Based Charge-Trap Memory,” IEEE Transactions on Electron Devices, vol. 53, no. 11, Nov. 2006, pp. 2847-2849
EX1023	M. Rosmeulen <i>et al.</i> , “Silicon Rich Oxides as an Alternative Charge Trapping Medium in Fowler-Nordheim and Hot Carrier Type Non-Volatile-Memory Cells,” Digest. International Electron Devices Meeting, San Francisco, CA, USA, 2002, pp. 189-192
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Exhibit	Description
	(N.D. Cal. January 29, 2025)

All emphases in quotations are added unless otherwise noted.

Direct quotations of claim language are italicized.

This paper includes color illustrations and should be viewed in color.

I. INTRODUCTION

Yangtze Memory Technologies Company, Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1-12, 14, 15, 18, and 20-22 (“challenged claims”) of U.S. Patent No. 10,475,737 (“’737 patent,” EX1001) assigned to Micron Technology, Inc. (“PO”).

The challenged claims recite stack structures in three-dimensional (3D) NAND memory devices, which had been well-known in the semiconductor industry prior to the earliest possible priority date of the ’737 patent. For instance, the components of the claimed stack structures, including the horizontally extending and vertically overlapping “*gate lines*,” as well as the “*operative structures*,” “*dummy structures*,” and “*contacts*” that extend vertically through the “*gate lines*” in different regions of the stack structures, are clearly and extensively disclosed in each of U.S. Patent Application Publication No. 2010/0133598 in the name of Chae *et al.* (“Chae,” EX1004), U.S. Patent Application Publication No. 2011/0156132 in the name of Kiyotoshi *et al.* (“Kiyotoshi,” EX1005), U.S. Patent Application Publication No. 2017/0352674 in the name of Jeong *et al.* (“Jeong,” EX1006), and U.S. Patent Application Publication No. 2011/0151667 in the name of Hwang *et al.* (“Hwang,” EX1007). The additional claim limitations merely represent minor design variations or industry-standard practices, all of which were known or obvious, as demonstrated by the cited prior art references.

Petitioner's expert, Dr. Kelin Kuhn, a semiconductor industry veteran with four decades of experience, confirms that the challenged claims are unpatentable over these references, as well as others predating the '737 patent.

Petitioner thus respectfully requests the Board cancel the challenged claims.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest

The real parties-in-interest are Yangtze Memory Technologies Company, Ltd. and Yangtze Memory Technologies, Inc.

B. Related Matters

The '737 patent is not currently asserted in any pending civil action. In *Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. et al.*, No. 3:23-cv-05792-RFL (N.D. Cal.) ("NDCA case"), however, PO has filed an unopposed motion for leave to amend its counterclaims to assert the '737 patent in the NDCA case.¹ That motion remains pending.

Petitioner filed an IPR (Case IPR2025-00098, "'098 IPR") on November 18, 2024, against U.S. Patent No. 8,945,996 ("'996 patent," EX1011), which is the earliest parent patent of the '737 patent and asserted in the NDCA case. The '098

¹ The '737 patent was initially included in PO's February 16, 2024 Answer and Counterclaim, but the Court dismissed it under FRCP 12(b)(6), with leave to amend. EX1024-EX1025. Rather than amending the pleadings, PO chose to drop the '737 patent on August 1, 2024. EX1026. Months later, PO now seeks to reassert the '737 patent. EX1027.

IPR is currently pending institution decision.

C. Lead and Back-up Counsel and Service Information

Petitioner identifies the following lead and back-up counsels:

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Petitioner consents to electronic service at YMTC-Micron-IPR@bayes.law,
as well as the above email addresses.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that the '737 patent is available for IPR, and Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified in this Petition.

IV. RELIEF REQUESTED

Under 35 U.S.C. § 311, Petitioner requests IPR of claims 1-12, 14, 15, 18, and 20-22 of the '737 patent.

A. Claims for Which Review Is Requested

Petitioner requests IPR and cancellation of challenged claims 1-12, 14, 15, 18, and 20-22 of the '737 patent under 35 U.S.C. § 311 based on the following grounds. This Petition is supported by the Declaration of Dr. Keln Kuhn ("Kuhn Decl.," EX1003).

B. Statutory Grounds of Challenge

1. Claims 1-12, 14, 15, 21, and 22

Petitioner relies on the following prior art and statutory grounds of challenge to claims 1-12, 14, 15, 21, and 22 of the '737 patent:

Name	Ex.	Publication No.	Filed	Published	Prior art under at least
Chae	1004	US2010/0133598	12/3/2009	6/3/2010	§§ 102(a) & (e)
Kiyotoshi	1005	US2011/0156132	5/20/2010	6/30/2011	§ 102(e)

Ground	Claims	Basis	References
1 & 2	1-12, 14, 15, 21, and 22	§§ 102/103	Chae
3	5-8, 10-12, 14, and 15	§ 103	Chae in view of Kiyotoshi

Each of Chae and Kiyotoshi was filed before the earliest possible priority date of the '737 patent, April 12, 2011, and therefore qualifies as prior art under pre-AIA 35 U.S.C. § 102(e). Chae also qualifies as prior art under pre-AIA 35 U.S.C. § 102(a) as it was published before April 12, 2011.

2. Claims 18 and 20

Petitioner relies on the following additional prior art and statutory grounds of

challenge to claims 18 and 20 of the '737 patent:

Name	Ex.	Publication No.	Filed	Published	Prior art under at least
Jeong	1006	US2017/0352674	8/23/2017	12/7/2017	§ 102(a)(1)
Hwang	1007	US2011/0151667	12/8/2010	6/23/2011	§ 102(a)(1)

Ground	Claims	Basis	References
4 & 5	18 and 20	§§102/103	Jeong
6	18 and 20	§103	Chae in view of Hwang

Petitioner demonstrates in Section V.D that claims 18 and 20 of the '737 patent are not entitled to any priority date earlier than its actual filing date of February 20, 2018. Accordingly, the '737 patent will be subject to the first inventor to file provisions of the AIA. Thus, both Jeong and Hwang, published before February 20, 2018, qualify as prior art under at least AIA 35 U.S.C. § 102(a)(1) against claims 18 and 20.

Hwang still qualifies as prior art under pre-AIA 35 U.S.C. § 102(e), even if the Board finds that claims 18 and 20 of the '737 patent are entitled to the April 12, 2011 priority date, as the filing date of Hwang predates April 12, 2011.

In addition, under the AIA provisions, Chae would qualify as prior art against all the challenged claims, including claims 18 and 20, under at least AIA 35 U.S.C. § 102(a)(1) as it was published before April 12, 2011, and Kiyotoshi would qualify as prior art under at least AIA 35 U.S.C. § 102(a)(2) as it names another inventor and was effectively filed before April 12, 2011.

Petitioner emphasizes that the analysis of the proposed grounds for unpatentability remains unchanged, regardless of whether evaluated under the pre-AIA or AIA statutes.

V. THE '737 PATENT

A. Overview

The '737 patent describes stacks of horizontally extending and vertically overlapping features, and methods of forming circuitry components and an array of memory cells. EX1001, 1:36-39. During the process of forming the stacks, the features in the end portion of the stack “may be sagged, bent, or broken due to lack of support” when the sacrificial material between the features is removed. EX1001, 7:58-64. The '737 patent purportedly solves this problem by forming “dummy structures” vertically through the features in the end portion to support the features from vertical movement. EX1001, 7:52-58, 7:64-8:2.

FIG. 13 of the '737 patent (annotated in Kuhn Decl. as FIG. C below) shows a stack of vertically overlapping materials 40 that extend horizontally across a primary portion 18 and an end portion 20 of the stack in a substrate fragment 10. EX1003, ¶61. End portion 20 has a “stair step-like construction” where materials 40 extend farther in the horizontal direction, moving deeper into the stack. EX1001, 4:57-59; 5:1-7. Material 40 includes a horizontal extending conductive line 42 (in red), which is a “feature” according to the '737 patent. EX1001, 8:31-39, 11:28-31,

FIGs. 11 and 11A; EX1003, ¶62. Operative structures 31 (in green) and dummy structures 32 (in yellow) are formed vertically through conductive lines 42 of materials 40 in primary portion 18 and end portion 20, respectively. EX1001, 8:17-20; EX1003, ¶63. Contacts 60 (in black) in end portion 20 are connected to conductive lines 42 of materials 40, respectively. EX1001, 8:45-48, 51-56.

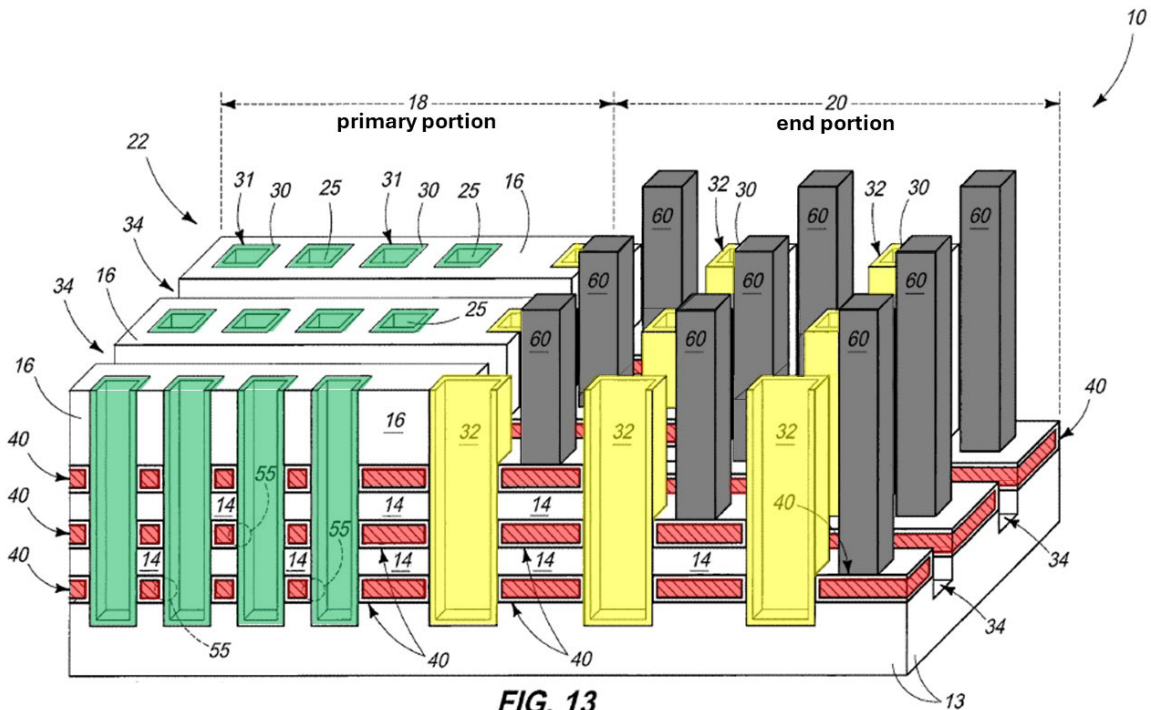


FIG. 13
EX1003 — FIG. C

The '737 patent discloses that the operative structure may be “circuit components,” and the dummy structure is “a structure which is used to mimic a physical property of another structure (*e.g.*, load carrying ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (*e.g.*, is not part of a current flow path of a circuit even if conductive).” EX1001, 6:22-32.

B. Prosecution History

In the first Office Action on the merits, the Examiner rejected issued claims 1-17 of the '737 patent on the ground of nonstatutory double patenting over U.S. Patent No. 9,929,175 (“’175 patent,” EX1008)² but allowed issued claims 18-22, noting that the prior art on the record did not teach the claim limitations related to “*vertical contacts*.” EX1002, 38-49. In response, PO filed a terminal disclaimer against the ’175 patent without presenting arguments on the merits. EX1002, 35. The Examiner subsequently issued the Notice of Allowance. EX1002, 9.

C. The Level of Ordinary Skill in the Art

A person of ordinary skill in the art (POSITA) at the time of the claimed invention would have had a Bachelor’s degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. EX1003, ¶32. A higher level of education might make up for less experience, and vice versa. EX1003, ¶32.

D. The Priority Date of Claims 18 and 20

The ’737 patent is a continuation of the ’175 patent, filed on January 4, 2017, which is a continuation of U.S. Patent No. 9,564,471 (“’471 patent,” EX1009), filed on April 11, 2016, which is a divisional of U.S. Patent No. 9,318,430 (“’430 patent,”

² Issued claim 12 was rejected over the parent ’175 patent in view of U.S. Patent Application Publication No. 2010/0244119 in the name of Fukuzumi *et al.* (“Fukuzumi”).

EX1010), filed on January 22, 2015, which is a divisional of the '996 patent, filed on April 12, 2011. To obtain priority benefit of an earlier-filed application, the claims must meet the written description requirement of 35 U.S.C. §112. 35 U.S.C. §§ 112 and 120³.

Claims 18 and 20 of the '737 patent are not entitled to priority benefit of any of the '175 patent, '471 patent, '430 patent, and '996 patent (collectively “parent patents”) because none of the parent patents provides written disclosure support for at least the limitations of “*the **contacts** and dummy structures having different horizontal cross-sections relative one another*” in independent claim 18 and that “*different horizontal cross-sections have different values of total horizontal area relative one another*” in dependent claim 20.

The specifications of the parent patents do not describe the horizontal cross-section of **contacts** at all, let alone provide any comparison with the horizontal cross-section of dummy structures. The only mention of any “cross-section” or “cross section” in the specifications pertains to openings 25 and 27, in which **operative structures** 31 and dummy structures 32 are formed, respectively. EX1008, 5:53-58, 6:45-49; EX1009, 5:45-50, 6:37-41; EX1010, 5:39-44, 6:30-35; EX1011, 5:27-32,

³ It is PO's burden to establish that the claims are entitled to the priority date of the earlier-filed applications. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1379–80 (Fed. Cir. 2015).

6:18-23. At best, the specifications disclose that the cross-sections of openings 25 and 27 (**operative structures 31** and dummy structures 32) may differ. EX1008, 5:55-58; EX1009, 5:47-50; EX1010, 5:42-44; EX1011, 5:30-32. However, openings 25 (operative structures 31) do not correspond to the claimed “*contacts*” (e.g., contacts 60), and the horizontal cross-section of openings 25 (operative structures 31) is not even associated with the horizontal cross-section of the contacts. EX1003, ¶71. As such, the parent patents fail to satisfy the written description requirement, as they do not convey with reasonable clarity to a POSITA that the inventor was in possession of the claimed subject matters pertinent to the horizontal cross-section of contacts. *Vas-Cath Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64 (Fed. Cir. 1991).

Should PO argue that FIG. 13 of the parent patents illustrates the horizontal cross-sections of dummy structures 32 and contacts 60, it is important to note that the parent patents clearly indicate that contacts 60 are “**diagrammatically** shown in FIG. 13.” EX1008, 8:42-46; EX1009, 8:34-38; EX1010, 8:22-26; EX1011, 8:10-14. Since the parent patents do not disclose that FIG. 13 is to scale and are silent as to the dimensions or shapes, FIG. 13 cannot establish that the inventor was in possession of the claim limitation pertaining to the horizontal cross-sections of contacts and dummy structures. *Hockerson-Halberstadt, Inc. v. Avia Group Int’l*, 222 F.3d 951, 956 (Fed. Cir. 2000). Furthermore, as the schematic illustration of

FIG. 13 does not depict a **complete** horizontal cross-section of any dummy structure 32, a POSITA would not be able to compare the horizontal cross-sections of dummy structures 32 and contacts 60 based on FIG. 13. EX1003, ¶72.

Further, any argument of written description support based on obviousness must fail as a matter of law because entitlement to a filing date does not extend to subject matter that is not disclosed but would be obvious over what is expressly disclosed. *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1306 (Fed. Cir. 2008).

Claims 18 and 20 of the '737 patent, therefore, cannot claim priority to any parent patent because the subject matters of claims 18 and 20 were not disclosed in the manner required by pre-AIA 35 U.S.C. §112, ¶1 or AIA 35 U.S.C §112(a) in any parent patent.

VI. CLAIM CONSTRUCTIONS

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). The only term needing construction is “*dummy structure*,” which the parties agreed in the NDCA case⁴ to

⁴ The same term “*dummy structure*” is recited in claims 1, 2, 11, and 12 of the parent '996 patent asserted in the NDCA case.

mean “electrically inoperable structure that mimics a physical property of an operative structure.” EX1012, 2; *see* EX1001, 6:27-32. For all other limitations, because the prior art asserted herein discloses embodiments indisputably within the claims’ scope, the Board need not construe the claims’ outer bounds, and all other claim terms should be construed according to their plain and ordinary meaning.

VII. GROUNDS 1 AND 2: CHAE ANTICIPATES OR OTHERWISE RENDERS OBVIOUS CLAIMS 1-12, 14, 15, 21, AND 22

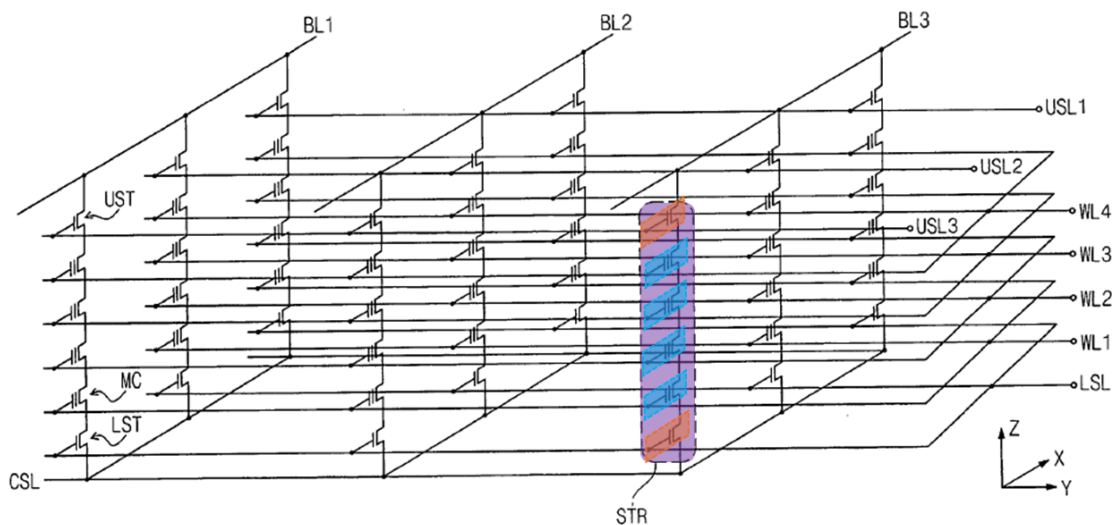
A. Overview of Chae

Chae relates to nonvolatile memory devices and their fabricating methods. EX1004, [0002]. Similar to the ’737 patent, Chae recognizes the issue of stack collapsing in the edge portion when removing the sacrificial layers in the stack, and solves the problem by forming supporters penetrating the stack to support the edge portion during the sacrificial layers etching process. EX1004, [0159], [0162]. Chae also aims at “reducing the resistance of gate electrodes,” “preventing process defects,” and improving the “operation speed of the three-dimensional nonvolatile memory device” EX1004, [0007]-[0008], [0160].

As shown in the circuit diagram of annotated FIG. 1 below, which applies to “exemplary embodiments of the inventive concept” of Chae in general, a 3D NAND-type nonvolatile memory device includes strings STR (in purple) each including “upper and lower select transistors UST and LST [(in brown)], and memory cells

MC [(in blue)] that are connected in series between the upper and lower select transistors UST and LST.” EX1004, [0041]-[0043]; EX1003, ¶78. “The upper select transistors UST are connected to the upper select lines USL1~USL3, and the lower select transistors LST are connected respectively to the lower select lines LSL. The memory cells MC are connected respectively to the word lines WL1~WL4.” EX1004, [0044].

Fig. 1



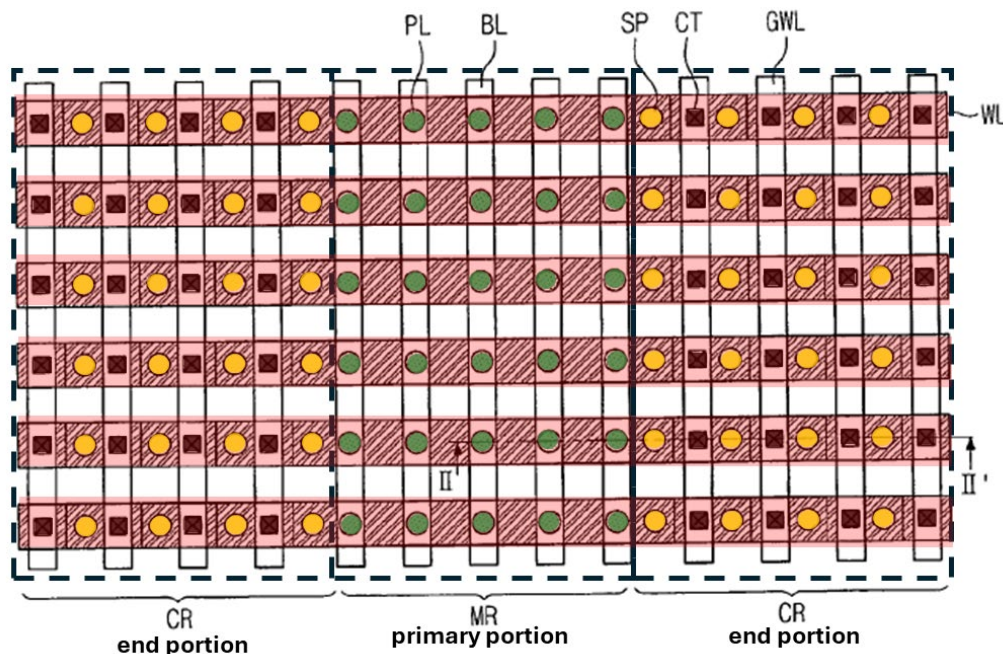
EX1003 — FIG. D

In the fifth embodiment of Chae, as shown in the plan view of annotated FIG. 10 and the cross-sectional view of annotated FIG. 15E⁵ below, a nonvolatile memory device includes a stack of conductive line-shaped gate electrodes 250 (in red)

⁵ FIG. 15E refers to the same fifth embodiment as FIG. 10, which is taken along the line II-II' of FIG. 10. EX1004, [0122].

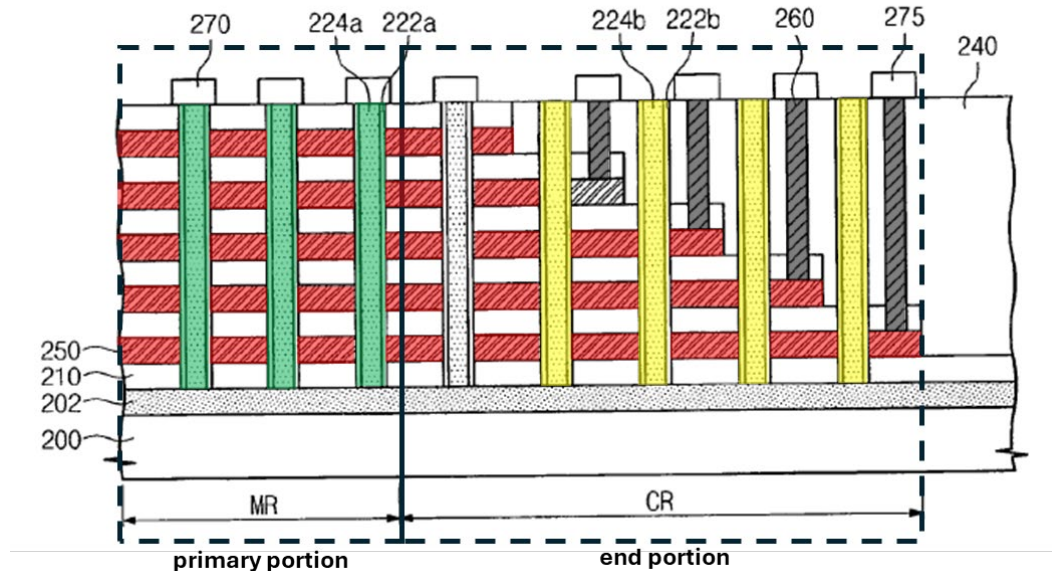
extending horizontally and overlapping vertically, including upper and lower select lines USL and LSL and word lines WL. EX1004, [0078], [0130]; EX1003, ¶79. The stack includes a memory cell region MR (“*primary portion*”) and a contact region CR (“*end portion*”) “formed in a stair shape.” EX1004, [0078], [0132]; EX1003, ¶79. The nonvolatile memory device also includes active pillars PL 224a with charge storage layers 222a (in green) and supporters SP 224b with charge storage layers 222b (in yellow) extending vertically through gate electrodes 250 in memory cell region MR and contact region CR, respectively. EX1004, [0078], [0126], [0128]; EX1003, ¶80. Chae further discloses contact plugs CT 260 (in black), each extending to a respective gate electrode 250 in contact region CR. EX1004, [0131].

Fig. 10



EX1003 — FIG. E

Fig. 15E



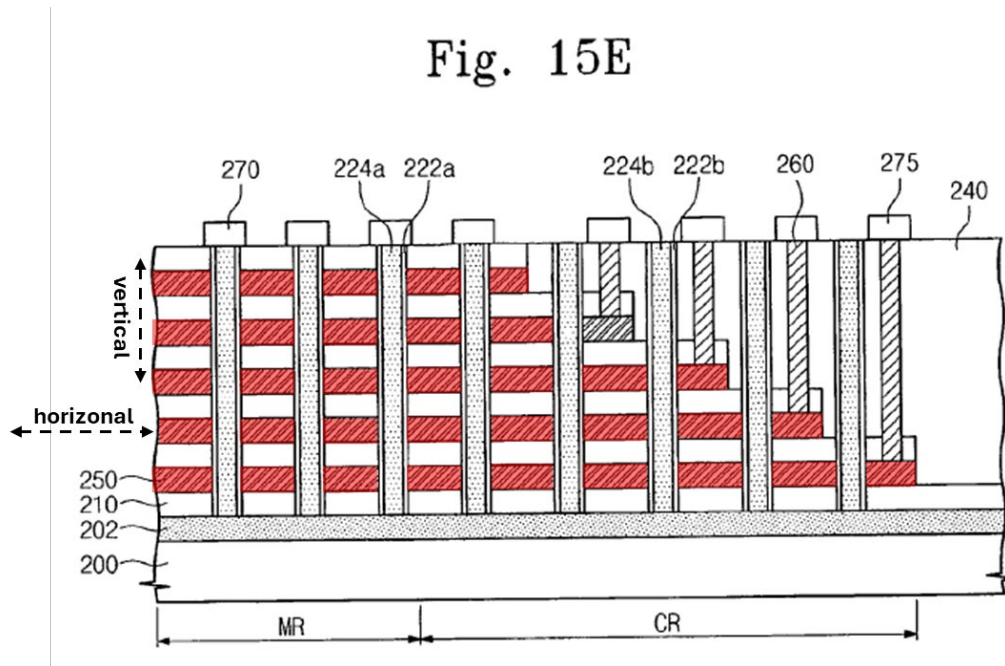
EX1003 — FIG. F

B. Independent Claim 1

1. Chae discloses “[i]ntegrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines” [1.P].

Chae discloses a nonvolatile memory device (“[i]ntegrated circuitry”) including a stack of conductive line-shaped gate electrodes 250. EX1004, [0122], [0130]. Specifically, as shown in annotated FIG. 15E below, a stack of gate electrodes 250 (in red) extend horizontally and overlap vertically. EX1003, ¶107. A POSITA would have understood that gate electrodes 250, functioning as select lines USL and LSL and word lines WL, control the operations of select **transistors** UST and LST and memory cell **transistors** MC connected thereto, respectively, and thus,

are “*transistor gate lines.*” EX1004, [0043]-[0044], [0078], FIG. 1; EX1003, ¶107.



EX1003 — FIG. L

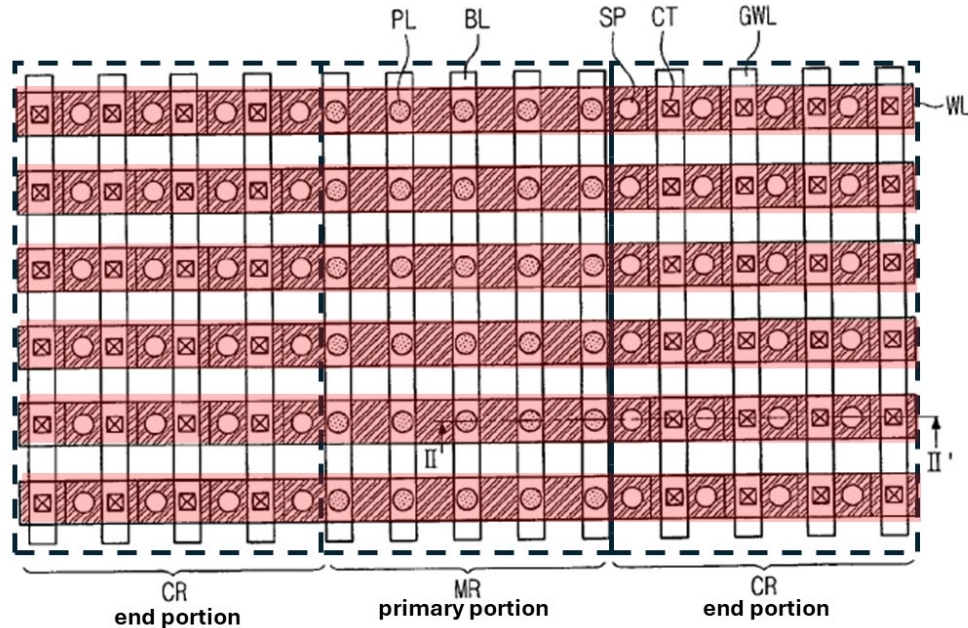
Thus, Chae discloses [1.P].

2. Chae discloses “*a primary portion and an end portion*” [1.a.1], and “*at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion*” [1.a.2].

Chae discloses a memory cell region MR and a contact region CR. EX1004, [0078]. Specifically, as shown in the plan view of annotated FIG. 10 and the cross-sectional view of annotated FIG. 15E below, the nonvolatile memory device (“*integrated circuitry*”) includes memory cell region MR and contact region CR. EX1003, ¶109. A POSITA would have understood that memory cell region MR is the “*primary portion*” since it is where the memory cells are formed, and that contact region CR is the “*end portion*” since it is at the end/edge of the stack. EX1004,

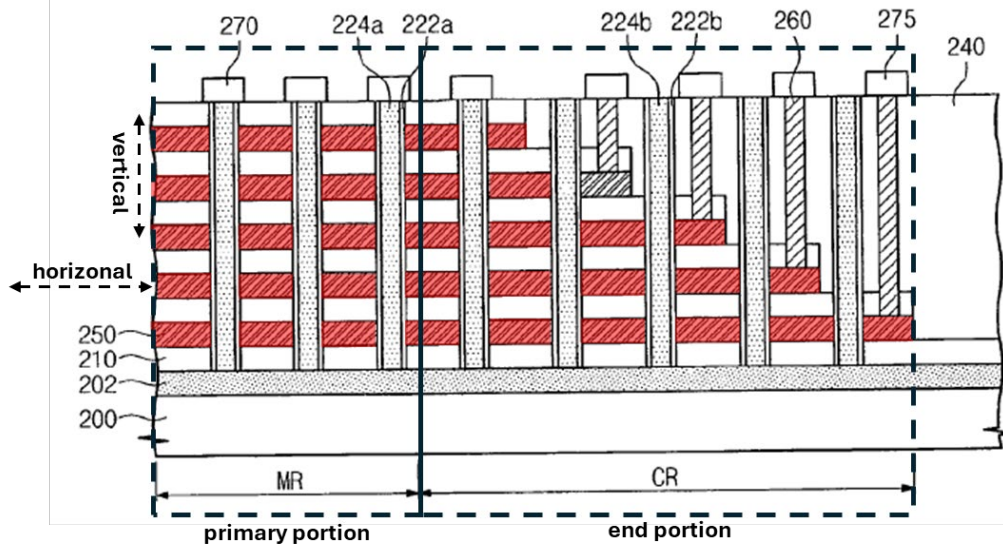
[0078], [0162]; EX1003, ¶110. Thus, Chae discloses [1.a.1].

Fig. 10



EX1003 — FIG. M

Fig. 15E



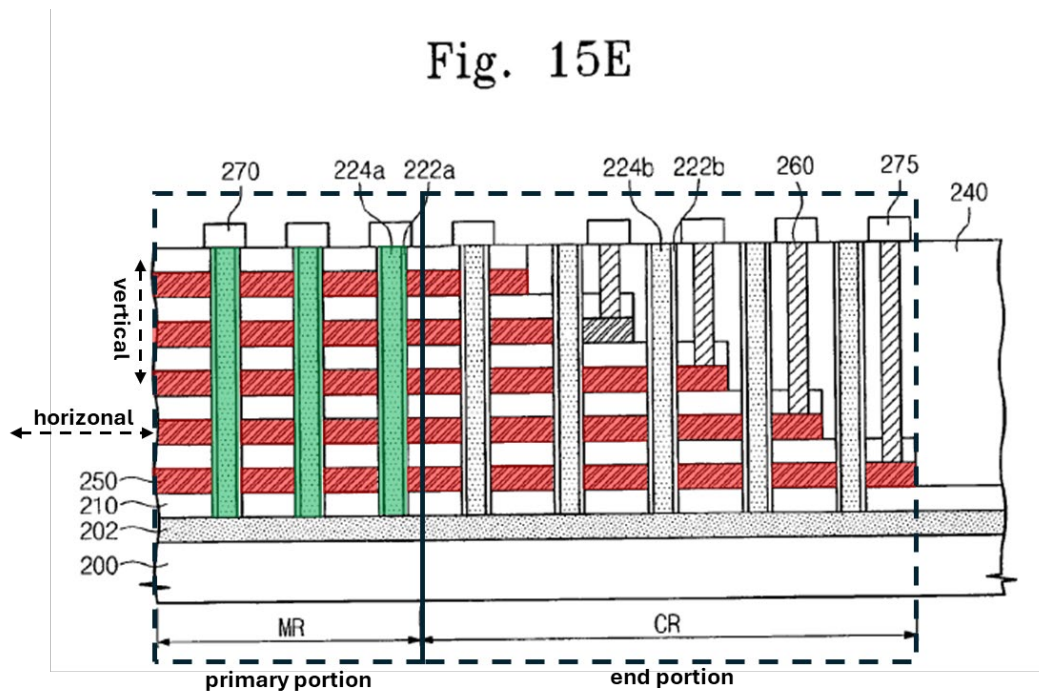
EX1003 — FIG. L

As to [1.a.2], it requires nothing more than the well-known stair-like structure.

EX1003, ¶111. Chae further discloses that “gate electrodes 250 of the contact region CR are formed in **a stair shape.**” EX1004, [0124], [0130], [0132]. As further illustrated in the annotated FIG. 15E above, a POSITA would have understood that in contact region CR (“*end portion*”), gate electrode 250 (in red) at a lower level in the vertical direction of the stack (“*moving deeper into the stack*”) extends farther in the horizontal direction. EX1003, ¶112. Thus, Chae also discloses [1.a.2].

3. Chae discloses or otherwise renders obvious “*operative structures extending vertically through the gate lines in the primary portion*” [1.b.1], “*the operative structures comprising semiconductive material*” [1.b.2], and “*the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines*” [1.b.3].

As shown in annotated FIG.15E below, Chae discloses active pillars 224a with charge storage layers 222a (in green) extending vertically through gate electrodes 250 (in red, “*gate lines*”) in memory cell region MR (“*primary portion*”). EX1004, [0126], [0128]; EX1003, ¶114.

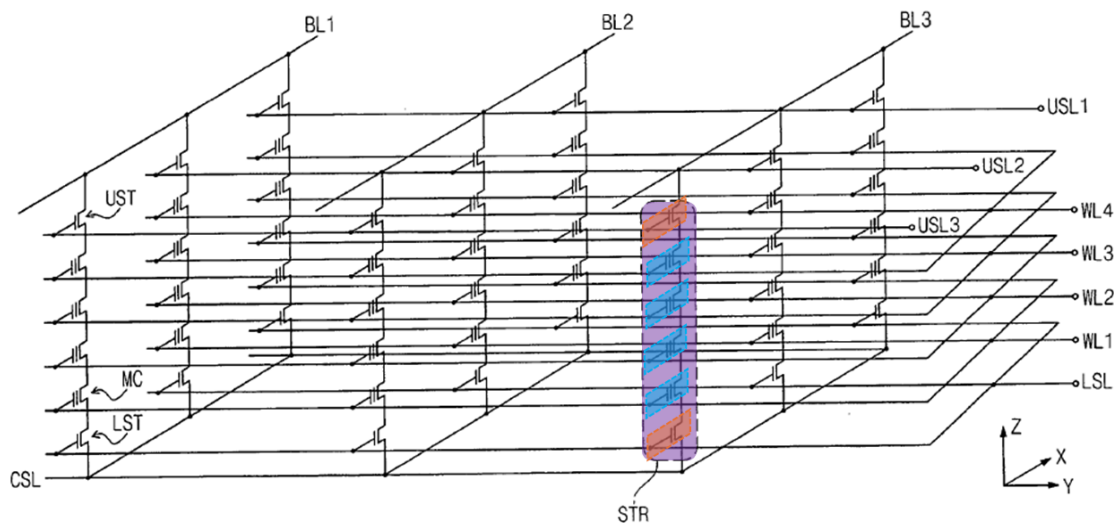


Regarding active pillars 224a and charge storage layers 222a, Chae discloses that “active pillars PL are provided for the channels of transistors” and “the channels of memory cell transistors and select transistors (LST, UST, and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.” EX1004, [0054]-[0055]⁶. Also, according to the ’737 patent, “*operative structures*” may be “circuit components.” EX1001, 6:22-25. Based on these disclosures, a POSITA would have understood that active pillar PL 224a, along with charge storage layer

⁶ A POSITA would have understood that descriptions of the “active pillars PL” and “charge storage layer CS” in paragraphs [0054] and [0055] apply to “active pillars 224a” and “charge storage layer 222a” in the “fifth exemplary embodiment of the inventive concept,” upon which the mappings of Chae are based. EX1004, [0121]; EX1003, ¶115.

222a, are parts of a string STR (in purple in annotated FIG. 1 below), including select transistors UST and LST (in brown) and memory cells MC (in blue), of the nonvolatile memory device and thus, are the “operative structures.” EX1003, ¶116. Thus, Chae discloses [1.b.1].

Fig. 1



EX1003 — FIG. D

Chae also discloses [1.b.2] because it discloses that active pillars 224a (parts of “operative structures”) include “semiconductor material,” such as “monocrystalline or polycrystalline semiconductor material.” EX1004, [0109], [0128].

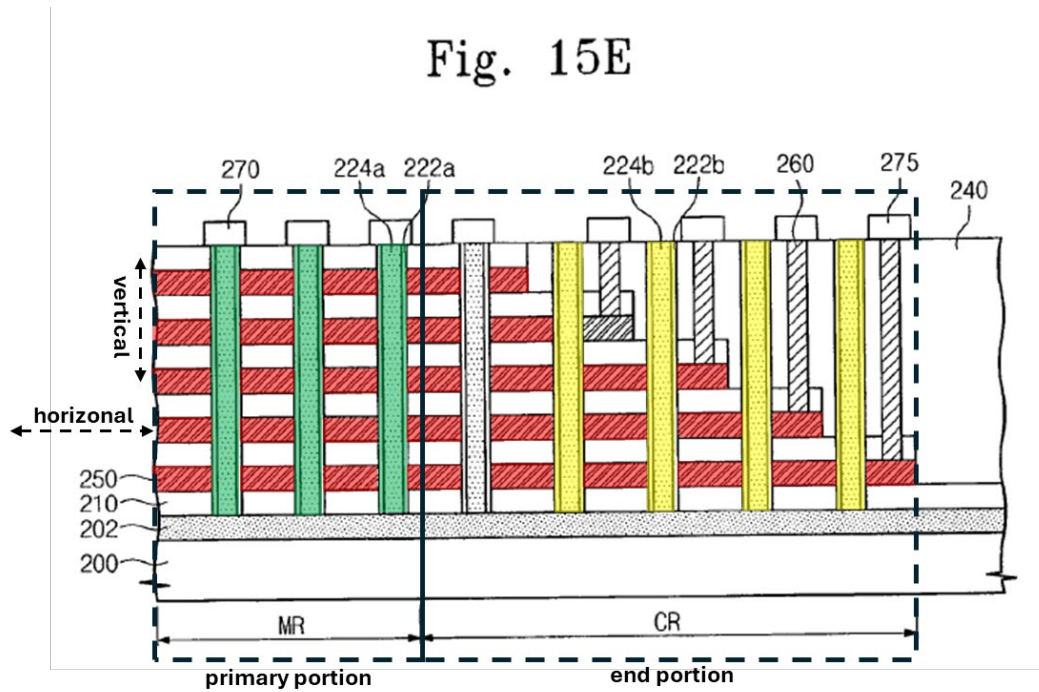
Regarding [1.b.3], Chae further discloses that the semiconductor material of active pillars PL 224a includes interconnected channels of a plurality of vertically oriented memory cell transistors MC, and that the memory cell transistors

individually include gate electrode 250. EX1004, [0043]-[0045], [0054]-[0055]. For example, Chae discloses that “memory cells MC are connected **in series in a Z-axis direction**,” and that “**the channels** of memory cell transistors and select transistors (LST, UST, and MC of FIG. 1) in each string may be **electrically connected through the active pillars PL**.” EX1004, [0045], [0054].

In view of the disclosures of Chae and as further shown in annotated FIG. 1 above, a POSITA would have understood, or at least found it obvious, that (i) the memory cell transistors MC (in blue) are vertically oriented and connected in a string STR (in purple), (ii) each memory cell transistor MC includes a respective gate electrode 250 (“*individual of the gate lines*”) and a channel, and (iii) the channels of the memory cell transistors MC in a string STR (“*a plurality of vertically oriented transistors*”) are vertically interconnected and provided in a respective active pillar PL 224a (part of “*operative structure*”). EX1003, ¶¶120-121. Thus, Chae discloses or otherwise renders obvious [1.b.3].

4. Chae discloses “dummy structures extending vertically through the gate lines in the end portion” [1.c].

As shown in annotated FIG.15E below, Chae discloses supporters 224b with charge storage layers 222b (in yellow) extending vertically through gate electrodes 250 (in red, “*gate lines*”) in contact region CR (“*end portion*”). EX1004, [0126], [0128]; EX1003, ¶123.



Chae discloses that “the first dielectric layers 210 spaced apart from each other may be **supported**” by supporters 224b in the “contact region CR,” and so can active pillars 224a in the “memory cell region MR,” such that “the second dielectric layers 215 can be prevented from collapsing or getting near to each other during the removing of the second dielectric layers 215 through a wet etch process.” EX1004, [0129], [0159], [0162]. Chae also discloses that supporters 224b with charge storage layers 222b and active pillars 224a with charge storage layers 222a are formed of the same materials in the same process with the same structures. EX1004, [0128], *see* [0037]; EX1003, ¶124. Therefore, a POSITA would have understood that supporters 224b with charge storage layers 222b mimic a physical property of active pillars 224a with charge storage layers 222a. EX1003, ¶124.

Chae further discloses that supporters 224b “do[] not affect the operation of the nonvolatile memory device” “[b]ecause a conductive pattern such as the global word line 275 or the bit line 270 is not formed on the supporters 224b.” EX1004, [0134]. Thus, a POSITA would have understood that supporter 224b with charge storage layer 222b is an electrically inoperable structure. EX1003, ¶124.

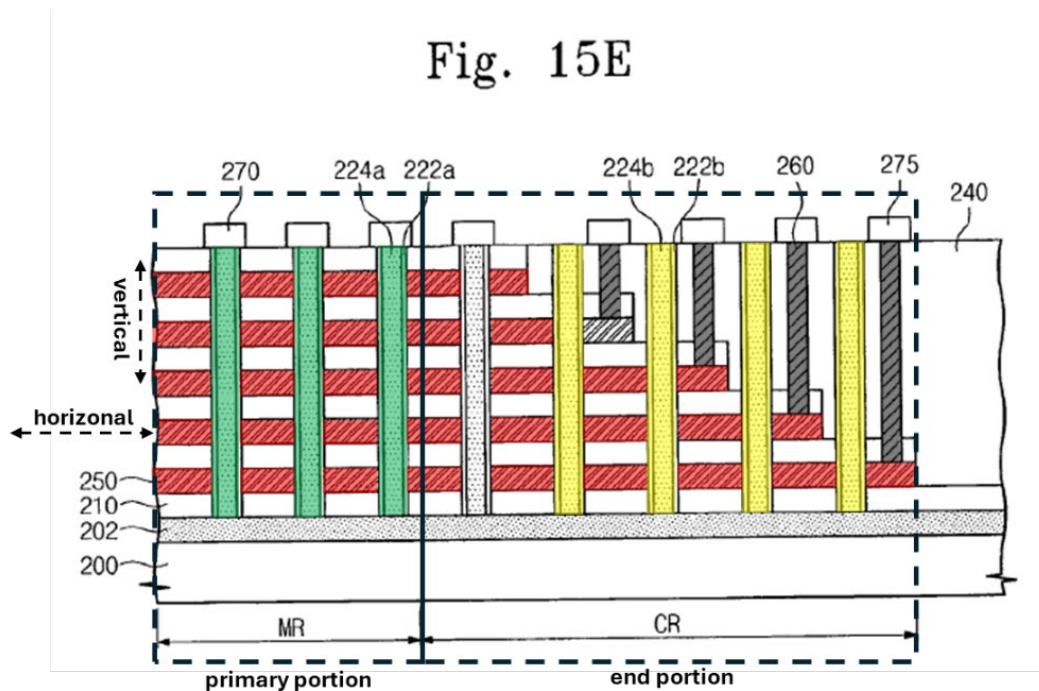
Accordingly, supporters 224b with charge storage layers 222b collectively are “*dummy structures*” under the construction of “electrically inoperable structure that mimics a physical property of an operative structure.” *See* Section VI. Thus, Chae discloses [1.c].

From the foregoing, Chae anticipates or otherwise renders obvious claim 1.

C. Dependent Claim 2

Chae further discloses “*contacts in the end portion that individual extend to the individual gate lines,*” additionally required by claim 2.

As shown in annotated FIG.15E below, Chae further discloses contact plugs 260 (in black, “*contacts*”) in contact region CR (“*end portion*”), each extending to a respective gate electrode 250 (in red, “*individual gate lines*”). EX1004, [0131]; EX1003, ¶128.



D. Dependent Claim 3

Chae further discloses or otherwise renders obvious that “*the vertically oriented transistors are charge storage transistors of individual memory cells,*” additionally required by claim 3. Specifically, Chae discloses or at least suggests that the memory cell transistors MC (“*vertically oriented transistors*”) include charge storage layers 222a. EX1004, [0054]-[0055], [0128].

It is known in the art that charge storage layer 222a surrounding semiconductor material, as recited in the fifth embodiment of Chae upon which the mappings are based, includes materials, such as silicon nitride in charge trapping memory, or polysilicon in floating gate memory. EX1021, Table 1; EX1022, 2847, §I; EX1003, ¶130. Charge stored in charge storage layer 222a alters the threshold

voltage, which is required at the corresponding gate electrode 250 to enable current flow through the semiconductor material. EX1003, ¶130. These varying threshold voltages of memory cell transistors MC can indicate the storage of information. EX1023, 189; EX1003, ¶130. Accordingly, a POSITA would readily appreciate that a memory cell transistor MC having charge storage layer 222a forms a “*charge storage transistor*.” EX1003, ¶130.

E. Dependent Claim 4

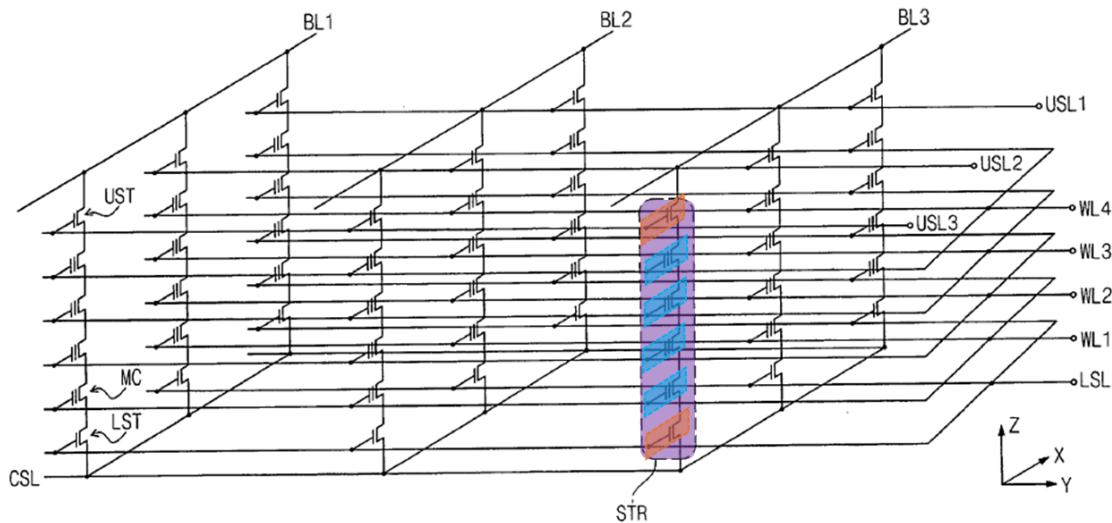
Chae further discloses that “*the memory cells comprise a portion of NAND architecture*,” additionally required by claim 4.

Chae discloses memory cell transistors MC are a portion of a NAND-type nonvolatile memory device (“*NAND architecture*”). EX1004, [0005]-[0006], [0043]. Specifically, Chae discloses that “the NAND-type nonvolatile memory device ... includes a cell string structure having a plurality of memory cell transistors connected in series,” and that “[e]ach string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series.” EX1004, [0005], [0043]. Chae’s disclosures are consistent with the Applicant-Admitted Prior Art (AAPA) of “*NAND architecture*” in the Background section of the ’737 patent. EX1001, 3:1-5.

As shown in the annotated FIG. 1 of Chae below, a POSITA would have understood that memory cell transistors MC (in blue) connected in series in a string

STR (in purple) are parts of the NAND architecture in the nonvolatile memory device. EX1003, ¶134.

Fig. 1



EX1003 — FIG. D

F. Dependent Claims 5 and 6

Chae further discloses or otherwise renders obvious that “*the operative and dummy structures comprise the same material*” additionally required by claim 5, and “*a plurality of the same materials*” additionally required by claim 6.

Specifically, Chae discloses that active pillars 224a with charge storage layers 222a (collectively “*operative structures*”) and supporters 224b with charge storage layers 222b (collectively “*dummy structures*”) include the same semiconductor material (“*the same material*”), as well as the same semiconductor and charge storage materials (“*a plurality of the same materials*”). EX1004, [0081], [0128], see

[0037].

A POSITA would have understood that since “the dummy holes and the channel holes are **filled with semiconductor material** to form active pillars 224a and supporters 224b,” the resulting active pillars 224a and supporters 224b are both made of the semiconductor material. EX1004, [0128]; EX1003, ¶¶136-137. A POSITA would have also understood that charge storage layers 222a and 222b are both made from a charge storage material, such as silicon nitride or polysilicon. EX1003, ¶¶136-137.

To the extent that the above-quoted disclosures do not explicitly teach that the semiconductor materials forming active pillars 224a and supporters 224b are the same, and/or the charge storage materials forming charge storage layers 222a and 222b are the same, a POSITA would have found it obvious to use the same materials fill both the dummy holes and channel holes to form active pillars 224a with charge storage layers 222a and supporters 224b with charge storage layers 222b, respectively. This is because doing so would advantageously reduce the number of processing steps. EX1003, ¶¶138-139. Fewer processing steps would have been advantageous because it would have reduced the chance of defects and shortened the manufacturing time, allowing higher fabrication yield. EX1014, 54; EX1015, [0004], [0108], [0190]; EX1003, ¶139.

A POSITA would have recognized that filling both the dummy holes and

channel holes using the same materials would predictably work and yield the expected resulting structures. EX1003, ¶140. This is because using well-known deposition processes, such as chemical vapor deposition (CVD) and/or atomic layer deposition (ALD), to achieve this is common practice in the art. EX1005, [0124]-[0125]; EX1003, ¶140.

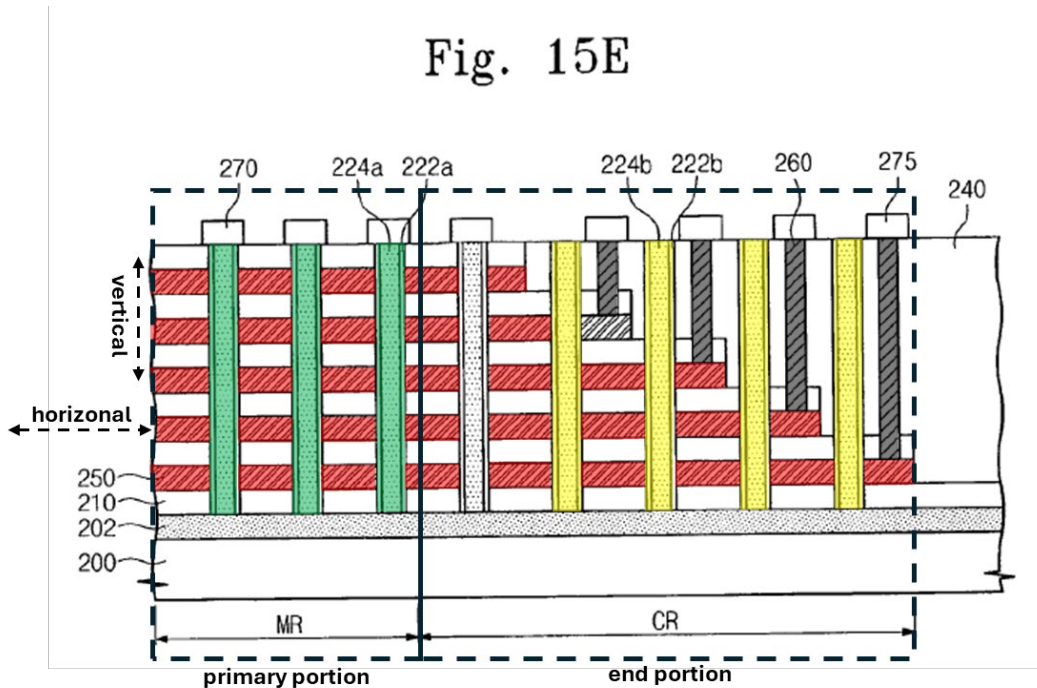
G. Dependent Claim 7

Chae further discloses or otherwise renders obvious that “*the same materials are arranged in the same lateral order relative one another in the operative and dummy structures,*” additionally required by claim 7.

Specifically, Chae discloses that the same charge storage material and the same semiconductor material are arranged in the same centripetal direction inward towards the centers of active pillars 224a and supports 224b (“*in the same lateral order relative one another in the operative and dummy structures*”). EX1004, [0128]; EX1003, ¶143.

As shown in the annotated FIG. 15E below, in both active pillars 224a with charge storage layers 222a (in green, “*operative structures*”) and supporters 224b with charge storage layers 222b (in yellow, “*dummy structures*”), the same charge storage material forming charge storage layers 222a and 222b is arranged on the side, and the same semiconductor material forming active pillars 224a and supporters

224b is arranged in the center and thus, are “*in the same lateral order relative one another.*” EX1003, ¶142.



EX1003 — FIG. P

H. Dependent Claim 8

Claim 8 additionally requires that “*the operative and dummy structures consist essentially of the same material.*”

It is well established that, absent a clear indication in the specification or claims of what the basic and novel characteristics actually are, “*consist essentially of*” will be construed as equivalent to “*comprise*” in evaluating patentability. *PPG Industries v. Guardian Industries*, 156 F.3d 1351, 1355 (Fed. Cir. 1998). Since the specification of the ’737 patent merely repeats the language of claim 8 without further elaboration—let alone specifying the basis and novel characteristics—claim

8 effectively has the same scope as claim 5. EX1001, 6:67-7:2, 7:50-52. Consequently, claim 8 is anticipated or otherwise rendered obvious by Chae for at least the reasons discussed in Section VII.F with respect to claim 5.

Thus, Chae discloses or otherwise renders obvious claim 8.

I. Dependent Claim 9

As discussed in Section VII.F, Chae discloses that supporters 224b with charge storage layers 222b (collectively “*dummy structures*”) “*comprise semiconductor material,*” which is additionally required by claim 9.

J. Dependent Claim 10

Claim 10 additionally requires that “*the dummy structures comprise the semiconductive material,*” which is disclosed by Chae. As discussed in Sections VII.B.3 and VII.F, since active pillars 224a and supporters 224b are made of the same semiconductor material, supporters 224b include the same semiconductive material as active pillars 224a (“*the semiconductive material*”). EX1003, ¶147.

K. Independent Claim 11

1. Chae discloses a “*stack of horizontally extending and vertically overlapping features*” [11.P].

As discussed in Section VII.B.1, Chae discloses a stack of horizontally extending and vertically overlapping conductive line-shaped gate electrodes 250.

The ’737 patent explains that “*features*” may be “horizontally extending lines,” such as horizontally extending conductive lines. EX1001, 11:28-34. Also, dependent

claim 15 further recites “*vertical contacts in the end portion connecting with **conductive material** of individual of the features.*” A POSITA would, therefore, have understood that conductive line-shaped gate electrodes 250 of Chae qualify as the claimed “*features.*” EX1003, ¶151. To the extent PO argues the “*features*” require a combination of horizontally extending conductive lines and dielectric lines⁷, each pair of gate electrode 250 and first dielectric layer 210 in Chae would still collectively qualify as one of the “*features,*” which would not affect the mapping of Chae to any claim limitations related to the “*features*” in Grounds 1-3 and 6. EX1003, ¶152.

2. Chae discloses “*a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion*” [11.a].

Chae discloses or otherwise renders obvious [11.a], which is essentially the same as [1.a.1] and [1.a.2]. See Section VII.B.2.

3. Chae discloses “*operative structures extending vertically through the features in the primary portion*” [11.b].

Chae discloses [11.b], which is essentially the same as [1.b.1]. See Section VII.B.3.

⁷ Petitioner does not concede such an overly narrowed construction, as it directly contradicts the explicit teachings of the ’737 patent, which states that “the features may be horizontally extending lines, for example formed of **any one** or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s).” EX1001, 11:28-31.

4. **Chae discloses or otherwise renders obvious “*dummy structures extending vertically through the features in the end portion*” [11.c.1], and “*the dummy structures individually comprising a cylinder of semiconductive material*” [11.c.2].**

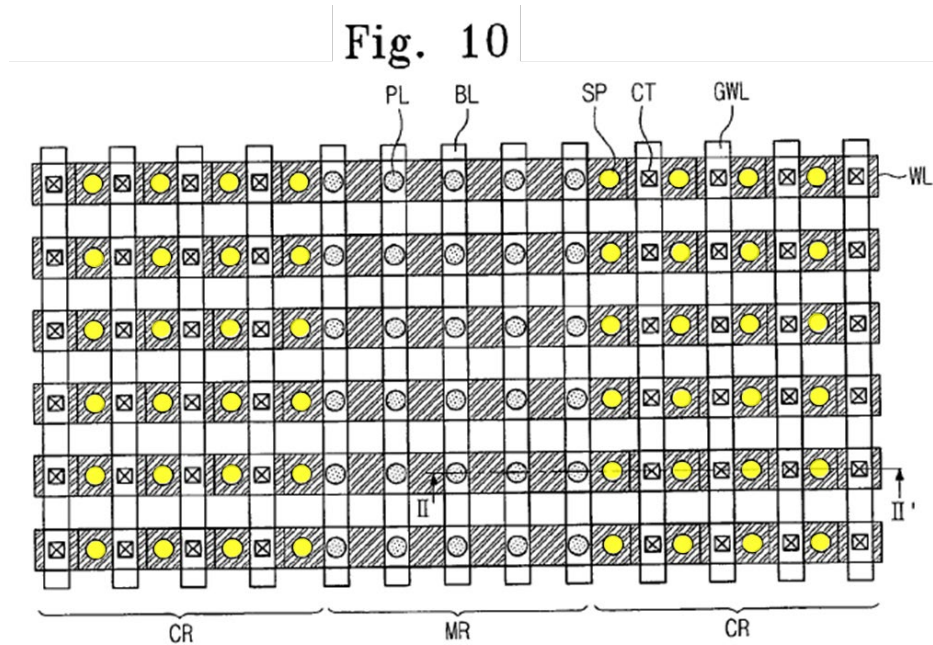
Chae discloses [11.c.1], which is essentially the same as [1.c]. *See* Section VII.B.4.

Regrading [11.c.2], as discussed in Sections VII.F, VII.I, and VII.J, Chae discloses that supporters SP 224b with charge storage layers 222b (collectively “*dummy structures*”) individually include a semiconductor material.

Moreover, Chae discloses that supporters SP can have various shapes, including “the shape of a cylindrical pillar” in FIG. 2A or “circular pillars” in FIG. 6, compared with “line-shaped” or “line patterns that are connected to each other and extend in different directions on the plane” in FIGs. 2B and 2C, respectively. EX1004, [0058]-[0060], [0071]. Thus, a POSITA would have understood that the plan-view drawings of Chae (e.g., FIGs. 2A, 2B, 2C, and 6) reflect the intended shapes of supporters SP. EX1003, ¶158. Similarly, FIG. 10, a plan view drawing of the fifth embodiment of Chae, reflects the shape of supporters SP in this embodiment, which is also the “shape of a cylindrical pillar,” the same as those shown in FIGs. 2A and 6. EX1004, [0058]; EX1003, ¶159.

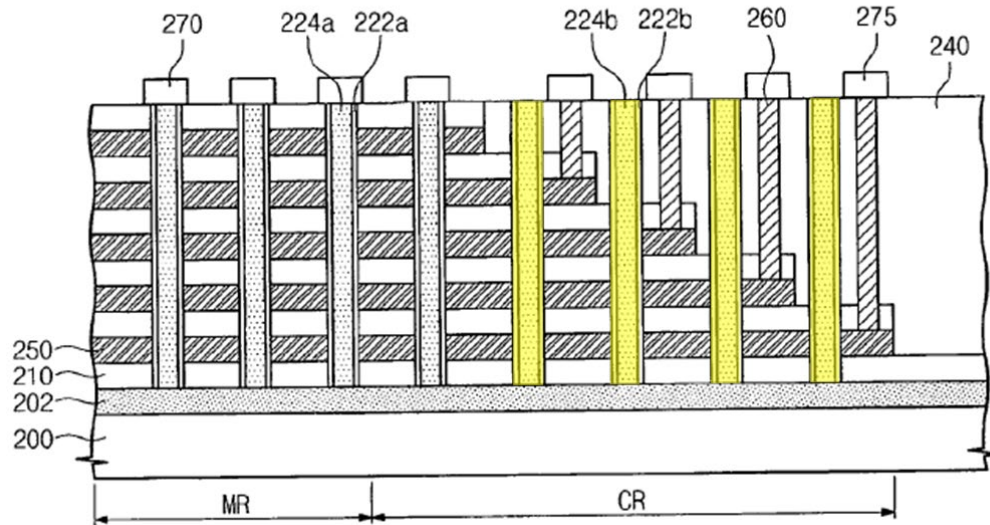
As shown in annotated FIG. 10 (plan view) and further in view of annotated FIG.15E (sectional view along the line II-II’ of FIG. 10) below, a POSITA would

have understood, or at least found it obvious, that each supporter SP 224b with charge storage layer 222b (in yellow, “*dummy structures individually*”) has a semiconductor material in the shape of a cylinder (“*a cylinder of semiconductive material*”). EX1003, ¶160.



EX1003 — FIG. Q

Fig. 15E



EX1003 — FIG. R

L. Dependent Claim 12

Chae discloses or otherwise renders obvious “*solid material filling radially internal regions of individual of the cylinders of semiconductive material,*” additionally recited in claim 12.

The term “*solid material*” should be interpreted under the plain and ordinary meaning, which refers to a material “without an internal cavity.” EX1013, 1a; EX1003, ¶162. While the phrase “*solid material*” itself is nowhere to be found in the specification of the ’737 patent, the specification’s usage of “solid” supports this interpretation. For example, the specification describes operative structures 31 and dummy structures 32 “may be in the form of laterally solid pillars.” EX1001, 6:55-57.

Chae discloses that “the dummy holes ... are **filled** with semiconductor material to form ... supporters 224b.” EX1004, [0128]. Under the plain and ordinary meaning of “*solid material*,” a POSITA would have understood, or at least found it obvious, that the semiconductor material disclosed by Chae is a “*solid material*,” which **fills**, *i.e.*, occupies the whole of, the radially internal region of each supporter 224b in the shape of a cylinder (“*individual of the cylinders of semiconductive material*”). EX1003, ¶¶163-164; *see* Sections VII.I, VII.K.4.

To the extent that PO contends the term “*solid material*” in [12] differs from the “*semiconductive material*” in [11.c], and/or that the “*cylinder*” in [11.c] is limited to a “[*hollow*] *cylinder*,” such interpretations are unsupported. Claim 12 does not require “*solid material*” to be distinct from the “*semiconductive material*.” Nor does the specification of the ’737 patent describe the relationship between a “*solid material*” and “*the semiconductive material*.” These interpretations also depart from the plain and ordinary meaning of “*cylinder*” and “*solid material*,” as the ’737 patent neither provides an explicit definition of these terms nor disavows their full scope in the specification or during prosecution. *HillRom Servs., Inc. v. Stryker Corp.*, 755 F.3d 1367, 1371 (Fed. Cir. 2014).

In fact, when the ’737 patent intends to refer to hollow structures, it explicitly

uses the term “**hollow** cylinders” rather than “cylinders.”⁸ EX1001, 6:53-55. This distinction reinforces that the plain and ordinary meaning of “*cylinder*” encompasses both hollow and solid structures, while “*solid material*” retains its interpretation as material without an internal cavity.

M. Dependent Claim 14

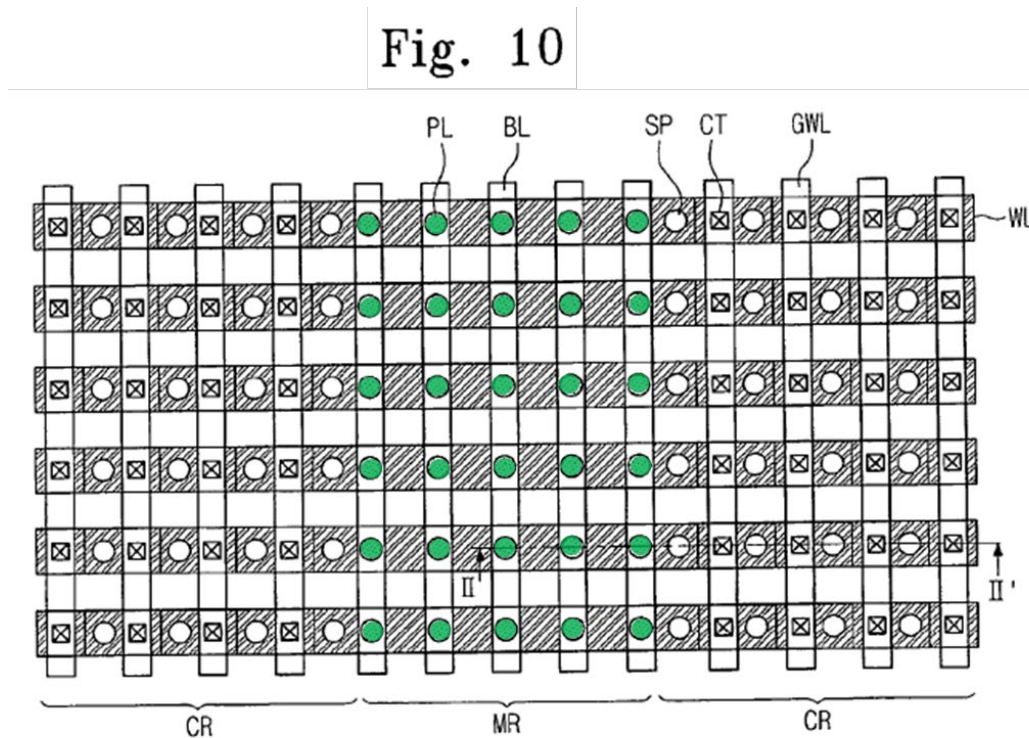
Chae discloses or otherwise renders obvious that “*the operative structures individually comprise a cylinder of semiconductor material,*” additionally required by claim 14. As discussed in Section VII.F, Chae discloses that active pillars PL 224a with charge storage layers 222a (collectively “*operative structures*”) individually include a semiconductor material.

Moreover, Chae discloses that active pillars PL can have various shapes, including “a cylindrical shape” in FIGs. 2A, 2B, 2C, and 4 of the first and second embodiments, compared with a line shape in FIG. 6 of the third embodiment. EX1004, [0070]. Thus, a POSITA would have understood that the plan view drawings of Chae (*e.g.*, FIGs. 2A, 2B, 2C, 4, and 6) reflect the intended shapes of active pillars PL. EX1003, ¶167. Similarly, FIG. 10, a plan view drawing of the fifth embodiment of Chae, reflects the shape of active pillars PL in this embodiment upon which the mappings are based, which is also the “cylindrical shape,” the same as

⁸ The parent ’175 patent also explicitly recites “**hollow** cylinder” in claims 6 and 10 when it intends to claim hollow structures. EX1008, 12:16, 31, 44-45, 48-50.

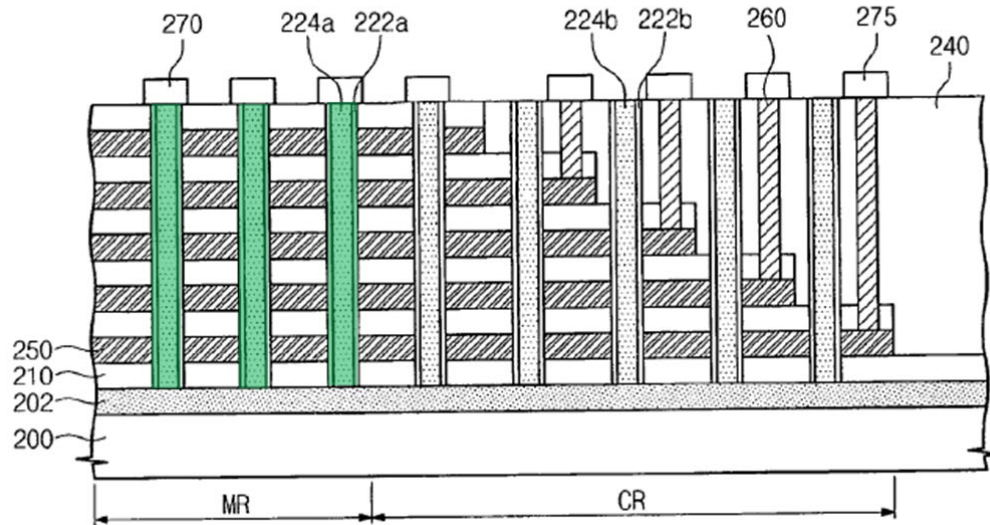
those shown in FIGs. 2A, 2B, 2C, and 4. EX1004, [0070]; EX1003, ¶168.

As shown in annotated FIG. 10 and further in view of annotated FIG.15E below, a POSITA would have understood, or at least found it obvious, that each active pillar PL 224a with charge storage layer 222a (in green, “*operative structures individually*”) has a semiconductor material in the shape of a cylinder (“*a cylinder of semiconductive material*”). EX1003, ¶169.



EX1003 — FIG. S

Fig. 15E



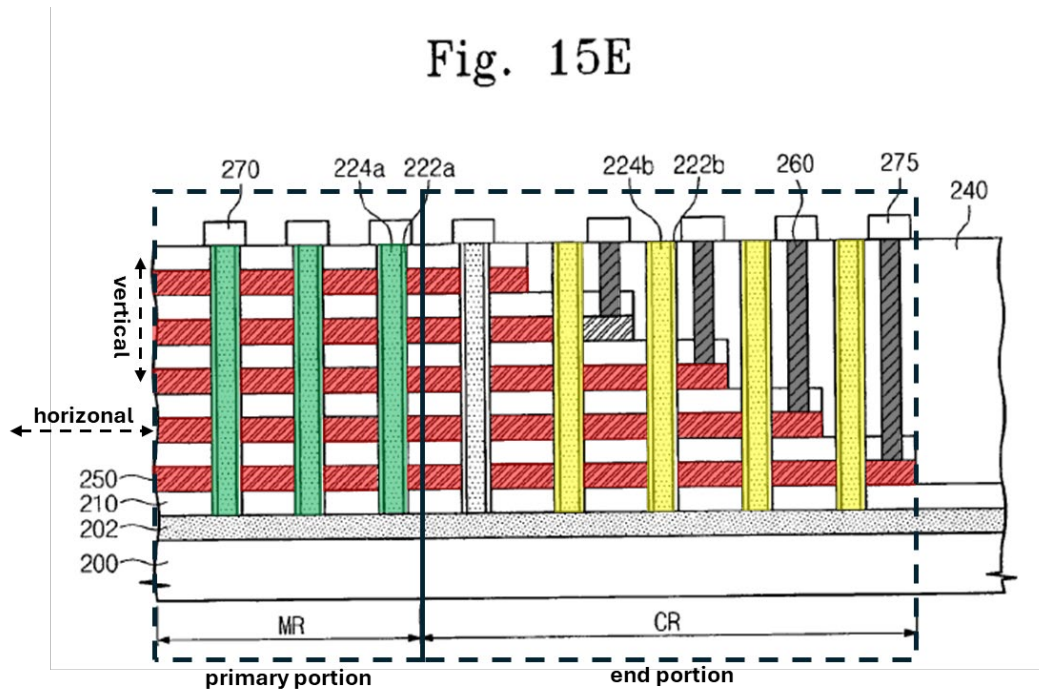
EX1003 — FIG. T

N. Dependent Claim 15

Chae discloses “vertical contacts in the end portion connecting with conductive material of individual of the features,” additionally required by claim 15.

As discussed in Section VII.C, Chae discloses that “contact plugs 260, connected respectively to the gate electrodes 250 of each layer, are formed in the contact region CR of the gate electrodes 250.” EX1004, [0131]. As shown in annotated FIG. 15E below, each contact plug 260 (in black) extends vertically to connect a respective global word line 275 “formed **on** the contact plugs 260,” and connect a respective gate electrode 250 underneath (in red, “individual of the

features”), and thus, are “**vertical contacts**.” EX1004, [0119]-[0120]; EX1003, ¶172.



Additionally, since each gate electrode 250 is formed of a conductive material, such as “polysilicon or metal material,” contact plugs 260 (“*vertical contacts*”) connect with the conductive material of each gate electrode 250 (“*individual of the features*”). EX1004, [0130]-[0131]; EX1003, ¶173.

O. Independent Claim 21

1. Chae discloses a “*stack of horizontally extending and vertically overlapping features*” [21.P].

Chae discloses [21.P], which is the same as [11.P]. See Section VII.K.1.

2. Chae discloses *“a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion”* [21.a].

Chae discloses or otherwise renders obvious [21.a], which is the same as [11.a]. *See* Section VII.K.2.

3. Chae discloses or otherwise renders obvious *“operative structures extending vertically through the features in the primary portion”* [21.b.1], *“the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string”* [21.b.2], and *“the at least some of the features comprising control gate lines”* [21.b.3].

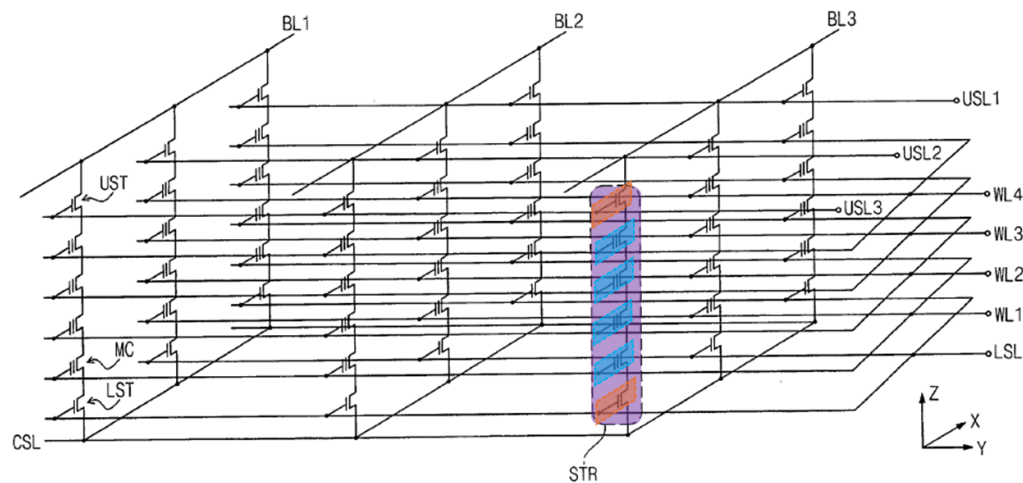
Chae discloses [21.b.1], which is essentially the same as [11.b]. *See* Section VII.K.3.

Regarding [21.b.2], Chae discloses that “active pillars PL are provided for the channels of transistors” and “the channels of memory cell transistors and select transistors (LST, UST, and MC of FIG. 1) in each string may be electrically connected through the active pillars PL.” EX1004, [0054], *see* [0043], [0045], [0055]. Chae further explains that “the NAND-type nonvolatile memory device ... includes a cell string structure having a plurality of memory cell transistors connected in series,” and that “[e]ach string STR includes upper and lower select transistors UST and LST, and memory cell transistors MC that are connected in series.” EX1004, [0005], [0043]. Chae’s disclosures are consistent with the “NAND

architecture” described in the Background section of the ’737 patent. EX1001, 3:1-5.

As shown in the annotated FIG. 1 of Chae below, a POSITA would have understood that (i) the memory cells MC (in blue) connected in series in a string STR (in purple, “*NAND string*”) are parts of the NAND architecture in the nonvolatile memory device, and (ii) active pillars PL (parts of “*operative structures*”) each includes interconnect channels of the memory cells MC (“*portions of memory cells*”) in the string STR. EX1003, ¶181. Thus, Chae discloses or otherwise renders obvious [21.b.2].

Fig. 1



EX1003 — FIG. D

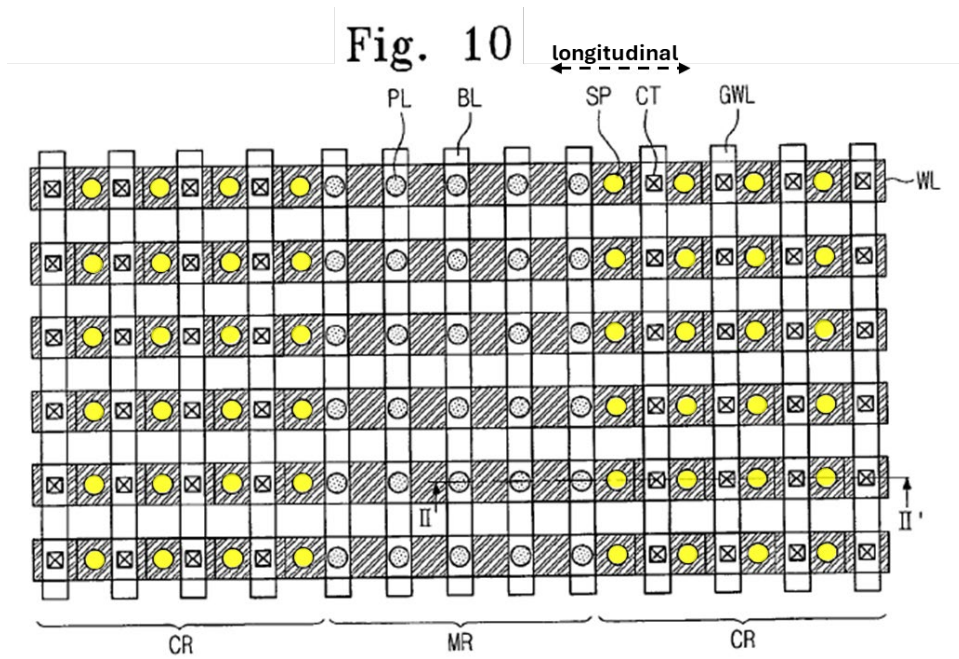
As to [21.b.3], Chae discloses that gate electrodes 250 (“*features*”) include word lines and select lines. EX1004, [0078], *see* [0044], [0051], FIG. 1. A POSITA would have understood that gate electrodes 250, functioning as word lines WL and

select lines USL and LSL, control the operations of memory cell transistors MC and select transistors UST and LST connected thereto, respectively, and thus, include “*control gate lines.*” EX1003, ¶183.

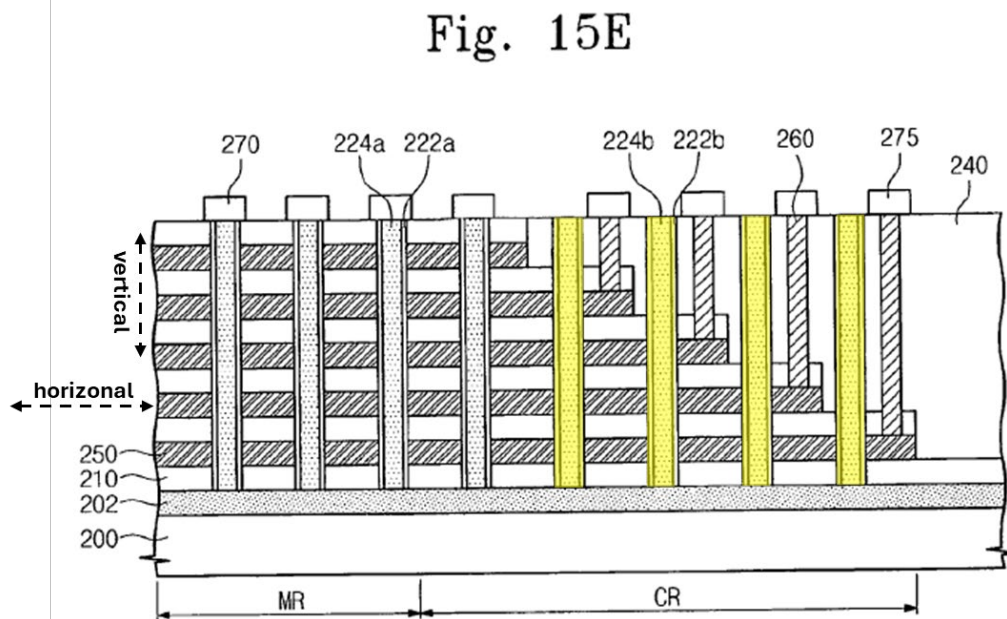
4. Chae discloses “*dummy structures extending vertically through the control gate lines in the end portion*” [21.c.1], and “*some of the dummy structures being longitudinally spaced along a horizontal line*” [21.c.2].

Chae discloses [21.c.1], which is essentially the same as [11.c.1]. See Section VII.K.4.

Regarding [21.c.2], Chae discloses that the dummy holes in which supporters SP 224b with charge storage layers 222b (collectively “*dummy structures*”) are formed “on the same line are spaced apart from each other” (“*longitudinally spaced along a horizontal line*”). EX1004, [0127]-[0128]; EX1003, ¶186. As further shown in annotated FIG. 10 (plan view) and FIG. 15E (sectional view along the line II-II’) below, Chae discloses that supporters SP 224b (in yellow) are longitudinally spaced along the line II-II’ (“*a horizontal line*”). EX1003, ¶187. Thus, Chae discloses [21.c.2].



EX1003 — FIG. U

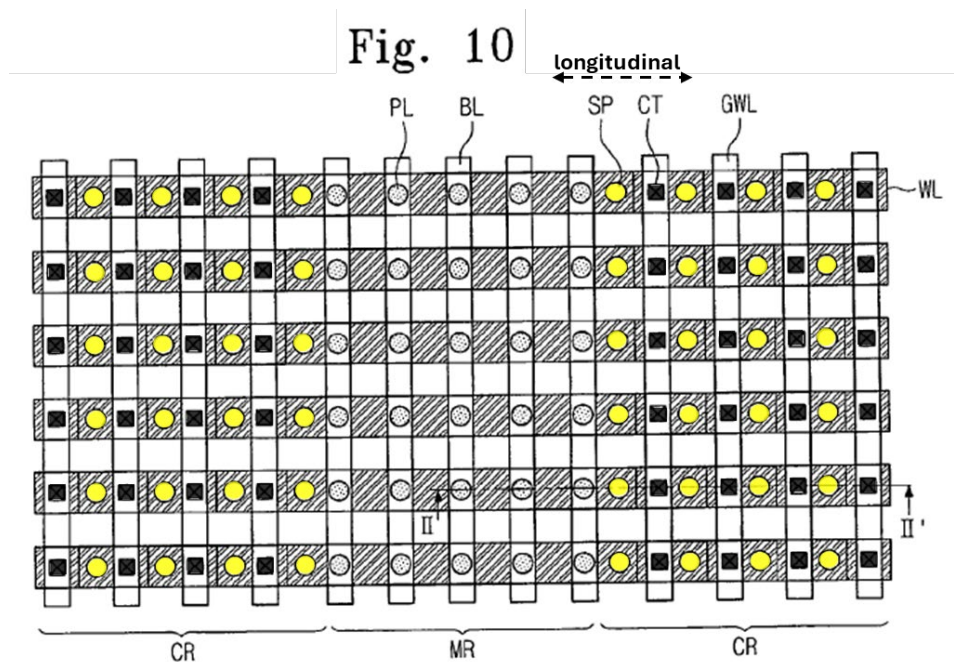


EX1003 — FIG. V

5. Chae discloses “vertical contacts in the end portion connecting with individual of the control gate lines” [21.d.1], and “at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line” [21.d.2].

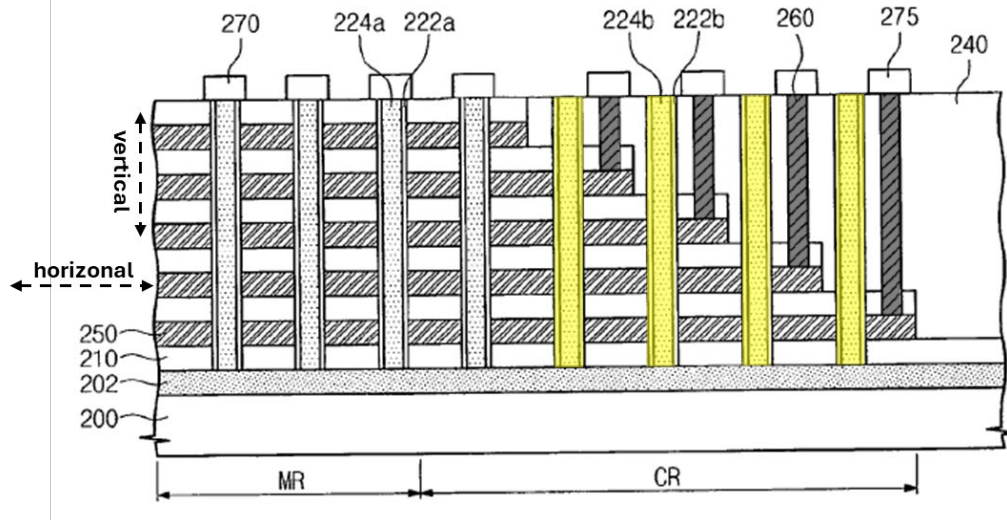
Chae discloses [21.d.1], which is essentially the same as [15]. Section VII.N.

Chae further discloses or otherwise renders obvious [21.d.2]. As depicted in annotated FIG. 10 and 15E below, a POSITA would have understood, or at least found it obvious, that at least one of contact plugs CT 260 (in black) is longitudinally between two immediately-longitudinally adjacent supporters SP 224b (in yellow) in the line II-II,’ along which supporters SP 224b are longitudinally spaced (“horizontal line”). EX1003, ¶190.



EX1003 — FIG. W

Fig. 15E



EX1003 — FIG. X

P. Dependent Claim 22

Chae further discloses that “*the horizontal line is linearly straight,*” additionally required by claim 22.

As discussed in Section VII.O.5 and particularly shown in FIG. 10 of Chae above, a POSITA would have understood that the line II-II’ (“*horizontal line*”) is linearly straight. EX1003, ¶191.

**VIII. GROUND 3: CHAE IN VIEW OF KIYOTOSHI RENDERS
OBVIOUS CLAIMS 5-8, 10-12, 14, AND 15**

As discussed in Section VII, Chae anticipates or otherwise renders obvious claims 5-8, 10-12, 14, and 15. To the extent further disclosure is required, Chae in

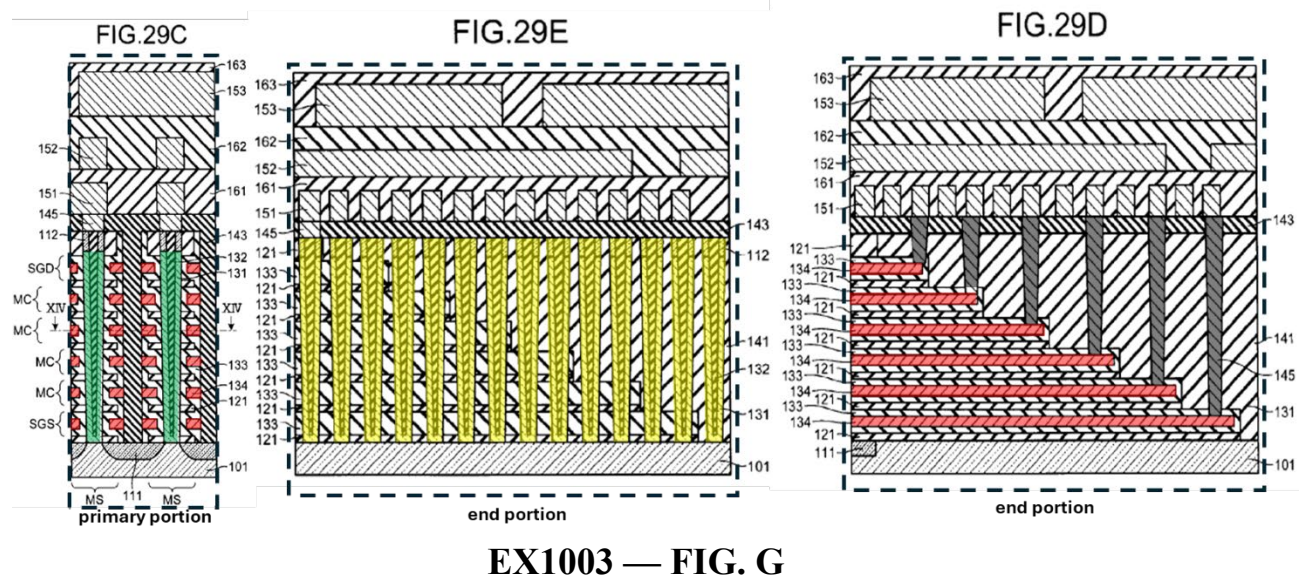
view of Kiyotoshi renders these claims obvious.

A. Overview of Kiyotoshi

Kiyotoshi is directed to a nonvolatile semiconductor memory device. EX1005, [0003]. Like Chae and the '737 patent, Kiyotoshi also recognizes the problem of dielectric layers collapsing while replacing sacrificial layers between the dielectric layers with conductive gate layers, and proposes addressing the problem by using dummy semiconductor films 131 to provide support in a word-line contact region 20. EX1005, [0127]; EX1003, ¶84. The hollow cylindrical semiconductor films 131 in a memory cell region 11 form “memory strings MS,” while the hollow cylindrical semiconductor films 131 in word-line contact region 20 “do not form the memory strings MS and are dummy semiconductor films 131.” EX1005, [0116]; EX1003, ¶85.

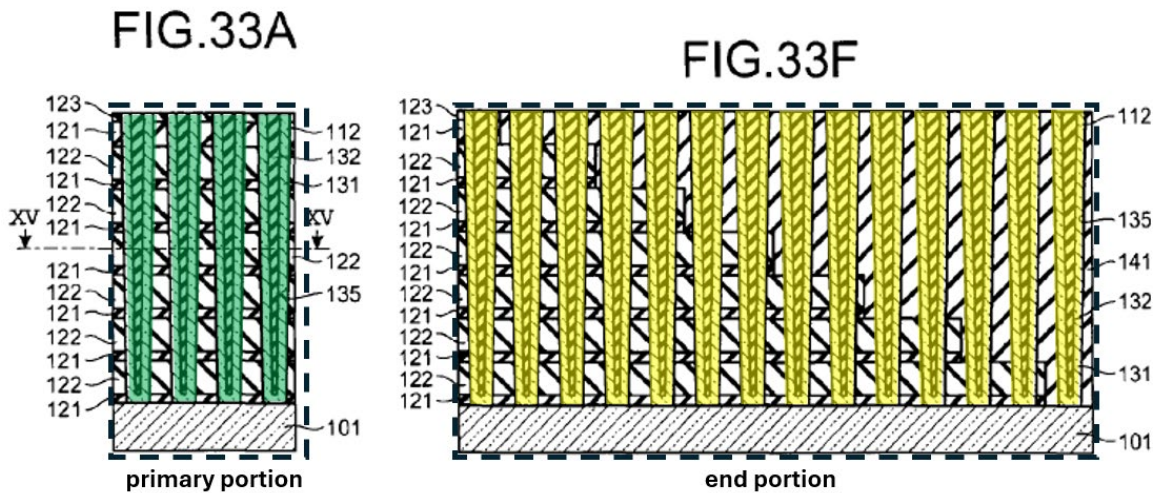
For example, as shown in the sectional view of the memory cell region in annotated FIG. 29C and two sectional views of the word-line contact region in annotated FIGs. 29E and 29D below, Kiyotoshi, in the fourth embodiment, discloses (i) a stack of horizontally extending and vertically overlapping gate electrode films 134 (in red, “*gate lines/features*”), (ii) semiconductor films 131 with dielectric films 132 (in green, collectively “*operative structures*”) extending vertically through gate electrode films 134 in memory cell region 11 (“*primary portion*”), (iii) dummy semiconductor films 131 with dielectric films 132 (in yellow, collectively “*dummy*”

structures”) extending vertically through gate electrode films 134 in word-line contact region 20 (“*end portion*”), and (iv) contacts 145 (in black) in word-line contact region 20 and connecting with individual of gate electrode films 134. EX1005, [0114], [0116]-[0117]; EX1003, ¶86.



Kiyotoshi further discloses the manufacturing process of semiconductor films 131 and dielectric films 132 with respect to the sectional view of the memory cell region in the annotated FIG. 33A and sectional view of the word-line contact region in annotated FIG. 33F below. EX1005, [0118], [0124]-[0125]. Specifically, Kiyotoshi discloses forming semiconductor film 131, such as boron (B)-doped polysilicon, in through-holes 135. EX1005, [0124]. Dielectric film 132, such as silicon oxide, is then formed to fill the inside of the hollow cylindrical semiconductor films 131. EX1005, [0125]. This process simultaneously forms the “*operative*

structures” (in green) and “*dummy structures*” (in yellow) in the memory cell region (FIG. 33A) and word-line contact region (FIG. 33F), respectively, using the same film-forming methods, such as CVD followed by ALD. EX1005, [0124]-[0125]. As a result, the same materials are arranged in the same lateral order. EX1003, ¶87.



EX1003 — FIG. H

B. Dependent Claims 5-8 and 10

As discussed in Sections VII.F-VII.H and VII.J, a POSITA would have understood, or at least found it obvious, that active pillars 224a with charge storage layers 222a (collectively “*operative structures*”) and supporters 224b with charge storage layers 222b (collectively “*dummy structures*”) have the same semiconductor material and charge storage material, arranged in the same lateral order.

To the extent further explicit teaching is required for filling both dummy holes and channel holes using the same materials (for claims 5, 6, 8, and 10) in the same process steps following the same sequence (for claim 7), Kiyotoshi discloses

forming semiconductor films 131 and dielectric films 132 in through-holes 135, both in memory cell region 11 (“*primary portion*”) as “*operative structures*” and in word-line contact region 20 (“*end portion*”) as “*dummy structures*,” using the same materials by the same film forming methods following the same sequence. EX1005, [0124]-[0125]; EX1003, ¶194.

Chae and Kiyotoshi are analogous art, in the same field as the ’737 patent, which relates to nonvolatile memory devices. EX1001, 1:36-39; EX1004, [0002]; EX1005, [0003]. Both Chae and Kiyotoshi are pertinent to the purported problem addressed by the ’737 patent: supporting dielectric layers while removing sacrificial layers between the dielectric layers. EX1001, 7:58-8:2; EX1004, [0129]; EX1005, [0127]; EX1003, ¶195.

Chae discloses that “the dummy holes and the channel holes are filled with semiconductor material to form active pillars 224a and supporters 224b.” EX1004, [0128]. A POSITA would have found it routine, straightforward, and advantageous to apply Kiyotoshi’s express teaching of forming the “*operative structures*” and “*dummy structures*” using the same semiconductor and dielectric materials arranged in the same lateral order to Chae, as it would simplify the process and advantageously reduce the number of processing steps and materials used. EX1003, ¶196. Reducing the number of processing steps would have been advantageous because it would decrease the chance of defects, shorten manufacturing time, and

improve fabrication yield. EX1014, 54; EX1015, [0004], [0108], [0190]; EX1003, ¶197.

A POSITA would have known that such an application, resulting in the claimed limitations, would predictably work and produce the expected structure. EX1003, ¶198. For instance, Kiyotoshi provides guidance on simultaneously filling both dummy holes and channel holes with the same materials, for example, by outlining the viable deposition materials and processes and methods for controlling the shape and thickness of the deposited semiconductor films 131. EX1005, [0124]-[0125]. Given Kiyotoshi's guidance and common knowledge in the art, a POSITA would have a reasonable expectation of success in applying Kiyotoshi's teachings to Chae's device. EX1003, ¶198. While Kiyotoshi discloses forming charge storage layers after filling the holes with semiconductive material (followed by dielectric material), and Chae discloses forming charge storage layers in the holes prior to forming the semiconductive material, a POSITA would have recognized that this difference does not impact the applicability of Kiyotoshi's teaching to Chae about simultaneous formation of the semiconductive material in the holes. EX1003, ¶199. The underlying benefit of depositing the same materials into multiple holes at the same time remains unchanged, regardless of whether the charge storage material is deposited before or after the semiconductor material. EX1003, ¶199.

Thus, Chae in view of Kiyotoshi renders obvious claims 5-8 and 10.

C. Independent Claim 11 and Dependent Claims 12 and 14

Even if the Board narrowly interprets the “*solid material*” in [12] to be distinct from the “*semiconductive material*” in [11.c.2] and [12], and/or the “*cylinder*” in [11.c.2] as “*hollow cylinder*,”⁹ Chae in view of Kiyotoshi still renders obvious “*the dummy structures individually comprising a [hollow] cylinder of semiconductive material*” [11.c.2], “*solid material filling radially internal regions of individual of the hollow cylinders of semiconductive material*” [12], and that “*the operative structures individually comprise a [hollow] cylinder of semiconductor material*” [14].

Kiyotoshi explicitly discloses that semiconductor film 131 (part of “*operative structure*”) in memory cell region 11 (“*primary portion*”) and dummy semiconductor film 131 (part of “*dummy structure*”) in word-line contact region 20 (“*end portion*”) are both “**hollow** cylindrical.” EX1005, [0116]. [0125]. Kiyotoshi also explains the process of forming such a hollow cylindrical shape by depositing using “a film forming method such as the LPCVD method” “in a macaroni shape along the inner surfaces of the through-holes 135.” EX1005, [0124]. Kiyotoshi further discloses that dielectric film 132 (another part of “*operative structure*”) in memory cell region 11 and dielectric film 132 (another part of “*dummy structure*”)

⁹ Petitioner does not concede such an interpretation as discussed in Section VII.L.

in word-line contact region 20 “fill the inside of the hollow cylindrical semiconductor films 131 by the ALD method” using the same dielectric material, such as silicon oxide. EX1005, [0125].

A POSITA reading Kiyotoshi would have found it obvious to apply the same macaroni/hollow cylindrical shape with uniform thickness among the stacked memory cells to Chae’s string of stack memory cells provided by active pillars PL 224a because doing so would improve device performance for various reasons, as detailed below. EX1003, ¶202. It would also have been obvious to a POSITA to fill the remaining space of the channel holes with a different material, such as a dielectric material, as taught by Kiyotoshi, ensuring that the semiconductor material maintains the desired macaroni/hollow cylindrical shape. EX1003, ¶202.

- 1. Kiyotoshi itself provides teaching, suggestions, or motivation that would have led a POSITA to replace Chae’s solid cylindrical semiconductor material in active pillars 224a with Kiyotoshi’s macaroni/hollow cylindrical semiconductor material filled with a dielectric material.**

Kiyotoshi teaches that “[w]hen the semiconductor films 131 are deposited in a macaroni shape, the thickness of the semiconductor films 131 controlled by the gate electrode films 134 is equal among the stacked memory cells MC. ... it is possible to reduce fluctuation in transistor characteristics among the memory cells MC. ... [i]nterference among the memory cells MC in independently writing electrons in the memory cells MC on both sides of one channel (semiconductor film)

less easily occurs.” EX1005, [0124]. That is, Kiyotoshi itself provides teaching, suggestions, or motivation that would have led a POSITA to replace Chae’s solid cylindrical semiconductor material in active pillars 224a with Kiyotoshi’s macaroni/hollow cylindrical semiconductor material filled with a dielectric material, because doing so would improve the characteristic uniformity among memory cells and reduce the interference between memory cells. EX1003, ¶204.

2. The proposed modification is merely the use of Kiyotoshi’s known techniques to improve Chae’s similar nonvolatile memory device in the same way.

It is well known in the semiconductor industry that reducing the thickness of semiconductor bodies of 3D NAND memory cells (or transistors in general) by adopting a macaroni/hollow cylindrical shape can improve the short-channel controllability over sub-threshold characteristics due to the operation as fully-depleted devices. EX1016, 451; EX1017, 903-904; EX1003, ¶205. Additionally, this approach enhances threshold voltage control by reducing the number of grain boundaries. EX1016, 451; EX1003, ¶206. Better controllability of NAND memory cell transistors can be achieved by reducing the thickness of semiconductor material (*e.g.*, silicon) below the depletion width. EX1016, 451. This reduction minimizes the material volume and the total number of traps, making the threshold voltage less sensitive to fluctuation in trap density. EX1016, 451; EX1003, ¶206. Additionally, the hollow center of the semiconductor material can be filled with a dielectric

material, which simplifies the process integration of making the NAND memory devices. EX1016, 451; EX1003, ¶207.

3. A POSITA would have a reasonable expectation of success in applying this modification.

A POSITA would have found it routine, straightforward, and advantageous to apply Kiyotoshi’s teaching of a hollow cylindrical semiconductor film filled with a dielectric material to Chae’s active pillars PL 224a. A POSITA would have known such a combination, yielding the claimed limitations, would provide the expected resulting structure, with a reasonable expectation of success, based on Kiyotoshi’s guidance on the process details and common knowledge in the art. EX1005, [0124]-[0125]; EX1003, ¶208.

Thus, Chae in view of Kiyotoshi renders obvious that “*the operative structures individually comprise a [hollow] cylinder of semiconductor material*” in [14].

Moreover, as discussed in Sections VII.F, VII.G, and VIII.B, Chae alone discloses, suggests, or at least in view of Kiyotoshi suggests, that the same materials fill both the dummy holes and channel holes in the same process steps following the same sequence to form supporters SP 224b and active pillars PL 224a, respectively. Thus, supporter 224b of Chae in the proposed modification/combination would have the same configuration as active pillar 224a—having a hollow cylindrical

semiconductor film and a different material, such as a dielectric material, filling the radially internal region of the hollow cylindrical semiconductor film. EX1003, ¶210.

Chae in view of Kiyotoshi thus also renders obvious “*the dummy structures individually comprising a [hollow] cylinder of semiconductive material*” in [11.c.2] and that “*solid material filling radially internal regions of individual of the [hollow] cylinders of semiconductive material*” in [12].

D. Dependent Claim 15

As discussed in Section VII.N, Chae discloses the additional features recited in claim 15 for the same reason. Thus, Chae in view of Kiyotoshi also renders obvious claim 15.

IX. GROUNDS 4 AND 5: JEONG ANTICIPATES OR OTHERWISE RENDERS OBVIOUS CLAIMS 18 AND 20

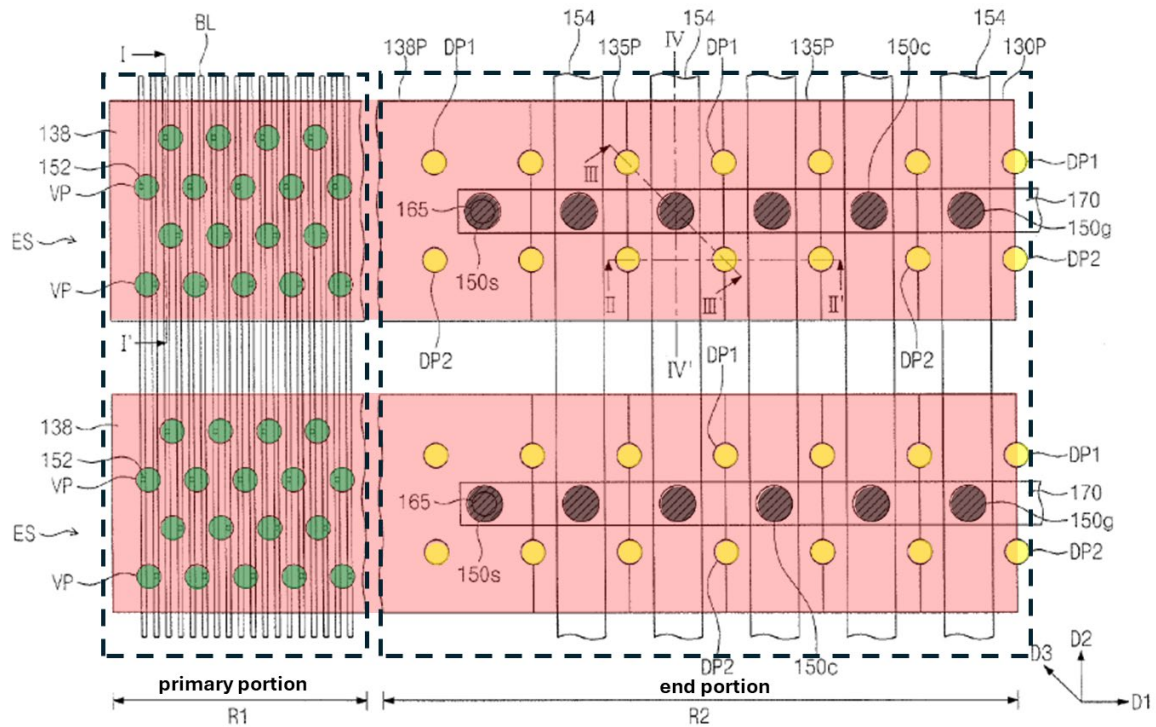
A. Overview of Jeong

Jeong relates to 3D semiconductor devices. EX1006, [0003]. Like the ’737 patent, Jeong discloses that “formation of the dummy pillars DP1 and DP2 through the insulating layers 110 in the second region R2 supports the insulating layers 110 during removal of the sacrificial layers 120, thereby minimizing or preventing the above problems, e.g., misalignment and/or breaking of the insulating layers 110.” EX1006, [0074], [0109]-[0110]; EX1003, ¶89.

As illustrated in the plan view of annotated FIG. 1 and cross-sectional view of annotated FIG. 3¹⁰, a 3D memory device includes electrode structures ES, each including a stack of horizontally extending and vertically overlapping ground selection electrodes 130, cell electrodes 135, and string selection electrodes 138 (in red). EX1006, [0055]-[0056]; EX1003, ¶90. The electrode structure ES includes a first/cell region R1, “in which memory cells are three-dimensionally arranged,” and a second/connection region R2, in which “a stepped structure” of electrodes 130, 135, and 138 is formed. EX1006, [0053], [0055]. The memory device also includes vertical patterns VP (in green) and dummy pillars DP1 and DP2 (in yellow) extending vertically through electrodes 130, 135, and 138 in first/cell region R1 and second/connection region R2, respectively. EX1006, [0058], [0060]. Jeong further discloses contact plugs 150 (in black), each connecting with a respective electrode 130, 135, or 138 in second/connection region R2. EX1006, [0066].

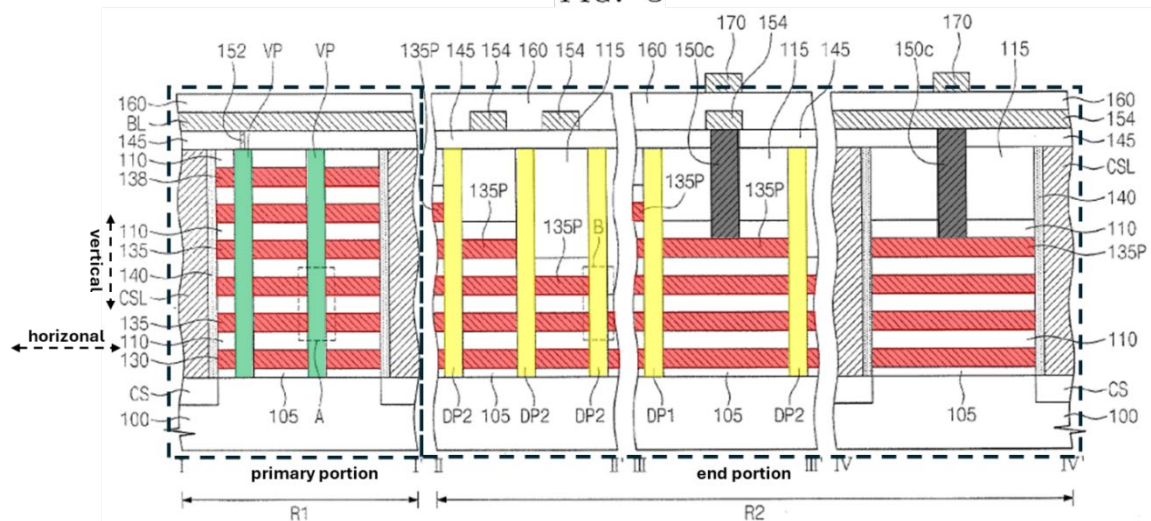
¹⁰ FIG. 3 refers to the same embodiment as FIG. 1 since FIG. 3 is taken along the lines I-I', II-II', III-III', and IV-IV' of FIG. 1. EX1006, [0052].

FIG. 1



EX1003 — FIG. I

FIG. 3

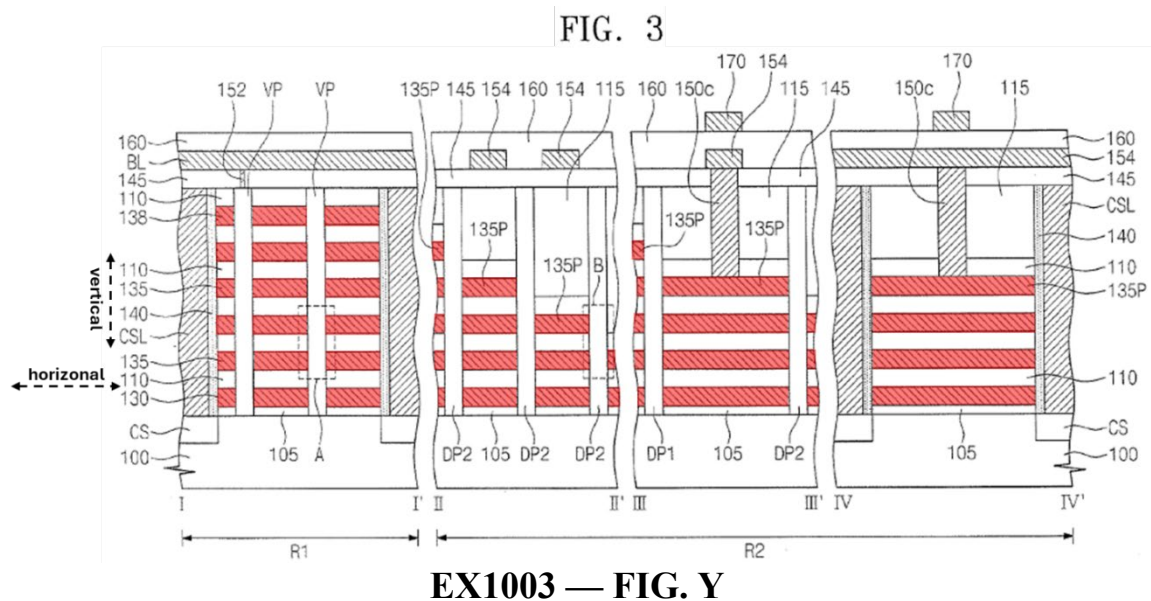


EX1003 — FIG. J

B. Independent Claim 18

1. Jeong discloses a “*stack of horizontally extending and vertically overlapping features*” [18.P].

Jeong discloses an electrode structure ES including a stack of horizontally extending and vertically overlapping electrodes 130, 135, and 138. EX1006, [0055]. As shown in the annotated FIG. 3 below, a stack of electrodes 130, 135, and 138 (in red) extend horizontally and overlap vertically. EX1003, ¶216.



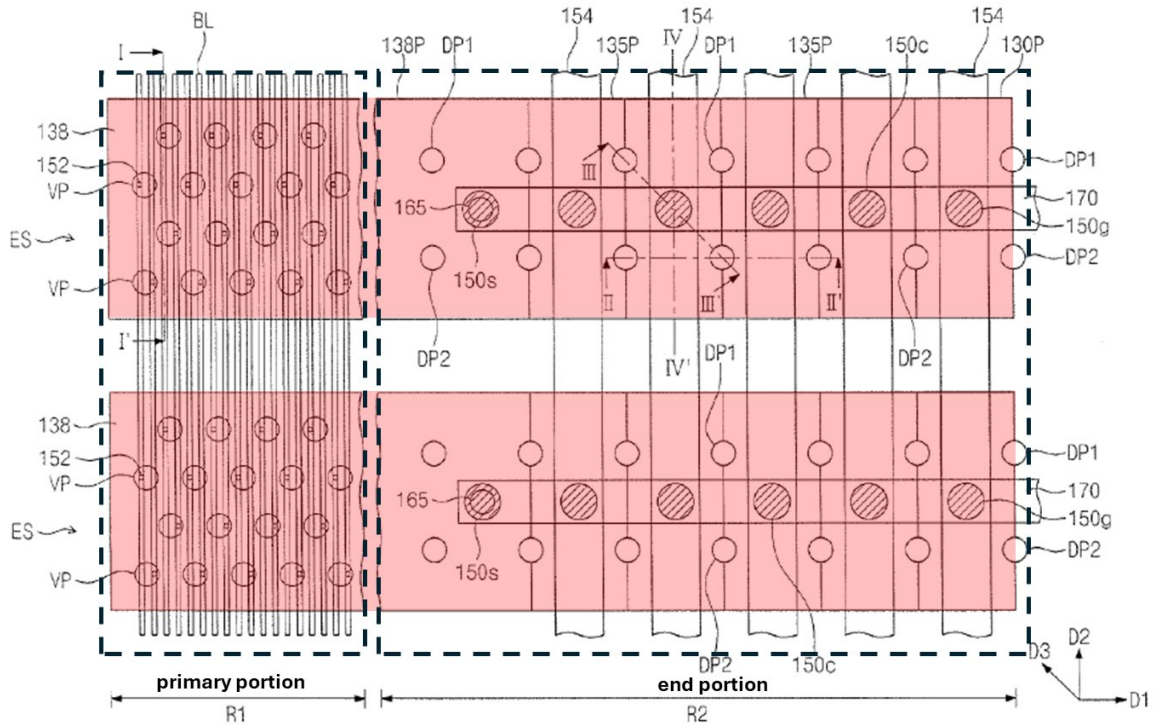
The '737 patent explains that “*features*” may be “horizontally extending lines,” such as horizontally extending conductive lines. EX1001, 11:28-34; *see* Section VII.K.1. Correspondingly, Jeong discloses that “cell electrodes 135 may correspond to word lines, the ground selection electrode 130 may correspond to a ground selection line, and the string selection electrode 138 may correspond to a string selection line.” EX1006, [0070].

Accordingly, a POSITA would have understood that electrodes 130, 135, and 138 (*i.e.*, ground selection lines, word lines, and string selection lines) of Jeong qualify as the claimed “*features*.” EX1003, ¶217. To the extent that the “*features*” require a combination of horizontally extending conductive and dielectric lines (which Petitioner does not concede), each pair of electrode 130, 135, or 138 and insulating layer 110 in Jeong collectively qualifies as one of the “*features*,” which would not affect the mapping of Jeong to any claim limitations related to the “*features*” in Grounds 4 and 5. EX1003, ¶218. Thus, Jeong discloses [1.P].

2. Jeong discloses “*a primary portion and an end portion*” [18.a.1], and “*at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion*” [18.a.2].

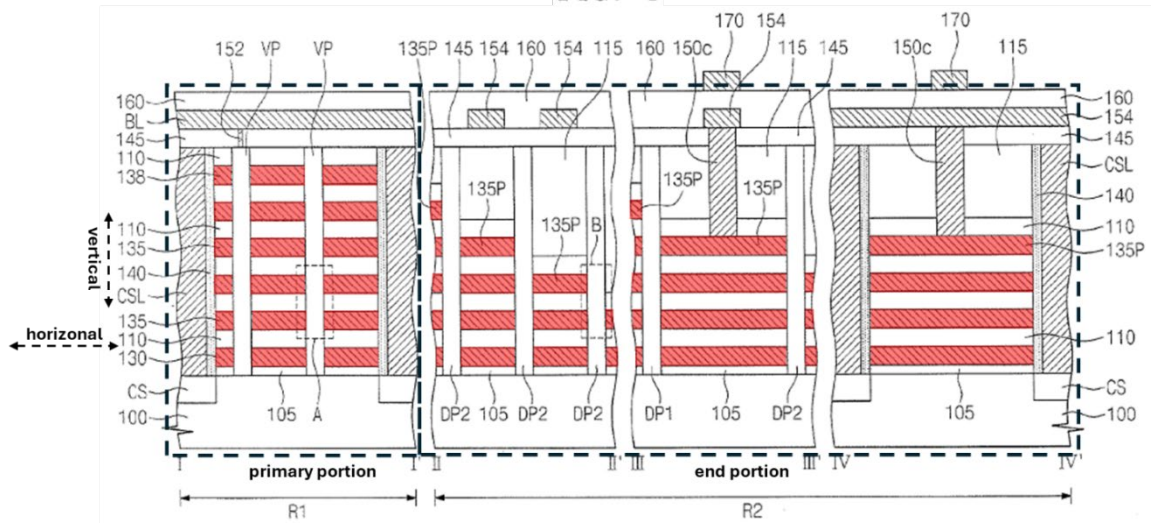
As shown in the plan view of annotated FIG. 1 and the cross-sectional view of annotated FIG. 3 below, the electrode structure ES includes a first/cell region R1 and a second/connection region R2. EX1006, [0053]-[0054]; EX1003, ¶220. A POSITA would have understood that first/cell region R1 is the “*primary portion*” since it is where “memory cells are three-dimensionally arranged,” and that second/connection region R2 is the “*end portion*” since it is located at the end of the electrode structure ES where “pads are provided.” EX1006, [0053]; EX1003, ¶221. Thus, Jeong discloses [18.a.1].

FIG. 1



EX1003 — FIG. Z

FIG. 3



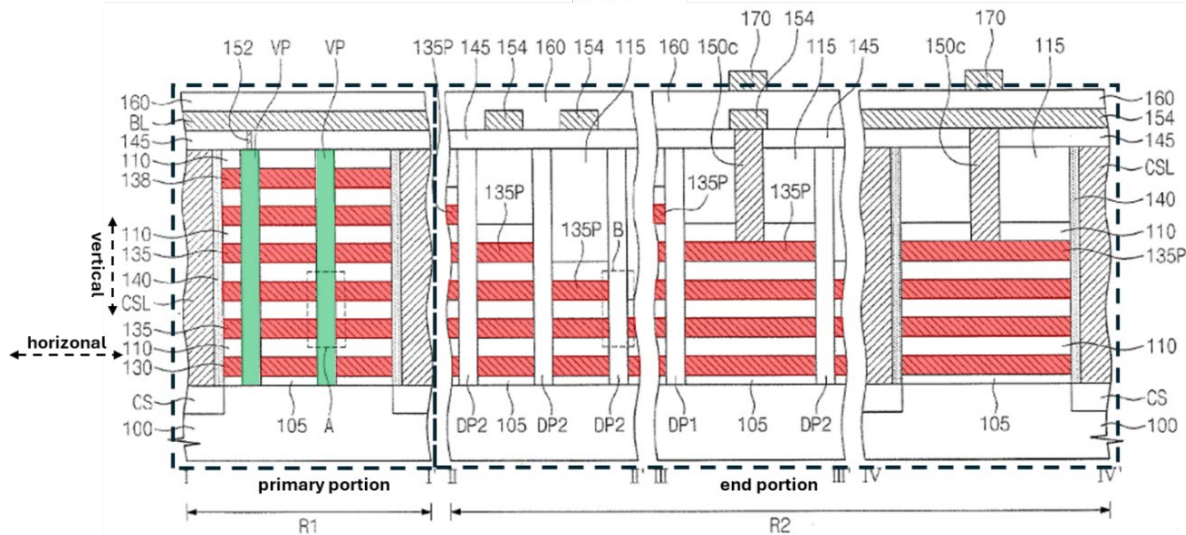
EX1003 — FIG. AA

Jeong further discloses that “electrodes 130, 135, and 138 may respectively include pads 130P, 135P, and 138P that constitute **a stepped structure** in the second region R2.” EX1006, [0055]. As further shown in annotated FIG. 3 above, a POSITA would have understood that in second/connection region R2, an electrode 130, 135, or 138 at a lower level in the vertical direction of the stack (“*moving deeper into the stack*”) extends farther in the horizontal direction. EX1003, ¶223. Thus, Jeong also discloses [18.a.2].

3. Jeong discloses or otherwise renders obvious “*operative structures extending vertically through the features in the primary portion*” [18.b.1], “*the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string*” [18.b.2], and “*at least some of the features comprising control gate lines*” [18.b.3].

As shown in the annotated FIG. 3 below, Jeong discloses vertical patterns VP (in green) extending vertically through electrodes 130, 135, and 138 (in red, “*features*”) in first/cell region R1 (“*primary portion*”). EX1006, [0058]; EX1003, ¶225.

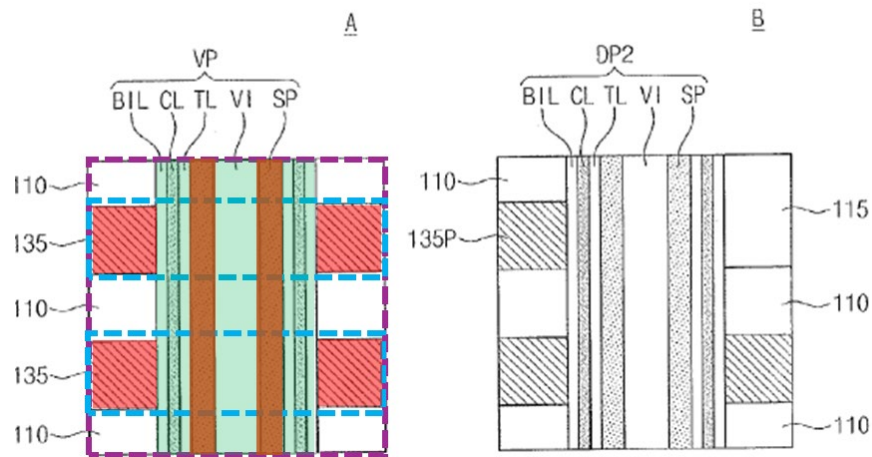
FIG. 3



EX1003 — FIG. AB

Regarding vertical patterns VP, Jeong discloses that “the vertical pattern VP may include a vertical semiconductor pattern SP extending upward from the substrate 100 ... a blocking insulating layer BIL, a charge storage layer CL, and a tunnel insulating layer TL which are disposed between the cell electrode 135 and the vertical semiconductor pattern SP.” EX1006, [0078], *see* [0079], [0082], [0085], [0088], FIGs. 4A-4D. As further shown in annotated FIG. 4A below, a vertical pattern VP (in green) is part of a NAND memory cell string (in purple dashed box), which includes memory cells (in blue dashed boxes). EX1003, ¶227. Thus, a POSITA would have readily appreciated that vertical patterns VP are the “*operative structures*,” which may be “circuit components” according to the ’737 patent. EX1001, 6:22-25; EX1003, ¶228. Thus, Jeong discloses [18.b.1].

FIG. 4A



EX1003 — FIG. AC

Jeong also discloses that vertical patterns VP (“operative structures”) include vertical semiconductor patterns SP. EX1006, [0078]-[0079]. As depicted in annotated FIG. 4A above, a POSITA would have understood, or at least found it obvious, that vertical pattern VP (in green) includes vertical semiconductor patterns SP (in brown), which form “interconnected channels” of the NAND memory cell string (in purple dashed box). EX1003, ¶230. A POSITA would have also understood, or at least found it obvious, that vertical pattern VP includes portions of the memory cells (in blue dashed boxes). EX1003, ¶230. A POSITA would have further understood, or at least found it obvious, that the memory cells are connected vertically in series in the NAND memory cell string and thus, include “a portion of NAND architecture,” which is consistent with the descriptions of “NAND architecture” of the ’737 patent. EX1001, 3:1-5; EX1003, ¶230. Thus, Jeong

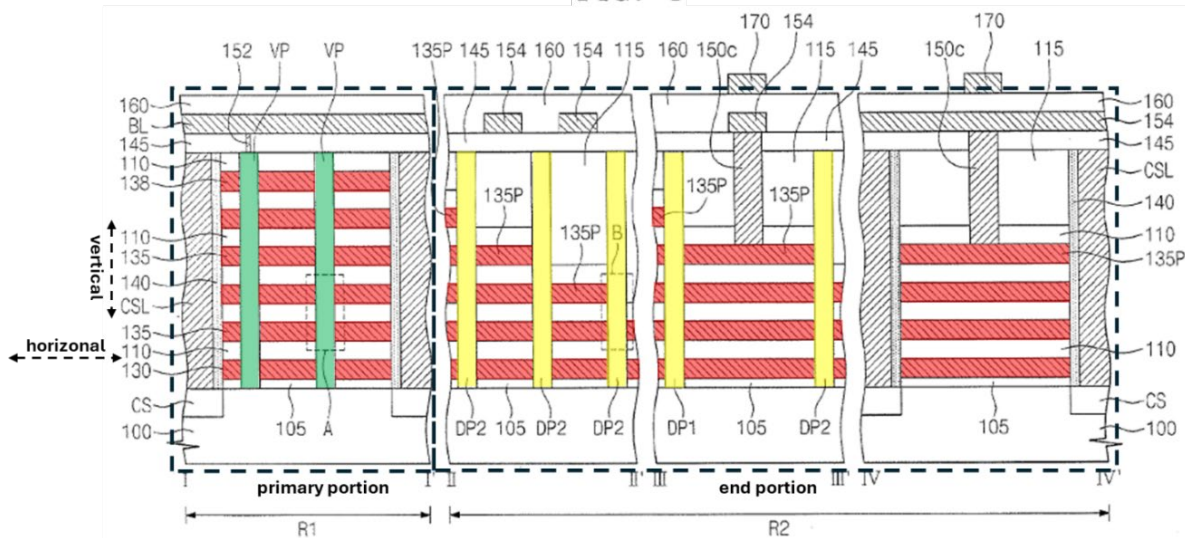
discloses or otherwise renders obvious [18.b.2].

Regarding [18.b.3], a POSITA would have understood that electrodes 130, 135, and 138 (“*features*”), including ground selection electrodes (ground selection lines) 130, string selection electrodes (string selection lines) 138, and cell electrodes (word lines) 135, control ground selection, string selection, and cell operation and thus, include “*control gate lines.*” EX1006, [0056], [0070]; EX1003, ¶233.

4. Jeong discloses “*dummy structures extending vertically through the control gate lines in the end portion*” [18.c].

As shown in the annotated FIG. 3 below, Jeong discloses dummy pillars DP1 and DP2 (in yellow) extending vertically through electrodes 130, 135, and 138 (in red, “*control gate lines*”) in second/connection region R2 (“*end portion*”). EX1006, [0060]-[0061]; EX1003, ¶235.

FIG. 3



EX1003 — FIG. AD

Regarding dummy pillars DP1 and DP2, Jeong discloses that “[w]hen the

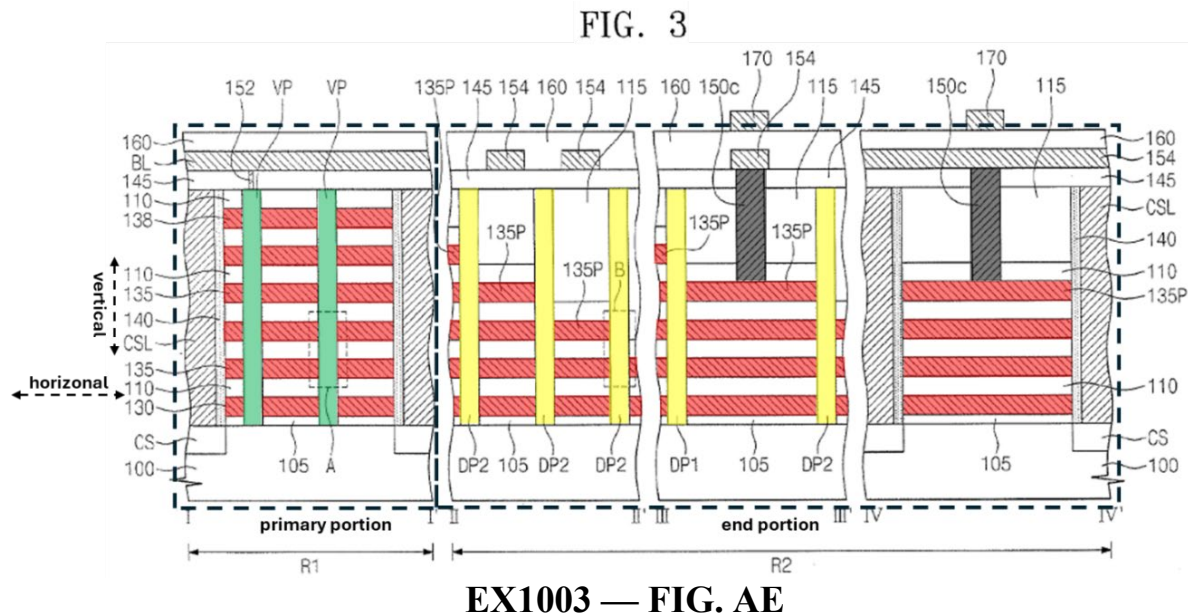
sacrificial layers 120 are removed, the dummy pillars DP1 and DP2 **support** the insulating layers 110 and the capping layer 115 in the second region R2, and the vertical patterns VP may support the insulating layers 110 in the first region R1.” EX1006, [0074], [0109]-[0110]. Jeong also discloses that “dummy pillar DP2 may include the same material as the vertical pattern VP” and “vertical patterns VP and the dummy pillars DP1 and DP2 may be formed at the same time.” EX1006, [0080], [0105]. Thus, a POSITA would have understood that dummy pillars DP1 and DP2 mimic a physical property of vertical patterns VP. EX1003, ¶236.

A POSITA would have also understood, or at least found it obvious, that dummy pillar DP1 or DP2 is an electrically inoperable structure from its name “dummy” and the fact that all dummy pillars DP1 and DP2 are covered by first insulating layer 145 as shown in FIG. 3, instead of conductive contacts such as bit line contact plugs 152. EX1006, FIG. 3; EX1003, ¶237. Therefore, dummy pillars DP1 and DP2 are “*dummy structures*” under the construction of “electrically inoperable structure that mimics a physical property of an operative structure.” See Section VI. Thus, Jeong discloses [18.c].

5. Jeong discloses “*vertical contacts in the end portion connecting with individual of the control gate lines*” [18.d.1], and “*the contacts and dummy structures having different horizontal cross-sections relative one another*” [18.d.2].

Regarding [18.d.1], as shown in annotated FIG. 3 below, Jeong discloses

contact plugs 150 (in black, “vertical contacts”) in second/connection region R2 (“end portion”), each connecting with a respective electrode 130, 135, or 138 (in red, “individual of the control gate lines”). EX1006, [0066]; EX1003, ¶240. Thus, Jeong discloses [18.d.1].



Regarding [18.d.2], Jeong further discloses that dummy pillars DP1 and DP2 (“dummy structures”) and contact plugs 150 (“vertical contacts”) have different sizes, e.g., diameters, from the plan view (“horizontal cross-sections relative one another”). EX1006, claims 25, 34, and 39.

For example, Jeong expressly states, “a size of each of the dummy pillars is smaller than that of each of the contact plugs, when viewed from a plan view” (EX1006, claims 25 and 39), and “a diameter of each of the dummy pillars is less than that of the contact plug, when viewed from a plan view” (EX1006, claim 34).

Thus, Jeong discloses [18.d.2].

From the foregoing, Jeong anticipates or otherwise renders obvious claim 18.

C. Dependent Claim 20

Jeong further discloses that “*the different horizontal cross-sections have different values of total horizontal area relative one another,*” additionally recited in claim 20. As discussed in Section IX.B.5, Jeong discloses that the size in the plan view (“*the total horizontal area*”) of each dummy pillar DP1 or DP2 (“*dummy structure*”) is smaller than that of contact plug 150 (“*vertical contact*”).

X. GROUND 6: CHAE IN VIEW OF HWANG RENDERS OBVIOUS CLAIMS 18 AND 20

Chae in view of Hwang renders obvious claims 18 and 20 under either pre-AIA or AIA 35 U.S.C § 103 regardless of whether claims 18 and 20 of the ’737 patent are entitled to any of its claimed priority dates.

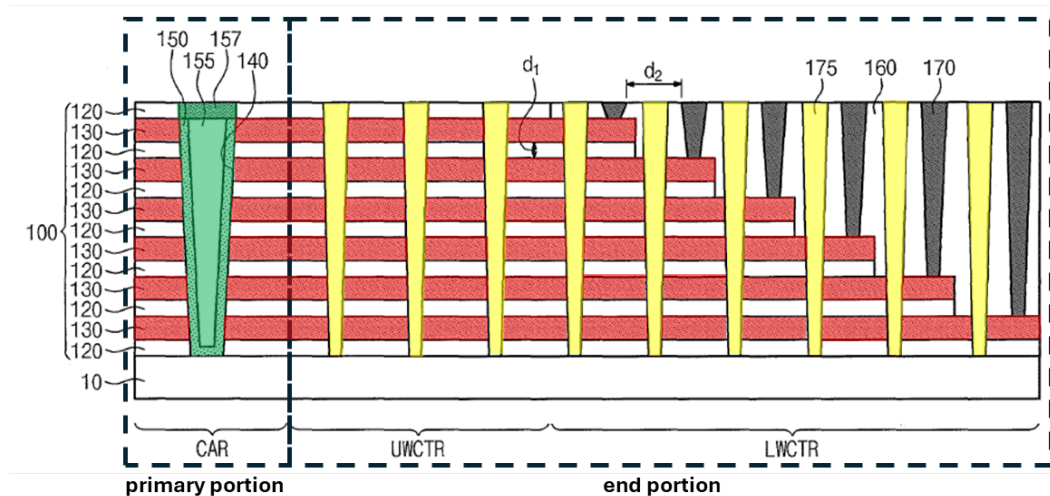
A. Overview of Hwang

Hwang relates to 3D semiconductor devices and manufacturing methods thereof. EX1007, [0002]. Similar to the ’737 patent, Hwang discloses that “supporting members 175 may prevent and/or reduce collapse of the lower inter-layer insulating layers 120 and the lower insulating layers 160 in the subsequent process of removing the lower sacrificial layers 130.” EX1007, [0118], [0120]

[0122]; EX1003, ¶95.

As shown in annotated FIG. 8 below, Hwang discloses, in the modified first embodiment, a 3D memory device having a lower thin film structure 100 including a stack of horizontally extending and vertically overlapping lower sacrificial layers 130 (in red), which are first removed to form lower recess regions 351 and eventually replaced with lower conductive patterns 430 (“gate lines/features”)¹¹. EX1007, [0033], [0080], [0091], [0093], [0119]; EX1003, ¶97.

Fig. 8



EX1003 — FIG. K

As shown in the annotated FIG. 8 above, lower thin film structure 100 includes a cell array region CAR (“primary portion”) where “[m]emory cells with a

¹¹ Since FIGs. 8 and 9, along with their accompanying disclosures, relate to a “modified example of the **first embodiments** of inventive concepts,” a POSITA would have understood that the disclosures of the first embodiments with respect to FIGs. 1-7 are also applicable to the modified first embodiment of FIGs. 8 and 9. EX1007, [0031], [0117]-[0118]; EX1003, ¶96.

three-dimensional structure are formed,” and a lower word line contact region LWCTR (“*end portion*”) “with a terraced shape.” EX1007, [0032], [0036]. The memory device also includes lower semiconductor patterns 150 with buried patterns 155 (in green, “*operative structures*”) and supporting members 175 (in yellow, “*dummy structures*”) extending vertically through lower sacrificial layers 130/lower conductive patterns 430 in cell array region CAR and lower word line contact region LWCTR, respectively. EX1007, [0044], [0050], [0109], [0119]; EX1003, ¶¶98-99.

The annotated FIG. 8 above also shows lower sacrificial contact patterns 170 (in black) in lower word line contact region LWCTR, each connecting with an individual of lower sacrificial layers 130/lower conductive patterns 430. EX1007, [0120]-[0121]. Hwang explains that lower sacrificial contact patterns 170 are first removed to form contact recess regions 353 and eventually replaced with buried contact plugs 450 (“*vertical contacts*”). EX1007, [0080], [0091], [0093]; EX1003, ¶103. Hwang further discloses that “buried contact plugs 450 are ... connected to lower conductive patterns 430, respectively.” EX1007, [0093].

Regarding supporting members 175, Hwang discloses that they are: (i) formed together with lower semiconductor patterns 150 with the same semiconductor material ([0119]), (ii) used to prevent lower inter-layer insulating layers 120 from collapsing in lower word line contact region LWCTR when removing lower sacrificial layers 130, similar to what lower semiconductor patterns 150 do in cell

array region CAR ([0118], [0120], [0122]), and (iii) electrically inoperable because supporting members 175 are covered by upper insulating layer 260, as opposed to conductive wirings such as global word lines or bit lines (FIG. 9). EX1003, ¶¶100-102.

Hwang, in the first embodiment, explicitly teaches that buried contact plugs 450 (“*contacts*”) have a “horizontal cross-section of a substantially **rectangular** shape.” EX1007, [0093], [0114], FIG. 7.

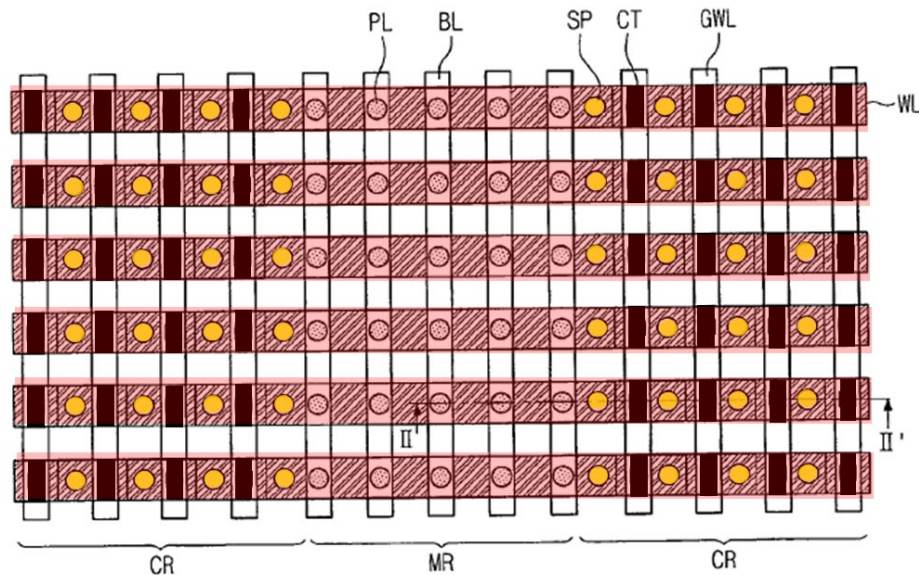
B. Reasons to Combine Chae and Hwang

A POSITA would have found it obvious to combine Chae’s stack with Hwang’s buried contact plugs 450, which have a rectangular horizontal cross-section, to modify Chae’s contact plugs CT to also have a rectangular horizontal cross-section, for the reasons discussed in detail below. EX1003, ¶245.

1. The proposed modification is a simple substitution of Hwang’s rectangular buried contact plugs for Chae’s contact plugs to obtain predictable results.

In a non-limiting example shown below, FIG. AF of Kuhn Decl. modifies FIG. 10 of Chae by making Chae’s contact plugs CT (in black) have a rectangular horizontal cross-section. EX1003, ¶246.

Fig. 10



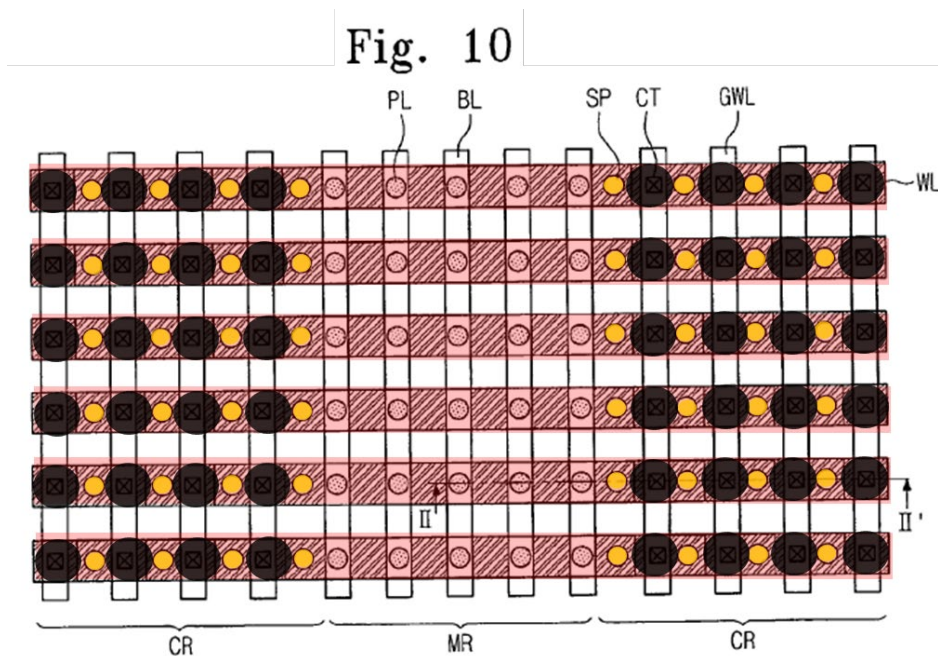
EX1003 — FIG. AF
(Annotated and Modified FIG. 10 of Chae)

The proposed modification is nothing more than a simple substitution of Hwang's rectangular buried contact plugs 450 for Chae's contact plugs CT to yield predictable results—increasing the horizontal area of Chae's contact plugs CT to reduce the resistance, while maintaining adequate margins and safe distances from adjacent supporters SP. EX1003, ¶247.

A POSITA would have been well aware that increasing the horizontal area of a contact plug, such as contact plug CT, reduces its bulk resistance. EX1018, [0032]; EX1003, ¶248. A larger horizontal area also expands the contact interfaces with both the word lines beneath and the global word lines above, effectively lowering contact resistance. EX1003, ¶248. As a result, this modification would improve the overall

electrical performance of the nonvolatile memory device. EX1003, ¶248.

On the other hand, the alternating arrangement of supporters SP and contact plugs CT in a straight horizontal line (*e.g.*, along the line II-II', *see* Section VII.O.5) in Chae imposes constraints on the possible horizontal shapes that contact plugs CT can take when considering resistance reduction through size increase. EX1003, ¶249.

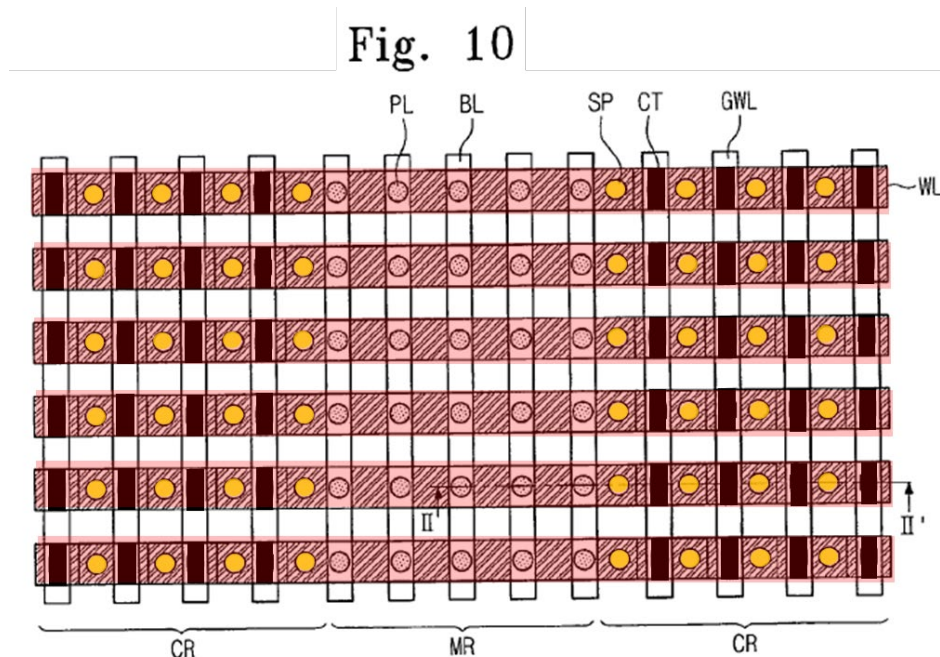


EX1003 — FIG. AH
(Annotated and Modified FIG. 10 of Chae)

As illustrated in another modified FIG. 10 of Chae above, since supporters SP have a circular horizontal cross-section (*see* Section VII.K.4), designing the horizontal cross-section of contact plugs CT to also be circular, like supporters SP, would present challenges. EX1003, ¶249. Specifically, increasing the horizontal area of a circular contact plug CT (by enlarging its diameter) to reduce resistance

would inevitably decrease the distance between adjacent supporters SP and contact plugs CT, increasing the risk of process defects and lowering production yield. EX1003, ¶249.

Thus, a POSITA would have found it obvious to design contact plugs CT with a **non-circular** horizontal cross-section, such as a rectangular shape, as taught by Hwang and shown in the modified FIG. 10 below. EX1003, ¶250.



EX1003 — FIG. AF
(Annotated and Modified FIG. 10 of Chae)

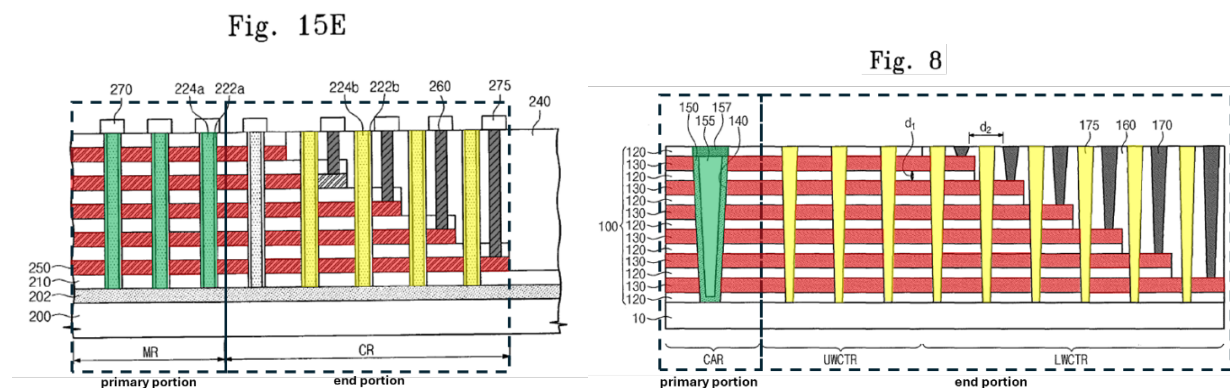
This design allows for an increase in the horizontal area of rectangular contact plug CT by only enlarging one side perpendicular to the line II-II', while preserving the margin between adjacent supporters SP and contact plug CT. EX1003, ¶250. Such a design is particularly advantageous for reducing the size of contact regions

CRs along the word line direction (*i.e.*, the line II-II'), thereby increasing memory cell density. EX1014, 50; EX1003, ¶251.

2. A POSITA would also have a reasonable expectation of success in combining Chae and Hwang.

A POSITA would also have a reasonable expectation of success in combining Chae and Hwang as the proposed combination would yield predictable results.

Chae and Hwang are analogous art, in the same field as the '737 patent, which relates to nonvolatile memory devices. EX1001, 1:36-39; EX1004, [0002]; EX1007, [0002]. Both Chae and Hwang are pertinent to the purported problem addressed by the '737 patent of supporting dielectric layers while removing sacrificial layers between the dielectric layers. EX1001, 7:58-8:2; EX1004, [0129]; EX1007, [0120]; EX1003, ¶252. Moreover, a comparison of FIG. 15E of Chae with FIG. 8 of Hwang below reveals that Chae and Hwang disclose substantially the same stack structure as recited in claim 18. EX1003, ¶253.



EX1003 — FIG. AG
(Comparison of FIG.15E of Chae with FIG. 8 of Hwang)

A POSITA would have found it routine, straightforward, and advantageous to substitute Hwang's rectangular horizontal cross-section design of buried contact plugs 450 in place of Chae's contact plugs CT. EX1003, ¶255. A POSITA would have known such a modification, yielding the claimed limitations, would predictably work and provide the expected resulting structure because both Hwang's buried contact plugs 450 and Chae's contact plugs CT (i) serve the same function—as gate line contacts connecting gate lines to global gate lines, and (ii) are arranged in a similar configuration (comparing FIG. 15E of Chae and FIG. 8 of Hwang). EX1003, ¶254. Therefore, substituting Hwang's rectangular buried contact plugs 450 for Chae's contact plugs CT would yield predictable results of reducing contact resistance without compromising production yield. EX1003, ¶255.

3. The teaching, suggestion, and motivation in Chae and Hwang would have led a POSITA to modify Chae's contact plugs to have a rectangular horizontal cross-section.

Chae's goals include improving the operation speed of its 3D nonvolatile memory device by reducing electrode resistance. EX1004, [0007], [0160]. While Chae proposes various designs to reduce the resistance of gate electrodes/word lines, it remains silent on the design of its contact plugs CT, which serve as the gate line contact structures directly interfacing the gate lines. EX1003, ¶256.

Given this gap in Chae's disclosure and its objectives, a POSITA would have

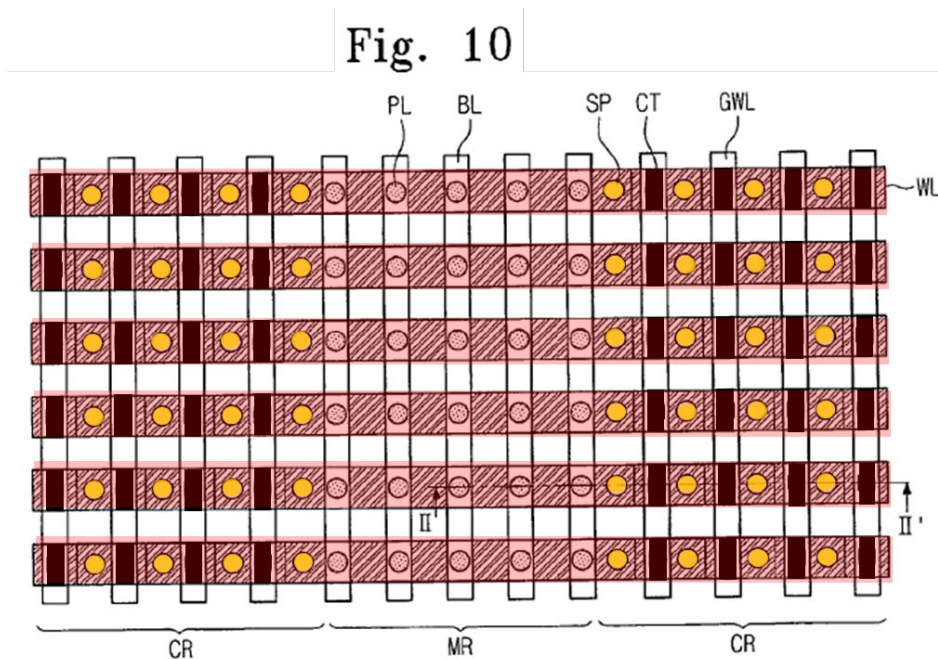
been motivated to explore designs that could also reduce the resistance of Chae's gate line contact plugs CT while remaining compatible with Chae's device. EX1003, ¶257.

Hwang specifically addresses gate line contact structures and provides detailed teachings on various designs, including buried contact plugs 450. EX1007, [0032], [0196]-[0197]; EX1003, ¶258. Hwang explicitly states that “the buried contact plugs 450 may have a horizontal cross-section of a substantially rectangular shape ... the length of one of two sides defining the horizontal cross-section of the rectangular shape may substantially be **the same as the width of the lower conductive pattern 430.**” EX1007, [0114]. A POSITA would have understood that Hwang teaches, or at least suggests, maximizing the horizontal cross-section of buried contact plug 450 to match the width of lower conductive patterns 430 (which serve as gate lines, such as word lines WL). EX1003, ¶258. A POSITA thus would have been motivated to apply Hwang's design to Chae's contact plugs CT to reduce their resistance by increasing the dimension of contact plugs CT. EX1003, ¶258.

Additionally, Hwang explains that “[a]ccording to the modified example, since the sacrificial contact pattern 170 and the supporting member 175 are disposed between the one-sidewalls of the lower sacrificial layers 130 vertically adjacent to each other, the distance d2 between the sacrificial contact patterns 170 may be larger than that of first embodiments of inventive concepts.” EX1007, [0121], FIGs. 2C, 8.

A POSITA would have understood this disclosure to teach, or at least suggest, increasing the distance between adjacent buried contact plugs 450 (which eventually replace sacrificial contact patterns 170) when supporting members 175 are arranged between them. EX1003, ¶259. This would ensure that an adequate distance is maintained between adjacent supporting members 175 and buried contact plugs 450. EX1003, ¶259.

Therefore, a POSITA would have been motivated to adopt the same rectangular design for Chae's contact plugs CT as Hwang's buried contact plugs 450. EX1003, ¶260.



EX1003 — FIG. AF
(Annotated and Modified FIG. 10 of Chae)

As shown in the example modification above, Chae's contact plugs CT (in black) would have a rectangular horizontal cross-section, with one side matching the width of word line WL (in red), while the other side would be smaller to maintain a sufficient distance from adjacent supporters SP (in yellow). EX1003, ¶260. This modification would enhance electrical performance by reducing resistance, while preserving production yield, thereby advancing Chae's goal of improving device operation speed. EX1003, ¶260.

C. Independent Claim 18

1. Chae in view of Hwang discloses [18.P].

Chae discloses [18.P], which is the same as [21.P]. *See* Section VII.O.1.

2. Chae in view of Hwang discloses [18.a].

Chae discloses [18.a], which is the same as [21.a]. *See* Section VII.O.2.

3. Chae in view of Hwang discloses or otherwise renders obvious [18.b].

Chae discloses or otherwise renders obvious [18.b], which is the same as [21.b.1]-[21.b.3]. *See* Section VII.O.3.

4. Chae in view of Hwang discloses [18.c].

Chae discloses [18.c], which is the same as [21.c.1]. *See* Section VII.O.4.

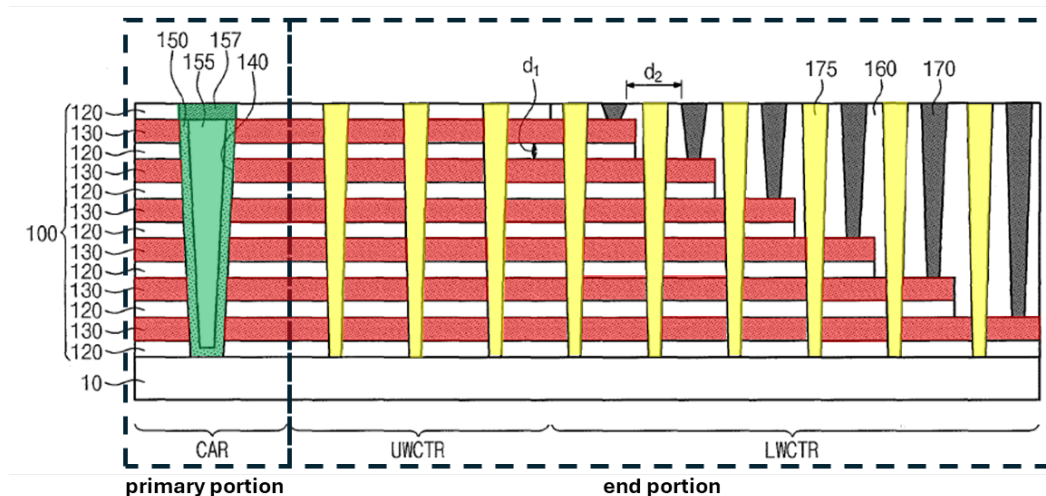
5. Chae in view of Hwang discloses or otherwise renders obvious [18.d.1] and [18.d.2].

Chae discloses [18.d.1], which is the same as [21.d.1]. *See* Section VII.O.5.

Hwang discloses that in lower word line contact region LWCTR (“*end*

portion”), “buried contact plugs 450 [(“vertical contacts”)] are ... connected to lower conductive patterns 430 [(“control gate lines”)], respectively.” EX1007, [0093]; EX1003, ¶262. As shown in the annotated FIG. 8 below, lower sacrificial contact patterns 170 (in black) in lower word line contact region LWCTR each connects with an individual of lower sacrificial layers 130 (in red). Hwang explains that lower sacrificial contact patterns 170 and lower sacrificial layers 130 are eventually replaced with buried contact plugs 450 and lower conductive patterns 430, respectively. EX1007, [0080], [0091], [0093]; EX1003, ¶262; *see* Section X.A. Thus, Hwang also discloses [18.d.1].

Fig. 8



EX1003 — FIG. K

Regarding [18.d.2], as discussed in Section VII.K.4, Chae discloses, or at least suggests, that in the fifth embodiment, supporters SP 224b with charge storage layers 222b (collectively “dummy structures”) have a **circular** horizontal cross-section.

EX1003, ¶263. Hwang, in the first embodiment, explicitly teaches that buried contact plugs 450 (“*contacts*”) have a “horizontal cross-section of a substantially **rectangular** shape.” EX1007, [0093], [0114], FIG. 7.

As discussed above in Section X.B, a POSITA would have found it obvious to modify Chae’s device by incorporating Hwang’s rectangular buried contact plugs 450, resulting in a modified device that includes supporters SP 224b with charge storage layers 222b (collectively “*dummy structures*”) having a **circular** horizontal cross-section, and contact plugs CT 260 (“*contacts*”) having a **rectangular** horizontal cross-section. EX1003, ¶264. Thus, Chae in view of Hwang renders obvious “*the contacts and dummy structures having different horizontal cross-sections relative one another.*”

From the foregoing, Chae in view of Hwang renders obvious claim 18.

D. Dependent Claim 20

As discussed in Section X.B, a POSITA would have found it obvious that, in the combination of Chae and Hwang, the total horizontal area of the rectangular cross-section of contact plugs CT 260 (“*vertical contacts*”) is larger than that of the circular cross-section of supporters SP 224b with charge storage layers 222b (collectively “*dummy structures*”), which would result in contact plugs CT 260 having lower resistance. EX1003, ¶¶265-267; *see* Section X.B.

Therefore, Chae in view of Hwang renders obvious claim 20.

XI. DISCRETION DENIAL DOES NOT APPLY

A. 35 U.S.C. § 325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion to deny institution under 35 U.S.C. § 325(d).

Chae, Jeong, and Hwang have never been presented or otherwise considered by the Office during the original examination of the '737 patent or any parent patents. *See generally* EX1002. None of the grounds raised in this Petition—including the combinations of prior art references, the disclosures of each prior art reference, and the motivations to combine/modify prior art references, as discussed in Sections VII-X—have ever been presented, much less discussed, during the original examination. The disclosures considered by the Examiner in the original examination are not substantially similar to those of the references relied upon in this Petition. *See generally* EX1002.

Even if any of Chae, Jeong, and Hwang, or arguments in this Petition, were considered substantially the same as those raised during the prosecution of the '737 patent or any parent patents, the original Examiner erred in a manner material to the patentability of the challenged claims by not rejecting the challenged claims over the prior art and arguments presented herein. For instance, at least the alleged allowable subject matters related to “*vertical contacts*” in claims 18-22 (*see* Section V.B) are

disclosed or otherwise rendered obvious by Jeong as well as by Chae in view of Hwang, as explained in Grounds 4-6. *See* Sections IX.B.5, IX.C, X.C.5, and X.D.

As to Kiyotoshi, it was cited in an IDS submitted by PO during the prosecution of the '737 patent without any substantive discussion regarding any of the challenged claims. EX1002, 56, 60. Kiyotoshi was also cited in the Notice of Allowance in the file history of the parent '175 patent as one of the three closest prior art references¹² of the allowed claims. EX1019, 22-25.

However, in Ground 3 of this Petition, Kiyotoshi is applied as a secondary reference in combination with Chae, which is neither the same nor substantially the same as Higashi or Uenaka.

To the extent Kiyotoshi was previously presented to the Office, the Office erred in a manner material to the patentability of at least claims 5-8, 10-12, 14, and 15 to which Ground 3 involving Kiyotoshi is applied. Specifically, the Examiner overlooked the disclosures of Kiyotoshi, as demonstrated in Ground 3, that clearly show various alleged allowable subject matters of the parent '175 patent, which are similar to claim limitations recited in claims 5-8, 10-12, 14, and 15 of the '737 patent, including those related to “*control gate lines*,” “*dummy structures*,” and “*a contact*” (EX1019, 22-23). *See* Section VIII.A.

¹² The other two references are U.S. Patent No. 8,426,908 to Higashi (“Higashi”) and U.S. Patent No. 8,581,323 to Uenaka *et al.* (“Uenaka”).

Moreover, the discussion of Kiyotoshi with respect to the challenged claims of the '737 patent was underdeveloped because Kiyotoshi was merely discussed in relation to the claims of the parent '175 patent, which are distinct from the challenged claims of the '737 patent, and was not extensively evaluated for the same purposes upon which Petitioner relies in this Petition. Here, the new and additional evidence and facts presented in Ground 3 regarding Kiyotoshi warrant reconsideration of its relevance to the challenged claims.

B. 35 U.S.C. § 314(a)

As stated in Section II.B, there is no currently pending parallel district court litigation addressing the '737 patent. To the extent the potential addition of the '737 patent to the NDCA case warrants a *Fintiv* analysis¹³, discretionary denial would be improper due to exceptional circumstances. *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020).

As noted above at FN1, after the Court dismissed PO's counterclaims for alleged infringement of the '737 patent with leave to amend, PO declined to amend its pleadings and instead withdrew its assertion of the '737 patent in August 2024. Moreover, minimal investment was made in the '737 patent before its dismissal—

¹³ Petitioner reserves the right to address *Fintiv* in view of the facts and the law as they stand following the POPR, should the PO argue for denial under *Fintiv*.

indeed, PO's counterclaims were dismissed due to deficiencies in pleading infringement. EX1025, 1.

This Petition is being filed before the Court decides whether to allow PO to amend its counterclaims, and PO's motion to reassert the '737 patent was filed only two weeks before this Petition. EX1027. In addition to the compelling merits of the grounds in this Petition—including the anticipation and single-reference obviousness grounds—these exceptional circumstances warrant institution as a matter of fairness.¹⁴

XII. CONCLUSION

Based on the grounds specified above, IPR of all challenged claims is respectfully requested.

¹⁴ To the extent the '737 patent becomes reasserted in the NDCA case, if this IPR is instituted, Petitioner will not pursue the same grounds of invalidity in the district court litigation. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 11-12 (PTAB June 16, 2020).

Respectfully submitted,

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CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

This Petition complies with the requirements of 37 C.F.R. § 42.24. As calculated by the word count feature of Microsoft Word, it contains 13,803 words, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices, Certification Under § 42.24(d), and Certificate of Service.

/Zhiwei Zou/

Zhiwei (Wayne) Zou

Registration No. 66,041

Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing **Petition for *Inter Partes* Review**, **the associated Power of Attorney, and Exhibits 1001-1027** are being served on February 12, 2025, by U.S. Priority Express Mail at the following address of record for the subject patent.

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A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel at the following addresses:

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