

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 10,373,974 B2
APPLICATION NO. : 16/051886
DATED : August 6, 2019
INVENTOR(S) : Eric H. Freeman and Justin B. Dorhout

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification
Column 11, Line 6, change "section line of" to --section line III-III of--

Signed and Sealed this
Tenth Day of September, 2019



Andrei Iancu
Director of the United States Patent and Trademark Office

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Eric H. Freeman et al.

Patent No.: 10,373,974

Issued: August 6, 2019

For: MICROELECTRONIC DEVICES
AND RELATED METHODS

Attorney Docket No.: 2269-P12935.2US
(2015-0059.02/US)

VIA ELECTRONIC FILING

August 13, 2019

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR
PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)**

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is noted that several errors appear in this patent of a typographical nature. These errors are due to mistakes in printing on the part of the U.S. Patent and Trademark Office, and occurred through no fault of the Applicant. A certificate of correction in the form attached hereto is requested.

Please send the Certificate to:

Name: Debra L. Mitchell
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

Patent No. 10,373,974

Attached hereto is Form PTO/SB/44, which is suitable for printing.

Respectfully submitted,

A handwritten signature in cursive script that reads "Debra L. Mitchell".

Debra L. Mitchell
Registration No. 71,683
Agent for Applicant
TRASKBRITT, P.C.
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: August 13, 2019
DLM/slr:cvd

Attachment: PTO/SB/44

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

PATENT NO : 10,373,974 B2
APPLICATION NO. : 16/051,886
ISSUE DATE : August 6, 2019
INVENTOR(S) : Eric H. Freeman and Justin B. Dorhout

Page 1 of 1

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the specification:

COLUMN 11, LINE 6, change "section line of" to --section line III-III of--

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Debra L. Mitchell
TRASKBRITT
230 South 500 East, Suite 300
Salt Lake City, Utah 84102 USA

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS.
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Electronic Acknowledgement Receipt	
EFS ID:	36863800
Application Number:	16051886
International Application Number:	
Confirmation Number:	6336
Title of Invention:	MICROELECTRONIC DEVICES AND RELATED METHODS
First Named Inventor/Applicant Name:	Eric H. Freeman
Customer Number:	63162
Filer:	Debra L. Mitchell/COLETTE DUBOIS
Filer Authorized By:	Debra L. Mitchell
Attorney Docket Number:	2269-12935.2(2015-0059.02
Receipt Date:	13-AUG-2019
Filing Date:	01-AUG-2018
Time Stamp:	17:09:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	Aug-13-2019- Request_COC-12935-2US.pdf	176379	no	3
			36edef43eef3ab80c3916ffc99cd8f8038e8e155		
Warnings:					

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Total Files Size (in bytes):	176379
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/06/2019	10373974	2269-12935.2(2015-0059.02)	6336

63162 7590 07/17/2019

TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)

(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Eric H. Freeman, Kuna, ID;
Micron Technology, Inc., Boise, ID;
Justin B. Dorhout, Boise, ID;

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IR103 (Rev. 10/09)



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/06/2019	10373974	2269-12935.2(2015-0059.02)	6336

63162 7590 07/17/2019

TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

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APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Eric H. Freeman, Kuna, ID;
Micron Technology, Inc., Boise, ID;
Justin B. Dorhout, Boise, ID;

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IR103 (Rev. 10/09)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/01/2018	Eric H. Freeman	2269-12935.2(2015-0059.02	6336
63162	7590	06/17/2019	EXAMINER	
TRASK BRITT, P.C./ MICRON TECHNOLOGY			BERNSTEIN, ALLISON	
P.O. BOX 2550				
SALT LAKE CITY, UT 84110				
			ART UNIT	PAPER NUMBER
			2824	
			NOTIFICATION DATE	DELIVERY MODE
			06/17/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com



UNITED STATES DEPARTMENT OF COMMERCE

U.S. Patent and Trademark Office

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Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
16/051,886	08/01/2018	Freeman et al.	2269-12935.2(2015)

TRASK BRITT, P.C./ MICRON TECHNOLOGY P.O. BOX 2550 SALT LAKE CITY, UT 84110		EXAMINER	
		ALLISON BERNSTEIN	
		ART UNIT	PAPER
		2824	20190612

DATE MAILED: _____

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

/ALLISON BERNSTEIN/ Primary Examiner, Art Unit 2824	12 June 2019

PTO-90C (Rev.04-03)

Response to Rule 312 Communication	Application No. 16/051,886	Applicant(s) Freeman et al.	
	Examiner ALLISON BERNSTEIN	Art Unit 2824	AIA Status Yes
-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address -- 1. ☒ The amendment filed on <u>10 June 2019</u> under 37 CFR 1.312 has been considered, and has been: a) ☐ entered. b) ☒ entered as directed to matters of form not affecting the scope of the invention. c) ☐ disapproved because the amendment was filed after the payment of the issue fee. Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue. d) ☐ disapproved. See explanation below. e) ☐ entered in part. See explanation below. _____			
/ALLISON BERNSTEIN/ Primary Examiner, Art Unit 2824		12 June 2019	

OK TO ENTER: /A.B/

06/12/2019

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Eric H. Freeman et al.

Serial No.: 16/051,886

Filed: August 1, 2018

For: MICROELECTRONIC DEVICES
AND RELATED METHODS (as amended)

Confirmation No.: 6336

Examiner: Allison Bernstein

Group Art Unit: 2824

Attorney Docket No.: 2269-P12935.2US
(2015-0059.02/US)

Notice of Allowance Dated:
April 17, 2019

**VIA ELECTRONIC FILING
June 10, 2019**

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Claims are set forth in the listing of claims that begins on page 2 of this paper; and

Remarks appear on page 7 of this paper.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Eric H. Freeman et al.

Serial No.: 16/051,886

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Attorney Docket No.: 2269-P12935.2US
(2015-0059.02/US)

Notice of Allowance Dated:
April 17, 2019

**VIA ELECTRONIC FILING
June 10, 2019**

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Claims are set forth in the listing of claims that begins on page 2 of this paper; and

Remarks appear on page 7 of this paper.

Amendments to the Claims:

Claim 18 is amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of the Claims:

1. (Previously presented) A microelectronic device comprising:
at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:
an array of memory cells in a memory cell region;
stair step structures in at least one stair step region;
conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region;
access lines extending through the at least one memory block; and
a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.
2. (Previously presented) The microelectronic device of claim 1, wherein the at least one memory block comprises a connection region physically and operatively connecting the adjacent access line portions of the individual access lines to one another, each of the adjacent access line portions separated from one another by the dielectric material.
3. (Previously presented) The microelectronic device of claim 2, wherein four access line portions of a single access line are connected to one another through the connection region, at least two of the four access line portions separated from one another by the dielectric material within an additional slot terminating at the connection region.

4. (Previously presented) The microelectronic device of claim 1, wherein at least some of the stair step structures comprise:
individual tiers aligned at different vertical levels from one another within a respective stair step structure; and
contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.

5. (Previously presented) The microelectronic device of claim 1, wherein the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region.

6. (Previously presented) The microelectronic device of claim 1, wherein a pitch between adjacent access lines in the at least one stair step region is about four times greater than a pitch between the adjacent access lines in the memory cell region.

7. (Previously presented) A method of forming a microelectronic device, the method comprising:
forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region;
forming an array of memory cells in the memory cell region;
forming stair step structures in the stair step region;
forming conductive vias in the via region;
forming access lines extending through the memory block;
forming slots extending between adjacent portions of individual access lines within the stair step region; and
forming a dielectric material within the slots.

8. (Original) The method of claim 7, further comprising forming a connection region within at least some of the access lines, wherein forming the access lines comprises connecting the portions of the individual access lines to one another within the connection region.

9. (Original) The method of claim 7, wherein forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.

10. (Original) The method of claim 7, wherein forming the slots comprises dividing at least some of the individual access lines into four distinct portions.

11. (Original) The method of claim 7, wherein forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots.

12. (Original) The method of claim 7, wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.

13. (Original) The method of claim 7, wherein:
forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials; and
forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

14. (Previously presented) A method of forming a microelectronic device, the method comprising:
forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials;
forming access lines coupled to memory cells of the array of memory cells;
forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;
forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and
removing at least a portion of the stair step structures using at least one chop mask.

15. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.

16. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.

17. (Previously presented) The method of claim 14, wherein forming the at least one stair step region comprises:
forming the stair step mask over the stack while exposing a width of a first step;
removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask;
recessing an edge of the stair step mask to expose a width of a second step; and
removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.

18. (Currently amended) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises: covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop ~~mask;~~mask; and vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed.

19. (Original) The method of claim 14, wherein forming the conductive vias comprises forming at least some of the conductive vias between the array of memory cells and the at least one stair step region.

20. (Original) The method of claim 14, wherein forming the conductive vias comprises forming at least some of the conductive vias between adjacent stair step structures.

REMARKS

No new matter has been added. The amendment to the claims corrects a typographical error, and does not affect the scope of the claims.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required.

Respectfully submitted,

A handwritten signature in cursive script that reads "Debra L. Mitchell".

Debra L. Mitchell
Registration No. 71,683
Agent for Applicant
TRASKBRITT, P.C.
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: June 10, 2019
DLM/cs

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Freeman et al.

Serial No.: 16/051,886

Filed: August 1, 2018

For: MICROELECTRONIC DEVICES
AND RELATED METHODS

Confirmation No.: 6336

Examiner: Allison Bernstein

Group Art Unit: 2824

Attorney Docket No.: 2269-P12935.2US
(2015-0059.02/US)

**VIA ELECTRONIC FILING
June 10, 2019**

COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop Issue Fee
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

This communication is filed in response to the Notice of Allowance dated April 17, 2019 and sets forth Applicant's comments, pursuant to 37 C.F.R. § 1.104(e), on the Examiner's Statement of Reasons for Allowance accompanying the Notice of Allowance and in the Office Action dated March 19, 2019.

In the Notice of Allowance, the Examiner states that "[t]he record as a whole makes clear the reasons for allowability."

In the Office Action dated March 19, 2019, the Examiner states:

The prior art of record fails to teach the claimed limitations in combination namely, a semiconductor device comprising: at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising: an array of memory cells in a memory cell region; *stair step structures in at least one stair step region; conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region; access lines extending through the at least one memory block; and a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region*, as recited in **independent claim 1**; and method of forming a semiconductor device, the method comprising: forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region; forming an array of memory cells in the memory cell region; forming *stair step structures in the stair step region; forming conductive vias in the via region; forming access lines extending through the memory block; forming slots extending between adjacent portions of individual access lines within the stair step region; and forming a dielectric material within the slots*, as recited in **independent claim 7**; and method of forming a memory block of a semiconductor device, the method comprising: forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials; forming access lines coupled to memory cells of the array of memory cells; *forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack; forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and removing at least a portion of the stair step structures using at least one chop mask*, as recited in **independent claim 14**.

Applicant concurs with the reasons as stated by the Examiner insofar as they identify certain claim elements that lend patentability to the claims in combination with other claim elements. However, the scope of the claims is based on the actual language of the claims and equivalents thereof, and not on a selection of certain elements of the claims.

The independent claims as allowed recite elements in addition to those quoted in the Statement of Reasons for Allowance. Furthermore, the dependent claims recite elements in addition to those of the independent claims, which are also not addressed in the Statement of Reasons for Allowance. Such additional elements, in combination with those of the independent claim from which each claim depends, provide additional reasons for patentability. Accordingly,

the scope of the claims must be determined from the literal language of each as a whole, as well as all equivalents thereof.

Therefore, to the extent that the Examiner's reasons for allowance as stated are not relevant to, or wholly encompassing of, a particular claim, independent or dependent, Applicant assumes that (pursuant to 37 C.F.R. § 1.104(e)) the Examiner has determined that the record of the prosecution as a whole of the application makes clear the reasons for allowing those claims. Further, it appears, pursuant to M.P.E.P. 1302.14, that the Examiner's Statement of Reasons for Allowance are not intended to encompass all of the reasons for allowance.

Respectfully submitted,



Debra L. Mitchell
Registration No. 71,683
Agent for Applicant
TRASKBRITT, P.C.
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: June 10, 2019
JAW/KAH/DLM/ljb

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For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

26809

OR



The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	16/051,886

Completed by (check one):



Applicant/Inventor

/Debra L. Mitchell/

Signature



Attorney or Agent of record 71,683

(Reg. No.)

Debra L. Mitchell

Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

801-532-1922

Requester's telephone number



Assignee recorded at Reel _____ Frame _____

June 10, 2019

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.



* Total of _____ forms are submitted.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		16051886		
Filing Date:		01-Aug-2018		
Title of Invention:		MICROELECTRONIC DEVICES AND RELATED METHODS		
First Named Inventor/Applicant Name:		Eric H. Freeman		
Filer:		Debra L. Mitchell/Leah Barrow		
Attorney Docket Number:		2269-12935.2(2015-0059.02		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt	
EFS ID:	36248833
Application Number:	16051886
International Application Number:	
Confirmation Number:	6336
Title of Invention:	MICROELECTRONIC DEVICES AND RELATED METHODS
First Named Inventor/Applicant Name:	Eric H. Freeman
Customer Number:	63162
Filer:	Debra L. Mitchell/Leah Barrow
Filer Authorized By:	Debra L. Mitchell
Attorney Docket Number:	2269-12935.2(2015-0059.02
Receipt Date:	10-JUN-2019
Filing Date:	01-AUG-2018
Time Stamp:	12:58:19
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1000
RAM confirmation Number	061019INTEFSW00012440201469
Deposit Account	201469
Authorized User	Leah Barrow
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)					
37 CFR 1.20 (Post Issuance fees)					
37 CFR 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Jun-10-2019-PartB-12935-2US.pdf	108507	no	1
			c6eec49b88a5c14d34c55a43982a81c76f9244c6		
Warnings:					
Information:					
2		Jun-10-2019-312_Amendment-12935-2US.pdf	110965	yes	7
			47c214ca5c96aafab9412df48901fe7b2c277cd9		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment after Notice of Allowance (Rule 312)		1	1	
	Claims		2	6	
	Applicant Arguments/Remarks Made in an Amendment		7	7	
Warnings:					
Information:					
3	Post Allowance Communication - Incoming	Jun-10-2019-CommentsonReasons-12935-2US.pdf	127852	no	3
			03b11118a4a0e9934c165079f11256329e6a8c9e		
Warnings:					
Information:					
4	Maintenance Fee Address Change	Jun-10-2019-FeeAddress-12935-2US.pdf	204048	no	2
			a5907bc2163c509ef0cbcf15ac9eb8a69d443429		
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30522	no	2
			04a7993b1bf2f66dc42bdc1a54c926c3a0bfdd4bf		

Warnings:	
Information:	
Total Files Size (in bytes):	581894
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

63162 7590 04/17/2019
TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

VIA ELECTRONIC FILING	(Typed or printed name)
	(Signature)
June 10, 2019	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/01/2018	Eric H. Freeman	2269-12935.2(2015-0059.02	6336

TITLE OF INVENTION: MICROELECTRONIC SEMICONDUCTOR DEVICES AND RELATED METHODS (as amended)

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	07/17/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
BERNSTEIN, ALLISON	2824	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 TraskBritt

2

3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Micron Technology, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Boise, ID

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 201469

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Debra L. Mitchell/

Date June 10, 2019

Typed or printed name Debra L. Mitchell

Registration No. 71,683



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/051,886	08/01/2018	2824	1720	2269-12935.2(2015-0059.02	20	3

63162

TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

CONFIRMATION NO. 6336
CORRECTED FILING RECEIPT



0000000108643178

Date Mailed: 06/04/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Eric H. Freeman, Kuna, ID;
Justin B. Dorhout, Boise, ID;

Applicant(s)

Micron Technology, Inc., Boise, ID;

Power of Attorney: The patent practitioners associated with Customer Number 63162

Domestic Priority data as claimed by applicant

This application is a CON of 15/666,064 08/01/2017 PAT 10062708
which is a CON of 14/942,573 11/16/2015 PAT 9728548

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/29/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/051,886**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

MICROELECTRONIC DEVICES AND RELATED METHODS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

63162 7590 04/17/2019
TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

EXAMINER

BERNSTEIN, ALLISON

ART UNIT

PAPER NUMBER

2824

DATE MAILED: 04/17/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/01/2018	Eric H. Freeman	2269-12935.2(2015-0059.02	6336

TITLE OF INVENTION: SEMICONDUCTOR DEVICES AND RELATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	07/17/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

63162 7590 04/17/2019
TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/01/2018	Eric H. Freeman	2269-12935.2(2015-0059.02	6336

TITLE OF INVENTION: SEMICONDUCTOR DEVICES AND RELATED METHODS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	07/17/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
BERNSTEIN, ALLISON	2824	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

- ☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/01/2018	Eric H. Freeman	2269-12935.2(2015-0059.02	6336
63162	7590	04/17/2019	EXAMINER	
TRASK BRITT, P.C./ MICRON TECHNOLOGY			BERNSTEIN, ALLISON	
P.O. BOX 2550			ART UNIT	
SALT LAKE CITY, UT 84110			PAPER NUMBER	
			2824	
DATE MAILED: 04/17/2019				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/051,886	Applicant(s) Freeman et al.	
	Examiner ALLISON BERNSTEIN	Art Unit 2824	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 26 March 2019.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	

/ALLISON BERNSTEIN/ Primary Examiner, Art Unit 2824	4/8/2019
--	----------

DETAILED ACTION

Acknowledgment is made of applicant's amendment, filed on 26 March 2019.

The changes and remarks disclosed therein have been considered.

Claims 1-20 are pending in the application. Claims 1-7 and 14 are currently amended. Claims 1, 7 and 14 are independent claims.

Terminal Disclaimer

The terminal disclaimer filed on 26 March 2019 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US 9,728,548 and US 10,062,708 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Allowable Subject Matter

Claims 1-20 are allowed.

The following is an examiner's statement of reasons for allowance:

The record as a whole makes clear the reasons for allowability.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALLISON BERNSTEIN whose telephone number is (571)272-9011. The examiner can normally be reached on M-F 8AM-5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ALLISON BERNSTEIN/
Primary Examiner, Art Unit 2824
4/8/2019

<i>Search Notes</i> 	Application/Control No. 16/051,886	Applicant(s)/Patent Under Reexamination Freeman et al.
	Examiner ALLISON BERNSTEIN	Art Unit 2824

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11526,11551,11573,11578,11582	03/11/2019	APB
Updated	04/08/2019	APB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
East	03/11/2019	APB
inventor and assignee search	03/11/2019	APB
Updated	04/08/2019	APB

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	H01L27/11526,11551,11573,11578,11582	03/14/2019	APB
	.CLM. search	03/14/2019	APB
	inventor and assignee search	03/14/2019	APB
	Updated	04/08/2019	APB

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Issue Classification 	Application/Control No. 16/051,886	Applicant(s)/Patent Under Reexamination Freeman et al.
	Examiner ALLISON BERNSTEIN	Art Unit 2824

CPC						
Symbol					Type	Version
H01L	/	27	/	11582	F	2013-01-01
H01L	/	27	/	11575	I	2013-01-01
H01L	/	27	/	11573	I	2013-01-01

CPC Combination Sets							
Symbol				Type	Set	Ranking	Version
	/		/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/ALLISON BERNSTEIN/ Primary Examiner, Art Unit 2824	08 April 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20190408

Issue Classification 	Application/Control No. 16/051,886	Applicant(s)/Patent Under Reexamination Freeman et al.
	Examiner ALLISON BERNSTEIN	Art Unit 2824

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L27/11573	/	27	/ 11573
H01L27/11575	/	27	/ 11575
H01L27/11582	/	27	/ 11582
NON-CLAIMED			
	/		/

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/ALLISON BERNSTEIN/ Primary Examiner, Art Unit 2824	08 April 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

U.S. Patent and Trademark Office

Part of Paper No.: 20190408

Issue Classification 	Application/Control No. 16/051,886	Applicant(s)/Patent Under Reexamination Freeman et al.
	Examiner ALLISON BERNSTEIN	Art Unit 2824

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/ALLISON BERNSTEIN/ Primary Examiner, Art Unit 2824	08 April 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	1

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/051,886		Filing Date 08/01/2018		☐ To be Mailed					
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO													
APPLICATION AS FILED - PART I													
		(Column 1)		(Column 2)									
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A							
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A							
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A							
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *				x \$100 =							
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *				x \$460 =							
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL							
APPLICATION AS AMENDED - PART II													
		(Column 1)		(Column 2)		(Column 3)							
AMENDMENT	03/26/2019		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))		* 20		Minus ** 20		= 0		x \$100 =		0		
	Independent (37 CFR 1.16(h))		* 3		Minus *** 3		= 0		x \$460 =		0		
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
										TOTAL ADD'L FEE		0	
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))		*		Minus **		=		x \$0 =				
	Independent (37 CFR 1.16(h))		*		Minus ***		=		x \$0 =				
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
										TOTAL ADD'L FEE		LIE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.										/ROBERT J TALBERT/			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".													
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".													
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed		PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce
Electronic Petition Request	TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	
Application Number	16051886	
Filing Date	01-Aug-2018	
First Named Inventor	Eric Freeman	
Attorney Docket Number	2269-12935.2(2015-0059.02	
Title of Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS	
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action ☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.		
Owner	Percent Interest	
Micron Technology, Inc.	100%	
The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s) 9728548 10062708 as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns. In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later: - expires for failure to pay a maintenance fee; - is held unenforceable; - is found invalid by a court of competent jurisdiction; - is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321; - has all claims canceled by a reexamination certificate; - is reissued; or - is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.		

☒ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request. ☐ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.	
Applicant claims the following fee status: ☐ Small Entity ☐ Micro Entity ☒ Regular Undiscounted	
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.	
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number <u>71683</u> ☐ A sole inventor ☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ☐ A joint inventor; all of whom are signing this request	
Signature	/Debra L. Mitchell/
Name	Debra L. Mitchell

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
 Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal				
Application Number:		16051886		
Filing Date:		01-Aug-2018		
Title of Invention:		SEMICONDUCTOR DEVICES AND RELATED METHODS		
First Named Inventor/Applicant Name:		Eric H. Freeman		
Filer:		Debra L. Mitchell/Catherine Winslow		
Attorney Docket Number:		2269-12935.2(2015-0059.02		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				160

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 16051886

Filing Date: 01-Aug-2018

Applicant/Patent under Reexamination: Freeman

Electronic Terminal Disclaimer filed on March 26, 2019

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt	
EFS ID:	35530559
Application Number:	16051886
International Application Number:	
Confirmation Number:	6336
Title of Invention:	SEMICONDUCTOR DEVICES AND RELATED METHODS
First Named Inventor/Applicant Name:	Eric H. Freeman
Customer Number:	63162
Filer:	Debra L. Mitchell/Catherine Winslow
Filer Authorized By:	Debra L. Mitchell
Attorney Docket Number:	2269-12935.2(2015-0059.02
Receipt Date:	26-MAR-2019
Filing Date:	01-AUG-2018
Time Stamp:	15:34:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 160
RAM confirmation Number	032719INTEFSW00002697201469
Deposit Account	201469
Authorized User	Catherine Winslow
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees) 37 CFR 1.20 (Post Issuance fees) 37 CFR 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33482	no	2
			4c89b5a2a8ba27491b97b6b237d5013aaac4abf6		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30614	no	2
			ab1021d8260423c64323fced3a94a8042fd37437		
Warnings:					
Information:					
Total Files Size (in bytes):			64096		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Eric H. Freeman

Serial No.: 16/051,886

Filed: August 1, 2018

For: SEMICONDUCTOR DEVICES AND
RELATED METHODS

Confirmation No.: 6336

Examiner: Allison Bernstein

Group Art Unit: 2824

Attorney Docket No.: 2269-12935.2US
(2015-0059.02/US)

**VIA ELECTRONIC FILING
March 26, 2019**

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following amendments and remarks are filed in response to the Examiner's remarks in the Office Action of March 19, 2019, the three-month shortened statutory period for response to which expires on June 19, 2019. This response is submitted on or before three months from the date of the Office Action.

Amendments to the Title appear on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims that begins on page 3 of this paper.

Remarks begin on page 8 of this paper.

Electronic Acknowledgement Receipt	
EFS ID:	35533335
Application Number:	16051886
International Application Number:	
Confirmation Number:	6336
Title of Invention:	SEMICONDUCTOR DEVICES AND RELATED METHODS
First Named Inventor/Applicant Name:	Eric H. Freeman
Customer Number:	63162
Filer:	Debra L. Mitchell/Catherine Winslow
Filer Authorized By:	Debra L. Mitchell
Attorney Docket Number:	2269-12935.2(2015-0059.02
Receipt Date:	26-MAR-2019
Filing Date:	01-AUG-2018
Time Stamp:	15:32:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Mar-26-2019- Amendment-12935-2US.pdf	113809	yes	9
			7daf91cdeecf526ad1f5e034d227006a3df417a1		

Multipart Description/PDF files in .zip description			
	Document Description	Start	End
	Applicant Arguments/Remarks Made in an Amendment	8	9
	Claims	3	7
	Specification	2	2
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Warnings:			
Information:			
Total Files Size (in bytes):		113809	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

REMARKS

The Office Action of March 19, 2019 has been received and reviewed. Claims 1 through 20 are currently pending in the application, each of which stands rejected. Claims 1 through 20 have been objected to as being dependent upon rejected base claims, but the indication of allowable subject matter in such claims is noted with appreciation. Applicant has amended claims 1 through 7 and 14. Support for the amendments to independent claims 1, 7, and 14 is found at least in ¶¶ [0003], [0024], and [0025] of the as-filed disclosure. Claims 2 through 6 have been amended for clarity in light of the amendments to claim 1. No new matter has been added. Applicant respectfully requests reconsideration of the application as amended herein in light of the remarks below.

Double Patenting Rejections

Claims 1 through 20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 3, 5, 7, 9, 10, 12, 13, 17, 22, 24 and 25 of U.S. Patent No. 9,728,548 ('548).

Claims 1 through 20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 10,062,708 ('708).

In order to avoid further expenses and time delay, Applicant elects to expedite the prosecution of the present application by filing a terminal disclaimer to obviate the double patenting rejections in compliance with 37 CFR § 1.321 (b) and (c). Applicant's filing of the terminal disclaimer should not be construed as acquiescence to the Examiner's obviousness-type double patenting rejections. The terminal disclaimer and accompanying fee are filed herewith.

CONCLUSION

Claims 1 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, the Examiner is respectfully invited to contact Applicant's undersigned representative.

Respectfully submitted,

A handwritten signature in cursive script that reads "Debra L. Mitchell".

Debra L. Mitchell
Registration No. 71,683
Agent for Applicant
TraskBritt, P.C.
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: March 26, 2019
JAW/DLM/cw

Amendments to the Claims:

Claims 1 through 7 and 14 are amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A ~~semiconductor~~-microelectronic device comprising:
at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:
an array of memory cells in a memory cell region;
stair step structures in at least one stair step region;
conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region;
access lines extending through the at least one memory block; and
a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.
2. (Currently Amended) The ~~semiconductor~~-microelectronic device of claim 1, wherein the at least one memory block comprises a connection region physically and operatively connecting the adjacent access line portions of the individual access lines to one another, each of the adjacent access line portions separated from one another by the dielectric material.
3. (Currently Amended) The ~~semiconductor~~-microelectronic device of claim 2, wherein four access line portions of a single access line are connected to one another through the connection region, at least two of the four access line portions separated from one another by the dielectric material within an additional slot terminating at the connection region.

4. (Currently Amended) The ~~semiconductor~~microelectronic device of claim 1, wherein at least some of the stair step structures comprise: individual tiers aligned at different vertical levels from one another within a respective stair step structure; and contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.

5. (Currently Amended) The ~~semiconductor~~microelectronic device of claim 1, wherein the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region.

6. (Currently Amended) The ~~semiconductor~~microelectronic device of claim 1, wherein a pitch between adjacent access lines in the at least one stair step region is about four times greater than a pitch between the adjacent access lines in the memory cell region.

7. (Currently Amended) A method of forming a ~~semiconductor~~microelectronic device, the method comprising:
forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region;
forming an array of memory cells in the memory cell region;
forming stair step structures in the stair step region;
forming conductive vias in the via region;
forming access lines extending through the memory block;
forming slots extending between adjacent portions of individual access lines within the stair step region; and
forming a dielectric material within the slots.

8. (Original) The method of claim 7, further comprising forming a connection region within at least some of the access lines, wherein forming the access lines comprises connecting the portions of the individual access lines to one another within the connection region.

9. (Original) The method of claim 7, wherein forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.

10. (Original) The method of claim 7, wherein forming the slots comprises dividing at least some of the individual access lines into four distinct portions.

11. (Original) The method of claim 7, wherein forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots.

12. (Original) The method of claim 7, wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.

13. (Original) The method of claim 7, wherein:
forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials; and
forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

14. (Currently Amended) A method of forming a ~~memory block of a semiconductor~~ microelectronic device, the method comprising:
forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials;
forming access lines coupled to memory cells of the array of memory cells;
forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;
forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and
removing at least a portion of the stair step structures using at least one chop mask.

15. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.

16. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.

17. (Previously Presented) The method of claim 14, wherein forming the at least one stair step region comprises:
forming the stair step mask over the stack while exposing a width of a first step;
removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask;
recessing an edge of the stair step mask to expose a width of a second step; and
removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.

18. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises:
covering a first portion of the stair step structures with the at least one chop mask while exposing
a second portion of the stair step structures through the at least one chop mask;
vertically recessing the second portion of the stair step structures such that at least one exposed
tier is removed.

19. (Original) The method of claim 14, wherein forming the conductive vias
comprises forming at least some of the conductive vias between the array of memory cells and
the at least one stair step region.

20. (Original) The method of claim 14, wherein forming the conductive vias
comprises forming at least some of the conductive vias between adjacent stair step structures.

Serial No. 16/051,886

Amendments to the Title:

Please amend the Title as follows:

~~SEMICONDUCTOR~~MICROELECTRONIC DEVICES AND RELATED METHODS



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/051,886	08/01/2018	Eric H. Freeman	2269-12935.2(2015-0059.02	6336
63162	7590	03/19/2019	EXAMINER	
TRASK BRITT, P.C./ MICRON TECHNOLOGY			BERNSTEIN, ALLISON	
P.O. BOX 2550				
SALT LAKE CITY, UT 84110				
			ART UNIT	PAPER NUMBER
			2824	
			NOTIFICATION DATE	DELIVERY MODE
			03/19/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USPTOMail@traskbritt.com

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claims 1-20 are pending in the application.

Information Disclosure Statement

Acknowledgment is made of applicant's Information Disclosure Statement(s) (IDS), Form PTO-1449, filed 01 August 2018. The information therein was considered.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(I)(1) - 706.02(I)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 3, 5, 7, 9, 10, 12, 13, 17, 22, 24 and 25 of U.S. Patent No. 9,728,548 ('548). Although the claims at issue are not identical, they are not patentably distinct from each other because the limitations of the instant application are

recited in the claims of '548 with only nominal differences which would have been obvious to one of ordinary skill in the art.

Claims 1-20 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 10,062,708 ('708). Although the claims at issue are not identical, they are not patentably distinct from each other because the limitations of the instant application are recited in the claims of '708 with only nominal differences which would have been obvious to one of ordinary skill in the art.

Allowable Subject Matter

Claims 1-20 would be allowable if the double patenting rejection set forth in this Office Action is overcome.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach the claimed limitations in combination namely, a semiconductor device comprising: at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising: an array of memory cells in a memory cell region; *stair step structures in at least one stair step region; conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region*; access lines extending through the at least one memory block; and *a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region*, as recited in **independent claim 1**; and method of forming a

semiconductor device, the method comprising: forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region; forming an array of memory cells in the memory cell region; *forming stair step structures in the stair step region; forming conductive vias in the via region; forming access lines extending through the memory block; forming slots extending between adjacent portions of individual access lines within the stair step region; and forming a dielectric material within the slots,* as recited in **independent claim 7**; and method of forming a memory block of a semiconductor device, the method comprising: forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials; forming access lines coupled to memory cells of the array of memory cells; *forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack; forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and removing at least a portion of the stair step structures using at least one chop mask,* as recited in **independent claim 14**.

Conclusion

The examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific

limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALLISON BERNSTEIN whose telephone number is (571)272-9011. The examiner can normally be reached on M-F 8AM-5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic

Application/Control Number: 16/051,886
Art Unit: 2824

Page 7

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ALLISON BERNSTEIN/
Primary Examiner, Art Unit 2824
3/14/2019

Search Notes 	Application/Control No. 16/051,886	Applicant(s)/Patent Under Reexamination Freeman et al.
	Examiner ALLISON BERNSTEIN	Art Unit 2824

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11526,11551,11573,11578,11582	03/11/2019	APB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
East	03/11/2019	APB
inventor and assignee search	03/11/2019	APB

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	H01L27/11526,11551,11573,11578,11582	03/14/2019	APB
	.CLM. search	03/14/2019	APB
	inventor and assignee search	03/14/2019	APB

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Bibliographic Data

Application No: 16/051,886

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No

☐ Met After Allowance

Verified and Acknowledged: /ALLISON BERNSTEIN/

Examiner's Signature

Initials

Title: SEMICONDUCTOR DEVICES AND RELATED METHODS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
08/01/2018	257	2824	2269-12935.2(2015-0059.02
RULE			

APPLICANTS

Micron Technology, Inc., Boise, ID,

INVENTORS

Eric H. Freeman Kuna, ID, UNITED STATES

Justin B. Dorhout Boise, ID, UNITED STATES

CONTINUING DATA

This application is a CON of 15666064 08/01/2017 PAT 10062708

15666064 is a CON of 14942573 11/16/2015 PAT 9728548

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

08/29/2018

STATE OR COUNTRY

UNITED STATES

ADDRESS

TRASK BRITT, P.C./ MICRON TECHNOLOGY

P.O. BOX 2550

SALT LAKE CITY, UT 84110

UNITED STATES

FILING FEE RECEIVED

\$1,720

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	0	("14942573").PN.	US-PGPUB; USPAT	OR	OFF	2016/12/16 15:02
S3	7	((("8507341") or ("8530350") or ("8609536") or ("8693250") or ("20140061747") or ("20140241026") or ("20150001613"))).PN.	US-PGPUB; USPAT	OR	OFF	2016/12/16 15:04
S4	201	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/27 11:55
S5	17439	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/27 13:08
S6	1468	S5 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/27 13:08
S7	893	S5 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/27 13:09
S8	1	("8405142").PN.	US-PGPUB; USPAT	OR	OFF	2016/12/27 17:44
S9	17439	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 12:01
S10	893	S9 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 12:01

S11	17439	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 12:56
S12	893	S11 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 12:56
S13	612	S11 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area) and (distance pitch)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 12:56
S14	128	S11 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area) and (distance pitch) and (isolat\$3 separat\$3 slot trench) near4 (word\$1line "word line")	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 12:58
S15	9	memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area) with (distance pitch) and (isolat\$3 separat\$3 slot trench) near4 (word\$1line "word line")	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 13:08
S16	79	memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area) with (distance pitch)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2016/12/28 13:12
S17	1	("9401309").PN.	US-PGPUB; USPAT	OR	OFF	2016/12/28 17:13
S18	0	("14942573").PN.	US-PGPUB; USPAT	OR	OFF	2016/12/28 18:13
S19	19671	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO;	OR	ON	2017/03/21 13:13

			DERWENT			
S20	137	S19 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical) adj2 (region array area) and (distance pitch) and (isolat\$3 separat\$3 slot trench) near4 (word\$1line "word line")	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/03/21 13:13
S21	28	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 with (oxide dielectric insulat\$3) and (via contact plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and stair	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/03/21 13:17
S22	147	S19 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 with (oxide dielectric insulat\$3) and (contact via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical via) adj2 (region array area) and stair	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/03/21 13:20
S32	72	memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (contact via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (logic peripheral periphery connection via contact logical via) adj2 (region array area) and stair and (slot trench) with (memory array block)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/03/22 06:57
S33	2	("14942573").PN.	US-PGPUB; USPAT	OR	OFF	2017/12/10 13:31
S34	21695	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/12/10 14:34
S35	10	("20120068253" "20130020647" "20140061747" "20140241026" "20150001613" "8405142" "8507341" "8530350" "8609536" "8693250").PN.	US-PGPUB; USPAT	OR	ON	2017/12/10 14:34
S36	75	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 near4 (oxide dielectric insulat\$3) and (via plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (below under underneath sub) near3 (peripheral driver logic control\$5 circuit\$2 array)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/12/10 14:37
S37	1	(13/599793).APP.	USPAT; USOCR	OR	ON	2017/12/10 14:41
S38	10	("20100090286" "20110057249" "20110058418" "20110084397"	US-PGPUB;	OR	ON	2017/12/10 14:43

		"20110115010" "20110244666" "20120061744" "20120306090" "5828621" "6777777").PN. OR ("9595533").URPN.	USPAT; USOCR			
S39	1	(13/774522).APP.	USPAT; USOCR	OR	ON	2017/12/10 14:49
S40	17	("20030072172" "20070252201" "20090268522" "20090310415" "20100258913" "20110084397" "20110244666" "20110286283" "20120007167" "20120091413" "20120119287" "20120306089" "5707885" "7618894" "7669172" "8264866" "8284601").PN. OR ("9111591").URPN.	US- PGPUB; USPAT; USOCR	OR	ON	2017/12/10 14:50
S41	194	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (below under underneath sub) near3 (peripheral driver logic control\$5 circuit\$2 array)	US- PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/12/10 15:10
S42	734	S34 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (below under underneath sub) near3 (peripheral driver logic control\$5 circuit\$2 array)	US- PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/12/10 15:10
S43	0	("9728548").URPN.	USPAT	OR	ON	2017/12/10 15:18
S44	126	S34 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (below under underneath sub) near3 (peripheral driver logic control\$5 circuit\$2 array) and ("stair step" stair\$1step\$3 stair)	US- PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2017/12/10 15:21
S45	22667	H01L27/11526,11551,11573,11578,11582.cpc.	US- PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2018/01/31 06:53
S46	130	S45 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (below under underneath sub) near3 (peripheral driver logic control\$5 circuit\$2 array) and ("stair step" stair\$1step\$3 stair)	US- PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2018/01/31 06:53
S47	197	(micron.as. micron.aanm. freeman-eric\$.in.	US-	OR	ON	2018/01/31

		dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (below under underneath sub) near3 (peripheral driver logic control\$5 circuit\$2 array)	PGPUB; USPAT; FPRS; EPO; JPO; DERWENT			06:53
S52	8	("7972955" "8383512" "8497533" "8557661" "8759217" "9082772" "9257444" "9455268").PN.	US-PGPUB; USPAT	OR	ON	2018/07/23 08:54
S53	20	("20120068253" "20130020647" "20140061747" "20140241026" "20150001613" "7972955" "8383512" "8405142" "8497533" "8507341" "8530350" "8557661" "8609536" "8693250" "8759217" "8933502" "9082772" "9257444" "9449966" "9455268").PN.	US-PGPUB; USPAT	OR	ON	2019/03/11 15:38
S54	3	"16051886"	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2019/03/11 15:57
S55	27017	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2019/03/11 16:08
S56	58	S55 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (separat\$3 spac\$3 trench groove) with (dielectric insulat\$3 oxide)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2019/03/11 16:11
S57	27026	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2019/03/13 09:02
S58	170	S57 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (mask\$3 photo\$1resist)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2019/03/13 09:02
S59	48	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2019/03/13 09:05

		(peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (mask\$3 photo\$1resist)				
S60	28	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (separat\$3 spac\$3 trench groove) with (dielectric insulat\$3 oxide)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	OR	ON	2019/03/13 09:08
S61	2	("14942573").PN.	US-PGPUB; USPAT	OR	OFF	2019/03/13 14:48

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	12405	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT	OR	ON	2019/03/14 08:09
L2	6	L1 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and ((alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (mask\$3 photo\$1resist)).clm.	US-PGPUB; USPAT	OR	ON	2019/03/14 08:09
L3	9	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and ((alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (mask\$3 photo\$1resist)).clm.	US-PGPUB; USPAT	OR	ON	2019/03/14 08:10
S23	9318	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT	OR	ON	2017/03/21 13:19
S24	27	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 with (oxide dielectric insulat\$3) and (via contact plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and stair	US-PGPUB; USPAT	OR	ON	2017/03/21 19:37
S25	9318	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT	OR	ON	2017/03/21 19:37
S26	211	S25 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 with (oxide dielectric insulat\$3) and (via contact plug) and (pillar vertical\$2	US-PGPUB; USPAT	OR	ON	2017/03/21 19:37

		perpendicular\$2) near3 (memory channel active) and stair				
S27	16	(memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 with (oxide dielectric insulat\$3) and (via contact plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and stair).clm.	US-PGPUB; USPAT	OR	ON	2017/03/21 19:37
S28	15	S25 and (memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and alternat\$3 with (oxide dielectric insulat\$3) and (via contact plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and stair).clm.	US-PGPUB; USPAT	OR	ON	2017/03/21 19:39
S29	0	S25 and (memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (via contact plug) near5 (region area) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and stair and (trench slot) with "between" with (memory array block)).clm.	US-PGPUB; USPAT	OR	ON	2017/03/21 19:41
S30	0	(memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (via contact plug) near5 (region area) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and stair and (trench slot) with "between" with (memory array block)).clm.	US-PGPUB; USPAT	OR	ON	2017/03/21 19:41
S31	0	(memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (via contact plug) near5 (region area) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and stair and (trench slot) with (memory array block)).clm.	US-PGPUB; USPAT	OR	ON	2017/03/21 19:42
S48	10646	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT	OR	ON	2018/01/31 13:01
S49	3	S48 and (memory and alternat\$3 with (oxide dielectric insulat\$3) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (stair stair\$1step) with (via contact plug) with distance).clm.	US-PGPUB; USPAT	OR	ON	2018/01/31 13:09
S50	15	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and (memory and alternat\$3 with (oxide dielectric insulat\$3) and (via contact plug) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (stair stair\$1step)).clm.	US-PGPUB; USPAT	OR	ON	2018/01/31 13:10
S51	3	(memory and alternat\$3 with (oxide dielectric insulat\$3) and (pillar vertical\$2 perpendicular\$2) near3 (memory channel active) and (stair stair\$1step) with (via contact plug) with distance).clm.	US-PGPUB; USPAT	OR	ON	2018/01/31 13:11
S62	27	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2	US-PGPUB; USPAT	OR	ON	2019/03/13 18:15

		sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (separat\$3 spac\$3 trench groove) with (dielectric insulat\$3 oxide)				
S63	12377	H01L27/11526,11551,11573,11578,11582.cpc.	US-PGPUB; USPAT	OR	ON	2019/03/13 18:16
S64	57	S63 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (separat\$3 spac\$3 trench groove) with (dielectric insulat\$3 oxide)	US-PGPUB; USPAT	OR	ON	2019/03/13 18:16
S65	46	(micron.as. micron.aanm. freeman-eric\$.in. dorhout-justin\$.in.) and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (mask\$3 photo\$1resist)	US-PGPUB; USPAT	OR	ON	2019/03/13 18:18
S66	168	S63 and memory near4 (vertical\$2 (three adj dimensional\$2) three\$1dimensional\$2) and (alternat\$3 stack\$3) near4 (oxide dielectric insulat\$3) and (via interconnect\$4 plug connection) and (peripheral driver logic control\$5 circuit\$2 sub\$1array array) and ("stair step" stair\$1step\$3 stair) with (mask\$3 photo\$1resist)	US-PGPUB; USPAT	OR	ON	2019/03/13 18:18

3/ 14/ 2019 8:20:25 AM

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Receipt date: 08/01/2018

16/051,886 - GAU: 2824

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)

Approved for use through 11/30/2020. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2018-08-01
	First Named Inventor	Eric H. Freeman	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	2269-12935.2(2015-0059.02)	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7972955		2011-07-05	Choi et al.	
	2	8383512		2013-02-26	Chen et al.	
	3	8405142		2013-03-26	Katsumata et al.	
	4	8497533		2013-07-30	Hyun et al.	
	5	8507341		2013-08-13	Tran et al.	
	6	8530350		2013-09-10	Freeman et al.	
	7	8557661		2013-10-15	Yu et al.	
	8	8609536		2013-12-17	Ha et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		2018-08-01
First Named Inventor	Eric H. Freeman	
Art Unit		
Examiner Name		
Attorney Docket Number		2269-12935.2(2015-0059.02

9	8693250		2014-04-08	Maejima	
10	8759217		2014-06-24	Chen	
11	8933502		2015-01-13	Higashitani et al.	
12	9082772		2015-07-14	Ha et al.	
13	9257444		2016-02-09	Oh et al.	
14	9449966		2016-09-20	Chen	
15	9455268		2016-09-27	Oh et al.	

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	1	20120068253		2012-03-22	Oota et al.	
	2	20130020647		2013-01-24	Hwang et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		
Filing Date		2018-08-01
First Named Inventor	Eric H. Freeman	
Art Unit		
Examiner Name		
Attorney Docket Number		2269-12935.2(2015-0059.02)

	3	20140061747	A1	2014-03-06	Tanzawa et al.	
	4	20140241026	A1	2014-08-28	Tanzawa	
	5	20150001613	A1	2015-01-01	Yip et al.	

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/051,886	08/01/2018	Eric H. Freeman	2269-12935.2(2015-0059.02

CONFIRMATION NO. 6336

63162
TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

PUBLICATION NOTICE



OC000000104269417

Title:SEMICONDUCTOR DEVICES AND RELATED METHODS

Publication No.US-2018-0350836-A1

Publication Date:12/06/2018

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/051,886		Filing Date 08/01/2018		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$	=			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$	=			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL				
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	10/19/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0			X \$100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0			X \$460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA			RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=			X \$	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=			X \$	=
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									
						LIE CORALIA BETANCOURT			

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Freeman et al.

Serial No.: 16/051,886

Filed: August 1, 2018

For: SEMICONDUCTOR DEVICES AND
RELATED METHODS

Confirmation No.: 6336

Examiner: Not yet assigned

Group Art Unit: 2811

Attorney Docket No.: 2269-P12935.2US
(2015-0059.02/US)

VIA ELECTRONIC FILING

October 19, 2018

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Prior to examination of the above-referenced patent application on the merits, entry of the amendments as set forth herein is respectfully solicited.

Amendments to the Specification appear on page 2 of this paper;

Amendments to the Claims are set forth in the listing of the claims that begins on page 3 of this paper; and

Remarks appear on page 8 of this paper.

YMTC EXHIBIT 1002

Page 87 of 158

Amendments to the Specification:

Please amend paragraph [0001] as follows:

[0001] This application is a continuation of U.S. Patent Application Serial No. 15/666,064, filed August 1, 2017, ~~pending~~, now U. S. Patent 10,062,708, issued August 28, 2018, which is a continuation of U.S. Patent Application Serial No. 14/942,573, filed November 16, 2015, now U.S. Patent 9,728,548, issued August 8, 2017, the disclosure of each of which is hereby incorporated herein in its entirety by this reference.

Please amend paragraph [0028] as follows:

[0028] As shown in FIGS. 1 and 2, the slots 114 may be separated from each other by a first distance D_1 in the memory array region 102. In some embodiments, the first distance D_1 may be between about 400 nm and about 1000 nm. As shown in FIG. 1, in the via region 106, at least some of the slots 114 may be separated from each other by a second distance D_2 that is greater than the first distance D_1 . In some embodiments, the second distance D_2 is at least about twice the first distance D_1 , such as about four times the first distance D_1 . The slots 114 may be provided for the introduction of an electrically conductive (e.g., metal) material to be coupled to (e.g., into contact with) the memory cell pillars 108 throughout the memory array region 102 to form conductive ~~access-word~~ lines 116, as will be explained below. The conductive ~~access-word~~ lines 116 are conductive word lines 116 in the embodiments shown herein, although the present disclosure is not so limited. As shown by dashed lines in FIGS. 1 and 2, the conductive word lines 116 may extend along the slots 114 and be coupled to the memory cell pillars 108. In some embodiments, the conductive word lines 116 may include a metal, such as titanium, tantalum, tantalum nitride, tungsten, or tungsten nitride. The conductive word lines 116 and memory cell pillars 108 may form an array of so-called “MONOS” (metal - oxide - nitride - oxide - semiconductor) memory cells. In some embodiments, the memory cells may be so-called “TANOS” (tantalum nitride - aluminum oxide - nitride - oxide - semiconductor) or “BETANOS” (band/barrier engineered TANOS) memory cells, which are subsets of the general category of MONOS memory cells.

Amendments to the Claims:

Claims 4 and 17 are amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of the Claims:

1. (Original) A semiconductor device comprising:
at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:
an array of memory cells in a memory cell region;
stair step structures in at least one stair step region;
conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region;
access lines extending through the at least one memory block; and
a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.
2. (Original) The semiconductor device of claim 1, wherein the at least one memory block comprises a connection region physically and operatively connecting the adjacent access line portions of the individual access lines to one another, each of the adjacent access line portions separated from one another by the dielectric material.
3. (Original) The semiconductor device of claim 2, wherein four access line portions of a single access line are connected to one another through the connection region, at least two of the four access line portions separated from one another by the dielectric material within an additional slot terminating at the connection region.

4. (Currently Amended) The semiconductor device of claim 1, wherein at ~~last~~least some of the stair step structures comprise:
individual tiers aligned at different vertical levels from one another within a respective stair step structure; and
contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.

5. (Original) The semiconductor device of claim 1, wherein the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region.

6. (Original) The semiconductor device of claim 1, wherein a pitch between adjacent access lines in the at least one stair step region is about four times greater than a pitch between the adjacent access lines in the memory cell region.

7. (Original) A method of forming a semiconductor device, the method comprising:
forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region;
forming an array of memory cells in the memory cell region;
forming stair step structures in the stair step region;
forming conductive vias in the via region;
forming access lines extending through the memory block;
forming slots extending between adjacent portions of individual access lines within the stair step region; and
forming a dielectric material within the slots.

8. (Original) The method of claim 7, further comprising forming a connection region within at least some of the access lines, wherein forming the access lines comprises connecting the portions of the individual access lines to one another within the connection region.

9. (Original) The method of claim 7, wherein forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.

10. (Original) The method of claim 7, wherein forming the slots comprises dividing at least some of the individual access lines into four distinct portions.

11. (Original) The method of claim 7, wherein forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots.

12. (Original) The method of claim 7, wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.

13. (Original) The method of claim 7, wherein:
forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials; and
forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

14. (Original) A method of forming a memory block of a semiconductor device, the method comprising:
forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials;
forming access lines coupled to memory cells of the array of memory cells;
forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;
forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and
removing at least a portion of the stair step structures using at least one chop mask.

15. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.

16. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.

17. (Currently Amended) The method of claim 14, wherein forming ~~at least the at least~~ one stair step region comprises:
forming the stair step mask over the stack while exposing a width of a first step;
removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask;
recessing an edge of the stair step mask to expose a width of a second step; and
removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.

18. (Original) The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises:
covering a first portion of the stair step structures with the at least one chop mask while exposing
a second portion of the stair step structures through the at least one chop mask;
vertically recessing the second portion of the stair step structures such that at least one exposed
tier is removed.

19. (Original) The method of claim 14, wherein forming the conductive vias
comprises forming at least some of the conductive vias between the array of memory cells and
the at least one stair step region.

20. (Original) The method of claim 14, wherein forming the conductive vias
comprises forming at least some of the conductive vias between adjacent stair step structures.

REMARKS

Please amend the application as set forth herein prior to examination on the merits. All amendments are made without prejudice or disclaimer, and do not surrender any scope of any claim as originally filed. If questions remain after consideration of the foregoing, the Office is kindly requested to contact applicant's representative at the address or telephone number given herein.

Respectfully submitted,

A handwritten signature in cursive script that reads "Debra L. Mitchell".

Debra L. Mitchell
Registration No. 71,683
Agent for Applicant
TRASKBRITT, P.C.
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: October 19, 2018
DLM/slr

Electronic Acknowledgement Receipt	
EFS ID:	34062314
Application Number:	16051886
International Application Number:	
Confirmation Number:	6336
Title of Invention:	SEMICONDUCTOR DEVICES AND RELATED METHODS
First Named Inventor/Applicant Name:	Eric H. Freeman
Customer Number:	63162
Filer:	Debra L. Mitchell/Deidra Pfeil
Filer Authorized By:	Debra L. Mitchell
Attorney Docket Number:	2269-12935.2(2015-0059.02
Receipt Date:	19-OCT-2018
Filing Date:	01-AUG-2018
Time Stamp:	14:48:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Oct-19-2018- PreliminaryAmendment-12935- 2US.pdf	101767 73f485d304a23d7214635af5813111dbfe739d30	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Preliminary Amendment	1	1
	Specification	2	2
	Claims	3	7
	Applicant Arguments/Remarks Made in an Amendment	8	8
Warnings:			
Information:			
Total Files Size (in bytes):		101767	
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PATENT APPLICATION FEE DETERMINATION RECORD						Application or Docket Number 16/051,886				
Substitute for Form PTO-875										
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760			
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 460 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
			TOTAL			TOTAL	1720			
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
						TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/051,886	08/01/2018	2811	1720	2269-12935.2(2015-0059.02	20	3

CONFIRMATION NO. 6336

FILING RECEIPT



0000000101948258

63162

TRASK BRITT, P.C./ MICRON TECHNOLOGY
P.O. BOX 2550
SALT LAKE CITY, UT 84110

Date Mailed: 08/31/2018

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Inventor(s)

Eric H. Freeman, Kuna, ID;
Justin B. Dorhout, Boise, ID;

Applicant(s)

Micron Technology, Inc., Boise, ID;

Power of Attorney: The patent practitioners associated with Customer Number 63162

Domestic Priority data as claimed by applicant

This application is a CON of 15/666,064 08/01/2017 PAT 10062708
which is a CON of 14/942,573 11/16/2015 PAT 9728548

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/29/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/051,886**

Projected Publication Date: 12/06/2018

Non-Publication Request: No

Early Publication Request: No

Title

SEMICONDUCTOR DEVICES AND RELATED METHODS

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Application Number	
Filing Date	2018-08-01
First Named Inventor	Eric H. Freeman
Title	SEMICONDUCTOR DEVICES AND RELATED METHODS
Art Unit	
Examiner Name	
Attorney Docket Number	2269-12935.2(2015-0059.02)

SIGNATURE of Applicant or Patent Practitioner

Signature	/Debra L. Mitchell/	Date (Optional)	2018-08-01
Name	Debra L. Mitchell	Registration Number	71683
Title (if Applicant is a juristic entity)	Patent Practitioner (Agent for Applicant)		
Applicant Name (if Applicant is a juristic entity)	Micron Technology, Inc.		
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
☐ *Total of _____ forms are submitted.			

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

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- OR
- ☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

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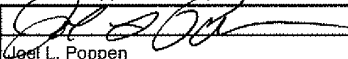
I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Micron Technology, Inc.

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	7/9/14
Name	Jeff L. Poppen		
Title	VP of Legal Affairs, General Counsel and Corporate Secretary		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)

Approved for use through 11/30/2020. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2018-08-01
	First Named Inventor	Eric H. Freeman	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	2269-12935.2(2015-0059.02)	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7972955		2011-07-05	Choi et al.	
	2	8383512		2013-02-26	Chen et al.	
	3	8405142		2013-03-26	Katsumata et al.	
	4	8497533		2013-07-30	Hyun et al.	
	5	8507341		2013-08-13	Tran et al.	
	6	8530350		2013-09-10	Freeman et al.	
	7	8557661		2013-10-15	Yu et al.	
	8	8609536		2013-12-17	Ha et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2018-08-01
	First Named Inventor	Eric H. Freeman	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	2269-12935.2(2015-0059.02	

	9	8693250		2014-04-08	Maejima	
	10	8759217		2014-06-24	Chen	
	11	8933502		2015-01-13	Higashitani et al.	
	12	9082772		2015-07-14	Ha et al.	
	13	9257444		2016-02-09	Oh et al.	
	14	9449966		2016-09-20	Chen	
	15	9455268		2016-09-27	Oh et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS

Remove

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20120068253		2012-03-22	Oota et al.	
	2	20130020647		2013-01-24	Hwang et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2018-08-01
	First Named Inventor	Eric H. Freeman	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	2269-12935.2(2015-0059.02)	

	3	20140061747	A1	2014-03-06	Tanzawa et al.	
	4	20140241026	A1	2014-08-28	Tanzawa	
	5	20150001613	A1	2015-01-01	Yip et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button.

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		

If you wish to add additional non-patent literature document citation information please click the Add button.

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2018-08-01
	First Named Inventor	Eric H. Freeman	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	2269-12935.2(2015-0059.02	

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		
	Filing Date		2018-08-01
	First Named Inventor	Eric H. Freeman	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	2269-12935.2(2015-0059.02)	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Debra L. Mitchell/	Date (YYYY-MM-DD)	2018-08-01
Name/Print	Debra L. Mitchell	Registration Number	71683

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SEMICONDUCTOR DEVICES AND RELATED METHODS		
First Named Inventor/Applicant Name:		Eric H. Freeman		
Filer:		Debra L. Mitchell/Deidra Pfeil		
Attorney Docket Number:		2269-12935.2(2015-0059.02		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1720

Electronic Acknowledgement Receipt	
EFS ID:	33344530
Application Number:	16051886
International Application Number:	
Confirmation Number:	6336
Title of Invention:	SEMICONDUCTOR DEVICES AND RELATED METHODS
First Named Inventor/Applicant Name:	Eric H. Freeman
Customer Number:	63162
Filer:	Debra L. Mitchell/Deidra Pfeil
Filer Authorized By:	Debra L. Mitchell
Attorney Docket Number:	2269-12935.2(2015-0059.02
Receipt Date:	01-AUG-2018
Filing Date:	
Time Stamp:	14:33:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$1720
RAM confirmation Number	080218INTEFSW14362800
Deposit Account	201469
Authorized User	Deidra Pfeil
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)					
37 CFR 1.20 (Post Issuance fees)					
37 CFR 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	Aug-01-2018-Application-Data-Sheet-12935-2US.pdf	1794593	no	8
			444e64ed76661560a8a4c712c5287d61f704eb2f		
Warnings:					
Information:					
2		Aug-01-2018-Application-12935-2US.pdf	168442	yes	24
			66dd81222f9c6ea27d9e6ffeeb6b356c685832c6		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Abstract		24	24	
	Claims		20	23	
	Specification		1	19	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	Aug-01-2018-Drawings-12935-2US.pdf	129422	no	8
			98ae16f7a012b64a4b8aec33f079d7fcbeca33f1		
Warnings:					
Information:					
4	Oath or Declaration filed	Aug-01-2018-Declaration-12935-2US.pdf	214861	no	2
			a47fa0ffa4204b38f69a0900d03cae07fed7bac		
Warnings:					
Information:					
5	Power of Attorney	Aug-01-2018-POA-12935-2US.pdf	210607	no	2
			777bf83f0dee793bc39ad1479ad9ad14981fe63c		

Warnings:					
Information:					
6	Information Disclosure Statement (IDS) Form (SB08)	Aug-01-2018-IDS-12935-2US. pdf	1083157 3ff10b1c7dc6f48aaa02b2e704d8ec19182f115	no	6
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	34955 bea599bbe65adff86ba7f491122bb2e8496947fbb	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			3636037		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2269-12935.2(2015-0059.02)
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor	1				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Eric	H.	Freeman		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Kuna	State/Province	ID	Country of Residence	US
Mailing Address of Inventor:					
Address 1	1250 South Luker Road				
Address 2					
City	Kuna	State/Province	ID		
Postal Code	83634	Country	i	US	
Inventor	2				Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Justin	B.	Dorhout		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Boise	State/Province	ID	Country of Residence	US
Mailing Address of Inventor:					
Address 1	P.O. Box 8023				
Address 2					
City	Boise	State/Province	ID		
Postal Code	83707	Country	i	US	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					
Add					

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2269-12935.2(2015-0059.02)
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS		

☐ An Address is being provided for the correspondence information of this application.

Customer Number	63162		
Email Address	usptomail@traskbritt.com	Add Email	Remove Email

Application Information:

Title of the Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS		
Attorney Docket Number	2269-12935.2(2015-0059.02)	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	63162		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2269-12935.2(2015-0059.02)
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	15666064	2017-08-01		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15666064	Continuation of	14942573	2015-11-16	9728548	2017-08-08
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)	Remove
Additional Foreign Priority Data may be generated within this form by selecting the Add button.				Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2269-12935.2(2015-0059.02)
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2269-12935.2(2015-0059.02)
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant	1		Remove
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	2269-12935.2(2015-0059.02)
		Application Number	
Title of Invention	SEMICONDUCTOR DEVICES AND RELATED METHODS		

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ABSTRACT

Vertical memory blocks for semiconductor devices include a memory cell region including an array of memory cell pillars and at least one via region including a dielectric stack of alternating dielectric materials and at least one conductive via extending through the dielectric stack.

Semiconductor devices including a vertical memory block include at least one vertical memory block, which includes slots extending between adjacent memory cells of a three-dimensional array.

The slots are separated by a first distance in a first portion of the block, and by a second, greater distance in a second portion of the block. Methods of forming vertical memory blocks include forming slots separated by a first distance in a memory array region and by a second, greater distance in a via region. At least one conductive via is formed through a stack of alternating first and second dielectric materials in the via region.

CLAIMS

What is claimed is:

1. A semiconductor device comprising:
at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:
an array of memory cells in a memory cell region;
stair step structures in at least one stair step region;
conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region;
access lines extending through the at least one memory block; and
a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.
2. The semiconductor device of claim 1, wherein the at least one memory block comprises a connection region physically and operatively connecting the adjacent access line portions of the individual access lines to one another, each of the adjacent access line portions separated from one another by the dielectric material.
3. The semiconductor device of claim 2, wherein four access line portions of a single access line are connected to one another through the connection region, at least two of the four access line portions separated from one another by the dielectric material within an additional slot terminating at the connection region.
4. The semiconductor device of claim 1, wherein at least some of the stair step structures comprise:
individual tiers aligned at different vertical levels from one another within a respective stair step structure; and
contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.

5. The semiconductor device of claim 1, wherein the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region.

6. The semiconductor device of claim 1, wherein a pitch between adjacent access lines in the at least one stair step region is about four times greater than a pitch between the adjacent access lines in the memory cell region.

7. A method of forming a semiconductor device, the method comprising:
forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region;
forming an array of memory cells in the memory cell region;
forming stair step structures in the stair step region;
forming conductive vias in the via region,
forming access lines extending through the memory block;
forming slots extending between adjacent portions of individual access lines within the stair step region; and
forming a dielectric material within the slots.

8. The method of claim 7, further comprising forming a connection region within at least some of the access lines, wherein forming the access lines comprises connecting the portions of the individual access lines to one another within the connection region.

9. The method of claim 7, wherein forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.

10. The method of claim 7, wherein forming the slots comprises dividing at least some of the individual access lines into four distinct portions.

11. The method of claim 7, wherein forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots.

12. The method of claim 7, wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.

13. The method of claim 7, wherein:
forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials; and
forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

14. A method of forming a memory block of a semiconductor device, the method comprising:
forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials;
forming access lines coupled to memory cells of the array of memory cells;
forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;
forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and
removing at least a portion of the stair step structures using at least one chop mask.

15. The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.

16. The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.

17. The method of claim 14, wherein forming at least one stair step region comprises: forming the stair step mask over the stack while exposing a width of a first step; removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask; recessing an edge of the stair step mask to expose a width of a second step; and removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.

18. The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises: covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask; vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed.

19. The method of claim 14, wherein forming the conductive vias comprises forming at least some of the conductive vias between the array of memory cells and the at least one stair step region.

20. The method of claim 14, wherein forming the conductive vias comprises forming at least some of the conductive vias between adjacent stair step structures.

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APPLICATION FOR UNITED STATES LETTERS PATENT

for

SEMICONDUCTOR DEVICES AND RELATED METHODS

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TITLE
SEMICONDUCTOR DEVICES AND RELATED METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application Serial No. 15/666,064, filed August 1, 2017, pending, which is a continuation of U.S. Patent Application Serial No. 14/942,573, filed November 16, 2015, now U.S. Patent 9,728,548, issued August 8, 2017, the disclosure of each of which is hereby incorporated herein in its entirety by this reference.

FIELD

[0002] Embodiments of the present disclosure relate to semiconductor devices including vertical memory block constructions that include slots for forming conductive elements within the vertical memory block. Embodiments of the present disclosure also relate to vertical memory blocks that include conductive through-array vias.

BACKGROUND

[0003] A continuing goal of the semiconductor industry has been to increase the memory density (e.g., the number of memory cells per memory die) of memory devices, such as non-volatile memory devices (e.g., NAND Flash memory devices). One way of increasing memory density in non-volatile memory devices is to utilize vertical memory array (also referred to as a “three-dimensional (3D) memory array”) architectures. A conventional vertical memory array includes semiconductor pillars extending through openings in tiers of conductive structures (e.g., word line plates, control gate plates, access lines, word lines) and dielectric materials at each junction of the semiconductor pillars and the conductive structures. Such a configuration permits a greater number of transistors to be located in a unit of die area by building the array upwards (e.g., vertically) on a die, as compared to structures with conventional planar (e.g., two-dimensional) arrangements of transistors.

[0004] Conventional vertical memory arrays include tiers of conductive structures (e.g., access lines, word lines) separated by dielectric materials. One such vertical memory array is a so-called “MONOS” type memory array, which stands for metal – oxide – nitride – oxide – semiconductor, referring to the materials forming each individual memory cell. Conventional

MONOS type memory arrays may be formed by forming the semiconductor pillars through a stack of alternating first and second dielectric materials, forming slots through the stack adjacent to the semiconductor pillars, removing the second dielectric materials through the slots, and replacing the second dielectric materials with a conductive material to form word line plates. During such a process, all or substantially all of the second dielectric material is replaced by the conductive material, such that a body of the vertical memory array includes alternating layers of the first dielectric material and the conductive word line plates.

[0005] Some conventional vertical memory arrays include so-called “through-array vias,” which are conductive vias that extend through the vertical memory array to a sub-array feature. Through-array vias potentially reduce an area that the vertical memory array and associated circuitry covers on a semiconductor device, compared to vias or other contacts that are formed outside of an area of the vertical memory array. However, the formation of the through-array vias requires additional processing acts and cost. For example, to conventionally form such through-array vias that are electrically isolated from the conductive word line materials, a portion of the alternating layers of the first dielectric material and the conductive word line material is removed and replaced with a dielectric material, through which the through-array vias are formed.

[0006] It would, therefore, be desirable to develop improved structures and methods of forming vertical memory arrays with through-array vias for semiconductor devices (e.g., vertical memory devices, such as NAND Flash memory devices) that reduce the number and complexity of additional processing acts practiced in conventional methods and structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 shows a schematic top view of a vertical memory block including via regions laterally adjacent to conductive word lines according to an embodiment of the present disclosure.

[0008] FIG. 2 shows a detailed top view of a portion of the vertical memory block of FIG. 1, taken from dashed box A of FIG. 1.

[0009] FIG. 3 shows a partial cross-sectional view taken of the vertical memory block of FIGS. 1 and 2, taken from section line I-I of FIG. 2.

[0010] FIG. 4 shows a top view of a portion of a vertical memory block with diverging slots and a via region having a variable width according to an embodiment of the present disclosure.

[0011] FIG. 5 shows a partial top view of a vertical memory block having a via region in a memory array region of the vertical memory block according to an embodiment of the present disclosure.

[0012] FIG. 6 shows a partial top view of a vertical memory block including an enlarged via region according to an embodiment of the present disclosure.

[0013] FIG. 7 shows a top view of a stair step region of a vertical memory block according to an embodiment of the present disclosure.

[0014] FIG. 8 shows a partial cross-sectional view of the stair step region of the vertical memory array block of FIG. 7, taken from section line II-II of FIG. 7.

[0015] FIGS. 9A through 13 illustrate different views of a vertical memory block at progressive stages of forming the vertical memory block according to an embodiment of the present disclosure.

[0016] FIG. 14 shows a memory device including at least one vertical memory block according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0017] The following description provides specific details, such as material types and processing conditions in order to provide a thorough description of embodiments of the present disclosure. However, a person of ordinary skill in the art will understand that the embodiments of the present disclosure may be practiced without employing these specific details. Indeed, the embodiments of the present disclosure may be practiced in conjunction with conventional fabrication techniques and materials employed in the industry, which are known to one of ordinary skill in the art.

[0018] The fabrication processes described herein do not describe a complete process flow for processing semiconductor structures. The remainder of the process flow is known to those of ordinary skill in the art. Accordingly, only the methods and memory device structures necessary to understand embodiments of the present disclosure are described herein.

[0019] In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the present disclosure may be practiced. These embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the present disclosure.

However, other embodiments may be utilized, and structural, material, and electrical changes may be made without departing from the scope of the disclosure. The illustrations presented herein are not meant to be actual views of any particular system, device, structure, or process, but are idealized representations that are employed to describe the embodiments of the present disclosure. The drawings presented herein are not necessarily drawn to scale.

[0020] Similar structures or components in the various drawings may retain the same or similar numbering for the convenience of the reader; however, the similarity in numbering does not mean that the structures or components are necessarily identical in size, composition, configuration, or other property.

[0021] As used herein, the term “substantially” in reference to a given parameter, property, or condition means and includes to a degree that one skilled in the art would understand that the given parameter, property, or condition is met with a small degree of variance, such as within acceptable manufacturing tolerances. For example, a parameter that is substantially met may be at least about 90% met, at least about 95% met, or even at least about 99% met.

[0022] As used herein, any relational term, such as “first,” “second,” “over,” “top,” “bottom,” “underlying,” etc., is used for clarity and convenience in understanding the disclosure and accompanying drawings and does not connote or depend on any specific preference, orientation, or order, except where the context clearly indicates otherwise.

[0023] As used herein, the term “forming” means and includes any method of creating, building, or depositing a material. For example, forming may be accomplished by atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, co-sputtering, spin-coating, diffusing, depositing, growing, or any other technique known in the art of semiconductor fabrication. Depending on the specific material to be formed, the technique for forming the material may be selected by a person of ordinary skill in the art.

[0024] Embodiments of the present disclosure include memory devices including a vertical memory block that has one or more conductive vias extending through alternating dielectric materials in a via region thereof. The vertical memory block may include a three-dimensional (3D) array of MONOS-type memory cells having conductive access lines (e.g., metal word lines) extending through the 3D array adjacent to slots formed vertically through the 3D array. The slots may be separated from one another by a first distance in a memory array region of the vertical memory block. The slots may be separated by a second, greater distance in

a via region of the vertical memory block, in which the one or more conductive vias are located and vertically extend. The via region may be located laterally adjacent to a stair step structure of the vertical memory block, longitudinally adjacent to the stair step structure, or in the memory array region of the vertical memory block.

[0025] FIG. 1 shows a top view of a vertical memory block 100 (also simply “memory block 100”) of a memory device (e.g., a semiconductor memory device) according to an embodiment of the present disclosure. Portions of the vertical memory block 100 depicted in FIG. 1 do not show all features, so that underlying structures and elements can be seen more clearly. FIG. 2 shows a detailed top view of a portion of the vertical memory block 100 of FIG. 1, taken from dashed box A of FIG. 1. FIG. 3 shows a partial cross-sectional view taken of the vertical memory block 100 of FIGS. 1 and 2, taken from section line I-I of FIG. 2.

[0026] Referring to FIG. 1, the vertical memory block 100 may be elongated in a longitudinal direction y , may have a width in a lateral direction x , and may also have a height in a vertical direction in and out of the page from the perspective of FIG. 1. By way of example and not limitation, the width of the vertical memory block 100 in the lateral direction x may be between about 3 μm and about 5 μm . In some embodiments, the width of the vertical memory block 100 in the lateral direction x may be about 3.4 μm . A memory array region 102 may be generally centrally located in the vertical memory block in the longitudinal direction y . The vertical memory block 100 may include a stair step region 104 at one or both longitudinal ends of the vertical memory block 100. As shown in FIG. 1, a via region 106 may be located longitudinally between the array region 102 and each of the stair step regions 104.

[0027] FIG. 2 illustrates a detailed view, marked by dashed box A in FIG. 1, of a portion of the memory array region 102 and the via region 106 of the vertical memory block 100 of FIG. 1. Referring to FIGS. 1 and 2, in the memory array region 102, an array of memory cell pillars 108 may each extend vertically through the vertical memory block 100. Each of the memory cell pillars 108 may include a central region 110 of a semiconductor material, such as a polysilicon or silicon-germanium material, at least partially surrounded by a charge trapping material 112, such as an oxide-nitride-oxide (“ONO”) material. Slots 114 (shown in FIG. 1 as solid lines), filled with a dielectric material (e.g., a silicon oxide material), may extend through the memory array region 102 proximate to and between adjacent memory cell pillars 108.

[0028] As shown in FIGS. 1 and 2, the slots 114 may be separated from each other by a first distance D_1 in the memory array region 102. In some embodiments, the first distance D_1 may be between about 400 nm and about 1000 nm. As shown in FIG. 1, in the via region 106, at least some of the slots 114 may be separated from each other by a second distance D_2 that is greater than the first distance D_1 . In some embodiments, the second distance D_2 is at least about twice the first distance D_1 , such as about four times the first distance D_1 . The slots 114 may be provided for the introduction of an electrically conductive (e.g., metal) material to be coupled to (e.g., into contact with) the memory cell pillars 108 throughout the memory array region 102 to form conductive access lines 116, as will be explained below. The conductive access lines 116 are conductive word lines 116 in the embodiments shown herein, although the present disclosure is not so limited. As shown by dashed lines in FIGS. 1 and 2, the conductive word lines 116 may extend along the slots 114 and be coupled to the memory cell pillars 108. In some embodiments, the conductive word lines 116 may include a metal, such as titanium, tantalum, tantalum nitride, tungsten, or tungsten nitride. The conductive word lines 116 and memory cell pillars 108 may form an array of so-called “MONOS” (metal - oxide - nitride - oxide - semiconductor) memory cells. In some embodiments, the memory cells may be so-called “TANOS” (tantalum nitride - aluminum oxide - nitride - oxide - semiconductor) or “BETANOS” (band/barrier engineered TANOS) memory cells, which are subsets of the general category of MONOS memory cells.

[0029] Where the slots 114 are sufficiently distant from each other, such as the slots 114 in the via region 106 separated by the second distance D_2 , the conductive word lines 116 may have a width from the slots 114 of at least a third distance D_3 . On the other hand, where the slots 114 are sufficiently close to one another, such as the slots 114 in the memory array region 102 separated by the first distance D_1 that is about twice the third distance D_3 or less, the conductive material may form a conductive word line 116 having a width greater than the third distance D_3 (e.g., a width of the first distance D_1).

[0030] In the via region 106, adjacent conductive word lines 116 may be separated by dielectric stacks 118 of at least two different alternating dielectric materials (e.g., alternating oxide and nitride materials). Conductive vias 120 may extend through the vertical memory block 100 within the dielectric stacks 118. Since the conductive vias 120 extend through the vertical memory block 100, the conductive vias 120 are also referred to as “through-array vias” or “TAVs.” Thus, the slots 114 being separated by the second distance D_2 in the via region 106 provides space for the

conductive vias 120 to be positioned through the vertical memory block 100, without having to use space beyond the footprint of the vertical memory block 100.

[0031] Referring again to FIG. 1, the stair step region 104 may include one or more stair step structures 122 for electrically contacting and accessing different overlapping conductive word lines 116. The stair step structures 122 may include contact regions 124 (e.g., “stairs”) (for clarity, labeled at the top portion of FIG. 1, but also present in the bottom portion of FIG. 1) arranged like a staircase. Word line contacts 126 (for clarity, shown and labeled at the bottom portion of FIG. 1, but also present in the top portion of the vertical memory block shown in FIG. 1) may physically and electrically contact the contact regions 124 of the stair step structures 122 to provide electrical access to the conductive word lines 116.

[0032] In some embodiments, electrical connections 128 may connect the word line contacts 126 to respective conductive vias 120, as shown near the bottom of FIG. 1. In some embodiments, the electrical connections 128 may connect the conductive vias 120 to other portions of one or more of the conductive word lines 116, as shown near the top of FIG. 1. In some embodiments, the conductive vias 120 may be electrically connected to other features or elements within the vertical memory block 100 or external to the vertical memory block 100.

[0033] Although FIG. 1 illustrates adjacent stair step structures 122 that are separated by dielectric stacks 118 of at least two different alternating dielectric materials in the via region 106, the present disclosure is not so limited. For example, rather than splitting a single conductive word line 116 into two adjacent stair step structures 122, two or more adjacent conductive word lines 116 may be merged into a single stair step structure 122. Thus, the present disclosure includes various embodiments of vertical memory blocks with split and merged word lines 116 in different regions of the vertical memory blocks, depending upon the arrangement and proximity of the slots 114.

[0034] Referring to FIG. 2, dielectric support pillars 130 (shown as dashed squares) may, optionally, be located to support dielectric materials (e.g., oxide materials) in the vertical memory block 100 during fabrication. The memory cell pillars 108 may support the dielectric materials in the memory array region 102 during fabrication. However, in portions of the vertical memory block 100 that may lack memory cell pillars 108, such as in the via region 106 or in the stair step region 104, the dielectric support pillars 130 may be used to support the dielectric materials during fabrication of the vertical memory block 100. The dielectric support pillars 130 may include a dielectric material, such as an oxide material (e.g., silicon dioxide).

[0035] FIG. 3 illustrates a partial cross-sectional view of the vertical memory block 100, taken from section line I-I of FIG. 2. In the memory array region 102, the memory cell pillars 108 (each including the central region 110 of a semiconductor material at least partially surrounded by the charge trapping material 112) and the slots 114 may vertically extend through a stack of alternating conductive word lines 116 and first dielectric materials 132. An individual memory cell (e.g., a MONOS memory cell) may be formed at each junction between the respective conductive word lines 116 and memory cell pillars 108. FIG. 3 illustrates five overlying conductive word lines 116 and five overlying first dielectric materials 132 between the conductive word lines 116. Thus, the vertical memory block 100 shown in FIG. 3 has five tiers. However, the present disclosure is not limited to vertical memory blocks 100 with five tiers. Rather, vertical memory blocks according to the present disclosure may have any number of tiers, such as at least 16, 32, 36, or 72 tiers, by way of non-limiting examples.

[0036] In the via region 106, conductive vias 120 (only one shown in FIG. 3) vertically extend through the dielectric stack 118. The dielectric stack 118 may include alternating first dielectric materials 132 and second dielectric materials 134. By way of example and not limitation, the first dielectric materials 132 may include an oxide (e.g., silicon dioxide) material, and the second dielectric materials 134 may include a nitride (e.g., silicon nitride) material. To form the conductive word lines 116, a portion of the second dielectric material 134 along the slots 114 may be selectively removed, while the first dielectric material 132 remains. A conductive material may then be formed to replace the second dielectric material 134 that was removed. Both the first and second dielectric materials 132, 134 may be present in the dielectric stack 118 because the slots 114 are sufficiently far away from each other in the via region 106 that the second dielectric material 134 is not removed in the dielectric stack 118. Thus, the first and second dielectric materials 132, 134 remain and form the dielectric stack 118, through which the conductive vias 120 may be formed to electrically isolate the conductive vias 120 from the conductive word lines 116. The conductive vias 120 may be electrically coupled to sub-array circuitry 136, such as a driver circuit, in or on a substrate 138. For example, at least one of the conductive vias 120 may operatively couple the sub-array circuitry 136 to the vertical memory block 100.

[0037] Vertical memory blocks 100 having the features and configurations described in the present disclosure may enable dense wiring with no exit channel for wires from a group of sub-blocks.

[0038] Although the present disclosure describes, by way of example, vertical memory blocks including arrays of MONOS memory cells, the present disclosure is not so limited. For example, the present disclosure may be applicable to any vertical memory block or device that is fabricated by forming memory cell materials prior to forming associated conductive materials (e.g., word lines, gate materials) coupled to the memory cell materials, such as through slots formed according to this disclosure. For example, the present disclosure also applies to so-called “floating gate” memory cells including a metal control gate as a charge trapping material 112.

[0039] Accordingly, vertical memory blocks are disclosed including a memory cell region and at least one via region. The memory cell region includes an array of memory cell pillars extending vertically through the vertical memory block. The at least one via region includes a dielectric stack of alternating dielectric materials and at least one conductive via extending through the dielectric stack.

[0040] Additionally, semiconductor devices including a vertical memory block are disclosed. The semiconductor devices include at least one driver circuit on or in a substrate and at least one vertical memory block having a longitudinal length and a lateral width on the substrate and operatively coupled to the at least one driver circuit. The at least one vertical memory block includes a three-dimensional array of memory cells, slots extending vertically through the at least one memory block laterally between adjacent memory cells of the three-dimensional array, and conductive access lines extending along and adjacent to the slots. The slots are separated by a first lateral distance in a first portion of the vertical memory block along the three-dimensional array of memory cells, and by a second, greater lateral distance in a second portion of the at least one vertical memory block adjacent to the three-dimensional array of memory cells.

[0041] Referring again to FIGS. 1 and 2, rectangular (when viewed from the top as in FIGS. 1 and 2) dielectric stacks 118 may be formed by routing the slots 114 from the first distance D_1 apart from each other to the second distance D_2 apart from each other in a step-wise fashion (i.e., by forming the slots 114 with 90 degree angles). However, the present disclosure is not so limited.

[0042] As shown in FIG. 4, in some embodiments, a vertical memory block 200 may include slots 214 that gradually diverge from each other at an acute angle. Such diverging slots 214 may result in conductive word lines 216 and dielectric stacks 218 that are not rectangular. Rather, the dielectric stacks 218 between adjacent conductive word lines 216 (or adjacent portions of a

single conductive word line 216) may have a shape that includes a narrow end region 219 corresponding to the adjacent diverging slots 214.

[0043] Referring to FIG. 5, in some embodiments, a vertical memory block 300 may include a dielectric stack 318 through which conductive vias 320 extend that is positioned in a memory array region 302 of the vertical memory block 300 rather than in a separate via region. For example, an area 340 of the memory array region 302 may be left free of slots 314, such that the dielectric stack 318 is between conductive word lines 316 along the slots 314 within the memory array region 302.

[0044] Additionally or alternatively, one or more dielectric stacks 318 and associated conductive vias 320 may be positioned in a stair step region 304 of the vertical memory array 300, such as adjacent to stair step structures 322.

[0045] Accordingly, the dielectric stack 318 and associated conductive vias 320 may be located at any desired location (depending on, e.g., a location of sub-array circuitry to which the conductive vias 320 are to be connected) in the vertical memory block 300. To locate the dielectric stack 318 and associated conductive vias 320 in a desired location, a sufficiently large space between adjacent slots 314 is provided at the desired location, such that adjacent conductive word lines 316 (or adjacent portions of a single conductive word line 316) do not extend all the way across the space.

[0046] Referring to FIG. 6, a vertical memory block 400 may include a relatively large (compared to the embodiments described above) dielectric stack 418 in a via region 406 adjacent to a stair step region 404. A relatively wider (compared to the embodiments described above) memory array region 402 in the lateral direction x may be formed to provide additional lateral space for the dielectric stack 418 and associated conductive vias 420 in the via region 406. The additional lateral space for the dielectric stack 418 may be utilized by spacing the conductive vias 420 farther apart, by forming additional conductive vias 420 therein, or both.

[0047] The width of the memory array region 402 may be increased without reducing a density of memory cells by routing slots 414A, 414B to fill the extra width. By way of example and not limitation, the slots 414A, 414B may be routed in an interlocking-J pattern. Thus, first slots 414A for forming first conductive word lines 416A associated with a first stair step region 404 (e.g., at the bottom of the memory array block 400 depicted in FIG. 6) may extend away from the first stair step region 404 in a longitudinal direction y , laterally across a portion of the memory array

block 400, and longitudinally back towards the first stair step region 404. Complementary, second slots 414B for forming conductive word lines 416B associated with another stair step region 404 (not shown in FIG. 6, but in a direction toward the top of the memory array block 400 depicted in FIG. 6) may extend away from the associated stair step region 404 in a longitudinal direction y , laterally across a portion of the memory array block 400, and longitudinally back towards the second stair step region 404. Thus, the width of the memory array region 402 and, consequently, of the vertical memory block 400, may be enlarged while substantially filling the memory array region 402 with slots 414A, 414B and corresponding conductive word lines 416A, 416B, to maintain a density of memory cells coupled to the word lines 416A, 416B within the memory array region 402.

[0048] Embodiments including slots 414A, 414B arranged in an interlocking-J pattern may enable each word line contact to connect to two or more conductive word lines 416A, 416B, such that the stair step region 404 may exhibit up to about four times the pitch between the slots 414A, 414B. The extra space may be used for a large array region 406 (as shown in FIG. 6) or for multiple dielectric stacks 418 positioned throughout the stair step region 404.

[0049] FIG. 7 shows a top view of a stair step region of a vertical memory block 500 according to an embodiment of the present disclosure. FIG. 8 shows a partial cross-sectional view of the stair step portion of the vertical memory block 500 of FIG. 7, taken from section line II-II of FIG. 7. The vertical memory block 500 of FIGS. 7 and 8 includes many features and elements that are similar to the vertical memory block 100 described above with reference to FIGS. 1 through 3. For example, the vertical memory block 500 of FIGS. 7 and 8 includes slots 514, conductive word lines 516, dielectric stacks 518 of alternating dielectric materials, conductive vias 520 extending through the vertical memory block 500 within the dielectric stacks 518, and stair step structures 522 including contact regions 524 for electrically contacting and accessing different overlapping conductive word lines 516 using word line contacts 526. The conductive word lines 516 extend along the slots 514. As discussed above, the conductive word lines 516 may have a width from the corresponding slots 514 that is the third distance D_3 in locations where the slots 514 are sufficiently far apart from each other (e.g., more than twice the third distance D_3). In locations where the slots 514 are apart from each other about twice the third distance D_3 or less, the conductive word lines 516 may have a greater width than the third distance D_3 , as the material of the conductive word lines 516 formed from adjacent slots 514 contact or are integrally formed with each other.

[0050] However, compared to the vertical memory block 100 of FIGS. 1 through 3, the vertical memory block 500 of FIGS. 7 and 8 includes an additional slot 514A in the stair step region that splits one area of the conductive word lines 516 into four distinct word line portions 516A, 516B, 516C, and 516D that terminate in respective stair step structures 522A, 522B, 522C, and 522D. The additional slot 514A may extend from the stair step structures 522A, 522B, 522C, and 522D in a longitudinal direction y to proximate (e.g., within about twice the third distance D_3 or less), but not connecting with, another one of the slots 514. A word line connection region 550 may remain between the additional slot 514A and the proximate slot 514. As shown in FIG. 8, multiple conductive word lines 516 may be vertically positioned over each other in tiers T_1 , T_2 , T_3 , and T_4 . Referring to a single conductive word line 516 (i.e., a conductive word line 516 at a particular tier T_1 , T_2 , T_3 , or T_4), the four word line portions 516A, 516B, 516C, and 516D are physically and electrically connected to each other at the word line connection region 550. Thus, due to the presence of the additional slot 514A and the word line connection region 550 (FIG. 7), the four word line portions 516A, 516B, 516C, and 516D at any one of the tiers T_1 , T_2 , T_3 , or T_4 are physically and electrically connected fingers of the same conductive word line 516.

[0051] As is known by those of ordinary skill in the art, stair step structures for electrical connection to conductive word lines (or word line plates) at the tiers of vertical memory blocks may be formed by utilizing a so-called “stair step mask” and, optionally, one or more so-called “chop masks.” A stair step mask may be formed over the vertical memory block while leaving one step-width (e.g., a width of one contact region 524 measured in the longitudinal direction y) exposed. One or more tiers of conductive material (e.g., of the conductive word lines 516) exposed through the stair step mask may be removed, such as by a first cycle of anisotropic material removal (e.g., etching). An edge of the stair step mask may be removed to recess the edge of the stair step mask and to expose another step-width, in addition to the original exposed step-width. Another cycle of material removal may be performed to remove another one or more tiers of conductive material exposed through the recessed stair step mask. The process may be repeated to form a desired number of contact regions (e.g., contact regions 524, also referred to as “stairs”).

[0052] A chop mask may be used cover one or more particular stair step structures or portions thereof (e.g., one or more of the stair step structures 522, 522A, 522B, 522C, 522D), while leaving one or more other stair step structures or portions thereof exposed through the chop mask. The entire exposed one or more other stair step structures or portions thereof is vertically recessed,

such that one or more exposed tiers is removed. Thus, the one or more stair step structures exposed through the chop mask may be vertically recessed from the one or more stair step structures that is covered by the chop mask, such that the one or more exposed stair step structures defines contact regions (“stairs”) for tiers that are lower than the tiers having contact regions (“stairs”) for the one or more stair step structures covered by the chop mask. A chop mask may be used before or after the stair step mask is used. Chop masks are used to provide contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover. In addition, process control of removing material utilizing a stair step mask to form a stair step structure, as described above, may be difficult to maintain for a large number of cycles (e.g., more than about 12 cycles) and tiers. A single chop mask may be used to double the number of contact regions (“stairs”) of a stair step structure formed using a single stair step mask. By way of a non-limiting example, a stair step mask may be used to form a stair step structure of 12 contact regions, for accessing 12 respective tiers. A chop mask may be used to expose and access 12 additional tiers underlying the 12 tiers formed by the stair step mask alone.

[0053] Returning to methods and structures of the present disclosure, as shown in FIG. 8, after (or, alternatively, before) a stair step mask is used to form an initial stair step structure, a first chop mask may be positioned to cover the first and fourth stair step structures 522A, 522D, while leaving the second and third stair step structures 522B, 522C exposed, as indicated under a first bracket 560 in FIG. 8. One material removal cycle may be performed to remove exposed portions of the topmost conductive word line 516 in a first tier T_1 . The first chop mask may be removed, and a second chop mask may be positioned to cover the first and second stair step structures 522A, 522B, while leaving the third and fourth stair step structures 522C, 522D exposed, as indicated under a second bracket 562 in FIG. 8. Two material removal cycles may be performed to remove exposed portions of the conductive word lines 516 in a second tier T_2 and third tier T_3 in the third stair step structure 522C, and to remove exposed portions of the two conductive word lines 516 in the first tier T_1 and a second tier T_2 of the fourth stair step structure 522D. In this manner, a contact region 524 for the first tier T_1 may be defined in the first stair step structure 522A, a contact region 524 for the second tier T_2 may be defined in the second stair step structure 522B, a contact region 524 for the third tier T_3 may be defined in the fourth stair step structure 522D, and a contact region 524 for the fourth tier T_4 may be defined in the third stair step structure 522C.

[0054] In the embodiment shown in FIGS. 7 and 8, four cycles of material removal may be performed in connection with each time a corresponding stair step mask is recessed, such that successively lower “stairs” in a single stair step structure 522, 522A, 522B, 522C, 522D are four tiers lower than a successively higher “stair” in the same stair step structure 522, 522A, 522B, 522C, 522D.

[0055] In some embodiments, a single material removal cycle may be performed in connection with each time a corresponding stair step mask is recessed to form “stairs.” In such embodiments, assuming S number of stairs are formed using the stair step mask alone, a first chop mask may be used to remove exposed portions of the same S number of conductive word lines 516 from the second and third stair step structures 522B, 522C, and a second chop mask may be used to remove exposed portions of twice the S number of eight conductive word lines 516 from the third and fourth stair step structures 522C, 522D. The embodiment shown in FIGS. 7 and 8 is an example of such embodiments, in which the S number of stairs formed using the stair step mask alone is four.

[0056] Thus, in embodiments employing the additional slot 514A and including a word line connection region 550, as shown by way of example in FIGS. 7 and 8, a single stair step mask and two chop masks may be sufficient to form distinct contact regions 524 for a quantity of tiers up to four times the number of contact regions 524 exposed by the single stair step mask alone.

[0057] FIGS. 9A through 13 illustrate a method of forming a vertical memory block, such as the vertical memory block 100 of FIG. 1. FIG. 9A shows a top view of a vertical memory block structure 100A, and FIG. 9B shows a cross-sectional view of the vertical memory block structure 100A taken from section line III-III of FIG. 9A. Referring to FIG. 9B, a stack 178 of alternating first and second dielectric materials 132, 134 is formed over the substrate 138, which may include the sub-array circuitry 136. The first dielectric material 132 may be, for example, an oxide material such as silicon dioxide. The second dielectric material 134 may be, for example, a nitride material such as silicon nitride. The memory cell pillars 108 may be formed in the memory array region 102 (FIG. 9A), each of which may include the central region 110 of a semiconductor material at least partially surrounded by a charge trapping material 112. By way of example, the memory cell pillars 108 may be formed by anisotropically removing portions of the first dielectric material 132 and second dielectric material 134 to form holes through the stack 178, after which an oxide, nitride, and oxide material is formed along sidewalls defining the holes through the stack 178

to form the charge trapping material 112. A semiconductor material may be formed to fill the remaining holes to form the central region 110 of the memory cell pillars 108. Optionally, dielectric support pillars 130 (FIG. 2) of a dielectric material (e.g., an oxide material, such as silicon dioxide) may additionally be formed in locations lacking memory cell pillars 108, to provide support for the first dielectric materials 132 in those locations during subsequent operations.

[0058] Referring to FIGS. 9A and 9B, the slots 114 may be formed by anisotropically removing portions of the first dielectric material 132 and second dielectric material 134. The slots 114 may be formed to be separated from adjacent slots 114 by a first distance D_1 in the memory array region 102 of the stack 178, and at least some of the slots 114 in the stair step region 104 and the via region 106 may be separated by a second distance D_2 greater than the first distance D_1 .

[0059] FIG. 10A shows a top view of a vertical memory block structure 100B formed from the vertical memory block structure 100A of FIGS. 9A and 9B after additional processing. FIG. 10B shows a cross-sectional view of the vertical memory block structure 100B taken from section line IV-IV of FIG. 10A.

[0060] Referring to FIGS. 10A and 10B, portions of the second dielectric material 134 of the stack 178 adjacent to the slots 114 may be removed through the slots 114, such as by an isotropic material removal process that selectively removes the second dielectric material 134 relative to the first dielectric material 132 and the charge trapping material 112 of the memory cell pillars 108. One of ordinary skill in the art is familiar with such isotropic removal processes. The material removal process may form access line gaps 180 (referred to below as “word line gaps 180”) between the first dielectric materials 132. Based on the amount of time and chemistry used to remove the portions of the second dielectric material 134 and to form the word line gaps 180, the word line gaps 180 may have a width from the slots 114 of the third distance D_3 . The third distance D_3 may be about half the first distance D_1 between the slots 114 in the array region 102 or more, such that the word line gaps 180 extend from one slot 114 to an adjacent slot 114 in locations where the slots 114 are separated by the first distance D_1 , such as in the memory array region 102. The second distance D_2 may be about twice the first distance D_1 or more, such that portions of the stack 178 of alternating dielectric materials remains between adjacent slots 114 in locations where the slots 114 are separated by the second distance D_2 , such as in the stair step region 104 and the via region 106, to define the dielectric stacks 118 in those locations.

[0061] FIG. 11 shows a cross-sectional view of a vertical memory block structure 100C formed from the vertical memory block structure 100B of FIGS. 10A and 10B after additional processing. Referring to FIG. 11, the word line gaps 180 (FIG. 10B) may be filled with a conductive material (e.g., titanium, tantalum, tantalum nitride, tungsten, or tungsten nitride) to form the conductive word lines 116. Any residual conductive material within the slots 114 may be removed, and the slots 114 may be filled with a dielectric material (e.g., an oxide material, a nitride material).

[0062] FIG. 12 shows a cross-sectional view of a vertical memory block structure 100D formed from the vertical memory block structure 100C of FIG. 11 after additional processing. Referring to FIG. 12, conductive vias 120 may be formed to extend through the dielectric stacks 118 of the alternating first and second dielectric materials 132, 134 to electrically contact the sub-array circuitry 136 in or on the substrate 138. To form the conductive vias 120, portions of the first and second dielectric materials 132, 134 in the dielectric stacks 118 may be anisotropically removed to form through holes, which may be at least partially filled with a conductive via material (e.g., titanium, tantalum, tantalum nitride, tungsten, or tungsten nitride).

[0063] FIG. 13 is a top view of a vertical memory block structure 100E formed from the vertical memory block structure 100D of FIG. 12 after additional processing. As shown in FIG. 13, ends of the conductive word lines 116 proximate longitudinal ends of the vertical memory block structure 100E may be processed to form the stair step structures 122, defining the contact regions 124 for electrically contacting and accessing the conductive word lines 116 of different tiers. As generally described above with reference to FIGS. 7 and 8, the stair step structures 122 may be formed using a stair step mask and, optionally, one or more chop masks, as is known to one of ordinary skill in the art. After the stair step structures 122 are formed to define the contact regions 124, the word line contacts 126 may be formed to physically and electrically contact the respective conductive word lines 116. Electrical connections 128 (FIG. 1) may be formed between the conductive vias 120 and other conductive elements, such as the word line contacts, for example.

[0064] Although the formation of the conductive vias 120 has been explained and illustrated as occurring subsequent to the formation of the conductive word lines 116 and the filling of the slots 114 with a dielectric material, the present disclosure is not so limited. For example, the conductive vias 120 may be formed prior to, during, or after the formation of the conductive word lines 116 and the filling of the slots 114 with a dielectric material. In some embodiments, the

conductive vias 120 may be formed after forming the stair step structures 122, such as during a same process in which the word line contacts 126 are formed.

[0065] The methods described herein enable the formation of through-array vias 120 without the need for removing conductive material 116 and other portions of the vertical memory block 100 in a separate material removal act to form the conductive vias 120. Rather, the methods of the present disclosure utilize dielectric materials (e.g., the first and second dielectric materials 132, 134) that are already present during the formation of the vertical memory block 100 as a location for forming the conductive vias 120. Such methods provide efficient use of the materials and processes used to form the vertical memory block 100.

[0066] Accordingly, the present disclosure includes methods of forming a vertical memory block of a semiconductor device. In accordance with such methods, a stack of alternating first dielectric materials and second dielectric materials is formed. Portions of the first dielectric materials and second dielectric materials are removed to form slots extending through the stack. The slots are separated by a first distance in a memory array region of the vertical memory block and by a second, greater distance in a via region of the vertical memory array block. Portions of the second dielectric materials adjacent to the slots are removed to form access line gaps extending along the slots. Portions of the second dielectric material are left in the via region. A conductive material is formed within the access line gaps to form conductive access lines. At least one conductive via is formed to extend through the first dielectric materials and the second dielectric materials in the via region.

[0067] The present disclosure also includes devices and systems that include one or more of the vertical memory blocks 100, 200, 300, 400, 500 described above. As shown in FIG. 14, a semiconductor memory device 600 may include one or more of the vertical memory blocks 100, 200, 300, 400, 500 described above. The semiconductor memory device 600 may also include additional elements, such as communication circuitry 610, drivers 620, a memory controller 630, an amplifier 640, and a decoder 650, for example. In some embodiments, one or more of the additional elements may be formed under the vertical memory blocks 100, 200, 300, 400, 500 and electrically contacted using through-array vias (e.g., the conductive vias 120, 220, 320, 420, 520 described above). A semiconductor system may include a semiconductor memory device 600 as described herein.

[0068] The embodiments of the disclosure described above and illustrated in the accompanying drawing figures do not limit the scope of the invention, since these embodiments are merely examples of embodiments of the disclosure. The invention is encompassed by the appended claims and their legal equivalents. Any equivalent embodiments lie within the scope of this disclosure. Indeed, various modifications of the present disclosure, in addition to those shown and described herein, such as other combinations and modifications of the elements described, will become apparent to those of ordinary skill in the art from the description. Such embodiments, combinations, and modifications also fall within the scope of the appended claims and their legal equivalents.



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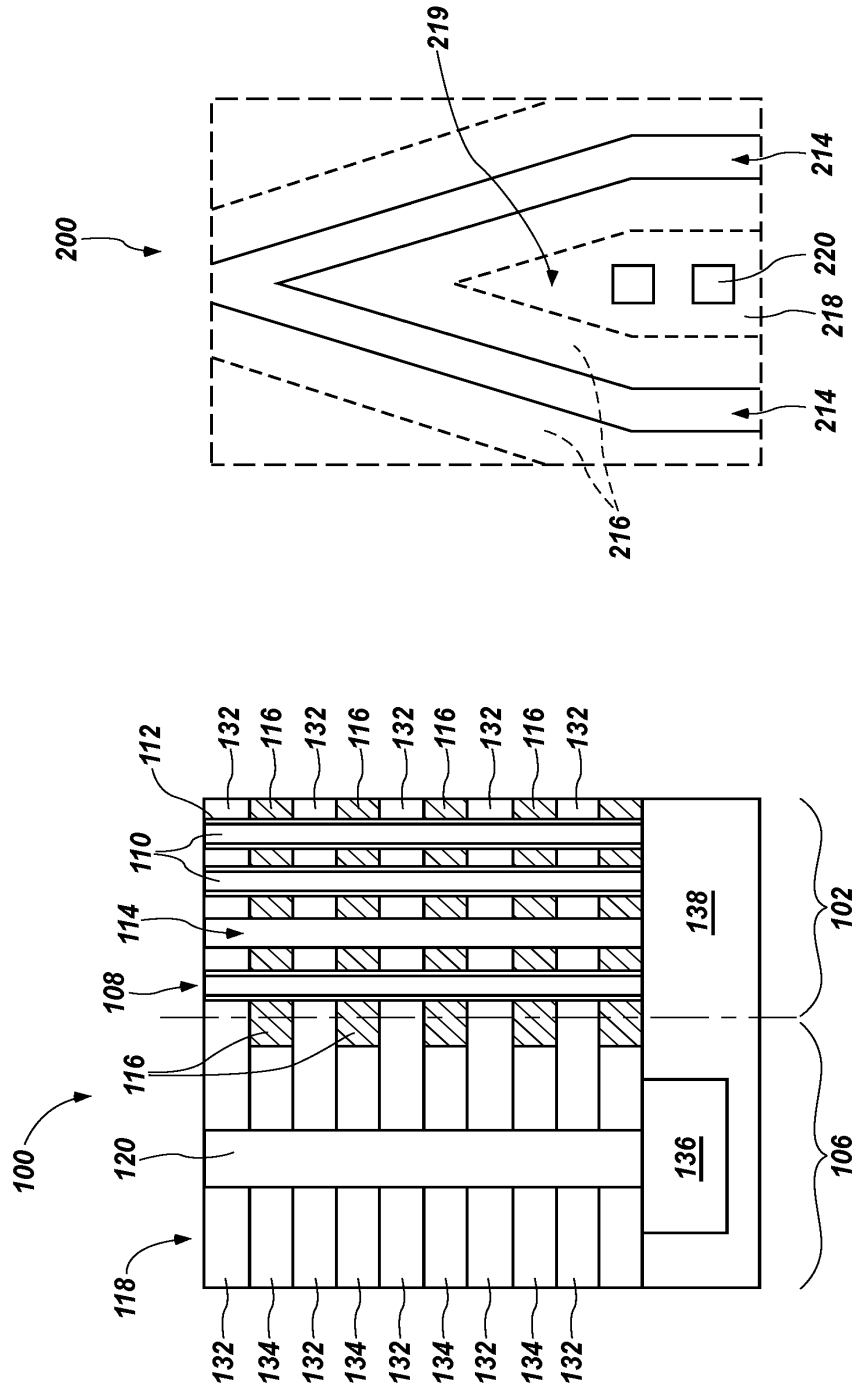


FIG. 4

FIG. 3

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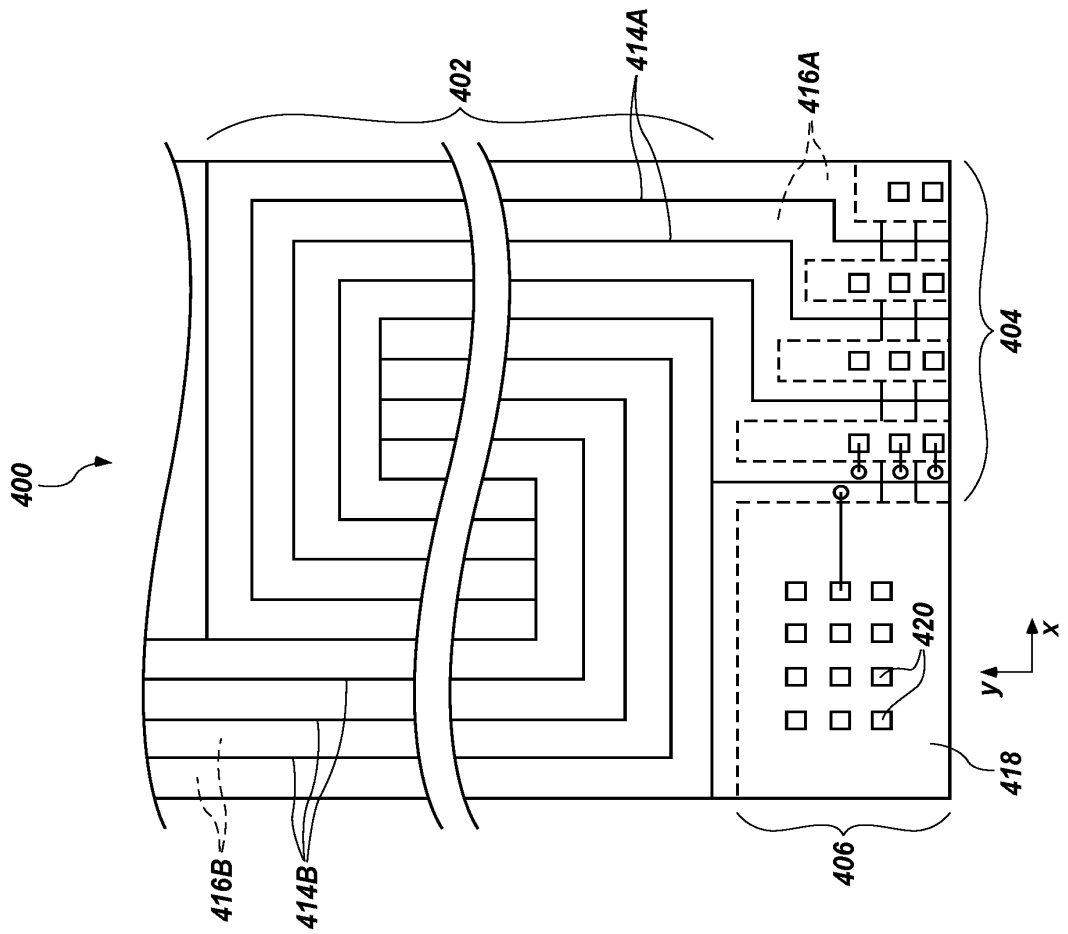


FIG. 6

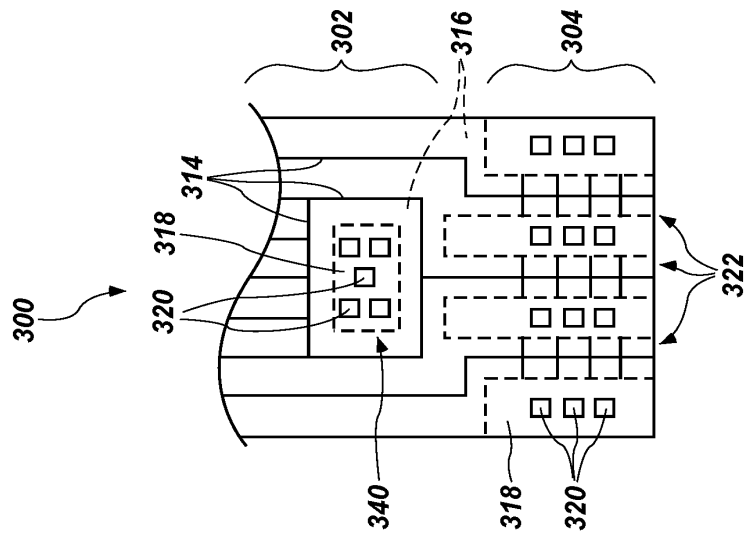


FIG. 5

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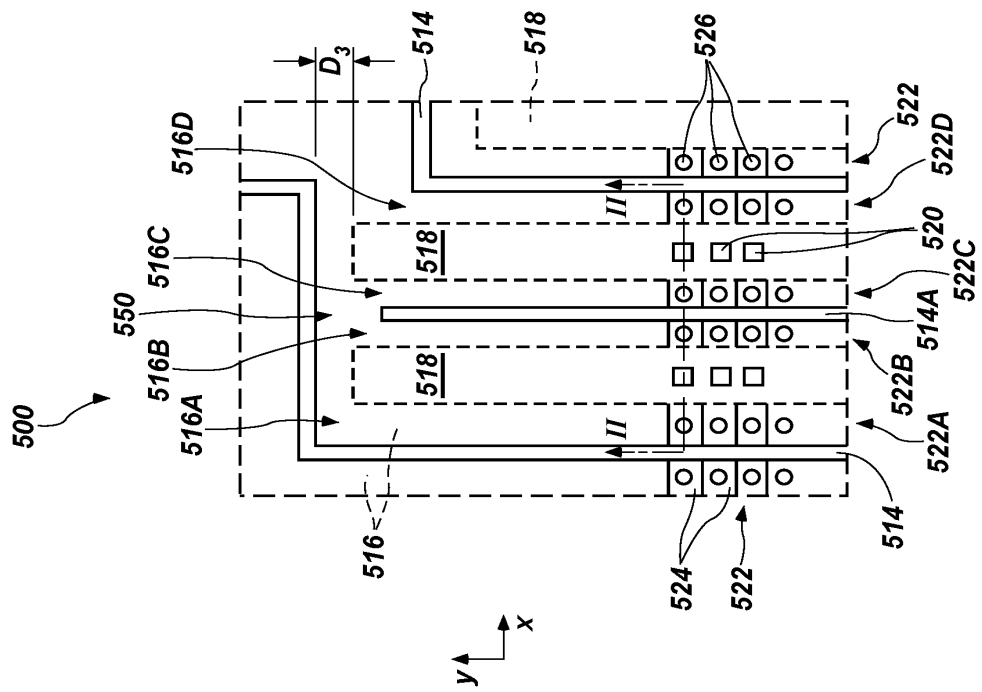


FIG. 7

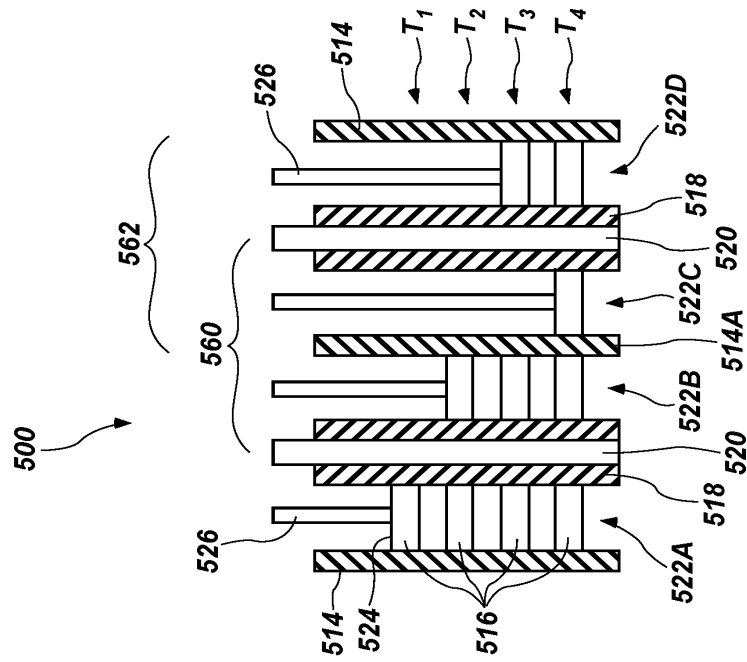


FIG. 8

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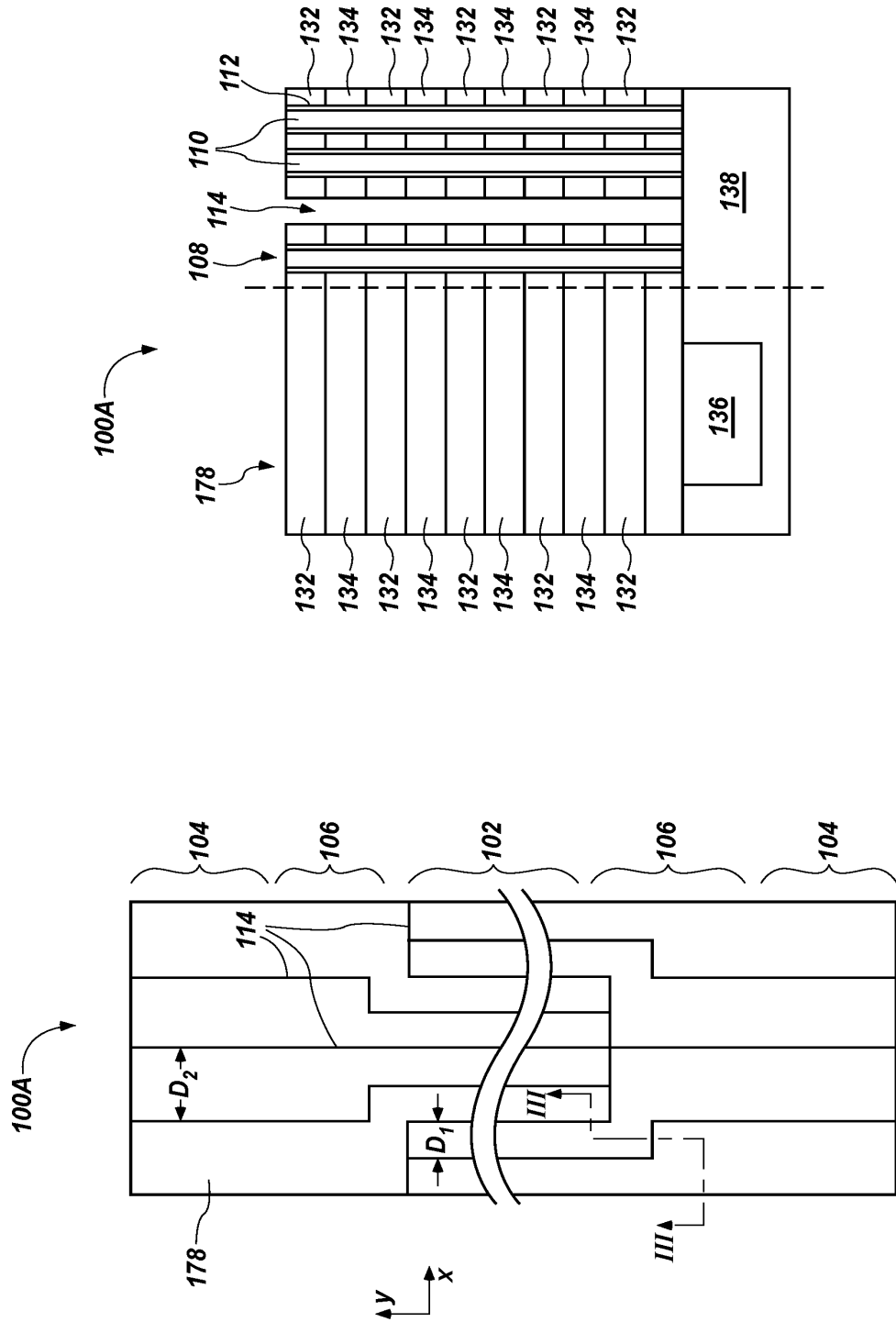


FIG. 9B

FIG. 9A

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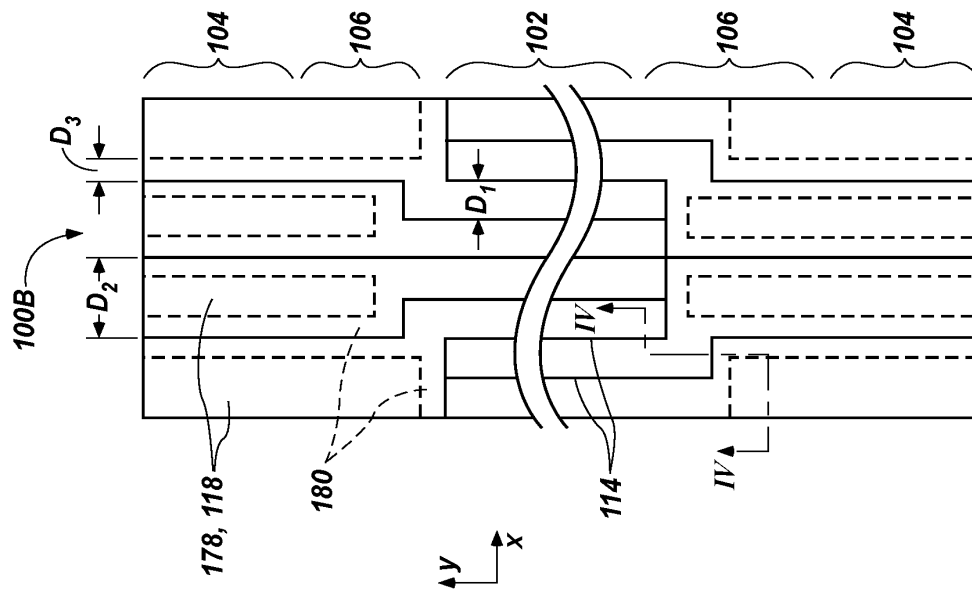


FIG. 10A

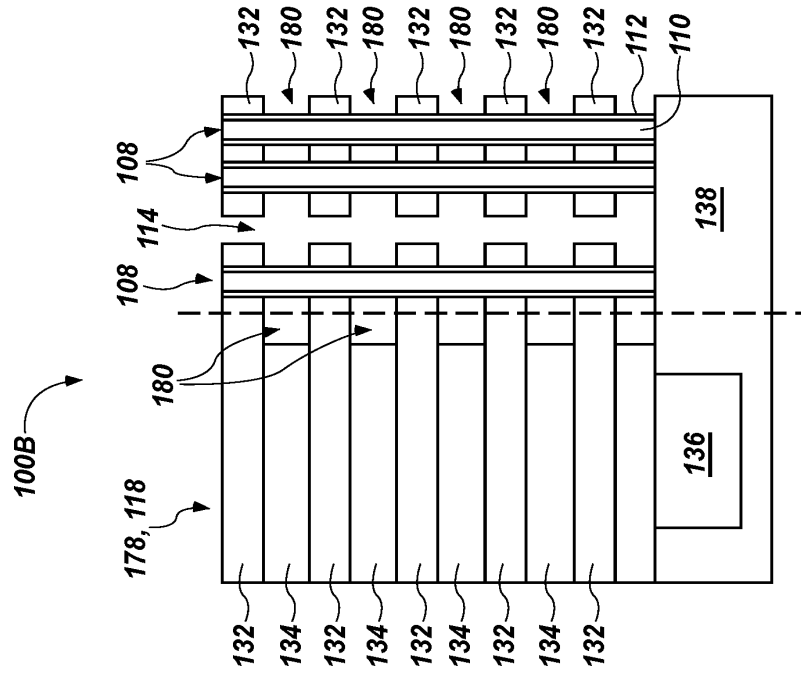


FIG. 10B

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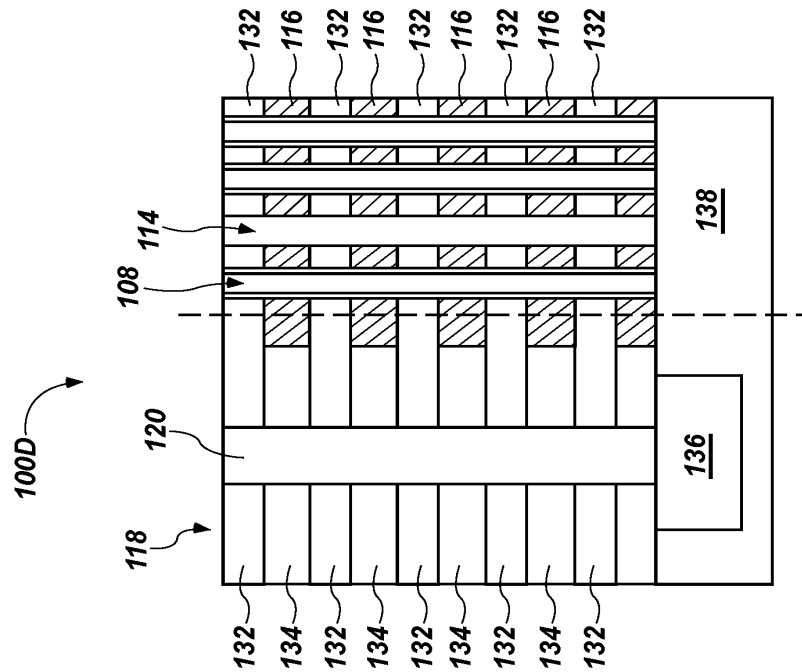


FIG. 12

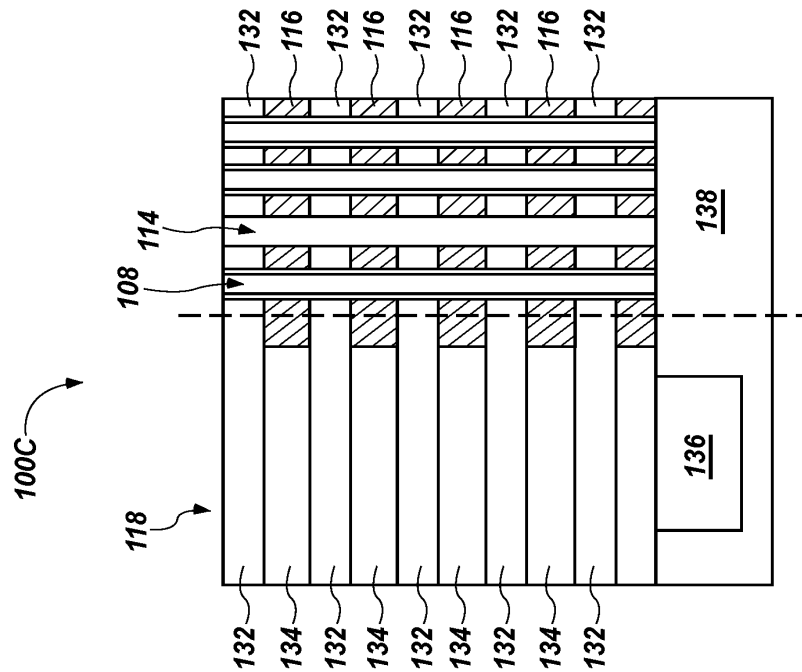


FIG. 11

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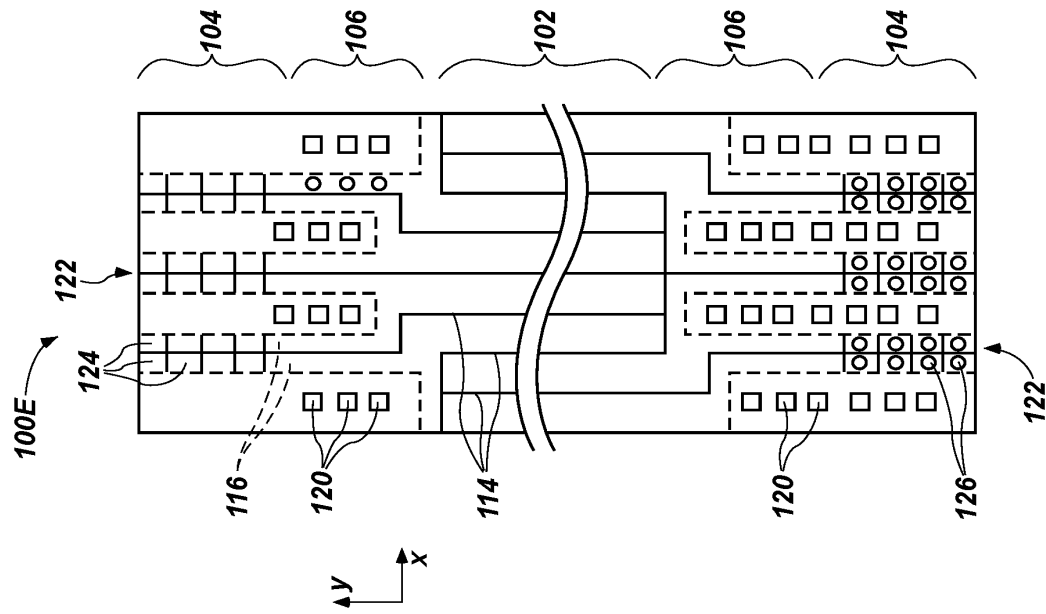


FIG. 13

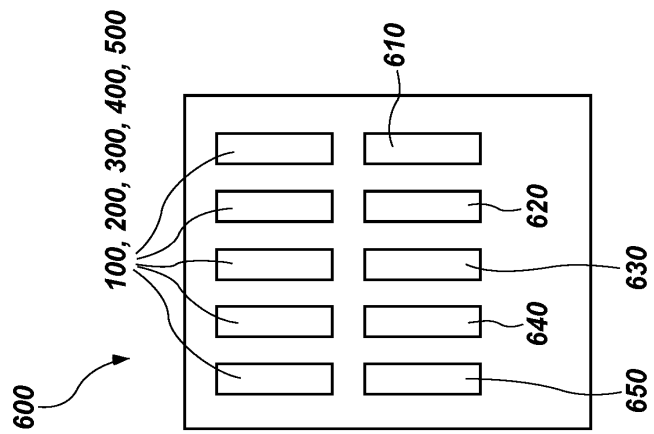


FIG. 14

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First Named Inventor	Eric H. Freeman	DECLARATION FOR UTILITY PATENT APPLICATION (37 CFR § 1.63) USING AN APPLICATION DATA SHEET (37 CFR § 1.76)
Serial No.		
Filing Date		
Group Art Unit	Unknown	
Examiner Name	Unknown	
Confirmation No.		
Attorney Docket No.	2269-12935US	
Title: VERTICAL MEMORY BLOCKS AND RELATED DEVICES AND METHODS		

Micron Ref. No. 2015-0059.00/US

As a below named inventor, I hereby declare that this declaration is directed to the application identified by Attorney Docket No. 2269-12935US filed in the name of the following inventors:

Eric H. Freeman
Justin B. Dorhout

The above-identified application was made or authorized to be made by me.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Direct all correspondence to the address associated with Customer No. **63162**.

Signature: 

Date: 16 NOV 2015

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First Named Inventor	Eric H. Freeman	DECLARATION FOR UTILITY PATENT APPLICATION (37 CFR § 1.63) USING AN APPLICATION DATA SHEET (37 CFR § 1.76)
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Attorney Docket No.	2269-12935US	
Title: VERTICAL MEMORY BLOCKS AND RELATED DEVICES AND METHODS		

Micron Ref. No. 2015-0059.00/US

As a below named inventor, I hereby declare that this declaration is directed to the application identified by Attorney Docket No. 2269-12935US filed in the name of the following inventors:

Eric H. Freeman
Justin B. Dorhout

The above-identified application was made or authorized to be made by me.

I believe I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Direct all correspondence to the address associated with Customer No. **63162**.

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Date: 11 / 16 / 2015

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Payment information:

Submitted with Payment	yes
Payment Type	CARD
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	Aug-01-2018-Application-Data-Sheet-12935-2US.pdf	1794593	no	8
			444e64ed76661560a8a4c712c5287d61f704eb2f		
Warnings:					
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2		Aug-01-2018-Application-12935-2US.pdf	168442	yes	24
			66dd81222f9c6ea27d9e6ffeeb6b356c685832c6		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Abstract		24	24	
	Claims		20	23	
	Specification		1	19	
Warnings:					
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3	Drawings-only black and white line drawings	Aug-01-2018-Drawings-12935-2US.pdf	129422	no	8
			98ae16f7a012b64a4b8aec33f079d7fcbeca33f1		
Warnings:					
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4	Oath or Declaration filed	Aug-01-2018-Declaration-12935-2US.pdf	214861	no	2
			a47fa0ffa4204b38f69a0900d03cae07fed7bac		
Warnings:					
Information:					
5	Power of Attorney	Aug-01-2018-POA-12935-2US.pdf	210607	no	2
			777bf83f0dee793bc39ad1479ad9ad14981fe63c		

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6	Information Disclosure Statement (IDS) Form (SB08)	Aug-01-2018-IDS-12935-2US. pdf	1083157 3ff10b1c7dc6f48aaa02b2e704d8ec19182f115	no	6
Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	34955 bea599bbe65adff86ba7f491122bb2e8496947fb0b	no	2
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