US 20160163732A1

(19) United States

(12) Patent Application Publication

LIM et al.

(10) Pub. No.: US 2016/0163732 A1

(43) Pub. Date: Jun. 9, 2016

(54) **SEMICONDUCTOR DEVICES**

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(21) Appl. No.: **14/962,263**

(22) Filed: **Dec. 8, 2015**

(30) **Foreign Application Priority Data**

Dec. 9, 2014 (KR) 10-2014-0176089

Publication Classification

(51) **Int. Cl.**

H01L 27/115	(2006.01)
H01L 23/522	(2006.01)
H01L 23/528	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 27/11582*** (2013.01); ***H01L 23/528*** (2013.01); ***H01L 23/5226*** (2013.01)

(57) **ABSTRACT**

Semiconductor devices and methods of manufacturing the semiconductor devices are provided. The semiconductor devices may include a semiconductor pattern including an opening on a semiconductor substrate. A peripheral transistor and a peripheral interconnection structure may be disposed between the semiconductor substrate and the semiconductor pattern. The peripheral interconnection structure may be electrically connected to the peripheral transistor. Cell gate conductive patterns may be disposed on the semiconductor pattern. The cell vertical structures may extend through the cell gate conductive patterns and may be connected to the semiconductor pattern. Cell bit line contact plugs may be disposed on the cell vertical structures. A bit line may be disposed on the cell bit line contact plugs. A peripheral bit line contact structure may be disposed between the bit line and the peripheral interconnection structure. The peripheral bit line contact structure may extend through the opening of the semiconductor.

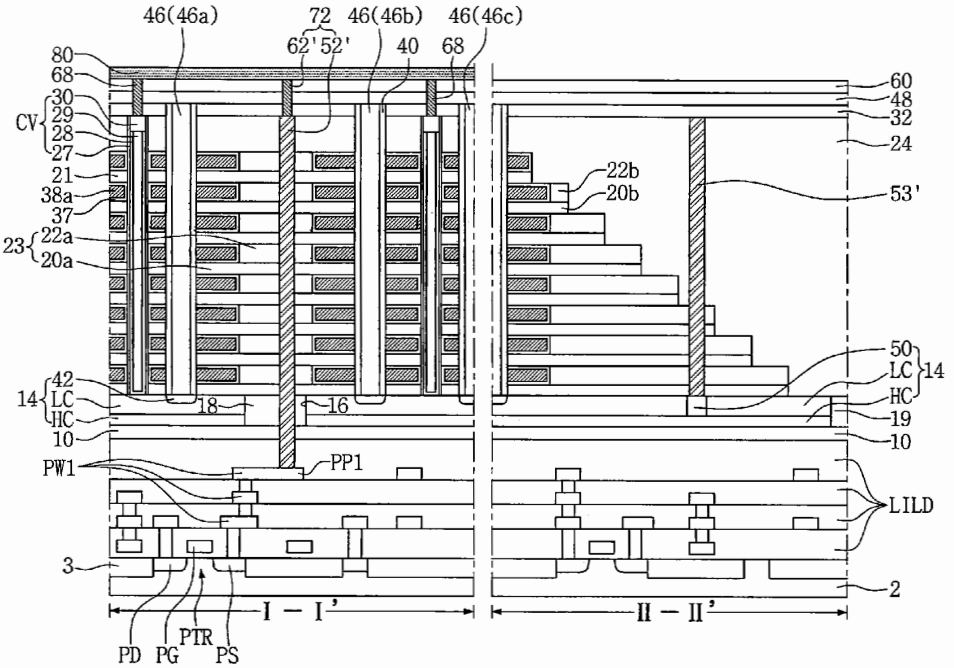


FIG. 1

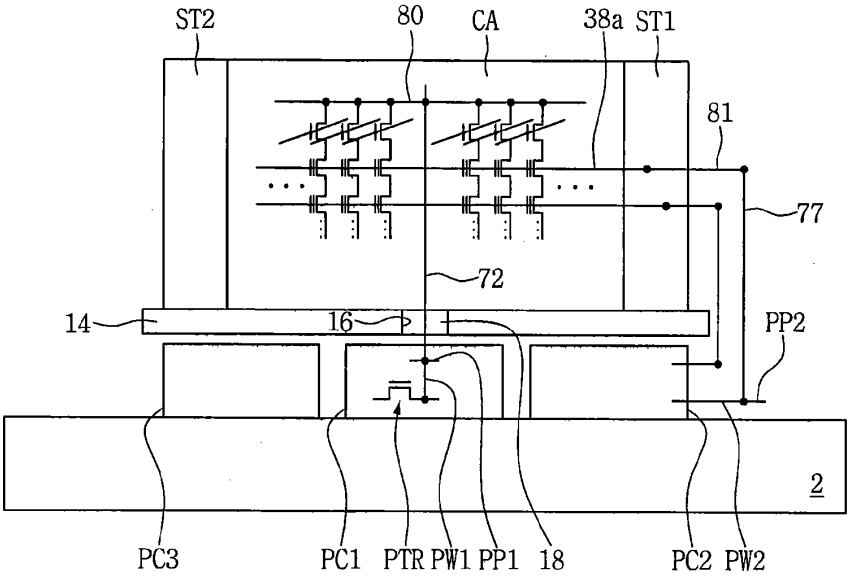

ST2
80
CA
38a
ST1
81
77
72
14
16
PP2
2
PC3
PC1
PTR
PW1
PP1
18
PC2
PW2

FIG. 2A

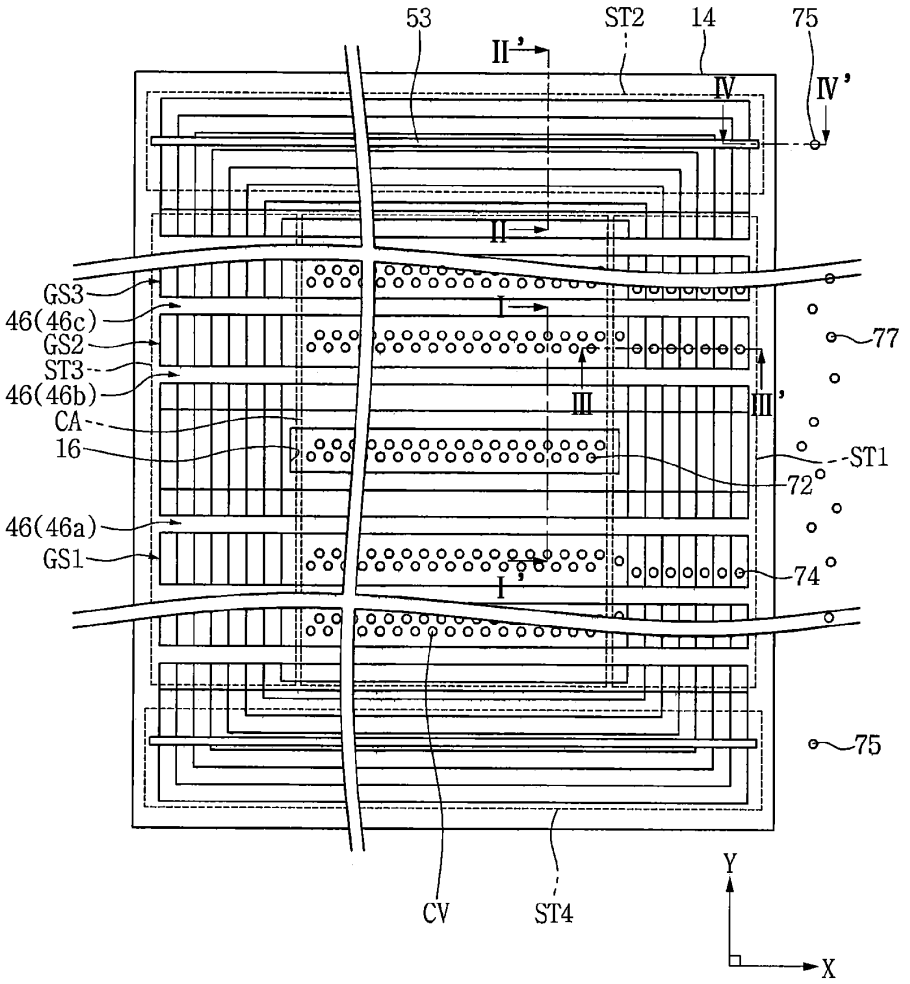

53
ST2
14
75
II'
IV
IV'
II
GS3
46(46c)
GS2
ST3
46(46b)
CA
16
I
III
III'
77
ST1
72
46(46a)
GS1
I'
74
75
CV
ST4
Y
X

FIG. 2B

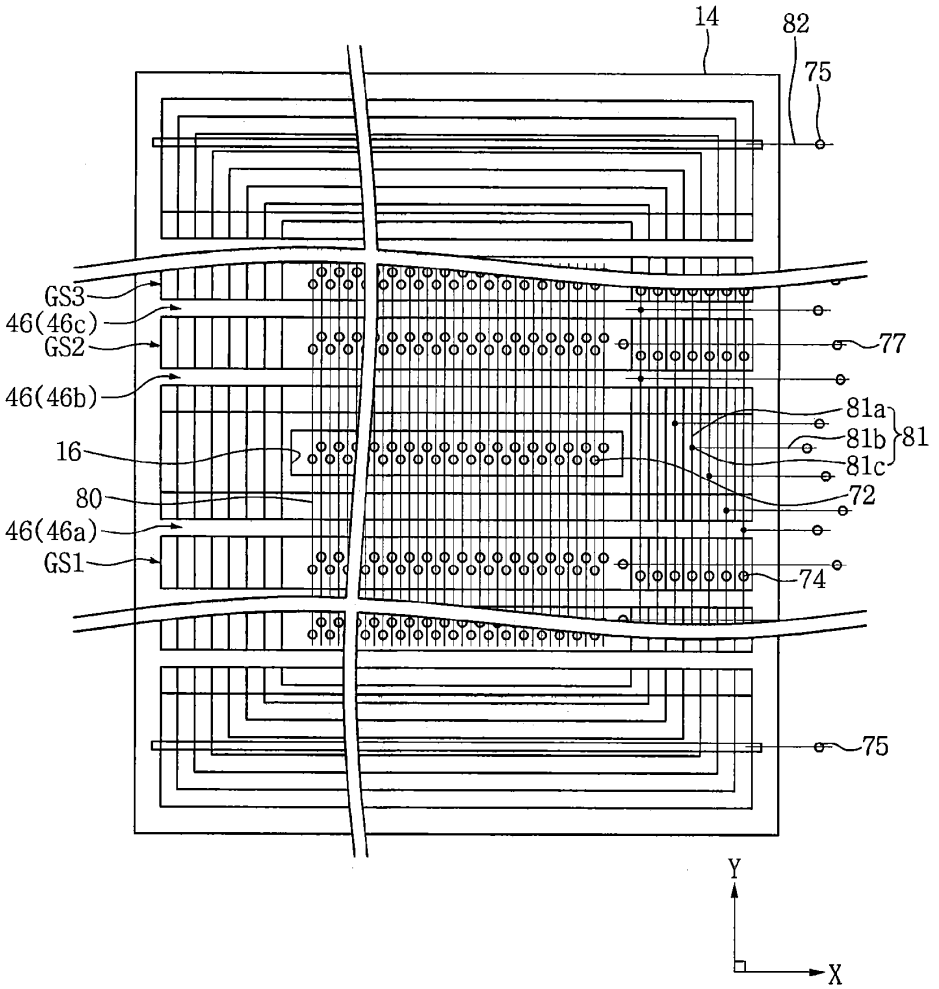

14
82
75
GS3
46(46c)
GS2
46(46b)
16
80
46(46a)
GS1
77
81a
81b
81c
81
72
74
75
Y
X

FIG. 3A

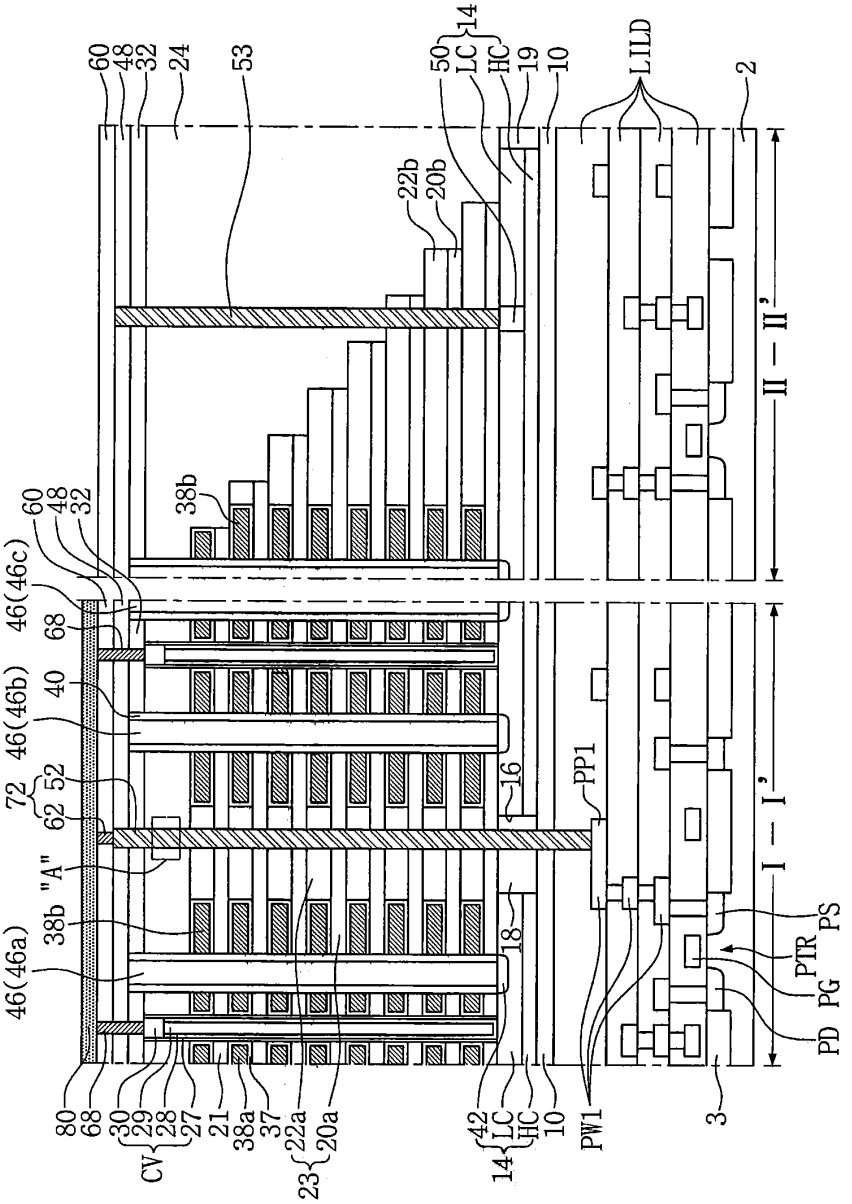

60
48
32
24
53
50
LC
14
HC
19
10
LILD
2
22b
20b
II — II'
38b
46(46c)
68
40
46(46b)
72
52
62
"A"
16
PP1
I — I'
46(46a)
18
PS
PTR
PG
PD
80
30
29
28
27
21
38a
37
22a
20a
CV
23
42
PW1
3

FIG. 3B

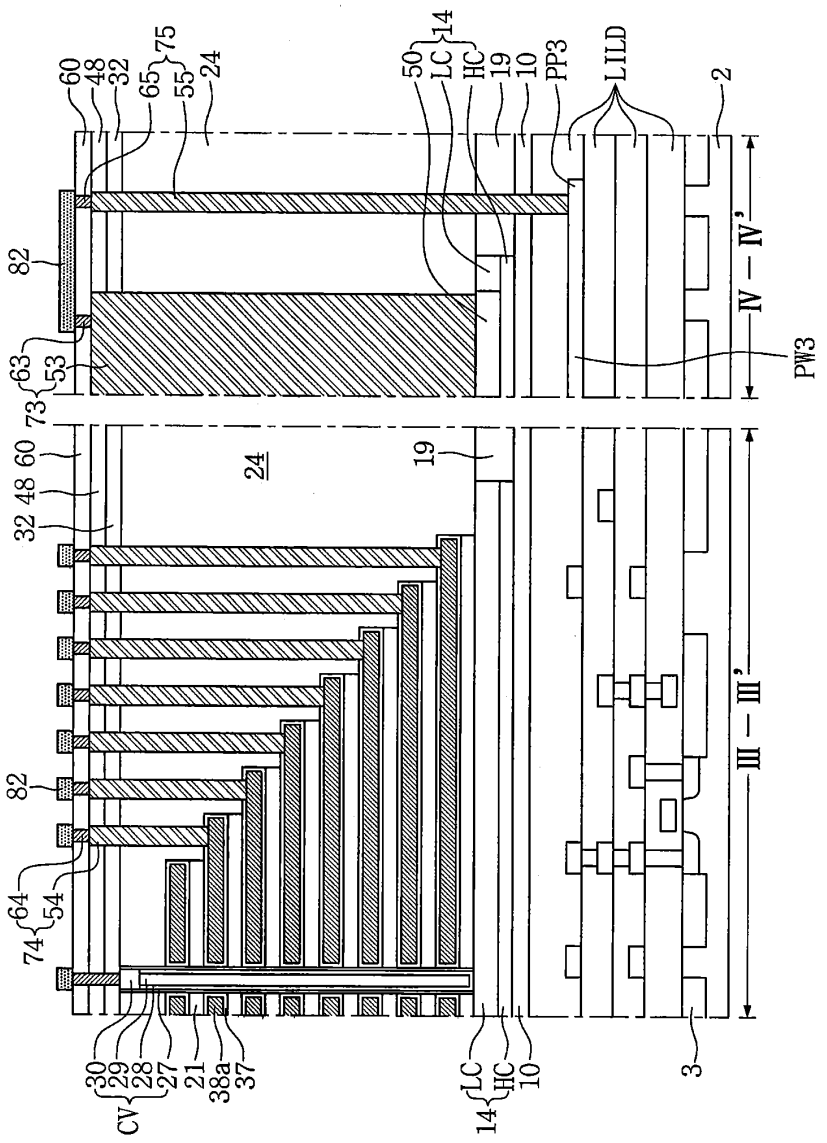

60
48
32
65
75
55
24
50
LC
14
HC
19
10
PP3
LILD
2
82
63
53
73
IV — IV'
PW3
60
48
32
24
19
82
64
54
74
III — III'
30
29
28
27
21
38a
37
CV
LC
HC
14
10
3

FIG. 3C

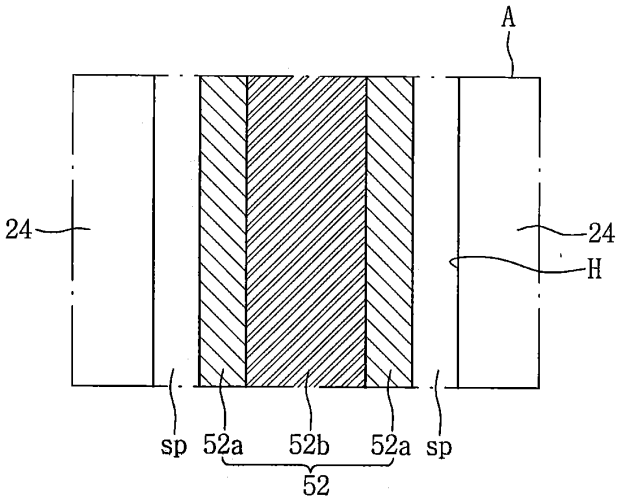


FIG. 4A

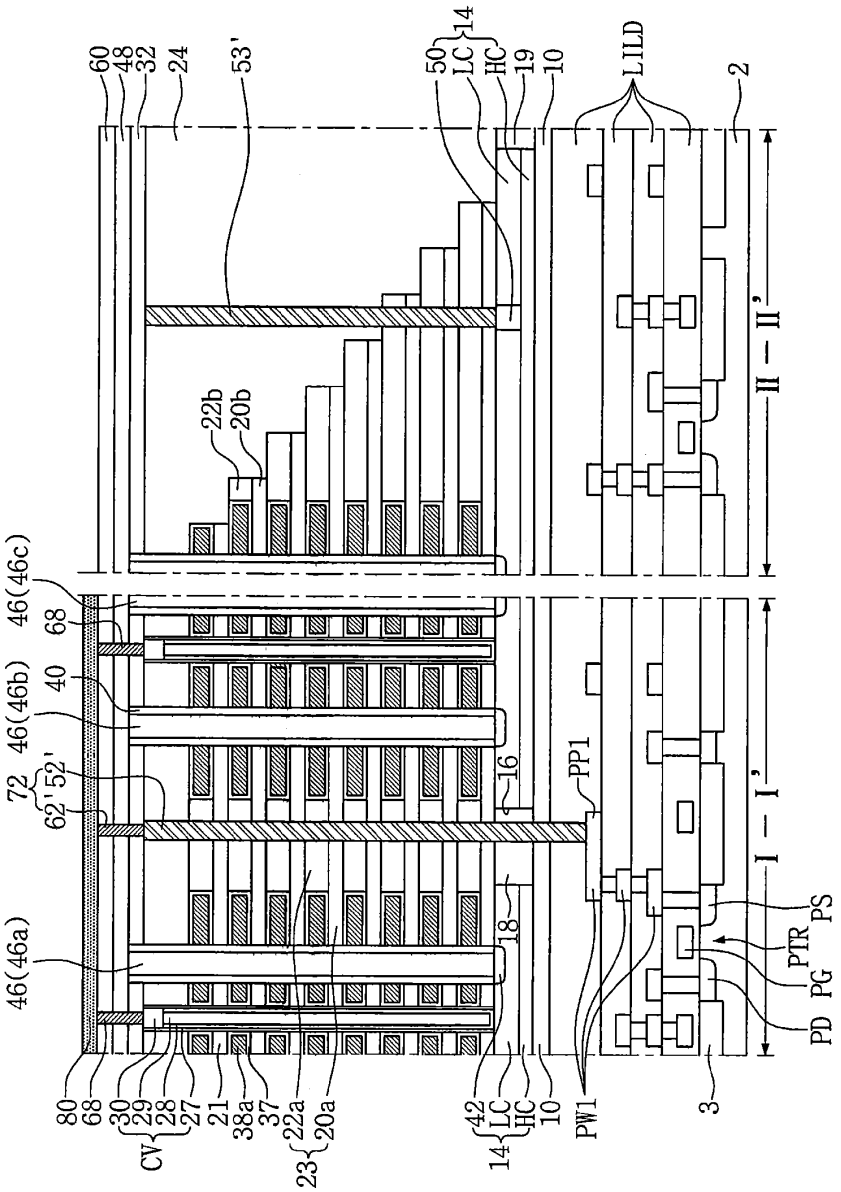

60
48
32
24
53'
50
LC
14
HC
19
10
LILD
2
II — II'
22b
20b
46(46c)
68
46(46b)
40
72
52'
62'
16
PP1
I — I'
46(46a)
18
PS
PTR
PG
PD
80
68
30
29
28
27
CV
21
38a
37
22a
20a
23
42
LC
HC
14
10
PW1
3

FIG. 4B

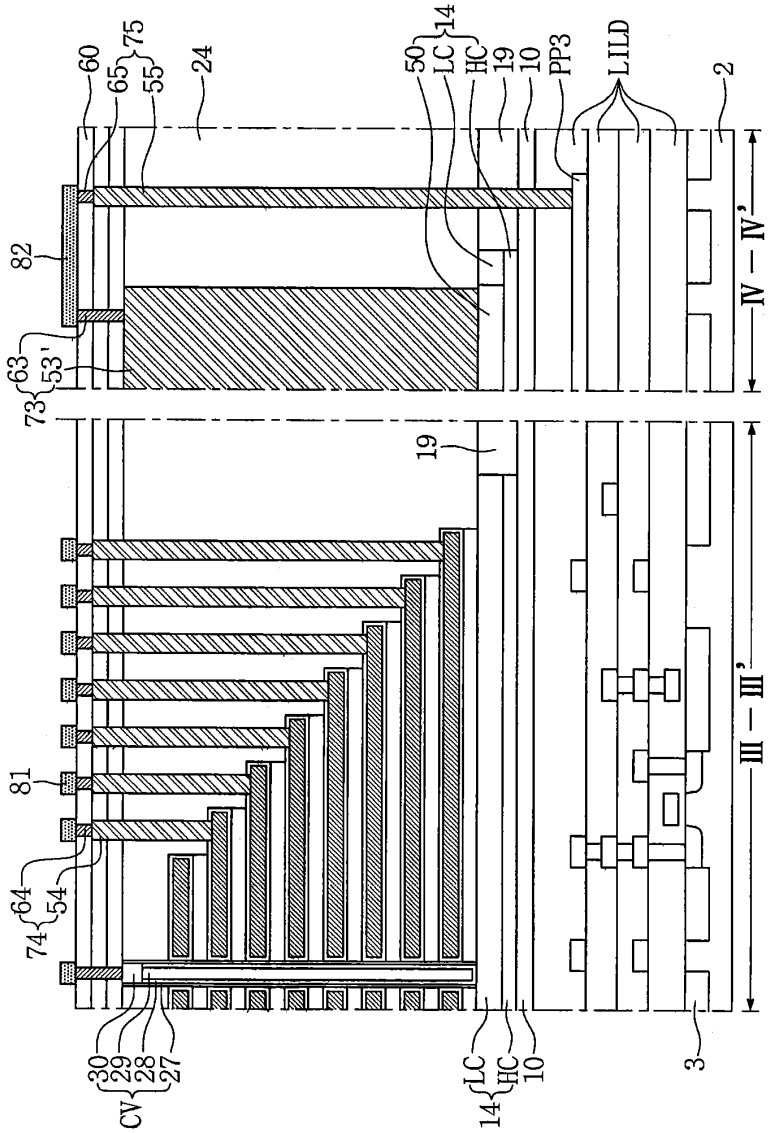

60
65
75
55
24
50
LC
14
HC
19
10
PP3
LILD
2
82
63
53'
73
IV – IV'
19
81
64
54
74
III – III'
30
29
28
27
CV
LC
HC
14
10
3

FIG. 5A

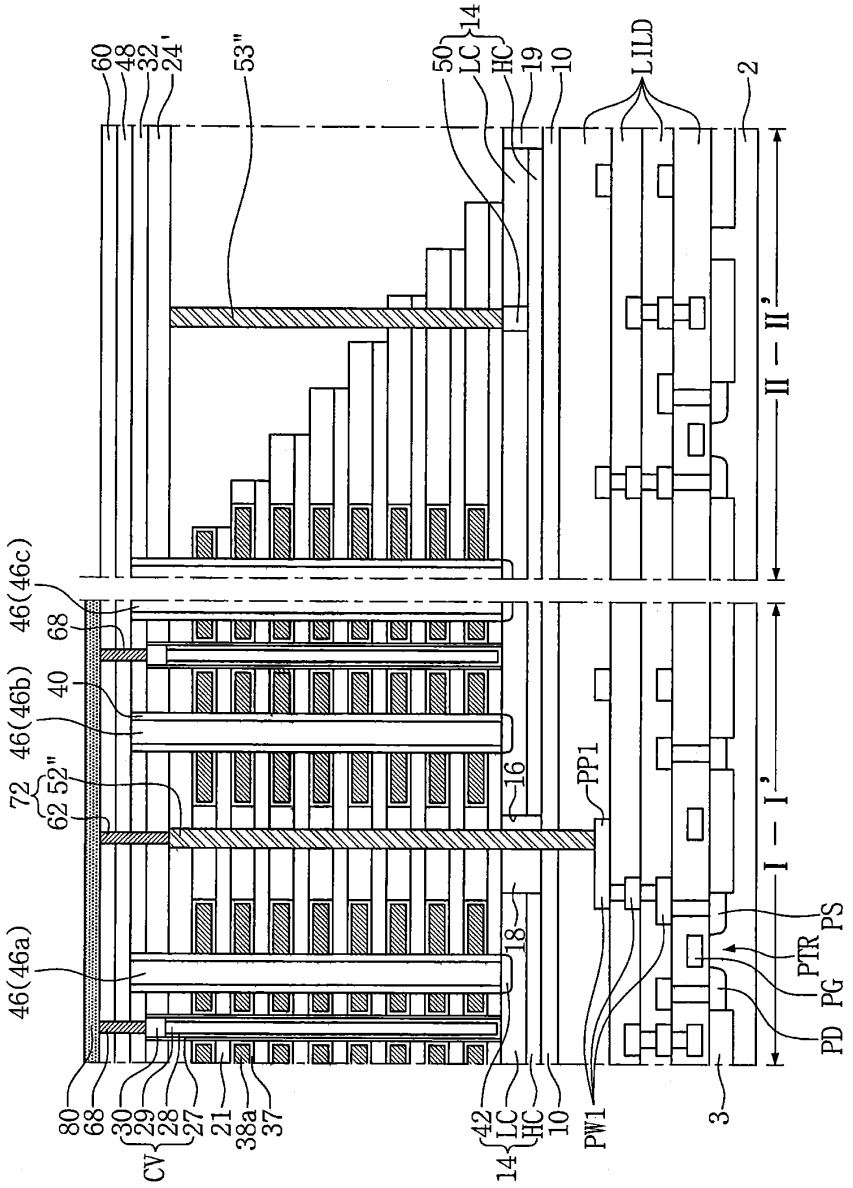

60
48
32
24'
53"
50
LC
14
HC
19
10
LILD
2
II – II'
46(46c)
68
46(46b)
40
72
52"
62
16
PP1
I – I'
46(46a)
18
PS
PTR
PG
PD
80
68
30
29
28
27
21
38a
37
CV
42
LC
14
HC
10
PW1
3

FIG. 5B

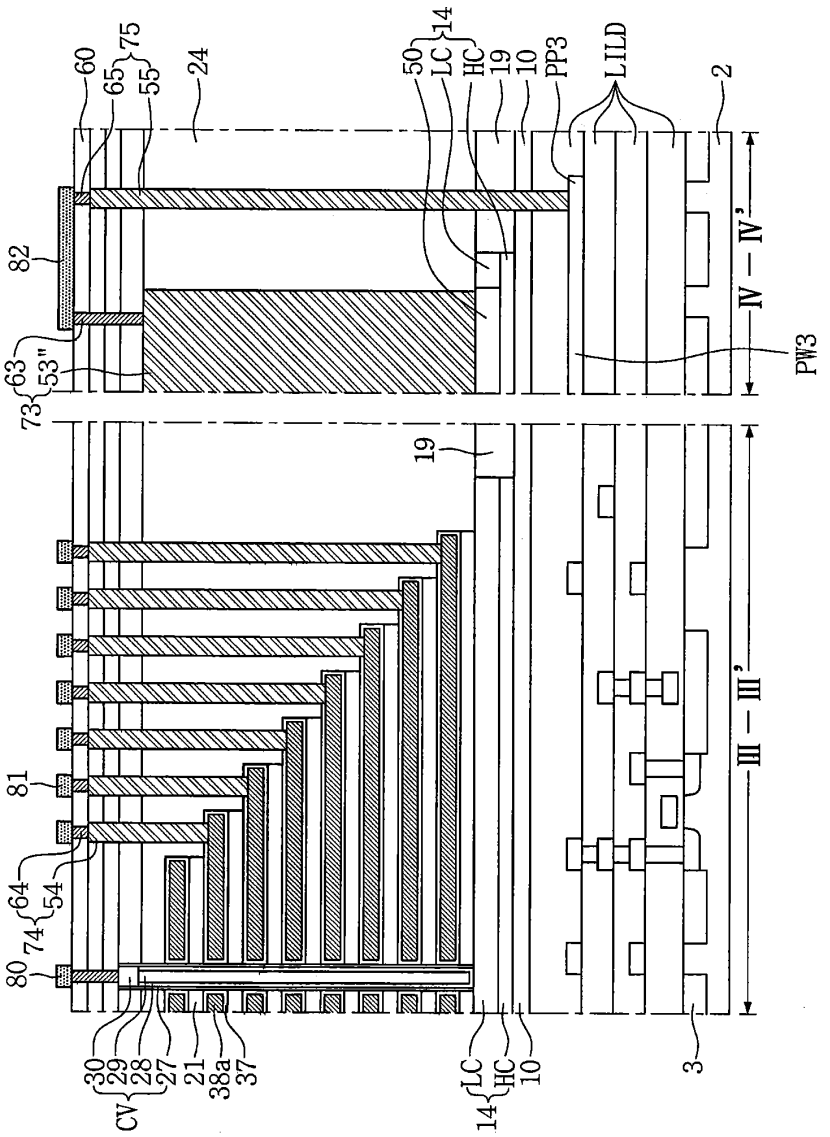

60
65
75
55
24
50
14
LC
HC
19
10
PP3
LILD
2
82
63
53"
73
IV – IV'
PW3
19
III – III'
81
64
54
74
80
30
29
28
27
21
38a
37
CV
14
LC
HC
10
3

FIG. 6

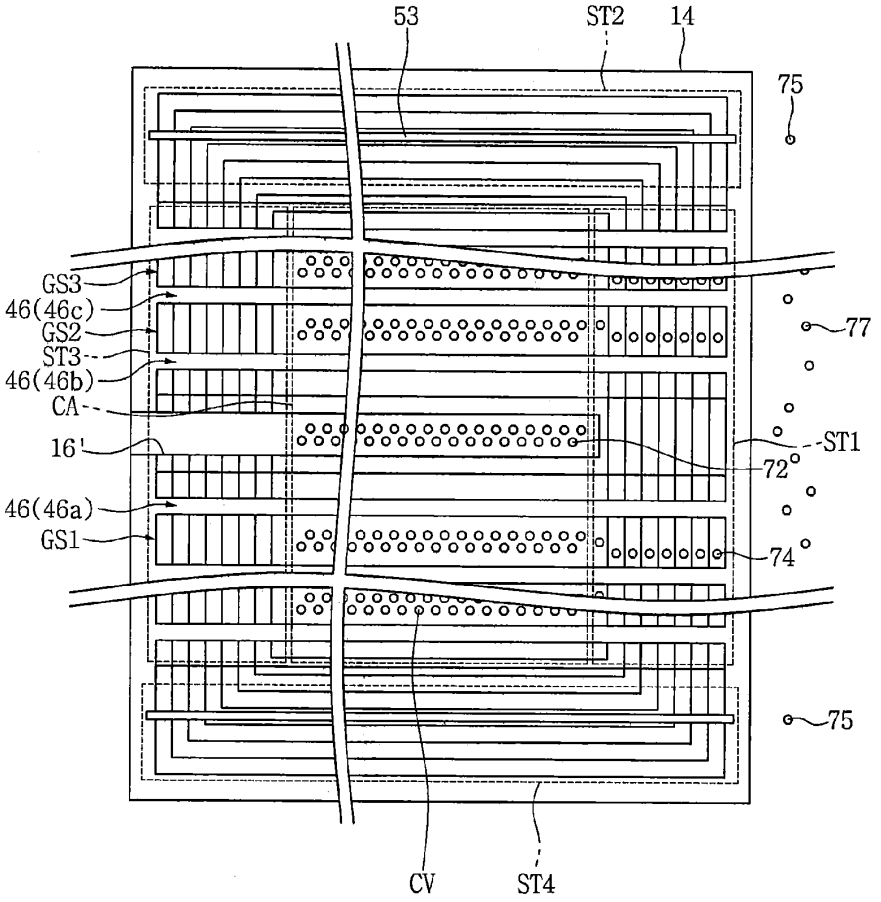

53
ST2
14
75
GS3
46(46c)
GS2
ST3
46(46b)
CA
16'
46(46a)
GS1
77
ST1
72
74
75
CV
ST4

FIG. 7

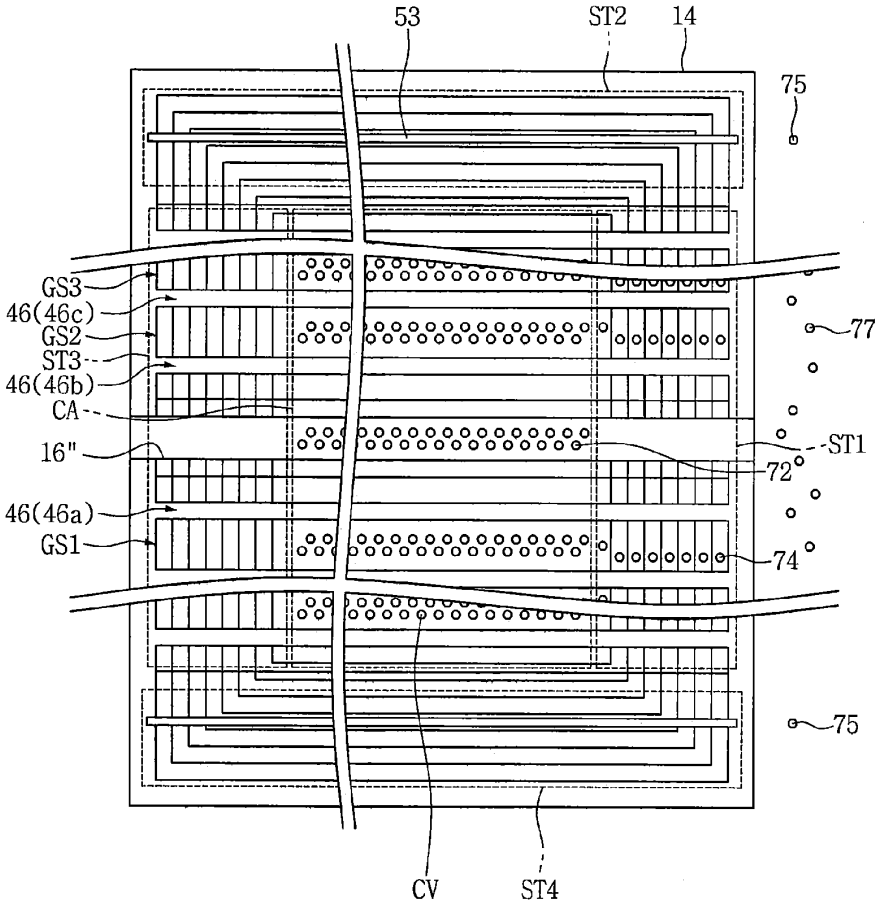

53
ST2
14
75
GS3
46(46c)
GS2
ST3
46(46b)
CA
16"
46(46a)
GS1
77
ST1
72
74
75
CV
ST4

FIG. 8

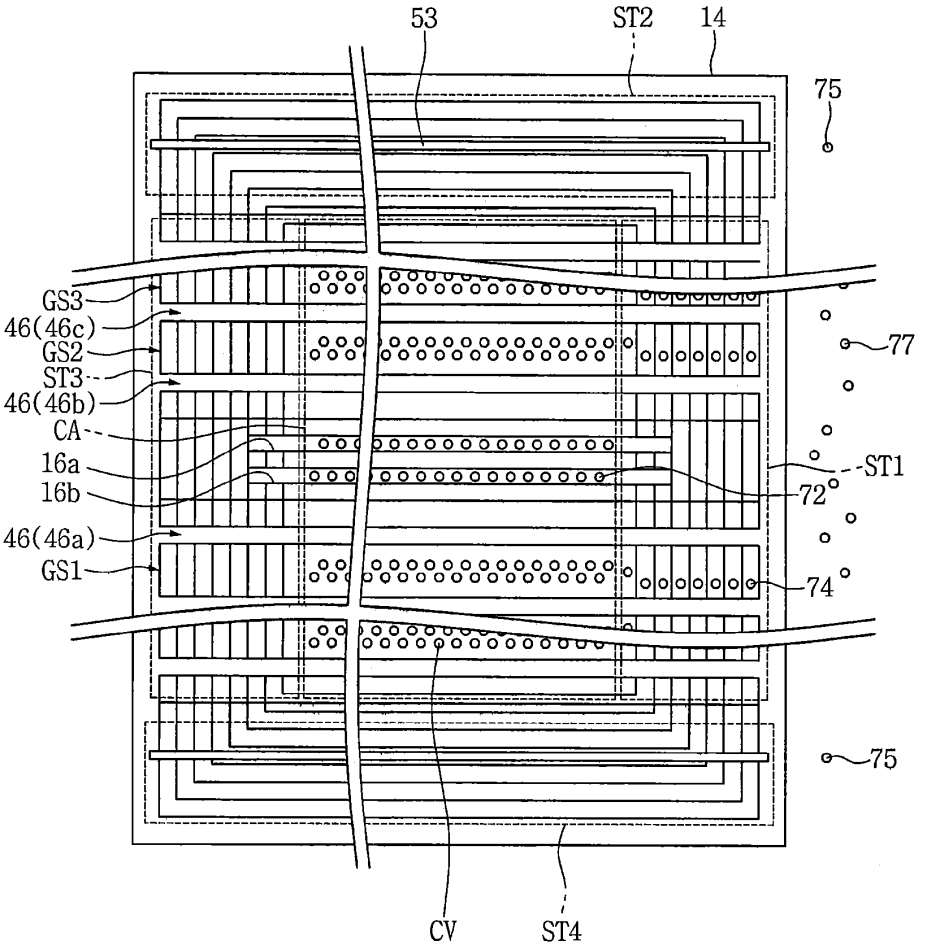

53
ST2
14
75
GS3
46(46c)
GS2
ST3
46(46b)
CA
16a
16b
46(46a)
GS1
77
ST1
72
74
75
CV
ST4

FIG. 9

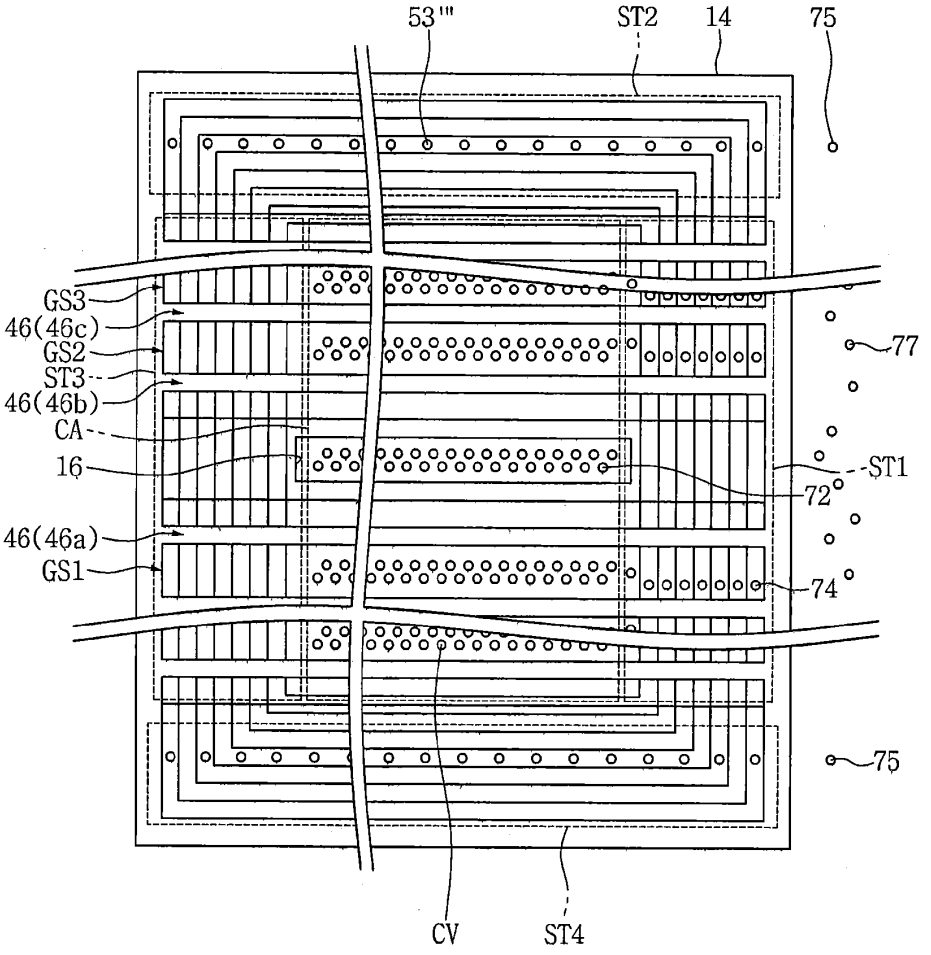

53'''
ST2
14
75
GS3
46(46c)
GS2
ST3
46(46b)
CA
16
46(46a)
GS1
77
ST1
72
74
75
CV
ST4

FIG. 10

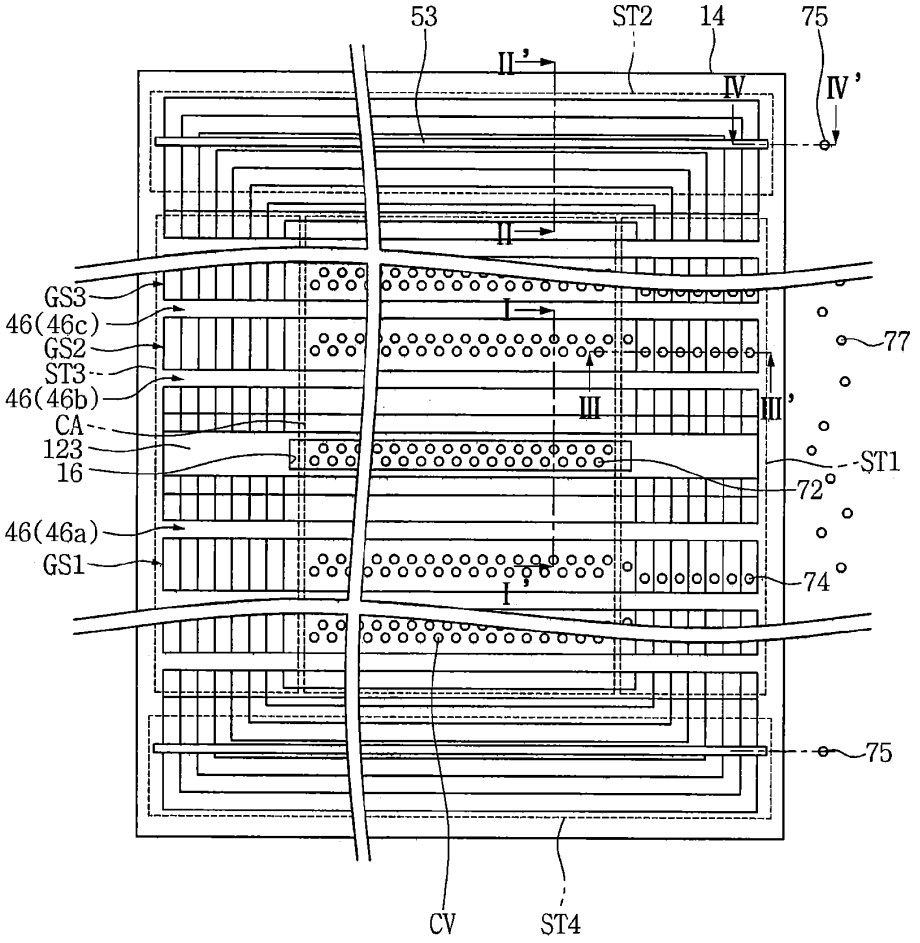

53
ST2
14
75
II'
IV
IV'
II
GS3
46(46c)
GS2
ST3
46(46b)
CA
123
16
I
III
III'
77
ST1
72
46(46a)
GS1
74
I'
75
CV
ST4

FIG. 11A

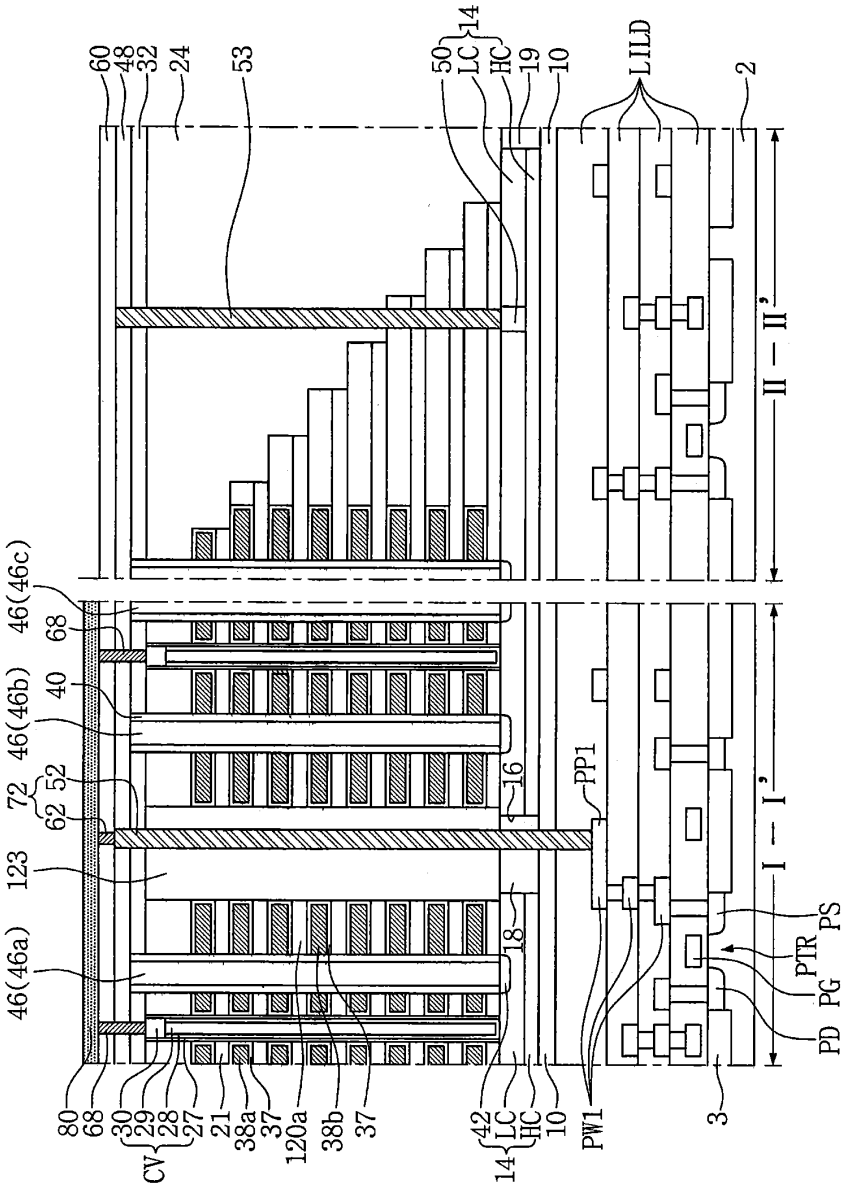

60
48
32
24
53
50
LC
14
HC
19
10
LILD
2
II – II'
46(46c)
68
40
46(46b)
72
52
62
123
46(46a)
16
PP1
18
I – I'
PS
PTR
PG
PD
80
68
30
29
28
27
CV
21
38a
37
120a
38b
37
42
LC
14
HC
10
PW1
3

FIG. 11B

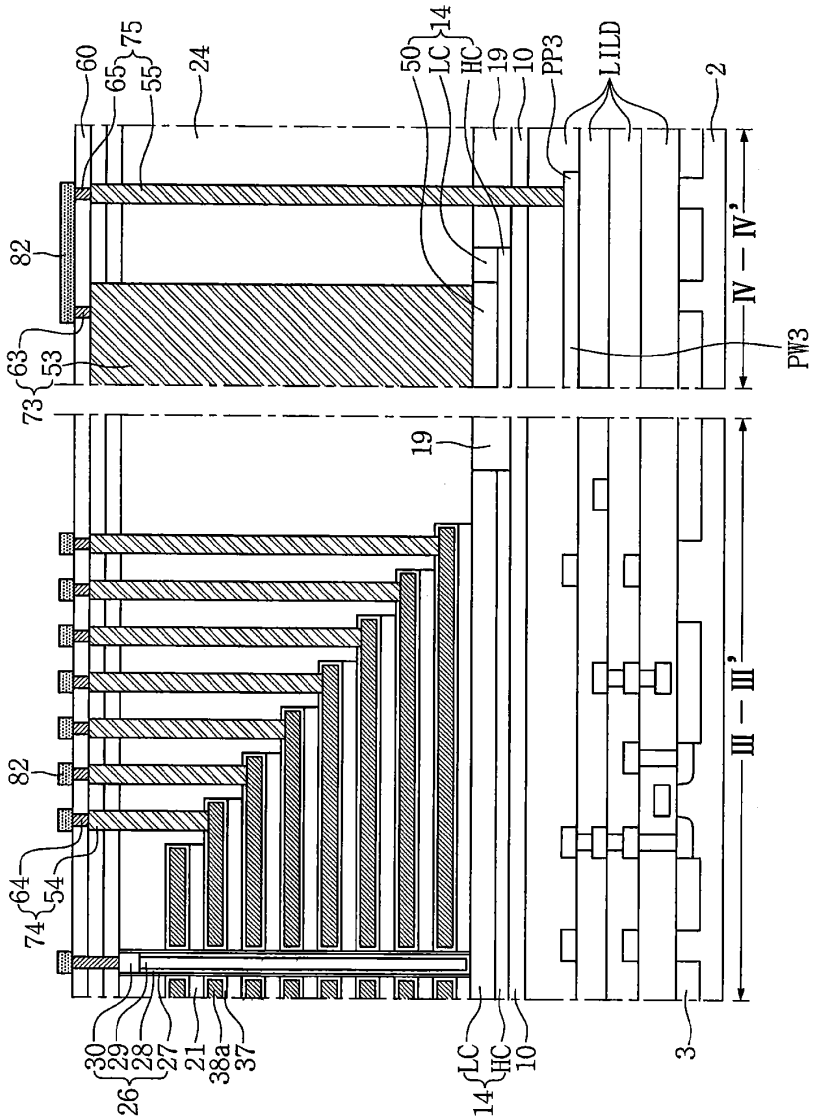

60
65
75
55
24
50
LC
14
HC
19
10
PP3
LILD
2
82
63
53
73
IV – IV'
PW3
19
III – III'
82
64
54
74
30
29
28
27
26
21
38a
37
LC
HC
14
10
3

FIG. 12

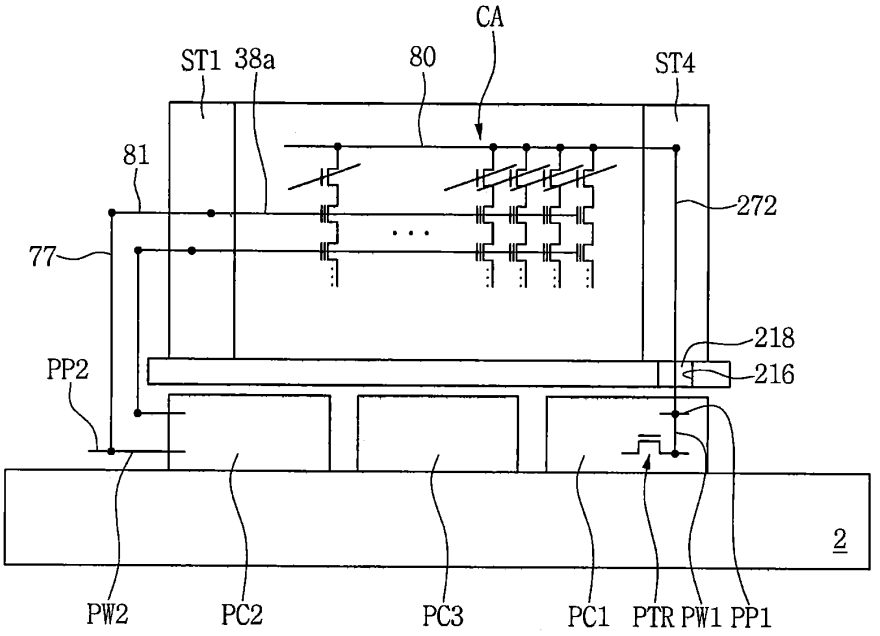

CA
ST1
38a
80
ST4
81
272
77
218
216
PP2
2
PW2
PC2
PC3
PC1
PTR
PW1
PP1

FIG. 13A

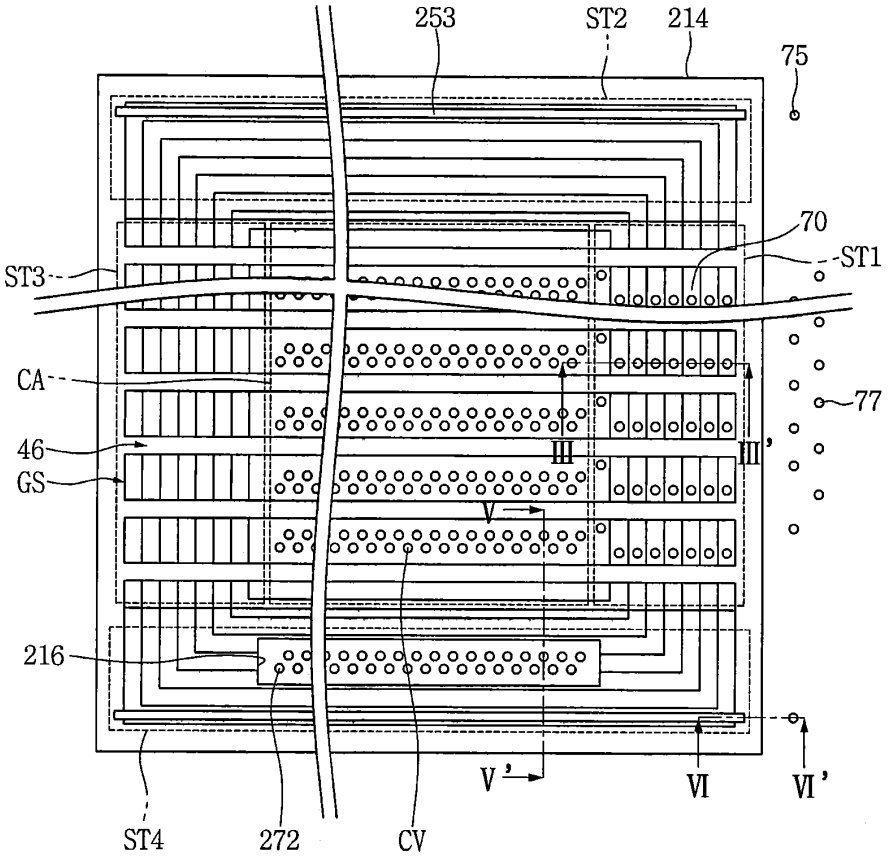

253
ST2
214
75
70
ST1
ST3
CA
77
46
GS
III
III'
V
216
V'
VI
VI'
ST4
272
CV

FIG. 13B

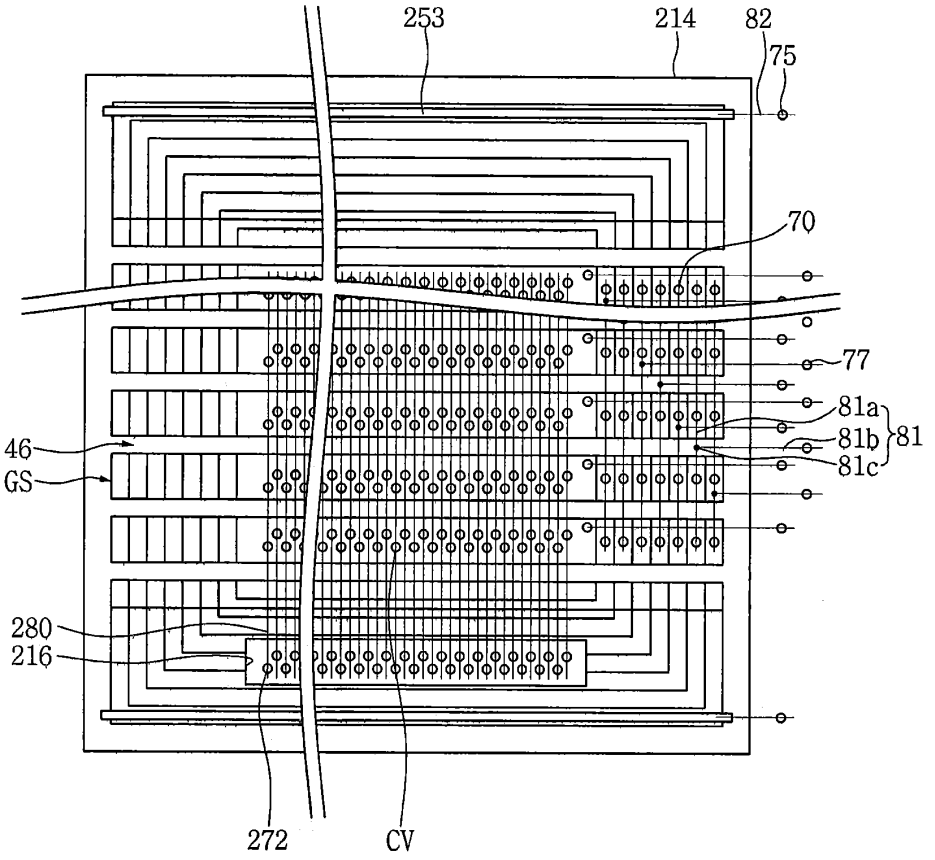


FIG. 14

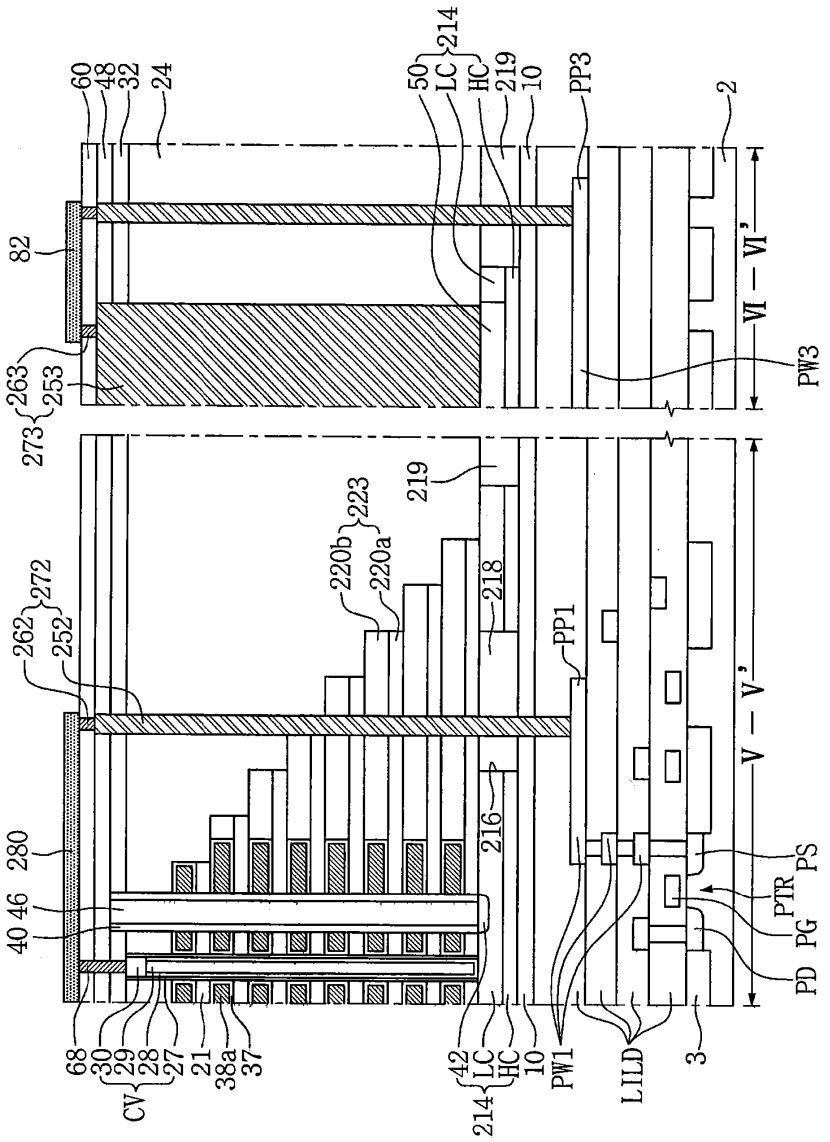
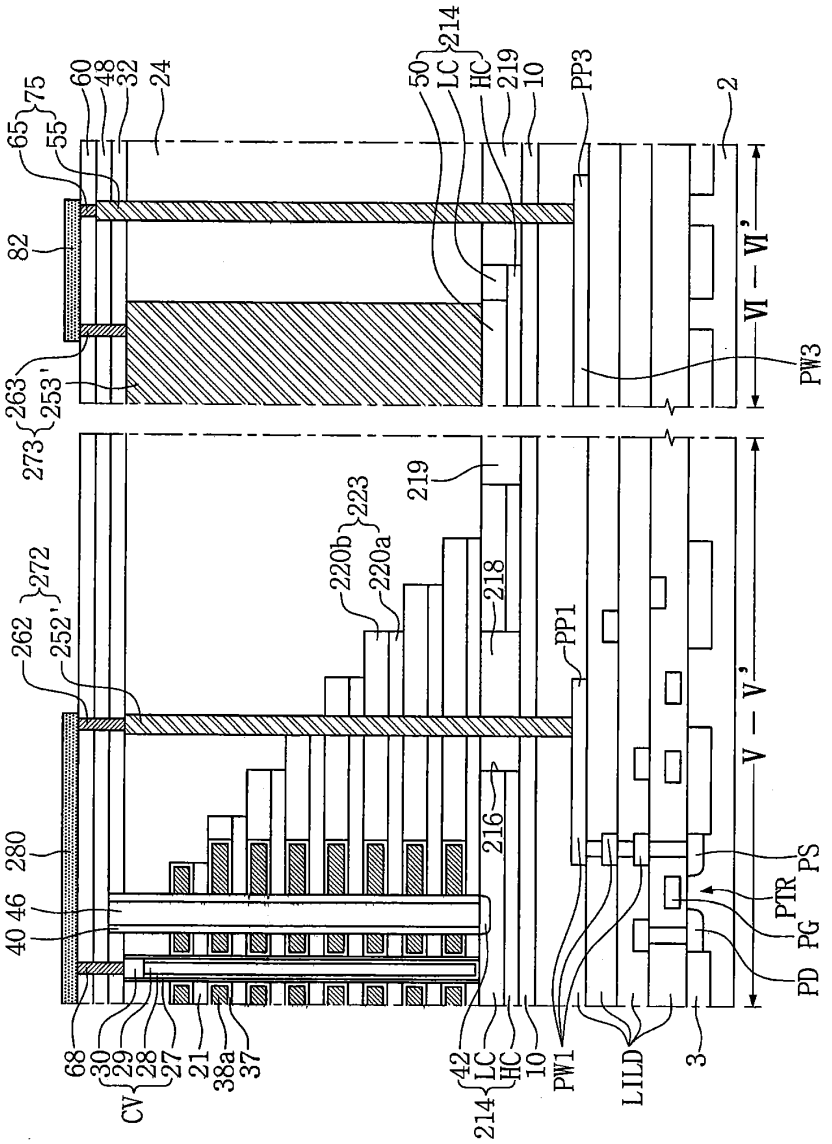
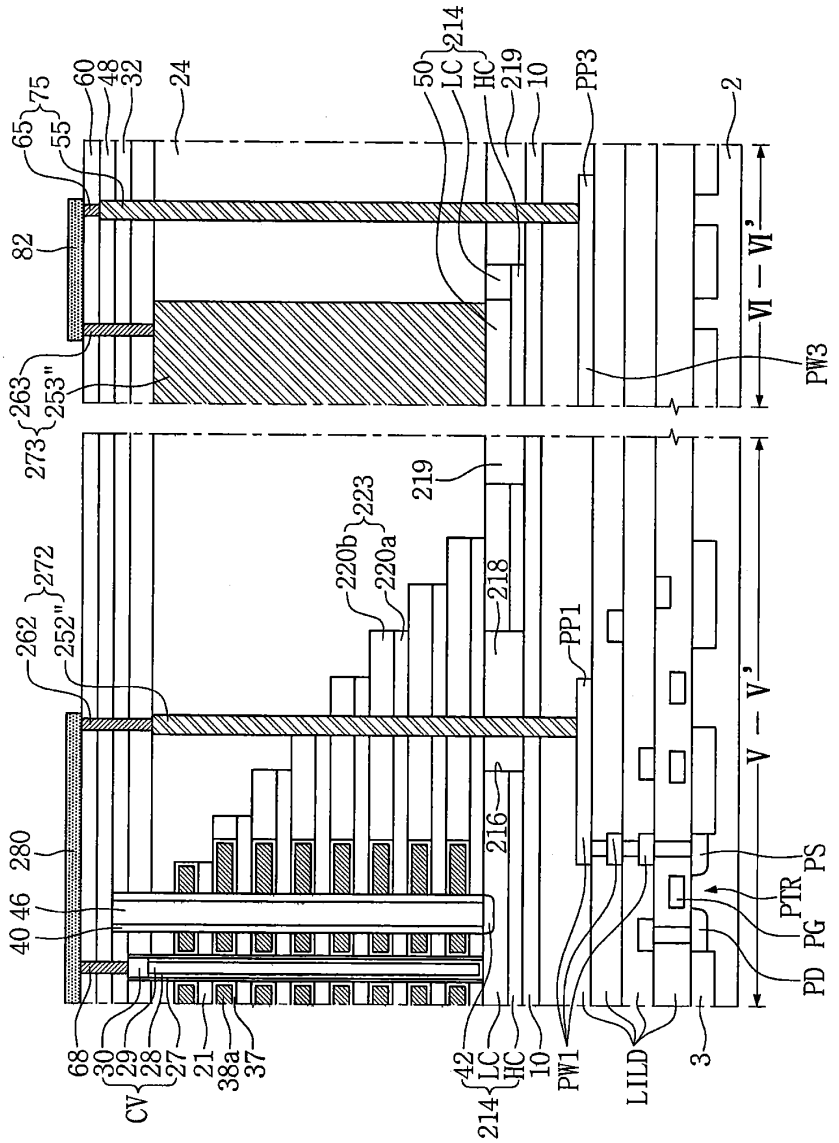

60
48
32
24
82
263
253
273
262
252
272
280
40
46
68
30
29
28
27
21
38a
37
CV
50
LC
214
HC
219
10
PP3
2
VI — VI'
PW3
223
220b
220a
218
216
PP1
V — V'
PS
PTR
PG
PD
42
PW1
LILD
3

FIG. 15



65
75
55
60
48
32
24
82
263
253'
273
50
LC
214
HC
219
10
PP3
2
VI – VI'
PW3
262
252'
272
220b
220a
223
219
218
PP1
V – V'
280
40
46
216
PS
PTR
PG
PD
68
30
29
28
27
21
38a
37
CV
42
LC
HC
10
214
PW1
LILD
3

FIG. 16



65
55
75
60
48
32
24
82
263
253"
273
50
LC
214
HC
219
10
PP3
2
VI – VI'
PW3
262
252"
272
220b
220a
223
218
PP1
V – V'
280
40
46
216
PS
PTR
PG
PD
68
30
29
28
27
21
38a
37
CV
42
LC
HC
214
10
PW1
LILD
3

FIG. 17

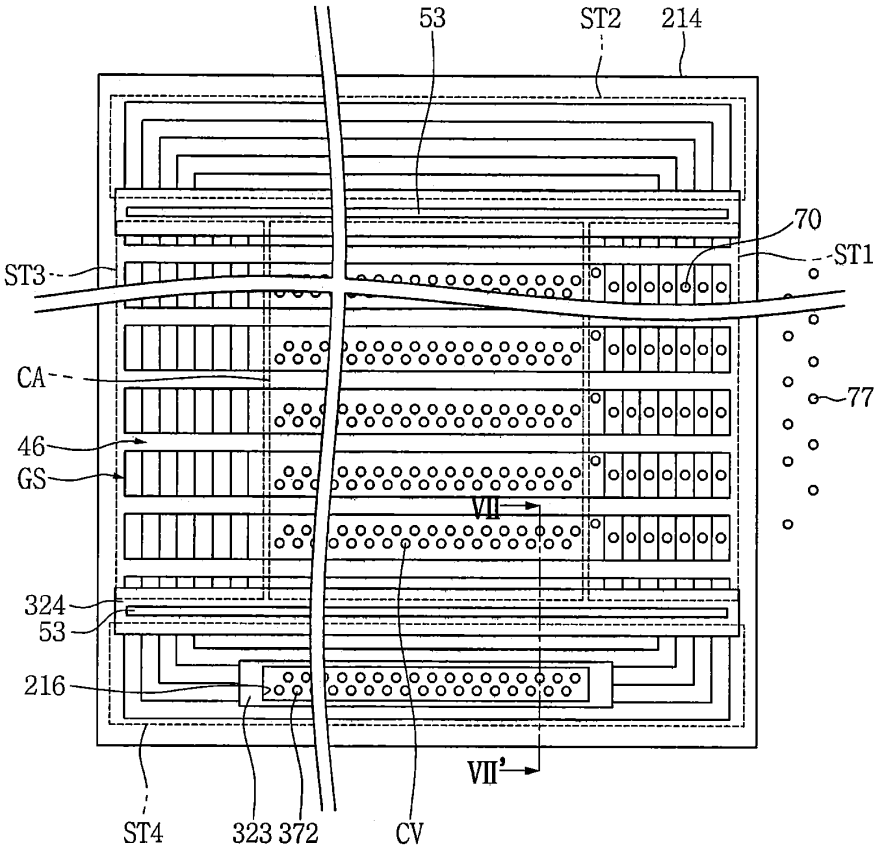


FIG. 18

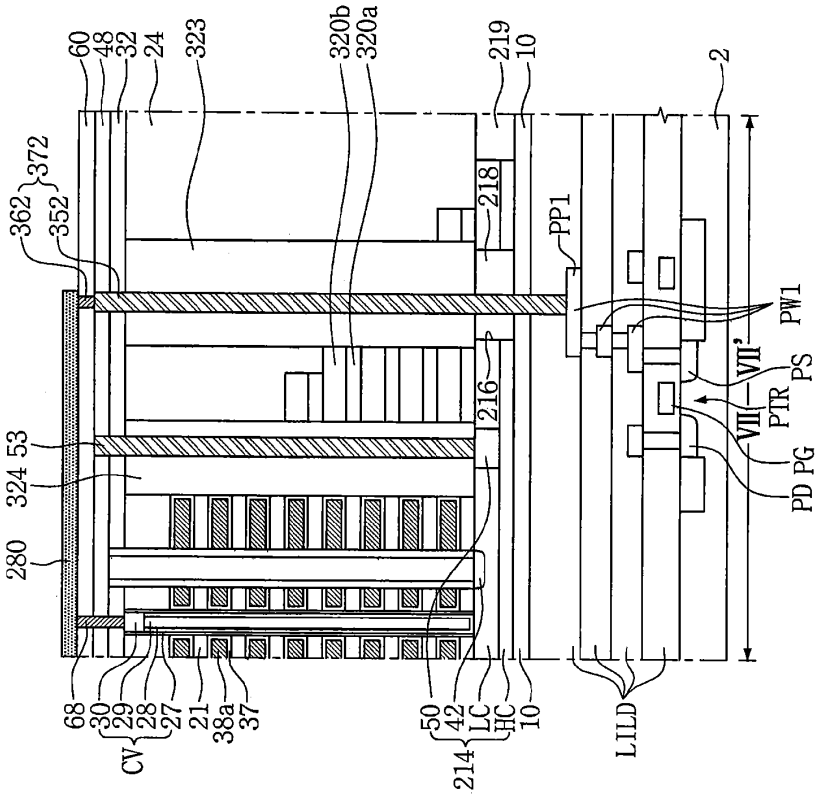

60
48
32
24
323
320b
320a
219
10
2
372
362
352
218
PP1
PW1
VII'
PS
PTR
VII
PG
PD
216
53
324
280
68
30
29
28
27
21
38a
37
CV
50
42
214
LC
HC
10
LILD

FIG. 19

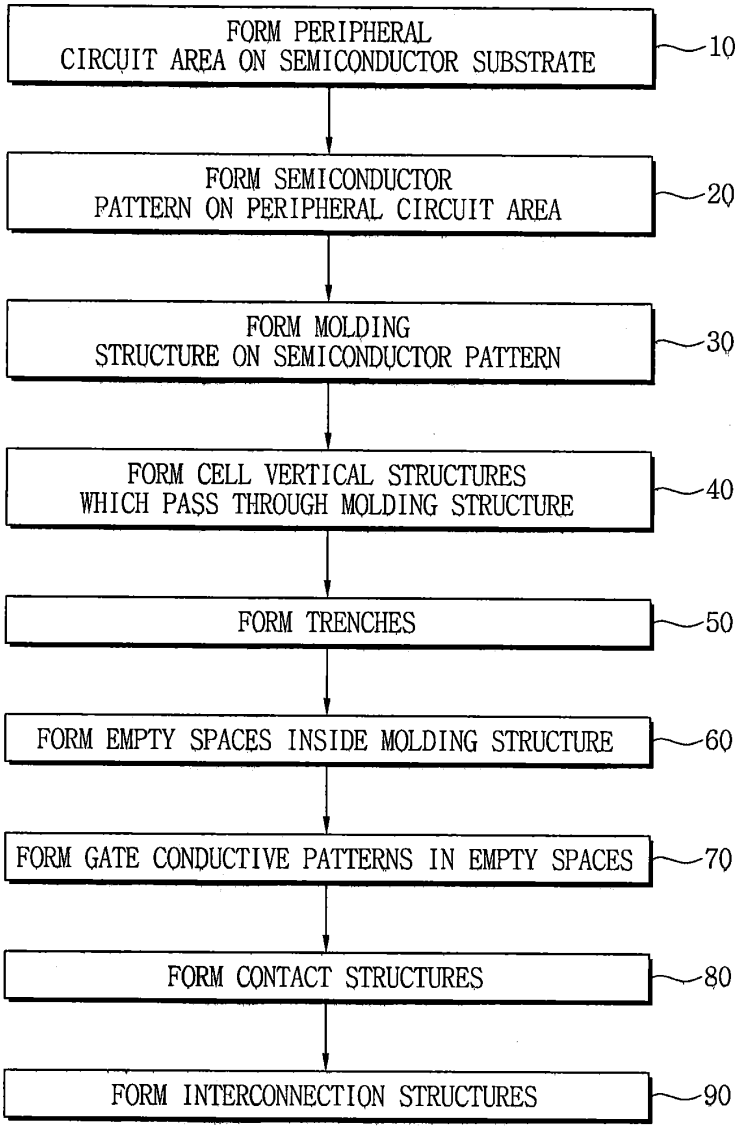

FORM PERIPHERAL CIRCUIT AREA ON SEMICONDUCTOR SUBSTRATE
10
FORM SEMICONDUCTOR PATTERN ON PERIPHERAL CIRCUIT AREA
20
FORM MOLDING STRUCTURE ON SEMICONDUCTOR PATTERN
30
FORM CELL VERTICAL STRUCTURES WHICH PASS THROUGH MOLDING STRUCTURE
40
FORM TRENCHES
50
FORM EMPTY SPACES INSIDE MOLDING STRUCTURE
60
FORM GATE CONDUCTIVE PATTERNS IN EMPTY SPACES
70
FORM CONTACT STRUCTURES
80
FORM INTERCONNECTION STRUCTURES
90

FIG. 20A

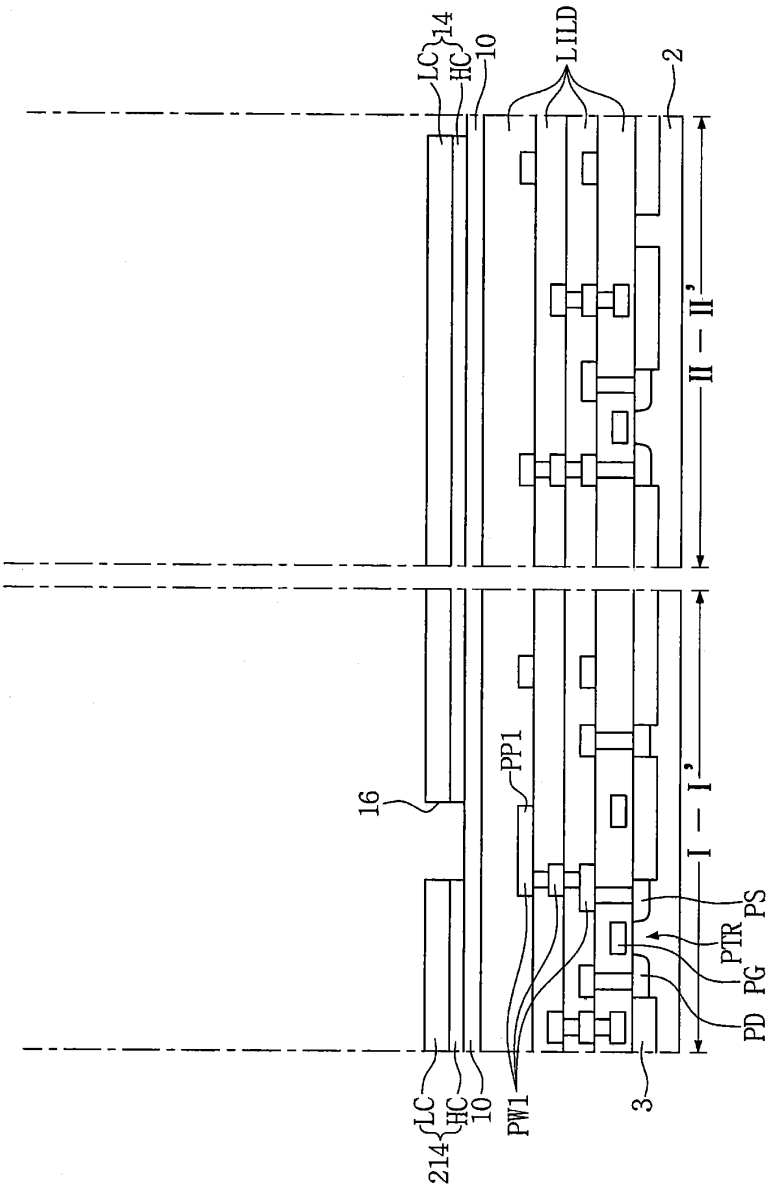


FIG. 20B

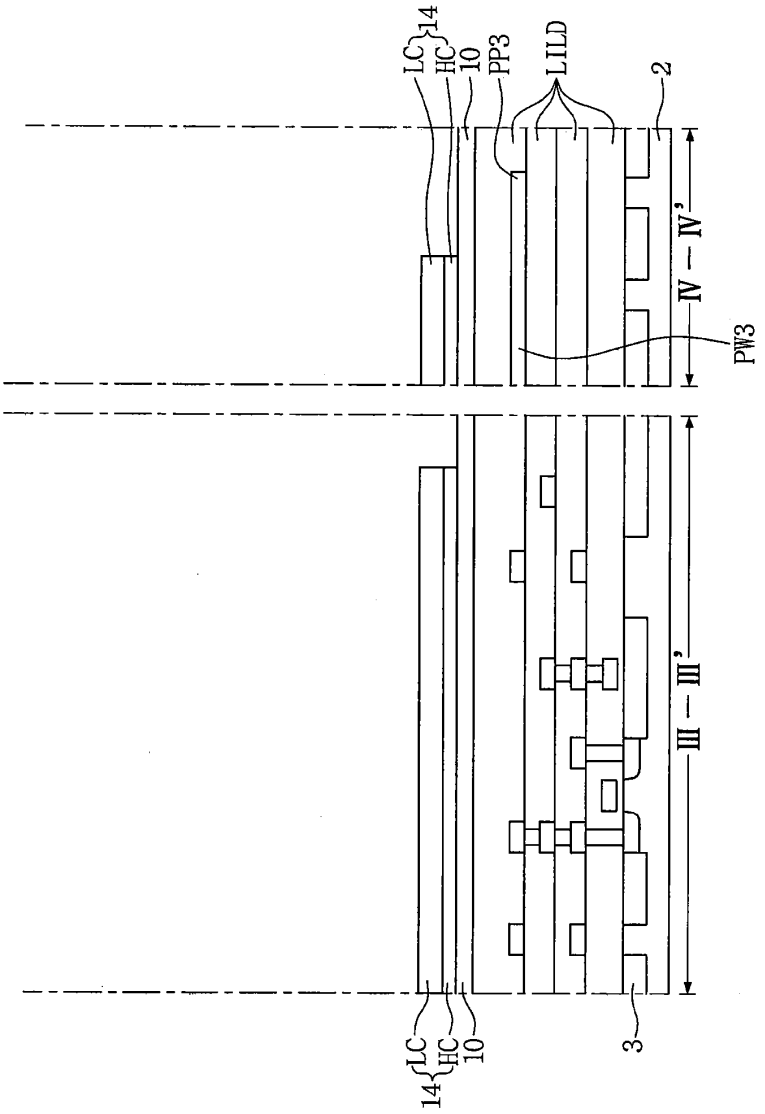


FIG. 21A

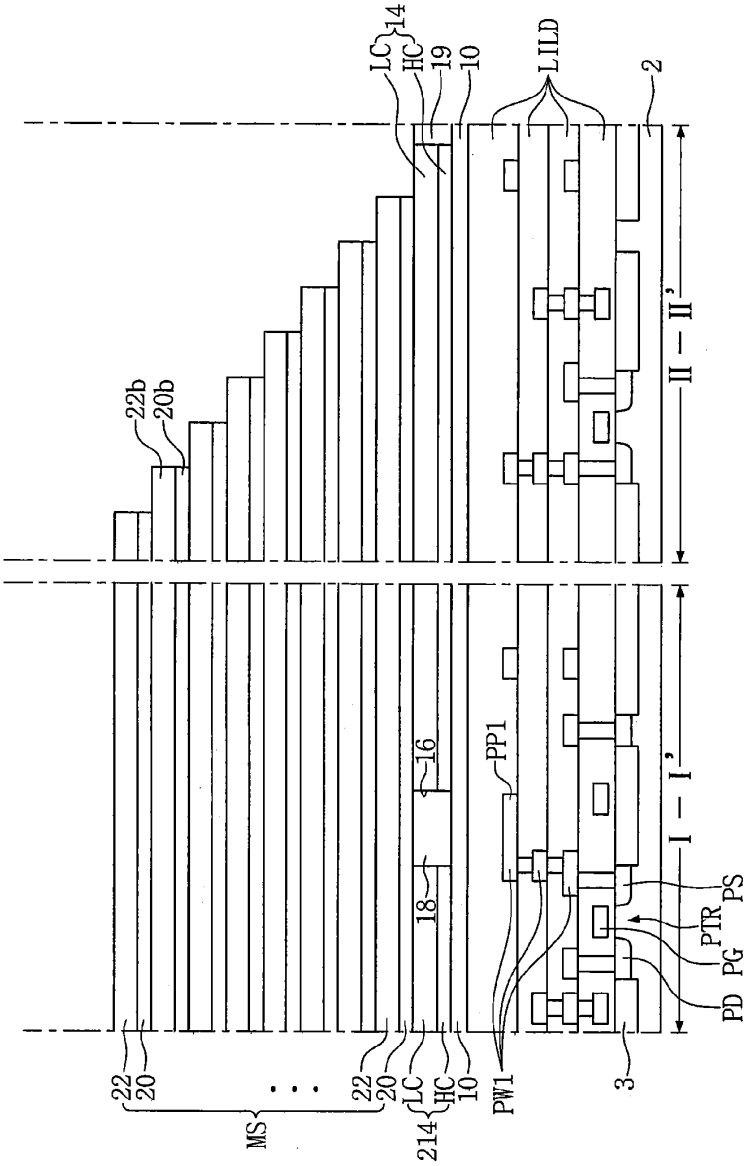

LC
HC
14
19
10
LILD
2
22b
20b
II – II'
I – I'
16
18
PP1
PS
PTR
PG
PD
22
20
MS
LC
HC
214
10
PW1
3

FIG. 21B

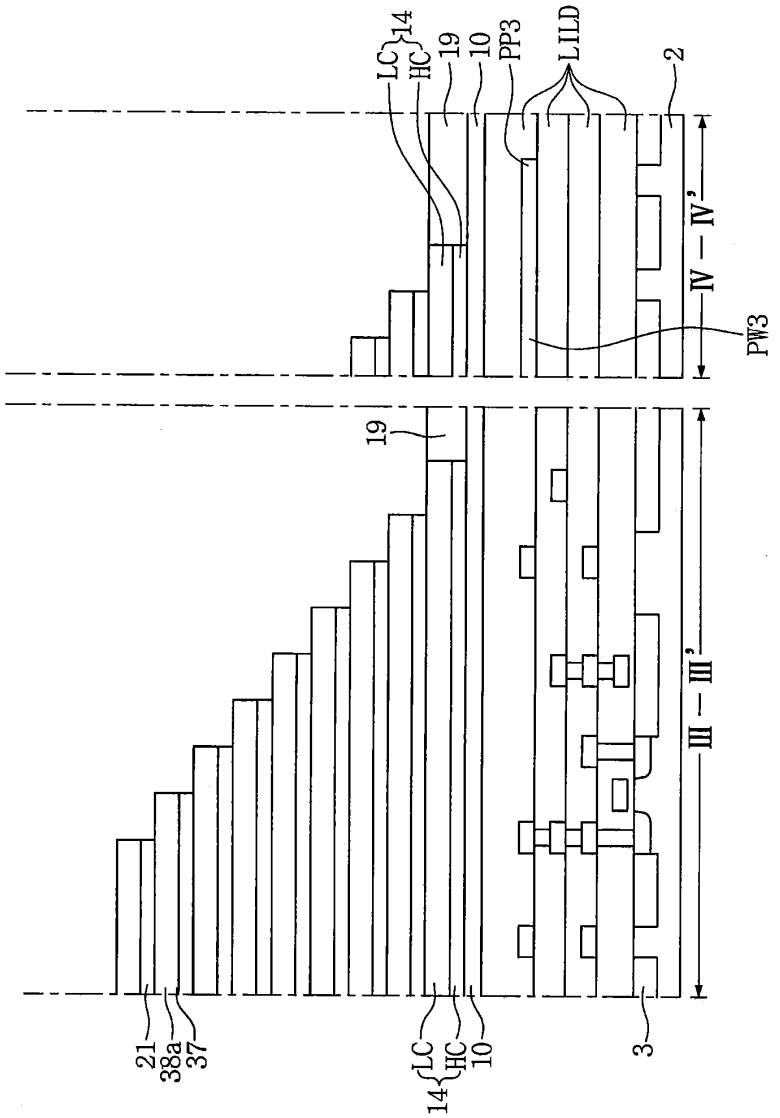


FIG. 22A

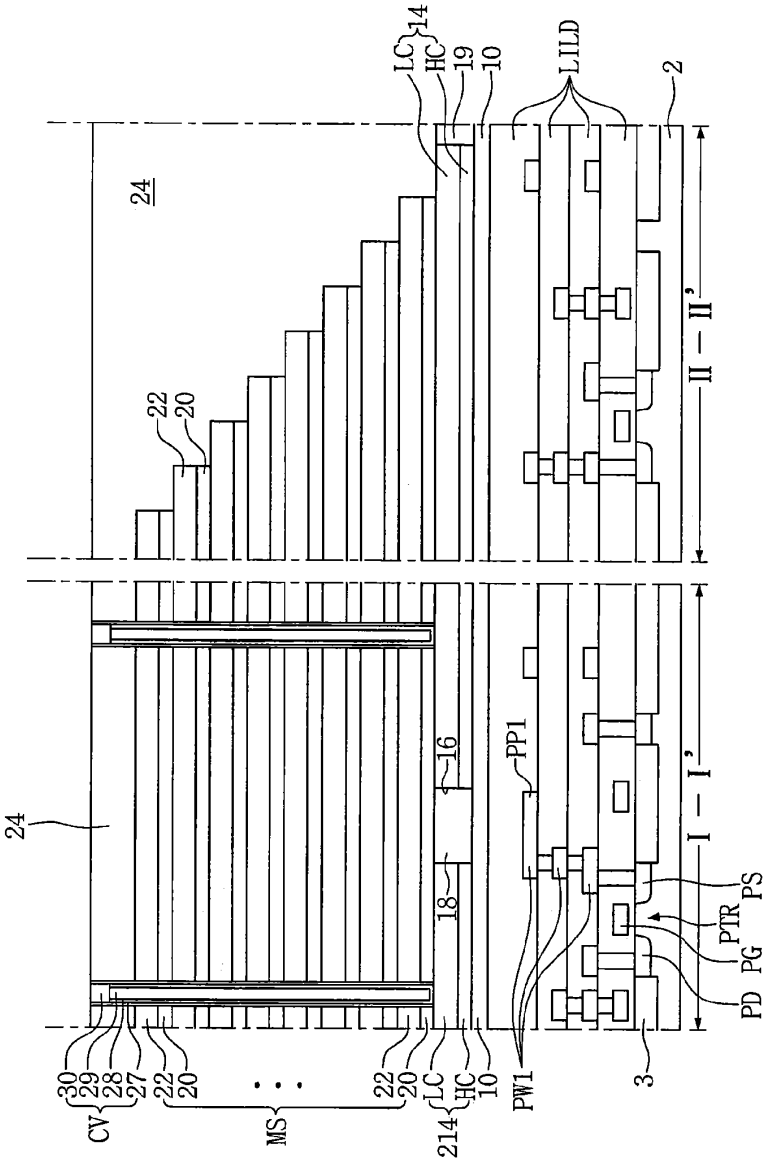

24
22
20
LC
14
HC
19
10
LILD
2
II – II'
24
16
18
PP1
I – I'
PS
PTR
PG
PD
3
30
29
28
27
22
20
CV
MS
22
20
LC
214
HC
10
PW1

FIG. 22B

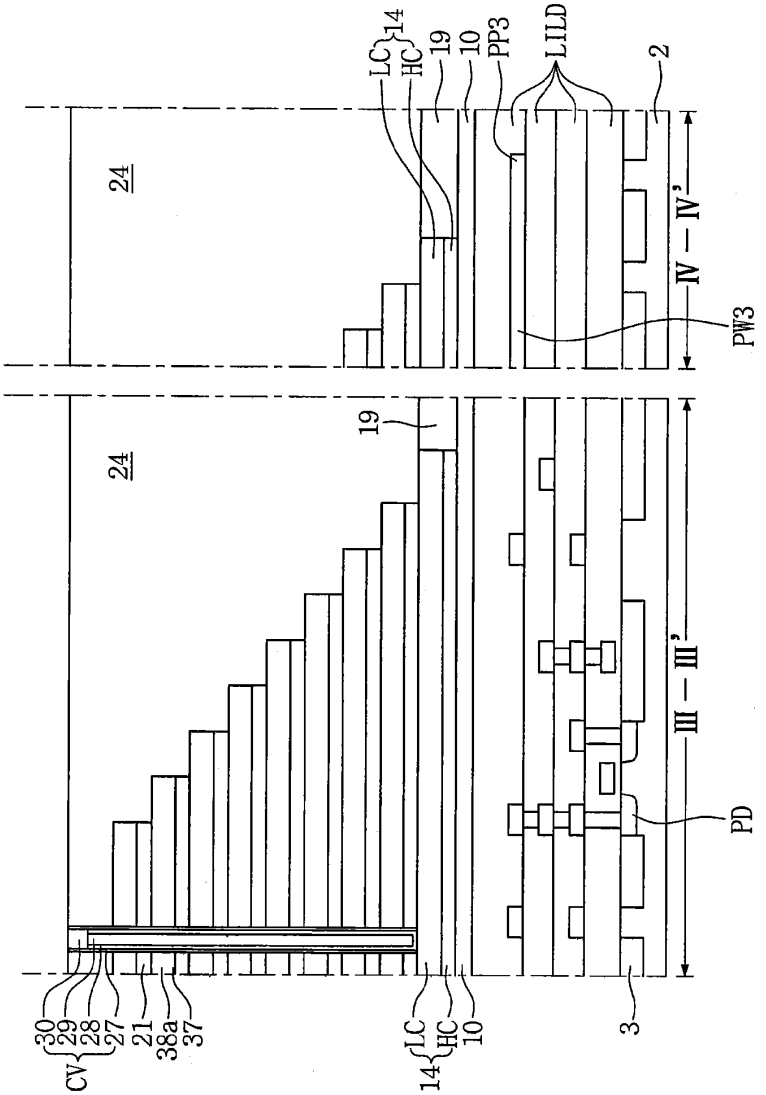

24
24
LC
HC
14
19
10
PP3
LILD
2
IV – IV'
PW3
19
III – III'
PD
3
30
29
28
27
21
38a
37
CV
LC
HC
14
10

FIG. 23A

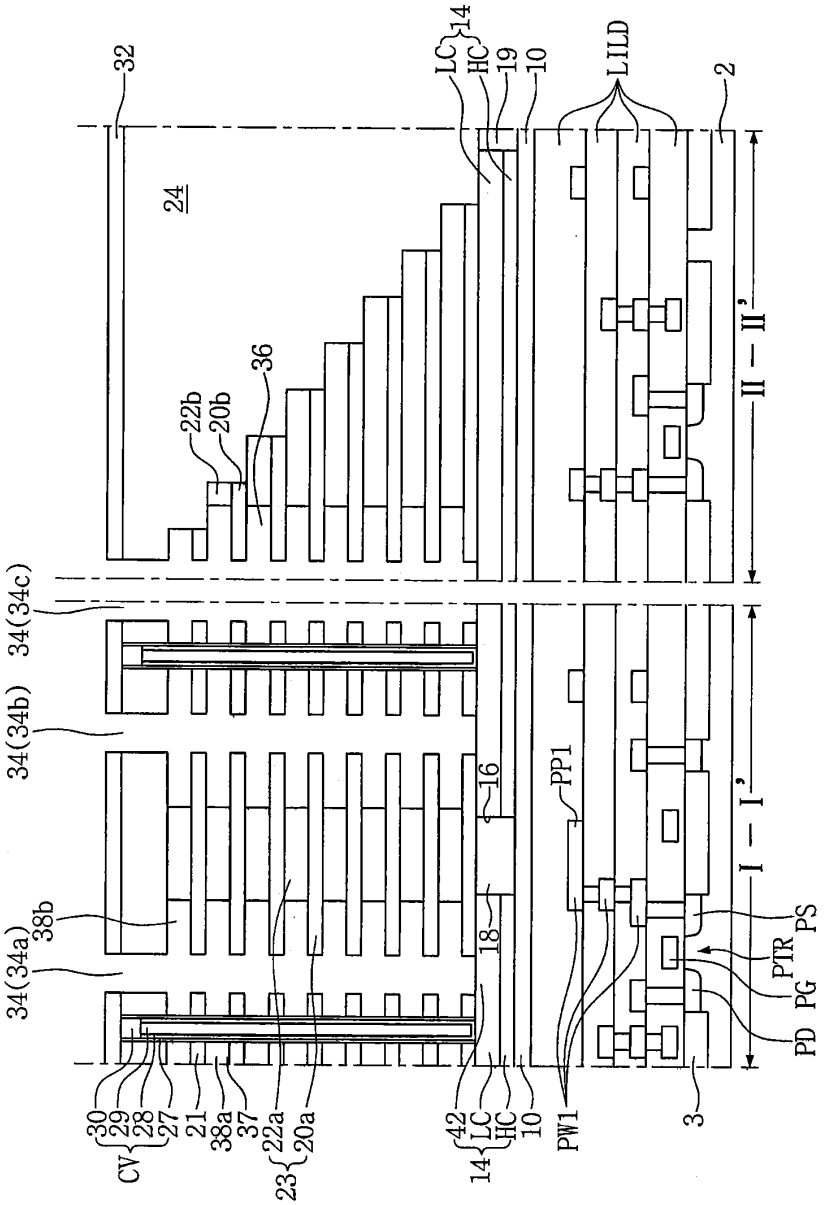

32
24
LC
14
HC
19
10
LILD
2
II – II'
22b
20b
36
34(34c)
34(34b)
34(34a)
38b
16
18
PP1
I – I'
PS
PTR
PG
PD
30
29
28
27
CV
21
38a
37
22a
20a
23
42
LC
HC
14
10
PW1
3

FIG. 23B

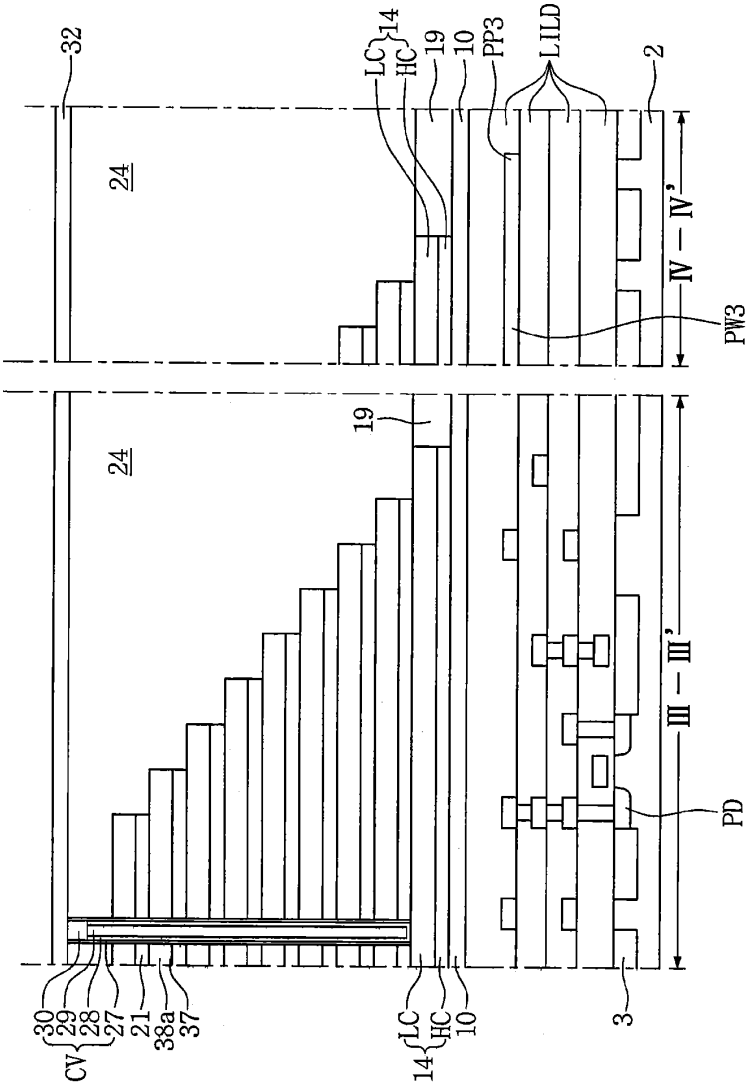

32
24
LC
HC
14
19
10
PP3
LILD
2
IV – IV'
PW3
24
19
III – III'
PD
CV
30
29
28
27
21
38a
37
LC
HC
14
10
3

FIG. 24A

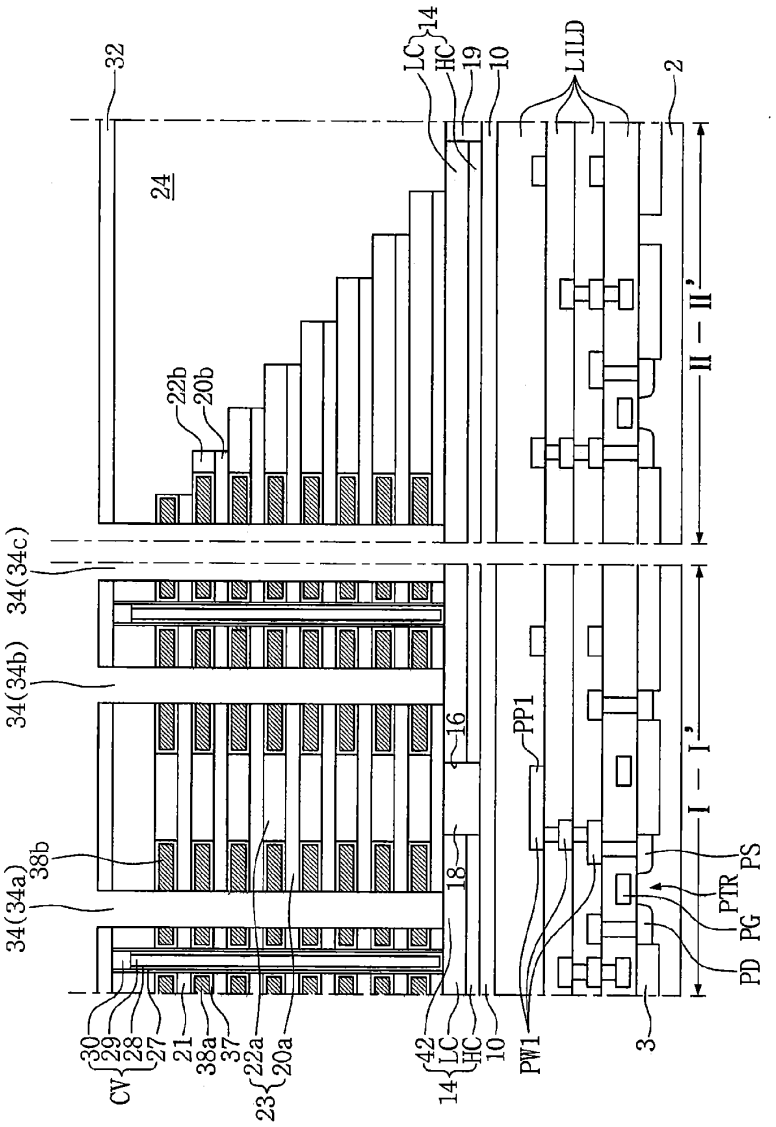

32
24
LC
HC
14
19
10
LILD
2
22b
20b
II – II'
34(34c)
34(34b)
34(34a)
38b
16
18
PP1
I – I'
PS
PTR
PG
PD
30
29
28
27
21
38a
37
22a
20a
CV
23
42
14
LC
HC
10
PW1
3

FIG. 24B

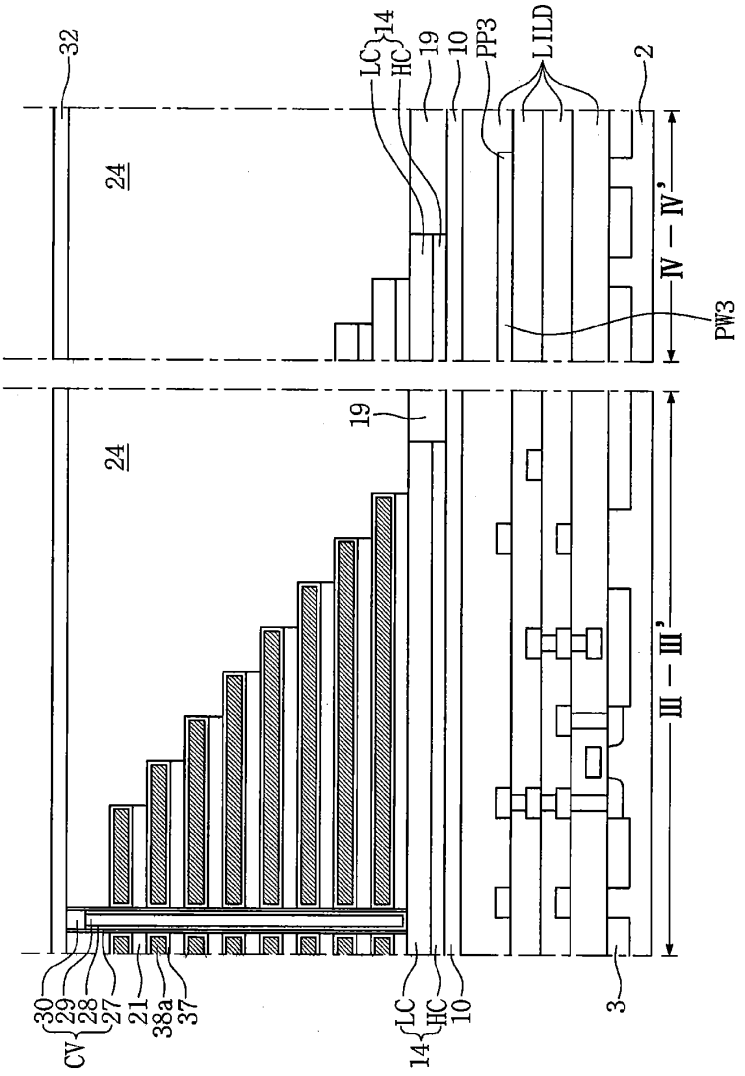

32
24
LC
14
HC
19
10
PP3
LILD
2
IV – IV'
PW3
24
19
III – III'
30
29
28
27
21
38a
37
CV
LC
14
HC
10
3

FIG. 25A

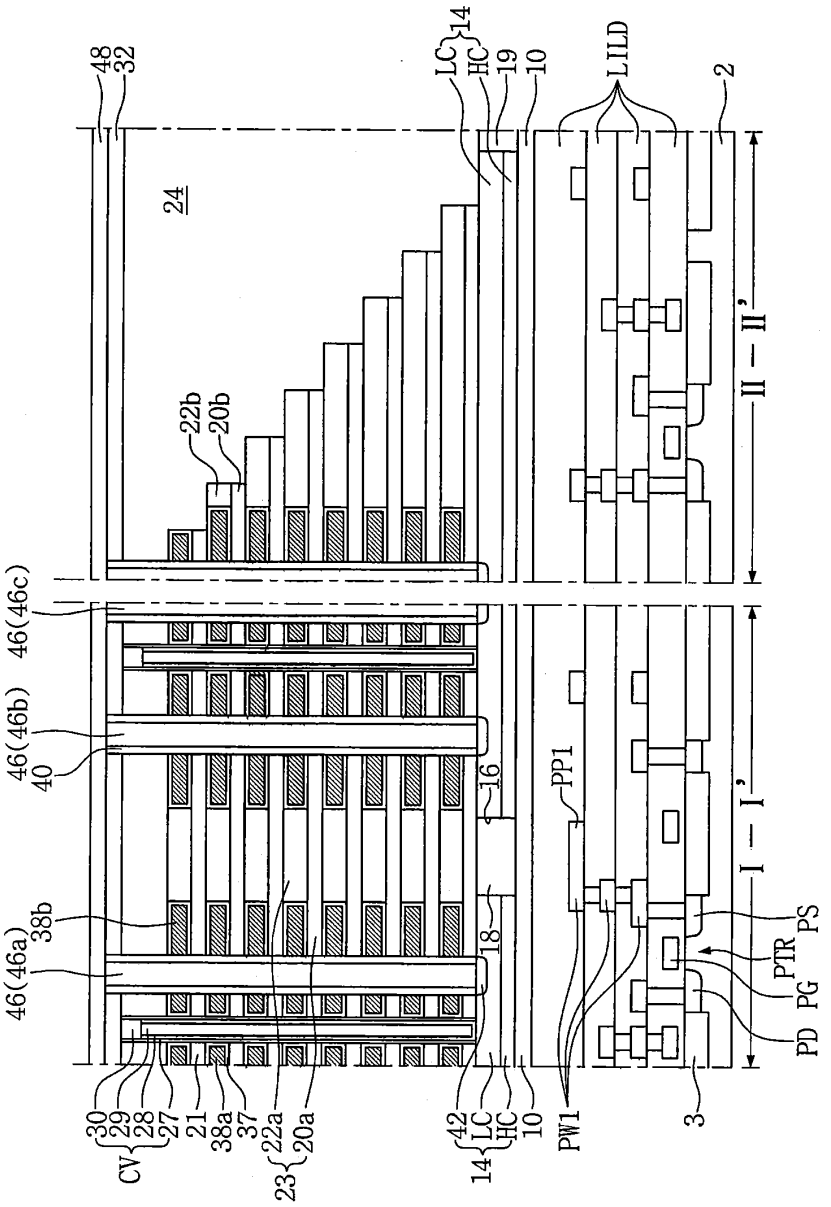

48
32
24
LC
HC
14
19
10
LILD
2
22b
20b
II – II'
46(46c)
46(46b)
40
16
PP1
I – I'
46(46a)
38b
18
PS
PTR
PG
PD
30
29
28
27
21
38a
37
22a
20a
CV
23
42
LC
HC
14
10
PW1
3

FIG. 25B

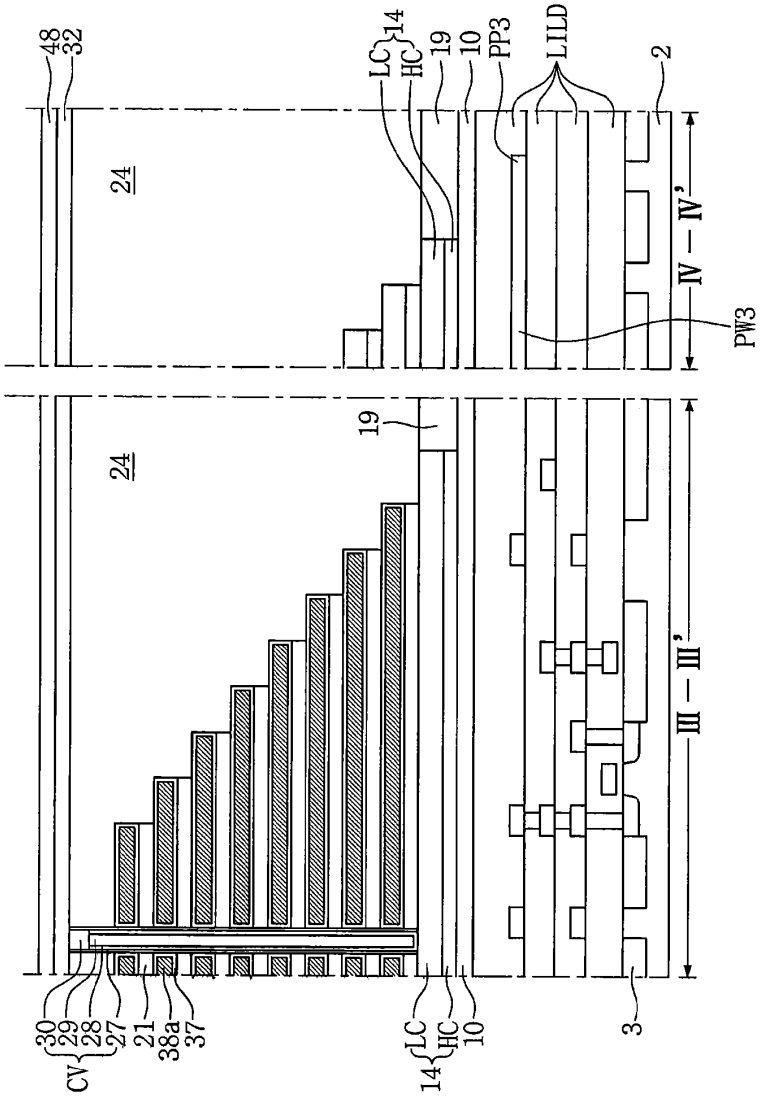

48
32
24
LC
14
HC
19
10
PP3
LILD
2
IV — IV'
PW3
24
19
III — III'
30
29
28
27
CV
21
38a
37
LC
14
HC
10
3

FIG. 26A

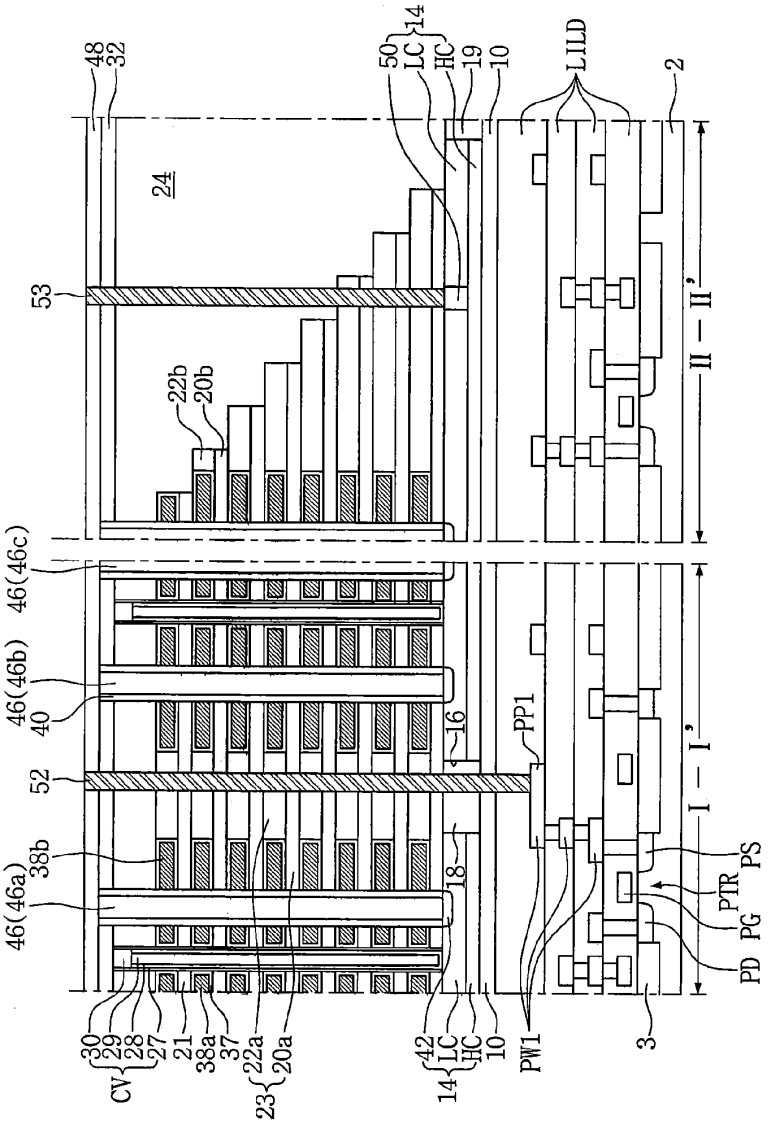

48
32
24
53
50
LC
14
HC
19
10
LILD
2
22b
20b
II – II'
46(46c)
46(46b)
40
16
PP1
52
I – I'
38b
46(46a)
18
PS
PTR
PG
PD
30
29
28
27
21
38a
37
22a
20a
CV
23
42
14
LC
HC
10
PW1
3

FIG. 26B

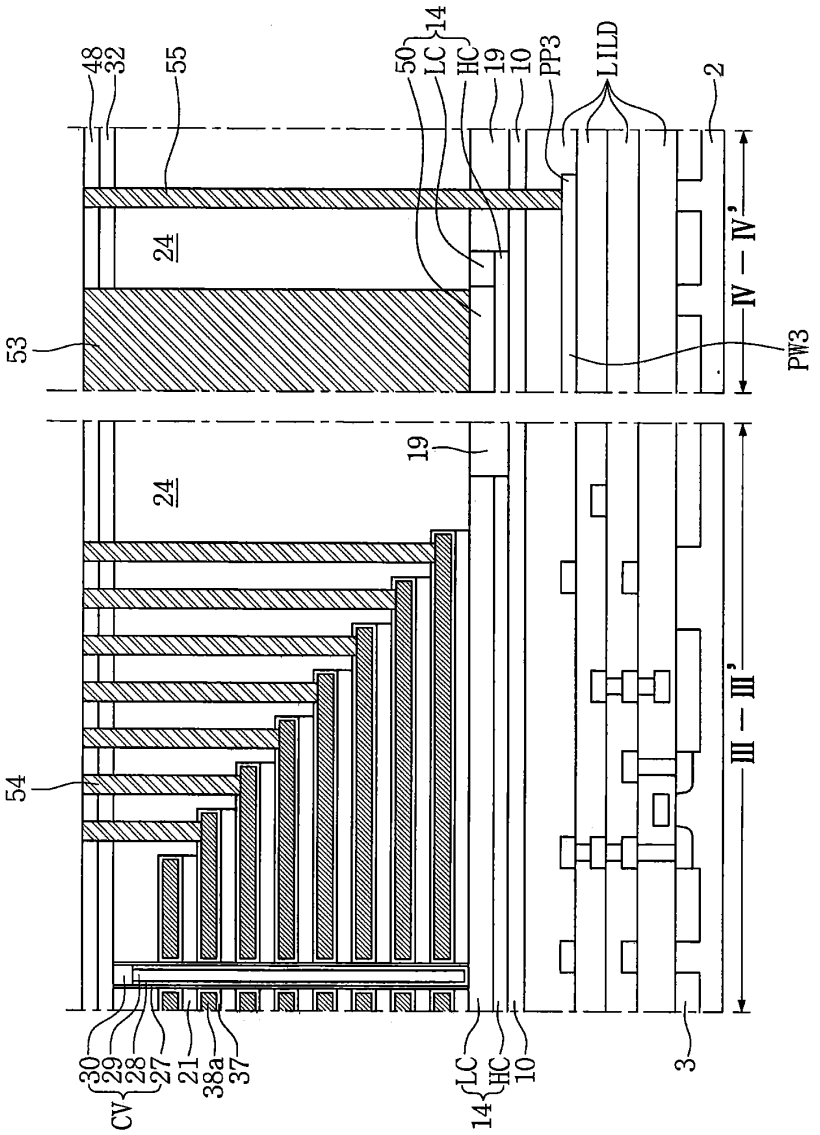

48
32
55
50
LC
14
HC
19
10
PP3
LILD
2
24
53
IV – IV'
PW3
19
24
54
III – III'
30
29
28
27
21
38a
37
CV
LC
14
HC
10
3

FIG. 27

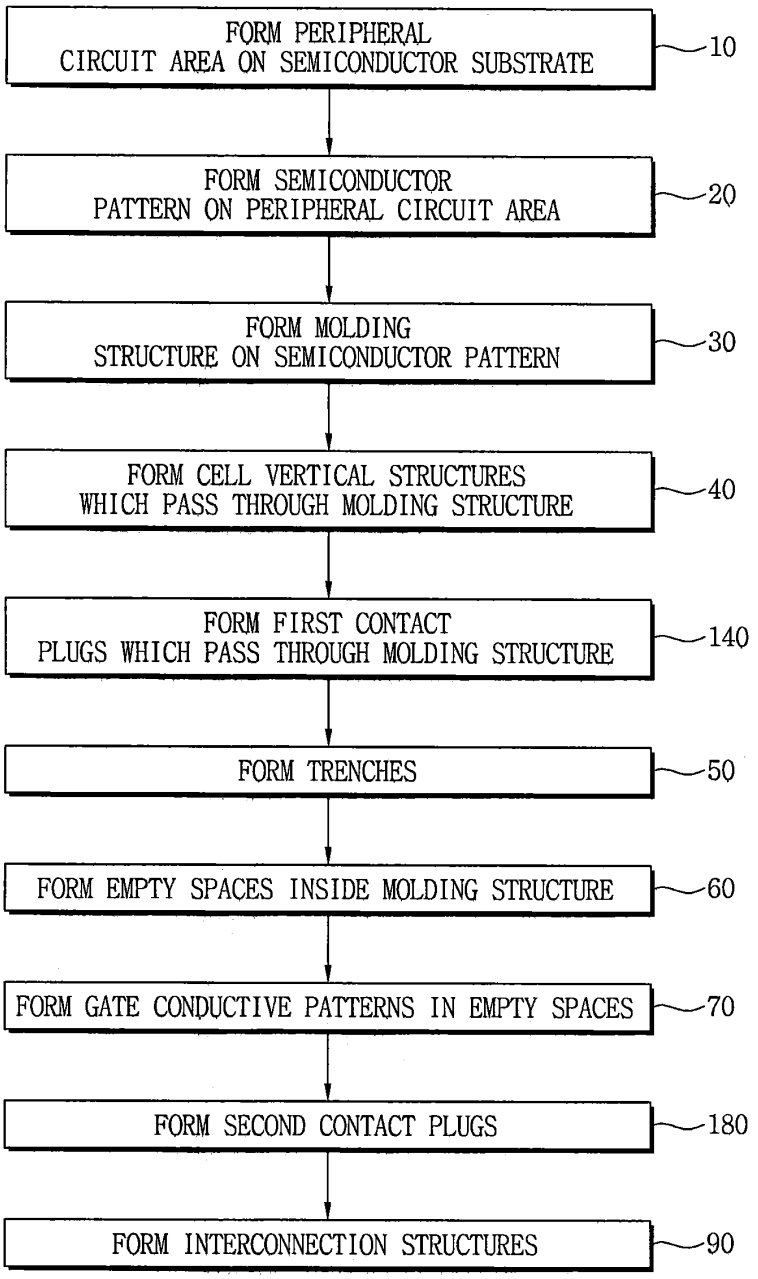

FORM PERIPHERAL CIRCUIT AREA ON SEMICONDUCTOR SUBSTRATE
10
FORM SEMICONDUCTOR PATTERN ON PERIPHERAL CIRCUIT AREA
20
FORM MOLDING STRUCTURE ON SEMICONDUCTOR PATTERN
30
FORM CELL VERTICAL STRUCTURES WHICH PASS THROUGH MOLDING STRUCTURE
40
FORM FIRST CONTACT PLUGS WHICH PASS THROUGH MOLDING STRUCTURE
140
FORM TRENCHES
50
FORM EMPTY SPACES INSIDE MOLDING STRUCTURE
60
FORM GATE CONDUCTIVE PATTERNS IN EMPTY SPACES
70
FORM SECOND CONTACT PLUGS
180
FORM INTERCONNECTION STRUCTURES
90

FIG. 28

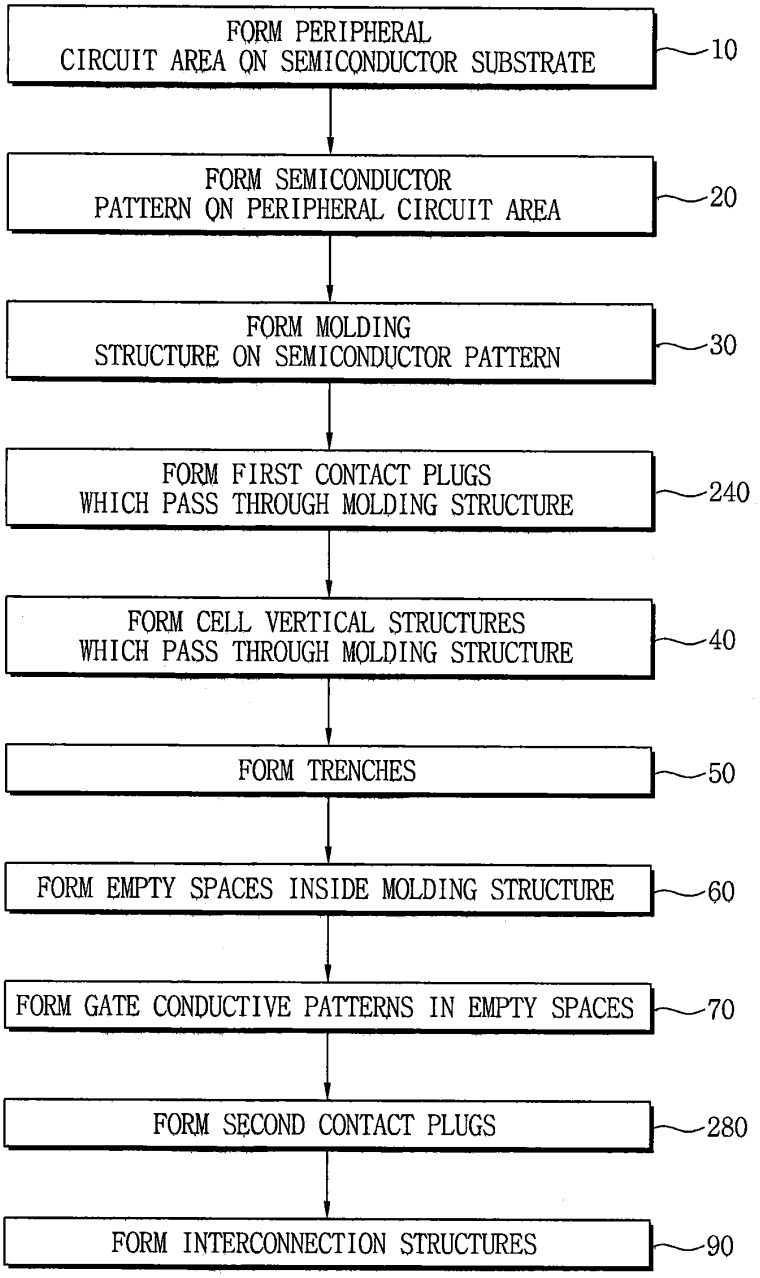

FORM PERIPHERAL CIRCUIT AREA ON SEMICONDUCTOR SUBSTRATE
10
FORM SEMICONDUCTOR PATTERN ON PERIPHERAL CIRCUIT AREA
20
FORM MOLDING STRUCTURE ON SEMICONDUCTOR PATTERN
30
FORM FIRST CONTACT PLUGS WHICH PASS THROUGH MOLDING STRUCTURE
240
FORM CELL VERTICAL STRUCTURES WHICH PASS THROUGH MOLDING STRUCTURE
40
FORM TRENCHES
50
FORM EMPTY SPACES INSIDE MOLDING STRUCTURE
60
FORM GATE CONDUCTIVE PATTERNS IN EMPTY SPACES
70
FORM SECOND CONTACT PLUGS
280
FORM INTERCONNECTION STRUCTURES
90

FIG. 29

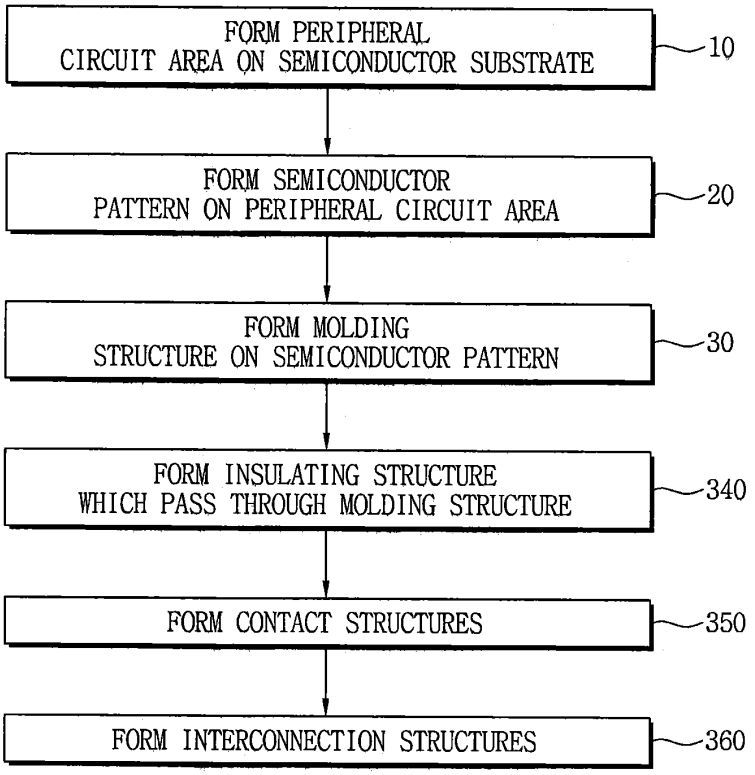

FORM PERIPHERAL CIRCUIT AREA ON SEMICONDUCTOR SUBSTRATE
10
FORM SEMICONDUCTOR PATTERN ON PERIPHERAL CIRCUIT AREA
20
FORM MOLDING STRUCTURE ON SEMICONDUCTOR PATTERN
30
FORM INSULATING STRUCTURE WHICH PASS THROUGH MOLDING STRUCTURE
340
FORM CONTACT STRUCTURES
350
FORM INTERCONNECTION STRUCTURES
360

FIG. 30A

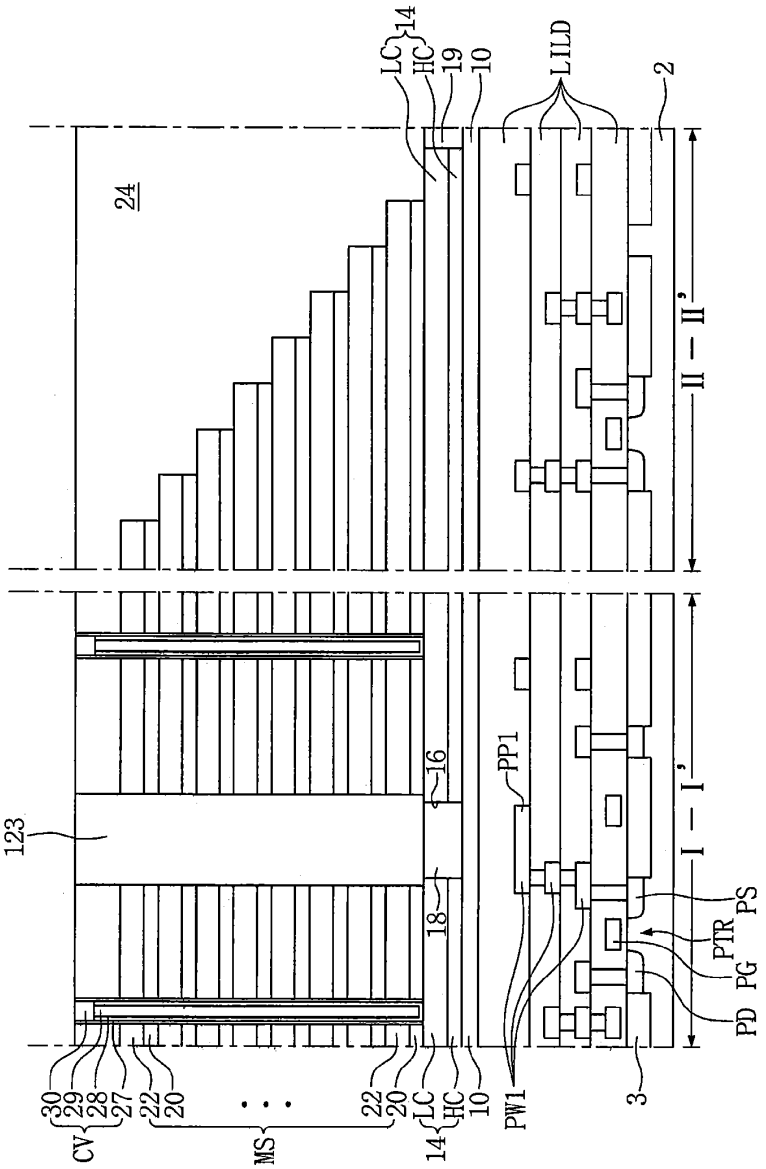

24
LC
14
HC
19
10
LILD
2
II – II'
123
16
PP1
I – I'
18
PS
PTR
PG
PD
30
29
28
27
22
20
CV
MS
22
20
LC
14
HC
10
PW1
3

FIG. 30B

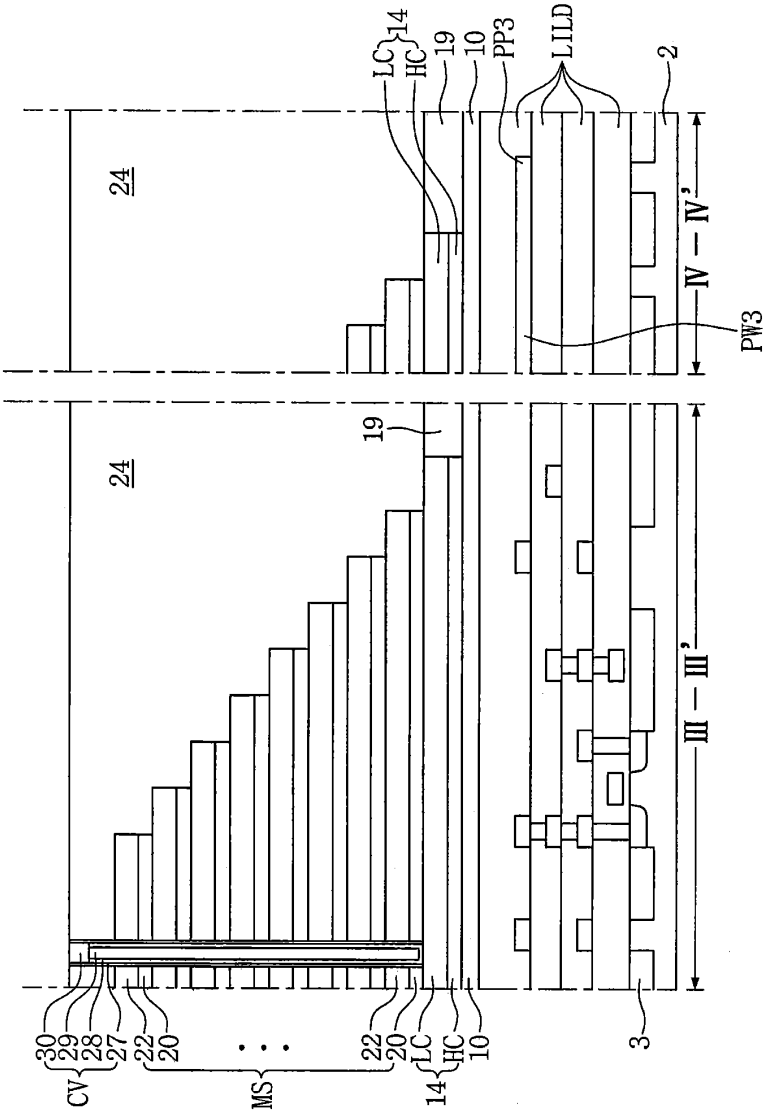

24
24
LC
HC
14
19
10
PP3
LILD
2
IV — IV'
PW3
19
III — III'
30
29
28
27
22
20
CV
MS
22
20
LC
HC
14
10
3

FIG. 31A

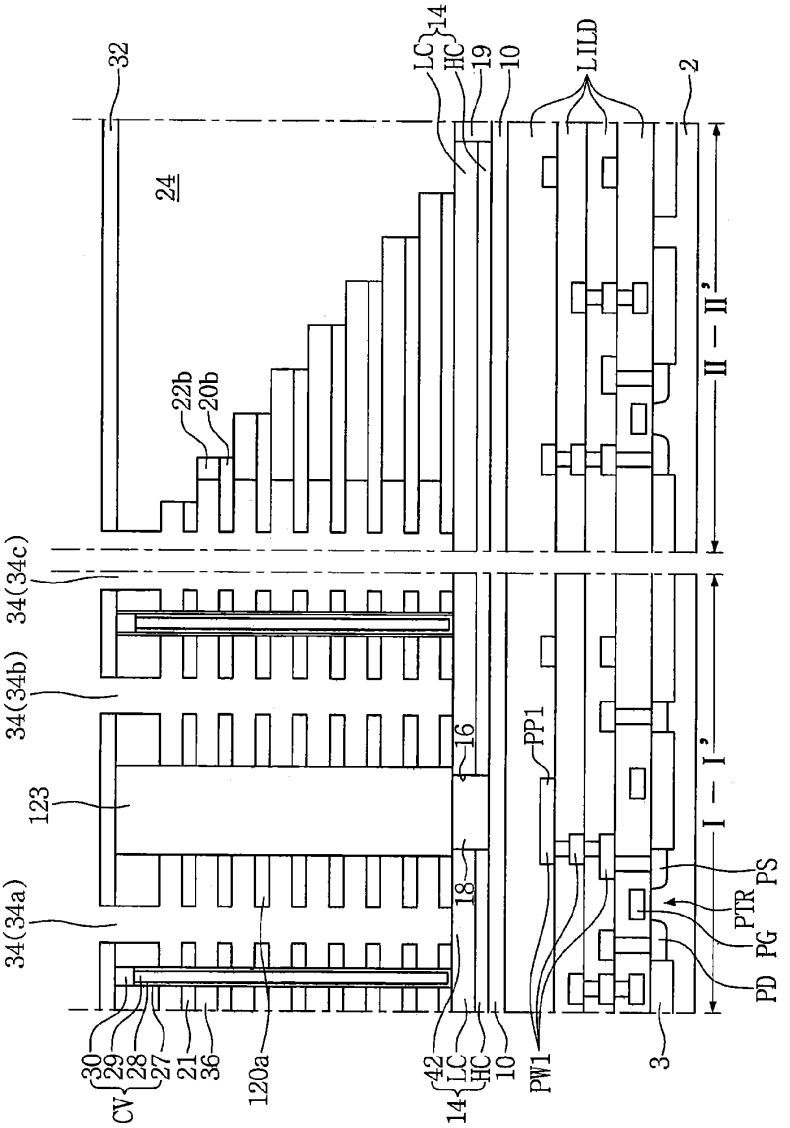

32
24
LC
HC
14
19
10
LILD
2
22b
20b
II – II'
34(34c)
34(34b)
34(34a)
123
16
18
PP1
I – I'
PS
PTR
PG
PD
30
29
28
27
21
36
CV
120a
42
14
LC
HC
10
PW1
3

FIG. 31B

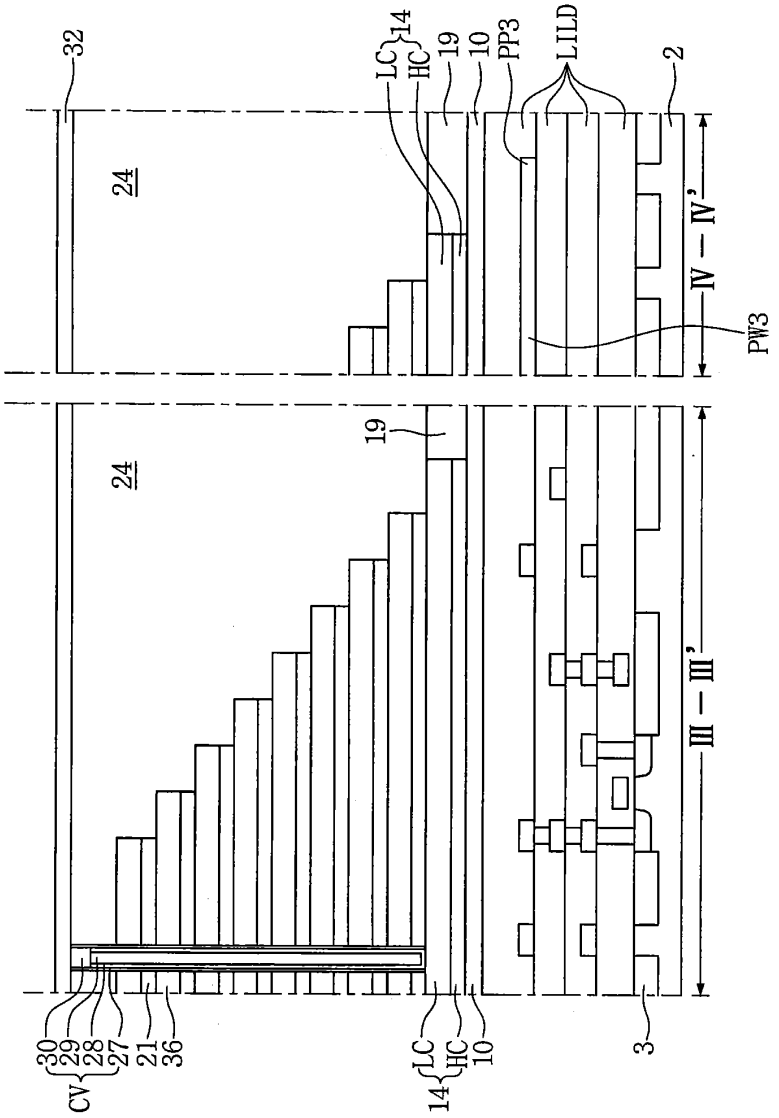

32
24
LC
HC
14
19
10
PP3
LILD
2
IV — IV'
PW3
24
19
III — III'
30
29
28
27
21
36
CV
LC
HC
14
10
3

FIG. 32A

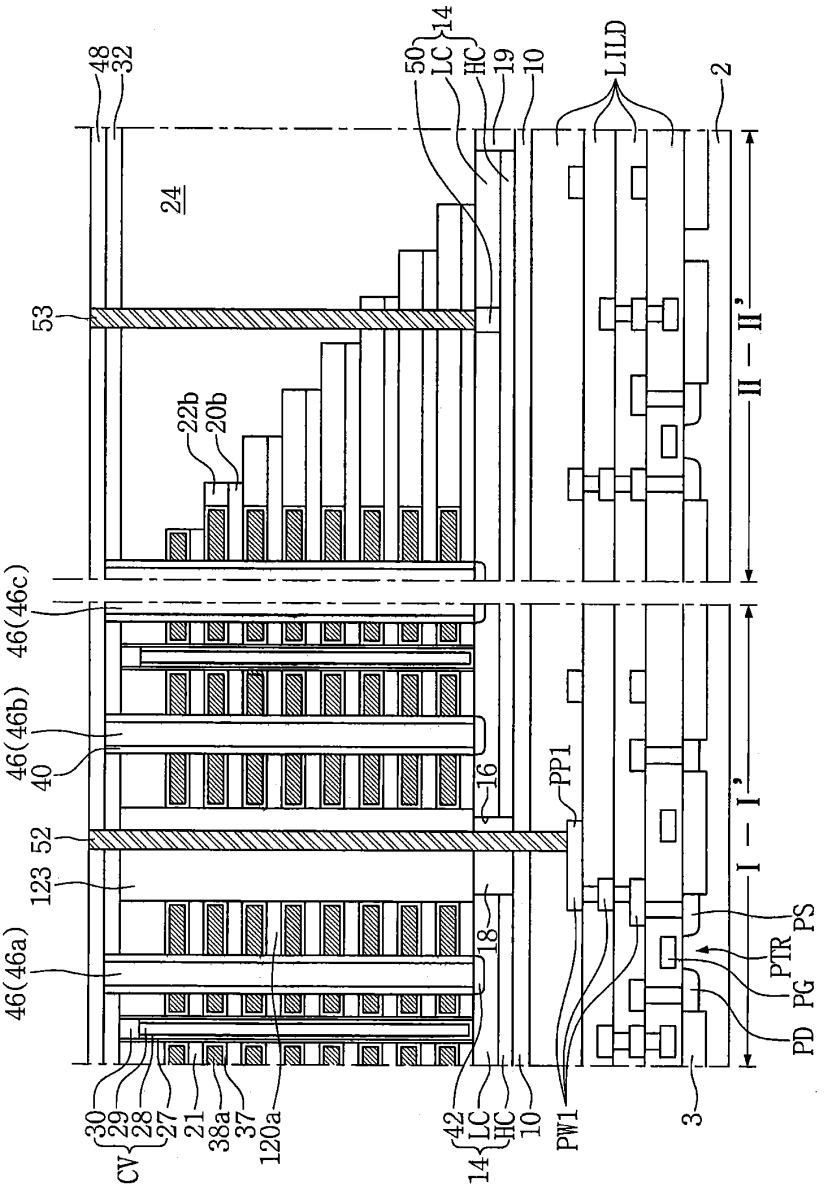

48
32
24
53
22b
20b
50
LC
14
HC
19
10
LILD
2
II – II'
46(46c)
46(46b)
40
16
PP1
52
123
18
46(46a)
I – I'
PS
PTR
PG
PD
30
29
28
27
21
38a
37
120a
CV
42
LC
HC
14
10
PW1
3

FIG. 32B

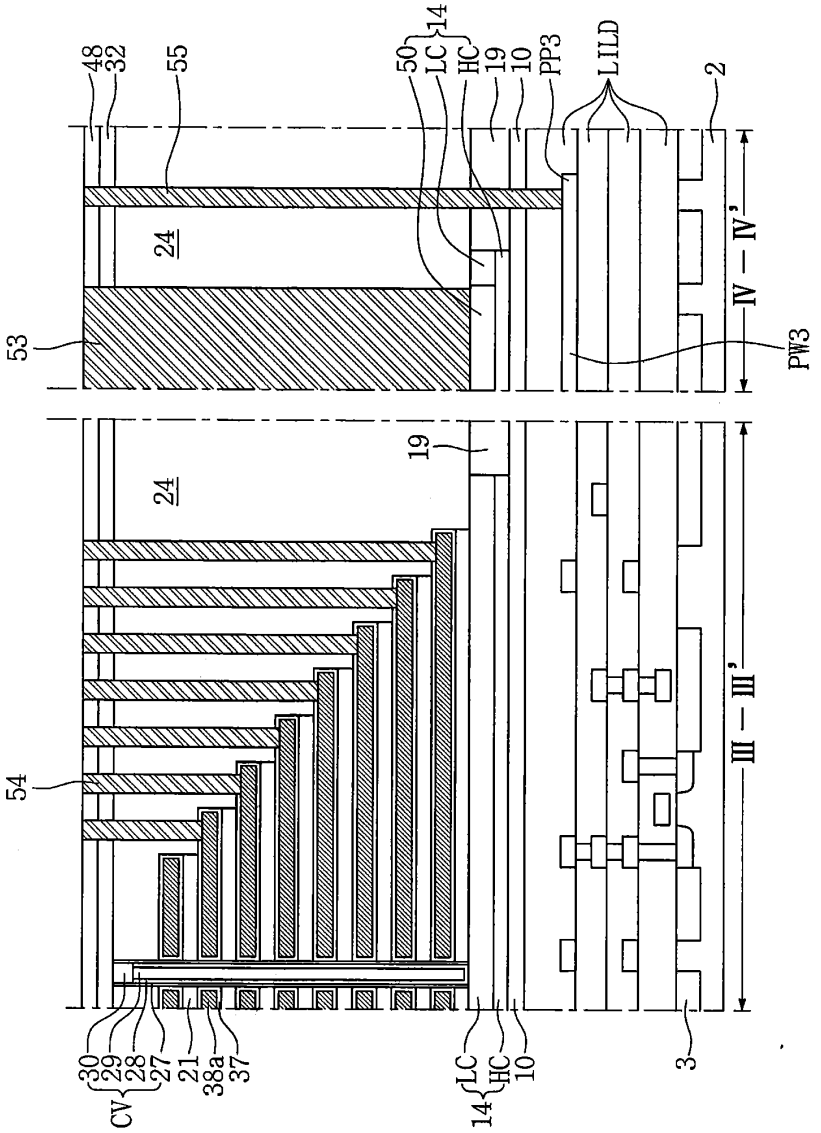

48
32
55
50
LC
14
HC
19
10
PP3
LILD
2
24
53
IV — IV'
PW3
24
19
54
III — III'
30
29
28
27
21
38a
37
CV
LC
HC
14
10
3

FIG. 33

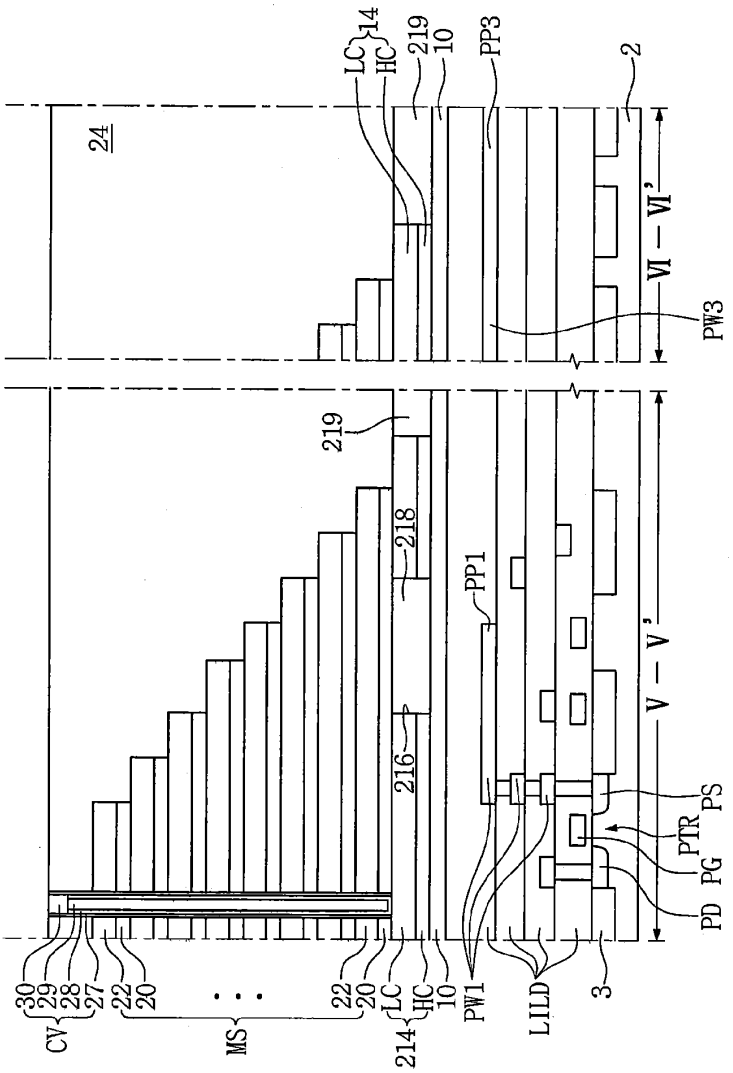

CV
30
29
28
27
22
20
MS
22
20
214
LC
HC
10
PW1
LILD
3
PD
PG
PTR
PS
V – V'
216
218
219
PP1
24
LC
HC
14
219
10
PP3
2
VI – VI'
PW3

FIG. 34

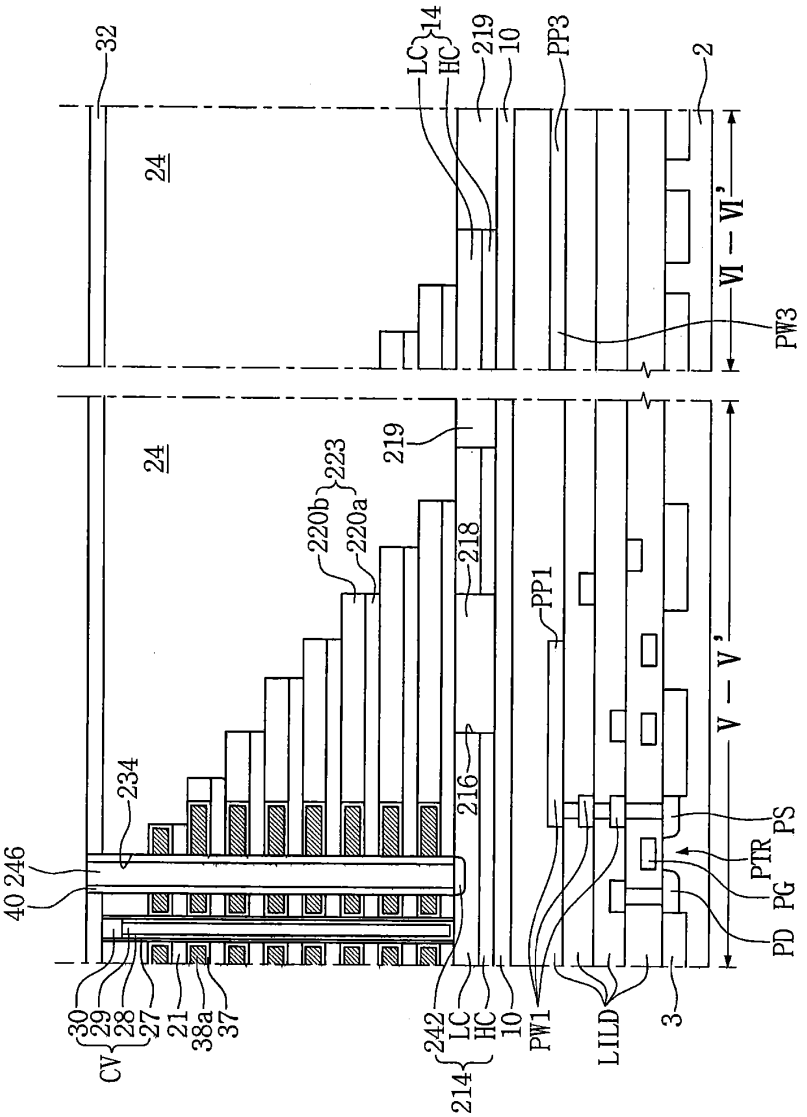

32
24
LC
HC
14
219
10
PP3
2
VI – VI'
PW3
24
219
223
220b
220a
218
PP1
V – V'
234
216
40 246
PS
PTR
PG
PD
30
29
28
27
21
38a
37
CV
242
LC
HC
214
10
PW1
LILD
3

FIG. 35

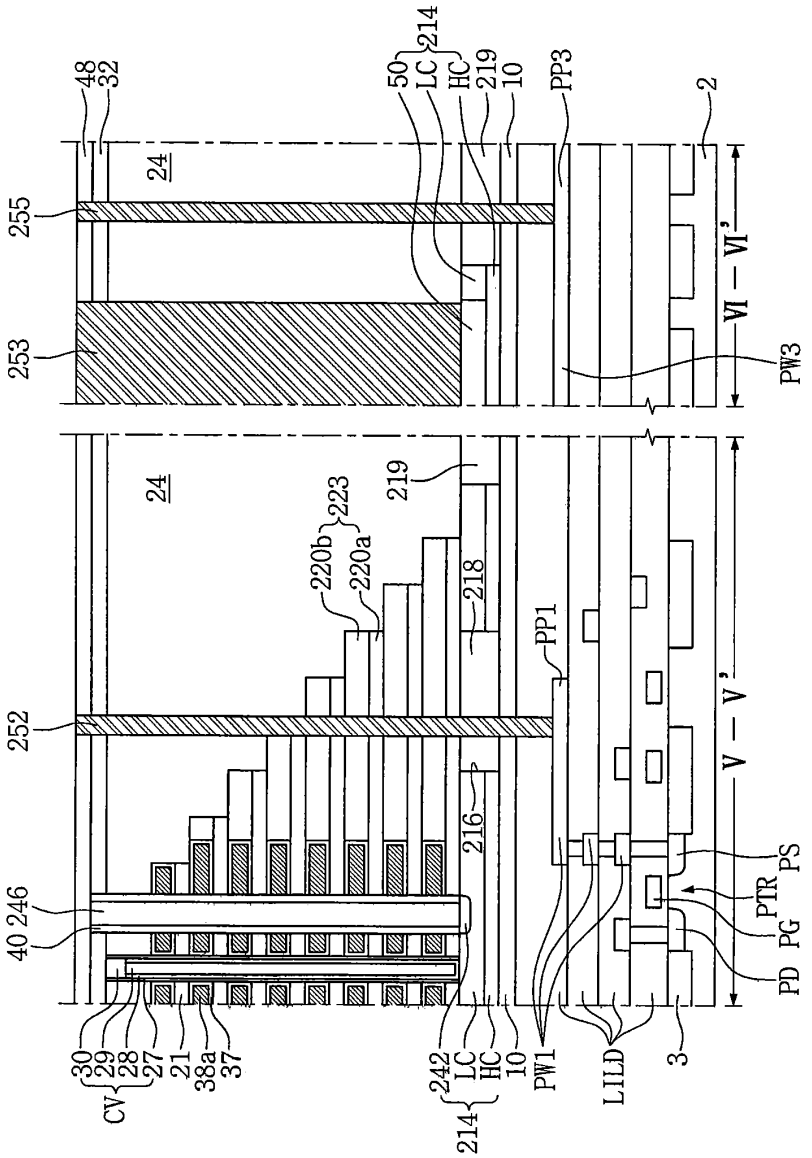
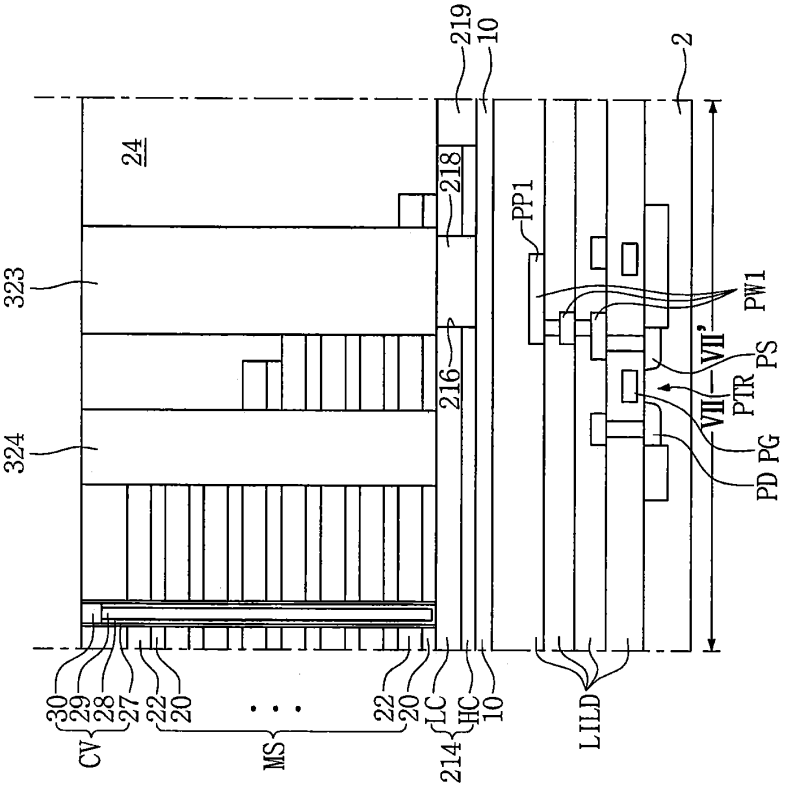

48
32
24
255
253
50
LC
214
HC
219
10
PP3
2
VI – VI'
PW3
24
219
223
220b
220a
218
PP1
252
216
V – V'
40
246
PS
PTR
PG
PD
30
29
28
27
21
38a
37
CV
242
LC
HC
214
10
PW1
LILD
3

FIG. 36



24
323
324
218
216
219
10
2
PP1
PW1
VII'
VII
PS
PTR
PG
PD
30
29
28
27
22
20
CV
MS
LC
HC
214
LILD

FIG. 37

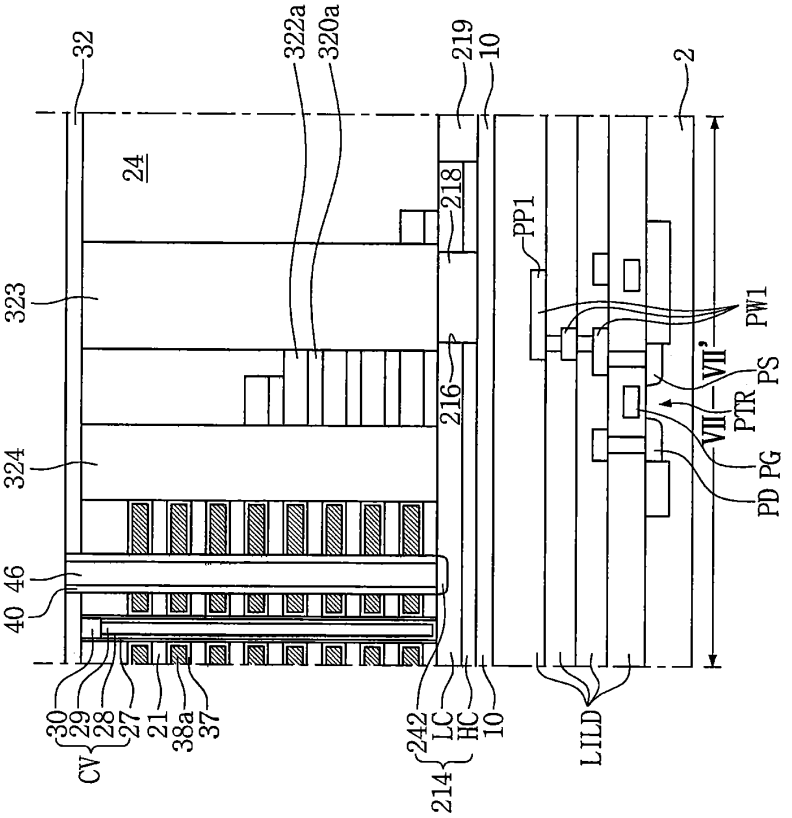

32
322a
320a
219
10
2
24
218
PP1
323
PW1
VII'
PS
216
VII
PTR
324
PG
PD
46
40
30
29
28
27
21
38a
37
CV
242
LC
HC
10
214
LILD

FIG. 38

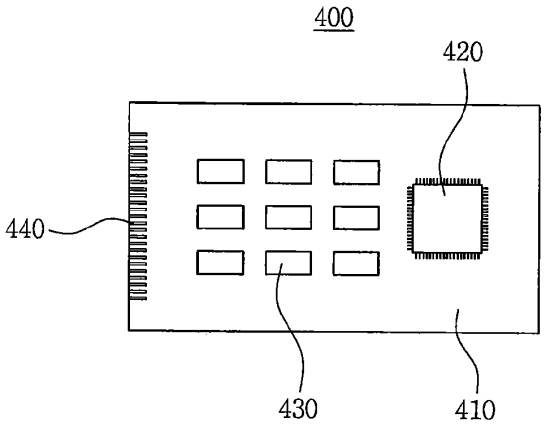

400
420
440
430
410

FIG. 39

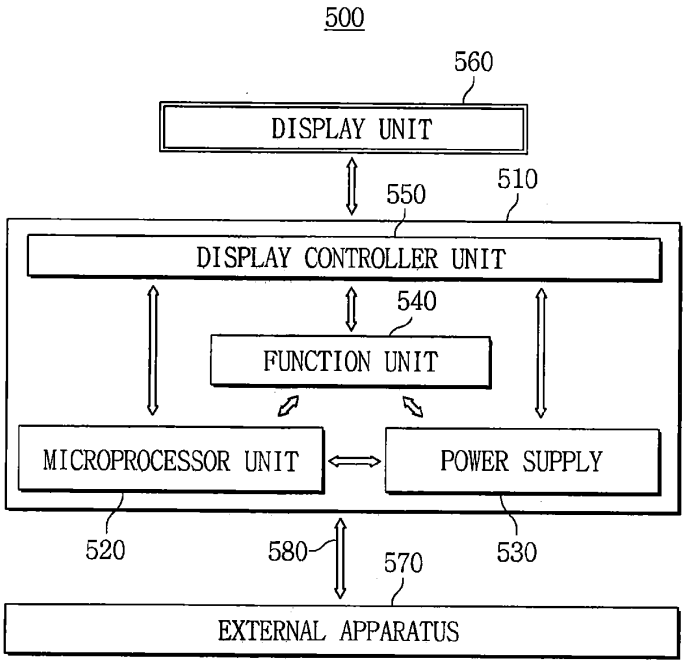
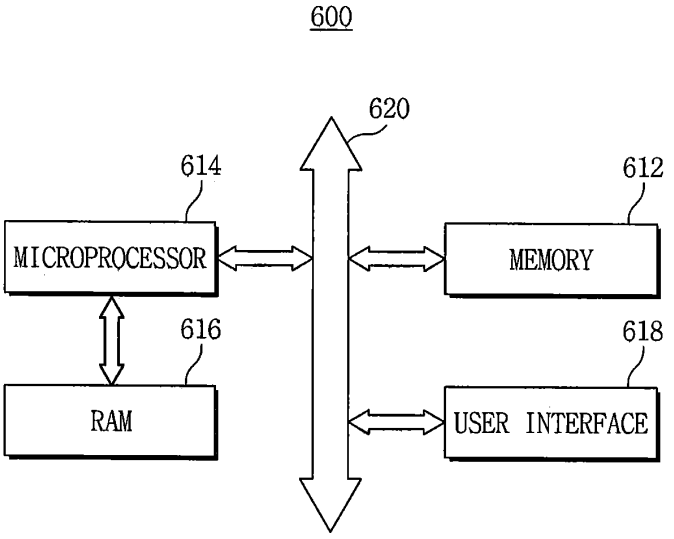

500
560
DISPLAY UNIT
550
510
DISPLAY CONTROLLER UNIT
540
FUNCTION UNIT
MICROPROCESSOR UNIT
POWER SUPPLY
520
580
570
530
EXTERNAL APPARATUS

FIG. 40


600
620
614
612
MICROPROCESSOR
MEMORY
616
618
RAM
USER INTERFACE

SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. §119 to Korean Patent Application No. 10-2014-0176089 filed on Dec. 9, 2014, the disclosure of which is hereby incorporated by reference in its entirety.

BACKGROUND

[0002] 1. Technical Field

[0003] Embodiments of the inventive concepts relate to semiconductor devices, a method of manufacturing the semiconductor devices, and an electronic system including the semiconductor devices.

[0004] 2. Description of Related Art

[0005] A degree of integration is one of several factors for determining a price of a semiconductor product (e.g., semiconductor device such as flash memories.) Manufacturing two-dimensional semiconductor devices including two-dimensionally arranged memory cells may require relatively expensive systems for fine patterning in order to increase a degree of integration. Therefore, there may be limits to increase a degree of integration of two-dimensional semiconductor devices. Three-dimensional semiconductor devices including three-dimensionally arranged memory cells have been proposed to further increase a degree of integration of semiconductor devices.

SUMMARY

[0006] A semiconductor device may include a semiconductor pattern disposed on a semiconductor substrate. The semiconductor pattern may include an opening, a first impurity region having a first conductivity type and a second impurity region having a second conductivity type that is different from the first conductivity type. The device may also include a peripheral transistor disposed between the semiconductor substrate and the semiconductor pattern, a first peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern and electrically connected to the peripheral transistor, cell gate conductive patterns disposed on the semiconductor pattern, cell vertical structures extending through respective ones of the cell gate conductive patterns and being connected to the semiconductor pattern, cell bit line contact plugs disposed on respective ones of the cell vertical structures, a bit line disposed on the cell bit line contact plugs and a peripheral bit line contact structure being disposed between the bit line and the first peripheral interconnection structure and extending through the opening of the semiconductor pattern.

[0007] According to various embodiments, the semiconductor pattern may further include a body contact impurity region that has the first conductivity type and has an impurity concentration higher than an impurity concentration of the first impurity region.

[0008] In various embodiments, the device may also include a cell body contact structure disposed on the body contact impurity region.

[0009] In various embodiments, the device may further include a second peripheral interconnection structure that is disposed between the semiconductor substrate and the semiconductor pattern and extends outside of the semiconductor pattern, a peripheral body contact structure that is disposed outside of the semiconductor pattern and is disposed on the second peripheral interconnection structure and a cell body interconnection structure that is disposed on the peripheral body contact structure and the cell body contact structure and is electrically connected to the peripheral body contact structure and the cell body contact structure.

[0010] According to various embodiments, the device may also include a third impurity region that is disposed in the semiconductor pattern and under the first impurity region. The third impurity region may have the first conductivity type and may have an impurity concentration higher than an impurity concentration of the first impurity region.

[0011] According to various embodiments, the device may also include a cell source pattern disposed on the second impurity region of the semiconductor pattern.

[0012] A semiconductor device may include a semiconductor pattern that is disposed on a semiconductor substrate and includes an opening, a first peripheral interconnection structure that is disposed between the semiconductor substrate and the semiconductor pattern and includes a first peripheral contact pad and a second peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern. The second peripheral interconnection structure extends outside of the semiconductor pattern and includes a second peripheral contact pad. The semiconductor device may also include a cell array area disposed on the semiconductor pattern, a step area disposed on the semiconductor pattern and on a side of the cell array area and a cell gate conductive pattern disposed on the semiconductor pattern. The cell gate conductive pattern may be disposed in the cell array area and may extend to the step area. The semiconductor device may further include a cell vertical structure that extends through the cell gate conductive pattern in the cell array area and is connected to the semiconductor pattern, a bit line disposed on the cell vertical structure, a peripheral bit line contact structure that is disposed between the bit line and the first peripheral contact pad and extends through the opening of the semiconductor pattern, a cell gate contact structure disposed on the cell gate conductive pattern of the step area on the semiconductor pattern, a peripheral word line contact structure disposed on the second peripheral contact pad and outside of the semiconductor pattern and a word line interconnection structure that electrically connects the cell gate contact structure to the peripheral word line contact structure.

[0013] According to various embodiments, the opening may be disposed in the cell array area.

[0014] In various embodiments, the opening may be disposed in the step area.

[0015] In various embodiments, the opening may disposed in the cell array area and may extend to the step area.

[0016] A semiconductor device may include a semiconductor pattern disposed on a semiconductor substrate, a peripheral transistor disposed between the semiconductor substrate and the semiconductor pattern and a peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern. The peripheral interconnection structure is electrically connected to the peripheral transistor and includes a peripheral contact pad. The semiconductor device may also include a gate conductive structure disposed on the semiconductor pattern, a cell vertical structure extending through the gate conductive structure, a cell conductive line disposed on the cell vertical structure and a peripheral contact structure disposed between the cell conductive line and the peripheral contact pad. The gate conduc-

tive structure may include a plurality of cell gate conductive patterns stacked in a direction perpendicular to the semiconductor pattern, and the cell conductive line has a length smaller than a width of the semiconductor pattern.

[0017] According to various embodiments, the cell conductive line may have a line shape which extends in a first direction and the width of the semiconductor pattern may be a width of the semiconductor pattern in the first direction.

[0018] In various embodiments, the semiconductor device may further include a lower interlayer insulating layer on the semiconductor substrate and a buffer insulating layer disposed between the lower interlayer insulating layer and the semiconductor pattern.

[0019] In various embodiments, the semiconductor pattern may include an opening. The semiconductor device may also include a gap fill insulating layer filling the opening of the semiconductor pattern. The gap fill insulating layer may include a material having an etch selectivity with respect to the buffer insulating layer, and the peripheral contact structure may extend through the gap fill insulating layer.

[0020] According to various embodiments, the semiconductor device may also include an insulating structure disposed on the semiconductor pattern. The peripheral contact structure may extend through the insulating structure.

[0021] In various embodiments, the insulating structure may include first insulating patterns and second insulating patterns that are alternately stacked, and the first insulating patterns may include a material having an etch selectivity with respect to the second insulating patterns.

[0022] In various embodiments, ones of the first insulating patterns may have widths greater than widths of ones of the second insulating patterns.

[0023] According to various embodiments, sides of ones of the first insulating patterns may be co-planar with sides of ones of the cell gate conductive patterns.

[0024] In various embodiments, the semiconductor device may further include third insulating patterns and fourth insulating patterns that are disposed on the semiconductor pattern and alternately stacked. Ones of the third insulating patterns and respective ones of the first insulating patterns may be disposed at an equal height and may include a first material, and ones of the fourth insulating patterns and respective ones of the second insulating patterns may be disposed at an equal height and comprise a second material.

[0025] According to various embodiments, the semiconductor device may also include a body contact structure that extends through the third and fourth insulating patterns and is connected to the semiconductor pattern

[0026] A semiconductor device may include a peripheral transistor disposed on a semiconductor substrate and a peripheral interconnection structure disposed on the semiconductor substrate. The peripheral interconnection structure is electrically connected to the peripheral transistor and may include a peripheral contact pad. The semiconductor device may also include a lower interlayer insulating layer that is disposed on the semiconductor substrate and on the peripheral transistor and the peripheral interconnection structure, a buffer insulating layer disposed on the lower interlayer insulating layer and a semiconductor pattern disposed on the buffer insulating layer. The semiconductor pattern may overlap the peripheral transistor and the peripheral interconnection structure. The semiconductor device may further include a first gate conductive structure, a second gate conductive structure, and a third gate conductive structure that are disposed on the semiconductor pattern and are sequentially arranged in a horizontal direction, cell vertical structures extending through respective ones of the first, second and third gate conductive structures, cell bit line contact plugs disposed on respective ones of the cell vertical structures, a bit line disposed on the cell bit line contact plugs and a peripheral bit line contact structure that extends through the semiconductor pattern and is disposed between the bit line and the peripheral contact pad. Each of the first, second and third gate conductive structures may include a plurality of cell gate conductive patterns stacked in a direction perpendicular to the semiconductor pattern;

[0027] According to various embodiments, a distance between the first and second gate conductive structures may be greater than a distance between the second and third gate conductive structures, and the peripheral bit line contact structure may extend between the first and second gate conductive structures.

[0028] In various embodiments, the semiconductor device may additionally include a cell body contact structure disposed on the semiconductor pattern and a body interconnection structure disposed on the cell body contact structure.

[0029] According to various embodiments, the peripheral bit line contact structure may include a peripheral bit line lower contact plug and a peripheral bit line upper contact plug disposed on the peripheral bit line lower contact plug. The cell body contact structure may include a cell body lower contact plug and a cell body upper contact plug disposed on the cell body lower contact plug.

[0030] In various embodiments, lower surfaces of the peripheral bit line lower contact plug and the cell body lower contact plug may be non-coplanar, and upper surfaces of the peripheral bit line lower contact plug and the cell body lower contact plug may be coplanar.

[0031] A semiconductor device may include a substrate and a bit line on the substrate. The bit line extends in a first direction. The semiconductor device may also include first and second semiconductor patterns between the substrate and the bit line. The first and second semiconductor patterns are spaced apart from each other in the first direction by a gap therebetween and lower surfaces of the first and second semiconductor patterns are coplanar. The semiconductor device may further include first and second gate structures between an upper surface of the first semiconductor pattern and the bit line and a first cell vertical structure extending through the first gate structure and a second cell vertical structure extending through the second gate structure. The first and second gate structures may be disposed along the first direction. Each of the first and second cell vertical structures may include a channel layer and both the first and second cell vertical structures may extend away from the upper surface of the first semiconductor pattern and may be connected to the bit line. The semiconductor device may also include an insulating layer between the substrate and the first and second semiconductor patterns, a conductive contact pad in the insulating layer and a bit line contact structure extending through the gap between the first and second semiconductor patterns and extending away from an upper surface of the substrate. An upper portion of the bit line contact structure may contact the bit line and a lower portion of the bit line contact structure may contact the conductive contact pad.

[0032] According to various embodiments, the bit line may overlie at least a portion of the gap between the first and second semiconductor patterns.

[0033] In various embodiments, the bit line may overlie top surfaces of the first cell vertical structure, the second cell vertical structure and the bit line contact structure.

[0034] According to various embodiments, each of the first and second gate structures may include a plurality of stacked gate electrodes, and an upper most gate electrode of the plurality of stacked gate electrodes may be at a first height from the upper surface of the substrate. the bit line contact structure may include a portion having an unitary structure that extends from the first height to the conductive contact pad.

[0035] In various embodiments, the semiconductor device may also include a third gate structure between an upper surface of the second semiconductor pattern and the bit line and a third cell vertical structure extending through the third gate structure and extending away from the upper surface of the second semiconductor pattern. The third cell vertical structure may include a channel layer and may be connected to the bit line.

[0036] According to various embodiments, the bit line may cross over the gap between the first and second semiconductor patterns.

[0037] In various embodiments, the bit line may overlie top surfaces of the second cell vertical structure, the third cell vertical structure and the bit line contact structure.

[0038] In various embodiments, the first and second semiconductor patterns may be portions of a same semiconductor pattern, and the gap may include a portion of an opening in the semiconductor pattern. The opening may have a line shape extending in a second direction when viewed from a plan perspective, and the bit line contact structure may include one of a plurality bit line contact structures, and ones of the plurality bit line contact structures may be disposed along the second direction and may extend through the opening.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] The foregoing and other features and advantages of the inventive concepts will be apparent from the more particular description of embodiments of the inventive concepts, as illustrated in the accompanying drawings. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the inventive concepts. In the drawings:

[0040] FIG. **1** is a diagram illustrating a semiconductor device in accordance with some embodiments of the inventive concepts;

[0041] FIGS. **2**A and **2**B are plan views showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0042] FIGS. **3**A and **3**B are cross-sectional views showing a semiconductor device in accordance with some embodiments of the inventive concepts, and FIG. **3**C is an enlarged view of the portion "A" shown in FIG. **3**A;

[0043] FIGS. **4**A and **4**B are cross-sectional views showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0044] FIGS. **5**A and **5**B are cross-sectional views showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0045] FIGS. **6** through **10** are plan views showing semiconductor devices in accordance with some embodiments of the inventive concepts;

[0046] FIGS. **11**A and **11**B are cross-sectional views showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0047] FIG. **12** is a diagram illustrating a semiconductor device in accordance with some embodiments of the inventive concepts;

[0048] FIGS. **13**A and **13**B are plan views showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0049] FIG. **14** is a cross-sectional view showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0050] FIG. **15** is a cross-sectional view showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0051] FIG. **16** is a cross-sectional view showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0052] FIG. **17** is a plan view showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0053] FIG. **18** is a cross-sectional view showing a semiconductor device in accordance with some embodiments of the inventive concepts;

[0054] FIG. **19** is a flowchart showing a method of forming a semiconductor device in accordance with some embodiments of the inventive concepts;

[0055] FIGS. **20**A, **20**B, **21**A, **21**B, **22**A, **22**B, **23**A, **23**B, **24**A, **24**B, **25**A, **25**B, **26**A and **26**B are cross-sectional views showing a method of forming a semiconductor device according to some embodiments of the inventive concepts;

[0056] FIG. **27** is a flowchart showing a method of forming a semiconductor device in accordance with some embodiments of the inventive concepts;

[0057] FIG. **28** is a flowchart showing a method of forming a semiconductor device in accordance with some embodiments of the inventive concepts;

[0058] FIG. **29** is a flowchart showing a method of forming a semiconductor device in accordance with some embodiments of the inventive concepts;

[0059] FIGS. **30**A, **30**B, **31**A, **31**B, **32**A and **32**B are cross-sectional views showing a method of forming a semiconductor device according to some embodiments of the inventive concepts;

[0060] FIGS. **33** through **35** are cross-sectional views showing a method of forming a semiconductor device according to some embodiments of the inventive concepts;

[0061] FIGS. **36** to **37** are cross-sectional views showing a method of forming a semiconductor device according to some embodiments of the inventive concepts;

[0062] FIG. **38** is a schematic view showing a semiconductor module according to some embodiments of the inventive concepts;

[0063] FIG. **39** is a block diagram showing an electronic system according to some embodiments of the inventive concepts; and

[0064] FIG. **40** is a schematic block diagram showing an electronic system according to some embodiments of the inventive concepts.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0065] The inventive concepts may be embodied in various different forms and should not be construed as limited by some embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough and complete and fully conveys the inventive concepts to those

skilled in the art. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity. The same reference numerals denote the same components throughout the specification.

[0066] Embodiments are described herein with reference to cross-sectional views, plan views, and/or block diagrams that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. Therefore, regions illustrated in the drawings are schematic in nature, and their shapes are not intended to limit the inventive concepts but only to illustrate characteristic forms of regions of devices.

[0067] The thicknesses of layers and regions in the drawings may be exaggerated for the sake of clarity. Further, it will be understood that when a layer is referred to as being "on" another layer or a substrate, the layer may be formed directly on the other layer or the substrate, or there may be an intervening layer therebetween.

[0068] Terms such as "top," "bottom," "upper," "lower," "above," "below," and the like are used herein to describe the relative positions of elements or features. It will be understood that such descriptions are intended to encompass different orientations in use or operation in addition to orientations depicted in the drawings. For example, when an upper part of a drawing is referred to as a "top" and a lower part of a drawing as a "bottom" for the sake of convenience, in practice, the "top" may also be called a "bottom" and the "bottom" a "top" without departing from the teachings of the inventive concepts.

[0069] Furthermore, throughout this disclosure, directional terms such as "upper," "intermediate," "lower," and the like may be used herein to describe the relationship of one element or feature with another, and the inventive concepts should not be limited by these terms. Accordingly, these terms such as "upper," "intermediate," "lower," and the like may be replaced by other terms such as "first," "second," "third," and the like to describe the elements and features.

[0070] It will be understood that, although the terms "first," "second," etc. may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another. Thus, a first element could be termed a second element without departing from the teachings of the present inventive concepts.

[0071] The terminology used herein to describe embodiments is not intended to limit the scope of the inventive concepts.

[0072] As used herein, the singular forms "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including," when used herein, specify the presence of stated features, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, steps, operations, elements, components, and/or groups thereof.

[0073] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which the inventive concepts belong. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0074] FIG. **1** is a conceptual view for schematically describing a semiconductor device in accordance with some embodiments of the inventive concepts. FIGS. **2**A and **2**B are plan views showing a semiconductor device in accordance with some embodiments of the inventive concepts. FIG. **2**B is a plan view in which interconnection structures are added to the drawing of FIG. **2**A in order to avoid complexity of the drawing. FIG. **3**A is a cross-sectional view showing areas taken along the lines I-I' and II-II' of FIG. **2**A, and FIG. **3**B is a cross-sectional view showing areas taken along the lines III-III' and IV-IV' of FIG. **2**B. FIG. **3**C is an enlarged view of the portion "A" shown in FIG. **3**A.

[0075] First, the semiconductor device in accordance with some embodiments of the inventive concepts will be described with reference to FIGS. **1**, **2**A, **2**B, **3**A, **3**B and **3**C.

[0076] Referring to FIGS. **1**, **2**A, **2**B, **3**A, **3**B and **3**C, a peripheral circuit area may be disposed on a semiconductor substrate **2**. The semiconductor substrate **2** may be formed of a semiconductor material such as silicon, etc. The peripheral circuit area may include a first peripheral circuit area PC**1**, a second peripheral circuit area PC**2**, and a third peripheral circuit area PC**3**. The first peripheral circuit area PC**1** may include a page buffer circuit. The first peripheral circuit area PC**1** may include a peripheral transistor PTR that may configure a circuit and a first peripheral interconnection structure PW**1** which is electrically connected to the peripheral transistor PTR. The first peripheral interconnection structure PW**1** may include a first peripheral contact pad part PP**1**.

[0077] The peripheral transistor PTR may include a peripheral gate PG and peripheral impurity regions PS and PD. The peripheral gate PG may be disposed in an active region defined by an isolation area **3**. The peripheral impurity regions PS and PD may be disposed in the active region on both sides of the peripheral gate PG and may serve as a source/drain.

[0078] A lower interlayer insulating layer LILD may be disposed to cover the first to third peripheral circuit areas PC**1**, PC**2**, and PC**3** of the semiconductor substrate **2**. The lower interlayer insulating layer LILD may be formed of an insulating material including silicon oxide. The first peripheral interconnection structure PW**1** and the first peripheral contact pad part PP**1** of the first peripheral interconnection structure PW**1** may be covered by the lower interlayer insulating layer LILD.

[0079] A buffer insulating layer **10** may be disposed on the lower interlayer insulating layer LILD. The buffer insulating layer **10** may have an etch selectivity with respect to a part of the lower interlayer insulating layer LILD being in contact with the buffer insulating layer **10**. For example, the buffer insulating layer **10** may be formed of silicon nitride and the part of the lower interlayer insulating layer LILD being in contact with the buffer insulating layer **10** may be formed of silicon oxide.

[0080] A semiconductor pattern **14** including an opening **16** may be disposed on the buffer insulating layer **10**. The semiconductor pattern **14** may overlap the first peripheral circuit area PC**1**, the second peripheral circuit area PC**2**, and/or the third peripheral circuit area PC**3**. The semiconductor pattern **14** may include a first impurity region LC having

a first conductivity type, a second impurity region **42** having a second conductivity type different from the first conductivity type, a cell body contact impurity region **50** having the first conductivity type and an impurity concentration higher than that of the first impurity region LC, and a third impurity region HC, which has the first conductivity type and an impurity concentration higher than that of the first impurity region LC and is disposed under the first impurity region LC. The first impurity region LC may be referred to as a low concentration impurity region, the second impurity region **42** may be referred to as a cell source impurity region, and the third impurity region HC may be referred to as a high concentration impurity region.

[0081] In some embodiments, the first impurity region LC, the third impurity region HC, and the cell body contact impurity region **50** may have P-type conductivity and the second impurity region **42** may have N-type conductivity.

[0082] The peripheral transistor PTR and the first peripheral interconnection structure PW**1** may be interposed between the semiconductor substrate **2** and the semiconductor pattern **14**.

[0083] A second peripheral interconnection structure PW**2** (shown in FIG. **1**) and a third peripheral interconnection structure PW**3** (shown in FIG. **3**B) may be disposed to be interposed between the semiconductor substrate **2** and the semiconductor pattern **14** and to extend to outside of the semiconductor pattern **14**.

[0084] The second peripheral interconnection structure PW**2** (shown in FIG. **1**) may have a second peripheral contact pad PP**2** in an area in which the second peripheral circuit area PC**2** does not overlap the semiconductor pattern **14**. The third peripheral interconnection structure PW**3** (shown in FIG. **3**B) may have a third peripheral contact pad PP**3** in an area in which the third peripheral circuit area PC**3** does not overlap the semiconductor pattern **14**. The first peripheral contact pad PP**1** of the first peripheral interconnection structure PW**1** may be located between the semiconductor substrate **2** and the semiconductor pattern **14**.

[0085] A gap fill insulating layer **18** may be disposed in the opening **16** of the semiconductor pattern **14**. An intermediate interlayer insulating layer **19** may be disposed on a side surface of the semiconductor pattern **14**. The gap fill insulating layer **18** and the intermediate interlayer insulating layer **19** may be formed of, for example, silicon oxide.

[0086] A cell array area CA and step areas ST**1**, ST**2**, ST**3**, and ST**4** may be disposed on the semiconductor pattern **14**. The step areas ST**1**, ST**2**, ST**3**, and ST**4** may include the first and third step areas ST**1** and ST**3** facing each other and the second and fourth step areas ST**2** and ST**4** facing each other. The cell array area CA may be interposed between the first and third step areas ST**1** and ST**3** and between the second and fourth step areas ST**2** and ST**4** in a plan view.

[0087] Cell gate conductive structures GS**1**, GS**2**, and GS**3** may be disposed on the semiconductor pattern **14**. The cell gate conductive structures GS**1**, GS**2**, and GS**3** may be disposed in the cell array area CA. The cell gate conductive structures GS**1**, GS**2**, and GS**3** may extend from the cell array area CA into the first and third step areas ST**1** and ST**3**.

[0088] The cell gate conductive structures GS**1**, GS**2**, and GS**3** may include a first gate conductive structure GS**1**, a second gate conductive structure GS**2**, and a third gate conductive structure GS**3**. A distance between the first and second gate conductive structures GS**1** and GS**2** may be greater than a distance between the second and third gate conductive structures GS**2** and GS**3**.

[0089] Each of the first to third gate conductive structures GS**1**, GS**2**, and GS**3** may include cell gate conductive patterns **38***a* that are sequentially stacked on the semiconductor pattern **14** and spaced apart from each other. The cell gate conductive patterns **38***a* may be disposed so as to have a step structure in the first step area ST**1** and the second step area ST**2** of the semiconductor pattern **14**. A height of the step structure may be lowered as further away from the cell array area CA.

[0090] Cell interlayer insulating patterns **21** may be interposed between the cell gate conductive patterns **38***a* and between a lowermost pattern of the cell gate conductive patterns **38***a* and the semiconductor pattern **14**. The cell interlayer insulating patterns **21** and the cell gate conductive patterns **38***a* may be alternately and repeatedly stacked.

[0091] An insulating structure **23** may be disposed on the semiconductor pattern **14** between the first and second gate conductive structures GS**1** and GS**2**.

[0092] The insulating structure **23** may include first insulating patterns **20***a* and second insulating patterns **22***a*, which are alternately and repeatedly stacked. Therefore, the insulating structure **23** may include the plurality first insulating patterns **20***a* and the plurality second insulating patterns **22***a*.

[0093] The first insulating pattern **20***a* may have a width greater than the second insulating pattern **22***a* and may have an etch selectivity with respect to the second insulating pattern **22***a*. For example, the first insulating pattern **20***a* may be formed of silicon oxide and the second insulating pattern **22***a* may be formed of silicon nitride.

[0094] Dummy gate conductive patterns **38***b* may be disposed in a horizontal direction of the second insulating pattern **22***a* on the semiconductor pattern **14** between the first and second gate conductive structures GS**1** and GS**2**. Ones of the second insulating patterns **22***a* and respective ones of the cell gate conductive patterns **38***a* may be disposed on the same plane.

[0095] The insulating structure **23** may overlap the opening **16**. The insulating structure **23** may overlap the gap fill insulating layer **18** included in the opening **16**.

[0096] Third insulating patterns **20***b* and fourth insulating patterns **22***b* may be disposed on the second and fourth step areas ST**2** and ST**4** on the semiconductor pattern **14**. The third insulating patterns **20***b* and fourth insulating patterns **22***b* may be alternately and repeatedly stacked and may have a step structure. A height of the step structure may be lowered in a direction further away from the cell array area CA. The third insulating patterns **20***b*, and the first insulating patterns **20***a* and the cell interlayer insulating patterns **21** may be formed of the same material and disposed on the same plane. Stated in other words, one of the third insulating patterns **20***b* , one of the first insulating patterns **20***a* and one of the cell interlayer insulating patterns **21** may be disposed at the same height from an upper surface of the semiconductor pattern **14**. The fourth insulating patterns **22***b* and the second insulating patterns **22***a* may be formed of the same material and disposed on the same plane. In other words, one of the fourth insulating patterns **22***b* and one of the second insulating patterns **22***a* may be disposed at the same height from the upper surface of the semiconductor pattern **14**. The second insulating patterns **22***a* and the fourth insulating patterns **22***b*, and the cell gate conductive patterns **38***a* may be disposed on the

same plane. In other words, one of the second insulating patterns **22***a*, one of the fourth insulating patterns **22***b* and one of the cell gate conductive patterns **38***a* may be disposed at the same height from the upper surface of the semiconductor pattern **14**.

[0097] A first upper interlayer insulating layer **24** may be disposed on the semiconductor substrate **2** on which the cell gate conductive structures GS**1**, GS**2**, and GS**3**, the insulating structure **23**, and the third and fourth insulating patterns **20***b* and **22***b* are disposed.

[0098] Cell vertical structures CV may be disposed in the cell array area CA on the semiconductor pattern **14**. The cell vertical structures CV may be disposed in the first impurity region LC of the semiconductor pattern **14**. The cell vertical structures CV may pass through the first upper interlayer insulating layer **24**, the cell gate conductive patterns **38***a*, and the cell interlayer insulating patterns **21** and may be connected to the first impurity region LC of the semiconductor pattern **14**.

[0099] Each of the cell vertical structures CV may include a first dielectric **27**, a cell semiconductor layer **28**, a core insulating pattern **29**, and a cell pad pattern **30**. The cell pad pattern **30** may be disposed on the core insulating pattern **29**. The cell pad pattern **30** may be formed of, for example, doped silicon. The cell pad pattern **30** may have N-type conductivity.

[0100] The cell semiconductor layer **28** may be disposed so as to surround a side surface and a bottom of the core insulating pattern **29**. The cell semiconductor layer **28** may be formed of a material that may be used as a channel of a transistor, for example, silicon. The first dielectric **27** may be disposed outside the cell semiconductor layer **28**. The cell semiconductor layer **28** may be interposed between the first dielectric **27** and the core insulating pattern **29**.

[0101] A second dielectric **37** may be interposed between the cell vertical structures CV and the cell gate conductive patterns **38***a*.

[0102] One of the first and second dielectrics **27** and **37** may include a data storage layer that may store data. For example, the first dielectric **27** may include a tunnel dielectric layer and a data storage layer, which are sequentially formed from the cell semiconductor layer **28**. The second dielectric **37** may include a blocking dielectric. The first and second dielectrics **27** and **37** may have the same structure as a dielectric between a control gate of a NAND flash memory device and a body of a cell transistor of the NAND flash memory device. However, the scope of the inventive concepts is not limited to a structure of the NAND flash memory device and the inventive concepts may be used for various memory devices.

[0103] A second upper interlayer insulating layer **32** may be disposed on the first upper interlayer insulating layer **24**.

[0104] A plurality of cell source patterns **46** may be disposed on the semiconductor pattern **14** to cross the cell array area CA and to extend into the first and third step areas ST**1** and ST**3**. The cell source patterns **46** may be disposed on the second impurity regions **42**, that is, the cell source impurity regions. The cell source patterns **46** may include a conductive material. The cell source patterns **46** may also include an insulating spacer **40** that may be formed of an insulating material such as silicon oxide, silicon nitride, or the like. The cell source patterns **46** may overlap and be electrically connected to the second impurity regions **42**. The cell source patterns **46** may have a line shape which extends in a first direction X in FIG. **2**A. The cell source patterns **46** may be sequentially arranged in a second direction Y in FIG. **2**A that is perpendicular to the first direction X and extend parallel to each other.

[0105] The cell source patterns **46** may pass through the first and second upper interlayer insulating layers **24** and **32**, vertically extend through the cell gate conductive patterns **38***a*, and be connected to the second impurity regions **42** of the semiconductor pattern **14**.

[0106] The cell source patterns **46** may include a first source pattern **46***a*, a second source pattern **46***b*, and a third source pattern **46***c*, which are sequentially arranged along the first direction X and spaced apart from each other. For example, a distance between the first and second source patterns **46***a* and **46***b* may be greater than a distance between the second and third source patterns **46***b* and **46***c*.

[0107] The cell gate conductive patterns **38***a* may be interposed between two of the cell source patterns **46** that are arranged to have a relatively small distance therebetween, for example, the second and third source patterns **46***b* and **46***c*. The cell gate conductive patterns **38***a* may not be interposed between two of the cell source patterns **46** that are arranged to have a relatively large distance therebetween, for example, the first and second source patterns **46***a* and **46***b*. The insulating structure **23** and the dummy gate conductive patterns **38***b* may be disposed between the two of the cell source patterns **46** that are arranged to have a relatively large distance.

[0108] A third upper interlayer insulating layer **48** may be disposed on the second upper interlayer insulating layer **32** and the cell source patterns **46**. A fourth upper interlayer insulating layer **60** may be disposed on the third upper interlayer insulating layer **48**.

[0109] A bit line contact structure **72** may be disposed to be electrically connected to the peripheral transistor PTR under the semiconductor pattern **14**. The bit line contact structure **72** may pass through the cell array area CA in a vertical direction and may be electrically connected to the first peripheral contact pad PP**1** of the first peripheral circuit area PC**1** under the cell array area CA. In some embodiments, the bit line contact structure **72** may extend through the opening **16** of the semiconductor pattern **14** as illustrated in FIG. **3**A when viewed in cross section. Stated in other words, the bit line contact structure **72** may extend through a gap between two portions of the semiconductor pattern **14** that are spaced apart from each other as illustrated in FIG. **3**A.

[0110] The peripheral bit line contact structure **72** may include a bit line lower contact plug **52** and a bit line upper contact plug **62** on the bit line lower contact plug **52**. The bit line lower contact plug **52** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48**, the insulating structure **23**, the gap fill insulating layer **18**, and a part of the lower interlayer insulating layer LILD which covers the first peripheral contact pad PP**1** and may be electrically connected to the first peripheral contact pad PP**1** of the first peripheral interconnection structure PW**1** which is electrically connected to the peripheral transistor PTR. The bit line upper contact plug **62** may pass through the fourth upper interlayer insulating layer **60** and may be electrically connected to the bit line lower contact plug **52**.

[0111] In some embodiments, as shown in FIG. **3**C, the bit line lower contact plug **52** (shown in FIG. **3**C) may include a plug metal layer **52***b* and a barrier metal layer **52***a* on a side surface of the plug metal layer **52***b*. For example, the plug

metal layer **52***b* may include a metal material and the barrier metal layer **52***a* may include a metal nitride.

[0112] In some embodiments, as shown in FIG. **3**C, an oxide spacer sp may be interposed between the bit line lower contact plug **52** (shown in FIG. **3**C) and a side of a contact hole H. The oxide spacer sp may be formed of silicon oxide.

[0113] Cell bit line plugs **68** may be disposed to be electrically connected to the cell vertical structures CV. The cell bit line plugs **68** may pass through the first to fourth upper interlayer insulating layers **24**, **32**, **48**, and **60**.

[0114] Cell gate contact structures **74** may be disposed to be electrically connected to the cell gate conductive patterns **38***a*. The cell gate contact structures **74** may be disposed in the first step area ST**1**.

[0115] Each of the cell gate contact structures **74** may include a cell gate lower contact structure **54** and a cell gate upper contact structure **64** on the cell gate lower contact structure **54**.

[0116] The cell gate lower contact structure **54** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48** and may be electrically connected to the cell gate conductive patterns **38***a*. The cell gate upper contact structure **64** may pass through the fourth upper interlayer insulating layer **60** and may be electrically connected to the cell gate lower contact structure **54**.

[0117] A cell body contact structure **73** may be disposed to be electrically connected to the cell body contact impurity region **50**. The cell body contact structure **73** may include a cell body lower contact structure **53** and a cell body upper contact structure **63** on the cell body lower contact structure **53**.

[0118] The cell body lower contact structure **53** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48** and the third and fourth insulating patterns **20***b* and **22***b* in step areas located in the second direction Y that is perpendicular to the cell source patterns **46**, and may be connected to the semiconductor pattern **14**. The cell body lower contact structure **53** and the peripheral bit line lower contact plug **52** may have lower surfaces which are located on different planes (i.e., at different height) and upper surfaces located on the same plane (i.e., at the same height). The cell body upper contact structure **63** may pass through the fourth upper interlayer insulating layer **60** and may be electrically connected to the cell body lower contact structure **53**.

[0119] A peripheral body contact structure **75** may be disposed to be interposed between the semiconductor substrate **2** and the semiconductor pattern **14** and to be electrically connected to the third peripheral contact pad PP**3** of the third peripheral interconnection structure PW**3** which extends the outside of the semiconductor pattern **14**. The cell body contact structure **73** may be disposed on and may overlap the semiconductor pattern **14** and the peripheral body contact structure **75** may not overlap the semiconductor pattern **14**. The peripheral body contact structure **75** may be disposed outside the semiconductor pattern **14**.

[0120] The peripheral body contact structure **75** may include a peripheral body lower contact structure **55** and a peripheral body upper contact structure **65** on the peripheral body lower contact structure **55**. The peripheral body lower contact structure **55** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48**, the buffer insulating layer **10**, and a portion of the lower interlayer insulating layer LILD and may be electrically connected to the third peripheral contact pad PP**3**. The peripheral body upper contact structure **65** may pass through the fourth upper interlayer insulating layer **60**.

[0121] An interconnection structure may be disposed on the fourth interlayer insulating layer **60**. The interconnection structure may include cell conductive lines **80**, word line interconnection structures **81**, and body interconnection structures **82**. The cell conductive lines **80** may be cell bit lines.

[0122] The cell conductive lines **80** may be disposed on the cell bit line contact plugs **68** and the peripheral bit line contact structure **72** and electrically connected to the cell bit line contact plugs **68** and the peripheral bit line contact structure **72**. In some embodiments, the cell conductive lines **80** may overlie upper surfaces of the cell bit line contact plugs **68** and the peripheral bit line contact structure **72** as illustrated in FIGS. **2**B and **3**A.

[0123] The cell conductive lines **80** (e.g., the cell bit lines) may each have a length smaller than a width of the semiconductor pattern **14**. The cell conductive lines **80** may have a line shape which extends in the second direction Y. The width of the semiconductor pattern **14** may be a width of the second direction Y. The cell conductive lines **80** may overlap the semiconductor pattern **14**. The cell conductive lines **80** may overlap the semiconductor pattern **14** and may be interposed between side surfaces of the semiconductor pattern **14** in a plan view.

[0124] As shown in FIG. **2**B, the word line interconnection structures **81** may each include a lower word line interconnection **81***a*, a upper word line interconnection **81***b*, and a word line interconnection contact plug **81***c* between the lower and upper word line interconnections **81***a* and **81***b*. The lower word line interconnection **81***a* (shown in FIG. **2**B) may have a line shape extending in the second direction Y that is perpendicular to the cell gate conductive structures GS**1**, GS**2**, and GS**3**, and the upper word line interconnection **81***b* (shown in FIG. **2**B) may have a line shape extending in the first direction X that is perpendicular to the lower word line interconnection **81***a*. The upper word line interconnection **81***b* (shown in FIG. **2**B) may extend from the first step area ST**1** to the outside of the semiconductor pattern **14**.

[0125] In the outside of the semiconductor pattern **14**, a peripheral word line contact structure **77** may be interposed between the word line interconnection structure **81** and the second peripheral contact pad PP**2** of the second peripheral interconnection structure PW**2** of the second peripheral circuit area PC**2**.

[0126] The body interconnection structures **82** may be electrically connected to the cell body contact structure **73** and the peripheral body contact structure **75**.

[0127] In some embodiments, the bit line lower contact plug **52** may have an upper surface disposed on the same plane as an upper surface of the body lower contact plug **53** as illustrated in FIG. **3**A.

[0128] In some embodiments, the bit line lower contact plug **52** may have an upper surface located at a level higher than the cell vertical structures CV and the source patterns **46**. However, the scope of the inventive concepts is not limited thereto.

[0129] In some embodiments, as shown in FIGS. **4**A and **4**B, a bit line lower contact plug **52'** and a body lower contact plug **53'** may be disposed to have upper surfaces which are disposed on the same plane as upper surfaces of the cell

vertical structures CV and are located at a level lower than upper surfaces of the source patterns **46**.

[0130] In some embodiments, as shown in FIGS. **5**A and **5**B, a bit line lower contact plug **52"** and a body lower contact plug **53"** may be disposed to have upper surfaces located at a level lower than the upper surfaces of the cell vertical structures CV and the source patterns **46**.

[0131] The opening **16** of the semiconductor pattern **14** may be formed in a rectangular shape inside the semiconductor pattern **14**. However, the scope of the inventive concepts is not limited thereto.

[0132] In some embodiments, referring to FIG. **6**, the semiconductor pattern **14** (shown in FIG. **6**) may have an opening **16'** having a shape which crosses the cell array area CA and crosses any one of the first and third step areas ST**1** and ST**3**.

[0133] In some embodiments, referring to FIG. **7**, the semiconductor pattern **14** (shown in FIG. **7**) may have an opening **16"** of a shape which crosses the cell array area CA and crosses all the first and third step areas ST**1** and ST**3**. Therefore, the semiconductor pattern **14** (shown in FIG. **7**) may be two semiconductor patterns spaced apart from each other.

[0134] In some embodiments, referring to FIG. **8**, the semiconductor pattern **14** (shown in FIG. **8**) may have a plurality of openings (e.g., **16***a* and **16***b*) which cross the cell array area CA.

[0135] The cell body lower plug **53** may have a line shape as illustrated in FIG. **8**. However, the scope of the inventive concepts is not limited thereto. For example, referring to FIG. **9**, cell body lower plugs **53'"** may include plural elements, and each of cell body lower plugs **53'"** (shown in FIG. **9**) may have a round shape.

[0136] A semiconductor device in accordance with some embodiments of the inventive concepts will be described with reference to FIGS. **1**, **10**, **11**A, and **11**B.

[0137] Referring to FIGS. **1**, **10**, **11**A, and **11**B, as described in FIGS. **2**A, **2**B, **3**A, and **3**B, the peripheral circuit areas PC**1**, PC**2**, and PC**3** may be disposed on the semiconductor substrate **2**, the semiconductor pattern **14** having the opening **16** may be disposed in the peripheral circuit areas PC**1**, PC**2**, and PC**3**, and the cell array area CA and the first to fourth step areas ST**1** to ST**4** may be disposed on the semiconductor pattern **14**.

[0138] As described in FIGS. **2**A, **2**B, **3**A, and **3**B, the cell vertical structures CV, the cell gate conductive patterns **38***a*, and the source patterns **46** may be disposed on the semiconductor pattern **14**, and the cell interlayer insulating patterns **21** may be interposed between the cell gate conductive patterns **38***a*.

[0139] The first to fourth upper interlayer insulating layers **24**, **32**, **48**, and **60** may be disposed as illustrated in FIGS. **2**A, **2**B, **3**A, and **3**B.

[0140] An insulating structure **123** may be interposed between the first and second source patterns **46***a* and **46***b* that are two of the source patterns **46** spaced apart from each other by a relatively long distance. The insulating structure **123** may be disposed on the opening **16** of the semiconductor pattern **14**. The insulating structure **123** may be formed of, for example, silicon oxide.

[0141] First insulating patterns **120***a* may be disposed on a side surface of the insulating structure **123**. The first insulating patterns **120***a* and the cell interlayer insulating patterns **21** may be disposed on the same plane and formed of the same material, for example, silicon oxide.

[0142] Dummy gate conductive patterns **38***b* may be disposed on the side surface of the insulating structure **123** and between the first insulating patterns **120***a*. A second dielectric **37** may be interposed between the dummy gate conductive patterns **38***b* and the insulating structure **123** and between the dummy gate conductive patterns **38***b* and the first insulating patterns **120***a*. The insulating structure **123** may be disposed to have a structure which passes through between the first insulating patterns **120***a* and the dummy gate conductive patterns **38***b*.

[0143] As described in FIGS. **2**A, **2**B, **3**A, and **3**B, the bit line contact structure **72** that is electrically connected to the peripheral transistor PTR under the semiconductor pattern **14**, the cell bit line plugs **68** that are electrically connected to the cell vertical structures CV, the cell gate contact structures **74** that are electrically connected to the cell gate conductive patterns **38***a*, the cell body contact structure **73** that is electrically connected to the cell body contact impurity region **50**, and the peripheral body contact structure **75** that is electrically connected to the third peripheral contact pad PP**3** that extends from the third peripheral interconnection structure PW**3** under the semiconductor pattern **14** to the outside of the semiconductor pattern **14** may be disposed.

[0144] As described in FIGS. **2**A, **2**B, **3**A, and **3**B, the peripheral bit line contact structure **72** may include the bit line lower contact plug **52** and the bit line upper contact plug **62** on the bit line lower contact plug **52**. The bit line lower contact plug **52** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48**, the insulating structure **123**, the gap fill insulating layer **18**, and a part of the lower interlayer insulating layer LILD which covers the first peripheral contact pad PP**1** and may be electrically connected to the first peripheral contact pad PP**1** which is electrically connected to the peripheral transistor PTR.

[0145] The cell conductive lines **80**, that may be, the cell bit lines, the word line interconnection structures **81**, and the body interconnection structures **82** such as those described in FIGS. **2**A, **2**B, **3**A, and **3**B may be disposed.

[0146] A semiconductor device in accordance with some embodiments of the inventive concepts will be described with reference to FIGS. **12**, **13**A, **13**B, **14**A, and **14**B.

[0147] FIG. **12** is a conceptual view showing a semiconductor device in accordance with some embodiments of the inventive concepts. FIGS. **13**A and **13**B are plan views showing a semiconductor device in accordance with some embodiments of the inventive concepts. FIG. **13**B is a plan view in which interconnection structures are added to the drawing of FIG. **13**A in order to avoid complexity of the drawing. A part indicated by line III-III' of FIG. **13**A may correspond to a part indicated by line III-III' of FIG. **2**A. A cross-sectional shape of the part indicated by line III-III' of FIG. **13**A may be substantially the same as a cross-sectional shape of the part indicated by line III-III' of FIG. **3**B. Therefore, since the cross-sectional shape of the part indicated by line III-III' of FIG. **13**A corresponds to the cross-sectional shape of the part indicated by line III-III' of FIG. **3**B, the cross-sectional shape of the part indicated by line III-III' of FIG. **3**B will be referred in below the drawings and descriptions in order to avoid duplication of the drawings.

[0148] FIG. **14** is a cross-sectional view showing areas taken along lines V-V' and VI-VI' of FIG. **13**A.

[0149] Referring to the part indicated by line III-III' of FIG. **3**B and FIGS. **12**, **13**A, **13**B, and **14**, a peripheral circuit area may be disposed on a semiconductor substrate **2**. The periph-

eral circuit area may include a first peripheral circuit area PC**1**, a second peripheral circuit area PC**2**, and a third peripheral circuit area PC**3**. The first peripheral circuit area PC**1** may include a page buffer circuit. As described in FIGS. **1**, **2**A, **2**B, **3**A, and **3**B, the first peripheral circuit area PC**1** may include a peripheral transistor PTR that may configure a peripheral circuit and a first peripheral interconnection structure PW**1** which is electrically connected to the peripheral transistor PTR. The first peripheral interconnection structure PW**1** may include a first peripheral contact pad part PP**1**.

[0150] A lower interlayer insulating layer LILD may be disposed to cover the first to third peripheral circuit areas PC**1**, PC**2**, and PC**3** of the semiconductor substrate **2**. The lower interlayer insulating layer LILD may be formed of an insulating material including silicon oxide. The first peripheral interconnection structure PW**1** and the first peripheral contact pad part PP**1** of the first peripheral interconnection structure PW**1** may be covered by the lower interlayer insulating layer LILD.

[0151] A buffer insulating layer **10** may be disposed on the lower interlayer insulating layer LILD. The buffer insulating layer **10** may have an etch selectivity with respect to a part of the lower interlayer insulating layer LILD being in contact with the buffer insulating layer **10**.

[0152] A semiconductor pattern **214** having an opening **216** may be disposed on the buffer insulating layer **10**. The semiconductor pattern **214** may be formed of polysilicon.

[0153] The semiconductor pattern **214** may include a first impurity region LC having a first conductivity type, a second impurity region **42** having a second conductivity type different from the first conductivity type, a cell body contact impurity region **50**, which has the first conductivity type and an impurity concentration higher than that of the first impurity region LC, and a third impurity region HC, which has the first conductivity type and an impurity concentration higher than that of the first impurity region LC and is disposed under the first impurity region LC. The first impurity region LC may be referred to as a low concentration impurity region, the second impurity region **42** may be referred to as a cell source impurity region, and the third impurity region HC may be referred to as a high concentration impurity region. In some embodiments, the first impurity region LC, the third impurity region HC, and the cell body contact impurity region **50** may have P-type conductivity and the second impurity region **42** may have N-type conductivity.

[0154] A gap fill insulating layer **218** may be disposed in the opening **216** of the semiconductor pattern **214**. An intermediate interlayer insulating layer **219** may be disposed on a side surface of the semiconductor pattern **214**. The gap fill insulating layer **218** and the intermediate interlayer insulating layer **219** may be formed of silicon oxide.

[0155] A cell array area CA and step areas ST**1**, ST**2**, ST**3**, and ST**4** may be disposed on the semiconductor pattern **214**. The step areas ST**1**, ST**2**, ST**3**, and ST**4** may include the first and third step areas ST**1** and ST**3** facing each other and the second and fourth step areas ST**2** and ST**4** facing each other. The cell array area CA may be disposed therebetween the first and third step areas ST**1** and ST**3** and between the second and fourth step areas ST**2** and ST**4**, in a plan view. The first and third step areas ST**1** and ST**3** may be interposed between the second and fourth step areas ST**2** and ST**4**.

[0156] The opening **216** of the semiconductor pattern **214** and the gap fill insulating layer **218** may not overlap the cell array area CA in a plan view. In some embodiments, the opening **216** of the semiconductor pattern **214** and the gap fill insulating layer **218** may be disposed outside of the cell array area CA as illustrated in FIG. **13**A. The opening **216** of the semiconductor pattern **214** and the gap fill insulating layer **218** may be disposed under any one step area of the second and fourth step areas ST**2** and ST**4**, for example, the fourth step area ST**4**.

[0157] Cell gate conductive structures GS may be disposed on the semiconductor pattern **214**. The cell gate conductive structures GS may be disposed in the cell array area CA and may extend to the first and third step areas ST**1** and ST**3**. The cell gate conductive structures GS may be spaced apart from each other by a constant distance. Each of the cell gate conductive structures GS may include cell gate conductive patterns **38***a* stacked in a vertical direction on the semiconductor pattern **214**. The cell gate conductive patterns **38***a* may be formed to have a step structure in the first and third step areas ST**1** and ST**3**. Cell interlayer insulating patterns **21** may be interposed between the cell gate conductive patterns **38***a*.

[0158] An insulating structure **223** may be disposed in any one step area of the second and fourth step areas ST**2** and ST**4** on the semiconductor pattern **214**, for example, the fourth step area ST**4**.

[0159] The insulating structure **223** may include first insulating patterns **220***a* and second insulating patterns **220***b*, which are alternately and repeatedly stacked to have a step structure. A height of the step structure may be lowered as further away from the cell array area CA.

[0160] The first insulating patterns **220***a* and the cell interlayer insulating patterns **21** may be disposed on the same plane and formed of the same material. The second insulating patterns **220***b* and the cell gate conductive patterns **38***a* may be disposed on the same plane. The insulating structure **223** may be disposed on the opening **216** of the semiconductor pattern **214**.

[0161] A first upper interlayer insulating layer **24** may be disposed on the semiconductor substrate **2** on which the cell gate conductive structures GS, the cell interlayer insulating patterns **21**, and the insulating structure **223** are disposed.

[0162] Cell vertical structures CV may be disposed in the cell array area CA on the semiconductor pattern **214**. The cell vertical structures CV may be disposed in the first impurity region LC of the semiconductor pattern **214**. The cell vertical structures CV may pass through the first upper interlayer insulating layer **24**, the cell gate conductive patterns **3 8***a*, and the cell interlayer insulating patterns **21** and may be connected to the first impurity region LC of the semiconductor pattern **214**.

[0163] Each of the cell vertical structures CV may include the first dielectric **27**, the cell semiconductor layer **28**, the core insulating pattern **29**, and the cell pad pattern **30** such as those described in FIGS. **2**A, **3**A, and **3**B.

[0164] As described in FIGS. **2**A, **3**A, and **3**B, a second dielectric **37** may be interposed between the cell vertical structures CV and the cell gate conductive patterns **38***a* and any one of the first and second dielectrics **27** and **37** may include a data storage layer that may store data.

[0165] A second upper interlayer insulating layer **32** may be disposed on the first upper interlayer insulating layer **24**. A plurality of cell source patterns **46** may be disposed on the semiconductor pattern **214** to cross the cell array area CA and to extend into the first and third step areas ST**1** and ST**3**. The source patterns **46** may be disposed on the second impurity regions **42** and may be electrically connected to the second

impurity regions **42**. The cell source patterns **46** may be parallel to each other. The cell source patterns **46** may pass through the first and second upper interlayer insulating layers **24** and **32**, may vertically cross the cell gate conductive patterns **38***a* and be connected to the second impurity regions **42** of the semiconductor pattern **214**.

[0166] A third upper interlayer insulating layer **48** may be disposed on the second upper interlayer insulating layer **32** and the cell source patterns **46**. A fourth upper interlayer insulating layer **60** may be disposed on the third upper interlayer insulating layer **48**.

[0167] A bit line contact structure **272** may be disposed to pass through the fourth step area ST**4** and the semiconductor pattern **214** under the fourth step area ST**4** and to be electrically connected to the peripheral transistor PTR under the semiconductor pattern **214**.

[0168] The bit line contact structure **272** may include a bit line lower contact plug **252** and a bit line upper contact plug **262** on the bit line lower contact plug **252**.

[0169] The bit line lower contact plug **252** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48**, the insulating structure **223**, the gap fill insulating layer **218** in the opening **216**, and a part of the lower interlayer insulating layer LILD which covers the first peripheral contact pad PP**1**, and may be electrically connected to the first peripheral contact pad PP**1** which is electrically connected to the peripheral transistor PTR. The bit line upper contact plug **262** may pass through the fourth upper interlayer insulating layer **60** and be electrically connected to the bit line lower contact plug **252**.

[0170] The cell bit line plugs **68**, the cell gate contact structures **74**, the cell body contact structure **73**, and the peripheral body contact structure **75** such as those described in FIGS. **2**A, **3**A, and **3**B may be disposed.

[0171] Cell conductive lines **280** (e.g., bit lines) may be disposed on the fourth interlayer insulating layer **60**. The cell conductive lines **280** may overlap the cell bit line contact plugs **68** and the bit line contact structure **272** and may be electrically connected to the cell bit line contact plugs **68** and the bit line contact structure **272**. The bit lines **280** may extend from the cell array area CA to the fourth step area ST**4**. In some embodiments, one of the cell conductive lines **280** may overlie upper surfaces of the cell bit line contact plugs **68**, cell vertical structures CV and the bit line contact structure **272** as illustrated in FIG. **14**.

[0172] The word line interconnection structures **81** and the body interconnection structures **82** such as those described in FIGS. **2**A, **3**A, and **3**B may be disposed on the fourth interlayer insulating layer **60**.

[0173] In some embodiments, the bit line lower contact plug **252** may have an upper surface disposed on the same plane as the upper surface of the body lower contact plug **253**.

[0174] In some embodiments, the bit line lower contact plug **252** may have an upper surface located at a level higher than the cell vertical structures CV and the source patterns **46**. However, the scope of the inventive concepts is not limited thereto.

[0175] In some embodiments, as shown in FIG. **15**, a bit line lower contact plug **252'** and a body lower contact plug **253'** may be disposed to be disposed on the same plane as the upper surfaces of the cell vertical structures CV and to have upper surfaces located at a level lower than the upper surfaces of the source patterns **46**.

[0176] In some embodiments, as shown in FIG. **16**, a bit line lower contact plug **252"** and a body lower contact plug **253"** may be disposed to have upper surfaces located at a level lower than the upper surfaces of the cell vertical structures CV and the source patterns **46**.

[0177] A semiconductor device in accordance with some embodiments of the inventive concepts will be described with reference to FIGS. **17** and **18**.

[0178] Referring to FIGS. **17** and **18**, as described in FIGS. **13**A, **13**B, and **14**, the first to third peripheral circuit areas PC**1**, PC**2**, and PC**3** may be disposed on the semiconductor pattern **214**. As described in FIGS. **1**, **2**A, **2**B, **3**A, **3**B, the first peripheral circuit area PC**1** may include a peripheral transistor PTR that may configure a peripheral circuit and a first peripheral interconnection structure PW**1** which is electrically connected to the peripheral transistor PTR. The first peripheral interconnection structure PW**1** may include a first peripheral contact pad part PP**1**.

[0179] A lower interlayer insulating layer LILD may be disposed to cover the first to third peripheral circuit areas PC**1**, PC**2**, and PC**3** of the semiconductor substrate **2**.

[0180] As described in FIGS. **13**A, **13**B, and **14**, the buffer insulating layer **10** may be disposed on the lower interlayer insulating layer LILD, the semiconductor pattern **214** having the opening **216** may be disposed on the buffer insulating layer **10**, and the gap fill insulating layer **218** which fills the opening **216** and the intermediate interlayer insulating layer **219** which is disposed on the side surface of the semiconductor pattern **214** may be disposed.

[0181] The cell gate conductive patterns **38***a*, the second dielectric **37**, the cell vertical structures CV, the cell source patterns **46**, the cell interlayer insulating patterns **21**, and the first to fourth upper interlayer insulating layers **24**, **32**, **48**, and **60** such as those described in FIGS. **13**A, **13**B, and **14** may be disposed on the semiconductor pattern **214**.

[0182] A first insulating structure **323** may be disposed on the gap fill insulating layer **218** of the opening **216** of the semiconductor pattern **214**.

[0183] A second insulating structure **324** may be disposed to be spaced apart from the opening **216** of the semiconductor pattern **214** and the cell gate conductive patterns **38***a*. The first and second insulating structures **323** and **324** may be formed of silicon oxide.

[0184] In some embodiments, the second insulating structure **324** may be disposed on the semiconductor pattern **214** between the first insulating structure **323** and the cell gate conductive patterns **38***a*.

[0185] In some embodiments, first insulating patterns **320***a* and second insulating patterns **320***b* may be disposed to be alternately and repeatedly stacked between the first and second insulating structures **323** and **324**. The first insulating pattern **320***a* may be formed of silicon oxide and the second insulating pattern **320***b* may be formed of silicon nitride.

[0186] In some embodiments, the first and second insulating structures **323** and **324** may be disposed to have a structure which passes through the first upper interlayer insulating layer **24** and the first and second insulating patterns **320***a* and **320***b*.

[0187] As described in FIGS. **13**A, **13**B, and **14**, a bit line contact structure **372** may be disposed to pass through the fourth step area ST**4** and the semiconductor pattern **214** under the fourth step area ST**4** and to be electrically connected to the peripheral transistor PTR under the semiconductor pattern **214**.

[0188] The bit line contact structure **372** may include a bit line lower contact plug **352** and a bit line upper contact plug **362** on the bit line lower contact plug **352**.

[0189] The bit line lower contact plug **352** may pass through the second and third upper interlayer insulating layers **32** and **48**, the first insulating structure **323**, the gap fill insulating layer **218** in the opening **216**, and a part of the lower interlayer insulating layer LILD which covers the first peripheral contact pad PP**1**, and may be electrically connected to the first peripheral contact pad PP**1** which is electrically connected to the peripheral transistor PTR.

[0190] The bit line upper contact plug **362** may pass through the fourth upper interlayer insulating layer **60** and be electrically connected to the bit line lower contact plug **352**.

[0191] In some embodiments, the cell body lower contact structure **53** of the cell body contact structure **73** such as those described in FIGS. **2**A, **3**A, and **3**B may pass through the second insulating structure **324** and be connected to the semiconductor pattern **214**.

[0192] The cell bit line plugs **68**, the cell gate contact structures **74**, and the peripheral body contact structure **75** such as those described in FIGS. **2**A, **3**A, and **3**B may be disposed.

[0193] Cell conductive lines, for example, the bit lines **280**, may be disposed on the fourth interlayer insulating layer **60**. The bit lines **280** may overlap the cell bit line contact plugs **68** and the bit line contact structure **372** and be electrically connected to the cell bit line contact plugs **68** and the bit line contact structure **372** when viewed from a plan perspective. The bit lines **280** may extend from the cell array area CA to the fourth step area ST**4**.

[0194] The word line interconnection structures **81** and the body interconnection structures **82** such as those described in FIGS. **2**A, **3**A, and **3**B may be disposed on the fourth interlayer insulating layer **60**.

[0195] A method of forming a semiconductor device in accordance with some embodiments of the inventive concepts will be described with reference to FIG. **19**.

[0196] Referring to FIG. **19**, a peripheral circuit area may be formed on a semiconductor substrate (Block **10**). A semiconductor pattern may be formed on the peripheral circuit area (Block **20**). A molding structure may be formed on the semiconductor pattern (Block **30**). Cell vertical structures may be formed on the semiconductor pattern to pass through the molding structure (Block **40**). Trenches may be formed (Block **50**). Empty spaces may be formed inside the molding structure (Block **60**). Gate conductive patterns may be formed in the empty spaces (Block **70**). Contact structures may be formed (Block **80**). Interconnection structures may be formed (Block **90**).

[0197] An example of the method of forming the semiconductor device in accordance with some embodiments of the inventive concepts described with reference to FIG. **19** will be described with reference to FIGS. **20**A, **20**B, **21**A, **21**B, **22**A, **22**B, **23**A, **23**B, **24**A, **24**B, **25**A, **25**B, **26**A and **26**B in addition to FIGS. **1**, **2**A, **2**B, **3**A, and **3**B.

[0198] Referring to FIGS. **1**, **2**A, **19**, **20**A, and **20**B, a semiconductor substrate **2** may be prepared. The semiconductor substrate **2** may be a semiconductor substrate formed of a semiconductor material such as silicon, etc. A peripheral circuit area may be formed on the semiconductor substrate **2** (Block **10**). The peripheral circuit area may include a first peripheral circuit area PC**1**, a second peripheral circuit area PC**2**, and/or a third peripheral circuit area PC**3**.

[0199] The first peripheral circuit area PC**1** may include a peripheral transistor PTR that may configure a peripheral circuit and a first peripheral interconnection structure PW**1** electrically connected to the peripheral transistor PTR. The first peripheral interconnection structure PW**1** may be disposed in the first peripheral circuit area PC**1** and may include a first peripheral contact pad PP**1**. The formation of the peripheral transistor PTR may include forming an isolation area **3** which defines an active region, forming a peripheral gate PG in the active region, and forming peripheral impurity regions PS and PD that may serve as a source and a drain on both sides of the peripheral gate PG.

[0200] The second peripheral circuit area PC**2** (shown in FIG. **1**) may include a second peripheral interconnection structure PW**2** (shown in FIG. **1**) having a second peripheral contact pad PP**2**. The third peripheral circuit area PC**3** may include a third peripheral interconnection structure PW**3** having a third peripheral contact pad PP**3**.

[0201] A lower interlayer insulating layer LILD may be formed to cover the peripheral circuits in the first to third peripheral circuit areas PC**1**, PC**2**, and PC**3** of the semiconductor substrate **2**.

[0202] The first peripheral interconnection structure PW**1** may be configured to have a plurality of components including a peripheral plug, a peripheral interconnection, the first peripheral contact pad part PP**1**, etc. The peripheral plug of the first peripheral interconnection structure PW**1** may be formed so as to pass through a part of the lower interlayer insulating layer LILD after the part of the lower interlayer insulating layer LILD may be formed. The peripheral interconnection of the first peripheral interconnection structure PW**1** may be formed so as to be electrically connected to the peripheral plug. The peripheral interconnection and the first peripheral contact pad part PP**1** of the first peripheral interconnection structure PW**1** may be covered by the lower interlayer insulating layer LILD.

[0203] A buffer insulating layer **10** may be formed on the lower interlayer insulating layer LILD. The buffer insulating layer **10** may be formed of a material having an etch selectivity with respect to the lower interlayer insulating layer LILD being in contact with the buffer insulating layer **10**. For example, the part of the lower interlayer insulating layer LILD which covers the first peripheral contact pad part PP**1** of the first peripheral interconnection structure PW**1** may be formed of silicon oxide and the buffer insulating layer **10** may be formed of silicon nitride.

[0204] A semiconductor pattern **14** may be formed on the buffer insulating layer **10**. The semiconductor pattern **14** may have an opening **16**. Portions of the semiconductor pattern **14** may be spaced apart from each other by a gap therebetween as illustrated in FIG. **20**. The formation of the semiconductor pattern **14** having the opening **16** may include forming a semiconductor layer on the buffer insulating layer **10** and patterning the semiconductor layer. The semiconductor pattern **14** may be formed of silicon. The semiconductor pattern **14** may be formed of polysilicon.

[0205] The semiconductor pattern **14** may overlap the first peripheral circuit area PC**1**, the second peripheral circuit area PC**2**, and/or the third peripheral circuit area PC**3** when viewed from a plan perspective. The semiconductor pattern **14** may be formed in the first to third peripheral circuit areas PC**1**, PC**2**, and PC**3** (Block **20**).

[0206] The semiconductor pattern **14** may include a high concentration impurity region HC and a low concentration

impurity region LC which is formed on the high concentration impurity region HC and has an impurity concentration lower than the high concentration impurity region HC. The high concentration impurity region HC and the low concentration impurity region LC may have P-type conductivity.

[0207] Referring to FIGS. **1**, **2**A, **19**, **21**A, and **21**B, after an insulating material layer is formed on the semiconductor substrate **2** on which the semiconductor pattern **14** is formed, the insulating material layer is planarized until the semiconductor pattern **14** is exposed, a gap fill insulating layer **18** is formed to fill an inside of the opening **16** of the semiconductor pattern **14**, and an intermediate interlayer insulating layer **19** may be formed on a side surface of the semiconductor pattern **14**. The gap fill insulating layer **18** and the intermediate interlayer insulating layer **19** may be formed of silicon oxide.

[0208] A molding structure MS may be formed on the semiconductor pattern **14** (Block **30**). The formation of the molding structure MS may include alternately and repeatedly forming a first molding layer **20** and a second molding layer **22** on the semiconductor substrate **2** having the semiconductor pattern **14**, the gap fill insulating layer **18**, and the intermediate interlayer insulating layer **19**, patterning the first and second molding layers **20** and **22**, and then forming end parts of the first and second molding layers **20** and **22** to have a step structure. An end part of the molding structure MS may be formed to have a step structure.

[0209] The first molding layer **20** may be formed of a material having an etch selectivity with respect to the second molding layer **22**. For example, the first molding layer **20** may be formed of silicon oxide and the second molding layer **22** may be formed of silicon nitride.

[0210] Referring to FIGS. **1**, **2**A, **19**, **22**A, and **22**B, a first upper interlayer insulating layer **24** may be formed on the semiconductor substrate **2** having the molding structure MS. The first upper interlayer insulating layer **24** may be formed of silicon oxide. The first upper interlayer insulating layer **24** may be formed so as to cover the molding structure MS and have a substantially flat upper surface.

[0211] Cell vertical structures CV may be formed to pass through the molding structure MS (Block **40**). The cell vertical structures CV may be formed on the semiconductor pattern **14**. The cell vertical structures CV may pass through the first upper interlayer insulating layer **24** and the molding structure MS and be connected to the semiconductor pattern **14**.

[0212] Each of the cell vertical structures CV may include a first cell dielectric **27**, a cell semiconductor layer **28**, a core insulating pattern **29**, and a cell pad pattern **30**. For example, the formation of the cell vertical structures CV may include forming holes which pass through the first upper interlayer insulating layer **24** and the molding structure MS, forming the first cell dielectric **27** on side walls of the holes, conformally forming the cell semiconductor layer **28** on the semiconductor substrate **2** in which the first cell dielectric **27** is formed, forming the core insulating pattern **29** which partially fills the holes in the cell semiconductor layer **28**, forming a pad layer on the semiconductor substrate **2** having the core insulating pattern **29**, and planarizing the pad layer and the cell semiconductor layer **28** until the first upper interlayer insulating layer **24** is exposed, and then forming the cell pad pattern **30** defined in the hole and the cell semiconductor layer **28**.

[0213] The cell semiconductor layer **28** may be connected to the semiconductor pattern **14**. The cell semiconductor layer **28** and the cell pad pattern **30** may be formed of silicon. For example, the cell semiconductor layer **28** and the cell pad pattern **30** may be formed of polysilicon.

[0214] The forming of the first cell dielectric **27** may include forming a data storage material layer (e.g., a silicon nitride layer that may trap the charge, etc.) and a tunnel oxide layer (e.g., silicon oxide). The cell pad pattern **30** may be formed to have N-type conductivity using an ion implantation process.

[0215] Referring to FIGS. **1**, **2**A, **19**, **23**A, and **23**B, a second upper interlayer insulating layer **32** may be formed on the semiconductor substrate **2** having the cell vertical structures CV. The second upper interlayer insulating layer **32** may be formed of silicon oxide.

[0216] Trenches **34** may be formed (Block **50**). The trenches **34** may pass through the first and second upper interlayer insulating layers **24** and **32** and the molding structure MS and may expose the semiconductor pattern **14**.

[0217] In some embodiments, the trenches **34** may cross the molding structure MS.

[0218] The trenches **34** may have line shapes which extend in a first direction X. The trenches **34** may be arranged in a second direction Y perpendicular to the first direction X and extend parallel each other.

[0219] The trenches **34** may be sequentially arranged in the second direction Y and may include a first trench **34***a*, a second trench **34***b*, and a third trench **34***c*, which are parallel to each other. A distance between the adjacent first and second trenches **34***a* and **34***b* may be greater than a distance between the adjacent second and third trenches **34***b* and **34***c*. The cell vertical structures CV may be interposed between the trenches **34** which are more closely spaced apart from each other, for example, between the second and third trenches **34***b* and **34***c* in FIG. **23**A. It will be understood that the second and third trenches **34***b* and **34***c* in FIG. **23**A are more closely spaced apart from each other than the first and second trenches **34***a* and **34***b*.

[0220] The opening **16** of the semiconductor pattern **14** may be disposed in the semiconductor pattern **14** between the trenches **34** which are more widely spaced apart from each other, for example, between the first and second trenches **34***a* and **34***b*.

[0221] Empty spaces **36** may be formed inside the molding structure MS (Block **60**). The formation of the empty spaces **36** may include etching the second molding layers **22** exposed by the trenches **34**. Parts in which the second molding layers **22** are etched may be formed as the empty spaces **36**.

[0222] The second molding layers **22**, which are selected from the second molding layers **22** and are located between the first and second trenches **34***a* and **34***b* which are more widely spaced apart from each other, may remain by partially etching. As described above, the second molding layers **22** which remain between the first and second trenches **34***a* and **34***b* may be defined as second insulating patterns **22***a*.

[0223] Further, the second molding layers **22**, which are selected from the second molding layers **22** and are located in the step areas located at the second direction Y perpendicular to the trenches **34**, may remain by partially etching. As described above, the second molding layers **22** which remain in the step areas may be defined as fourth insulating patterns **22***b*.

[0224] The first molding layers **20** located between the trenches **34**, which are selected from the trenches **34** and are more closely spaced apart from each other, for example, between the second and third trenches **34***b* and **34***c* may be

defined as cell interlayer insulating patterns **21**. The first molding layer **20** located between the first and second trenches **34***a* and **34***b* may be defined as first insulating patterns **20***a*. The first molding layers **20** located in the step areas located at the second direction Y perpendicular to the trenches **34** may be defined as third insulating patterns **20***b*.

[0225] The first insulating patterns **20***a* and the second insulating patterns **22***a* located between the first and second trenches **34***a* and **34***b* which are more widely spaced apart from each other may be defined as an insulating structure **23**. Therefore, the insulating structure **23** may include the first insulating pattern **20***a* and the second insulating pattern **22***a*, which are alternately and repeatedly stacked. The second insulating pattern **22***a* may have a width smaller than that of the first insulating pattern **20***a*.

[0226] Referring to FIGS. **1**, **2**A, **19**, **24**A, and **24**B, a second cell dielectric **37** may be conformally formed on the semiconductor substrate **2** having the empty spaces **36**. Gate conductive patterns may be formed in the empty spaces **36**. The formation of the gate conductive patterns may include forming a conductive material layer on the semiconductor substrate **2** having the second cell dielectric **37** and removing the conductive material layer formed, which is on the second upper interlayer insulating layer **32** and in the trenches **34**, using an etching process.

[0227] The gate conductive patterns may be formed in the empty spaces **36** between the trenches **34**, which are selected from the trenches **34** and are more closely spaced apart from each other, for example, between the second and third trenches **34***b* and **34***c*, the gate conductive patterns which surround side surfaces of the cell vertical structures CV may be defined as cell gate conductive patterns **38***a*, and the gate conductive patterns, that may be formed in the empty spaces **36** between the trenches **34** which are more widely spaced apart, for example, between the first and second trenches **34***a* and **34***b* and in the empty spaces located in the step areas located at a direction perpendicular to the trenches **34**, may be defined as dummy gate conductive patterns **38***b*. The cell gate conductive patterns **38***a* may be formed on end parts located at the first direction X parallel to the trenches **34** to have a step structure.

[0228] Referring to FIGS. **1**, **2**A, **25**A, and **25**B, insulating spacers **40** may be formed on side walls of the trenches **34**. The insulating spacer **40** may be formed of an insulating material such as silicon oxide, silicon nitride, or the like.

[0229] A cell source impurity region **42** may be formed in the semiconductor pattern **14** exposed by the trenches **34** by performing an ion implantation process. The cell source impurity region **42** may be formed in the low concentration impurity region LC of the semiconductor pattern **14**. The cell source impurity region **42** may have a conductivity type differ from the low concentration impurity region LC. For example, the low concentration impurity region LC may have P-type conductivity and the cell source impurity region **42** may have N-type conductivity.

[0230] Cell source patterns **46** may be formed in the trenches **34**. The cell source patterns **46** may be formed of a conductive material (e.g., a material such as Ti, TiN, W, or the like).

[0231] The cell source patterns **46** may include first to third source patterns **46***a*, **46***b*, and **46***c* corresponding to the first to third trenches **34***a*, **34***b*, and **34***c* described in FIGS. **23**A and **23**B.

[0232] A third upper interlayer insulating layer **48** may be formed on the semiconductor substrate **2** having the cell source patterns **46**. The third upper interlayer insulating layer **48** may be formed of silicon oxide.

[0233] Referring to FIGS. **1**, **2**A, **26**A, and **26**B, a peripheral bit line lower contact plug **52**, a cell body lower contact structure **53**, a cell gate lower contact plug **54**, and a peripheral body lower contact structure **55** may be formed.

[0234] The peripheral bit line lower contact plug **52** may be interposed between the first and second source patterns **46***a* and **46***b*. The peripheral bit line lower contact plug **52** may pass through insulating material layers located on the first peripheral contact pad PP**1** and may be connected to the first peripheral contact pad PP**1**. For example, the peripheral bit line lower contact plug **52** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48**, the first and second insulating patterns **20***a* and **22***a*, the gap fill insulating layer **18**, and a part of the lower interlayer insulating layers LILD, which is selected from the lower interlayer insulating layers LILD and covers the peripheral pads PP**1** and PP**2**, and may be electrically connected to the first peripheral contact pad PP**1**.

[0235] The cell body lower contact structure **53** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48** and the third and fourth insulating patterns **20***b* and **22***b* in the step areas located in the second direction Y perpendicular to the cell source patterns **46**, and may be connected to the semiconductor pattern **14**.

[0236] In some embodiments, the cell body lower contact structure **53** may be formed in a line shape.

[0237] In some embodiments, the cell body lower contact structure **53** may be formed in a shape of a plurality of circles spaced apart from each other.

[0238] The cell gate lower contact plug **54** may pass through the first to third upper interlayer insulating layers **24**, **32**, and **48** and be connected to the cell gate conductive patterns **38***a* in the step area located between the cell source patterns **46**.

[0239] The peripheral body lower contact structure **55** may sequentially pass through a part of the lower interlayer insulating layer LILD located on the third peripheral contact pad PP**3**, the buffer insulating layer **10**, the intermediate interlayer insulating layer **19**, and the first to third upper interlayer insulating layers **24**, **32**, and **48**, and may be electrically connected to the third peripheral contact pad PP**3**.

[0240] The formation of the peripheral bit line lower contact plug **52**, the cell body lower contact structure **53**, the cell gate lower contact plug **54**, and the peripheral body lower contact structure **55** may include forming contact holes by performing a photolithography process and an etching process, and forming a conductive material layer which fills the contact holes.

[0241] In some embodiments, before the contact holes are formed and filled with the conductive material layer, impurities may be implanted in contact parts exposed by the contact holes by performing an ion implantation process. Therefore, a cell body contact impurity region **50** may be formed in the semiconductor pattern **14** under the cell body lower contact structure **53**. The cell body contact impurity region **50** may have P-type conductivity. The cell body contact impurity region **50** may be formed to have an impurity concentration higher than the low concentration impurity region LC.

[0242] Referring again to FIGS. **1**, **2**A, **2**B, **3**A, **3**B, and **19**, a fourth upper interlayer insulating layer **60** may be formed on

the semiconductor substrate **2** having the peripheral bit line lower contact plug **52**, the cell body lower contact structure **53**, the cell gate lower contact plug **54**, and the peripheral body lower contact structure **55**.

[0243] A peripheral bit line upper contact plug **62**, a cell body upper contact structure **63**, cell gate upper contact plugs **64**, a peripheral body upper contact structure **65**, and cell bit line contact plugs **68** may be formed.

[0244] The peripheral bit line upper contact plug **62** may pass through the fourth upper interlayer insulating layer **60** and may be electrically connected to the peripheral bit line lower contact plug **52**. A peripheral bit line contact structure **72** may include the peripheral bit line upper contact plug **62** and the peripheral bit line lower contact plug **52**.

[0245] The cell body upper contact structure **63** may pass through the fourth upper interlayer insulating layer **60** and be electrically connected to the cell body lower contact structure **53**. A cell body contact structure **73** may include the cell body upper contact structure **63** and the cell body lower contact structure **53**.

[0246] The cell gate upper contact plugs **64** may pass through the fourth upper interlayer insulating layer **60** and be electrically connected to the cell gate lower contact plug **54**.

[0247] A cell gate contact structure **74** may include the cell gate upper contact plugs **64** and the cell gate lower contact plug **54**.

[0248] The peripheral body upper contact structure **65** may pass through the fourth upper interlayer insulating layer **60** and be electrically connected to the peripheral body lower contact structure **55**. A peripheral body contact structure **75** may include the peripheral body upper contact structure **65** and the peripheral body lower contact structure **55**.

[0249] In some embodiments, the peripheral word line contact structure **77** (shown in FIG. **1**) may be formed. The peripheral word line contact structure **77** may be simultaneously or concurrently formed with the peripheral body contact structure **75** to have the same structure as the peripheral body contact structure **75**. Therefore, the peripheral word line contact structure **77** may include a peripheral lower word line contact plug and a peripheral upper word line contact plug corresponding to the peripheral body lower contact structure **55** and the peripheral body upper contact structure **65** of the peripheral body contact structure **75**.

[0250] The cell bit line contact plugs **68** may pass through the second to fourth upper interlayer insulating layers **32**, **48**, and **60** and be formed on the cell pad patterns **30**.

[0251] Then, interconnection structures may be formed on the fourth interlayer insulating layer **60** by performing an interconnection process (Block **90**). The interconnection structures may include bit lines **80**, word line interconnection structures **81**, and body interconnection structures **82**.

[0252] The bit lines **80** may overlap and may be electrically connected to the cell bit line contact plugs **68** and the peripheral bit line contact structure **72**.

[0253] The word line interconnection structures **81** may be electrically connected to the cell gate contact structure **74** and the peripheral word line contact structure **77**.

[0254] The body interconnection structures **82** may be electrically connected to the cell body contact structure **73** and the peripheral body contact structure **75**.

[0255] Therefore, the semiconductor device such as that described in FIGS. **1**, **2**A, **2**B, **3**A, and **3**B may be formed. An example of the method of forming the semiconductor device such as that described in FIGS. **4**A and **4**B will be described with reference to FIG. **27** using the method of forming the semiconductor device in accordance with some embodiments of the inventive concepts.

[0256] Referring to FIG. **27**, as described in FIG. **19**, the peripheral circuit area may be formed on the semiconductor substrate (Block **10**), the semiconductor pattern may be formed on the peripheral circuit area (Block **20**), the molding structure may be formed on the semiconductor pattern (Block **30**), and the vertical structures which pass through the molding structure may be formed on the semiconductor pattern (Block **40**).

[0257] First contact plugs may be formed to pass through the molding structure (Block **140**). The first contact plugs may be a peripheral bit line lower contact plug **52'** and a cell body lower contact plug **53'** shown in FIGS. **4**A and **4**B.

[0258] As described in FIG. **19**, the trenches may be formed (Block **50**), the empty spaces may be formed inside the molding structure (Block **60**), and the gate conductive patterns may be formed inside the empty spaces (Block **70**).

[0259] Second contact plugs may be formed (Block **180**). The second contact plugs may be the cell gate lower contact plugs **54** and the peripheral body lower contact plugs **55** shown in FIG. **4**B. Cell bit line contact plugs **68**, a bit line upper contact plug **62'**, and a peripheral upper body contact plug **65** may be formed. Then, as described in FIG. **19**, the interconnection structures may be formed (Block **90**).

[0260] Next, an example of the method of forming the semiconductor device such as that described in FIGS. **5**A and **5**B will be described with reference to FIG. **28**.

[0261] Referring to FIG. **28**, as described in FIG. **19**, the peripheral circuit area may be formed on the semiconductor substrate (Block **10**), the semiconductor pattern may be formed on the peripheral circuit area (Block **20**), and the molding structure may be formed on the semiconductor pattern (Block **30**). First contact plugs may be formed to pass through the molding structure (Block **240**). The first contact plugs may be a bit line lower contact plug **52"** and a body lower contact plug **53"** shown in FIGS. **5**A and **5**B.

[0262] As described in FIG. **19**, the vertical structures may be formed to pass through the molding structure (Block **40**), the trenches may be formed (Block **50**), the empty spaces may be formed inside the molding structure (Block **60**), and the gate conductive patterns may be formed in the empty spaces (Block **70**). Second contact plugs may be formed (Block **280**). The second contact plugs may be the cell gate lower contact plug **54** and the peripheral body lower contact plugs **55** shown in FIG. **5**B. Cell bit line contact plugs **68**, a bit line upper contact plug **62**, a cell gate upper contact structure **64**, and a peripheral upper body contact plug **65** may be formed. Then, as described in FIG. **19**, the interconnection structures may be formed (Block **90**).

[0263] Next, an example of the method of forming a semiconductor device in accordance with some embodiments of inventive concepts will be described with reference to FIG. **29**.

[0264] Referring to FIG. **29**, as described in FIG. **19**, the peripheral circuit area may be formed on the semiconductor substrate (Block **10**), the semiconductor pattern may be formed on the peripheral circuit area (Block **20**), and the molding structure may be formed on the semiconductor pattern (Block **30**). An insulating structure may be formed to pass through the molding structure (Block **340**). Contact structures may be formed (Block **350**). Interconnection structures may be formed (Block **360**).

[0265] A method of forming a semiconductor device in accordance with some embodiments of inventive concepts will be described with reference to FIGS. **1**, **10**, **29**, **30**A, **30**B, **31**A, **31**B, **32**A and **32**B.

[0266] Referring to FIGS. **1**, **10**, **29**, **30**A, **30**B, **31**A, **31**B, **32**A and, as described in FIGS. **20**A and **20**B, the peripheral circuit areas PC**1**, PC**2**, and PC**3** may be formed on the semiconductor substrate **2** (Block **10**), the peripheral transistor PTR that may be included in the peripheral circuit areas PC**1**, PC**2**, and PC**3** and the lower interlayer insulating layer LILD which covers the peripheral interconnection structure PW may be formed on the semiconductor substrate **2**, and the buffer insulating layer **10** and the semiconductor pattern **14** having the opening **16** may be formed on the lower interlayer insulating layer LILD. The semiconductor pattern **14** may be formed on the peripheral circuit areas PC**1**, PC**2**, and PC**3** (Block **20**).

[0267] As described in FIGS. **21**A and **21**B, the gap fill insulating layer **18** which fills the opening **16** of the semiconductor pattern **14** and the intermediate interlayer insulating layer **19** which covers a side surface of the semiconductor pattern **14** may be formed, and the molding structure MS may be formed on the semiconductor pattern **14** and the gap fill insulating layer **18**. The molding structure MS may include the first molding layer **20** and the second molding layer **22**, which are alternately and repeatedly stacked.

[0268] As described in FIGS. **22**A and **22**B, the first upper interlayer insulating layer **24** may be formed on the semiconductor substrate **2** having the molding structure MS and a plurality of cell vertical structures CV may be formed to pass through the first upper interlayer insulating layer **24** and the molding structure MS on the molding structure MS and to be connected to the semiconductor pattern **14**.

[0269] In some embodiments, the insulating structure **123** may be formed to be interposed between the cell vertical structures CV and on the opening **16** of the semiconductor pattern **14** and to pass through the first upper interlayer insulating layer **24** on the molding structure MS and the molding structure MS.

[0270] The insulating structure **123** may be formed of silicon oxide. An area size (e.g., width) of the insulating structure **123** may be greater than an area size (e.g., width) of the opening **16** of the semiconductor pattern **14**.

[0271] In some embodiments, after the cell vertical structures CV are formed, the insulating structure **123** may be formed. However, the scope of the inventive concepts is not limited thereto. For example, after the insulating structure **123** is formed, the cell vertical structures CV may be formed.

[0272] Referring to FIGS. **1**, **20**, **31**A, and **31**B, as described in FIGS. **23**A and **23**B, the second upper interlayer insulating layer **32** may be formed on the semiconductor substrate **2** having the cell vertical structures CV and the insulating structure **123**, trenches **34** may be formed to pass through the first and second upper interlayer insulating layers **24** and **32** and the molding structure MS, and empty spaces **36** may be formed by partially etching the second molding layers **22** exposed by the trenches **34**.

[0273] Since the insulating structure **123** may be formed of a material having an etch selectivity with respect to the second molding layers **22**, the insulating structure **123** may have an etch-resistant characteristic in a process of etching the second molding layers **22**.

[0274] As described in FIGS. **23**A and **23**B, the trenches **34** may include the first trench **34***a*, the second trench **34***b*, and the third trench **34***c*, the first molding layers **20** may remain between the first and second trenches **34***a* and **34***b* which are more closely spaced apart from each other and may be formed as first insulating patterns **120***a*, and the insulating structure **123** may be located therebetween. Therefore, the first insulating patterns **120***a* may have a shape which is disposed on a side surface of the insulating structure **123**.

[0275] Referring to FIGS. **1**, **10**, **32**A, and **32**B, as described in FIGS. **24**A and **24**B, the second dielectric **37** may be formed on the semiconductor substrate **2** having the empty spaces **36**, and the cell gate conductive patterns **38***a* and the dummy gate conductive patterns **38***b* and **38***c* may be formed.

[0276] As described in FIGS. **25**A and **25**B, the method may include forming the insulating spacer **40** on side walls of the trenches **34**, forming the cell source impurity region **42** in the semiconductor pattern **14** under the trenches **34**, forming the source patterns **46** which fill the trenches **34**, and forming the third upper interlayer insulating layer **48**.

[0277] As described in FIGS. **26**A and **26**B, the peripheral bit line lower contact plug **52**, the cell body lower contact structure **53**, the cell gate lower contact plug **54**, and the peripheral body lower contact structure **55** may be formed.

[0278] The peripheral bit line lower contact plug **52** may pass through the second and third upper interlayer insulating layers **32** and **38**, insulating structure **123**, the gap fill insulating layer **18** in the opening **16** of the semiconductor pattern **14**, the buffer insulating layer **10**, and the lower interlayer insulating layer LILD on the first peripheral contact pad PP**1**.

[0279] As described in FIGS. **26**A and **26**B, after contact holes for forming the peripheral bit line lower contact plug **52**, the cell body lower contact structure **53**, the cell gate lower contact plug **54**, and the peripheral body lower contact structure **55** are formed, the cell body contact impurity region **50** may be formed in the semiconductor pattern **14**.

[0280] Referring again to FIGS. **1**, **10**, **11**A, and **11**B, as described with reference to FIGS. **3**A and **3**B in addition to in FIGS. **1**, **2**A, **2**B, and **19**, the fourth upper interlayer insulating layer **60** may be formed, the peripheral bit line upper contact plug **62**, the cell body upper contact structure **63**, the cell gate upper contact plugs **64**, the peripheral body upper contact structure **65**, and the cell bit line contact plugs **68** may be formed, and the interconnection structures **80**, **81**, and **82** may be formed.

[0281] Next, an example of a method of forming the semiconductor device such as that described in FIGS. **12**, **13**A, **13**B, and **14** will be described with reference to FIGS. **33** to **35**.

[0282] Referring to FIGS. **12**, **13**A, and **33**, as described in FIGS. **20**A and **20**B, the peripheral circuit areas PC**1**, PC**2**, and PC**3** may be formed on the semiconductor substrate **2**, the peripheral transistor PTR that configures circuits of the peripheral circuit areas PC**1**, PC**2**, and PC**3** on the semiconductor substrate **2** and the lower interlayer insulating layer LILD which covers the peripheral interconnection structure PW may be formed on the semiconductor substrate **2**, and the buffer insulating layer **10** may be formed on the lower interlayer insulating layer LILD.

[0283] A semiconductor pattern **214** having an opening **216** may be formed on the buffer insulating layer **10**.

[0284] A gap fill insulating layer **218** which fills the opening **216** of the semiconductor pattern **214** and an intermediate interlayer insulating layer **219** which covers the side surface of the semiconductor pattern **214** may be formed.

[0285] As shown in FIGS. **21**A and **21**B, the molding structure MS may be formed on the semiconductor pattern **214** and the gap fill insulating layer **218**. The molding structure MS may include the first molding layer **20** and the second molding layer **22**, which are alternately and repeatedly stacked.

[0286] As shown in FIGS. **22**A and **22**B, the first upper interlayer insulating layer **24** may be formed on the semiconductor substrate **2** having the molding structure MS and the plurality of cell vertical structures CV may be formed to pass through the first upper interlayer insulating layer **24** on the molding structure MS and the molding structure MS and to be connected to the semiconductor pattern **14**.

[0287] Referring to FIGS. **12**, **13**A and **34**, the second upper interlayer insulating layer **32** may be formed on the semiconductor substrate **2** having the cell vertical structures CV.

[0288] The trenches **234** may be formed to pass through the first and second upper interlayer insulating layers **24** and **32** and the molding structure MS. The trenches **234** may be arranged to have a predetermined distance.

[0289] The empty spaces **36** may be formed by partially etching the second molding layers **22** exposed by the trenches **234**, and the second dielectric **37** and cell gate conductive patterns **38***a* may be formed in the empty spaces **36** by performing substantially the same process described in FIGS. **23**A and **23**B.

[0290] In some embodiments, the molding structure MS may be formed as an insulating structure **223** by remaining in the second and fourth step areas ST**2** and ST**4**. The insulating structure **223** may include a first insulating pattern **220***a* and a second insulating pattern **220***b*, which are alternately and repeatedly stacked to have a step structure.

[0291] The first molding layer **20** which remains between the cell gate conductive patterns **38***a* may be defined as cell interlayer insulating patterns **21**.

[0292] An insulating spacer **40** may be formed on side walls of the trenches **234**.

[0293] A cell source impurity region **242** may be formed in the semiconductor pattern **214** under the trenches **234** by performing an ion implantation process. The cell source impurity region **242** may be formed to have a conductivity type different from a low concentration impurity region LC of the semiconductor pattern **214**. Source patterns **246** may be formed on the trenches **234**.

[0294] Referring to FIGS. **12**, **13**A, and **35**, a second upper interlayer insulating layer **32** may be formed on the semiconductor substrate **2** having the source patterns **246**. Lower contact plugs **252**, **253**, and **255** may be formed to pass through the second upper interlayer insulating layer **32**.

[0295] In some embodiments, before the lower contact plugs **252**, **253**, and **255** are formed, contact holes for forming the lower contact plugs **252**, **253**, and **255** may be formed, and impurities may be implanted in contact parts exposed by the contact holes by performing an ion implantation process. Therefore, a cell body contact impurity region **50** may be formed in the semiconductor pattern **14** under the cell body lower contact plug **253**.

[0296] Referring again to FIGS. **12**, **13**A, **13**B, and **14**, a fourth upper interlayer insulating layer **60** may be formed on the semiconductor substrate **2** having the lower contact plugs **252**, **253**, and **255**. Cell bit line plugs **68** may be formed to pass through the second to fourth interlayer insulating layers **32**, **48**, and **60** and to be connected to the cell vertical structures CV. A bit line upper contact plug **262** may be formed to pass through the fourth upper interlayer insulating layer **60** and to be connected to the lower contact plug **252**. A cell body upper contact structure **63** may be formed to be connected to the cell body lower contact structure **53**. A peripheral body upper contact structure **65** may be formed to be connected to the peripheral body lower contact structure **55**.

[0297] Then, interconnection structures may be formed on the fourth upper interlayer insulating layer **60**. The interconnection structures may include bit lines **280**, word line interconnection structures **81**, and body interconnection structures **82**. The bit lines **280** may be connected to the cell bit line plugs **68** and the bit line upper contact plug **262**.

[0298] Next, an example of the method of forming the semiconductor device such as that described in FIGS. **12**, **17**, and **18** will be described with reference to FIGS. **36** and **37**.

[0299] Referring to FIGS. **12**, **17**, and **36**, as described in FIG. **33**, the peripheral circuit areas PC**1**, PC**2**, and PC**3**, the buffer insulating layer **10**, the semiconductor pattern **214** having the opening **216**, the molding structure MS, the first upper interlayer insulating layer **24**, and the vertical structures CV may be formed on the semiconductor substrate **2**.

[0300] In some embodiments, before the vertical structures CV are formed, a first insulating structure **323** and a second insulating structure **324** may be formed to pass through the first upper interlayer insulating layer **24** and the molding structure MS. However, the scope of the inventive concepts is not limited thereto. For example, after the vertical structures CV are formed, the first insulating structure **323** and the second insulating structure **324** may be formed to pass through first upper interlayer insulating layer **24** and the molding structure MS.

[0301] The first and second insulating structures **323** and **324** may be formed of silicon oxide. The first insulating structure **323** may overlap the opening **216** of the semiconductor pattern **214** when viewed from a plan perspective. The second insulating structure **324** may not overlap the opening **216** of the semiconductor pattern **214** when viewed from a plan perspective.

[0302] Referring to FIGS. **12**, **17**, and **37**, a second upper interlayer insulating layer **32** may be formed on the first upper interlayer insulating layer **24**. The cell source patterns **46**, the cell source impurity region **242** under the cell source patterns **46**, and the insulating spacers **40** on side surfaces of the cell source patterns **46** may be formed by performing substantially the same process described in FIGS. **25**A and **25**B.

[0303] Referring again to FIGS. **12**, **17**, and **18**, a third upper interlayer insulating layer **48** may be formed on the second upper interlayer insulating layer **32** to cover the cell source patterns **46**.

[0304] A bit line lower contact plug **352** may be formed to pass through the second and third upper interlayer insulating layers **32** and **48**, the first insulating structure **323**, and the gap fill insulating layer **218** in the opening **216** of the semiconductor pattern **214** and to be connected to the first peripheral pad PP**1** of the first peripheral circuit area PC**1**.

[0305] In some embodiments, while the bit line lower contact plug **352** is formed, a cell body lower contact plug **355** may be formed to pass through the second and third upper interlayer insulating layers **32** and **48** and the second insulating structure **324** and to be connected to the semiconductor pattern **214**.

[0306] In some embodiments, the formation of the lower contact plugs **352** and **355** may include forming a bit line peripheral lower contact hole which exposes the first peripheral pad PP**1** and a cell body contact hole which exposes the

semiconductor pattern **214**, forming a cell body contact impurity region **50** in the semiconductor pattern **214** by performing an ion implantation process, and filling the contact holes with a metal material. Then, a fourth upper interlayer insulating layer **60** may be formed, upper contact plugs **68** and **372** may be formed, and interconnection structures may be formed.

[0307] FIG. **38** is a schematic view showing a semiconductor module **400** according to some embodiments of the inventive concepts.

[0308] Referring to FIG. **38**, the semiconductor module **400** may include memory devices **430** formed on a module substrate **410**. The semiconductor module **400** may include a semiconductor device **420** mounted on the module substrate **410**.

[0309] The memory device **430** may include the semiconductor device according to some embodiments of the inventive concepts. Input/output terminals **440** may be disposed on at least one side of the module substrate **410**.

[0310] FIG. **39** is a block diagram showing an electronic system **500** according to some embodiments of the inventive concepts.

[0311] Referring to FIG. **39**, the electronic system **500** including the semiconductor device manufactured according to some embodiments of the inventive concepts may be provided.

[0312] The electronic system **500** may include a body **510**. The body **510** may include a microprocessor unit **520**, a power supply **530**, a function unit **540**, and/or a display controller unit **550**. The body **510** may be a system board or a motherboard having a printed circuit board (PCB), etc.

[0313] The microprocessor unit **520**, the power supply **530**, the function unit **540**, and the display controller unit **550** may be installed or mounted on the body **510**. A display unit **560** may be disposed on an upper surface of the body **510** or outside the body **510**. For example, the display unit **560** may be disposed on a surface of the body **510**, and then may display an image processed by the display controller unit **550**. The power supply **530** may receive a constant voltage from an external power supply, divide the voltage into various voltage levels, and supply those voltages to the microprocessor unit **520**, the function unit **540**, the display controller unit **550**, etc. The microprocessor unit **520** may receive a voltage from the power supply **530** to control the function unit **540** and the display unit **560**.

[0314] The function unit **540** may perform various functions of the electronic system **500**. For example, when the electronic system **500** is a mobile electronic product such as a cellular phone, etc., the function unit **540** may include various components which perform dialing, or wireless communication functions such as outputting an image to the display unit **560** or outputting a voice to a speaker through communication with an external apparatus **570**, and when a camera is included, the function unit **540** may serve as an image processor.

[0315] In some embodiments, when the electronic system **500** is connected to a memory card to expand the capacity thereof, the function unit **540** may be a memory card controller. The function unit **540** may exchange signals with the external apparatus **570** through a wired or wireless communication unit **580**.

[0316] Further, when the electronic system **500** requires a Universal Serial Bus (USB) to extend the functions thereof, the function unit **540** may serve as an interface controller.

[0317] FIG. **40** is a schematic block diagram showing an electronic system **600** according to some embodiments of the inventive concepts

[0318] Referring to FIG. **40**, the electronic system **600** may include the semiconductor device in accordance with some embodiments of the inventive concepts. The electronic system **600** may include a memory system **612**, a microprocessor **614**, a RAM **616**, and a user interface **618** which performs data communication using a bus **620**. The microprocessor **614** may program and control the electronic system **600**. The RAM **616** may be used as an operational memory of the microprocessor **614**. The microprocessor **614**, the RAM **616**, and/or other components may be assembled within a single package. The memory system **612** may include the semiconductor device according to some embodiments of the inventive concepts.

[0319] The user interface **618** may be used to input data to the electronic system **600** or output data from the electronic system **600**. The memory system **612** may store operational codes of the microprocessor **614**, data processed by the microprocessor **614**, or data received from the outside. The memory system **612** may include a controller and a memory.

[0320] According to some embodiments of the inventive concepts, a 3-dimentional semiconductor device capable of improving a degree of integration can be provided.

[0321] According to some embodiments of the inventive concepts, since a peripheral circuit area and a memory cell array area are vertically arranged, and a contact structure, which electrically connects a bit line of the memory cell array area to the peripheral circuit area, is disposed to vertically pass through the memory cell array area or is disposed at a location close to the memory cell array area, a degree of integration can be improved.

[0322] Although a few embodiments have been described, those skilled in the art will readily appreciate that many modifications are possible in embodiments without materially departing from the novel teachings and advantages. Accordingly, all such modifications are intended to be included within the scope of the inventive concepts as defined in the claims.

1. A semiconductor device comprising:

a semiconductor pattern disposed on a semiconductor substrate, wherein the semiconductor pattern comprises an opening, a first impurity region having a first conductivity type and a second impurity region having a second conductivity type that is different from the first conductivity type;

a peripheral transistor disposed between the semiconductor substrate and the semiconductor pattern;

a first peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern and electrically connected to the peripheral transistor;

cell gate conductive patterns disposed on the semiconductor pattern;

cell vertical structures extending through respective ones of the cell gate conductive patterns and being connected to the semiconductor pattern;

cell bit line contact plugs disposed on respective ones of the cell vertical structures;

a bit line disposed on the cell bit line contact plugs; and

a peripheral bit line contact structure being disposed between the bit line and the first peripheral interconnection structure and extending through the opening of the semiconductor pattern.

2. The device of claim **1**, wherein the semiconductor pattern further comprises a body contact impurity region that has

the first conductivity type and has an impurity concentration higher than an impurity concentration of the first impurity region.

3. The device of claim **2**, further comprising a cell body contact structure disposed on the body contact impurity region.

4. The device of claim **3**, further comprising:

a second peripheral interconnection structure that is disposed between the semiconductor substrate and the semiconductor pattern and extends outside of the semiconductor pattern;

a peripheral body contact structure that is disposed outside of the semiconductor pattern and is disposed on the second peripheral interconnection structure; and

a cell body interconnection structure that is disposed on the peripheral body contact structure and the cell body contact structure and is electrically connected to the peripheral body contact structure and the cell body contact structure.

5.-**10**. (canceled)

11. A semiconductor device comprising:

a semiconductor pattern disposed on a semiconductor substrate;

a peripheral transistor disposed between the semiconductor substrate and the semiconductor pattern;

a peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern, wherein the peripheral interconnection structure is electrically connected to the peripheral transistor and comprises a peripheral contact pad;

a gate conductive structure disposed on the semiconductor pattern, wherein the gate conductive structure comprises a plurality of cell gate conductive patterns stacked in a direction perpendicular to the semiconductor pattern;

a cell vertical structure extending through the gate conductive structure;

a cell conductive line disposed on the cell vertical structure, wherein the cell conductive line has a length smaller than a width of the semiconductor pattern; and

a peripheral contact structure disposed between the cell conductive line and the peripheral contact pad.

12. The device of claim **11**, wherein the cell conductive line has a line shape which extends in a first direction and the width of the semiconductor pattern is a width of the semiconductor pattern in the first direction.

13. The device of claim **11**, further comprising a lower interlayer insulating layer on the semiconductor substrate and a buffer insulating layer disposed between the lower interlayer insulating layer and the semiconductor pattern.

14. The device of claim **13**, wherein the semiconductor pattern comprises an opening,

wherein the device further comprises a gap fill insulating layer filling the opening of the semiconductor pattern, and

wherein the gap fill insulating layer comprises a material having an etch selectivity with respect to the buffer insulating layer, and the peripheral contact structure extends through the gap fill insulating layer.

15. The device of claim **11**, further comprising an insulating structure disposed on the semiconductor pattern, wherein the peripheral contact structure extends through the insulating structure.

16. The device of claim **15**, wherein the insulating structure comprises first insulating patterns and second insulating patterns that are alternately stacked, and

wherein the first insulating patterns comprise a material having an etch selectivity with respect to the second insulating patterns.

17. The device of claim **16**, wherein ones of the first insulating patterns have widths greater than widths of ones of the second insulating patterns.

18. The device of claim **16**, wherein sides of ones of the first insulating patterns are co-planar with sides of ones of the cell gate conductive patterns.

19.-**25**. (canceled)

26. A semiconductor device comprising:

a substrate;

a bit line on the substrate, the bit line extending in a first direction;

first and second semiconductor patterns between the substrate and the bit line, the first and second semiconductor patterns being spaced apart from each other in the first direction by a gap therebetween and lower surfaces of the first and second semiconductor patterns being coplanar;

first and second gate structures between an upper surface of the first semiconductor pattern and the bit line, the first and second gate structures being disposed along the first direction;

a first cell vertical structure extending through the first gate structure and a second cell vertical structure extending through the second gate structure, each of the first and second cell vertical structures comprising a channel layer and both the first and second cell vertical structures extending away from the upper surface of the first semiconductor pattern and being connected to the bit line;

an insulating layer between the substrate and the first and second semiconductor patterns;

a conductive contact pad in the insulating layer; and

a bit line contact structure extending through the gap between the first and second semiconductor patterns and extending away from an upper surface of the substrate, an upper portion of the bit line contact structure contacting the bit line and a lower portion of the bit line contact structure contacting the conductive contact pad.

27. The device of claim **26**, wherein the bit line overlies at least a portion of the gap between the first and second semiconductor patterns.

28. The device of claim **27**, wherein the bit line overlies top surfaces of the first cell vertical structure, the second cell vertical structure and the bit line contact structure.

29. The device of claim **26**, wherein each of the first and second gate structures comprises a plurality of stacked gate electrodes, and an upper most gate electrode of the plurality of stacked gate electrodes is at a first height from the upper surface of the substrate, and

wherein the bit line contact structure comprises a portion having an unitary structure that extends from the first height to the conductive contact pad.

30. The device of claim **26** further comprising:

a third gate structure between an upper surface of the second semiconductor pattern and the bit line; and

a third cell vertical structure extending through the third gate structure and extending away from the upper sur-

face of the second semiconductor pattern, the third cell vertical structure comprising a channel layer and being connected to the bit line.

31. The device of claim **30**, wherein the bit line crosses over the gap between the first and second semiconductor patterns.

32. The device of claim **31**, wherein the bit line overlies top surfaces of the second cell vertical structure, the third cell vertical structure and the bit line contact structure.

33. The device of claim **26**, wherein the first and second semiconductor patterns comprise portions of a same semiconductor pattern, and the gap comprises a portion of an opening in the semiconductor pattern,

wherein the opening has a line shape extending in a second direction when viewed from a plan perspective, and

wherein the bit line contact structure comprises one of a plurality bit line contact structures, and ones of the plurality bit line contact structures are disposed along the second direction and extend through the opening.

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