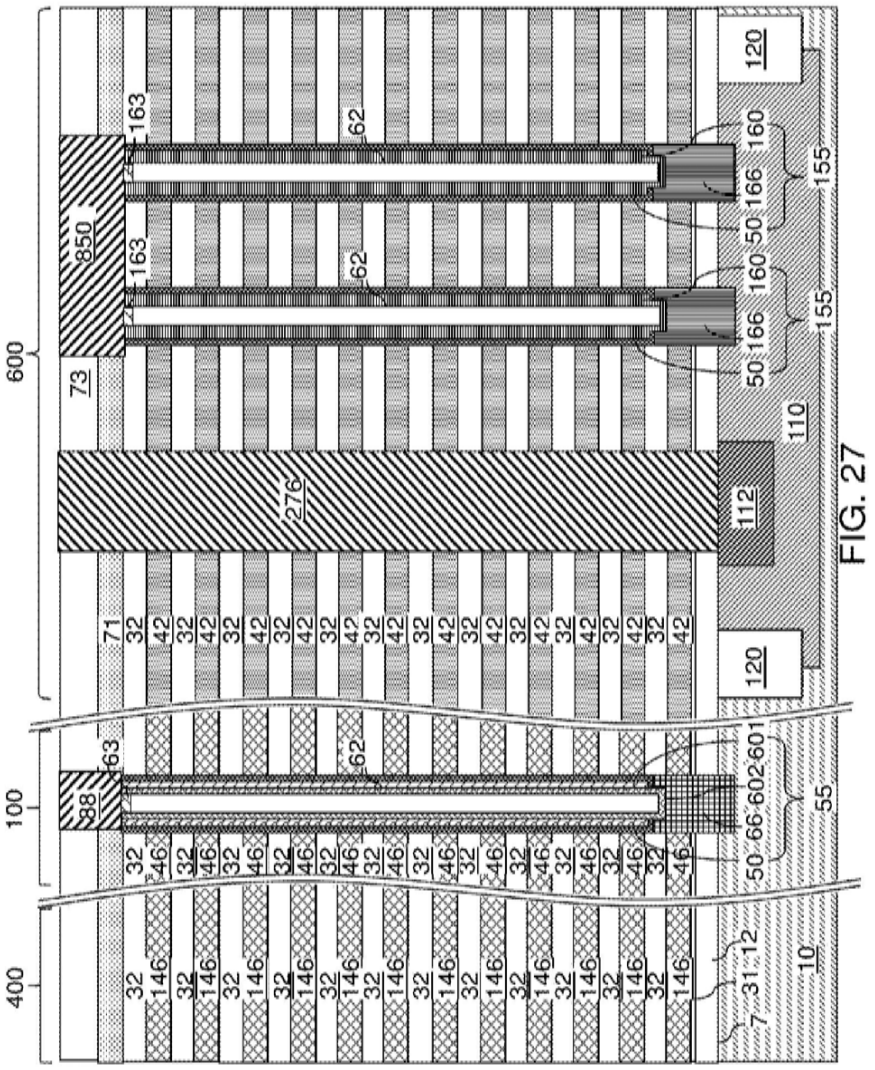

600
100
400
850
73
163
62
276
71
32
42
46
146
120
160
166
50
155
110
112
601
602
66
55
31
12
7
10

FIG. 27

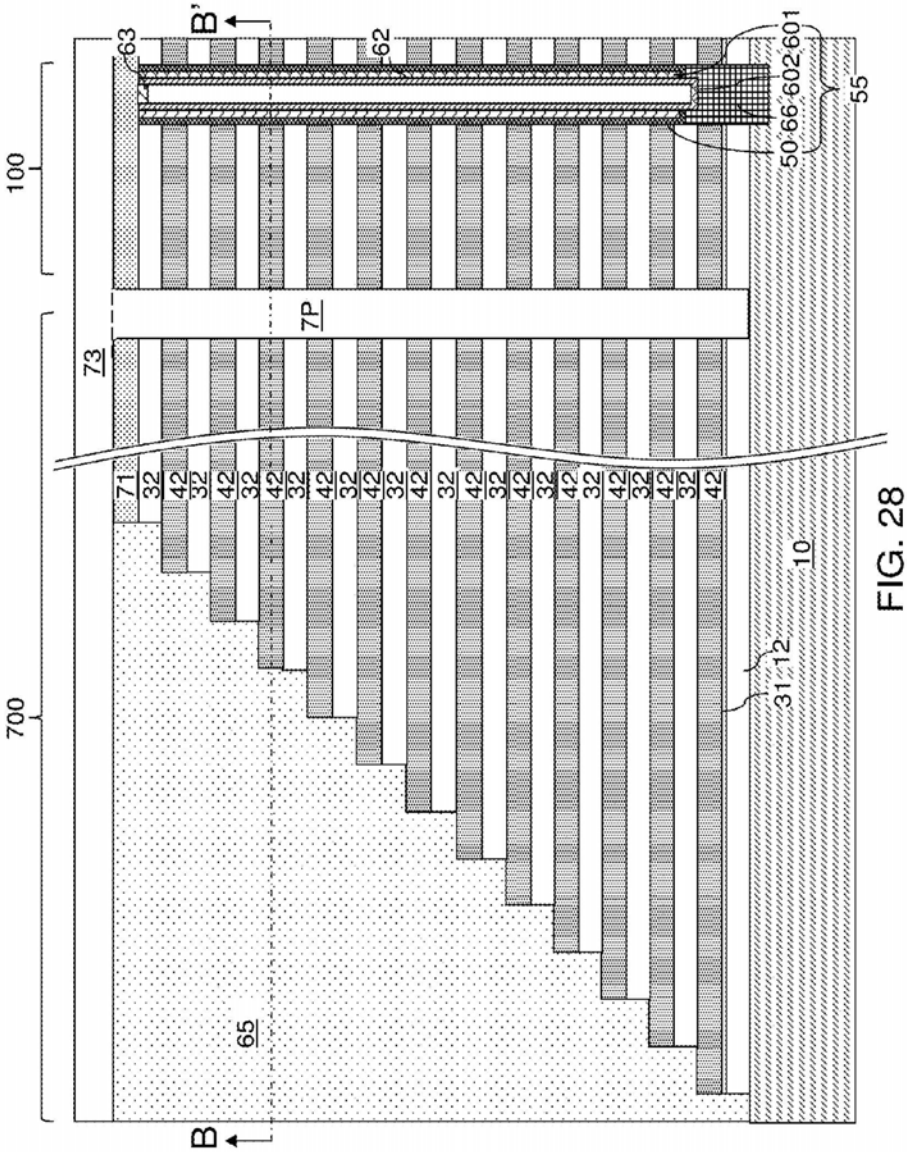


FIG. 28

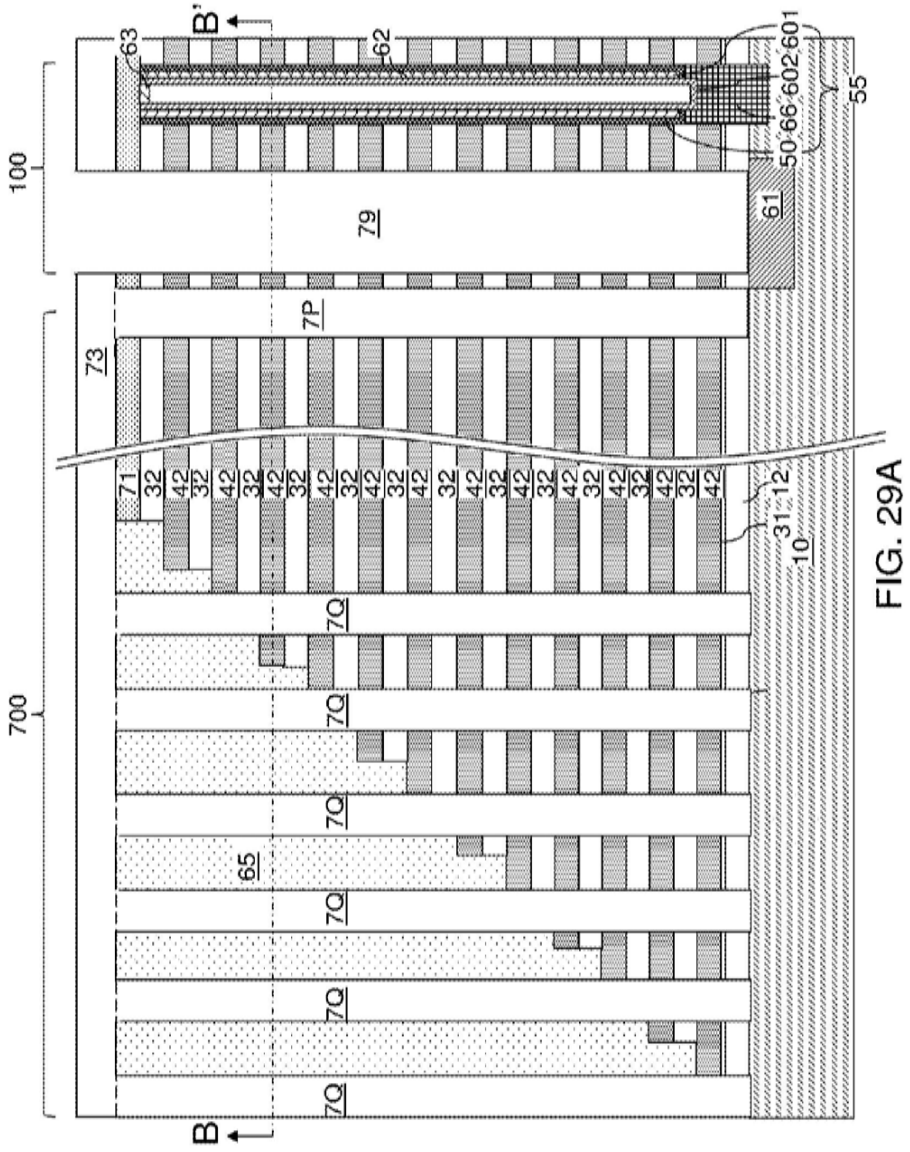


FIG. 29A

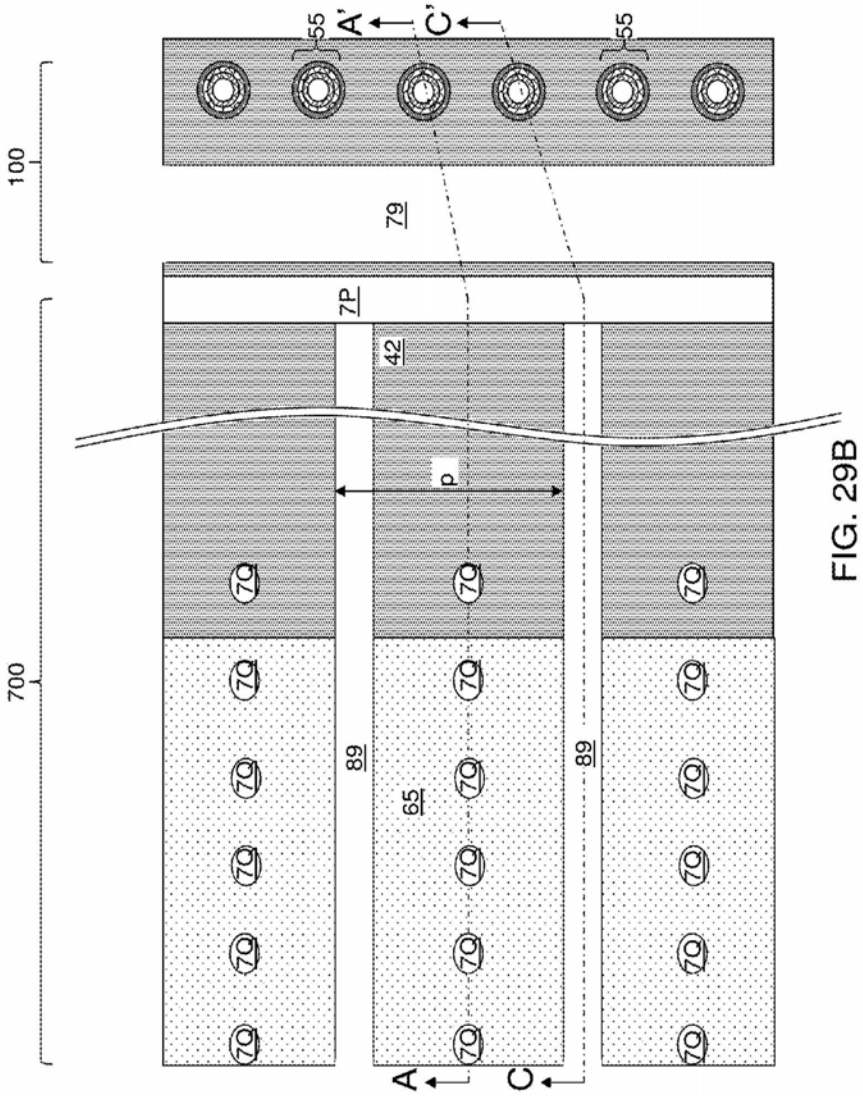


FIG. 29B

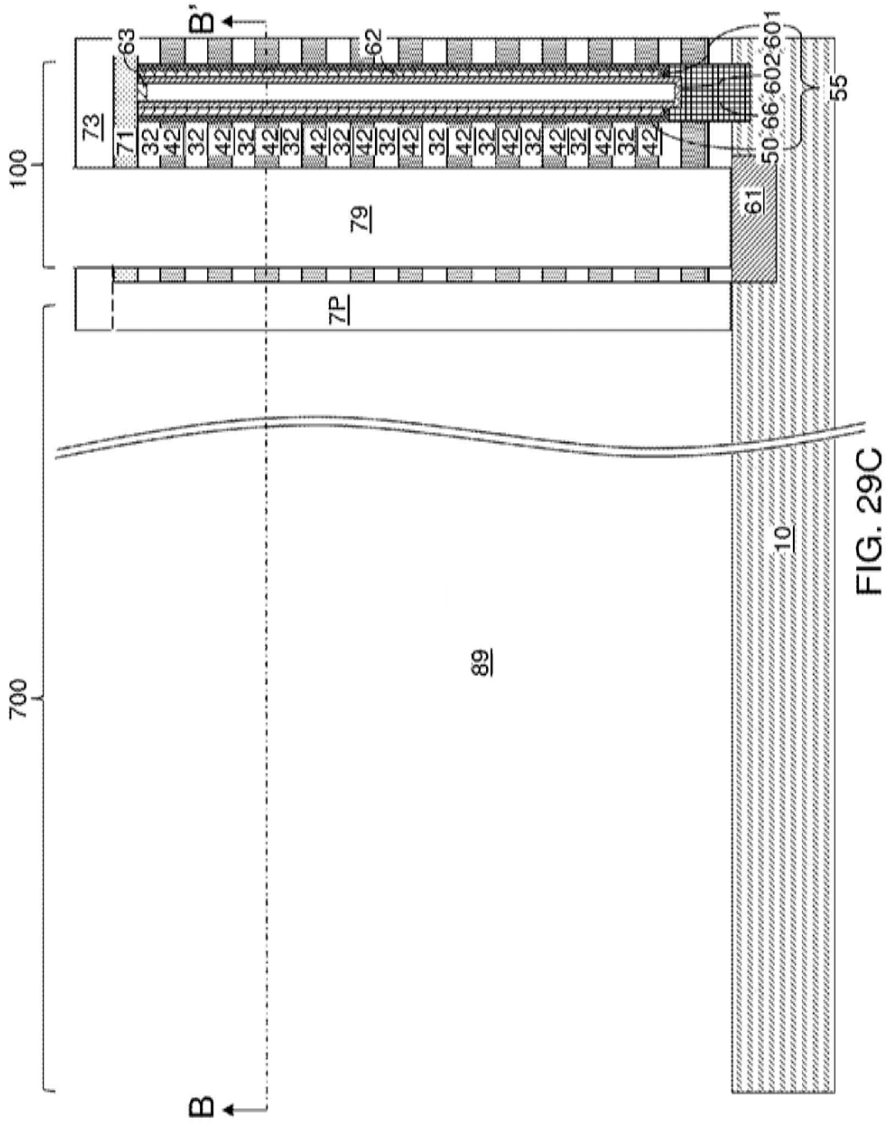


FIG. 29C

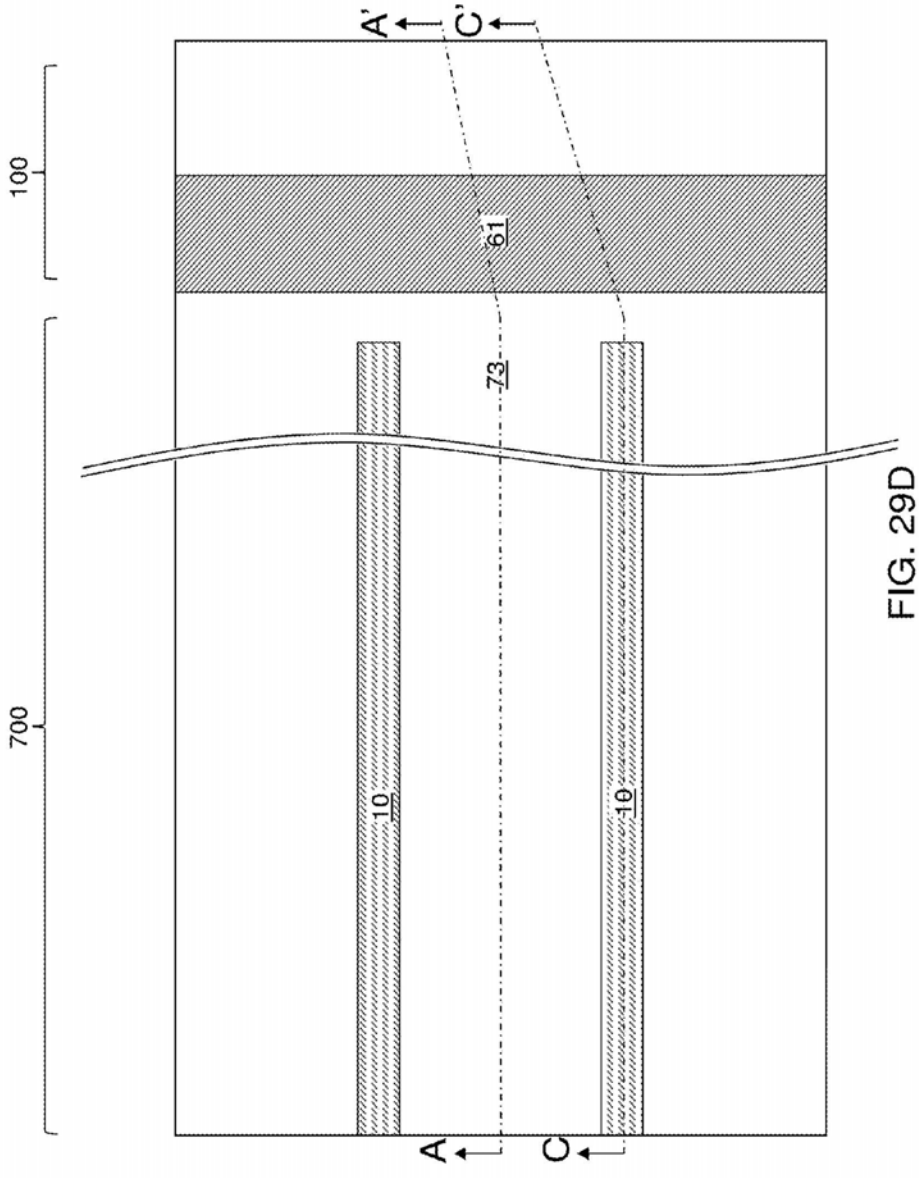


FIG. 29D

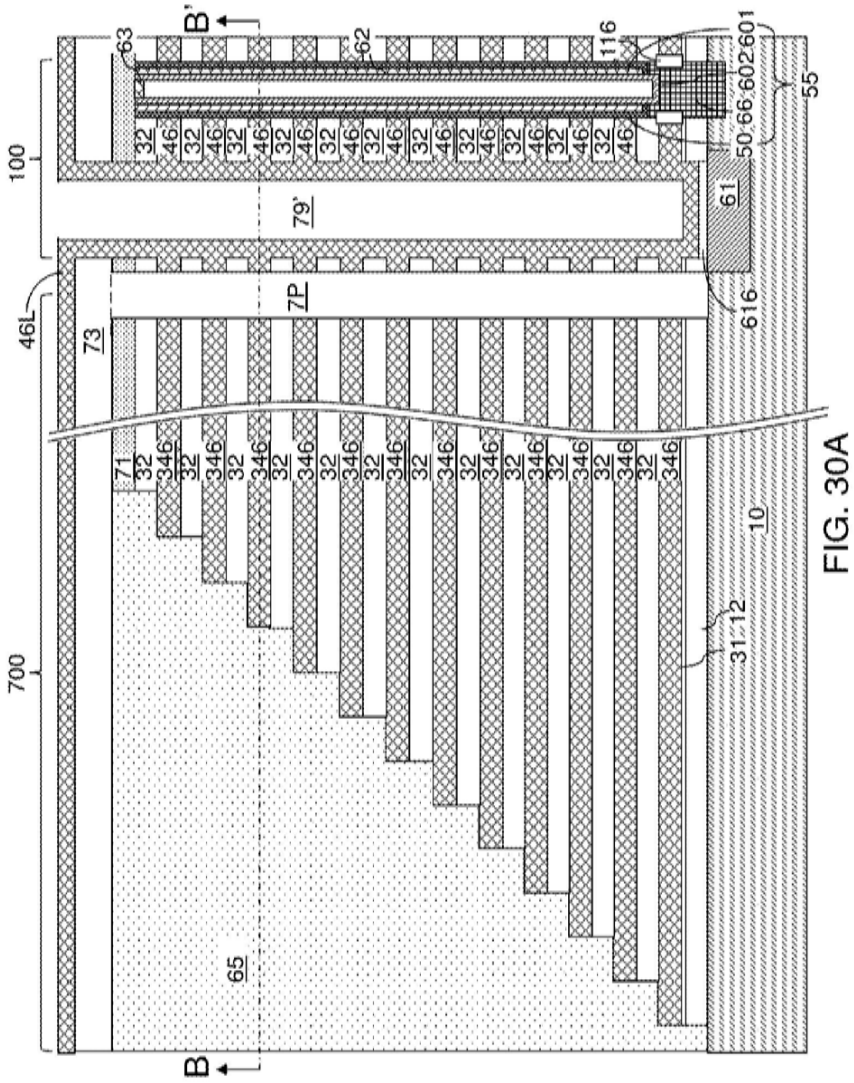

B'
B
63
62
116
601
602
66
50
55
100
700
46L
73
79'
7P
61
616
71
32
346
46
10
31
12
65

FIG. 30A

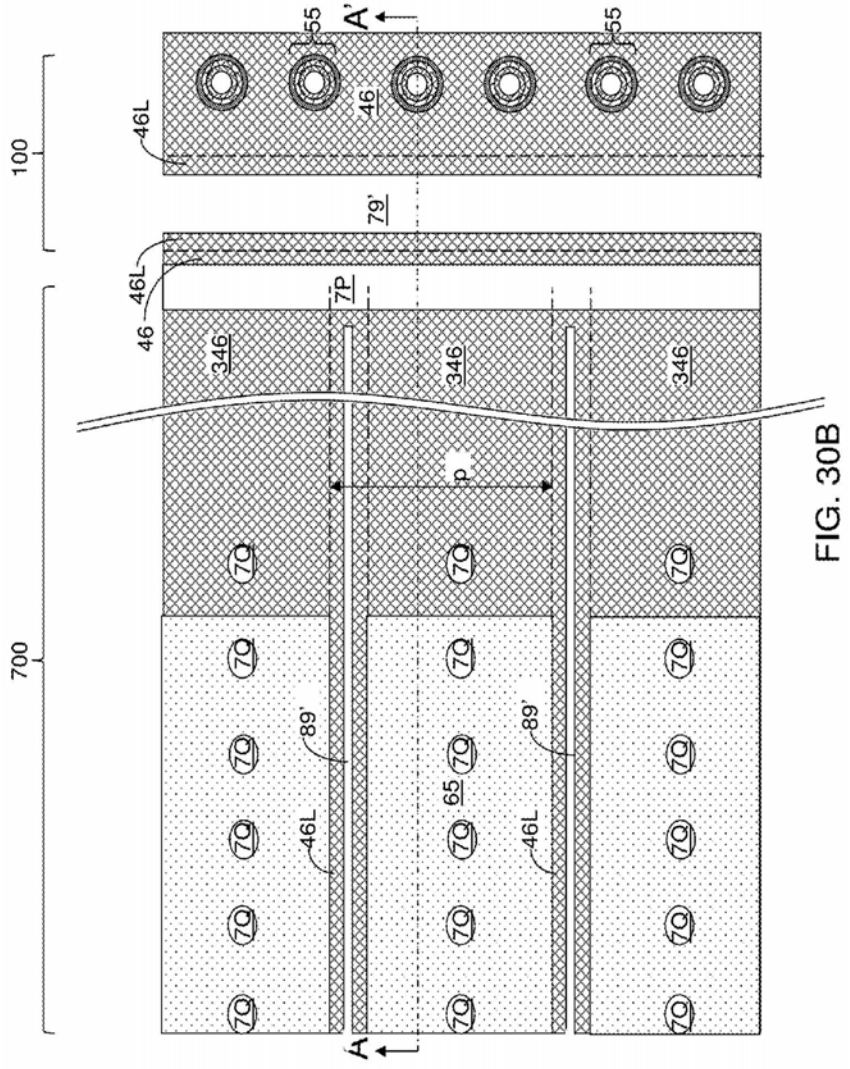

A'
55
55
46L
46
100
79'
46L
7P
46
346
346
346
P
70
89'
89'
65
46L
46L
700
A

FIG. 30B

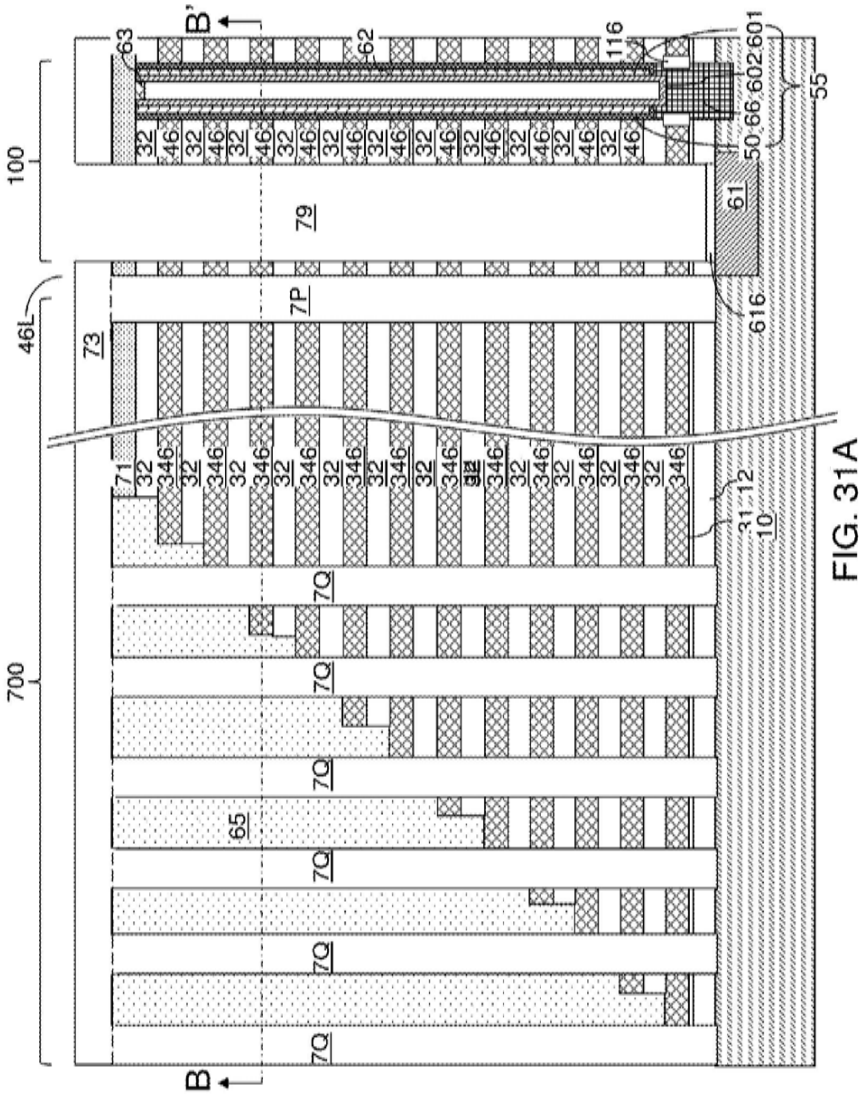

B'
B
63
62
116
601
602
66
50
55
100
79
61
7P
616
46L
73
71
32
346
46
31
12
10
700
7Q
65

FIG. 31A

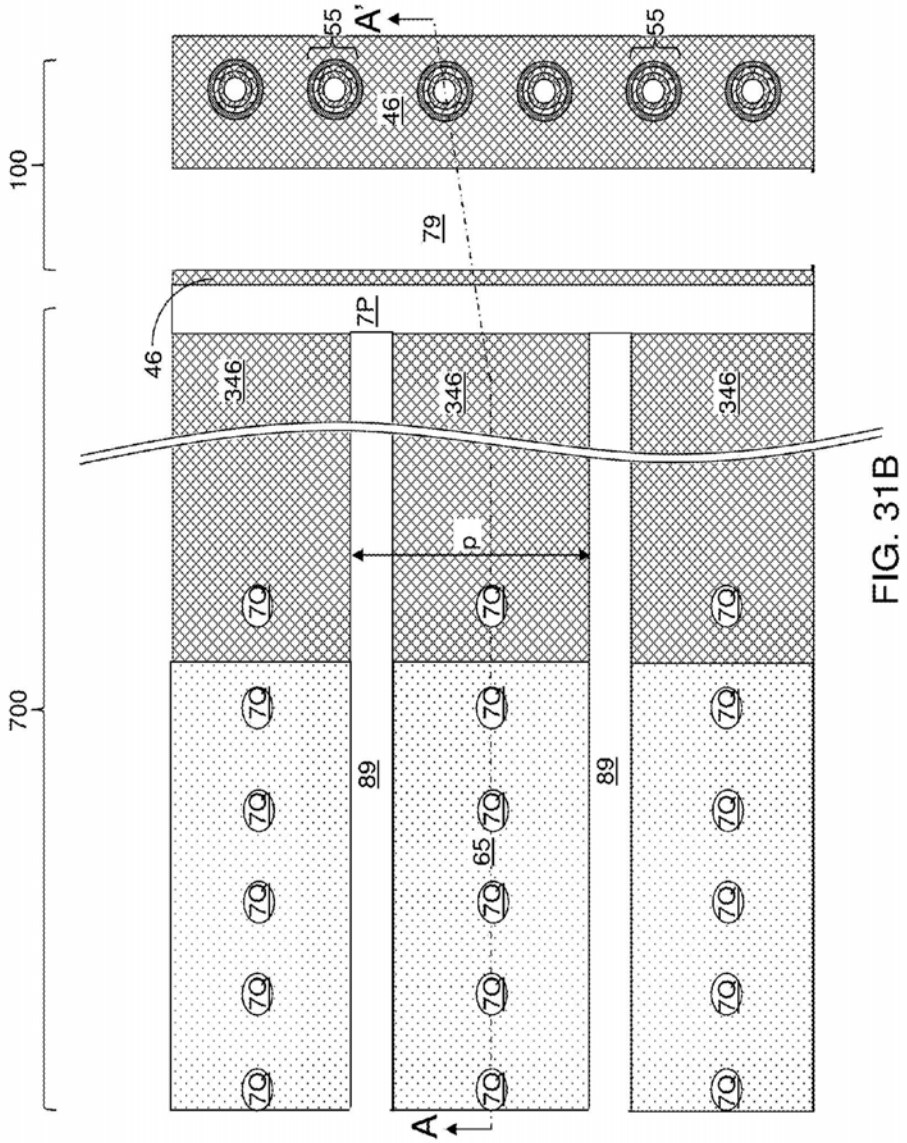


FIG. 31B

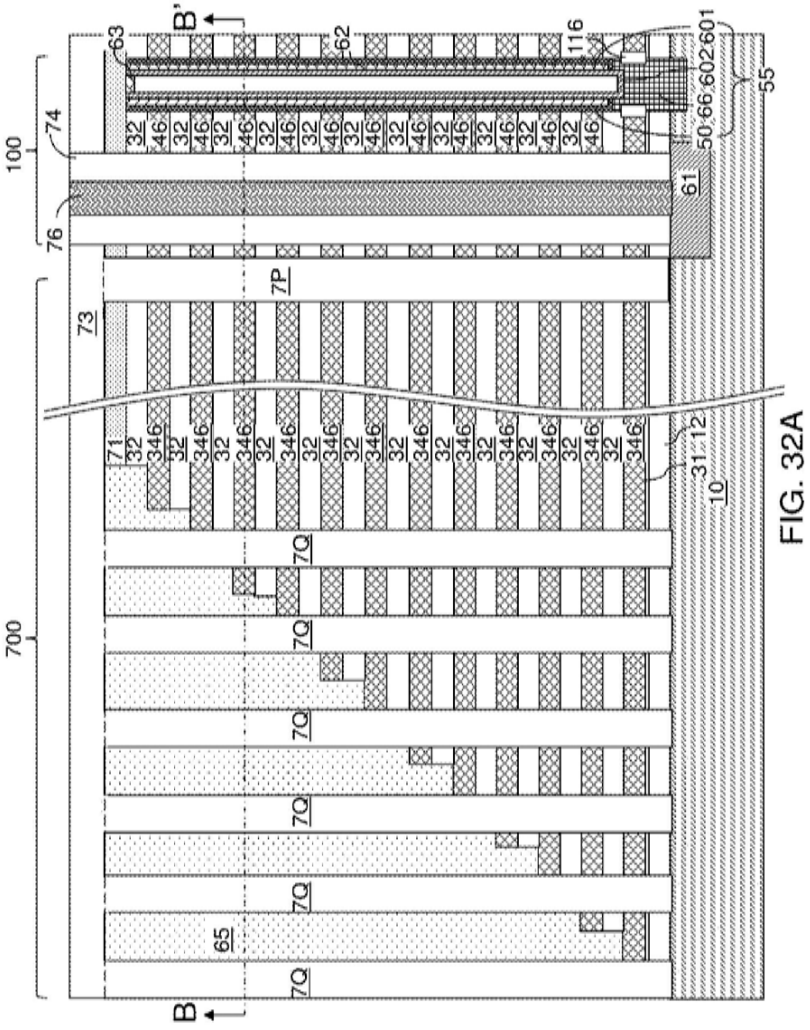

B'
B
63
62
116
601
602
66
50
55
74
100
76
61
7P
73
71
32
346
46
31
12
10
7Q
65
700

FIG. 32A

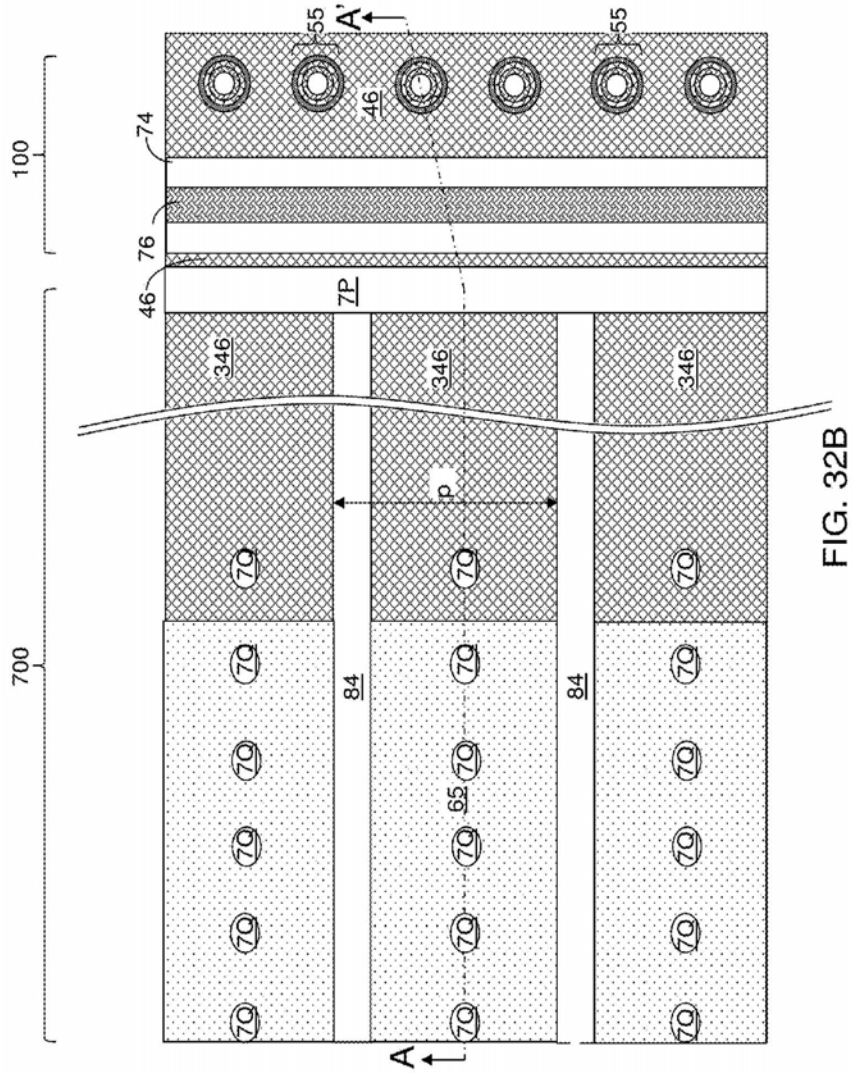


FIG. 32B

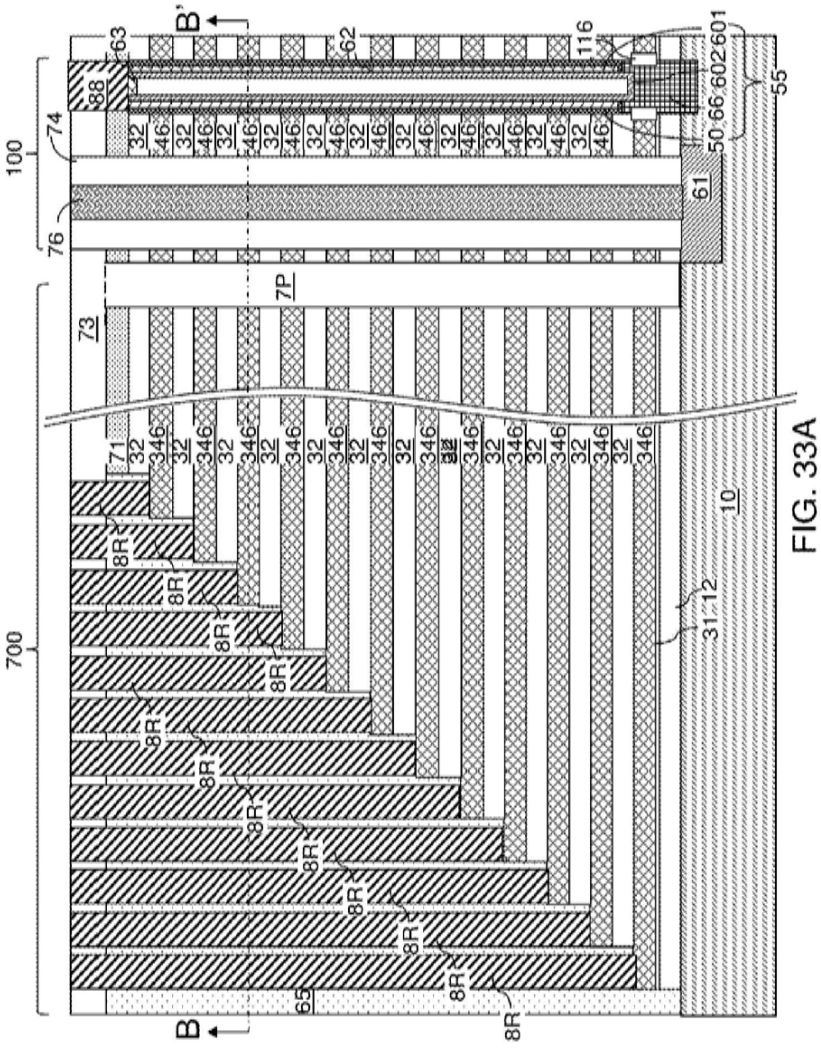

B'
B
100
700
74
76
73
7P
71
63
62
116
601
602
66
50
55
61
10
12
31
65
88
32
46
346
8R

FIG. 33A

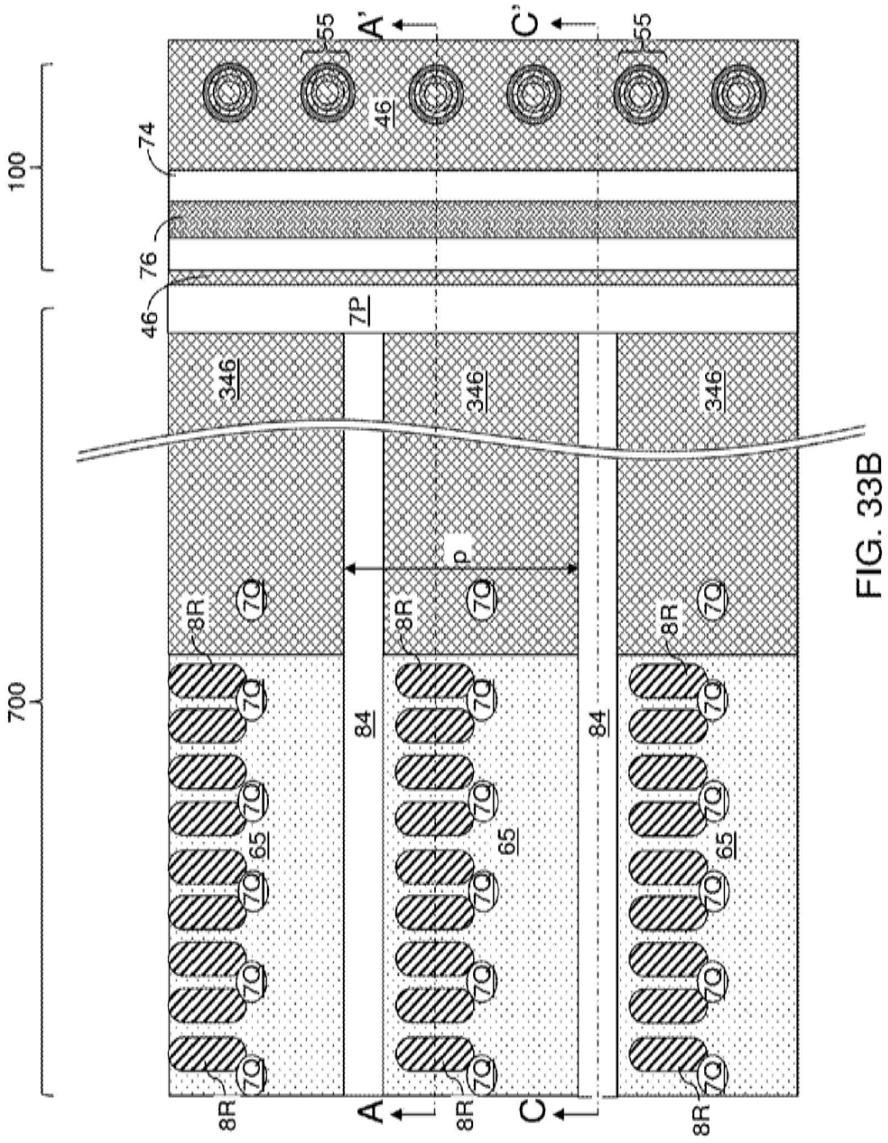


FIG. 33B

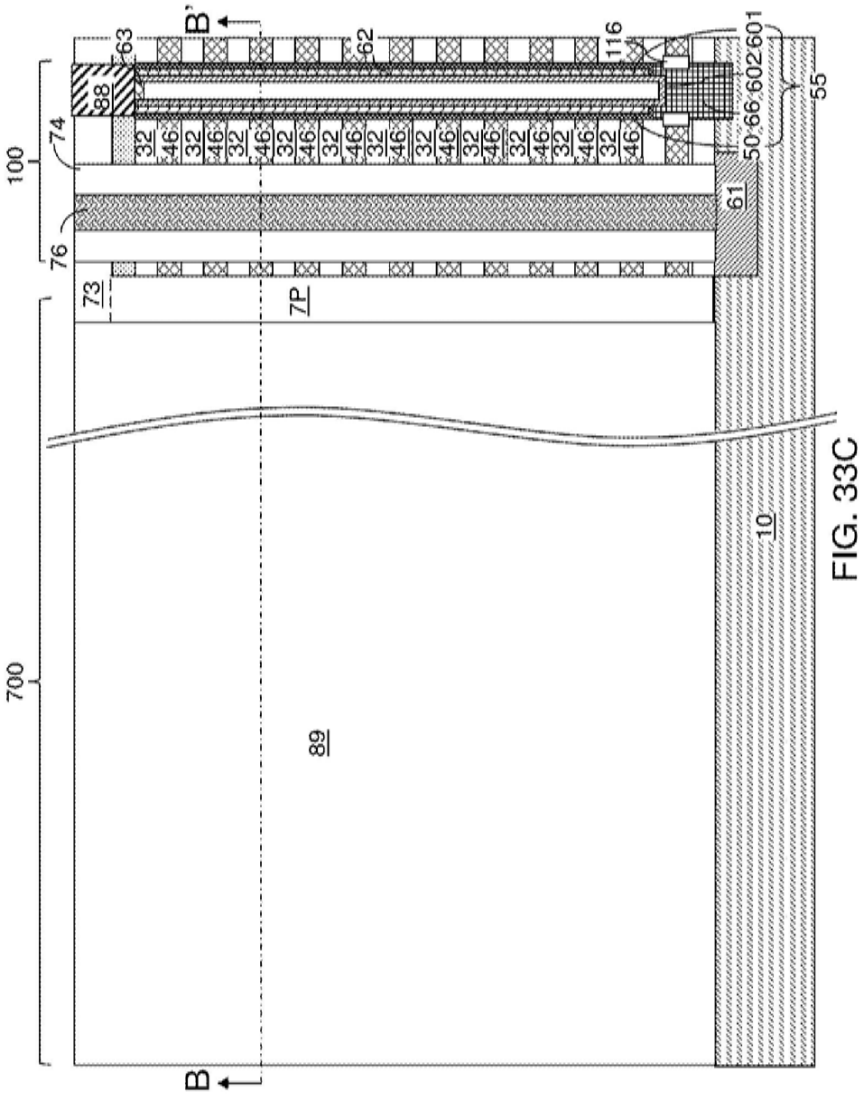


FIG. 33C

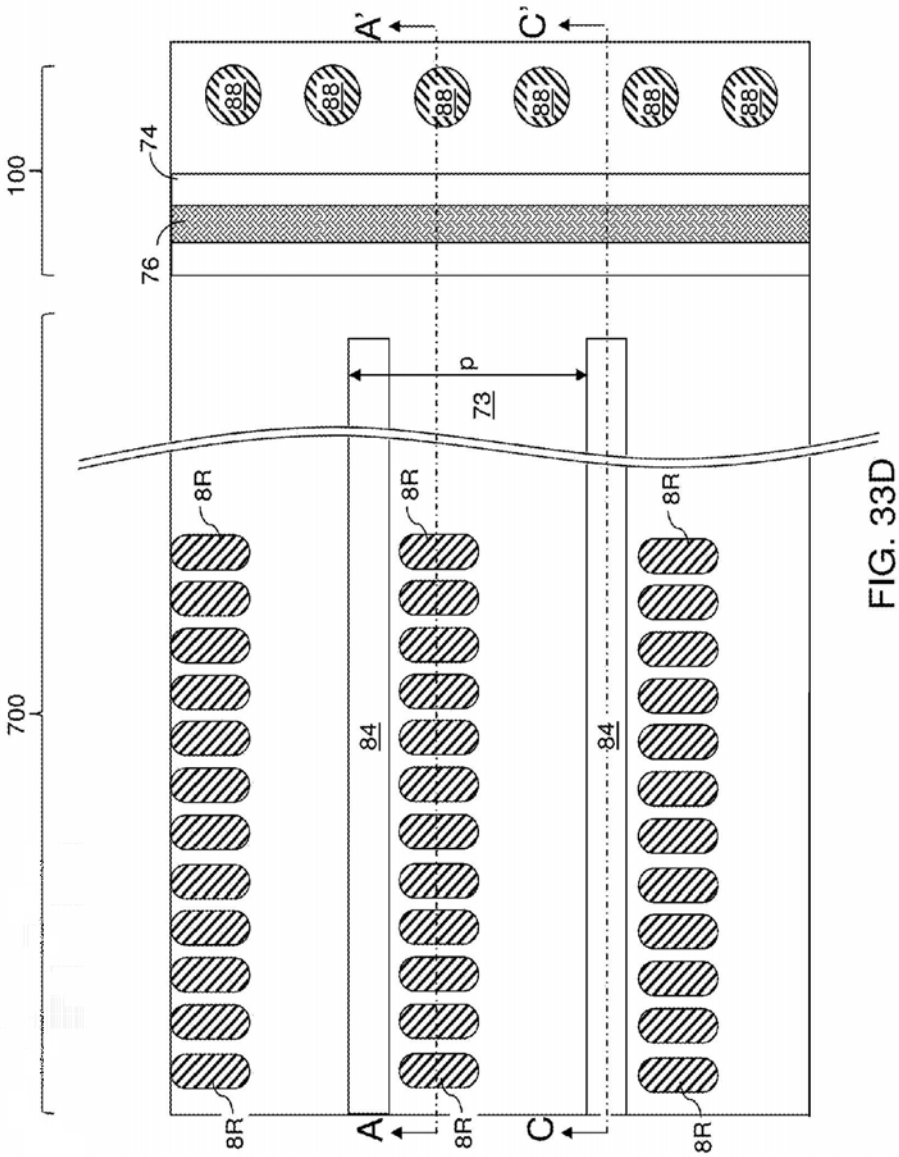


FIG. 33D

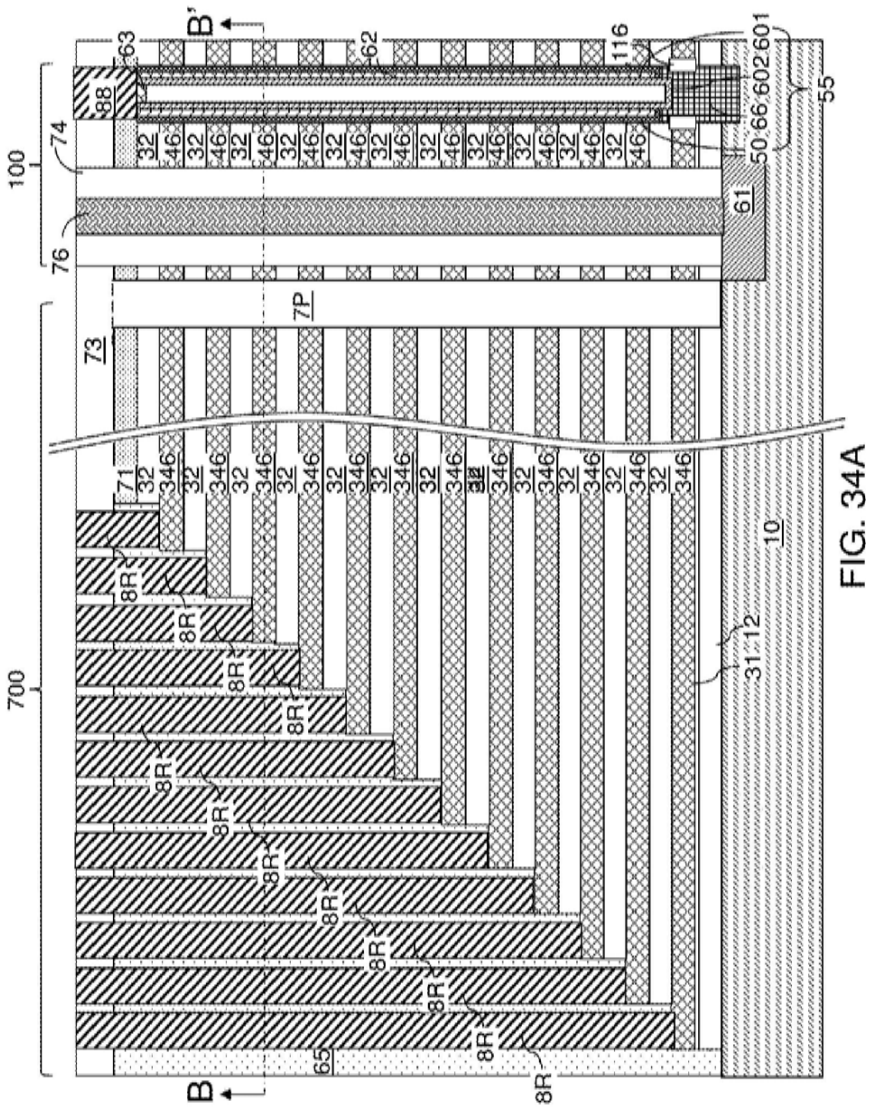

B'
B
63
62
116
601
602
66
50
55
88
74
100
76
61
7P
73
71
32
346
46
8R
700
10
12
31
65

FIG. 34A

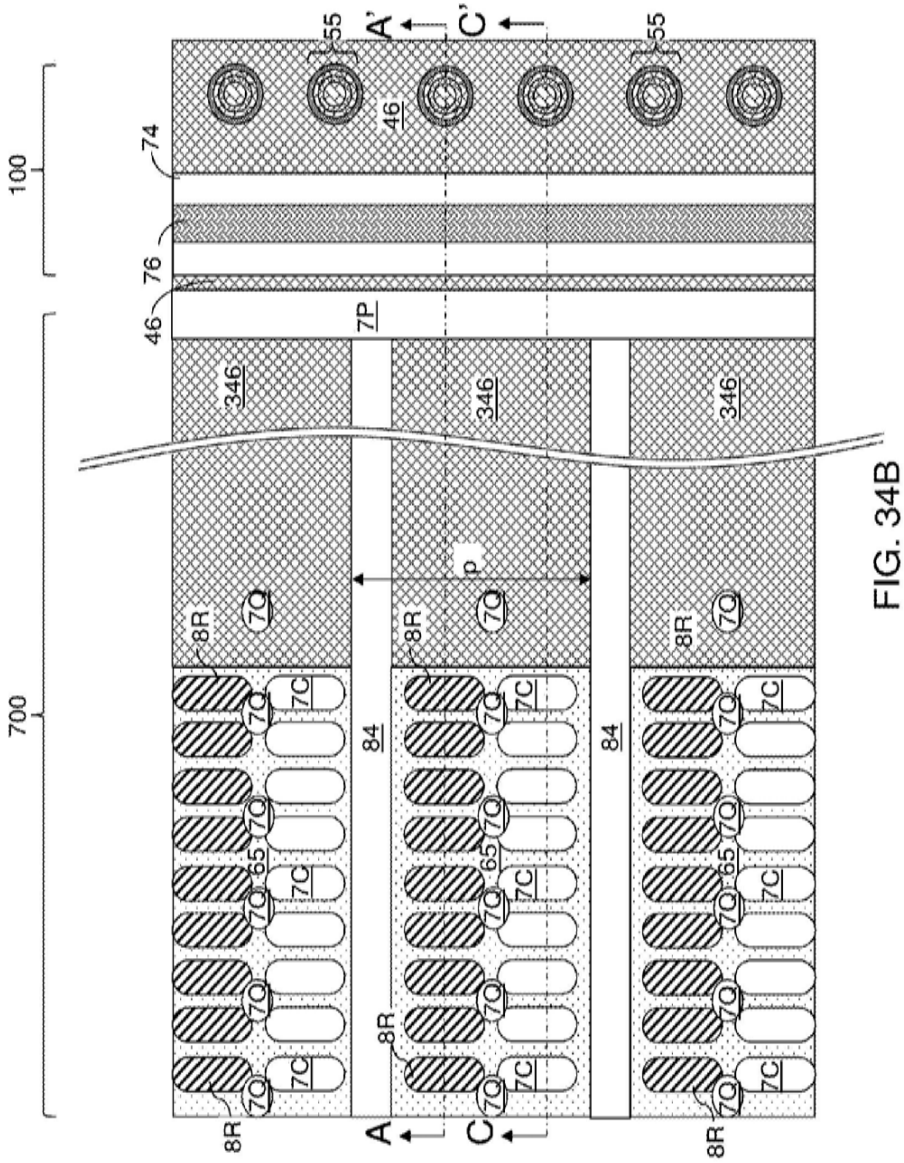

A'
C'
55
55
46
74
100
76
46
7P
346
346
346
P
8R
7Q
7C
84
84
65
700
A
C
8R
8R

FIG. 34B

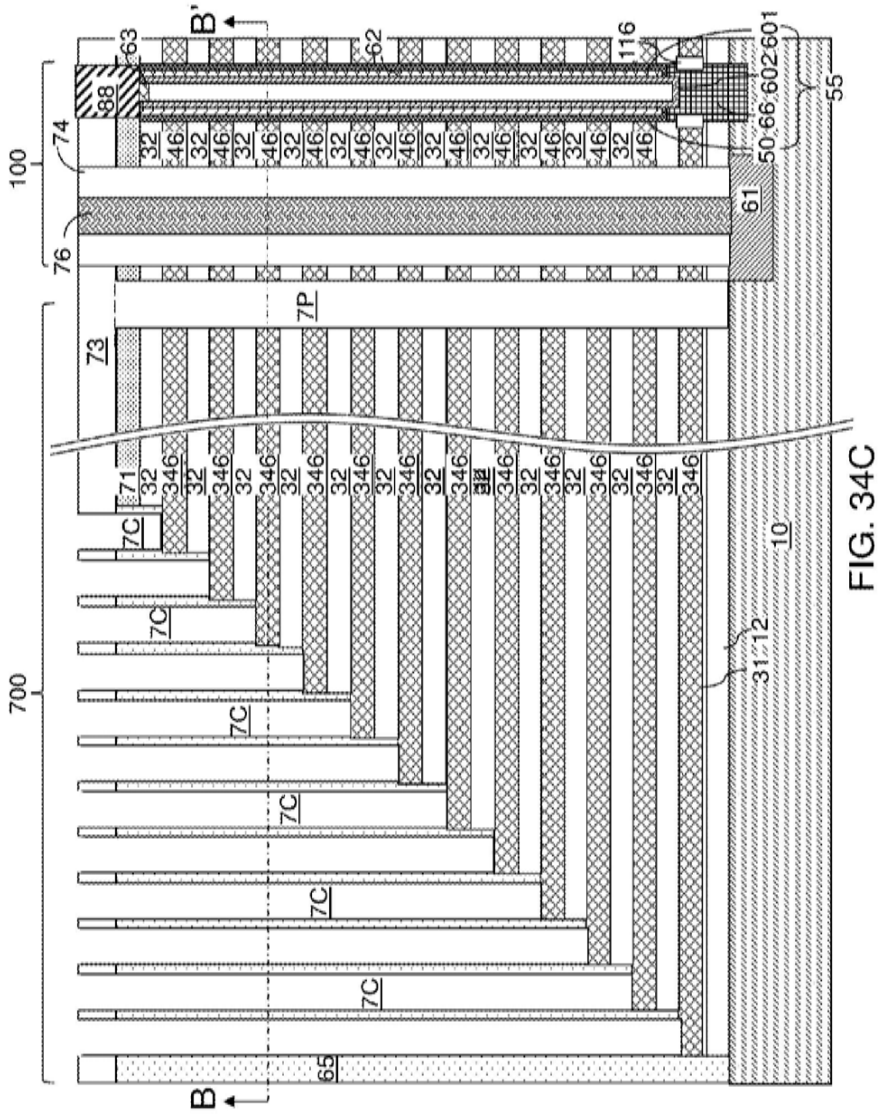

B'
B
63
62
116
601
602
66
50
55
74
100
76
61
7P
73
71
32
346
7C
10
31/12
700
65

FIG. 34C

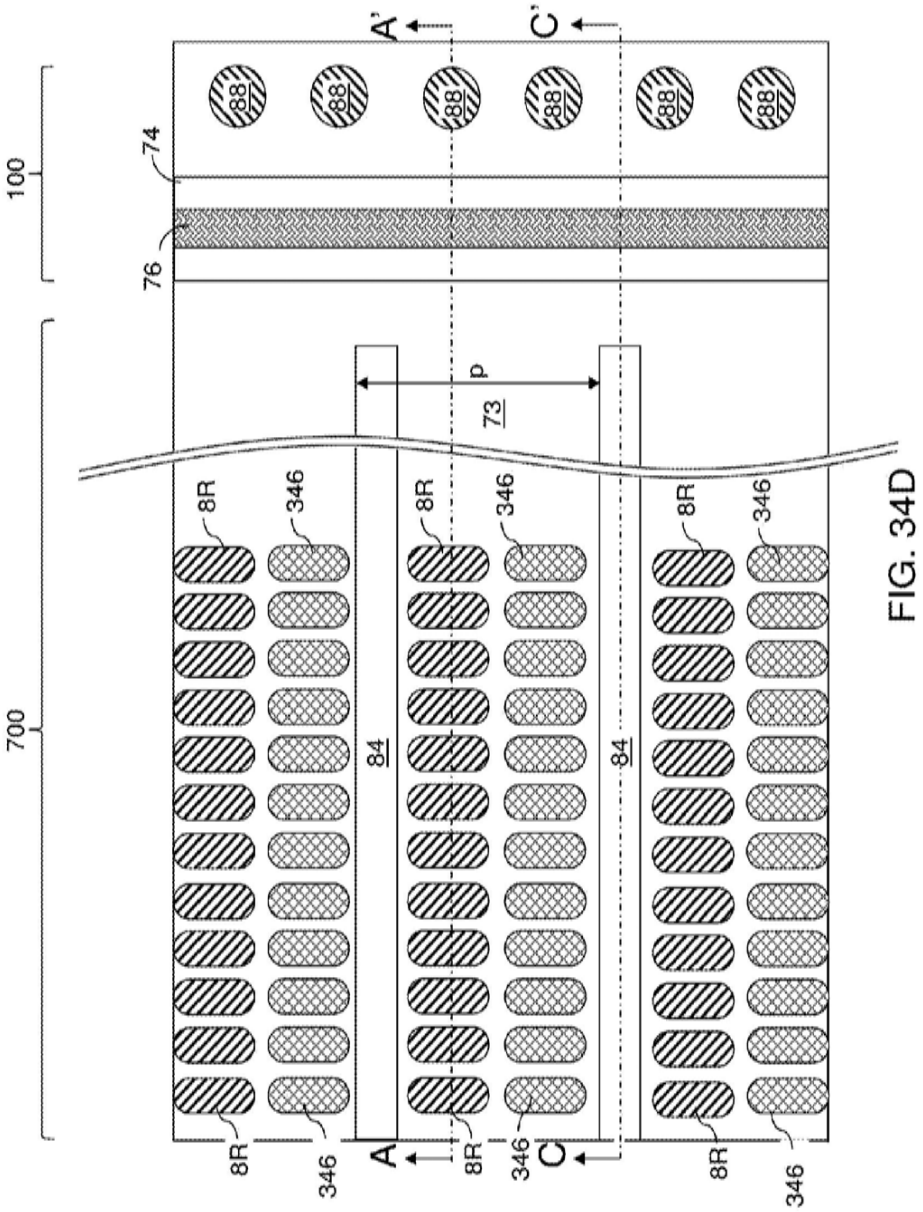


FIG. 34D

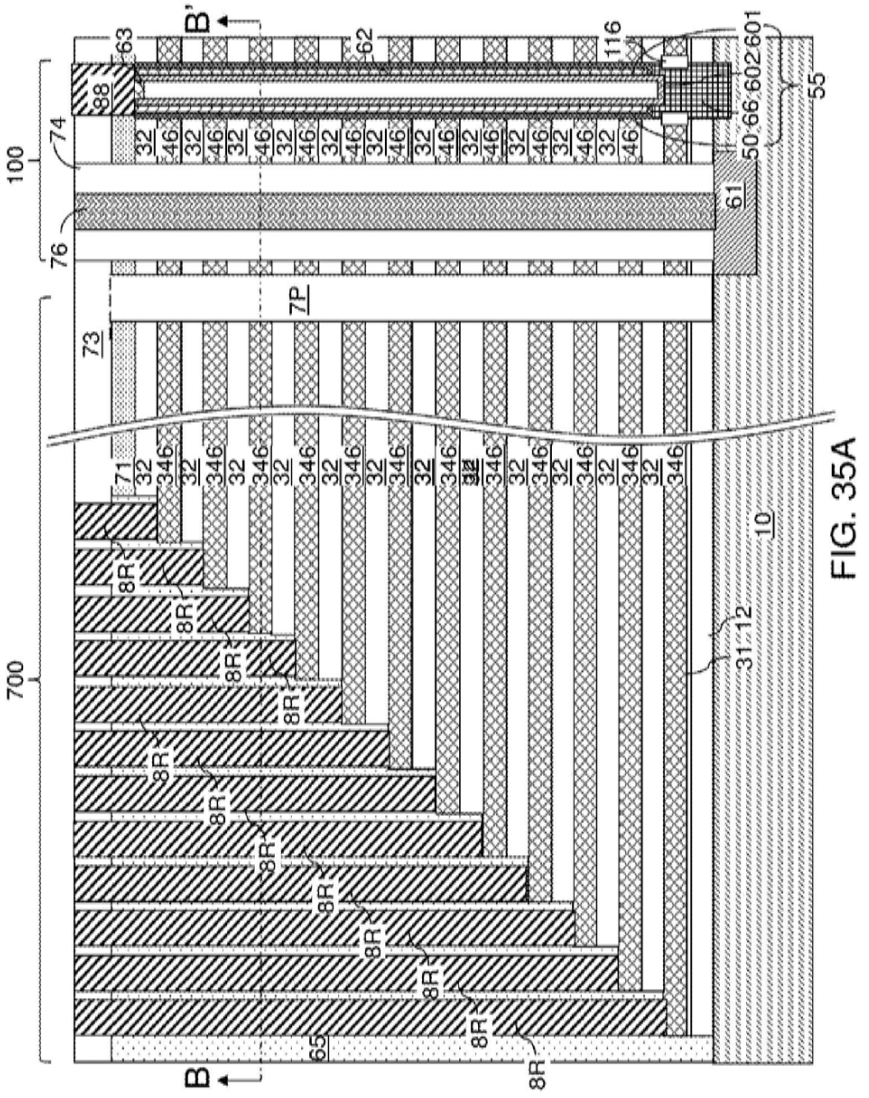

B'
B
63
62
116
601
602
66
50
55
88
74
100
76
61
7P
73
71
32
346
46
8R
10
31
12
700
65

FIG. 35A

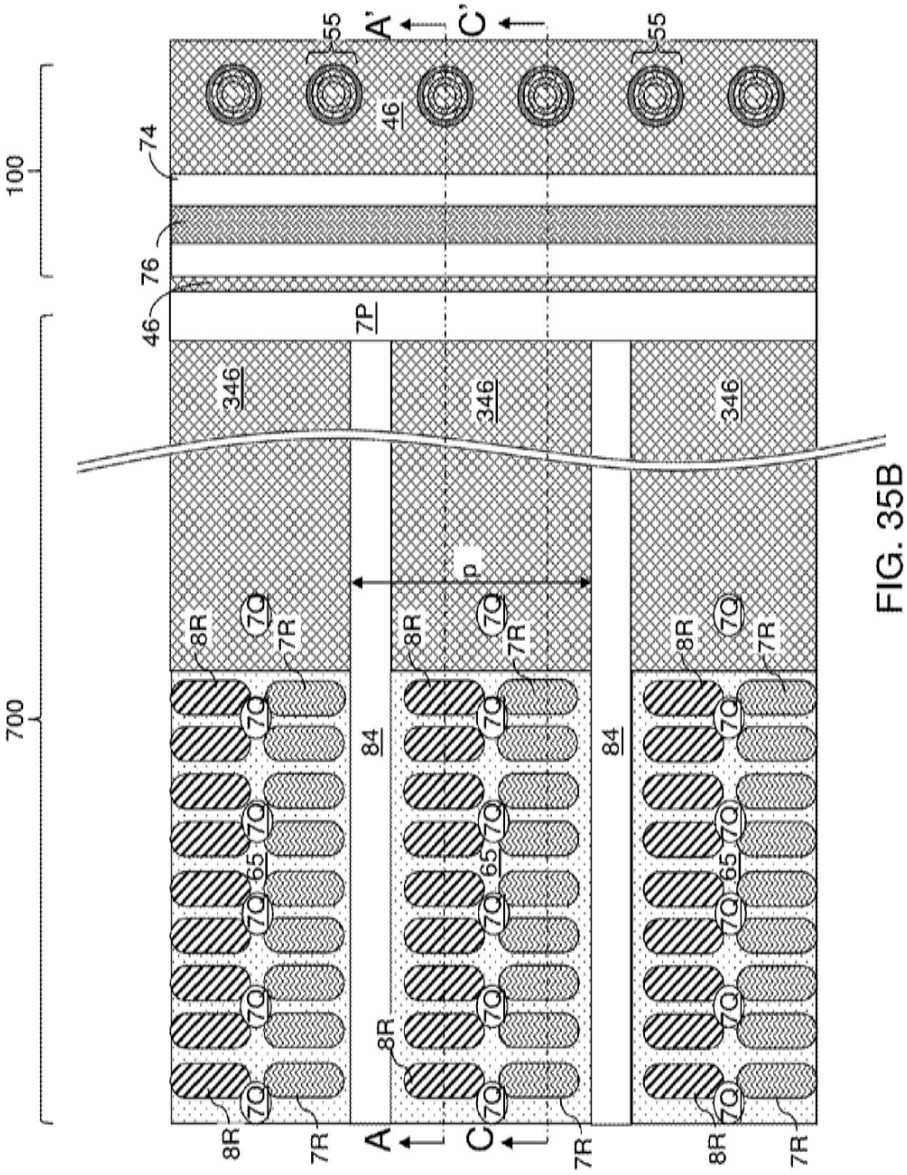


FIG. 35B

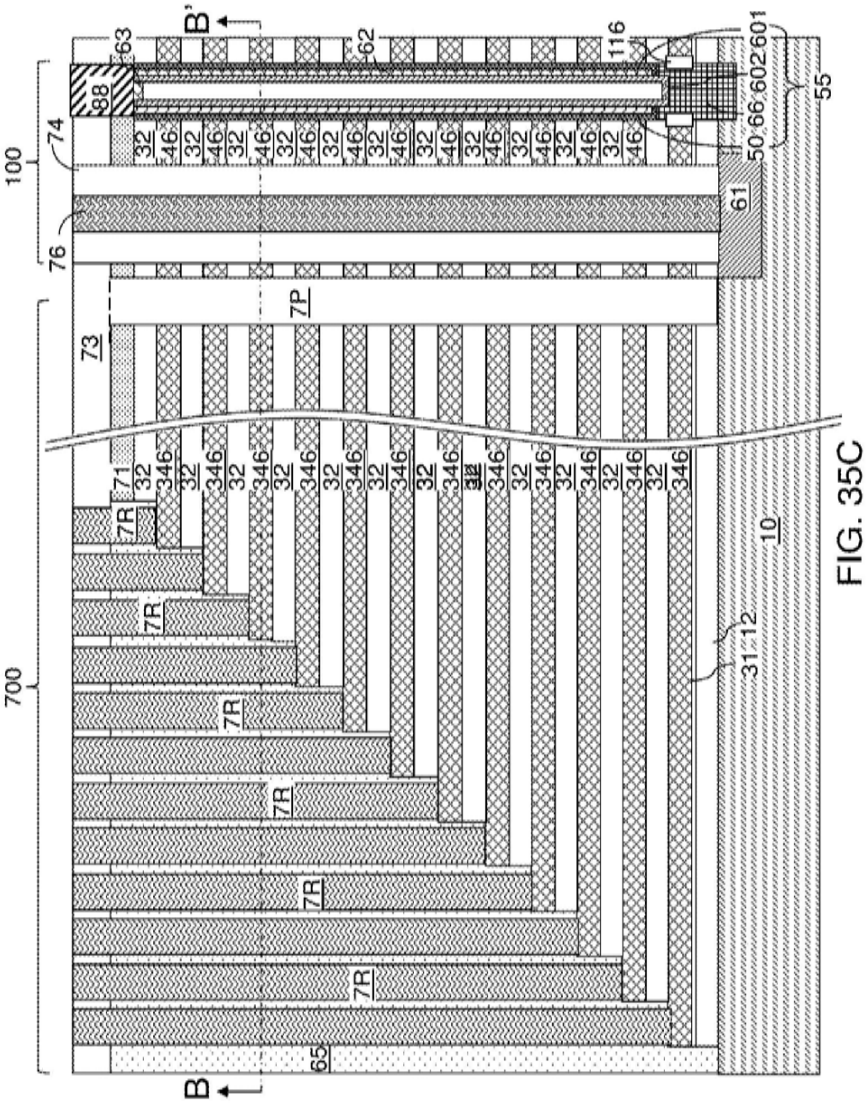

B'
B
63
62
116
601
602
66
50
55
88
74
100
76
61
7P
73
71
32
346
46
7R
10
31
12
700
65

FIG. 35C

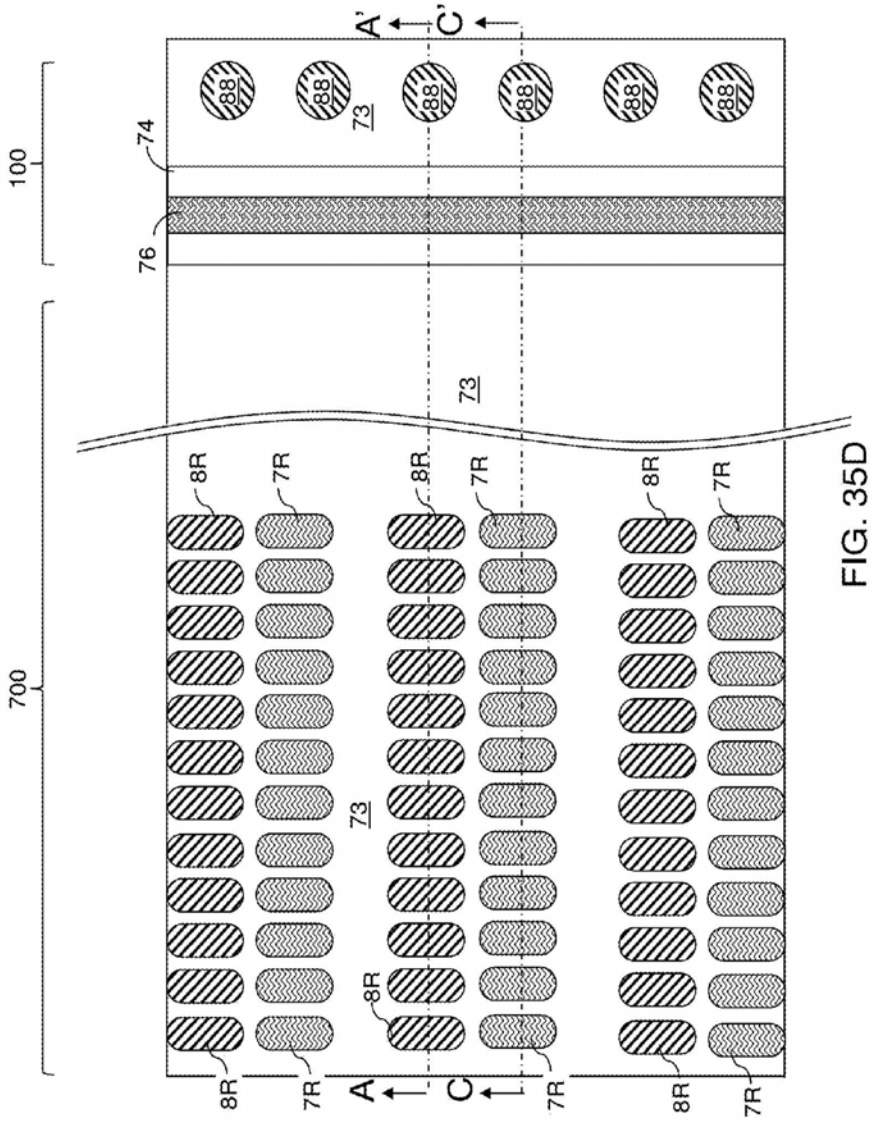


FIG. 35D

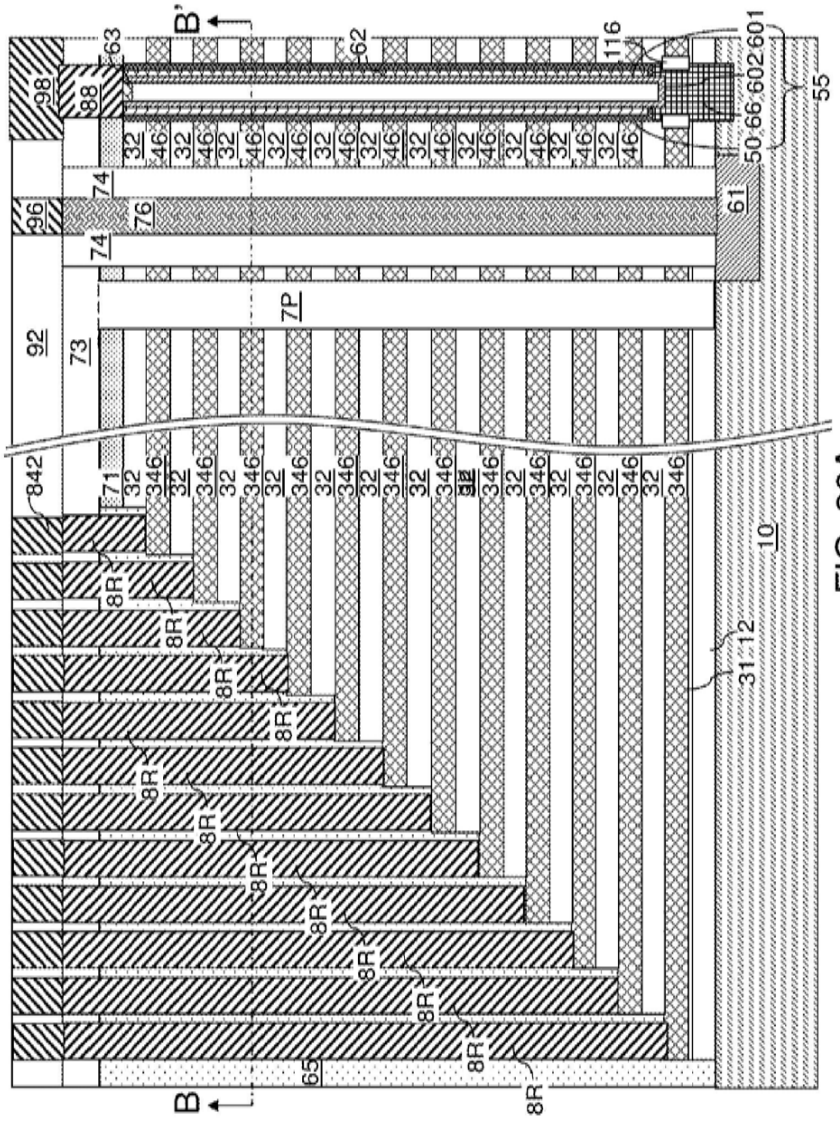

B'
B
63
62
116
601
602
66
50
55
98
88
32
46
74
96
76
61
92
73
7P
842
71
346
8R
65
31
12
10

FIG. 36A

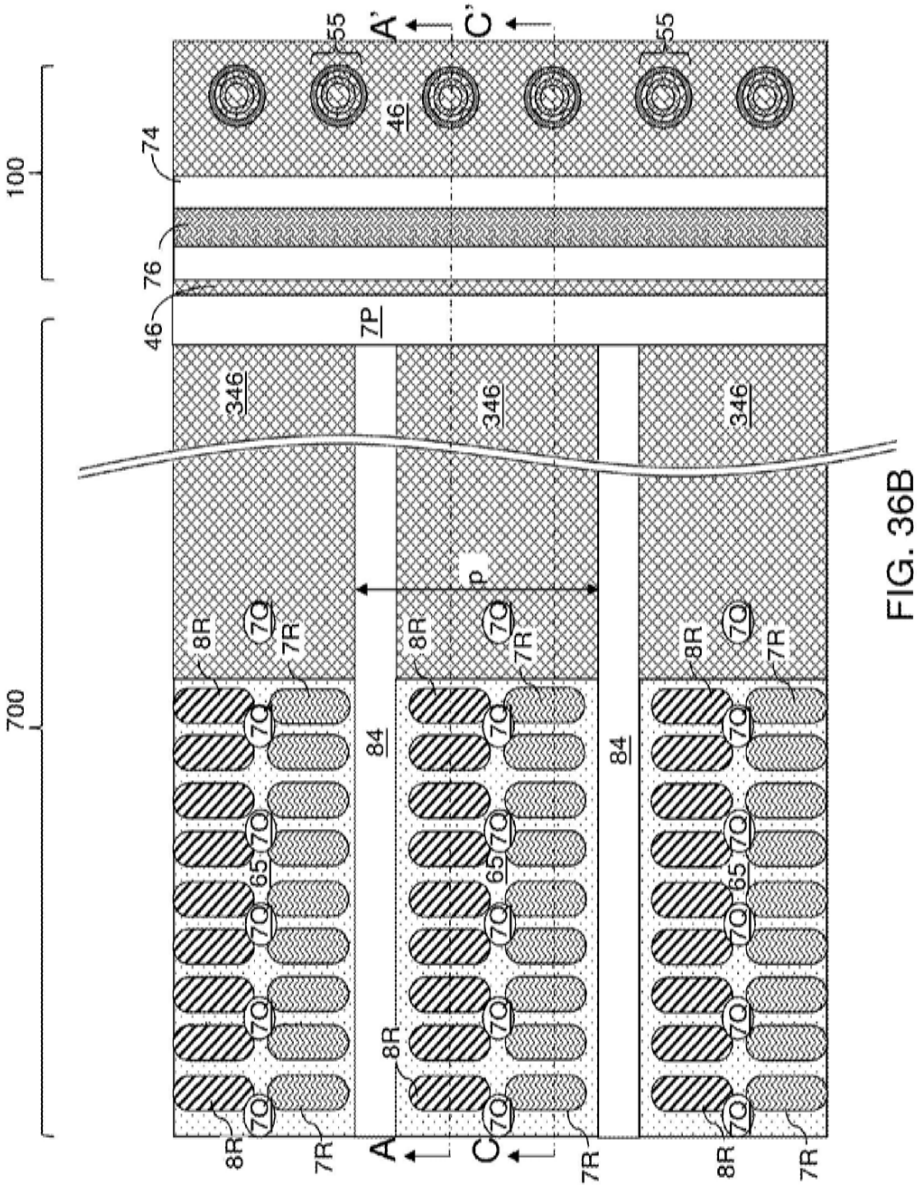


FIG. 36B

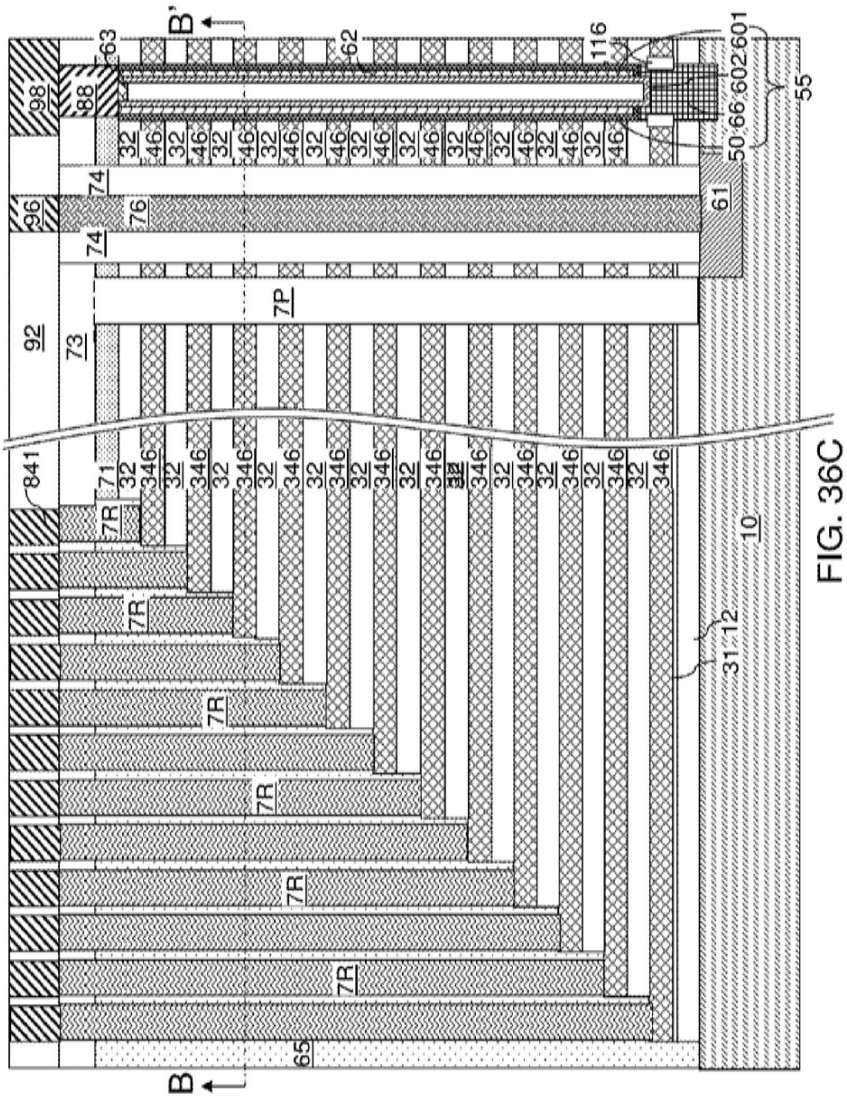

B'
B
63
62
116
601
602
66
50
55
98
88
96
74
76
61
92
73
7P
841
71
32
346
46
7R
10
31
12
65

FIG. 36C

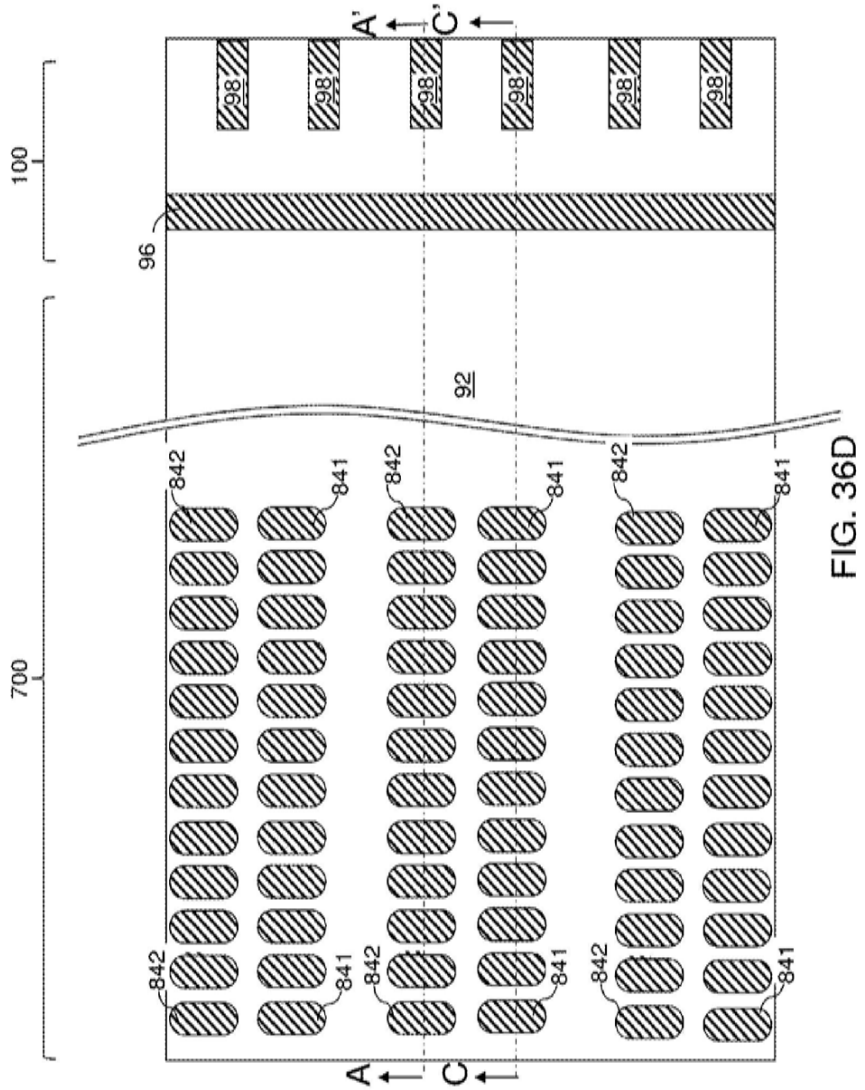


FIG. 36D

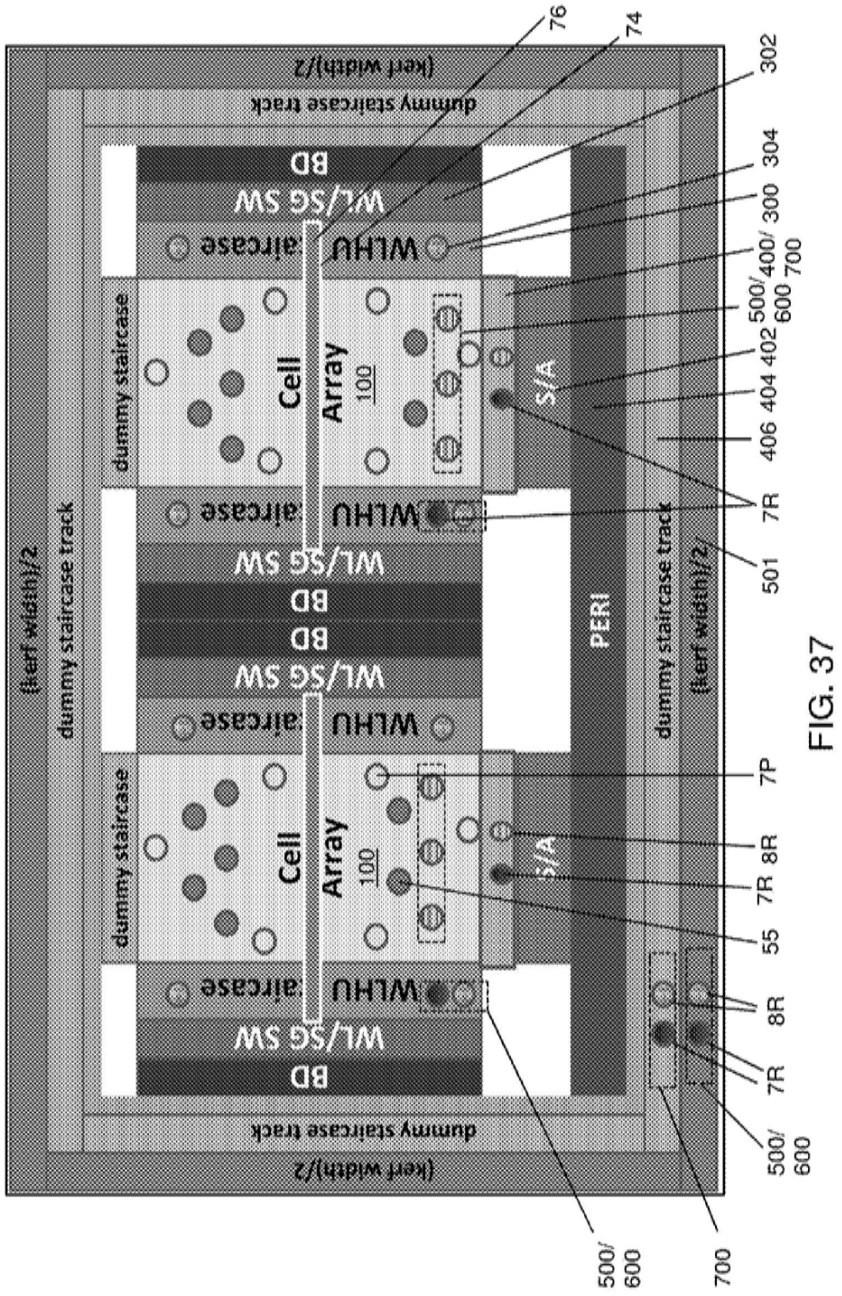

(kerf width)/2
dummy staircase track
dummy staircase track
(kerf width)/2
BD
WL/SG SW
staircase
WLHU
dummy staircase
Cell Array
100
S/A
PERI
76
74
302
304
300
500/ 600
400/ 700
402
404
406
7R
501
7P
8R
55
700

FIG. 37

PASSIVE DEVICES FOR INTEGRATION WITH THREE-DIMENSIONAL MEMORY DEVICES

FIELD

[0001] The present disclosure relates generally to the field of semiconductor devices and specifically to passive devices that are compatible with three-dimensional memory devices and methods of making thereof.

BACKGROUND

[0002] Passive devices refer to devices that provide an output with, or without, a phase change in linear proportion to a sinusoidal electrical input. Passive devices do not have the ability to switch on, or off, the output. Passive devices include, for example, resistors, capacitors, and inductors. Semiconductor circuits routinely employ passive devices in addition to active devices such as transistors.

SUMMARY

[0003] According to an aspect of the present disclosure a three dimensional memory device is provided, comprising a memory device region containing a plurality of non-volatile memory devices, a peripheral device region containing active driver circuit devices, and a first stepped surface region between the peripheral device region and the memory device region containing a plurality of passive driver circuit devices. According to another aspect of the present disclosure, a device comprising a set of capacitors is provided, the device comprising a stack of alternating layers including electrically insulating layers and electrically conductive layers located over a substrate, wherein each underlying electrically conductive layer that is located within the stack and has at least one overlying electrically conductive layer that laterally extends farther than the underlying electrically conductive layer to form a stepped surface region on a side of the stack, and a dielectric material portion located over the stepped surface region of the stack, wherein an interface between the dielectric material portion and the stack includes a contiguous set of horizontal surfaces and vertical surfaces to provide the stepped surface region. The device further comprises a set of dielectric fill material portions located within trenches that vertically extend through the stack of alternating layers and laterally contact sidewalls of the stack of alternating layers in the stepped surface region and a plurality of contact via structures in contact with respective electrically conductive layers within the stack of alternating layers. The electrically conductive layers constitute conductive components of a set of capacitors and a subset of the electrically insulating layers constitutes node dielectrics of the set of capacitors, Each capacitor in the set comprises a first node that includes an underlying electrically conductive layer of a respective vertically neighboring pair and a respective contact via structure that extends upward from the underlying electrically conductive layer and through the dielectric material portion, and a second node that includes an overlying electrically conductive layer of the respective vertically neighboring pair and a respective contact via structure that extends upward from the overlying electrically conductive layer and through the dielectric material portion.

[0004] According to another aspect of the present disclosure a method of forming a memory device comprises forming a plurality of memory devices in a memory device region; forming a plurality of passive devices outside the memory device region, and forming a conductive layer in one deposition step such that a first portion of the conductive layer comprises a portion of at least one of the passive device and a second portion of the conductive layer forms a portion of at least one memory device.

[0005] According to yet another aspect of the present disclosure, a semiconductor device is provided, comprising an alternating stack of first material layers and second material layers located over a substrate, at least one pillar structure extending from a first horizontal plane including a top surface of the alternating stack through at least a portion of the alternating stack, a laterally-extending semiconductor or conductive structure contacting a bottom surface of the at least one pillar structure, and a contact via structure contacting a top surface of the laterally-extending semiconductor or conductive structure and laterally spaced from the at least one pillar structure. Each of the at least one pillar structure comprises at least one doped semiconductor material portion therein, and each semiconductor material portion within the at least one pillar structure has a doping of a same second conductivity type.

[0006] According to still another aspect of the present disclosure a method of forming at least one resistor structure comprises forming an alternating stack of first material layers and second material layers over a substrate, and forming at least one vertically-extending cavity from a first horizontal plane including a top surface of the alternating stack to a laterally-extending semiconductor or conductive structure. A physically exposed portion of a top surface of the laterally-extending semiconductor or conductive structure is present within a second horizontal plane located in the alternating stack below the first horizontal plane. The method further comprises forming a resistor comprising a pillar structure within each of the at least one vertically-extending cavity, wherein each pillar structure comprises at least one doped semiconductor material portion, and wherein each semiconductor material within the pillar structure has a doping of a same second conductivity type, and forming a contact via structure contacting another portion of the top surface of the laterally-extending semiconductor or conductive structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. **1** is a vertical cross-sectional view of a first exemplary structure after formation of a stack of an alternating plurality of first material layers and second material layers according to a first embodiment of the present disclosure.

[0008] FIG. **2** is a vertical cross-sectional view of the first exemplary structure after formation of memory stack structures and an insulating cap layer according to the first embodiment of the present disclosure.

[0009] FIG. **3** is a vertical cross-sectional view of the first exemplary structure after formation of an optional dielectric material portion according to the first embodiment of the present disclosure.

[0010] FIG. **4** is a vertical cross-sectional view of the first exemplary structure during formation of stepped surfaces according to the first embodiment of the present disclosure.

[0011] FIG. **5**A is a vertical cross-sectional view of the first exemplary structure after formation of stepped surfaces according to the first embodiment of the present disclosure.

[0012] FIG. **5**B is a top-down view of the first exemplary structure of FIG. **5**A.

[0013] FIG. **6**A is a vertical cross-sectional view of the first exemplary structure after formation of a retro-stepped dielectric material portion and dielectric pillar structures according to the first embodiment of the present disclosure.

[0014] FIG. **6**B is a horizontal cross-sectional view of the first exemplary structure of FIG. **6**A along the horizontal plane B-B'.

[0015] FIG. **7**A is a vertical cross-sectional view of the first exemplary structure after formation of a backside contact trench according to the first embodiment of the present disclosure.

[0016] FIG. **7**B is a horizontal cross-sectional view of the first exemplary structure of FIG. **7**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **7**A.

[0017] FIG. **7**C is a vertical cross-sectional view of the first exemplary structure of FIG. **8**B along the vertical plane C-C'.

[0018] FIG. **7**D is a top-down view of the first exemplary structure of FIGS. **7**A-**7**C.

[0019] FIG. **8**A is a vertical cross-sectional view of the first exemplary structure after formation of lateral recesses according to the first embodiment of the present disclosure.

[0020] FIG. **8**B is a horizontal cross-sectional view of the first exemplary structure of FIG. **8**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **8**A.

[0021] FIG. **8**C is a vertical cross-sectional view of the first exemplary structure of FIG. **7**B along the vertical plane C-C'.

[0022] FIG. **9**A is a vertical cross-sectional view of the first exemplary structure after formation of electrically conductive layers according to the first embodiment of the present disclosure.

[0023] FIG. **9**B is a horizontal cross-sectional view of the first exemplary structure of FIG. **9**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **9**A.

[0024] FIG. **10**A is a vertical cross-sectional view of the first exemplary structure after removal of a metallic material from trenches according to the first embodiment of the present disclosure.

[0025] FIG. **10**B is a horizontal cross-sectional view of the first exemplary structure of FIG. **10**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **10**A.

[0026] FIG. **11**A is a vertical cross-sectional view of the first exemplary structure after formation of dielectric fill material portions and a backside contact via structure according to the first embodiment of the present disclosure.

[0027] FIG. **11**B is a horizontal cross-sectional view of the first exemplary structure of FIG. **11**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **11**A.

[0028] FIG. **12**A is a vertical cross-sectional view of the first exemplary structure after formation of capacitor plate contact via structures and drain contact via structures according to the first embodiment of the present disclosure.

[0029] FIG. **12**B is a horizontal cross-sectional view of the first exemplary structure of FIG. **12**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **12**A.

[0030] FIG. **12**C is a vertical cross-sectional view of the first exemplary structure of FIG. **12**B along the vertical plane C-C'.

[0031] FIG. **12**D is a top-down view of the first exemplary structure of FIGS. **12**A-**12**C.

[0032] FIG. **13**A is a top-down view of the first exemplary structure after formation of a line level dielectric material layer and interconnect line structures according to the first embodiment of the present disclosure.

[0033] FIG. **13**B is a vertical cross-sectional view of the first exemplary structure of FIG. **13**A along the vertical plane B-B'.

[0034] FIG. **13**C is a vertical cross-sectional view of the first exemplary structure of FIG. **13**A along the vertical plane C-C'.

[0035] FIG. **13**D is a vertical cross-sectional view of the first exemplary structure of FIG. **13**A along the vertical plane D-D'.

[0036] FIG. **13**E is a vertical cross-sectional view of the first exemplary structure of FIG. **13**A along the vertical plane E-E'.

[0037] FIGS. **14**A and **14**X are schematic top down views of devices of embodiments of the invention. FIGS. **14**B, **14**E, **14**H, **14**K, **14**N, **14**Q and **14**T are top-down views of the alternative exemplary structures during fabrication steps of the device of FIG. **14**X. FIGS. **14**C, **14**F, **14**I, **14**L, **140**, **14**R and **14**U are vertical cross-sectional views along respective lines C-C', F-F', I-I', L-L', O-O', R-R' and U-U' in FIGS. **14**B, **14**E, **14**H, **14**K, **14**N, **14**Q and **14**T, respectively. FIGS. **14**D, **14**G, **14**J, **14**M, **14**P, **14**S and **14**V are vertical cross-sectional views along respective lines D-D', G-G', J-J', M-M', P-P', S-S' and V-V' in FIGS. **14**B, **14**E, **14**H, **14**K, **14**N, **14**Q and **14**T, respectively.

[0038] FIGS. **14**Y and **14**Z are schematic top down views of capacitor interconnection schemes of embodiments of the invention.

[0039] FIG. **15**A is a vertical cross-sectional view of a second exemplary structure after formation of a doped semiconductor well and an optional doped contact region according to a second embodiment of the present disclosure.

[0040] FIG. **15**B is a vertical cross-sectional view of the second exemplary structure after formation of an alternating stack of first material layers and second material layers according to the second embodiment of the present disclosure.

[0041] FIG. **16** is a vertical cross-sectional view of the second exemplary structure after formation of memory openings and vertically-extending cavities according to the second embodiment of the present disclosure.

[0042] FIG. **17** is a vertical cross-sectional view of the second exemplary structure after formation of memory stack structures and pillar structures according to the second embodiment of the present disclosure.

[0043] FIG. **18** is a vertical cross-sectional view of the second exemplary structure after implantation of dopants of a second conductivity type into the pillar structures according to the second embodiment of the present disclosure.

[0044] FIG. **19** is a vertical cross-sectional view of the second exemplary structure after formation of an optional insulating cap layer according to the second embodiment of the present disclosure.

[0045] FIG. **20** is a vertical cross-sectional view of the second exemplary structure after formation of a resistor contact trench according to the second embodiment of the present disclosure.

[0046] FIG. **21** is a vertical cross-sectional view of the second exemplary structure after formation of an insulating spacer and a substrate contact via structure according to the second embodiment of the present disclosure.

[0047] FIG. **22** is a vertical cross-sectional view of the second exemplary structure after formation of drain contact via structures, pillar contact via structures, and interconnect line structures according to the second embodiment of the present disclosure.

[0048] FIG. **23** is a vertical cross-sectional view of an alternate embodiment of the second exemplary structure according to the second embodiment of the present disclosure.

[0049] FIG. **24** is a vertical cross-sectional view of a third exemplary structure after replacement of first portions of second material layers with electrically conductive layers while maintaining second portions of the second material layers intact according to a third embodiment of the present disclosure.

[0050] FIG. **25** is a vertical cross-sectional view of the third exemplary structure after formation of drain contact via structures and a pillar contact line structure according to the third embodiment of the present disclosure.

[0051] FIG. **26** is a vertical cross-sectional view of the third exemplary structure after formation of a resistor contact trench according to the third embodiment of the present disclosure.

[0052] FIG. **27** is a vertical cross-sectional view of the third exemplary structure after formation of a substrate contact via structure according to the third embodiment of the present disclosure.

[0053] FIG. **28** is a vertical cross-sectional view of a fourth exemplary structure after formation of a dielectric material layer according to a fourth embodiment of the present disclosure.

[0054] FIG. **29**A is a vertical cross-sectional view of the fourth exemplary structure after formation of a backside contact trench according to the fourth embodiment of the present disclosure.

[0055] FIG. **29**B is a horizontal cross-sectional view of the fourth exemplary structure along the horizontal plane B-B' of FIG. **29**A. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **29**A.

[0056] FIG. **29**C is a vertical cross-sectional view of the first exemplary structure of FIG. **29**B along the vertical plane C-C'.

[0057] FIG. **29**D is a top-down view of the first exemplary structure of FIGS. **29**A-**29**C.

[0058] FIG. **30**A is a vertical cross-sectional view of the fourth exemplary structure after formation of electrically conductive layers according to the fourth embodiment of the present disclosure.

[0059] FIG. **30**B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. **30**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **30**A.

[0060] FIG. **31**A is a vertical cross-sectional view of the fourth exemplary structure after removal of a metallic material from trenches according to the fourth embodiment of the present disclosure.

[0061] FIG. **31**B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. **31**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **31**A.

[0062] FIG. **32**A is a vertical cross-sectional view of the fourth exemplary structure after formation of a backside insulating spacer and a backside contact via structure according to the fourth embodiment of the present disclosure.

[0063] FIG. **32**B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. **32**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **32**A.

[0064] FIG. **33**A is a vertical cross-sectional view of the fourth exemplary structure after formation of substrate contact via structures and drain contact via structures according to the fourth embodiment of the present disclosure.

[0065] FIG. **33**B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. **33**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **33**A.

[0066] FIG. **33**C is a vertical cross-sectional view of the fourth exemplary structure of FIG. **33**B along the vertical plane C-C'.

[0067] FIG. **33**D is a top-down view of the fourth exemplary structure of FIGS. **33**A-**33**C.

[0068] FIG. **34**A is a vertical cross-sectional view of the fourth exemplary structure after formation of vertically-extending cavities according to the fourth embodiment of the present disclosure.

[0069] FIG. **34**B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. **34**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **34**A.

[0070] FIG. **34**C is a vertical cross-sectional view of the fourth exemplary structure of FIG. **34**B along the vertical plane C-C'.

[0071] FIG. **34**D is a top-down view of the fourth exemplary structure of FIGS. **34**A-**34**C.

[0072] FIG. **35**A is a vertical cross-sectional view of the fourth exemplary structure after formation of resistor pillar structures according to the fourth embodiment of the present disclosure.

[0073] FIG. **35**B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. **35**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **35**A.

[0074] FIG. **35**C is a vertical cross-sectional view of the fourth exemplary structure of FIG. **35**B along the vertical plane C-C'.

[0075] FIG. **35**D is a top-down view of the fourth exemplary structure of FIGS. **35**A-**35**C.

[0076] FIG. **36**A is a vertical cross-sectional view of the fourth exemplary structure after formation of interconnect line structures according to the fourth embodiment of the present disclosure.

[0077] FIG. **36**B is a horizontal cross-sectional view of the fourth exemplary structure of FIG. **36**A along the plane B-B'. The vertical plane. A-A' is the plane of vertical cross-sectional view of FIG. **36**A.

[0078] FIG. **36**C is a vertical cross-sectional view of the fourth exemplary structure of FIG. **36**B along the vertical plane C-C'. FIG. **36**D is a top-down view of the fourth exemplary structure of FIGS. **36**A-**36**C.

[0079] FIG. **37** is a schematic top down view of devices of embodiments of the invention.

DETAILED DESCRIPTION

[0080] As discussed above, the present disclosure is directed to passive devices that are compatible with three-dimensional memory devices and methods of making thereof, the various aspects of which are described below. The embodiments of the disclosure can be employed to form various structures including a device structure, a non-limiting example of which includes capacitors and/or resistors that can be formed on a same substrate as additional semiconductor devices such as three-dimensional monolithic memory array devices comprising a plurality of NAND memory strings. The drawings are not drawn to scale. Multiple instances of an element may be duplicated where a single instance of the element is illustrated, unless absence of duplication of elements is expressly described or clearly indicated otherwise. Ordinals such as "first," "second," and "third" are employed merely to identify similar elements, and different ordinals may be employed across the specification and the claims of the instant disclosure. As used herein, a first element located "on" a second element can be located on the exterior side of a surface of the second element or on the interior side of the second element. As used herein, a first element is located "directly on" a second element if there exist a physical contact between a surface of the first element and a surface of the second element.

[0081] As used herein, a "layer" refers to a material portion including a region having a substantially uniform thickness. A layer may extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer may be a region of a homogeneous or inhomogeneous contiguous structure that has a thickness less than the thickness of the contiguous structure. For example, a layer may be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the contiguous structure. A plane is horizontal when it is parallel to a flat portion of the top surface of the substrate. However, it should be understood that the substrate may be positioned at any angle with respect to the direction of gravity and that the term "horizontal" does not imply that a horizontal direction must be perpendicular to the direction of gravity. A layer may extend horizontally, vertically, and/or along a tapered surface. A substrate may be a layer, may include one or more layers therein, and/or may have one or more layer thereupon, thereabove, and/or therebelow.

[0082] A monolithic three dimensional memory array is one in which multiple memory levels are formed above a single substrate, such as a semiconductor wafer, with no intervening substrates. The term "monolithic" means that layers of each level of the array are directly deposited on the layers of each underlying level of the array. In contrast, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device. For example, non-monolithic stacked memories have been constructed by forming memory levels on separate substrates and vertically stacking the memory levels, as described in U.S. Pat. No. 5,915,167 titled "Three Dimensional Structure Memory." The substrates may be thinned or removed from the memory levels before bonding, but as the memory levels are initially formed over separate substrates, such memories are not true monolithic three dimensional memory arrays. The various three dimensional memory devices of the present disclosure include a monolithic three-dimensional NAND string memory device, and can be fabricated employing the various embodiments described herein.

[0083] Referring to FIG. **1**, a first exemplary structure according to a first embodiment of the present disclosure is illustrated, which can be employed, for example, to fabricate a device structure containing vertical NAND memory devices. The first exemplary structure includes a substrate, which can be a semiconductor substrate. The substrate can include a semiconductor material layer **10**. The semiconductor material layer **10** can include at least one elemental semiconductor material, at least one III-V compound semiconductor material, at least one II-VI compound semiconductor material, at least one organic semiconductor material, or other semiconductor materials known in the art. The substrate can have a major surface **7**, which can be, for example, a topmost surface of the semiconductor material layer **10**. The major surface **7** can be a semiconductor surface. In one embodiment, the major surface **7** can be a single crystalline semiconductor surface.

[0084] As used herein, a "semiconductor material" refers to a material having electrical conductivity in the range from 1.0×10^{-6} S/cm to 1.0×10^{5} S/cm, and is capable of producing a doped material having electrical resistivity in a range from 1.0 S/cm to 1.0×10^{5} S/cm upon suitable doping with an electrical dopant. As used herein, an "electrical dopant" refers to a p-type dopant that adds a hole to a valence band within a band structure, or an n-type dopant that adds an electron to a conduction band within a band structure. As used herein, a "conductive material" refers to a material having electrical conductivity greater than 1.0×10^{5} S/cm. As used herein, an "insulator material" or a "dielectric material" refers to a material having electrical conductivity less than 1.0×10^{-6} S/cm. All measurements for electrical conductivities are made at the standard condition. Optionally, at least one doped well (not expressly shown) can be formed within the semiconductor material layer **10**.

[0085] At least one semiconductor device (not shown) for a peripheral circuitry can be formed on a portion of the semiconductor material layer **10**. The region in which the at least one semiconductor device for the peripheral circuitry is herein referred to as a peripheral device region. The at least one semiconductor device can include, for example, field effect transistors. The least one semiconductor device for the peripheral circuitry can contain a driver circuit for memory devices to be subsequently formed, which can include at least one NAND device.

[0086] Optionally, a dielectric pad layer **12** can be formed above the semiconductor material layer **10**. The dielectric pad layer **12** can be, for example, silicon oxide layer. The thickness of the dielectric pad layer **12** can be in a range from 3 nm to 30 nm, although lesser and greater thicknesses can also be employed. A dielectric cap layer **31** can be optionally formed. The dielectric cap layer **31** includes a dielectric material such as silicon oxide, a dielectric metal oxide, and silicon nitride (in case the material of second material layers to be subsequently formed is not silicon nitride).

[0087] A stack of an alternating plurality of first material layers (which can be insulating layers **32**) and second material layers (which can be sacrificial material layer **42**) is

formed over the top surface of the substrate, which can be, for example, on the top surface of the dielectric cap layer **31**. As used herein, an alternating plurality of first elements and second elements refers to a structure in which instances of the first elements and instances of the second elements alternate. Each instance of the first elements that is not an end element of the alternating plurality is adjoined by two instances of the second elements on both sides, and each instance of the second elements that is not an end element of the alternating plurality is adjoined by two instances of the first elements on both ends. The first elements may have the same thickness thereamongst, or may have different thicknesses. The second elements may have the same thickness thereamongst, or may have different thicknesses. The alternating plurality of first material layers and second material layers may begin with an instance of the first material layers or with an instance of the second material layers, and may end with an instance of the first material layers or with an instance of the second material layers. In one embodiment, an instance of the first elements and an instance of the second elements may form a unit that is repeated with periodicity within the alternating plurality.

[0088] Each first material layer includes a first material, and each second material layer includes a second material that is different from the first material. In one embodiment, each first material layer can be an insulator layer **32**, and each second material layer can be a sacrificial material layer **42**. In this case, the stack can include an alternating plurality of insulator layers **32** and sacrificial material layers **42**.

[0089] The stack of the alternating plurality is herein referred to as an alternating stack (**32**, **42**). In one embodiment, the alternating stack (**32**, **42**) can include insulator layers **32** composed of the first material, and sacrificial material layers **42** composed of a second material different from that of insulator layers **32**. The first material of the insulator layers **32** can be at least one electrically insulating material. As such, each insulator layer **32** can be an electrically insulating material layer. Electrically insulating materials that can be employed for the insulator layers **32** include, but are not limited to silicon oxide (including doped or undoped silicate glass), silicon nitride, silicon oxynitride, organosilicate glass (OSG), spin-on dielectric materials, dielectric metal oxides that are commonly known as high dielectric constant (high-k) dielectric oxides (e.g., aluminum oxide, hafnium oxide, etc.) and silicates thereof, dielectric metal oxynitrides and silicates thereof, and organic insulating materials. In one embodiment, the first material of the insulator layers **32** can be silicon oxide.

[0090] The second material of the sacrificial material layers **42** is a sacrificial material that can be removed selective to the first material of the insulator layers **32**. As used herein, a removal of a first material is "selective to" a second material if the removal process removes the first material at a rate that is at least twice the rate of removal of the second material. The ratio of the rate of removal of the first material to the rate of removal of the second material is herein referred to as a "selectivity" of the removal process for the first material with respect to the second material.

[0091] The sacrificial material layers **42** may comprise an electrically insulating material, a semiconductor material, or a conductive material. The second material of the sacrificial material layers **42** can be subsequently replaced with electrically conductive electrodes which can function, for example, as control gate electrodes of a vertical NAND device. Non-limiting examples of the second material include silicon nitride, an amorphous semiconductor material (such as amorphous silicon), and a polycrystalline semiconductor material (such as polysilicon). In one embodiment, the sacrificial material layers **42** can be material layers that comprise silicon nitride or a semiconductor material including at least one of silicon and germanium.

[0092] In one embodiment, the insulator layers **32** can include silicon oxide, and sacrificial material layers can include silicon nitride sacrificial material layers. The first material of the insulator layers **32** can be deposited, for example, by chemical vapor deposition (CVD). For example, if silicon oxide is employed for the insulator layers **32**, tetraethyl orthosilicate (TEOS) can be employed as the precursor material for the CVD process. The second material of the sacrificial material layers **42** can be formed, for example, CVD or atomic layer deposition (ALD).

[0093] The sacrificial material layers **42** can be suitably patterned so that conductive material portions to be subsequently formed by replacement of the sacrificial material layers **42** can function as electrically conductive electrodes, such as the control gate electrodes of the monolithic three-dimensional NAND string memory devices to be subsequently formed. The sacrificial material layers **42** may comprise a portion having a strip shape extending substantially parallel to the major surface **7** of the substrate.

[0094] The thicknesses of the insulator layers **32** and the sacrificial material layers **42** can be in a range from 20 nm to 50 nm, although lesser and greater thicknesses can be employed for each insulator layer **32** and for each sacrificial material layer **42**. The number of repetitions of the pairs of an insulator layer **32** and a sacrificial material layer (e.g., a control gate electrode or a sacrificial material layer) **42** can be in a range from 2 to 1,024, and typically from 8 to 256, although a greater number of repetitions can also be employed. The top and bottom gate electrodes in the stack may function as the select gate electrodes. In one embodiment, each sacrificial material layer **42** in the alternating stack (**32**, **42**) can have a uniform thickness that is substantially invariant within each respective sacrificial material layer **42**. The first exemplary structure may include a memory device region **100** in which an array of memory devices can be subsequently formed, and a capacitor region **400** in which at least one passive device can be subsequently formed.

[0095] Referring to FIG. **2**, a lithographic material stack (not shown) including at least a photoresist layer can be formed over the alternating stack (**32**, **42**), and can be lithographically patterned to form openings therein. The pattern in the lithographic material stack can be transferred through the entirety of the alternating stack (**32**, **42**) by at least one anisotropic etch that employs the patterned lithographic material stack as an etch mask. Portions of the alternating stack (**32**, **42**) underlying the openings in the patterned lithographic material stack are etched to form memory openings. In other words, the transfer of the pattern in the patterned lithographic material stack through the alternating stack (**32**, **42**) forms the memory openings that extend through the alternating stack (**32**, **42**). The chemistry of the anisotropic etch process employed to etch through the materials of the alternating stack (**32**, **42**) can alternate to optimize etching of the first and second materials in the alternating stack (**32**, **42**). The anisotropic etch can be, for example, a series of reactive ion etches. Optionally, the

dielectric cap layer **31** may be used as an etch stop layer between the alternating stack (**32**, **42**) and the substrate. The sidewalls of the memory openings can be substantially vertical, or can be tapered. The patterned lithographic material stack can be subsequently removed, for example, by ashing. The memory openings can be formed in the memory device region **100**.

[0096] The memory openings are formed through the dielectric cap layer **31** and the dielectric pad layer **12** so that the memory openings extend from the top surface of the alternating stack (**32**, **42**) to the top surface of the semiconductor material layer **10**. In one embodiment, an overetch into the semiconductor material layer **10** may be optionally performed after the top surface of the semiconductor material layer **10** is physically exposed at a bottom of each memory openings. The overetch may be performed prior to, or after, removal of the lithographic material stack. In other words, the recessed surfaces of the semiconductor material layer **10** may be vertically offset from the undressed top surfaces of the semiconductor material layer **10** by a recess depth. The recess depth can be, for example, in a range from 1 nm to 50 nm, although lesser and greater recess depths can also be employed. The overetch is optional, and may be omitted. If the overetch is not performed, the bottom surface of each memory openings can be coplanar with the topmost surface of the semiconductor material layer **10**. Each of the memory openings can include a sidewall (or a plurality of sidewalls) that extends substantially perpendicular to the topmost surface of the substrate. The region in which the array of memory openings is formed is herein referred to as a device region.

[0097] A memory stack structure **55** can be formed within each memory opening through the alternating stack (**32**, **42**). The memory stack structures **55** can be formed, for example, by forming an optional epitaxial channel portion **66** at a bottom portion of each memory opening by selectively depositing a semiconductor material that is intrinsic or has a doping of a same conductivity type as the semiconductor material layer **10**. Alternatively, portion **66** may be omitted or replaced by a trench in layer **10**. A memory film layer is deposited in the memory openings over the alternating stack (**32**, **42**) by a series of conformal deposition processes. The memory film layer can be a stack of contiguous material layers that overlie the entirety of the alternating stack (**31**, **42**,). The memory film layer contacts all sidewall surface(s) and all bottom surface(s) of the memory openings. The memory film layer is a contiguous film stack that provides the functionality of charge storage in the absence of an external electrical bias voltage, while enabling charge transfer in the presence of a suitable external electrical bias voltage.

[0098] In one embodiment, the memory film layer can be a stack, in the order of formation, of a blocking dielectric layer, a charge storage layer, and a tunnel dielectric layer. In one embodiment, a plurality of floating gates or a charge storage dielectric can be located between the tunneling dielectric layer and the blocking dielectric layer.

[0099] The blocking dielectric layer contacts the sidewalls of the memory openings. Specifically, the blocking dielectric layer can contact the sidewalls of the sacrificial layers **42**. The blocking dielectric layer may include one or more dielectric material layers that can function as the control gate dielectrics for control gate electrodes to be subsequently formed. The blocking dielectric layer can include silicon oxide, a dielectric metal oxide, a dielectric metal oxynitride, or a combination thereof. In one embodiment, the blocking dielectric layer can include a stack of at least one silicon oxide layer and at least one dielectric metal oxide layer. The blocking dielectric layer can be formed by a conformal deposition process such as chemical vapor deposition (CVD) and/or atomic layer deposition (ALD), and/or by deposition of a conformal material layer (such as an amorphous silicon layer) and subsequent conversion of the conformal material layer into a dielectric material layer (such as a silicon oxide layer). The thickness of the blocking dielectric layer can be in a range from 6 nm to 24 nm, although lesser and greater thicknesses can also be employed. Alternatively, the blocking dielectric layer may be omitted from the memory opening, and instead be formed through the backside contact trench in recesses formed by removal of the sacrificial layers **42** prior to forming the metal control gate electrodes through a backside contact trench.

[0100] The charge storage layer includes a dielectric charge trapping material, which can be, for example, silicon nitride, or a conductive material such as doped polysilicon or a metallic material. In one embodiment, the charge storage layer includes silicon nitride. The charge storage layer can be formed as a single charge storage layer of homogeneous composition, or can include a stack of multiple charge storage material layers. The multiple charge storage material layers, if employed, can comprise a plurality of spaced-apart floating gate material layers that contain conductive materials (e.g., metal such as tungsten, molybdenum, tantalum, titanium, platinum, ruthenium, and alloys thereof, or a metal silicide such as tungsten silicide, molybdenum silicide, tantalum silicide, titanium silicide, nickel silicide, cobalt silicide, or a combination thereof) and/or semiconductor materials (e.g., polycrystalline or amorphous semiconductor material including at least one elemental semiconductor element or at least one compound semiconductor material). Alternatively or additionally, the charge storage layer may comprise an insulating charge trapping material, such as one or more silicon nitride segments. Alternatively, the charge storage layer may comprise conductive nanoparticles such as metal nanoparticles, which can be, for example, ruthenium nanoparticles. The charge storage layer can be formed, for example, by chemical vapor deposition (CVD), atomic layer deposition (ALD), physical vapor deposition (PVD), or any suitable deposition technique for the selected material(s) for the charge storage layer. The thickness of the charge storage layer can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0101] The tunnel dielectric layer includes a dielectric material through which charge tunneling can be performed under suitable electrical bias conditions. The charge tunneling may be performed through hot-carrier injection or by Fowler-Nordheim tunneling induced charge transfer depending on the mode of operation of the monolithic three-dimensional NAND string memory device to be formed. The tunneling dielectric layer can include silicon oxide, silicon nitride, silicon oxynitride, dielectric metal oxides (such as aluminum oxide and hafnium oxide), dielectric metal oxynitride, dielectric metal silicates, alloys thereof, and/or combinations thereof. In one embodiment, the tunneling dielectric layer can include a stack of a first silicon oxide layer, a silicon oxynitride layer, and a second silicon oxide layer, which is commonly known as an ONO

stack. In one embodiment, the tunneling dielectric layer can include a silicon oxide layer that is substantially free of carbon or a silicon oxynitride layer that is substantially free of carbon. The thickness of the tunnel dielectric layer can be in a range from 2 nm to 20 nm, although lesser and greater thicknesses can also be employed.

[0102] Optionally, a permanent channel material layer (such as a polysilicon layer) and/or a sacrificial layer (such as a dielectric material layer) may be formed on the memory film layer. The memory film layer (and any additional layer such as a permanent channel material layer or a sacrificial layer) can be anisotropically etched so that horizontal portions of the memory film layer (and any additional layer) are removed from above the top surface of the alternating stack (**32**, **42**) and at the bottom of each memory opening. Each remaining vertical portion of the memory film layer that remains within a memory opening after the anisotropic etch constitutes a memory film **50**. Each memory film **50** can be homeomorphic to a torus. As used herein, an element is homeomorphic to a geometrical shape if the shape of the element can be mapped to the geometrical shape by continuous deformation without creation or destruction of any hole. If an electrode underlies the memory openings, a top surface of the electrode can be physically exposed within the cavity defined by the inner sidewalls of an overlying memory film **50**.

[0103] In one embodiment, a first semiconductor channel layer can be deposited directly on the surfaces of the tunnel dielectric layer as a permanent channel material layer by a conformal deposition method such as chemical vapor deposition (CVD). The first semiconductor channel layer and the memory films can be anisotropically etched to form an opening at a bottom portion of each memory opening. A top surface of the substrate semiconductor layer **10** is physically exposed at the bottom of each memory opening. Each remaining portion of the first semiconductor channel layer within a memory opening constitutes a first semiconductor channel portion **601**.

[0104] After formation of a memory film **50** and a first semiconductor channel portion **601** within each memory opening, a second semiconductor channel layer can be deposited on the sidewalls of the first semiconductor channel portions **601**, physically exposed surfaces of the substrate semiconductor layer **10** within the memory openings, and over the alternating stack (**32**, **42**). The semiconductor material of the second semiconductor channel layer can include a doped polycrystalline semiconductor material (such as doped polysilicon), or can include a doped amorphous semiconductor material (such as amorphous silicon) that can be subsequently converted into a doped polycrystalline semiconductor material after a suitable anneal at an elevated temperature.

[0105] Optionally, a dielectric core **62** can be formed within a cavity inside each semiconductor channel **60**, for example, by deposition of a dielectric material such as silicon oxide, and subsequent planarization of the dielectric material. The planarization of the dielectric material removes the portion of the deposited dielectric material from above the top surface of the horizontal plane including the top surface of the topmost layer of the alternating stack (**32**, **42**), which can be, for example, the top surface of the topmost insulator layer **32**. The planarization of the dielectric material can be performed, for example, by chemical mechanical planarization. Each remaining portion of the dielectric material inside a memory opening constitutes a dielectric core **62**. The dielectric core **62** is an optional component, and a combination of a memory film **50** and a semiconductor channel **60** may completely fill a memory opening

[0106] The horizontal portion of the second semiconductor channel layer above the top surface of the topmost layer of the alternating stack (**32**, **42**) can be removed, for example, by a recess etch. Each remaining portion of the second semiconductor channel layer constitutes a second semiconductor channel **602**. Each adjoined pair of a first semiconductor channel **601** and a second semiconductor channel **602** vertically extend through the alternating stack (**32**, **42**), and optional pillar collectively constitutes a portion of a semiconductor channel **60** for a memory stack structure **55**. A set of a memory film **50** and a semiconductor channel **60** within a same memory opening constitutes a memory stack structure **55**.

[0107] Drain regions **63** can be formed by recessing a top portion of each dielectric core and depositing a doped semiconductor material. The doped semiconductor material can be, for example, doped polysilicon. The drain regions **63** can have a doping of a second conductivity type, which is the opposite of the first conductivity type (that is the conductivity type of the semiconductor material layer **10**). Excess portions of the deposited semiconductor material can be removed from above the top surface of the alternating stack (**32**, **42**), for example, by chemical mechanical planarization (CMP) or a recess etch.

[0108] Optionally, an insulating cap layer **71** can be formed over the alternating stack (**32**, **42**) and the array of memory stack structures **55**. The insulating cap layer **71** can include a dielectric material such as silicon oxide, a dielectric metal oxide, and/or a nitrogen-doped organosilicate glass. The thickness of the insulating cap layer **71** can be in a range from 5 nm to 100 nm, although lesser and greater thicknesses can also be employed.

[0109] Referring to FIG. **3**, a portion of the alternating stack (**32**, **42**) can be removed, for example, by applying and patterning a photoresist layer (not shown), and by transferring the pattern of the photoresist layer through the alternating stack (**32**, **42**) employing an etch such as an anisotropic etch. A trench extending through the entire thickness of the alternating stack (**32**, **42**) can be formed. Subsequently, the trench can be filled with an optional dielectric material such as silicon oxide to form a dielectric material portion **64**. Excess portions of the dielectric material can be removed from above the top surface of the insulating cap layer **71** by a planarization process such as chemical mechanical planarization and/or a recess etch. The top surfaces of the insulating cap layer **71** can be employed as a stopping surface during the planarization. A top surface of the dielectric material portion **64** can be coplanar with a top surface of the insulating cap layer **71**.

[0110] Referring to FIG. **4**, a trimming material layer **67** is formed and patterned over the insulating cap layer **71**. The trimming material layer **67** comprises a material that can be continually trimmed, i.e., a material that can be gradually removed over a time duration from outside to inside at a controlled removal rate. For example, the trimming material layer **67** can be selected from a photoresist material, an organic polymer material, and an inorganic polymer material. Organic polymer materials that can be employed for the trimming material layer **67** can be an organic material made

of cross-linked carbon-containing monomers, and can be carbon-based self-planarizing material known in the art. Inorganic polymer material that can be employed for the trimming material layer **67** include silicon-based polymer materials such as silicon-based antireflective coating materials as known in the art. A portion of the trimming material layer **67** remains after repeated trimming that shifts an outer sidewall of the trimming material layer **67** to a periphery of the capacitor region **400** adjoining the memory device region **100**.

[0111] Portions of the insulating cap layer **71** and a topmost insulator layer **32** within the area of an opening in the trimming material layer **67** can be removed by an anisotropic etch. The last step of the anisotropic etch can be selective to the material of the sacrificial material layer **42** to minimize an overetch into the topmost sacrificial material layer **42**. A recess cavity is formed at the levels of the insulating cap layer **71** and the topmost insulator layer **32** within the area of the opening in the trimming material layer **67**.

[0112] Subsequently, a set of process steps is repeatedly performed to form stepped surfaces in the capacitor region **400**. Each set of processing steps can include a first processing step of trimming the trimming material layer **67** to widen the opening in the trimming material layer **67**, a second processing step of anisotropically etching the material of the sacrificial material layers **42** (with or without collateral etching of the material of the insulating cap layer **71**) within the opening in the trimming material layer **67**, a third step of anisotropically etching any remaining portion of the insulating cap layer **71** and the material of the insulator layers **32** within the opening in the trimming material layer **67**. In one embodiment, an anisotropic etch process employed in the second processing step can be selective to the material of the insulator layers **32**, and the anisotropic etch employed in the third processing step can be selective to the material of the sacrificial material layers **42**.

[0113] Referring to FIGS. **5**A and **5**B, the set of processing steps is repeated performed until the bottommost sacrificial material layer **42** is patterned. Optionally, the dielectric cap layer **31** and the dielectric pad layer **12** may be patterned with the same pattern as the bottommost sacrificial material layer **42**. The trimming material layer **67** can be subsequently removed, for example, by ashing.

[0114] A stepped surface region is formed in the capacitor region **400**. As used herein, a "stepped surface region" refers to a region in which stepped surfaces are present. As used herein, "stepped surfaces" refer to a set of surfaces that include at least two horizontal surfaces and at least two vertical surfaces such that each horizontal surface is adjoined to a first vertical surface that extends upward from a first edge of the horizontal surface, and is adjoined to a second vertical surface that extends downward from a second edge of the horizontal surface.

[0115] The cavity overlying the steppes surfaces is a stepped cavity. As used herein, a "stepped cavity" refers to a cavity having stepped surfaces. The stepped cavity **69** can straddle a remaining portion of the dielectric material portion **64** (not shown) and a remaining patterned portion of the alternating stack (**32**, **42**). Within the stepped surface region, each underlying second material layer (such as a sacrificial material layer **42**) laterally extends farther than any overlying second material layer, and each underlying first material layer (such as an insulator layer **32**) laterally extends farther than any overlying first material layer. A vertically adjoining pair of a first material layer (such as an insulator layer **32**) and a second material layer (such as a sacrificial material layer **42**) can have vertically coincident sidewalls. As used herein, a first surface and a second surface are vertically coincident with each other if there exists a vertical plane including both the first surface and the second surface.

[0116] Referring to FIGS. **6**A and **6**B, a dielectric material portion (i.e., insulating fill material portion) can be formed in the stepped cavity **69** by deposition of a dielectric material such as silicon oxide. Excess portions of the deposited dielectric material can be removed from above the top surface of the insulating cap layer **71**, for example, by chemical mechanical planarization (CMP). The remaining portion of the deposited dielectric material filling the stepped cavity **69** constitutes the dielectric material portion.

[0117] The dielectric material portion is retro-stepped, and is herein referred to as a retro-stepped dielectric material portion **65**. As used herein, a "retro-stepped" element refers to an element that has stepped surfaces and a horizontal cross-sectional area that increases monotonically as a function of a vertical distance from a top surface of a substrate on which the element is present. The retro-stepped dielectric material portion **65** is formed over the stepped structure of the alternating stack (**32**, **42**), and can have a planar top surface. If silicon oxide is employed for the retro-stepped dielectric material portion **65**, the silicon oxide of the retro-stepped dielectric material portion **65** may, or may not, be doped with dopants such as B, P, and/or F. The horizontal cross-sectional area of the retro-stepped dielectric material portion **65** at a horizontal plane is not less than the horizontal cross-sectional area of the retro-stepped dielectric material portion **65** at any horizontal plane that is more proximal to the substrate (i.e., the semiconductor material layer **10**).

[0118] At least one dielectric pillar structure **7**P may be optionally formed through the retro-stepped dielectric material portion **65** and/or through the alternating stack (**32**, **42**). Further, dielectric support pillar structures **7**Q may be formed in the contact region, which provide support for the insulator layers **32** in subsequent processing steps, and especially, during replacement of sacrificial material layers with conductive material layers. The at least one dielectric pillar structure **7**P and the dielectric support pillar structures **7**Q can be formed, for example, by forming openings extending through the retro-stepped dielectric material portion **65** and/or through the alternating stack (**32**, **42**) and at least to the top surface of the substrate **10**, and by filling the openings with a dielectric fill material that is resistant to the etch chemistry to be employed to remove the sacrificial material layers **42**. In one embodiment, the at least one dielectric pillar structure can include silicon oxide and/or a dielectric metal oxide such as aluminum oxide. In one embodiment, the portion of the dielectric material that is deposited over the insulating cap layer **71** concurrently with deposition of the at least one dielectric pillar structure **7**P and the dielectric support pillar structures **7**Q can be present over insulating cap layer **71** as a dielectric material layer **73**. The dielectric material layer **73** and the at least one dielectric pillar structure **7**P and the dielectric support pillar structures **7**Q can be formed as a single contiguous structure of integral construction, i.e., without any material interface therebetween. In another embodiment, the portion of the dielectric material that is deposited over insulating cap layer **71** concurrently with deposition of the at least one dielectric pillar structure **7**P and the dielectric support pillar structures

7Q can be removed, for example, by chemical mechanical planarization or a recess etch. In this case, the dielectric material layer **73** is not present, and the top surface of insulating cap layer **71** can be physically exposed.

[0119] In this embodiment, the shape of the at least one dielectric pillar structure 7P can be such that the at least one dielectric pillar structure 7P physically isolates a first portion of the alternating stack (**32**, **42**) located within the memory device region **100** from a second portion of the alternating stack (**32**, **42**) located within the capacitor region **400**. In one embodiment, a dielectric pillar structure 7P can be formed at a boundary between the memory device region **100** and the capacitor region **400**. However, other pillar 7P shapes, such as cylindrical pillar shapes may be used as described below with respect to FIG. **14**A of the alternative embodiment. The dielectric support pillar structures 7Q can be formed as an array of discrete dielectric support pillar structures so as to provide mechanical support to the structures in the contact region during subsequent processing steps.

[0120] FIGS. **7**A-**7**D, a photoresist layer (not shown) can be applied over the alternating stack (**32**, **42**) and the retro-stepped dielectric material portion **65** and the optional dielectric material layer **73**, and lithographically patterned to form openings therein. The pattern of the openings includes an opening in the memory device region **100** and a plurality of openings in the capacitor region **400**. The pattern of the opening in the memory device region **100** is selected such that a lateral distance from the opening in the memory device region **100** to a group of memory stack structures **55** does not exceed a predefined distance, which is the distance of a lateral etch to be subsequently employed to form lateral recesses. The pattern of the openings in the capacitor region **400** is selected such that trenches to be subsequently formed within the area of the openings within the capacitor region **400** can divide the second portion of the alternating stack (**32**, **42**) located within the capacitor region **400** into a plurality of physically disjoined alternating stacks (**32**, **42**).

[0121] An anisotropic etch can be performed to etch through portions of the optional dielectric material layer **73**, the optional insulating cap layer **71**, the retro-stepped dielectric material portion **65**, and the alternating stack (**32**, **42**) that underlie the openings within the photoresist layer. A backside contact trench **79** is formed directly underneath the opening in the photoresist layer within the memory device region **100**. A lateral separation trench **89** is formed directly underneath each opening in the photoresist layer within the capacitor region **400**. The backside contact trench **79** and the lateral separation trenches **89** can extend from the top surface of the dielectric material layer **73** (or the material layer contacting the bottom surface of the photoresist layer in case a dielectric material layer **73** is not employed) at least to the top surface of the semiconductor material layer **10** in the substrate. The lateral separation trenches **89** divides the second portion of the alternating stack (**32**, **42**) in the capacitor region **400** into a plurality of physically disjoined alternating stacks (**32**, **42**) that are laterally spaced apart by the lateral separation trenches **89**.

[0122] Each of the backside contact trench **79** and the lateral separation trenches **89** can be a line trench, i.e., a trench having a uniform width and extending along a lengthwise direction. The sidewalls of the backside contact trench **79** and the lateral separation trenches **89** may be vertical, or may be tapered. In one embodiment, the backside contact trench **79** may have a first trench width tw**1**, and the lateral separation trenches **89** may have a second trench width tw**2** that is less than the first trench width tw**1**. In one embodiment, the first trench width tw**1** can be in a range from 30 nm to 1,000 nm, and the second trench width w**2** can be in a range from 20 nm to 500 nm, although lesser and greater trench widths can be employed for each of the backside contact trench **79** and the lateral separation trenches **89**.

[0123] In one embodiment, a dielectric pillar structure 7P can extend along a first horizontal direction hd**1**, and the backside contact trench **79** can extend along the first horizontal direction hd**1**. The lateral separation trenches **89** can adjoin the dielectric pillar structure 7P such that a sidewall of each lateral separation trench **89** is a sidewall of the dielectric pillar structure 7P. The lateral separation trenches **89** can extend along a horizontal direction that is different from the first horizontal direction hd**1**, which is herein referred to as a second horizontal direction hd**2**. In one embodiment, the second horizontal direction hd**2** can be perpendicular to the first horizontal direction hd**1**. In one embodiment, the lateral separation trenches **89** can laterally extend along a lateral direction that is perpendicular to the stepped surfaces within the stepped surface region. As used herein, a lateral direction that is perpendicular to the stepped surfaces refers to the lateral direction that is perpendicular to vertical surfaces within the stepped surfaces. In other words, the second horizontal direction hd**2** can be perpendicular to the vertical surfaces (i.e., the sidewalls of the insulator layers **32** and the sacrificial material layers **42**) of the stepped surfaces.

[0124] Each lateral separation trench **89** extends through the stack of alternating layers (**32**, **42**) as embodied in multiple physically disjoined portions. Sidewalls of patterned portions of the stack of alternating layers (**32**, **42**) are physically exposed within each lateral separation trench **89**. The photoresist layer can be removed, for example, by ashing.

[0125] Referring to FIGS. **8**A-**8**C, an etchant that selectively etches the second material of the sacrificial material layers **42** with respect to the first material of the insulator layers **32** can be introduced into the backside contact trench **79** and the lateral separation trenches **89**, for example, employing an isotropic etch process. Backside recesses (**43**, **143**) are formed in volumes from which the sacrificial material layers **42** are removed. The removal of the second material of the sacrificial material layers **42** can be selective to the first material of the insulator layers **32**, the material of the at least one dielectric support pillar 7P, the material of the retro-stepped dielectric material portion **65**, the semiconductor material of the semiconductor material layer **10**, and the material of the outermost layer of the memory films **50**. In one embodiment, the sacrificial material layers **42** can include silicon nitride, and the materials of the insulator layers **32**, the at least one dielectric support pillar 7P, and the retro-stepped dielectric material portion **65** can be selected from silicon oxide and dielectric metal oxides. In another embodiment, the sacrificial material layers **42** can include a semiconductor material such as polysilicon, and the materials of the insulator layers **32**, the at least one dielectric support pillar 7P, and the retro-stepped dielectric material portion **65** can be selected from silicon oxide, silicon nitride, and dielectric metal oxides. In this case, the depth of the backside contact trench **79** can be modified so that the bottommost surface of the backside contact trench **79** is

located within the dielectric pad layer **12**, i.e., to avoid physical exposure of the top surface of the semiconductor substrate layer **10**.

[0126] The etch process that removes the second material selective to the first material and the outermost layer of the memory films **50** can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which the etchant is introduced in a vapor phase into the backside contact trench **79**. For example, if the sacrificial material layers **42** include silicon nitride, the etch process can be a wet etch process in which the exemplary structure is immersed within a wet etch tank including phosphoric acid, which etches silicon nitride selective to silicon oxide, silicon, and various other materials employed in the art. The at least one dielectric support pillar **7**P, the retro-stepped dielectric material portion **65**, and the memory stack structures **55** provide structural support while the backside recesses (**43**, **143**) are present within volumes previously occupied by the sacrificial material layers **42**.

[0127] Each backside recess (**43**, **143**) can be a laterally-extending cavity having a lateral dimension that is greater than the vertical extent of the cavity. In other words, the lateral dimension of each backside recess (**43**, **143**) can be greater than the height of the backside recess (**43**, **143**). A plurality of backside recesses (**43**, **143**) can be formed in the volumes from which the second material of the sacrificial material layers **42** is removed. The plurality of backside recesses (**43**, **143**) include first backside recesses **43** that are formed within the memory device region **100** by introduction of the etchant through the backside contact trench **79**, and second backside recesses that are formed within the capacitor region **400** by introduction of the etchant through the lateral separation trenches **89**.

[0128] Each of the plurality of first backside recesses (**43**, **143**) can extend substantially parallel to the top surface of the substrate **10**. A backside recess (**43**, **143**) can be vertically bounded by a top surface of an underlying insulator layer **32** and a bottom surface of an overlying insulator layer **32**. In one embodiment, each backside recess (**43**, **143**) can have a uniform height throughout.

[0129] The memory openings in which the memory stack structures **55** are formed are herein referred to as front side recesses or front side cavities in contrast with the first backside recesses **43**. In one embodiment, the memory device region **100** comprises an array of monolithic three-dimensional NAND strings having a plurality of device levels disposed above the substrate **10**. In this case, each first backside recess **43** can define a space for receiving a respective word line of the array of monolithic three-dimensional NAND strings.

[0130] The second lateral recesses **143** can be formed at each level of the sacrificial material layers **42** in the capacitor region **400**. Each second lateral recess **143** can be adjoined to at least one of the lateral separation trenches **89**. At least one set of second lateral recesses **143** can be laterally adjoined to a neighboring pair of lateral separation trenches **89**. Thus, a stacked cavity structure is formed between each neighboring pair of lateral separation trenches **89** such that a set of second backside recesses **143** is interlaced with a set of insulator layers **32**. In one embodiment, the lateral separation trenches **89** can be formed with a periodicity p. The lateral distance between neighboring pairs of the lateral separation trenches **89** can be uniform. In this case, the second backside recesses **143** within a stacked cavity structure (**143**, **32**) between a neighboring pair of lateral separation trenches **89** can have the same lateral extent along the first horizontal direction hd**1**, and can have different lateral extents along the second horizontal direction hd**2**.

[0131] Physically exposed surface portions of epitaxial channel portions **66** and the semiconductor material layer **10** can be converted into dielectric material portions by thermal conversion and/or plasma conversion of the semiconductor materials into dielectric materials. For example, thermal conversion and/or plasma conversion can be employed to convert a surface portion of each epitaxial channel portion **66** into a dielectric spacer **116**, and to convert a surface portion of the semiconductor material layer **10** underneath each backside contact trench **79** and trenches **89** into a sacrificial dielectric portion **616**. In one embodiment, each dielectric spacer **116** can be topologically homeomorphic to a torus, i.e., generally ring-shaped. As used herein, an element is topologically homeomorphic to a torus if the shape of the element can be continuously stretched without destroying a hole or forming a new hole into the shape of a torus.

[0132] The dielectric spacers **116** include a dielectric material that includes the same semiconductor element as the epitaxial channel portions **66** and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the dielectric spacers **116** is a dielectric material. In one embodiment, the dielectric spacers **116** can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the epitaxial channel portions **66**. Likewise, each sacrificial dielectric portion **616** includes a dielectric material that includes the same semiconductor element as the semiconductor material layer **10** and additionally includes at least one non-metallic element such as oxygen and/or nitrogen such that the material of the sacrificial dielectric portions **616** is a dielectric material. In one embodiment, the sacrificial dielectric portions **616** can include a dielectric oxide, a dielectric nitride, or a dielectric oxynitride of the semiconductor material of the semiconductor material layer **10**.

[0133] Referring to FIGS. **9**A and **9**B, a backside blocking dielectric layer (not shown) including a dielectric material (such as aluminum oxide) can be formed in the backside recesses (**43**, **143**) by a conformal deposition. At least one conductive material can be deposited in the plurality of backside recesses (**43**, **143**), on the sidewalls of the backside contact trench **79** and trenches **89**, and over the topmost layer of the first exemplary structure. The conductive material can be deposited by a conformal deposition method, which can be, for example, chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless plating, electroplating, or a combination thereof. The conductive material can be an elemental metal, an intermetallic alloy of at least two elemental metals, a conductive nitride of at least one elemental metal, a conductive metal oxide, a conductive doped semiconductor material, a conductive metal-semiconductor alloy such as a metal silicide, alloys thereof, and combinations or stacks thereof. Non-limiting exemplary conductive materials that can be deposited in the plurality of backside recesses (**43**, **143**) include tungsten, tungsten nitride, titanium, titanium nitride, tantalum, and tantalum nitride. In one embodiment, the conductive material can comprise a metal such as tungsten and/or metal nitride. In one embodiment, the conductive material for filling the

plurality of backside recesses (**43**, **143**) can be a combination of titanium nitride and tungsten. In one embodiment, the conductive material can be deposited by chemical vapor deposition. The second material layers **42** are replaced with conductive material portions.

[0134] A plurality of first electrically conductive layers **46** can be formed in the plurality of first backside recesses **43** in the memory device region. A plurality of second electrically conductive layers **146** can be formed in the plurality of second backside recesses **143**. A contiguous conductive material layer **46**L can be formed on the sidewalls of the backside contact trench **79** and over the topmost layer of the first exemplary structure. Thus, each sacrificial material layer **42** can be replaced with a first electrically conductive layer **46** in the memory device region **100** and a second electrically conductive layer **146** in the capacitor region **400**. A backside cavity **79'** is present in the portion of each backside contact trench **79** that is not filled with the contiguous conductive material layer **46**L. A lateral separation cavity **89'** is present in the portion of each lateral separation trench **89** that is not filled with the contiguous conductive material layer **46**L.

[0135] In one embodiment, the thickness of the deposited conductive material can be selected that the lateral separation trenches **89** and the backside contact trench **79** are not completely filled with the contiguous conductive material layer **46**L. In this case, a cavity (**79'**, **89'**) is present within each of the lateral separation trenches **89** and the backside contact trench **79** after deposition of the conductive material. The contiguous conductive material layer **46**L, the first electrically conductive layers **46**, and the second electrically conductive layers **146** are formed as a single contiguous structure.

[0136] Referring to FIGS. **10**A and **10**B, the deposited conductive material of the contiguous conductive material layer **46**L is etched back from the sidewalls of each backside contact trench **79**, from the sidewalls of each lateral separation trench **89**, and from the dielectric material layer **73**, for example, by an isotropic etch. Each remaining portion of the deposited conductive material in the first backside recesses **43** constitutes a first electrically conductive layer **46**. Each remaining portion of the deposited conductive material in the second backside recesses **143** constitutes a second electrically conductive layer **146**. Each electrically conductive layer (**46**, **146**) can be a conductive line structure.

[0137] Each first electrically conductive layer **46** can function as a combination of a plurality of control gate electrodes and a word line electrically connecting, i.e., electrically shorting, the plurality of control gate electrodes. The plurality of control gate electrodes within each first electrically conductive layer **46** can include control gate electrodes located at the same level for the vertical memory devices including the memory stack structures **55**. In other words, each first electrically conductive layer **46** can be a word line that functions as a common control gate electrode for the plurality of vertical memory devices.

[0138] A patterned stack comprising an alternating plurality of the first material layers (i.e., the insulator layers **32**) and second electrically conductive layers **146** is formed in the capacitor region **400**. The second electrically conductive layers **146** in the patterned stack (**32**, **146**) are formed at each level of the second material layers (i.e., the sacrificial material layers **42**).

[0139] Referring to FIGS. **11**A-**11**B, a dielectric material can be conformally deposited within the backside contact trench **79** and the lateral separation trenches **89**. The dielectric material can include, for example, silicon oxide, silicon nitride, a dielectric metal oxide, or a combination thereof. In one embodiment, the dielectric material can comprise silicon oxide.

[0140] In one embodiment, the lateral separation trenches **89** can be completely filled with the dielectric material to form trench fill dielectric material portions **84**, while the backside contact trench **79** is not completely filled with the dielectric material. In other words, a backside cavity can be present within the portions of the deposited dielectric material within the backside contact trench **79**.

[0141] An anisotropic etch can be performed to remove horizontal portions of the deposited dielectric material from above the dielectric material layer **73**. A contiguous remaining vertical portion of the deposited dielectric material within the backside contact trench **79** constitutes an insulating spacer **74**. The insulating spacer **74** comprises the same dielectric material as the form trench fill dielectric material portions **84**. In one embodiment, the trench fill dielectric material portions **84** can have a same width throughout, and the insulating spacer **74** has a lateral thickness, as measured on the sidewalls of the backside contact trench **79**, that is greater than one half of the width of the trench fill dielectric material portions **84**. A remaining annular portion of the sacrificial dielectric portions **616** can be incorporated into a bottom portion of the insulating spacer **74**.

[0142] Electrical dopants (p-type dopants or n-type dopants) can be implanted into portions of the semiconductor material layer **10** that underlies the backside cavity within the backside contact trench **79**. In one embodiment, the conductivity type of the implanted dopants can be the opposite of the conductivity type of the semiconductor material layer **10**. The implanted portion of the semiconductor material layer **10** can function as a source region **61** for the memory stack structures **55**, and a surface portion of the semiconductor material layer **10** between the source region **61** and the epitaxial channel portions **66** can be a horizontal channel portion. In one embodiment, the semiconductor material layer **10** can have a doping of a first conductivity type, and the source region **61** can have a doping of a second conductivity type that is the opposite of the first conductivity type.

[0143] The backside cavity surrounded by an insulating spacer **74** can be filled with a conductive material to form a backside contact via structure **76**. The backside contact via structure **76** can be electrically shorted to a portion of the substrate (**10**, **61**), which can be the source region **61**. The backside contact via strcuture **76** extends through, and is laterally surrounded by, the insulating spacer **74**.

[0144] The patterned stack comprising an alternating plurality of the first material layers (i.e., the insulator layers **32**) and second electrically conductive layers **146** in the capacitor region **400** is laterally contacted by dielectric material fill portions on all sides. Specifically, the patterned stack (**32**, **146**) is laterally contacted by a set of dielectric fill material portions (**7**P, **84**, **65**) formed within trenches. In one embodiment, each trench laterally surrounding an alternating stack of insulator layers **32** and the second electrically conductive layers **146** can be filled with a dielectric fill material. The trench including a dielectric pillar structure **7**P and contact-

ing a sidewall of the alternating stack (**32**, **146**) can be filled with a first dielectric fill material. Two lateral separation trenches **89** including the trench fill dielectric material portions **84** and contacting a pair of sidewalls of the alternating stack (**32**, **146**) can be filled with a second dielectric material. The pair of sidewalls of the alternating stack (**32**, **146**) can be substantially parallel to each other. The retro-stepped cavity including the retro-stepped dielectric material portion **65** and contacting stepped surfaces of the alternating stack (**32**, **146**) includes another dielectric fill material.

[0145] Referring to FIGS. **12**A-**12**D, a photoresist layer (not shown) is applied over the dielectric material layer **73**, and is lithographically patterned to form openings in regions in which formation of additional contact via structures is desired. The pattern in the photoresist layer is transferred through the dielectric material layer **73**, the insulating cap layer **71**, and the retro-stepped dielectric material portion **65** to form various vertically-extending cavities. The anisotropic etch can be selective to the materials of the electrically conductive layers (**46**, **146**) and the drain region **63**, and optionally to additional materials within the memory stack structures **55**. A first subset of the vertically-extending cavities (not shown) can extend to stepped surfaces (not shown) of the first electrically conductive layers **46** adjacent to the memory device region **100**. A second subset of the vertically-extending cavities (subsequently filled with capacitor contact via structures **8**C) can extend to stepped surfaces of the second electrically conductive layers **146** in the capacitor region **400**. Another subset of the vertically-extending cavities (subsequently filled with drain contact via structures **88**) can extend to top surfaces of the drain regions **63**. The photoresist layer can be removed, for example, by ashing.

[0146] At least one conductive material is deposited in the vertically-extending cavities to fill each of the vertically-extending cavities. Excess portions of the at least one conductive material can be removed from above a horizontal plane including a top surface of the dielectric material layer **73**, for example, by chemical mechanical planarization (CMP). Each remaining portion of the at least one conductive material constitutes a contact via structure (**8**C, **88**), which include capacitor contact via structures **8**C formed in the capacitor region **400**, drain contact via structures **88** formed in the memory device region **100**, and control gate contact via structures (not shown) that are formed in a stepped surface region (not shown) adjacent to the memory device region **100**.

[0147] A plurality of contact via structures (i.e., the capacitor contact via structures **8**C) is formed on the second electrically conductive layers **146** in the capacitor region **400**. An additional plurality of contact via structures (i.e., the control gate contact via structures) is formed on the first electrically conductive layers **46** adjacent to the memory device region **100**, as will be described below with respect to FIG. **14**X.

[0148] In one embodiment, the capacitor contact via structures **8**C can be arranged to facilitate pairwise connection between upper second electrically conductive layers **146** (i.e., second electrically conductive layers **146** located within an upper half of the alternating stack (**32**, **146**)) and lower second electrically conductive layers **146** (i.e., second electrically conductive layers **146** located within a lower half of the alternating stack (**32**, **146**)) through line level interconnect structures to be subsequently formed over the dielectric material layer **73**. For example, capacitor contact via structures **8**C to be electrically shorted by overlying interconnect line structures (such as metal line structures) can be formed along the second horizontal direction hd**2**, which is parallel to the lengthwise direction of the trench fill dielectric material portions **84**.

[0149] As shown in FIGS. **13**A-**13**E, a line level dielectric material layer **92** including a dielectric material can be formed over the top surface of the dielectric material layer **73**. The dielectric material of the line level dielectric material layer **92** can be, for example, silicon oxide, silicon nitride, organosilicate glass, or a combination thereof. Interconnect line structures can be formed in the line level dielectric material layer **92**, for example, by forming line trenches in the line level dielectric material layer **92** and filling the line trenches with at least one conductive material. Excess portions of the at least one conductive material can be removed from above the top surface of the line level dielectric material layer **92**, for example, by chemical mechanical planarization.

[0150] Node-tying metal lines (**821**, **822**, **823**, **831**, **832**, **833**), source metal line **96**, and bit lines **98** (only portions of the word lines are shown for clarity) can be formed in the line level dielectric material layer **92**. The node-tying metal lines (**821**, **822**, **823**, **831**, **832**, **833**) tie, i.e., electrically short, the same node of capacitor structures. The node-tying metal lines (**821**, **822**, **823**, **831**, **832**, **833**) can include first node-tying metal lines (**821**, **822**, **823**) that tie the first node of a respective capacitor, and second node-tying metal lines (**831**, **832**, **833**) that tie the second node of a respective capacitor. The source metal line **96** provides electrical connection to the backside contact via structure **76** and the source region **61**. The bit lines **98** provide electrical connection to the drain contact via structures **88** and the drain regions **63**.

[0151] The second electrically conductive layers **146** constitute capacitor electrodes (e.g., plates) of a set of capacitors. Each capacitor plate is a conductive component of the set of capacitors. A subset of the electrically insulating layers **32** within the capacitor region **400** constitutes node dielectrics of the set of capacitors. Each capacitor in the set comprises a first node that includes an underlying second electrically conductive layer (**146**U**1** or **146**U**2**) (which is one of the second electrically conductive layers **146**) of a respective vertically neighboring pair and a respective contact via structure (**8**CU**1** or **8**CU**2**) that extends upward from the underlying second electrically conductive layer (**146**U**1** or **146**U**2**) and through the retro-stepped dielectric material portion **65**. Each capacitor in the set further comprises a second node that includes an overlying second electrically conductive layer (**146**O**1** or **146**O**2**) (which is one of the second electrically conductive layers **146**) of the respective vertically neighboring pair and a respective contact via structure (**8**CO**1** or **8**CO**2**) that extends upward from the overlying electrically conductive layer (**146**O**1** or **146**O**2**) and through the retro-stepped dielectric material portion **65**.

[0152] In one embodiment, each capacitor within the set of capacitors can comprises two pairs of vertically neighboring electrically conductive layers (**146**U**1**, **146**O**1**) and (**146**U**2**, **146**O**2**) such that the first node of the capacitor includes an underlying electrically conductive layer **146**U**1** of a first vertically neighboring pair (**146**U**1**, **146**O**1**) and an electrically conductive layer **146**U**2** of a second vertically neighboring pair (**146**U**2**, **146**O**2**); and the second node of

the capacitor includes an overlying electrically conductive layer **146**O**1** of the vertically neighboring pair (**146**U**1**, **146**O**1**) and another electrically conductive layer **146**O**2** of the second vertically neighboring pair (**146**U**2**, **146**O**2**).

[0153] In case the horizontal steps (i.e., the horizontal surface portions) of the stepped surfaces of the alternating stack (**32**, **146**) has a uniform width, upper vertically neighboring pairs of second electrically conductive layers **146** (located in the upper half of the alternating stack (**32**, **146**)) and lower vertically neighboring pairs (located in the lower half of the alternating stack (**32**, **146**)) of second electrically conductive layers **146** can be matches such that each set of an upper vertically neighboring pair of second electrically conductive layers **146** and a lower vertically neighboring pair of the second electrically conductive layers **146** has a same total overlap area between neighboring pairs of second electrically conductive layers **146**. If the insulator layers **32** have the same thickness throughout, the capacitance of each capacitor can be the same. If the alternating stack (**32**, **146**) in the capacitor region includes a total of N second electrically conductive layers **146**, the total number of capacitors including an upper vertically neighboring pair of second electrically conductive layers **146** and a lower vertically neighboring pair of the second electrically conductive layers **146** can be a positive integer that does not exceed N/4.

[0154] Alternatively, tying of the nodes of two pairs of vertically neighboring second electrically conductive layers **146** can be omitted. In this case, each capacitor can consist of a single vertically neighboring pair of second electrically conductive layers **146**.

[0155] The first exemplary structure can include a device comprising a set of capacitors. The set of capacitors can comprise: a stack of alternating layers (**32**, **146**) including electrically insulating layers **32** and electrically conductive layers **146** and located over a substrate **10**. Each electrically conductive layer **146** that is located within the stack (**32**, **146**), and has at least one overlying electrically conductive layer **146** which laterally extends farther than any overlying electrically conductive layer **146**. The set of capacitors includes a dielectric material portion **65** located over the stepped surface region of the stack (**32**, **146**). An interface between the dielectric material portion **65** and the stack (**32**, **146**) includes a contiguous set of horizontal surfaces and vertical surfaces to provide the stepped surface region. The device comprises a set of dielectric fill material portions (**84**, **7**P) are located within trenches that vertically extend through the stack (**32**, **146**) of alternating layers and laterally contacts sidewalls of the stack (**32**, **146**) of alternating layers. The device comprises a plurality of capacitor contact via structures **8**C in contact with respective electrically conductive layers **146** within the stack (**32**, **146**) of alternating layers. The electrically conductive layers **146** constitute conductive components of a set of capacitors and a subset of the electrically insulating layers **32** constitutes node dielectrics of the set of capacitors. Only the electrically insulating layers **32** located between a first node and a second node of a capacitor constitutes the node dielectrics. Each capacitor in the set comprises: a first node that includes an underlying electrically conductive layer **146**U**1** (or alternatively **146**U**2**) of a respective vertically neighboring pair and a respective capacitor contact via structure **8**CU**1** (or alternatively **8**CU**2**) that extends upward from the underlying electrically conductive layer **146**U**1** and through the dielectric material portion **65**; and a second node that includes an overlying electrically conductive layer **146**O**1** (or alternatively **146**O**2**) of the respective vertically neighboring pair and a respective capacitor contact via structure **8**CO**1** (or alternatively **8**CO**2**) that extends upward from the overlying electrically conductive layer **146**O**1** and through the dielectric material portion **65**.

[0156] In one embodiment, each of the trenches (i.e., the lateral separation trenches **89** and optionally the trench in which the dielectric pillar structure **7**P is present, or trenches **89**A, **89**B described below with respect to FIGS. **14**A-**14**X) can be entirely filled with a dielectric material of a respective dielectric fill material portion (**84**, and optionally **7**P). In one embodiment, all sidewall surfaces of the electrically conductive layers **146** within the stack of alternating layers (**32**, **146**) can be in contact with a surface selected from sidewall surfaces of the set of dielectric fill material portions (**84**, and optionally **7**P) and sidewall surfaces of the dielectric material portion **65**.

[0157] In one embodiment, the entire interface between an electrically conductive layer **146** within the stack (**32**, **146**) of alternating layers and the set of dielectric fill material portions (**84**, and optionally **7**P) can be a contiguous interface, and can be vertical or tapered. In one embodiment, the contiguous interface can be substantially vertical throughout an entirety thereof. As used herein, a surface is substantially vertical if the surface is vertical or a taper angle of the surface with respect to a vertical direction does not exceed 3 degrees. In one embodiment, the interface between the electrically conductive layer **146** and the set of dielectric fill material portions (**84**, and optionally **7**P) adjoins an interface between the electrically conductive layer **146** and the dielectric material portion **65** (which is located within a subset of the stepped surfaces in the stepped surface region). In one embodiment, the combination of the interface between the electrically conductive layer **146** and the set of dielectric fill material portions (**84**, and optionally **7**P) and the interface between the electrically conductive layer **146** and the dielectric material portion **65** includes all sidewall surfaces of the electrically conductive layer **146**.

[0158] In one embodiment, the set of dielectric fill material portions (**84**, and optionally **7**P) can be a contiguous (i.e., physically adjoined) set of material portions and contact the dielectric material portion **65**. In one embodiment, the dielectric material portion **65** can be a retro-stepped dielectric material portion in which a horizontal cross-sectional area of the dielectric material portion **65** at a horizontal plane is not less than a horizontal cross-sectional area of the dielectric material portion at any horizontal plane that is more proximal to the substrate **10**.

[0159] In one embodiment, each capacitor within the set of capacitors comprises two pairs of vertically neighboring electrically conductive layers (**146**U**1**, **146**O**1**) and (**146**U**2**, **146**O**2**). The first node of the capacitor includes an underlying electrically conductive layer **146**U**1** of a first vertically neighboring pair (**146**U**1**, **146**O**1**) and an electrically conductive layer (**146**U**2** or **146**O**2**) of a second vertically neighboring pair (**146**U**2**, **146**O**2**). The second node of the capacitor includes an overlying electrically conductive layer **146**O**1** of the first vertically neighboring pair (**146**U**1**, **146**O**1**) and another electrically conductive layer (**146**U**2** or **146**O**2**) of the second vertically neighboring pair (**146**U**2**, **146**O**2**).

[0160] In one embodiment, the underlying electrically conductive layer **146**U**1** of the first vertically neighboring

pair (**146**U**1**, **146**O**1**) and the electrically conductive layer (**146**U**2** or **146**O**2**) of the second vertically neighboring pair (**146**U**2**, **146**O**2**) are electrically shorted through two contact via structures (for example, **8**CU**1** and **8**CU**2**) and a first conductive line structure (for example, **833**). The overlying electrically conductive layer **146**O**1** of the first vertically neighboring pair (**146**U**1**, **146**O**1**) and the other electrically conductive layer of the second vertically neighboring pair (**146**U**2**, **146**O**2**) are electrically shorted through two additional contact via structures (for example, **8**CO**1** and **8**CO**2**) and a second conductive line structure (for example, **823**).

[0161] In one embodiment, the set of capacitors comprise at least a first capacitor and a second capacitor. In this case, the first capacitor can comprise a first upper pair of vertically neighboring electrically conductive layers (e.g., **146**U**2** and **146**O**2**) and a first lower pair of vertically neighboring electrically conductive layers (e.g., **146**U**1** and **146**O**1**). The second capacitor can comprise a second upper pair of vertically neighboring electrically conductive layers (located within an upper half of the alternating stack and at different levels than the first upper pair of vertically neighboring electrically conductive layers) and a second lower pair of vertically neighboring electrically conductive layers (located within a lower half of the alternating stack and at different levels than the first lower pair of vertically neighboring electrically conductive layers). In one embodiment, the second upper pair of vertically neighboring electrically conductive layers **146** overlies the first upper pair of vertically neighboring electrically conductive layers **146**; the first upper pair of vertically neighboring electrically conductive layers **146** overlies the first lower pair of vertically neighboring electrically conductive layers **146**; and the first lower pair of vertically neighboring electrically conductive layers **146** overlies the second lower pair of vertically neighboring electrically conductive layers **146**.

[0162] In one embodiment, the capacitors can be configured to provide the same capacitance for each capacitor. Such a configuration can be obtained by forming pairs of vertically neighboring electrically conductive layers **146**, and providing parallel connection for a pair of component capacitors. The first component capacitor is formed by a node dielectric employing an insulator layer **32** within the lower half of the alternating stack (**32**, **146**) and two neighboring electrically conductive layers **146**. The second component capacitor is formed by a node dielectric employing an insulator layer within the upper half of the alternating stack (**32**, **146**) and two neighboring electrically conductive layers **146**. The two component capacitors are connected in parallel such that the total capacitance is the same as the target capacitance for the capacitor formed by the parallel connection of the two component capacitors. By selecting the pairs of component capacitors for parallel connection, multiple capacitors having the same total capacitance can be formed.

[0163] In one embodiment, the thickness of the insulator layers **32** can be the same throughout, and the sum of an upper overlap area between the vertically neighboring electrically conductive layers (**146**U**2**, **146**O**2**) within the first upper pair (of a first capacitor) and a lower overlap area between the vertically neighboring electrically conductive layers (**146**U**1**, **146**O**2**) within the first lower pair (of the first capacitor) can be substantially the same as the sum of an upper overlap area between the vertically neighboring electrically conductive layers within the second upper pair (of the second capacitor) and a lower overlap area between the vertically neighboring electrically conductive layers within the second lower pair (of the second capacitor). In this case, the first capacitor and the second capacitor can have the same total capacitance. In one embodiment, each capacitor within the set of capacitors can have a substantially same total overlap area between vertically neighboring electrically conductive layers contained therein.

[0164] In one embodiment, the device can further comprise a monolithic three-dimensional memory device located on the substrate **10** and in the memory device region **100**. The monolithic three-dimensional memory device can comprise a memory opening **49** extending through the stack (**32**, **46**); a memory film **55** located within the memory opening **49**; and a semiconductor channel (**601**, **602** and optionally **66**) located within the memory film **55**.

[0165] In one embodiment, the set of capacitors can be a component of a peripheral device of the monolithic three-dimensional memory device; the monolithic three-dimensional memory device can be a vertical NAND memory device; the electrically conductive layers **46** comprise, or are electrically connected to, a respective word line of the vertical NAND memory device; and the substrate comprises a silicon substrate. In one embodiment, the vertical NAND memory device can comprise an array of monolithic three-dimensional NAND strings over the silicon substrate; at least one memory cell in the first device level of the three-dimensional array of NAND strings can be located over another memory cell in the second device level of the three-dimensional array of NAND strings; and the silicon substrate can contain an integrated circuit comprising a driver circuit for the memory device located thereon. The three-dimensional array of NAND strings can comprise: a plurality of semiconductor channels (**601**, **602**, and optionally **66**, and portions of **10**), wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the silicon substrate; a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the silicon substrate. The plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

[0166] FIG. **14**A illustrates a schematic top down view of a device of embodiments of the invention. As shown in FIG. **14**A, the capacitor region **400** is located in the stepped surface region of the stack between the sense amplifiers **402** and other bit line peripheral devices **404** (e.g., devices of the driver circuit, such as charge pump circuit devices, reference voltage and current circuit, and/pr power-on circuit, etc.) and the memory device region **100** (also referred to as the cell array) in direction hd**2** (i.e., the bit line direction). The capacitor region **400** is also referred to as a dummy staircase region because it includes the stepped surface without word line contact vias (i.e., control gate interconnects). The dummy staircase region is formed at the same time during the same etching steps as the word line stepped surface regions **300** (labeled WLHU staircase) in which the word line contact vias (i.e., control gate interconnects) will be formed during a subsequent step. In other words, the stepped surface regions are formed on plural (e.g., all) sides of the