

elevated memory device region. For a rectangular memory device region 100, the word line stepped surface regions 300 are formed on two opposing sides of the memory device region 100 such that word lines will eventually extend in the word line direction hd1 between opposing regions 300. The word line and select gate switching transistors are located in row decoder regions 302 (labeled WL/SG SW) adjacent to regions 300 in direction hd1.

[0167] The remaining two sides of the memory device region 100 contain the dummy staircase regions. The capacitors are formed in the dummy staircase capacitor region 400 located adjacent to the sense amplifier region 402. Thus, the size of the sense amplifier region 402 may be reduced by over 10%, such as about 20% by omitting the capacitors from region 402 and instead forming the capacitors in region 400 which is an unused dummy region in prior art devices.

[0168] The memory device region 100 contains the memory stack structures 55 and the support pillars (e.g., dielectric pillar structures) 7P, similar to that shown in FIG. 5A. However, in the embodiment of FIG. 14A, the support pillars 7P comprise cylindrical pillars instead of or in addition to the elongated dielectric pillar structures 7P shown in FIG. 6B. It should be understood that only a few of the memory stack structures 55 and the support pillars 7P are shown for clarity. If desired, the dielectric support pillar structures 7Q (not shown for clarity) as described and illustrated above may also be present in the device of the embodiment of FIG. 14A.

[0169] The periphery of the device (e.g., the periphery of the substrate, such as portion of a semiconductor wafer or a diced chip) contains a dummy staircase track 406 and a kerf region 501 (e.g., having half width of the original dicing region if the substrate is diced into chips). The dummy staircase track 406 surrounds the device and contains a stepped surface region which is a mirror image of the stepped surface region of the dummy staircases 400. The track 406 is formed during the same patterning (e.g., etching) steps as the other stepped regions 300 and 400 in the device.

[0170] FIGS. 14B-14D illustrate an exemplary structure according to an alternative of the first embodiment. The structure is similar to the structure shown in FIGS. 6A-6B, except that the support pillars 7P comprise cylindrical pillars (shown in FIG. 14A) located in region 100. The structure of FIGS. 14B-14D contains the alternating stack (32, 42), the dielectric material layer 73 and the retro-stepped dielectric material portion 65 described above with respect to FIG. 6A.

[0171] FIGS. 14E-14G illustrate the next step in the process in which the lateral separation trenches 89A, 89B are formed in the stack (32, 42) at the same time as the backside contact trenches 79, similar to that shown in FIGS. 7A-7D (the backside contact trenches are not shown in FIGS. 14E-14G for compactness). As shown in FIG. 14E, the lateral separation trenches include first trenches 89A which extend in the bit line direction hd2, similar to trenches 89 shown in FIG. 7B. However, in this embodiment, the lateral separation trenches also include at least one second trench 89B which extend in the word line direction hd1, similar to the pillar 7P shown in FIG. 7B. The second trench 89B connects the end portions of the first trenches 89A near the end of the capacitor region 400 closest to the memory device region 100 and farthest from the stepped surface in region 400.

[0172] As shown in FIGS. 14H-14J, portions of sacrificial material layers 42 are selectively removed from the alternating stack in regions 100, 300 and 400 through the trenches 89A, 89B and the backside contact trenches 79, similar to that shown in FIGS. 8A-8C. However, unlike the prior embodiment shown in FIGS. 8A-8C, portions 42A of the sacrificial material layers 42 remain in the alternating stack near the end of the capacitor region 400 closest to the memory device region 100 and farthest from the stepped surface in region 400. Thus, each backside recess 143 abuts a portion 42A of the sacrificial material layers 42. These portions 42A (instead of the elongated pillar 7P in the prior embodiment) electrically insulate region 400 from region 100.

[0173] A plurality of first electrically conductive layers 46 (e.g., word lines/control gates which extend in the word line direction hd1) can be formed in the plurality of first backside recesses 43 in the memory device region 100 and in region 300, as described above with respect to FIGS. 9A-9B. As shown in FIGS. 14K-14M, a plurality of second electrically conductive layers 146 can be formed in the plurality of second backside recesses 143 at the same time as layers 46. A contiguous conductive material layer 46L can be formed on the sidewalls of the trenches 89A, 89B, the backside contact trenches 79 (as described above) and over the topmost layer of the structure. The layer 46L partially fills the trenches 89A, 89B to leave remaining trenches 89'.

[0174] Referring to FIGS. 14N-14P, the deposited conductive material of the contiguous conductive material layer 46L is etched back from the sidewalls of each backside contact trench 79, from the sidewalls of each lateral separation trenches 89', and from the dielectric material layer 73, similar to that described above with respect to FIGS. 10A-10B. This leaves electrically conductive layers 146 which function as capacitor electrodes in region 400 separated from each other by trenches 89A and 89B. The electrically conductive layers 146 between trench 89B in region 400 and region 100 are separated from electrically conductive layers 46 in region 100 by the remaining portions 42A (e.g., silicon nitride or other insulating material layer portions) of layers 42.

[0175] Referring to FIGS. 14Q-14S, the lateral separation trenches 89A, 89B can be completely filled with the dielectric material to form trench fill dielectric material portions 84, while the backside contact trenches 79 are not completely filled with the dielectric material, as described above with respect to FIGS. 11A-11B. The insulating spacer 74 can be formed in the backside contact trenches and filled with a conductive material to form a backside contact via structure 76 which extends in the word line direction hd1, as shown in FIG. 14X and as described above with respect to FIGS. 11A-11B.

[0176] As described above with respect to FIGS. 12A-12D, first subset of the vertically-extending cavities can extend to stepped surfaces of the first electrically conductive layers 46 in region 300 adjacent to the memory device region 100. A second subset of the vertically-extending cavities (subsequently filled with capacitor contact via structures 8C) can extend to stepped surfaces of the second electrically conductive layers 146 in the capacitor region 400. Another subset of the vertically-extending cavities (subsequently filled with drain contact via structures 88) can extend to top surfaces of the drain regions 63.

[0177] Referring to FIGS. 14T-14X, at least one conductive material is deposited in the vertically-extending cavities to fill each of the vertically-extending cavities with capacitor contact via structures 8C formed in the capacitor region 400, drain contact via structures 88 formed in the memory device region 100, and control gate contact via structures 304 that are formed in a stepped surface region 300 adjacent to the memory device region 100.

[0178] The portions 146A of the electrically conductive layers 146 that are electrically insulated from layers 46 by the trench fill dielectric material portions 84 and which are contacted by via structures 8C comprise capacitor electrodes. The portions 32A of the electrically insulating layers 32 in region 400 located between the capacitor electrodes 146A comprise capacitor dielectrics.

[0179] As shown in FIGS. 14U and 14W, a resulting capacitor 410 includes adjacent electrode plates 146A separated by an insulating layer 32A, and respective electrical contacts (e.g., capacitor contact via structures 8C) to the electrode plates 146A.

[0180] Thus, as shown in FIG. 14X, in the first embodiment and in the alternative embodiment described above, a three dimensional memory device (e.g., such as the NAND device) includes the memory device region 100 containing a plurality of non-volatile memory devices (e.g., the NAND strings), a peripheral device region 402/404 containing active driver circuit devices (e.g., transistors), and first stepped surface region 400 located between the peripheral device region 402/404 and the memory device region 100, and containing a plurality of passive driver circuit devices, such as capacitors 410 or resistors as will be described with respect to additional embodiments below. It should be noted that the peripheral device region 402/404, the dummy staircase track 406 and the kerf region 501 may also contain additional passive devices (e.g., capacitors or resistors) or it may contain no passive devices. Thus, the capacitors 410 may be located in dummy staircase track 406 if desired. Likewise, region 400 may also contain additional active devices (e.g., transistors) or it may contain no active devices.

[0181] As described above, the stack of alternating layers including electrically insulating layers 32 and electrically conductive layers (46, 146) located over the substrate 10. The first stepped surface region 400 contains first portions of the electrically insulating layers 32 and first portions of the electrically conductive layers 146, and the first stepped region 400 is located on a first side of the stack facing the peripheral region. The second stepped surface region 300 contains second portions of the electrically insulating layers 32 and second portions of the electrically conductive layers 46 located on a second side of the stack (e.g. at a side perpendicular to the first side).

[0182] As described above, a plurality of semiconductor channels 60 are located in the memory device region 100 in the stack, such that at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the substrate 10. A plurality of charge storage elements (i.e., portions of the memory films 50) are located adjacent to a respective one of the plurality of semiconductor channels 60. A plurality of passive device contact via structures (e.g., capacitor via structures 8C) extend extending substantially perpendicular to the top surface 7 of the substrate 10 to the respective first portions of the electrically conductive layers 146 in the first stepped surface region 400. A plurality of control gate

contact via structures 304 extend substantially perpendicular to the top surface 7 of the substrate 10 to the respective second portions of the electrically conductive layers 46 in the second stepped surface region 300.

[0183] The peripheral device region contains sense amplifiers in region 402. The second stepped surface region 300 comprises a word line stepped surface region 300. The second portions of the electrically conductive layers 46 comprise a plurality of control gate electrodes extending substantially parallel to the top surface of the substrate, and the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

[0184] In the above embodiments, the passive driver circuit devices comprise capacitors 410, and the first portions 146A of the electrically conductive layers 146 comprise a plurality of capacitor electrodes. The first portions of the electrically insulating layers 32 in region 400 comprise capacitor dielectrics located between the capacitor electrodes 146A. The respective first 146A and second 46 portions of each of the electrically conductive layer are located at the same level above the substrate and are electrically insulated from each other (e.g., by material 84 and/or optionally by pillar 7P).

[0185] As shown in FIG. 14Y, N/2 capacitors 410 may be formed from N layers 146 in the stack, where N is any integer greater than 1. However, as described above with respect to FIGS. 13A-13D, layers 146 at the top of the stack are shorter than layers 146 at the bottom of the stack. This causes the capacitors to be of unequal size.

[0186] FIG. 14Z illustrates a capacitor interconnection configuration similar to that of FIGS. 13A-13D, where the longest layer 146 is electrically connected by interconnect (e.g., metal line) 833 to the second shortest layer 146 in the stack to form one capacitor electrode. The next longest layer 146 in the stack is electrically connected by interconnect (e.g., metal line 823) to the shortest layer 146 in the stack to form another capacitor electrode. The remaining layers 146 in the stack may be connected in a similar way. This results in a capacitor 410A having two overlying layers 146 of different length connected to each other to form an overlying electrode and two underlying layers 146 of different length connected to each other to form an underlying electrode, where the average electrode length of all capacitors in the stack is about the same. This results in N/4 capacitors in a stack containing N layers 146.

[0187] In a second exemplary structure according to a second embodiment of the present disclosure the passive device of the driver circuit comprises a pillar shaped resistor. Referring to FIG. 15A, a substrate includes a semiconductor material layer 10 having a major surface 7. A doped semiconductor well 110 can be formed in a device region, which is herein referred to as a resistor region 500. The resistor region 500 may be located in a portion of the memory device region 100, as shown in FIG. 37. A memory device region 100 and a capacitor region 400 can be provided for formation of the devices illustrated in the first embodiment. The semiconductor material layer 10 can have a doping of a first conductivity type (which can be p-type or n-type), and the doped semiconductor well 110 can have a doping of a second conductivity type which is the opposite of the first conductivity type. In one embodiment, the concentration of electrical dopants (which can be p-type dopants or n-type

dopants) in the doped semiconductor well 110 can be in a range from $1.0 \times 10^{17}/\text{cm}^3$ to $2.0 \times 10^{21}/\text{cm}^3$, although lesser and greater dopant concentrations can also be employed. In one embodiment, the doped semiconductor well 110 can include a conductive (e.g., degenerately doped semiconductor or metallic) material rather than a semiconductor material, i.e., a material having electrical conductivity greater than 1.0×10^5 S/cm. The doped semiconductor well 110 is a laterally-extending semiconductor or conductive structure, and can consist of at least one single crystalline semiconductor material portion having a doping of the second conductivity type (e.g., n-type well) and located in the substrate 10 (e.g., p-type substrate or substrate well). Optionally, a doped contact region 112 can be formed, which has a doping of the same conductivity type (e.g., n-type) as the doped semiconductor well 110 and has a greater dopant concentration than the doped semiconductor well 110 (e.g., N+ well). Optionally, shallow trench isolation structures 120 including at least one dielectric material can be formed at a periphery of the doped semiconductor well 110 for device isolation.

[0188] Referring to FIG. 15B, the processing steps of FIG. 1 are performed to form a stack (32, 42) of alternating layers including the first material layers 32 and the second material layers 42.

[0189] Referring to FIG. 16, memory openings 49 are formed in the memory device region 100 and at least one resistor opening 249 can be formed in the resistor region 500. The memory openings 49 and the at least one resistor opening 249 can be formed simultaneously employing the same processing steps employed to form the memory openings of the first embodiment. The size of each resistor opening 249 may be the same as, or may be different from, the size of the memory openings 49. If a plurality of resistor openings 249 is formed, the resistor openings 249 can have the same size, or can have different size. The size of the resistor openings 249 can be adjusted depending on the target resistance of a resistor to be subsequently formed. In one embodiment, the resistance of a resistor to be formed in a resistor opening 249 is generally inversely proportional to the diameter (or a lateral dimension if a non-circular cross-sectional shape is employed) of the resistor opening 249. The bottom of each resistor opening 249 can extend to a top surface of the doped semiconductor well 110.

[0190] Each resistor opening 249 is a vertically-extending cavity that extends from a first horizontal plane including a top surface of the alternating stack (32, 42) to the laterally-extending semiconductor or conductive structure of the combination of the doped semiconductor well 110 and the doped contact region 112. A physically exposed portion of the top surface of the laterally-extending semiconductor or conductive structure (i.e., the doped semiconductor well 110) is present within a second horizontal plane located underneath, and vertically spaced by a plurality of layers within the alternating stack (32, 42) from, the top surface of the alternating stack (32, 42). The second horizontal plane is the plane including the bottom surface of each resistor opening 249, which is the recessed, or non-recessed, top surface of the doped semiconductor well 110.

[0191] Referring to FIG. 17, the processing steps of FIG. 2 of the first embodiment can be performed to form memory stack structures 55 and at least one pillar structure 155 simultaneously. The memory stack structures 55 are formed in the memory openings 49 in the memory device region

100, and a pillar structure 155 is formed in each resistor opening 249 in the resistor region 500. Each pillar structure 155 can have the same set of components as a memory stack structure 55 and which are formed during the same formation (e.g., deposition) steps. Each component within a pillar structure 155 can have the same composition as the corresponding component (having the same reference numeral) within a memory stack structure 155. Each component within a pillar structure 155 can have the same height as the corresponding component within a memory stack structure 155. Except for an epitaxial channel portion 66 and a dielectric core 62, each component within a pillar structure 155 can have the same lateral dimension (such as a lateral thickness) as the corresponding component within a memory stack structure 155. If a horizontal cross-sectional shape of a pillar structure 155 is different from a horizontal cross-sectional shape of a memory stack structure 55 taken at a same vertical distance from the top surface of the substrate (10, 110, 112, 12), the epitaxial channel portion 66 and the dielectric core 62 within the pillar structure 155 can have different dimensions than the corresponding dimensions of a memory stack structure 55. If a horizontal cross-sectional shape of a pillar structure 155 is the same as a horizontal cross-sectional shape of a memory stack structure 55 taken at a same vertical distance from the top surface of the substrate (10, 110, 112, 12), the epitaxial channel portion 66 and the dielectric core 62 within the pillar structure 155 can have the same dimensions as the epitaxial channel portion 66 and the dielectric core 62 within the memory stack structure 55.

[0192] A pillar structure 155 is formed within each resistor opening 249. A semiconductor channel (601, 602) is formed on each optional epitaxial channel portion 66, which is a single crystalline semiconductor material portion and is intrinsic or has a doping of the first conductivity type. The single crystalline semiconductor material portion in the resistor opening 249 (as embodied as an epitaxial channel portion 66 in the resistor opening 249) is formed simultaneously with formation of the epitaxial channel portions 66 in the memory openings 49. The first conductivity type is the conductivity type of the semiconductor material layer 10, and is the opposite of the conductivity type of the doped semiconductor well 110 (which has a doping of the second conductivity type). The memory films 50 in the memory stack structures 55 and the at least one pillar structure 155 can be a layer stack of dielectric material layers as described above, i.e., a stack of a blocking dielectric layer, a memory material layer, and a tunneling dielectric layer.

[0193] Each semiconductor channel (601, 602) in the memory openings 49 and the at least one resistor opening 249 can be formed by deposition of an intrinsic semiconductor material or a semiconductor material of the first conductivity type. The semiconductor channels (601, 602) can include a polycrystalline semiconductor material or an amorphous semiconductor material. A vertically-extending semiconductor material portion in each resistor opening 249 (as embodied in a semiconductor channel (601, 602) in the resistor opening 249) is formed simultaneously with formation of the semiconductor channels (601, 602) in the memory openings 49.

[0194] Each drain region 63 formed in the at least one resistor opening 249 is a doped semiconductor material portion, and is formed with a doping of the second conductivity type. The drain regions 63 of the memory stack

structures 55 and each drain region 63 of the pillar structure 155 can be formed simultaneously.

[0195] Referring to FIG. 18, a photoresist layer 67 is applied over the second exemplary structure, and is lithographically patterned to form openings in the resistor region 500. Specifically, an opening in the photoresist layer 67 is formed in an area including the at least one pillar structure 155 by patterning the photoresist layer 67. In one embodiment, the thickness of the photoresist layer 67 can be selected such that electrical dopants to be subsequently implanted into the at least one pillar structure 155 can be implanted to the bottommost portion of the at least one pillar structure 155, while the electrical dopants are not implanted into any portion of the memory stack structures 55 in the memory device region 100. In one embodiment, the thickness of the photoresist layer 67 can be greater than the thickness of the alternating stack (32, 42).

[0196] Electrical dopants of the second conductivity type (e.g., n-type) can be implanted into the vertically-extending semiconductor material portion (embodied as a semiconductor channel (601, 602)) in each pillar structure 155, while implantation of the electrical dopants of the second conductivity type into the semiconductor channels (601, 602) of the memory stack structures 55 is prevented by the presence of the patterned photoresist layer 67. All semiconductor material portions in the pillar structure 155 can be doped with the implanted dopants of the second conductivity type. The dose of the implanted dopants of the second conductivity type is selected such that all semiconductor material portions are doped in the pillar structure 155.

[0197] The implantation of the electrical dopants of the second conductivity type converts each epitaxial semiconductor channel 66 (which is intrinsic or has a doping of the first conductivity type as formed) in the at least one pillar structure 155 into a epitaxial doped semiconductor portion 166 having a doping of the second conductivity type. Further, the implantation of the electrical dopants of the second conductivity type converts each semiconductor channel (601, 601) in the at least one resistor opening 249 into a vertically-extending doped semiconductor portion, which is herein referred to as a first doped semiconductor portion 160. Each epitaxial doped semiconductor portion 166 and each first doped semiconductor portion 160 are doped semiconductor material portions, and are formed by ion implantation of electrical dopants of the second conductivity type such that an atomic concentration of the dopants of the second conductivity type in a range from $1.0 \times 10^{17}/\text{cm}^3$ to $1.0 \times 10^{20}/\text{cm}^3$ therein. In one embodiment, all semiconductor material within each pillar structure 155 can have a doping of a same conductivity type, which is the second conductivity type.

[0198] An epitaxial doped semiconductor portion 166 is located at a bottom portion of each vertically-extending cavity (i.e., a resistor opening 249), and comprises the same semiconductor material as the epitaxial channel portions 66 of the memory stack structures 55. In one embodiment, each first doped semiconductor portion 160 can comprise a doped polycrystalline semiconductor material portion that is formed directly on inner surfaces of at least one electrically insulating material (i.e., the dielectric material of the memory film 50) within a respective resistor opening 249. Each drain region 63 within the at least one pillar structure 155 is herein referred to as a second doped semiconductor portion 163.

[0199] Referring to FIG. 19, the patterned photoresist layer 67 can be removed, for example, by ashing. A dielectric cap layer 71 can be formed employing the same method as in the first embodiment (as illustrated in FIG. 2).

[0200] Referring to FIG. 20, the processing steps of FIGS. 3, 4, 5A and 5B, 6A and 6B, and 7A-7C can be performed. Concurrently with formation of the backside contact trench 79 and optional formation of the lateral separation trenches 89 (See FIGS. 7B and 7C), a resistor contact trench 279 can be formed in an area overlying the doped contact region 112. The lateral separation trenches 89 may be omitted if the capacitor structures of the first embodiment are not to be formed.

[0201] The processing steps of FIGS. 8A-8C, 9A and 9B, and 10A and 10B can be subsequently performed to form first electrically conductive layers 46 in the memory device region 100, second electrically conductive layers 146 in the capacitor region 400, and third electrically conductive layers 246 in the resistor region 500. During the processing steps of FIGS. 8A-8C, portions of the sacrificial material layers 42 in the resistor region 500 can be removed by introduction of the etchant through the resistor contact trench 279 to form third backside recesses in each space from which the sacrificial material layers 42 are removed from the resistor region 500. The third electrically conductive layers 246 are formed in the third backside recesses by deposition of the same material as the first and second electrically conductive layers (46, 146) in the same processing step. The contiguous conductive material layer 46L can be deposited on the sidewalls of the resistor contact trench 279, and is subsequently removed from the sidewalls of the resistor contact trench 279 during the processing steps of FIGS. 10A and 10B.

[0202] Referring to FIG. 21, the processing steps of FIGS. 11A and 11B can be performed to form an insulating spacer 274 in each resistor contact trench 279 concurrently with formation of the insulating spacer 74 in the backside contact trench 79. The insulating spacer 274 in the resistor region 500 can have the same composition as, and the same lateral thickness as, the insulating spacer 74 in the memory device region 100. A substrate contact via structure 276 can be formed in the cavity extending through the insulating spacer 274 in the resistor region 500. The substrate contact via structure 276 in the resistor region 500 can be formed concurrently with formation of the backside contact via structure 76 in the memory device region 100. The substrate contact via structure 276 is a contact via structure that conducts a top surface of a laterally-extending semiconductor or conductive structure (which is a combination of the doped semiconductor well 110 and the doped contact region 112). In one embodiment, the backside contact via structure 76 and the substrate contact via structure 276 can be formed by deposition of a metallic material.

[0203] Referring to FIG. 22, the processing steps of FIGS. 12A-12D can be sequentially performed to form various contact via structures (8C, 88), which can include the capacitor contact via structures 8C, the control gate contact via structures 304, and the drain contact via structures 88. A pillar contact via structure 850 can be formed on a top surface of each pillar structure 155 concurrently with formation of other via contact structures such as the drain contact via structures 88. In one embodiment, as many pillar contact via structures 850 can be formed as the number of pillar structures 155. The pillar structures 850 can be formed

in the same processing step as, and can have the same composition as, the drain contact via structures 88. Optionally, the pillar contact via structures 850, the capacitor contact via structures 8C, the control gate contact via structures 304, and the drain contact via structures 88 can be formed employing a same set of processing steps, and can comprise a same set of conductive materials.

[0204] Subsequently, the processing steps of FIGS. 13A-13E can be performed to form a line level dielectric material layer 92 and various interconnect line structures therein. The interconnect line structures formed in the line level dielectric material layer 92 can include, for example, node-tying metal lines (821, 822, 823, 831, 832, 833), source metal line 96, and bit lines 98 as illustrated in FIGS. 13A-13E, and additionally include a first resistor node metal line 851 contacting the pillar contact structures 850 and a second resistor node metal liner 852 contacting the substrate contact via structure 276.

[0205] The second exemplary structure can comprise a semiconductor device. The semiconductor device can comprise an alternating stack (32, 246) of first material layers 32 and second material layers 246 located over a substrate (10, 110, 112, 120). The semiconductor device can further comprise at least one pillar structure 155 extending from a first horizontal plane including a top surface of the alternating stack (32, 246) to a second horizontal plane located underneath, and vertically spaced by a plurality of layers (such as the first material layers 32 and the second material layers 246) within the alternating stack (32, 246) from, the top surface of the alternating stack (32, 246). The semiconductor device further comprises a laterally-extending semiconductor or conductive structure (110, 112) contacting a bottom surface of the at least one pillar structure 155; and a contact via structure 276 contacting a top surface of the laterally-extending semiconductor or conductive structure (110, 112) and laterally spaced from the at least one pillar structure 155. Each of the at least one pillar structure 155 comprises a set of at least one doped semiconductor material portion (160, 166, 63) therein. All semiconductor material within each of the at least one pillar structure 155 has a doping of a same conductivity type, which can be the second conductivity type. The contact via structure (as embodied in the substrate contact via structure 276) can comprise a metallic via structure.

[0206] In one embodiment, the at least one doped semiconductor material portion (160, 166, 63) comprises a doped polycrystalline semiconductor material portion 160 contacting inner surfaces of at least one electrically insulating material, which can be a memory film 50.

[0207] The semiconductor device can further include a memory opening extending between the first horizontal plane and another horizontal plane including a bottom surface of the alternating stack (32, 46), and a memory stack structure 55 that comprises a memory film 50 located within the memory opening, and a semiconductor channel (601, 602) located within the memory film 50. Each of the at least one pillar structure 155 comprises a layer stack of at least two dielectric material layers (i.e., a memory film 50) located on an outer sidewall of a respective set of at least one doped semiconductor material portion (160, 166, 63). The memory film 50 in a memory stack structure 55 and the layer stack 50 of at least two dielectric material layers in the pillar structure 155 comprise an identical set of dielectric materials.

[0208] A first doped semiconductor material portion (as embodied in a doped polycrystalline semiconductor material portion 160) within each set of at least one doped semiconductor material portion (160, 166, 63) comprises the same semiconductor material as the semiconductor channel (601, 602), and further includes electrical dopants of the second conductivity type.

[0209] In one embodiment, the semiconductor channel (601, 602) can be intrinsic, or can have a doping of an opposite conductivity type from the set of at least one doped semiconductor material portion (160, 166, 63), which has a doping of the second conductivity type.

[0210] In one embodiment, the memory stack structure 55 further comprises a drain region 63 having a doping of the second conductivity type. A second doped semiconductor material portion, as embodied as a drain region 63, can be present within each set of at least one doped semiconductor material portion (160, 166, 63). The second doped semiconductor material portion 63 in each pillar structure 155 can comprise the same semiconductor material as the drain region 63 in the memory stack structure 55.

[0211] In one embodiment, the memory stack structure 55 further comprises an epitaxial channel portion 66 having a doping of the first conductivity type, and an epitaxial doped semiconductor portion 166 can be present within each set of at least one doped semiconductor material portion (160, 166, 63). The epitaxial doped semiconductor portion 166 comprises the same semiconductor material as the epitaxial channel portion 66, and further includes electrical dopants of the second conductivity type.

[0212] In one embodiment, the laterally-extending semiconductor or conductive structure (110, 112) consists of at least one single crystalline semiconductor material portion located in the substrate. In one embodiment, the laterally-extending semiconductor or conductive structure (110, 112) can consist of the doped semiconductor well 110 and the doped contact region 112, which have a doping of the second conductivity type.

[0213] In one embodiment, the first material layers 32 can be electrically insulating layers 32, and the second material layers (246, 46) can be electrically conductive layers. In one embodiment, the first material layers 32 comprise a first electrically insulating material, the second material layers (246, 46) comprise a second electrically insulating material, and the memory stack structure 55 extends through another alternating stack (32, 46) of the first material layers 32 and electrically conductive layers 46 located at each level of the second material layers (246, 46). In one embodiment, the set of at least one doped semiconductor material portion (160, 166, 63) comprises electrical dopants of the second conductivity type at an atomic concentration in a range from $1.0 \times 10^{17}/\text{cm}^3$ to $1.0 \times 10^{20}/\text{cm}^3$.

[0214] In one embodiment, the semiconductor structure can further include the vertical NAND memory device of the first embodiment.

[0215] Referring to FIG. 23, an alternate embodiment of the second exemplary structure can be derived from the second exemplary structure by forming a pillar contact via structure 850 that contacts a plurality of pillar structures 155 at the processing steps of FIG. 22.

[0216] In a third exemplary structure according to a third embodiment of the present disclosure the original insulating layers 42 are retained in the stack and are not replaced by the electrically conducting layers 246. Referring to FIG. 24, this

structure can be derived from the second exemplary structure of FIG. 19 by performing the processing steps of FIGS. 3, 4, 5A and 5B, and by forming the dielectric pillar structure(s) 7P and the dielectric material layer 73 employing the processing methods of FIGS. 6A and 6B. If desired, the dielectric support pillar structures 7Q (not shown for clarity) as described and illustrated above may also be present in the device of this embodiment. At least one pillar structure 155 can be formed in a resistor region 600, which can be a region that replaces the resistor region 500 of the second embodiment, or can be provided in addition to the resistor region 500 of the second embodiment. Regions 500 or 600 may be located in part of the memory device region 100 and/or in the kerf region 501, as shown in FIG. 37.

[0217] Subsequently, the processing steps of FIGS. 7A-7D, 8A-8C, 9A and 9B, 10A and 10B, and 11A and 11B are performed without forming the resistor contact trench 279 in the resistor region 600. If another resistor region 500 of the second embodiment is provided, a resistor contact trench 279 can be formed in such a resistor contact region 500.

[0218] In the third embodiment, first portions of second material layers 42 in the memory device region 100, an optional capacitor region 400, and an optional additional resistor region 500 are replaced with electrically conductive layers (46, 146, 246), while second portions of the second material layers 42 in the resistor region 600 remain intact. In this case, the second material layers 42 comprise a dielectric material, and are not removed within a region (i.e., the resistor region 600) including at least one vertically-extending cavity that is filled with a pillar structure 155.

[0219] Referring FIG. 25, at least one pillar contact via structure 850, drain contact via structures 88, and capacitor contact via structures 8C can be formed in the same manner as in the processing steps of FIG. 22.

[0220] Referring to FIG. 26, a resistor contact trench 279 can be formed through the alternating stack of first material layers 32 and second material layers 42 over the area of the doped contact region 112, for example, by application of a photoresist layer, lithographic patterning of the photoresist layer, and transfer of the pattern in the photoresist layer through the alternating stack (32, 42) by an anisotropic etch. In this case, the resistor contact trench 279 can be formed after formation of the backside contact trench 79 employed to replace portions of the second material layers 42 in the memory device region 100 and the capacitor region 400 with a conductive material. In one embodiment, the first material layers 32 can include a first insulating material (such as silicon oxide) and the second material layers 42 can include a second insulating material (such as silicon nitride).

[0221] Referring to FIG. 27, a substrate contact via structure 276 can be formed by filling the resistor contact trench 279 with at least one conductive material. An insulating spacer is not necessary in the resistor contact trench 279. Thus, the substrate contact via structure 276 can contact sidewalls of the first material layer 32 and the second material layer 42 in the resistor region 600. The at least one pillar contact via structure 850 can be a first resistor node via structure, and the substrate contact via structure 276 can be a second resistor node via structure.

[0222] In a fourth exemplary structure according to a fourth embodiment of the present disclosure, the resistors are formed in one or more of the stepped regions 700, which may be located in the word line stepped surface region(s)

300, the dummy staircase region(s) 400, and/or in the dummy staircase track 406, as shown in FIG. 37. Referring to FIG. 28, this structure can be derived from the first exemplary structure of FIGS. 6A and 6B, or the second exemplary structure of FIG. 19 by forming the optional dielectric pillar structure 7P and the dielectric support pillar structures 7Q and the dielectric material layer 73. The capacitor region 400 of the first embodiment may, or may not, be present in the fourth exemplary structure. The resistor region 500 of the second embodiment may, or may not, be present in the fourth exemplary structure. The resistor region 600 of the third embodiment may, or may not, be present in the fourth exemplary structure. A resistor region 700 is provided adjacent to a memory device region 100 (e.g., in stepped regions 300, 400 and/or 406). The optional dielectric pillar structure 7P can be formed at, or in proximity to, a boundary between the memory device region 100 and the resistor region 700 in a pattern same as, or similar to, the pattern of the dielectric pillar structure 7P of the first embodiment.

[0223] Referring to FIGS. 29A-29D, the processing steps of FIGS. 7A-7D are performed to form a backside contact trench 79 in the memory device region 100 and optional lateral separation trenches 89 in the resistor region 700.

[0224] Referring to FIGS. 30A and 30B, the processing steps of FIGS. 8A-8C and the processing steps of FIGS. 9A and 9B are performed to form an alternating stack (32, 346) of first material layers that are electrically insulating layers 32 and second material layers that are electrically conductive layers 346, which are herein referred to as fourth electrically conductive layers 346.

[0225] Referring to FIGS. 31A and 31B, the processing steps of FIGS. 10A and 10B are performed to remove any remaining metallic material from inside the backside contact trench 79.

[0226] Referring to FIGS. 32A and 32B, the processing steps of FIGS. 11A and 11B are performed to form an insulating spacer 74 and a backside contact via structure 76.

[0227] Referring to FIGS. 33A-33D, the processing steps of FIGS. 12A-12D are performed with a different lithographic pattern for forming contact via structures, which are herein referred to as resistor contact via structures 8R. A photoresist layer is applied over the dielectric material layer 73, and is lithographically patterned to form openings that overlie stepped horizontal surfaces of the fourth electrically conductive layers 346. A first set of vertically-extending via cavities is formed through the optional dielectric material layer 73 and the retro-stepped dielectric material layer 65. The lithographic pattern formed in the photoresist layer can be selected such that each horizontal stepped surface of the fourth electrically conductive layers 346 is physically exposed at the bottom of the first set of vertically-extending via cavities in the resistor region 700. The photoresist layer is removed, for example, by ashing. The first set of vertically-extending via cavities can be filled in the same manner as in the processing steps of FIGS. 12A-12D of the first embodiment to form the resistor contact via structures 8R. Each fourth electrically conductive layer 346 is a laterally-extending semiconductor or conductive structure that contacts a respective resistor contact via structure 8R.

[0228] Referring to FIGS. 34A-34D, another photoresist layer is applied over the dielectric material layer 73, and is lithographically patterned to form openings that overlie the stepped horizontal surfaces of the fourth electrically con-

ductive layers 346 and do not overlap with the resistor contact via structures 8R. A second set of vertically-extending via cavities 7C is formed through the optional dielectric material layer 73 and the retro-stepped dielectric material layer 65. The lithographic pattern formed in the photoresist layer can be selected such that each horizontal stepped surface of the fourth electrically conductive layers 346 is physically exposed at the bottom of the second set of vertically-extending via cavities in the resistor region 700 without etching, or physically exposing any surface of, the resistor contact via structures 8R. The photoresist layer is removed, for example, by ashing.

[0229] Referring to FIGS. 35A-35D, the second set of vertically-extending via cavities 7C can be filled with a suitable material that can provide a target level of resistivity. In one embodiment, the second set of vertically-extending via cavities can be filled with doped semiconductor material. The doped semiconductor material can be deposited in the second set of vertically extending via cavities by deposition of a semiconductor material with in-situ doping, or can be deposited as an intrinsic semiconductor material or a doped semiconductor material and implanted with electrical dopants employing an implantation mask layer (such as a photoresist layer). Excess portions of the doped semiconductor material above the top surface of the dielectric material layer 73 can be removed, for example, by chemical mechanical planarization.

[0230] Each remaining portion of the doped semiconductor material in a vertically-extending via cavity of the second constitutes a pillar structure 7R. Each pillar structure 7R can include a doped semiconductor material having a doping of at a preselected dopant level. In one embodiment, the pillar structures 7R can have a same horizontal cross-sectional area, and the resistance of each pillar structure 7R can be inversely proportional to the height of the pillar structure 346. Each fourth electrically conductive layer 346 is a laterally-extending semiconductor or conductive structure that contacts a respective resistor contact via structure 8R and a respective pillar structure 7R. In one embodiment, each of the pillar structure 7R can consist of a respective doped semiconductor material portion that is deposited within a respective vertically-extending cavity formed on the laterally-extending semiconductor or conductive structure (which is embodied as a fourth electrically conductive layer 346).

[0231] In one embodiment, a pillar structure 7R is formed within each vertically-extending cavity in the second set of vertically extending cavities, and each pillar structure 7P comprises a doped semiconductor material portion. All semiconductor material within each pillar structure 7R can have a doping of the same conductivity type, which can be the first conductivity type or the second conductivity type.

[0232] Referring to FIGS. 36A-36D and 37, a line level dielectric material layer 92 including a dielectric material can be formed over the top surface of the dielectric material layer 73 in the same manner as in the first embodiment. Interconnect line structures can be formed in the line level dielectric material layer 92, for example, by forming line trenches in the line level dielectric material layer 92 and filling the line trenches with at least one conductive material. Excess portions of the at least one conductive material can be removed from above the top surface of the line level dielectric material layer 92, for example, by chemical mechanical planarization.

[0233] First electrode metal lines 841, second electrode metal lines 842, source metal line 96, and bit lines 98, and optionally, additional metal line structures of the first, second, and third embodiments can be formed in the line level dielectric material layer 92. Each first electrode metal line 841 can contact a top surface of a pillar structure 7R, and each second electrode metal line 842 can contact a top surface of a resistor contact via structure 8R. The node-tying metal lines (821, 822, 823, 831, 832, 833) can include first node-tying metal lines (821, 822, 823) that tie the first node of a respective capacitor, and second node-tying metal lines (831, 832, 833) that tie the second node of a respective capacitor. The source metal line 98 provides electrical connection to the backside contact via structure 76 and the source region 61. The bit lines 98 provide electrical connection to the drain contact via structures 88 and the drain regions 63.

[0234] While the present disclosure is described employing an embodiment in which a single pillar structure 7R is formed per fourth electrically conductive layer 346, embodiments are contemplated herein in which multiple pillar structures 7R are formed per fourth exemplary conductive structure 346 at one or more levels.

[0235] Each physically adjoined set of a pillar structure 7R, a laterally-extending semiconductor or conductive structure as embodied as a portion of a fourth electrically conductive layer 346, and contact via structure 8R collectively constitute a resistor structure (7R, 346, 8R). A plurality of resistor structures can be simultaneously formed.

[0236] The fourth exemplary structure comprises a semiconductor device, which comprises an alternating stack (32, 346) of first material layers 32 and second material layers 346 located over a substrate (10, 61), at least one pillar structure 7P extending from a first horizontal plane including a top surface of the alternating stack (32, 346) to a second horizontal plane located underneath, and vertically spaced by a plurality of layers within the alternating stack (32, 346) from, the top surface of the alternating stack. For each pillar structure 7P, the second horizontal plane can be the plane that includes the top surface of a fourth electrically conductive layer 346 that contacts the pillar structure 7R. The plurality of layers that separates the first horizontal plane and the second horizontal plane can be the set of first and second material layers (32, 346) located between the first horizontal plane and the second horizontal plane. The first horizontal plane is common for all pillar structures 7P, and the second horizontal plane depends on the location of the bottommost portion of the pillar structure 7R.

[0237] A laterally-extending semiconductor or conductive structure, as embodied by a fourth electrically conductive layer 346, contacts a bottom surface of the at least one pillar structure 7P. A contact via structure 8R contacts a top surface of the laterally-extending semiconductor or conductive structure, as embodied by the fourth electrically conductive layer 346, and is laterally spaced from the at least one pillar structure 7P. Each of the at least one pillar structure 7P comprises a set of at least one doped semiconductor material portion therein (which can be a single doped semiconductor material portion). All semiconductor material within each of the at least one pillar structure has a doping of the same conductivity type, which can be the first conductivity type or the second conductivity type.

[0238] A plurality of resistor structures can be provided. Each resistor structure comprises at least one pillar structure

7R extending from the first horizontal plane to a respective electrically conductive layer 346 located at different levels. A fourth electrically conductive layer 346 can contact a bottom surface of each pillar structure 7R. A resistor contact via structure 8R can contact a top surface of each fourth electrically conductive layer 346. In one embodiment, each resistor contact via structure 8R can comprise a metallic via structure.

[0239] The doped semiconductor material portion of each pillar structure 7R can comprise a doped polycrystalline semiconductor material portion contacting inner surfaces of at least one electrically insulating material, which can be the insulating material of the retro-stepped dielectric material portion. In one embodiment, the first material layers 32 comprise electrically insulating layers, the second material layers 346 comprise electrically conductive layers, the laterally-extending semiconductor or conductive structure 346 comprises one of the electrically conductive layers. In one embodiment, each of the at least one pillar structure 7P can consist of a respective doped semiconductor material portion.

[0240] The alternating stack (32, 346) of the insulator layers 32 and the fourth electrically conductive layers 346 can comprise a stepped surface region in which each fourth electrically conductive layer 346 having at least one overlying fourth electrically conductive layer 346 laterally extends farther than any overlying fourth electrically conductive layer 346. Horizontal surfaces of the alternating stack (32, 346) that do not underlie any other layer within the alternating stack (32, 346) (and which contact one of the retro-stepped dielectric material portion 65, a pillar structure 7R, and/or a resistor contact via structure 8R) are adjoined to vertical surfaces of the first and second material layers. The retro-stepped dielectric material portion 65 overlies the stepped surface region. A set of at least one pillar structure 7R, a laterally-extending semiconductor or conductive structure as embodied in a portion of a fourth electrically conductive layer 346, and a resistor contact via structure 8R collectively constitute a resistor structure.

[0241] The first, second, third, and fourth exemplary structures can be formed alone, or in combination with any other among the first, second, third, and fourth exemplary structures. The exemplary structures of the present disclosure can provide passive components (such as resistors and capacitors) integrated with a three-dimensional device including an alternating stack of first material layers and second material layers, which can be a three-dimensional memory device such as a vertical NAND device. Some embodiments of the present disclosure provide capacitor structures and/or resistor structures employing stepped surfaces that are formed on the alternating stack of material layers. Thus, the processing steps of forming contact via structures for control gate electrodes of a vertical memory device can be employed to form the stepped surface region for the exemplary devices of the present disclosure. In some other embodiments, pillar structures that constitute a resistive portion of a resistor structure can be formed employing the same processing steps as the processing steps employed to form memory stack structures and by adding the processing step of a masked ion implantation to dope the semiconductor material therein. Thus, the passive devices of the present disclosure can be formed with minimal addition and/or modification to known processing steps for manufacturing a three-dimensional memory device, thereby reducing the production cost

for the passive devices. In addition, the passive devices of the present disclosure can be formed in proximity to memory stack structures by employing stepped surfaces that can be formed on an alternating stack of insulator layers and electrically conductive layers. Thus, integration of the passive devices into a peripheral circuit for a memory device can be done with minimal electrical wiring.

[0242] Although the foregoing refers to particular preferred embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. All of the publications, patent applications and patents cited herein are incorporated herein by reference in their entirety.

1. A three dimensional memory device, comprising:
 - a memory device region containing a plurality of non-volatile memory devices;
 - a peripheral device region containing active driver circuit devices;
 - a first stepped surface region between the peripheral device region and the memory device region containing a plurality of passive driver circuit devices;
 - a stack of alternating layers including electrically insulating layers and electrically conductive layers located over a substrate, wherein the first stepped surface region contains first portions of the electrically insulating layers and first portions of the electrically conductive layers, and the first stepped region is located on a first side of the stack;
 - a second stepped surface region containing second portions of the electrically insulating layers and second portions of the electrically conductive layers located on a second side of the stack;
 - a plurality of semiconductor channels located in the memory device region in the stack, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the substrate;
 - a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels;
 - a plurality of passive device contact via structures extending substantially perpendicular to the top surface of the substrate to the respective first portions of the electrically conductive layers in the first stepped surface region; and
 - a plurality of control gate contact via structures extending substantially perpendicular to the top surface of the substrate to the respective second portions of the electrically conductive layers in the second stepped surface region.
2. (canceled)
3. The device of claim 1, wherein:
 - the peripheral device region contains sense amplifiers;
 - the second stepped surface region comprises a word line stepped surface region; and
 - the second portions of the electrically conductive layers comprise a plurality of control gate electrodes extending substantially parallel to the top surface of the substrate, and the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

4. The device of claim 3, wherein:
the plurality of passive driver circuit devices comprise a plurality of capacitors;
the first portions of the electrically conductive layers comprise a plurality of capacitor electrodes;
the first portions of the electrically insulating layers comprise capacitor dielectrics located between the capacitor electrodes; and
the respective first and the second portions of each of the electrically conductive layer are located at the same level above the substrate and are electrically insulated from each other.
5. The device of claim 3, wherein the plurality of passive driver circuit devices comprises a plurality of resistors.
- 6-15. (canceled)
16. A method of forming a memory device comprising:
forming a plurality of memory devices in a memory device region;
forming a plurality of passive devices outside the memory device region;
forming a conductive layer in one deposition step such that a first portion of the conductive layer comprises a portion of at least one of the passive device and a second portion of the conductive layer forms a portion of at least one memory device;
forming a stack comprising an alternating plurality of electrically insulating layers and second material layers over a substrate;
forming trenches extending through the stack of alternating layers, wherein sidewalls of a patterned portion of the stack of alternating layers are physically exposed;
forming a patterned stack comprising an alternating plurality of the electrically insulating layers and electrically conductive layers, wherein the electrically conductive layers in the patterned stack are formed at each level of the second material layers, and the patterned stack is laterally contacted by a set of dielectric fill material portions formed within trenches; and
forming a plurality of contact via structures on the electrically conductive layers,
wherein:
portions of the electrically conductive layers located in a first stepped surface region between a peripheral device region and a memory device region constitute at least a portion of passive devices; and
forming the conductive layer comprises forming at least one of the electrically conductive layers or at least one of the plurality of contact via structures.
17. (canceled)
18. The method of claim 16, wherein:
the passive devices comprise capacitors;
a subset of the electrically insulating layers located in the first stepped surface region constitutes node dielectrics of the set of capacitors; and
each capacitor in the set comprises:
a first node that includes an underlying electrically conductive layer of a respective vertically neighboring pair and a respective contact via structure that extends upward from the underlying electrically conductive layer and through the dielectric material portion; and
a second node that includes an overlying electrically conductive layer of the respective vertically neighboring pair and a respective contact via structure that extends upward from the overlying electrically conductive layer and through the dielectric material portion.
19. The method of claim 18, further comprising replacing the second material layers with conductive material portions;
wherein:
the electrically conductive layers in the patterned stack comprises remaining portions of the conductive material portions;
the set of dielectric fill material portions is formed within the trenches after replacement of the second material layers with the conductive material portions; and
the second material layers are replaced with the conductive material portions by:
forming lateral recesses by etching the second material layers by introducing an etchant through one or more of the trenches;
depositing the conductive material portions within the lateral recesses; and
filling the one or more of the trenches with one or more dielectric fill material portions within the set of dielectric fill material portions.
20. The method of claim 18, further comprising:
filling each of the trenches with a dielectric material of a respective dielectric fill material portion;
forming a stepped surface region in which each underlying second material layer laterally extends farther than any overlying second material layer thereof; and
forming a dielectric material portion over the stepped surface region.
21. The method of claim 20, further comprising:
forming a support pillar trench through the alternating stack;
forming a dielectric pillar structure within the support pillar trench by depositing a first dielectric fill material;
forming lateral separation trenches through the alternating stack; and
forming dielectric trench fill structures by depositing a second dielectric fill material, wherein:
the set of dielectric fill material portions comprise the dielectric pillar structure and the dielectric trench fill structures;
the support pillar trench laterally extends along a same lateral direction as stepped surfaces within the stepped surface region; and
the lateral separation trenches laterally extend along a lateral direction that is perpendicular to the stepped surfaces within the stepped surface region.
22. The method of claim 20, wherein the dielectric material portion is a retro-stepped dielectric material portion in which a horizontal cross-sectional area of the dielectric material portion at a horizontal plane is not less than a horizontal cross-sectional area of the dielectric material portion at any horizontal plane that is more proximal to the substrate.
23. The method of claim 18, wherein:
each capacitor within the set of capacitors comprises two pairs of vertically neighboring electrically conductive layers;
the first node of the capacitor includes an underlying electrically conductive layer of a first vertically neighboring pair and an electrically conductive layer of a second vertically neighboring pair; and

the second node of the capacitor includes an overlying electrically conductive layer of the vertically neighboring pair and another electrically conductive layer of the second vertically neighboring pair.

24. The method of claim 16, wherein the passive devices comprise resistors.

25. (canceled)

26. A method of forming a memory device comprising: forming a plurality of memory devices in a memory device region;

forming a plurality of passive devices outside the memory device region; and

forming a conductive layer in one deposition step such that a first portion of the conductive layer comprises a portion of at least one of the passive device and a second portion of the conductive layer forms a portion of at least one memory device;

wherein:

forming the plurality of memory devices in a memory device region comprises forming a monolithic three-dimensional memory device located over the substrate; the monolithic three-dimensional memory device comprises:

a memory opening extending through the stack;

a memory film formed within the memory opening; and

a semiconductor channel formed within the memory film;

the passive devices are components of a peripheral device of the monolithic three-dimensional memory device;

the monolithic three-dimensional memory device is a vertical NAND memory device;

the electrically conductive layers comprise, or are electrically connected to, a respective word line of the vertical NAND memory device;

the substrate comprises a silicon substrate;

the vertical NAND memory device comprises an array of monolithic three-dimensional NAND strings over the silicon substrate;

at least one memory cell in the first device level of the three-dimensional array of NAND strings is located over another memory cell in the second device level of the three-dimensional array of NAND strings;

the silicon substrate contains an integrated circuit comprising a driver circuit for the memory device located thereon; and

the three-dimensional array of NAND strings comprises:

a plurality of semiconductor channels, wherein at least one end portion of each of the plurality of semiconductor channels extends substantially perpendicular to a top surface of the silicon substrate;

a plurality of charge storage elements, each charge storage element located adjacent to a respective one of the plurality of semiconductor channels; and

a plurality of control gate electrodes having a strip shape extending substantially parallel to the top surface of the silicon substrate, the plurality of control gate electrodes comprise at least a first con-

trol gate electrode located in the first device level and a second control gate electrode located in the second device level.

27. A method of forming a memory device comprising: forming a plurality of memory devices in a memory device region;

forming a plurality of passive devices outside the memory device region; and

forming a conductive layer in one deposition step such that a first portion of the conductive layer comprises a portion of at least one of the passive device and a second portion of the conductive layer forms a portion of at least one memory device;

wherein:

forming the plurality of memory devices in a memory device region comprises forming a monolithic three-dimensional memory device located over the substrate; the monolithic three-dimensional memory device comprises:

a memory opening extending through the stack;

a memory film formed within the memory opening; and

a semiconductor channel formed within the memory film; and

the first stepped surface region contains first portions of the electrically insulating layers and first portions of the electrically conductive layers, and the first stepped region is located on a first side of the stack.

28. The method of claim 27, further comprising forming a second stepped surface region containing second portions of the electrically insulating layers and second portions of the electrically conductive layers located on a second side of the stack during at the same time as forming the first stepped surface region.

29. The method of claim 28, wherein:

forming the plurality of contact via structures comprises forming a plurality of passive device contact via structures extending substantially perpendicular to the top surface of the substrate to the respective first portions of the electrically conductive layers in the first stepped surface region, and at the same time forming a plurality of control gate contact via structures extending substantially perpendicular to the top surface of the substrate to the respective second portions of the electrically conductive layers in the second stepped surface region;

the peripheral device region contains sense amplifiers;

the second stepped surface region comprises a word line stepped surface region; and

the second portions of the electrically conductive layers comprise a plurality of control gate electrodes extending substantially parallel to the top surface of the substrate, and the plurality of control gate electrodes comprise at least a first control gate electrode located in the first device level and a second control gate electrode located in the second device level.

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