

Device Electronics for Integrated Circuits

Third Edition

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Photomicrograph of the Pentium 4 microprocessor which contains 42 million transistors; see Fig. 2.2e for a block diagram. (Courtesy of Intel Corporation.)

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these conducting layers, but its low melting point (660°C) and its reactivity with other elements generally precludes heating it higher than 500°C after it is deposited. If, as an alternative, a thin layer of silicon is used as an interconnecting path, subsequent heat treatments can be carried out at 1000°C or higher. This high-temperature capability is extremely important in a number of IC applications.

Polycrystalline Silicon. To deposit silicon for interconnections, methods similar to those used for epitaxy are often employed. However, because these layers are not deposited directly on the single-crystal silicon wafer, but usually over an amorphous SiO_2 layer, they cannot grow epitaxially. These CVD films are typically composed of many small crystallites (often with ~ 50 – 100 nm dimensions) and are therefore called *polycrystalline silicon*, or simply *polysilicon*.

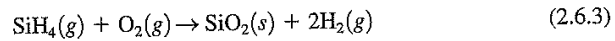
Polysilicon has special importance in MOS processing where it is used as a transistor electrode in *silicon-gate* MOSFETs, which are described in Chapter 9. Polysilicon is also found in bipolar ICs where it is used as a diffusion source, as discussed in Sec. 6.5. For this application, polysilicon is formed over the single-crystal substrate by lowering the CVD temperature to about 600 – 700°C . The limited thermal energy of the silicon atoms available for surface migration at these temperatures and the residual oxide on the silicon surface favor forming a polycrystalline, rather than a single-crystal, layer. The behavior of the layer during subsequent processing depends critically on the thin oxide layer (~ 1 atom-layer thick) between the polysilicon and the underlying single-crystal silicon.

Amorphous Silicon. When CVD silicon is deposited at still lower temperatures (below about 600°C), an amorphous film forms regardless of the nature of the substrate. Amorphous silicon has only very short-range order (typically over only a few atomic spacings), and no crystalline regions can be observed. During heat treatments at moderate temperatures ($\geq 600^{\circ}\text{C}$), silicon deposited in an amorphous form crystallizes to become polycrystalline silicon. Depositing silicon in an amorphous form and subsequently crystallizing it is becoming increasingly important in a number of applications, such as the active transistor matrix used in liquid-crystal displays.

Somewhat below 600°C amorphous silicon can be deposited by thermal decomposition of silane. However, at markedly lower temperatures in the 300°C range, additional energy in the form of a plasma is used to decompose the silane and produce an amorphous silicon layer. At this lower temperature, significant amounts of hydrogen from the decomposition of the silane remain in the deposited layer and modify its electrical properties.

Insulating Films. Insulating, as well as conducting, films can be formed by CVD. Especially important to IC processing are CVD films of silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) formed by reacting a gas such as silane (SiH_4) or dichlorosilane (SiH_2Cl_2) with oxygen or nitrous oxide (N_2O) (for SiO_2) or with ammonia (NH_3) (for Si_3N_4). Although CVD oxides are not usually as pure nor of equivalent electrical quality as thermally grown oxides, they do not require the high-temperature processing needed for thermal oxidation. For example, CVD oxide can be used above a polysilicon interconnection layer before aluminum or copper is deposited to avoid the dopant diffusion that would occur during a thermal oxidation. CVD oxide deposited at even lower temperatures can be used above aluminum or copper layers to separate different conducting layers that interconnect active devices and also to protect the finished integrated circuit from contamination. In the latter case, the oxide is usually doped with phosphorus to impede the migration of any contaminant through the oxide to the circuit. A deposited

oxide commonly used between conducting layers is formed by the reaction of silane and oxygen at about 400°C. The reaction



produces an oxide that is less dense and less chemically resistant than thermally grown oxide, but is very useful when high temperatures must be avoided.

Because silicon-nitride (Si_3N_4) layers do not oxidize as readily as does silicon, silicon-nitride layers are useful for limiting the regions where thermal oxide is grown in a *local oxidation* (LOCOS) process used for device isolation in integrated circuits [17]. In the LOCOS process, a layer of silicon nitride is deposited on the silicon substrate and lithographically defined to retain the nitride in the device regions (Figure 2.26a). The nitride is removed from the area between the devices where a thick, isolating oxide layer is to be grown. A thin, *stress-relief* SiO_2 layer is usually inserted between the nitride and the silicon wafer to prevent stress from the nitride from creating defects in the silicon wafer. After the nitride is defined, the wafer is inserted into an oxidation furnace, and a thick oxide is grown in the exposed silicon regions, usually in a steam or pyrogenic ($\text{H}_2\text{:O}_2$) ambient (Figure 2.26b). The nitride prevents oxidation of the device regions. A layer of SiO_2 more than one μm thick can be grown on exposed silicon while only a few tens of nm of Si_3N_4 are converted to SiO_2 . After the oxidation, the thin oxide over the nitride is removed, and the nitride and thin stress-relief oxide

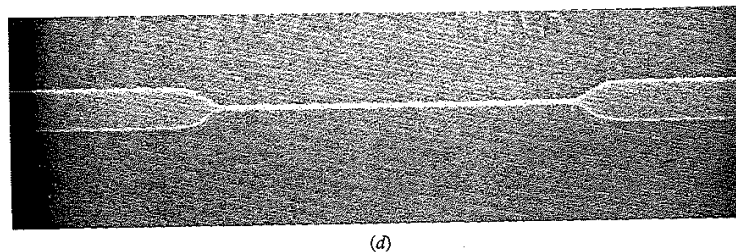
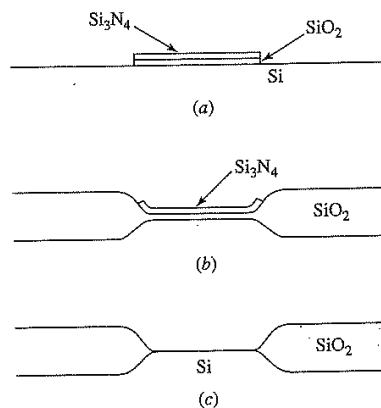


FIGURE 2.26 Local Oxidation of Silicon (LOCOS). (a) Defined pattern consisting of stress-relief oxide and Si_3N_4 covering the area over which further oxidation is not desired, (b) thick oxide layer grown over the bare silicon region, (c) stress-relief oxide and Si_3N_4 removed by etching to permit device fabrication, (d) scanning electron micrograph (5000 $\times$) showing LOCOS-processed wafer at step (b).

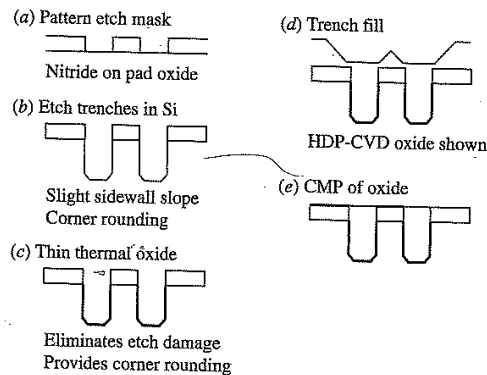


FIGURE 2.27 Trench isolation is used to form very narrow isolation regions between adjacent devices. After the trench pattern is etched in a masking material (a), the trench is etched directionally using a reactive ion etch process (b). A thin, high-quality oxide is formed (c), and the trench is filled with polysilicon or with oxide [shown for oxide in (d)]. The excess material is removed by chemical-mechanical polishing (e).

are etched away to expose the bare silicon in the device regions (Figure 2.26c). Figure 2.26d shows a cross section scanning-electron micrograph of a device region formed by a LOCOS process. The oxide thickness tapers gradually from the isolation region to the device region. This taper is an advantage in avoiding sharp edges that make continuous film coverage difficult. For devices made with very small dimensions, however, the taper is a disadvantage and limits formation of device regions with very small (submicrometer) dimensions.

To form isolation regions suitable for very fine features, *trench isolation* can be used, as shown in Figure 2.27. As the name implies, a very narrow and relatively deep trench is etched around the device to be isolated. Directional, *reactive ion etching* is used to form the nearly vertical sidewalls of the trench needed to allow the top of the trench to have the minimum feature size that can be defined and the trench to be adequately deep (Figure 2.27b). After a thin, high-quality, insulating oxide is formed on the walls and bottom of the trench (Figure 2.27c), the trench is filled with either an oxide or possibly with polysilicon. For deep trenches, polysilicon is useful because its thermal coefficient of expansion is virtually identical to that of single-crystal silicon, reducing thermal stress and bending of the wafer. For shallow trenches, oxide can be used with minimum effect on the stress. When oxide is used, it is often deposited by a CVD process using a *high-density plasma* (Figure 2.27d). The directionality of the high-density plasma allows filling of very deep and narrow trenches. The ion bombardment occurring during the deposition process improves the quality and density of the oxide by knocking weakly bound atoms from the surface of the depositing layer.

Reaction Kinetics. Layers deposited by CVD are usually formed in open-flow reactors, as illustrated in (Figure 2.25b). The gases flow continuously through the reaction chamber where the deposition takes place; gaseous byproducts are exhausted along with unused reactant gases. A *carrier gas* is often used to push the reactants through the chamber. The gases are usually mixed before entering the reaction chamber unless they react at low temperatures. At the surface of the wafers, there is a gas-phase boundary layer through which the reactants must diffuse (Figure 2.28a). This boundary layer is a transition region between the unrestricted flow region and the walls and fixtures in the chamber where the gas velocity is reduced by viscous forces that tend to pull against the moving gas and retard its flow (Figure 2.28b).

The reactants must pass through the boundary layer to reach the surface, where the reaction is promoted by heat. The deposition takes place on all heated surfaces reached by the gases. For example, if the walls of the chamber are hot, a generally undesired and troublesome film forms on the walls, as well as on the wafers. Either the rate of diffusion