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Micron Technology, Inc., and
Micron Consumer Products Group LLC

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Plaintiff,

v.

MICRON TECHNOLOGY, INC., et al.,

Defendants.

MICRON TECHNOLOGY, INC.,

Counterclaim Plaintiff,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD., and YANGTZE MEMORY TECHNOLOGIES, INC.,

Counterclaim Defendants.

Case No. 3:23-cv-05792-RFL

DEFENDANTS' ANSWER TO FIRST AMENDED COMPLAINT AND COUNTERCLAIMS

DEMAND FOR JURY TRIAL

Judge: Hon. Rita F. Lin

Defendants Micron Technology, Inc. ("Micron Technology" or "MTI") and Micron Consumer Products Group LLC ("MCPG") (collectively "Defendants" or "Micron"), by and through their undersigned counsel, hereby submit this answer to the First Amended Complaint ("FAC") filed by Yangtze Memory Technologies Company, Ltd. ("YMTC") on February 2, 2024, and hereby assert counterclaims against YMTC and Yangtze Memory Technologies, Inc. ("YMTC Inc.") (YMTC and YMTC Inc. collectively, "the YMTC Entities"). To the extent not expressly admitted below, Defendants deny each and every allegation of the FAC.

PRELIMINARY STATEMENT

1. Micron admits that YMTC filed its original complaint in this action on November 9, 2023. Micron avers that the original complaint was so deficient and conclusory that Micron moved to dismiss it for failure to state a claim – a motion that YMTC did not oppose. Micron further avers that the original complaint was so deficient and conclusory, and Micron's motion to dismiss was so meritorious, that YMTC abandoned its original complaint and filed an amended complaint that includes claim charts and other allegations that were not part of the original complaint. Except as so admitted and averred, Micron denies the allegations of paragraph 1 of the FAC.

2. Micron admits that it requested, and YMTC agreed to, a 45-day extension to respond to the original complaint. Micron further admits that the agreed extension is documented in a stipulation between the parties filed on November 29, 2023. Except as so admitted, Micron denies the allegations of paragraph 2 of the FAC.

3. Micron admits that MTI and/or one or more of its subsidiaries design and manufacture 3D NAND products, including the products accused of infringement in this action, and that MTI and/or one or more of its subsidiaries has information about the structure, layout, and fabrication of those 3D NAND products. Micron further avers that YMTC's original complaint was so deficient and conclusory that it did not put Micron on notice of YMTC's infringement claims. Micron further avers that, if YMTC's original complaint had put Micron on notice of YMTC's claims in compliance with the law, YMTC would have opposed Micron's motion to dismiss the complaint for failure to state a claim, which it did not. Micron further avers that the

failure of YMTC to oppose Micron's motion to dismiss, its abandonment of its original complaint, and the extensive differences between the original complaint and the FAC demonstrate that the original complaint failed to meet the requirements of Rules 8 and 12 of the Federal Rules of Civil Procedure and failed to put Micron on notice of YMTC's infringement claims. Except as so admitted and averred, Micron denies the allegations of paragraph 3 of the FAC.

4. Micron denies the allegations of paragraph 4 of the FAC.

5. Micron denies the allegations of paragraph 5 of the FAC.

6. Micron denies the allegations of paragraph 6 of the FAC.

NATURE OF THE ACTION

7. Micron is without knowledge or information sufficient to form a belief as to the truth of the allegations in the fourth and sixth sentences of paragraph 7 of the FAC and, on that basis, denies them. Micron denies the remaining allegations of paragraph 7 of the FAC.

8. Micron is without knowledge or information sufficient to form a belief as to the truth of the allegations in the second sentence of paragraph 8 of the FAC and, on that basis, denies them. Micron denies the remaining allegations of paragraph 8 of the FAC.

9. Micron admits that 3D NAND flash memory is a widely used form of memory, that it is used in a variety of products and solutions, and that competition and innovation are beneficial to society. Except as so admitted, Micron denies the allegations of paragraph 9 of the FAC.

10. Micron denies the allegations of paragraph 10 of the FAC.

11. Micron admits that YMTC is asserting the "Asserted Patents" against Micron in this lawsuit. Except as so admitted, Micron denies the allegations of paragraph 11 of the FAC.

THE PARTIES

12. Admitted.

13. Micron admits the first sentence of paragraph 13 of the FAC. Micron further admits that it does not contest the propriety of service of process in this action through CSC in Sacramento, California. Except as so admitted, Micron denies the allegations of paragraph 14 of the FAC.

14. Micron admits that MCPG is a wholly-owned subsidiary of MTI, that it is organized under the laws of the State of Delaware, and that it has a principal place of business at 110 Holger

Way, San Jose, California 95134. MCPG further admits that it does not contest the propriety of service of process in this action through CSC in Sacramento, California. Except as so admitted, Micron denies the allegations of paragraph 14 of the FAC.

15. Micron denies the allegations of paragraph 15 of the FAC.

16. Micron denies the allegations of paragraph 16 of the FAC.

JURISDICTION AND VENUE

17. Without admitting that YMTC has standing to maintain this lawsuit, Micron admits the allegations of paragraph 17 of the FAC.

18. Micron admits that the Court has personal jurisdiction over Micron for purposes of this action. Except as so admitted, Micron denies the allegations of paragraph 18 of the FAC.

19. Micron denies the allegations of paragraph 19 of the FAC.

20. Micron denies the allegations of paragraph 20 of the FAC.

21. Micron admits that venue for this action is proper in this judicial district. Except as so admitted, Micron denies the allegations of paragraph 21 of the FAC.

22. Micron denies the allegations of paragraph 22 of the FAC.

DIVISIONAL ASSIGNMENT

23. Micron admits that, under General Order No. 44, this district maintains a district-wide system of assignment for "intellectual property rights" actions. Except as so admitted, Micron denies the allegations of paragraph 23 of the FAC.

YMTC'S ALLEGED INNOVATIONS AND PATENTS

24. Micron admits that YMTC has a wholly-owned subsidiary, YMTC Inc., in this judicial district. Micron further admits that YMTC supplies 3D NAND products on a global basis, including in the United States. Micron denies the second sentence of paragraph 24 of the FAC. Except as so admitted and denied, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 24 of the FAC and, on that basis, denies them.

25. Micron denies the last sentence of paragraph 25 of the FAC. Except as so denied, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 25 of the FAC and, on that basis, denies them.

26. Micron denies the allegations of paragraph 26 of the FAC.

27. Micron denies the allegations of paragraph 27 of the FAC.

MICRON'S ACCUSED PRODUCTS AND ACTIVITIES

28. Micron admits that MTI is an industry leader in innovative computer-memory and data-storage solutions, including 3D NAND. Except as so admitted, Micron denies the allegations of paragraph 28 of the FAC.

29. Micron admits that MTI and/or one or more of its subsidiaries has designed, made, used, sold, and/or offered for sale 96-Layer 3D NAND memory products, including products with the B27A design ID. Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in the second sentence of paragraph 29 of the FAC and, on that basis, denies them. Except as so admitted and denied, Micron denies the allegations of paragraph 29 of the FAC.

30. Micron admits that MTI and/or one or more of its subsidiaries has designed, made, used, sold, and/or offered for sale 128-Layer 3D NAND memory products, including products with the B37R design ID. Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in the second sentence of paragraph 30 of the FAC and, on that basis, denies them. Except as so admitted and denied, Micron denies the allegations of paragraph 30 of the FAC.

31. Micron admits that MTI and/or one or more of its subsidiaries has designed, made, used, sold, and/or offered for sale 176-Layer 3D NAND memory products, including products with the N48R and B47R design IDs. Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in the second and third sentences of paragraph 31 of the FAC and, on that basis, denies them. Except as so admitted and denied, Micron denies the allegations of paragraph 31 of the FAC.

32. Micron admits that MTI and/or one or more of its subsidiaries has designed, made, used, sold, and/or offered for sale 232-Layer 3D NAND memory products, including products with the B58R design ID. Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in the second sentence of paragraph 32 of the FAC and, on that basis, denies them. Except as so admitted and denied, Micron denies the allegations of paragraph 32 of the FAC.

33. Micron admits that YMTC purports to call certain 3D NAND products the "Accused Memory Products." Except as so admitted, Micron denies the allegations of paragraph 33 of the FAC.

34. Micron admits that MTI and/or one or more of its subsidiaries has made, used, sold, and/or offered for sale the "Accused Memory Products." Micron further admits that various third parties may use one or more of the "Accused Memory Products" in their own products and solutions. Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 34 of the FAC and, on that basis, denies them.

35. Micron admits that MTI and/or one or more of its subsidiaries has conducted research, development, and testing of the "Accused Memory Products." Except as so admitted, Micron denies the allegations of paragraph 35 of the FAC.

36. Micron denies the allegations of paragraph 36 of the FAC.

37. Micron admits that MTI and/or one or more of its subsidiaries sells and/or offers to sell the Accused Memory Products. Except as so admitted, Micron denies the allegations of paragraph 37 of the FAC.

38. Micron admits that the micron.com website lists one or more distributors. Except as so admitted, Micron denies the allegations of paragraph 38 of the FAC.

39. Micron admits that MTI and/or one or more of its subsidiaries has used the Accused Memory Products and has sold and/or offered to sell the Accused Memory Products to one or more customers in a number of sectors. Except as so admitted, Micron denies the allegations of paragraph 39 of the FAC.

40. Micron denies the allegations of paragraph 40 of the FAC.

41. Micron denies the allegations of paragraph 41 of the FAC.

42. Micron denies the allegations of paragraph 42 of the FAC.

COUNT I

43. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

44. Micron admits that YMTC filed as Exhibit 1 what appears to be a copy of the '623 patent, which is entitled "3D NAND Memory Device and Method of Forming the Same." Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 44 of the FAC and, on that basis, denies them.

45. Micron denies the allegations of paragraph 45 of the FAC.

46. Micron denies the allegations of paragraph 46 of the FAC.

47. Micron denies the allegations of paragraph 47 of the FAC.

48. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products include or practice one or more claim limitations of the '623 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 48 of the FAC.

49. Micron denies the allegations of paragraph 49 of the FAC.

50. Micron denies the allegations of paragraph 50 of the FAC.

51. Micron denies the allegations of paragraph 51 of the FAC.

52. Micron denies the allegations of paragraph 52 of the FAC.

COUNT II

53. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

54. Micron admits that YMTC filed as Exhibit 2 what appears to be a copy of the '822 patent, which is entitled "Non-Volatile Memory Device and Control Method." Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 54 of the FAC and, on that basis, denies them.

55. Micron denies the allegations of paragraph 55 of the FAC.

56. Micron denies the allegations of paragraph 56 of the FAC.

57. Micron denies the allegations of paragraph 57 of the FAC.

58. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products

include or practice one or more claim limitations of the '822 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 58 of the FAC.

59. Micron denies the allegations of paragraph 59 of the FAC.

60. Micron denies the allegations of paragraph 60 of the FAC.

61. Micron denies the allegations of paragraph 61 of the FAC.

62. Micron denies the allegations of paragraph 62 of the FAC.

COUNT III

63. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

64. Micron admits that YMTC filed as Exhibit 3 what appears to be a copy of the '378 patent, which is entitled "Through Array Contact (TAC) for Three-Dimensional Memory Devices." Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 64 of the FAC and, on that basis, denies them.

65. Micron denies the allegations of paragraph 65 of the FAC.

66. Micron denies the allegations of paragraph 66 of the FAC.

67. Micron denies the allegations of paragraph 67 of the FAC.

68. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products include or practice one or more claim limitations of the '378 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 68 of the FAC.

69. Micron denies the allegations of paragraph 69 of the FAC.

70. Micron denies the allegations of paragraph 70 of the FAC.

71. Micron denies the allegations of paragraph 71 of the FAC.

72. Micron denies the allegations of paragraph 72 of the FAC.

73. Micron denies the allegations of paragraph 73 of the FAC.

COUNT IV

74. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

75. Micron admits that YMTC filed as Exhibit 4 what appears to be a copy of the '806 patent, which is entitled "Through Array Contact (TAC) for Three-Dimensional Memory Devices." Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 75 of the FAC and, on that basis, denies them.

76. Micron denies the allegations of paragraph 76 of the FAC.

77. Micron denies the allegations of paragraph 77 of the FAC.

78. Micron denies the allegations of paragraph 78 of the FAC.

79. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products include or practice one or more claim limitations of the '806 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 79 of the FAC.

80. Micron denies the allegations of paragraph 80 of the FAC.

81. Micron denies the allegations of paragraph 81 of the FAC.

82. Micron denies the allegations of paragraph 82 of the FAC.

83. Micron denies the allegations of paragraph 83 of the FAC.

84. Micron denies the allegations of paragraph 84 of the FAC.

COUNT V

85. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

86. Micron admits that YMTC filed as Exhibit 5 what appears to be a copy of the '872 patent, which is entitled "Three-Dimensional Memory Device and Method for Forming the Same." Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 86 of the FAC and, on that basis, denies them.

87. Micron denies the allegations of paragraph 87 of the FAC.

88. Micron denies the allegations of paragraph 88 of the FAC.

89. Micron denies the allegations of paragraph 89 of the FAC.

90. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products include or practice one or more claim limitations of the '872 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 90 of the FAC.

91. Micron denies the allegations of paragraph 91 of the FAC.

92. Micron denies the allegations of paragraph 92 of the FAC.

93. Micron denies the allegations of paragraph 93 of the FAC.

94. Micron denies the allegations of paragraph 94 of the FAC.

COUNT VI

95. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

96. Micron admits that YMTC filed as Exhibit 6 what appears to be a copy of the '957 patent, which is entitled "Architecture and Method for NAND Memory Operation." Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 96 of the FAC and, on that basis, denies them.

97. Micron denies the allegations of paragraph 97 of the FAC.

98. Micron denies the allegations of paragraph 98 of the FAC.

99. Micron denies the allegations of paragraph 99 of the FAC.

100. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products include or practice one or more claim limitations of the '957 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 100 of the FAC.

101. Micron denies the allegations of paragraph 101 of the FAC.

102. Micron denies the allegations of paragraph 102 of the FAC.

103. Micron denies the allegations of paragraph 103 of the FAC.

104. Micron denies the allegations of paragraph 104 of the FAC.

COUNT VII

105. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

106. Micron admits that YMTC filed as Exhibit 7 what appears to be a copy of the '342 patent, which is entitled "Method for Reading Three-Dimensional Flash Memory." Except as so admitted, Micron lacks knowledge or information sufficient to form a belief as to the truth of the allegations in paragraph 106 of the FAC and, on that basis, denies them.

107. Micron denies the allegations of paragraph 107 of the FAC.

108. Micron denies the allegations of paragraph 108 of the FAC.

109. Micron denies the allegations of paragraph 109 of the FAC.

110. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products include or practice one or more claim limitations of the '342 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 110 of the FAC.

111. Micron denies the allegations of paragraph 111 of the FAC.

112. Micron denies the allegations of paragraph 112 of the FAC.

113. Micron denies the allegations of paragraph 113 of the FAC.

114. Micron denies the allegations of paragraph 114 of the FAC.

COUNT VIII

115. Micron incorporates by reference and realleges its responses to all the foregoing paragraphs of this Answer as if fully set forth herein.

116. Micron admits that YMTC filed as Exhibit 8 what appears to be a copy of the '031 patent, which is entitled "Multiple-Stack Three-Dimensional Memory Device and Fabrication Method Thereof." Except as so admitted, Micron lacks knowledge or information sufficient to

form a belief as to the truth of the allegations in paragraph 116 of the FAC and, on that basis, denies them.

117. Micron denies the allegations of paragraph 117 of the FAC.

118. Micron denies the allegations of paragraph 118 of the FAC.

119. Micron denies the allegations of paragraph 119 of the FAC.

120. Micron admits that it identified numerous deficiencies in YMTC's original complaint in Micron's motion to dismiss, including YMTC's failure to plead that Micron's products include or practice one or more claim limitations of the '031 patent. Micron's motion to dismiss is on file with the Court and speaks for itself. Except as so admitted, Micron denies the allegations of paragraph 120 of the FAC.

121. Micron denies the allegations of paragraph 121 of the FAC.

122. Micron denies the allegations of paragraph 122 of the FAC.

123. Micron denies the allegations of paragraph 123 of the FAC.

124. Micron denies the allegations of paragraph 124 of the FAC.

PLAINTIFF'S PRAYER FOR RELIEF

Micron denies that YMTC is entitled to any relief whatsoever in this action, either as prayed for in the amended complaint or otherwise.

DEFENSES

Without assuming any burden other than that imposed by law, Micron asserts the following defenses in response to the allegations in the FAC. Micron reserves the right to assert additional defenses as they become known throughout the course of discovery in this action, including any defenses currently unknown to Micron. The assertion of a defense below is not a concession that Micron bears the burden of proving the matter asserted.

First Defense: Failure to State a Claim

1. The FAC fails to state a claim upon which relief can be granted.

Second Defense: Noninfringement

2. Micron has not infringed and does not infringe, directly or indirectly, any claim of the Asserted Patents.

Third Defense: Invalidity

3. One or more of the claims of the Asserted Patents are invalid for failure to satisfy the conditions for patentability set forth in 35 U.S.C. § 1 et seq., including 35 U.S.C. §§ 101, 102, 103, and/or 112.

Fourth Defense: Prosecution History Estoppel and/or Disclaimer

4. Based on proceedings before the U.S. Patent and Trademark Office during the prosecution of the applications that led to or resulted in the Asserted Patents, YMTC is precluded or otherwise estopped from asserting that any claim of the Asserted Patents covers, either literally or under the doctrine of equivalents, any product or method made, performed, used, sold, offered for sale, or imported by Micron.

Fifth Defense: Limitation on Damages and Costs

5. YMTC's claims and prayer for relief are barred in whole or in part by 35 U.S.C. §§ 286, 287, and/or 288, including without limitation based on failure to mark and lack of notice.

Sixth Defense: Government Sales

6. YMTC's claims are barred in whole or in part by 28 U.S.C. § 1498 to the extent they relate to use or manufacture of the alleged inventions of the Asserted Patents by or for the United States.

MTI'S COUNTERCLAIMS

MTI incorporates herein by reference the admissions, allegations, denials, and defenses contained in its answer above as if fully set forth herein. For its counterclaims against the YMTC Entities, MTI states as follows:

Nature of the Action

1. MTI asserts these patent infringement claims against the YMTC Entities arising from their infringement of U.S. Patent Nos. 10,475,737 (the "'737 patent"), 8,945,996 (the "'996 patent"), 8,803,214 (the "'214 patent"), 10,872,903 (the "'903 patent"), and 10,373,974 (the "'974 patent") (collectively, the "MTI Asserted Patents"). On information and belief, each of the YMTC Entities commits the acts of infringement described herein individually and together as one enterprise.

The Parties

2. MTI is a Delaware corporation with its principal place of business at 8000 South Federal Way, Boise, Idaho 83716.

3. On information and belief, YMTC is a Chinese company with its principal place of business at No.88 Weilai 3rd Road, East Lake High-tech Development Zone, Wuhan, Hubei, China.

4. On information and belief, YMTC Inc. is a California corporation with its principal place of business at 2953 Bunker Hill Lane, Ste. 206, Santa Clara, California 95054.

Jurisdiction and Venue

5. MTI brings these counterclaims under the Patent Laws of the United States, 35 U.S.C. §§ 1 et seq., against the YMTC Entities for their infringement of the MTI Asserted Patents.

6. This Court has subject matter jurisdiction over MTI's counterclaims pursuant to 28 U.S.C. §§ 1331 and 1338(a).

7. This Court has personal jurisdiction over YMTC, which is the plaintiff in this action. Further, YMTC commits acts of infringement in this District through its business and sales activities in the Northern District of California, including directly and/or indirectly selling, offering for sale, importing, and/or using products that practice (or are made in a manner that practices) one or more claims of the MTI Asserted Patents.

8. This Court has personal jurisdiction over YMTC Inc., which has its principal place of business in Santa Clara, California, in this judicial District. Further, YMTC Inc. commits acts of infringement in this District through its business and sales activities in the Northern District of California, including directly and/or indirectly selling, offering for sale, importing, and/or using products that practice (or are made in a manner that practices) one or more claims of the MTI Asserted Patents.

MTI's Innovations and Patents

9. MTI was founded in 1978 and is headquartered in Boise, Idaho. Since that time, MTI has become a world leader in innovative computer-memory and data-storage solutions, employing more than 43,000 employees worldwide with more than 5,000 employees in Idaho. Ex. 11 at 2; Ex. 12 at 5.

10. MTI is the only U.S.-based manufacturer of semiconductor memory devices, and its presence in the U.S. is growing. MTI recently announced plans to invest approximately $15 billion through the end of the decade to construct a new memory manufacturing plant in Boise and up to $100 billion over the next 20-plus years to build a fab near Syracuse, New York. Exs. 13-14. MTI's commitment to innovation is evident from its expansive patent portfolio that includes over 54,000 patents. Ex 11 at 2.

11. For over a decade, MTI has been at the forefront of developing new and innovative 3D NAND memory products. In March 2015, MTI launched its first 3D NAND product, a 32-layer high density memory chip. Ex. 15. Doing so required years of research and development before the product launch. These efforts led MTI to file dozens of patents on 3D NAND technology long before the product launch. Indeed, MTI described innovative 3D NAND arrays in patents it filed well before 2015. Exs. 16-17.

12. Since its initial 3D NAND product launch in 2015, MTI has continued to lead the world in 3D NAND innovation by developing and offering chips with greater memory capacity and capabilities. In early 2018, MTI doubled the number of layers in its 3D NAND products, releasing its 64-layer 3D NAND. Ex. 18. Thereafter, in 2019, MTI sampled its 128-layer 3D NAND (Ex. 19 at 7) and, in 2020, MTI was the first company in the world to launch 176-layer 3D NAND. Ex. 20. In July 2022, MTI became the first company to scale its 3D NAND technology to 232-layers in production. Ex 21. MTI has received numerous awards for and widespread recognition of its innovative 3D NAND technology. *See, e.g.*, Exs. 22-24.

The Accused YMTC Products and the YMTC Entities' Infringing Activities

13. YMTC is a global manufacturer and supplier of 3D NAND memory products. YMTC was founded in 2016 and is majority-owned by the Chinese government. Ex. 25. YMTC's founding followed the 2015 announcement of the Made in China 2025 initiative by Chinese President Xi Jinping. Ex. 26. The Made in China 2025 Initiative positioned semiconductors as a critical growth industry for the Chinese economy. *Id.* The Chinese Government's investment platform for funding the expansion of its semiconductor industry is the National Integrated Circuit Industry Investment Fund, more commonly known as the "Big Fund." *Id.*

14. Latecomer YMTC has developed four generations of NAND storage devices since its founding in 2016: a first-generation 3D NAND storage technology incorporating a 32-layer 3D NAND memory array, a second-generation 3D NAND storage technology incorporating at least a 64-layer 3D NAND memory array, a third-generation 3D NAND storage technology incorporating at least a 128-layer 3D NAND memory array, and a fourth generation 3D NAND storage technology incorporating at least a 232-layer 3D NAND memory array. Ex. 27.

15. Unsurprisingly, given MTI's nearly decade long head start over YMTC into 3D NAND memory development, YMTC Entities began to hire NAND engineers from MTI or its affiliates and has hired at least 20 such engineers to date. Indeed, at least five of the named inventors on the YMTC Asserted Patents previously worked as engineers on 3D NAND R&D at Micron before they filed the YMTC Asserted Patents.

16. The YMTC Entities have in the past and continue to directly and/or indirectly use, sell, offer for sale, import, supply, or otherwise distribute into the United States, and provide support for, their 64-layer 3D NAND storage technology and products containing the same (collectively, the "YMTC 64L Accused Products"), including the X1-9050 and X2-9060 and other memory chips (and memory products containing the same) that have the same or similar structures, features, or functionalities, and/or are made by the same or similar Xtacking® 1.0 technology manufacturing processes, as the aforementioned exemplary products.

17. The YMTC Entities have in the past and continue to directly and/or indirectly use, sell, offer for sale, import, supply, or otherwise distribute into the United States, and provide support for, their 128-layer 3D NAND storage technology and products containing the same (collectively, the "YMTC 128L Accused Products"), including the X2-6070 and other memory chips (and memory products containing the same) that have the same or similar structures, features, or functionalities, and/or are made by the same or similar Xtacking® 2.0 technology manufacturing processes, as the aforementioned exemplary product.

18. The YMTC Entities have in the past and continue to directly and/or indirectly use, sell, offer for sale, import, supply, or otherwise distribute into the United States, and provide support for, their 232-layer 3D NAND storage technology and products containing the same

(collectively, the "YMTC 232L Accused Products"), including the X3-9060, X3-9070, and X3-6070 and other memory chips (and memory products containing the same) that have the same or similar structures, features, or functionalities, and/or are made by the same or similar Xtacking® 3.0 technology manufacturing processes, as the aforementioned exemplary product.

19. Upon information and belief, each of the YMTC 64L Accused Products, YMTC 128L Accused Products, and YMTC 232L Accused Products have the same or similar structures, features, or functionalities, and/or are made by the same or similar manufacturing processes insofar as the structures, features, functionalities, and/or manufacturing processes of the Accused Products relate to the MTI Asserted Patents. Claim charts mapping the YMTC 232L Accused Products to the MTI Asserted Patents are provided as Exhibits 2, 4, 6, 8, 10.

20. The YMTC 64L Accused Products, YMTC 128L Accused Products, and YMTC 232L Accused Products are collectively referred to as the "YMTC Accused Storage Products."

21. The YMTC Accused Storage Products are, or are integrated into, devices made, used, sold, offered for sale, imported, supplied, or otherwise distributed in the United States by among others, YMTC, YMTC Inc., YMTC's customers, original equipment manufacturers ("OEMs"), original design manufacturers ("ODMs"), distributors, resellers, and other third parties, including under YMTC's own brand name and under the Lexar brand name. For example, the Lexar NM800 contains or contained one or more of the YMTC 64L Accused Products, the Lexar NM710 contains or contained one or more of the YMTC 128L Accused Products, and the Lexar NM790 contains YMTC 232L Accused Products. Exs. 28-30. Further, in connection with trademark application Serial Number 88496703 filed with the United States Patent and Trademark Office, YMTC submitted a statement of use on May 22, 2020, in which it declared that it first used the YMTC mark in U.S. commerce at least as early as September 9, 2016 in connection with integrated circuits and various other products. YMTC submitted images of integrated circuits bearing the markings "YMTC3GSQDPPKG0" and "PL385008 AAX 1822" as well as images of a YMTC NAND memory solid-state drive identifiable as such by its marking "M.2 NVMe PCIe Gen3.0x4" and its markings "YMTC" and "Xtacking" as specimens showing its use in commerce on chips and

integrated circuits. Ex. 36. Xtacking is described by YMTC as its "innovative 3D NAND technology." Ex. 37.

22. The YMTC Entities actively encourage others, such as their customers and distributors, to make, use, offer to sell, import, supply, or otherwise distribute into the United States the YMTC Accused Storage Products and products containing the YMTC Accused Storage Products. The YMTC Entities maintain a website that advertises the YMTC Accused Storage Products, including identifying the applications for which they can be used, along with specifications for the YMTC Accused Storage Products. *See* Ex. 38 (https://www.ymtc.com/en/buslist.html?cat=35). The YMTC Entities specifically intend for their customers and end-users to use the YMTC Accused Storage Products in such applications and provide instructions and encouragement for their customers and end-users to do so.

23. On information and belief, the YMTC Accused Storage Products are designed to comply with safety standards required for sale or import into the U.S. market and the YMTC Entities make their website and other materials available in the English language.

24. The YMTC Entities know that the YMTC Accused Storage Products and products incorporating the same are used, made, designed, marketed, sold, offered for sale in, and/or imported into, the United States. For example, David Duffin, the US General Manager and Head of International Customer Sales at YMTC is, on information and belief, based in and works out of San Jose, California. Ex. 31. Mr. Duffin advertises that he is "used to regularly and directly interacting with customers." *Id.*

25. From 2016-2019, Mr. Duffin was YMTC's Vice President of Product & Test Engineering and, on information and belief, worked out of San Jose, California. Ex. 31. During this period from 2016-2019, Mr. Duffin was "[l]eading all Product, Test and Assembly Engineering for YMTC." *Id.*

26. Mr. Duffin is listed as the CEO and Secretary of Yangtze Memory Technologies, Inc. Ex. 32. Mr. Duffin apparently has no prior executive-level experience and does not publicly advertise on his LinkedIn profile that he is the CEO of the U.S. arm of YMTC. Ex. 31.

27. Daesik Song, a former MTI Principal Design Engineer, with apparently no former management experience, was hired by YMTC Inc. as a "Director" in 2017 and has, on information and belief, worked from YMTC Inc.'s San Jose offices since that time. Ex. 33. Mr. Song has been and is listed as a YMTC Inc.'s Statement of Information filed with the California Secretary of State. Ex. 32.

28. On information and belief, YMTC controls and has controlled YMTC Inc.

29. YMTC admits that it is "dedicated to the development of memory products for the global market" and that it "maintains ties to Silicon Valley through a wholly-owned subsidiary, Yangtze Memory Technologies, Inc." ECF No. 29 ¶ 24. YMTC Inc. Director Daniel (Tuenlap) Chan recently stated that YMTC's "patent portfolio is designed to protect our innovations in markets that matter to YMTC and its partners." Ex. 34. Thus, YMTC's filing of U.S. patents demonstrates that YMTC considers the United States to be an important market for its products.

30. The YMTC Entities have also directly and/or indirectly imported into the United States, and offered to sell, sold, and used within the United States, the YMTC Accused Storage Products, which are made by a Micron process patented in the United States during the term of the MTI Asserted Patents. YMTC practices the patented processes, or owns or controls, or is owned or controlled by, the person who practices the patented processes. On information and belief, the YMTC Entities directly and/or indirectly sell their products to customers, including customers in this District, in the computer, networking, storage, consumer electronics, solid-state drive, and mobile telecommunications markets. The YMTC Entities encourage their customers to import, sell, resell, and/or offer to sell the YMTC Accused Storage Products in the United States. Exs. 28-30.

31. The YMTC Entities knew and know that MTI has patents in the 3D NAND technology space that are relevant to YMTC's own 3D NAND products. For example, YMTC Inc. Director and former MTI Principal Design Engineer Daesik Song is a named inventor of approximately seven of YMTC's patents or patent applications related to NAND power systems applicable to 3D NAND memory devices, four of which cite MTI prior art patents. YMTC has been issued at least 255 U.S. Patents that cite MTI prior art patents. These YMTC patents include,

for example, U.S. Patent Nos. 10,529,732 titled "Method for forming staircase structure of three-dimensional memory device," 10,658,378 titled "Through array contact (TAC) for three-dimensional memory devices," 10,680,009 titled "Method for forming gate structure of three-dimensional memory device," and 10,727,245 titled "Staircase etch control in forming three-dimensional memory device." Indeed, nearly all, if not all, of these 255 patents relate to 3D NAND memory devices. YMTC Inc. Director Daniel (Tuenlap) Chan is a Deputy General Counsel and the head of YMTC's intellectual property department. Ex. 35, Ex. 32. On information and belief, as head of IP for YMTC, Mr. Chan is and has been well aware of MTI and its patents in the field of 3D NAND technology.

32. Given the large number of former Micron NAND engineers now working at the YMTC Entities, the YMTC Entities have direct knowledge of the MTI Asserted Patents and MTI's underlying technology.

Counterclaim I
(Infringement of U.S. Patent No. 10,475,737)

33. MTI restates and incorporates by reference its allegations in Paragraphs 1 through 32 of its Counterclaims.

34. MTI, owns all right, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,475,737, entitled "Stack of horizontally extending and vertically overlapping features, methods of forming circuitry components, and methods of forming an array of memory cells." A true and correct copy of the '737 patent is attached as Exhibit 1.

35. The '737 patent was duly and legally issued by the United States Patent and Trademark Office on Nov. 12, 2019.

36. The YMTC Entities infringe at least claim 1 of the '737 patent under 35 U.S.C. § 271(a), literally and/or under the doctrine of equivalents, by using, offering for sale, selling, and/or importing into the United States, without authorization, the YMTC Accused Storage Products.

37. The YMTC Accused Storage Products are used to perform and/or practice each and every limitation of at least claim 11 of the '737 patent. A claim chart providing examples of how the YMTC Accused Storage Products practice each limitation of at least claim 11 of the '737 patent is attached as Exhibit 2 hereto and is incorporated by reference herein.

38. The YMTC Entities also actively induce infringement of at least claim 11 of the '737 patent under 35 U.S.C. § 271(b), and have done so since at least the filing of these counterclaims, by actively encouraging others to infringe (such infringement by others being by way of using, selling, offering to sell, or importing into the United States the YMTC Accused Storage Products).

39. Since at least the filing of these counterclaims, the YMTC Entities have known of the '737 patent and their infringement thereof. Since before the filing of these counterclaims, the YMTC Entities have had knowledge of MTI's patent portfolio with respect to 3D NAND technology and that portfolio's relevance and application to the YMTC Entities' own products. Accordingly, discovery may reveal the YMTC Entities knew of the '737 patent and the YMTC Entities unauthorized use thereof before the filing of these counterclaims.

40. The YMTC Entities know (or believe that there is a high probability) that their actions are inducing infringement and are intended to induce infringement. For example, the YMTC Entities encourage, train, instruct, and provide support and technical assistance to others to directly infringe the '737 patent by contracting with, encouraging, and instructing third parties, including equipment and design manufacturers, device manufacturers, distributors, customers, and other third parties to use, sell, offer for sale, and/or import into the United States, the YMTC Accused Storage Products and products that incorporate the YMTC Accused Storage Products. For instance, the YMTC Entities publish and provide technical materials, product specifications, and promotional literature for the YMTC Accused Storage Products that instruct and encourage the YMTC Entities' customers and other third parties to integrate the YMTC Accused Storage Products into products made, used, sold, offered for sale, and/or imported into the United States, and work with customers and potential customers to design their products using the YMTC Accused Storage Products with knowledge that those products will be used and sold in the United States.

41. Since at least the filing of these counterclaims, the YMTC Entities' infringement has been willful.

42. As a result of YMTC Entities' infringement of the '737 patent, MTI is entitled to monetary damages in an amount adequate to compensate for YMTC Entities' infringement, but in no event less than a reasonable royalty for the use made of the invention by the YMTC Entities, together with interest and costs as fixed by the Court.

Counterclaim II
(Infringement of U.S. Patent No. 8,945,996)

43. MTI restates and incorporates by reference its allegations in Paragraphs 1 through 42 of its Counterclaims.

44. MTI, owns all right, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 8,945,996, entitled "Methods of forming circuitry components and methods of forming an array of memory cells." A true and correct copy of the '996 patent is attached as Exhibit 3.

45. The '996 patent was duly and legally issued by the United States Patent and Trademark Office on Feb. 3, 2015.

46. The YMTC Entities infringe at least claim 1 of the '996 patent under 35 U.S.C. § 271(a), literally and/or under the doctrine of equivalents, by using, offering for sale, selling, and/or importing into the United States, without authorization, the YMTC Accused Storage Products.

47. The YMTC Entities infringe at least claim 1 of the '996 patent under 35 U.S.C. § 271(g), literally and/or under the doctrine of equivalents, by directly or indirectly importing into the United States the YMTC Accused Storage Products, which Products are made outside the United States using the patented process of at least claim 1 of the '996 patent, are not materially changed by subsequent processes, and are not a trivial and nonessential component of another product.

48. The YMTC Accused Storage Products are made with, used to perform, and/or practice each and every limitation of at least claim 1 of the '996 patent. A claim chart providing

examples of how the YMTC Accused Storage Products practice each limitation of at least claim 1 of the '996 patent is attached as Exhibit 4 hereto and is incorporated by reference herein.

49. The YMTC Entities also actively induce infringement of at least claim 1 of the '996 patent under 35 U.S.C. § 271(b), and have done so since at least the filing of these counterclaims, by actively encouraging others to infringe (such infringement by others being by way of using, selling, offering to sell, or importing into the United States the YMTC Accused Storage Products).

50. Since at least the filing of these counterclaims, the YMTC Entities have known of the '996 patent and their infringement thereof. Since before the filing of these counterclaims, the YMTC Entities have had knowledge of MTI's patent portfolio with respect to 3D NAND technology and that portfolio's relevance and application to YMTC Entities' own products. Accordingly, discovery may reveal the YMTC Entities knew of the '996 patent and the YMTC Entities' unauthorized use thereof before the filing of these counterclaims.

51. The YMTC Entities know (or believe that there is a high probability) that their actions are inducing infringement and are intended to induce infringement. For example, the YMTC Entities encourage, train, instruct, and provide support and technical assistance to others to directly infringe the '996 patent by contracting with, encouraging, and instructing third parties, including equipment and design manufacturers, device manufacturers, distributors, customers, and other third parties to use, sell, offer for sale, and/or import into the United States, the YMTC Accused Storage Products and products that incorporate the YMTC Accused Storage Products. For instance, the YMTC Entities publish and provide technical materials, product specifications, and promotional literature for the YMTC Accused Storage Products that instruct and encourage the YMTC Entities' customers and other third parties to integrate the YMTC Accused Storage Products into products made, used, sold, offered for sale, and/or imported into the United States, and work with customers and potential customers to design their products using the YMTC Accused Storage Products with knowledge that those products will be used and sold in the United States.

52. Since at least the filing of these counterclaims, the YMTC Entities' infringement has been willful.

53. As a result of YMTC Entities' infringement of the '996 patent, MTI is entitled to monetary damages in an amount adequate to compensate for YMTC Entities' infringement, but in no event less than a reasonable royalty for the use made of the invention by the YMTC Entities, together with interest and costs as fixed by the Court.

Counterclaim III
(Infringement of U.S. Patent No. 8,803,214)

54. MTI restates and incorporates by reference its allegations in Paragraphs 1 through 53 of its Counterclaims.

55. MTI, owns all right, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 8,803,214, entitled "Three dimensional memory and methods of forming the same." A true and correct copy of the '214 patent is attached as Exhibit 5.

56. The '214 patent was duly and legally issued by the United States Patent and Trademark Office on Aug. 12, 2014.

57. The YMTC Entities infringe at least claim 1 of the '214 patent under 35 U.S.C. § 271(a), literally and/or under the doctrine of equivalents, by using, offering for sale, selling, and/or importing into the United States, without authorization, the YMTC Accused Storage Products.

58. The YMTC Accused Storage Products are used to perform and/or practice each and every limitation of at least claim 1 of the '214 patent. A claim chart providing examples of how the YMTC Accused Storage Products practice each limitation of at least claim 1 of the '214 patent is attached as Exhibit 6 hereto and is incorporated by reference herein.

59. The YMTC Entities also actively induce infringement of at least claim 1 of the '214 patent under 35 U.S.C. § 271(b), and have done so since at least the filing of these counterclaims, by actively encouraging others to infringe (such infringement by others being by way of using, selling, offering to sell, or importing into the United States the YMTC Accused Storage Products).

60. Since at least the filing of these counterclaims, the YMTC Entities have known of the '214 patent and its infringement thereof. Since before the filing of these counterclaims, the

YMTC Entities have had knowledge of MTI's patent portfolio with respect to 3D NAND technology and that portfolio's relevance and application to the YMTC Entities' own products. Accordingly, discovery may reveal the YMTC Entities knew of the '214 patent and the YMTC Entities' unauthorized use thereof before the filing of these counterclaims.

61. The YMTC Entities know (or believe that there is a high probability) that their actions are inducing infringement and are intended to induce infringement. For example, the YMTC Entities encourage, train, instruct, and provide support and technical assistance to others to directly infringe the '214 patent by contracting with, encouraging, and instructing third parties, including equipment and design manufacturers, device manufacturers, distributors, customers, and other third parties to use, sell, offer for sale, and/or import into the United States, the YMTC Accused Storage Products and products that incorporate the YMTC Accused Storage Products. For instance, the YMTC Entities publish and provide technical materials, product specifications, and promotional literature for the YMTC Accused Storage Products that instruct and encourage the YMTC Entities' customers and other third parties to integrate the YMTC Accused Storage Products into products made, used, sold, offered for sale, and/or imported into the United States, and works with customers and potential customers to design their products using the YMTC Accused Storage Products with knowledge that those products will be used and sold in the United States.

62. Since at least the filing of these counterclaims, the YMTC Entities' infringement has been willful.

63. As a result of YMTC Entities' infringement of the '214 patent, MTI is entitled to monetary damages in an amount adequate to compensate for YMTC Entities' infringement, but in no event less than a reasonable royalty for the use made of the invention by the YMTC Entities, together with interest and costs as fixed by the Court.

Counterclaim IV
(Infringement of U.S. Patent No. 10,872,903)

64. MTI restates and incorporates by reference its allegations in Paragraphs 1 through 63 of its Counterclaims.

65. MTI, owns all right, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,872,903, entitled "Three dimensional memory and methods of forming the same." A true and correct copy of the '903 patent is attached as Exhibit 7.

66. The '903 patent was duly and legally issued by the United States Patent and Trademark Office on Dec. 22, 2020.

67. The YMTC Entities infringe at least claim 1 of the '903 patent under 35 U.S.C. § 271(a), literally and/or under the doctrine of equivalents, by using, offering for sale, selling, and/or importing into the United States, without authorization, the YMTC Accused Storage Products.

68. The YMTC Accused Storage Products are used to perform and/or practice each and every limitation of at least claim 1 of the '903 patent. A claim chart providing examples of how the YMTC Accused Storage Products practice each limitation of at least claim 1 of the '903 patent is attached as Exhibit 8 hereto and is incorporated by reference herein.

69. The YMTC Entities also actively induce infringement of at least claim 1 of the '903 patent under 35 U.S.C. § 271(b) and have done so since at least the filing of these counterclaims, by actively encouraging others to infringe (such infringement by others being by way of using, selling, offering to sell, or importing into the United States the YMTC Accused Storage Products).

70. Since at least the filing of these counterclaims, the YMTC Entities have known of the '903 patent and their infringement thereof. Since before the filing of these counterclaims, the YMTC Entities have had knowledge of MTI's patent portfolio with respect to 3D NAND technology and that portfolio's relevance and application to the YMTC Entities' own products. Accordingly, discovery may reveal the YMTC Entities knew of the '903 patent and the YMTC Entities' unauthorized use thereof before the filing of these counterclaims.

71. The YMTC Entities know (or believe that there is a high probability) that their actions are inducing infringement and are intended to induce infringement. For example, the YMTC Entities encourage, train, instruct, and provide support and technical assistance to others to directly infringe the '903 patent by contracting with, encouraging, and instructing third parties,

including equipment and design manufacturers, device manufacturers, distributors, customers, and other third parties to use, sell, offer for sale, and/or import into the United States, the YMTC Accused Storage Products and products that incorporate the YMTC Accused Storage Products. For instance, the YMTC Entities publish and provide technical materials, product specifications, and promotional literature for the YMTC Accused Storage Products that instruct and encourage the YMTC Entities' customers and other third parties to integrate the YMTC Accused Storage Products into products made, used, sold, offered for sale, and/or imported into the United States, and works with customers and potential customers to design their products using the YMTC Accused Storage Products with knowledge that those products will be used and sold in the United States.

72. Since at least the filing of these counterclaims, the YMTC Entities' infringement has been willful.

73. As a result of YMTC Entities' infringement of the '903 patent, MTI is entitled to monetary damages in an amount adequate to compensate for YMTC Entities' infringement, but in no event less than a reasonable royalty for the use made of the invention by the YMTC Entities, together with interest and costs as fixed by the Court.

Counterclaim V
(Infringement of U.S. Patent No. 10,373,974)

74. MTI restates and incorporates by reference its allegations in Paragraphs 1 through 73 of its Counterclaims.

75. MTI, owns all right, title, and interest, including the right to recover damages for past, present, and future infringement, in and to U.S. Patent No. 10,373,974, entitled "Microelectronic devices and related methods." A true and correct copy of the '974 patent is attached as Exhibit 9.

76. The '974 patent was duly and legally issued by the United States Patent and Trademark Office on Aug. 6, 2019.

77. The YMTC Entities infringe at least claim 1 of the '974 patent under 35 U.S.C. § 271(a), literally and/or under the doctrine of equivalents, by using, offering for sale, selling,

and/or importing into the United States, without authorization, the YMTC Accused Storage Products.

78. The YMTC Accused Storage Products are used to perform and/or practice each and every limitation of at least claim 1 of the '974 patent. A claim chart providing examples of how the YMTC Accused Storage Products practice each limitation of at least claim 1 of the '974 patent is attached as Exhibit 10 hereto and is incorporated by reference herein.

79. The YMTC Entities also actively induce infringement of at least claim 1 of the '974 patent under 35 U.S.C. § 271(b), and have done so since at least the filing of these counterclaims, by actively encouraging others to infringe (such infringement by others being by way of using, selling, offering to sell, or importing into the United States the YMTC Accused Storage Products).

80. Since at least the filing of these counterclaims, the YMTC Entities have known of the '974 patent and their infringement thereof. Since before the filing of these counterclaims, the YMTC Entities have had knowledge of MTI's patent portfolio with respect to 3D NAND technology and that portfolio's relevance and application to the YMTC Entities' own products. Accordingly, discovery may reveal the YMTC Entities knew of the '974 patent and the YMTC Entities' unauthorized use thereof before the filing of these counterclaims.

81. The YMTC Entities know (or believe that there is a high probability) that their actions are inducing infringement and are intended to induce infringement. For example, the YMTC Entities encourage, train, instruct, and provide support and technical assistance to others to directly infringe the '974 patent by contracting with, encouraging, and instructing third parties, including equipment and design manufacturers, device manufacturers, distributors, customers, and other third parties to use, sell, offer for sale, and/or import into the United States, the YMTC Accused Storage Products and products that incorporate the YMTC Accused Storage Products. For instance, the YMTC Entities publish and provide technical materials, product specifications, and promotional literature for the YMTC Accused Storage Products that instruct and encourage the YMTC Entities' customers and other third parties to integrate the YMTC Accused Storage Products into products made, used, sold, offered for sale, and/or imported into the United States, and works

with customers and potential customers to design their products using the YMTC Accused Storage Products with knowledge that those products will be used and sold in the United States.

82. Since at least the filing of these counterclaims, the YMTC Entities' infringement has been willful.

83. As a result of YMTC Entities' infringement of the '974 patent, MTI is entitled to monetary damages in an amount adequate to compensate for YMTC Entities' infringement, but in no event less than a reasonable royalty for the use made of the invention by the YMTC Entities, together with interest and costs as fixed by the Court.

DEMAND FOR A JURY TRIAL

Defendants and counterclaim plaintiff request a jury trial on all issues related to YMTC's claims and MTI's counterclaims that are so triable.

PRAYER FOR RELIEF OF DEFENDANTS AND COUNTERCLAIM PLAINTIFF

WHEREFORE, having fully answered, defendants and counterclaim plaintiff pray that the Court enter judgment as follows:

A. A judgment in favor of Micron and against YMTC on all of YMTC's claims, including a dismissal with prejudice of all of YMTC's claims;

B. A judgment declaring that Micron has not infringed, contributed to the infringement of, or induced others to infringe, either directly or indirectly, literally or under the doctrine of equivalents, any valid claims of the YMTC Asserted Patents;

C. A judgment declaring that the YMTC Asserted Patents are invalid;

D. A judgment declaring that this YMTC's case against Micron is exceptional and an award to Micron of its reasonable costs and expenses of litigation, including attorneys' fees and expert witness fees;

E. A judgment in favor of MTI and against the YMTC Entities on all of its Counterclaims;

F. A judgment in favor of MTI that the YMTC Entities have infringed and are infringing, either literally and/or under the doctrine of equivalents, one or more claims of each of the MTI Asserted Patents;

G. An order pursuant to 35 U.S.C. § 283 enjoining the YMTC Entities and their subsidiaries, parents, divisions, affiliates, successors, assigns, transferees, officers, directors, attorneys, agents, servants, employees, privies, and all other persons in active concert or participation with any of the foregoing, from continued acts of infringement of the claims of the MTI Asserted Patents;

H. A judgment and order requiring the YMTC Entities to pay Micron its damages, costs, expenses, and pre-judgment and post-judgment interest for the YMTC Entities' infringement;

I. If a permanent injunction is not granted, then a judicial determination of the conditions for the YMTC Entities future infringement, such as an ongoing royalty;

J. A determination that the YMTC Entities infringement has been willful;

K. A determination that the damages award against the YMTC Entities be increased pursuant to 35 U.S.C. § 284 because of the willful and deliberate nature of the YMTC Entities' conduct;

L. A judgment declaring that MTI's case against the YMTC Entities is exceptional and an award to MTI of its reasonable costs and expenses of litigation, including attorneys' fees and expert witness fees;

M. All other relief that the Court deems just and proper.

Dated: February 16, 2024

ORRICK, HERRINGTON & SUTCLIFFE LLP

By: */s/ Jared Bobrow*
Jared Bobrow

Attorneys for Defendants
Micron Technology, Inc., and
Micron Consumer Products Group LLC

Exhibit 1

US010475737B2

(12) **United States Patent**
Tang et al.

(10) **Patent No.: US 10,475,737 B2**
(45) **Date of Patent: *Nov. 12, 2019**

(54) **STACK OF HORIZONTALLY EXTENDING AND VERTICALLY OVERLAPPING FEATURES, METHODS OF FORMING CIRCUITRY COMPONENTS, AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS**

(71) Applicant: **Micron Technology, Inc.**, Boise, ID (US)

(72) Inventors: **Sanh D. Tang**, Boise, ID (US); **Roger W. Lindsay**, Boise, ID (US); **Krishna K. Parat**, Palo Alto, CA (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **15/900,188**

(22) Filed: **Feb. 20, 2018**

(65) **Prior Publication Data**

US 2018/0175059 A1 Jun. 21, 2018

Related U.S. Application Data

(60) Continuation of application No. 15/397,919, filed on Jan. 4, 2017, now Pat. No. 9,929,175, which is a (Continued)

(51) **Int. Cl.**
H01L 27/1157 (2017.01)
H01L 23/52 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 23/52*** (2013.01); ***G11C 13/0007*** (2013.01); ***H01L 23/528*** (2013.01);
(Continued)

(58) **Field of Classification Search**
CPC . H01L 27/10; H01L 27/101; H01L 27/11556; H01L 27/1157; H01L 27/11582;
(Continued)

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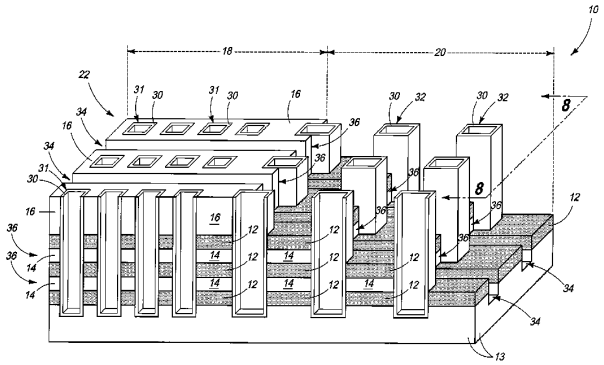
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Primary Examiner — Cuong Q Nguyen
(74) *Attorney, Agent, or Firm* — Wells St. John P.S.

(57) **ABSTRACT**

A method of forming circuitry components includes forming a stack of horizontally extending and vertically overlapping features. The stack has a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures are formed vertically through the features in the primary portion and dummy structures are formed vertically through the features in the end portion. Horizontally elongated openings are formed through the features to form horizontally elongated and vertically overlapping lines from material of the features. The lines individually extend from the primary portion into the end portion, and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures. Sacrificial material that is elevationally between the lines is at least partially removed in the primary and end portions laterally between the horizontally elongated openings. Other aspects and implementations are disclosed.

22 Claims, 18 Drawing Sheets



Related U.S. Application Data

continuation of application No. 15/095,208, filed on Apr. 11, 2016, now Pat. No. 9,564,471, which is a division of application No. 14/602,559, filed on Jan. 22, 2015, now Pat. No. 9,318,430, which is a division of application No. 13/085,083, filed on Apr. 12, 2011, now Pat. No. 8,945,996.

(51) **Int. Cl.**

H01L 27/10	(2006.01)
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H01L 27/11556	(2017.01)
H01L 27/11582	(2017.01)
H01L 27/24	(2006.01)
H01L 45/00	(2006.01)
H01L 27/11524	(2017.01)

(52) **U.S. Cl.**

CPC ***H01L 27/10*** (2013.01); ***H01L 27/101*** (2013.01); ***H01L 27/1157*** (2013.01); ***H01L 27/11556*** (2013.01); ***H01L 27/11582*** (2013.01); ***H01L 27/249*** (2013.01); ***H01L 45/142*** (2013.01); ***H01L 45/143*** (2013.01); ***H01L 45/144*** (2013.01); ***H01L 45/146*** (2013.01); ***H01L 45/147*** (2013.01); *G11C 2213/11* (2013.01); *G11C 2213/31* (2013.01); *G11C 2213/32* (2013.01); *G11C 2213/71* (2013.01); *G11C 2213/75* (2013.01); *H01L 27/11524* (2013.01); *H01L 45/141* (2013.01); *H01L 45/145* (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**

CPC H01L 27/249; H01L 29/66825; H01L 29/788

See application file for complete search history.

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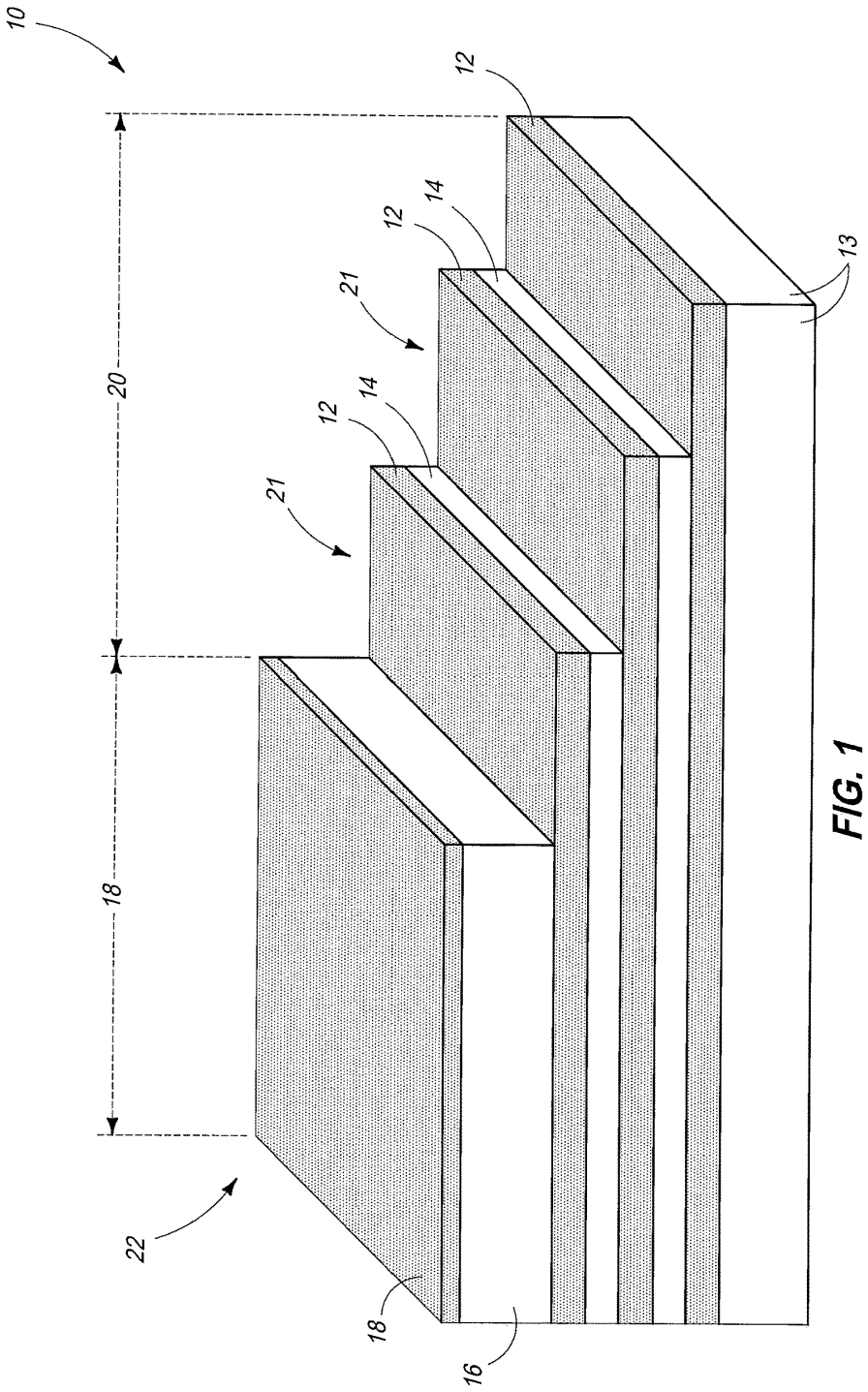


FIG. 1

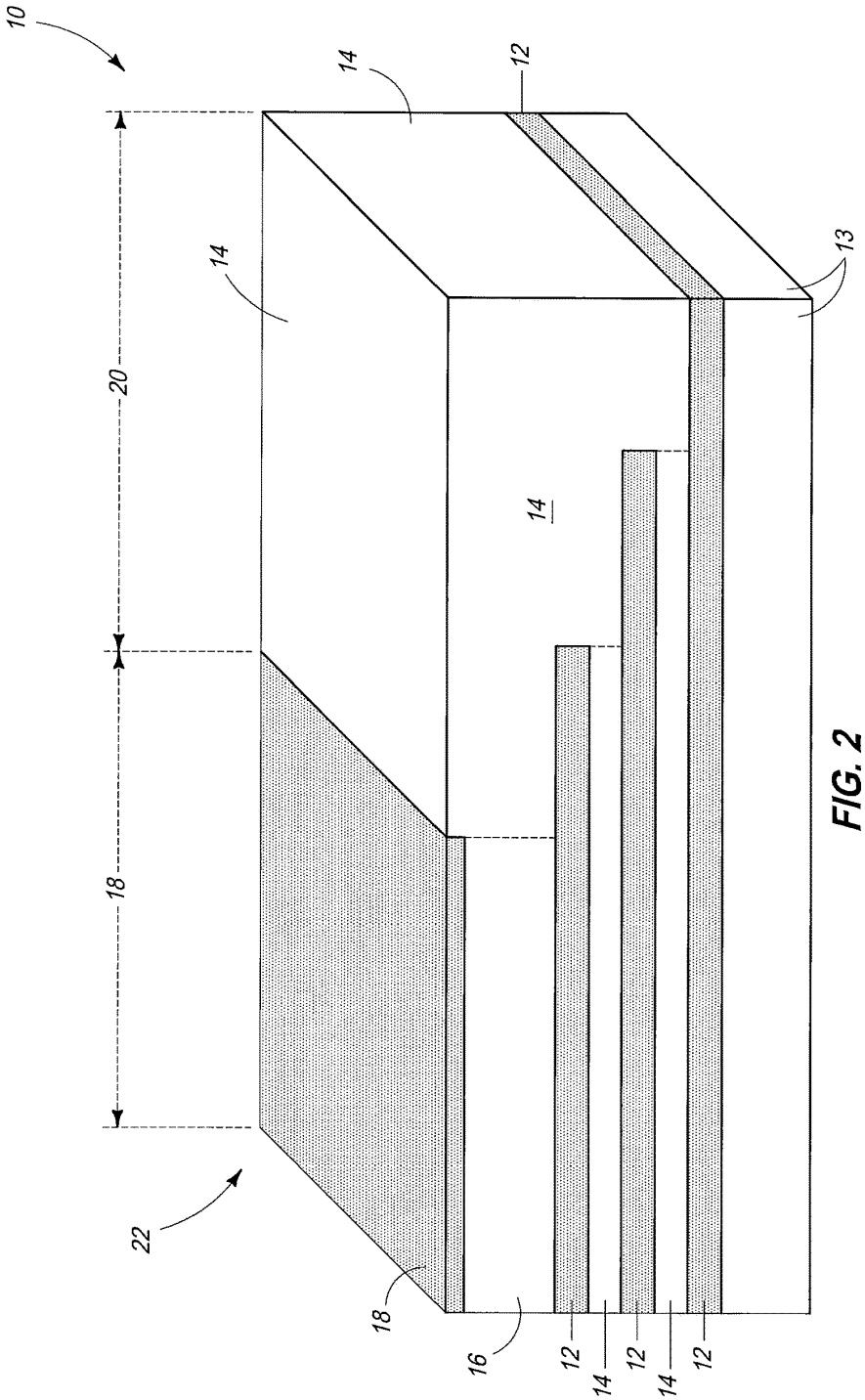
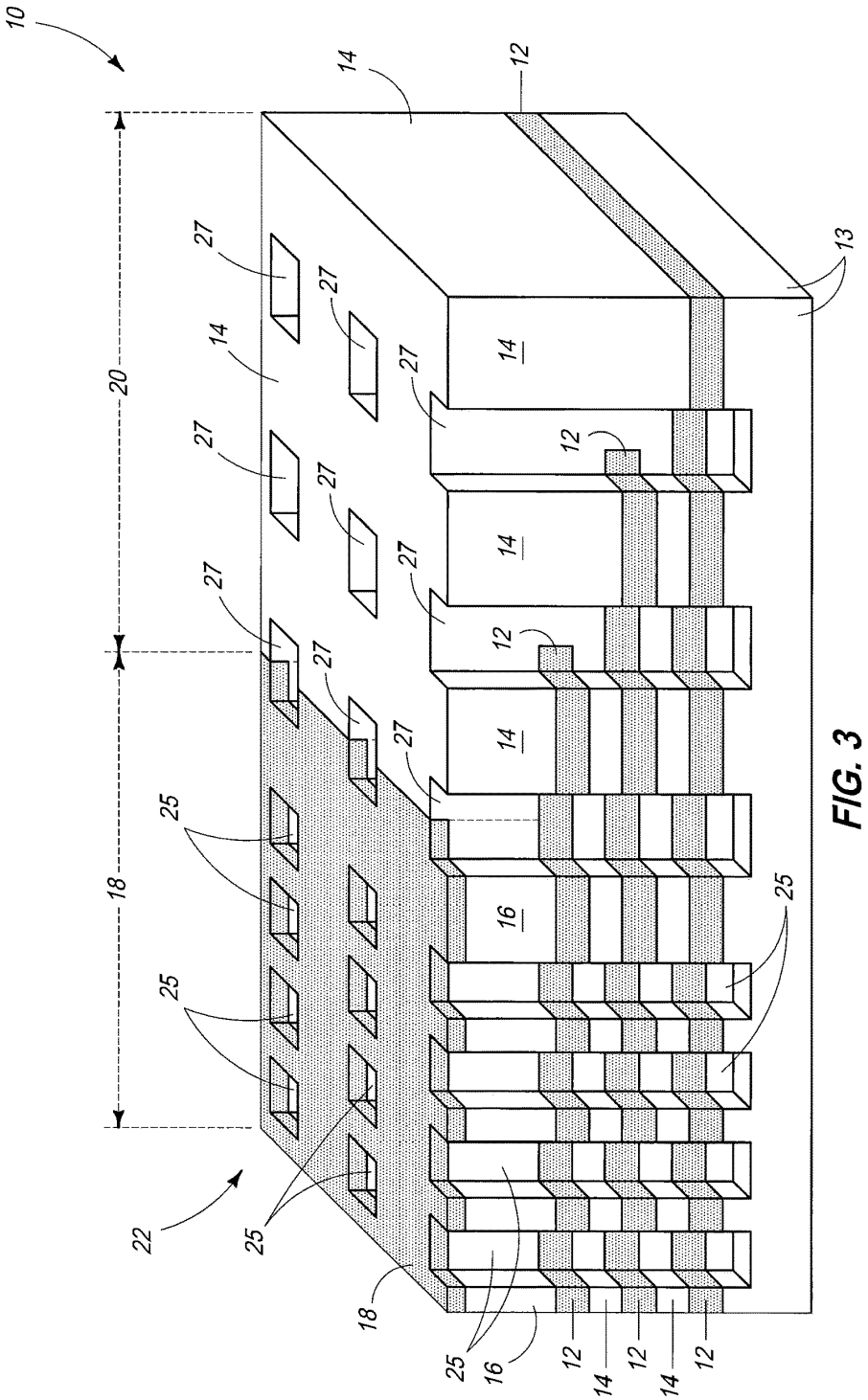


FIG. 2


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FIG. 3

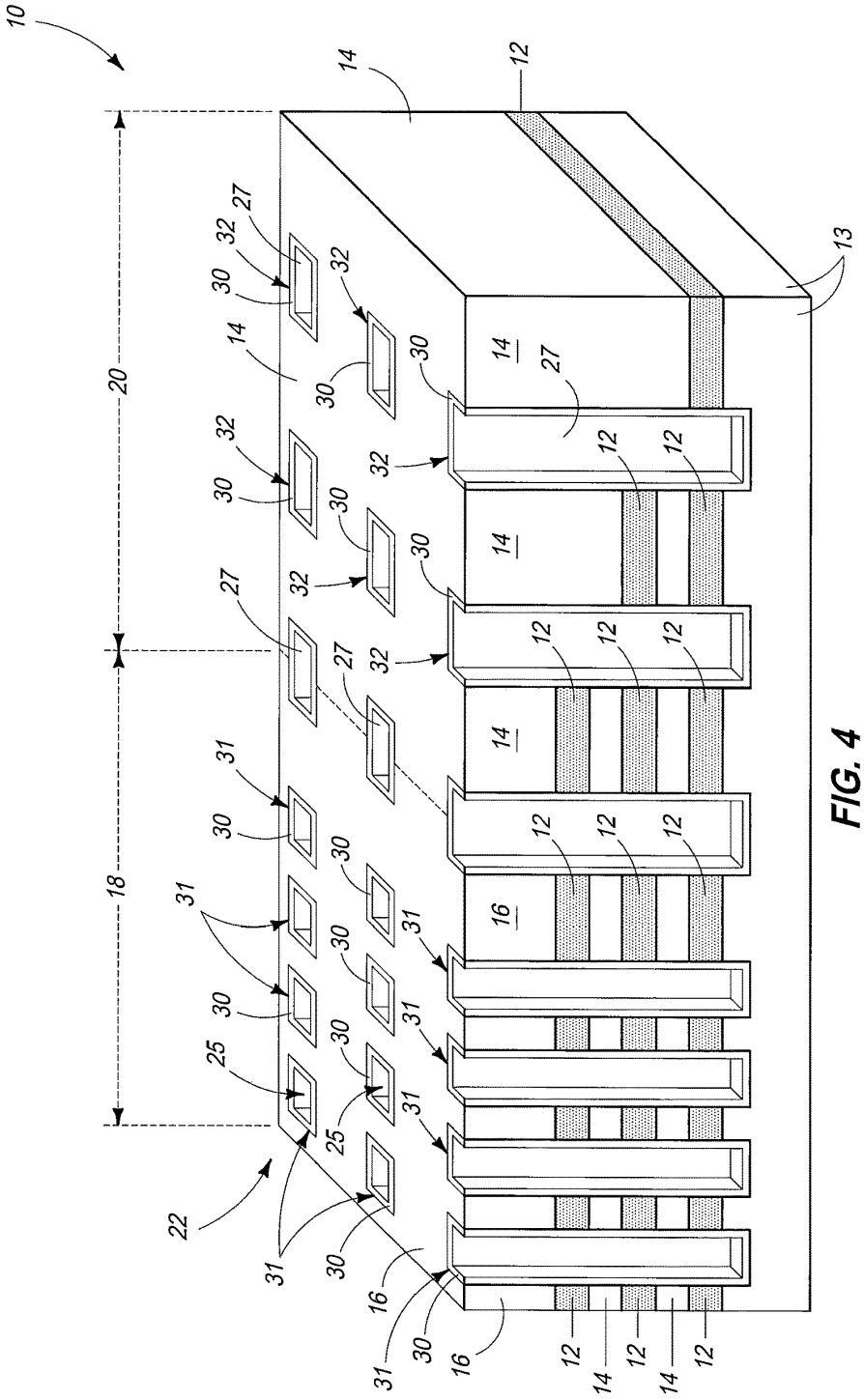


FIG. 4

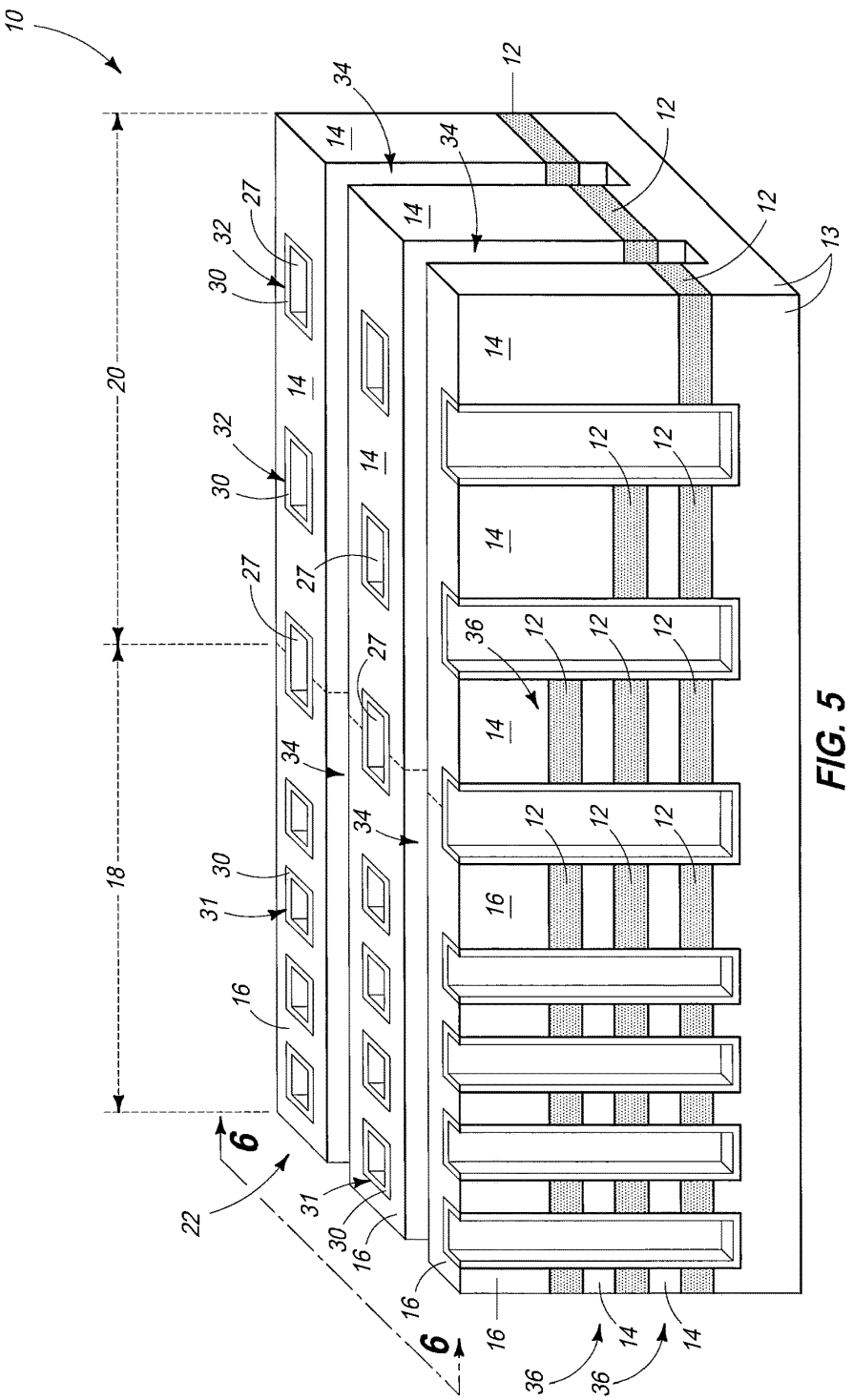


FIG. 5

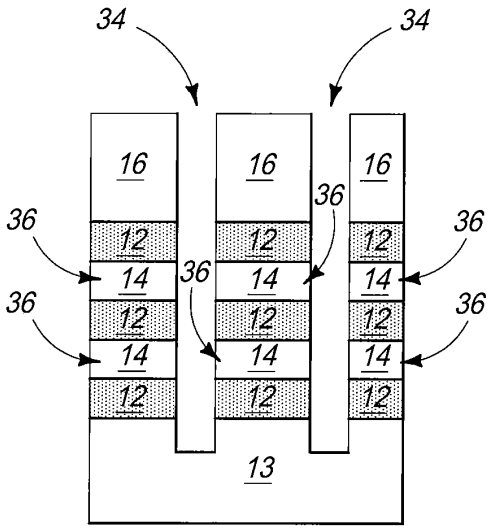


FIG. 6

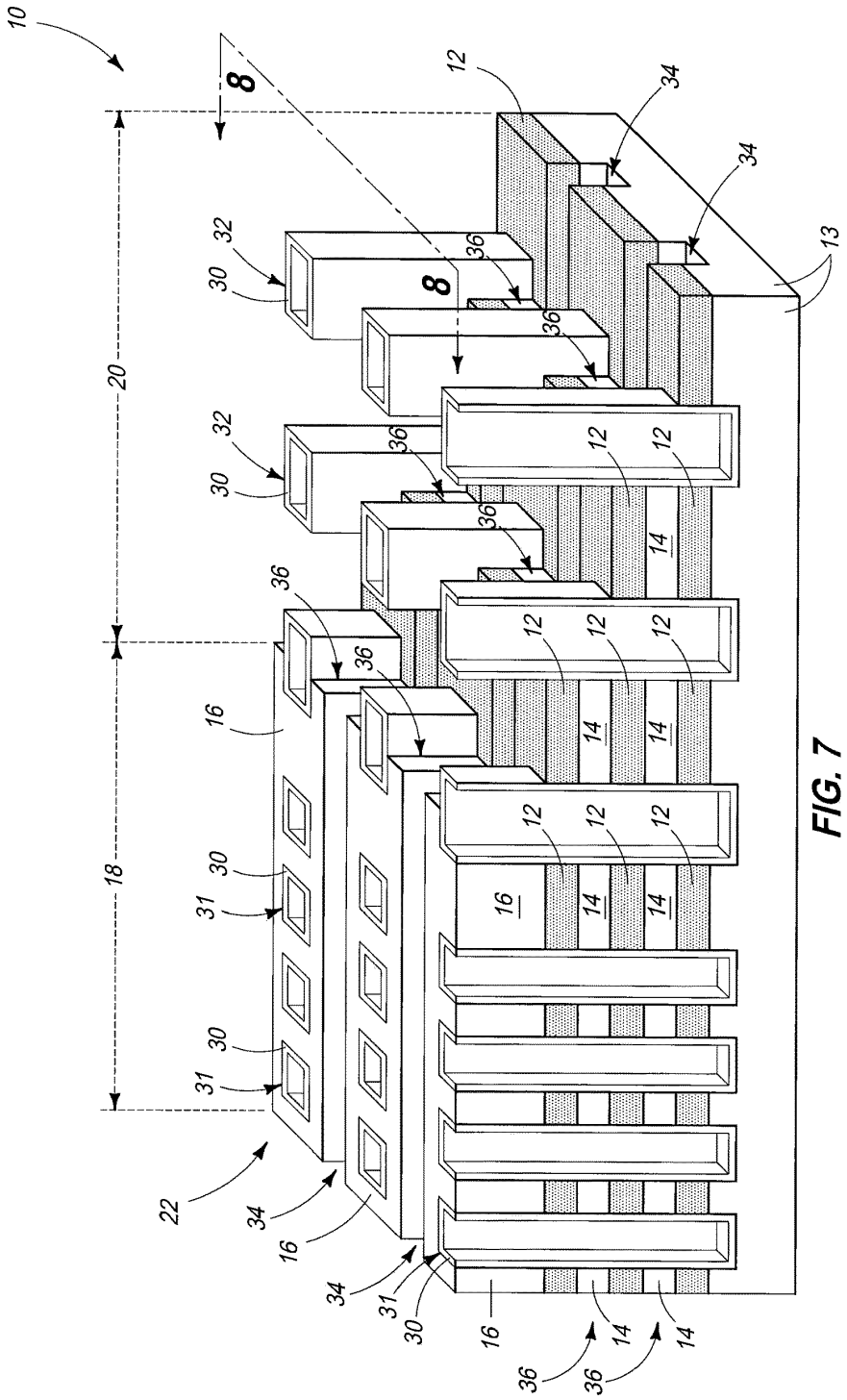

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FIG. 7

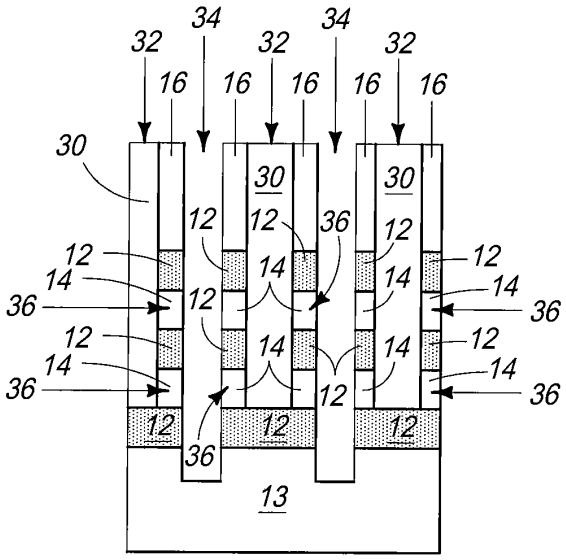

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FIG. 8

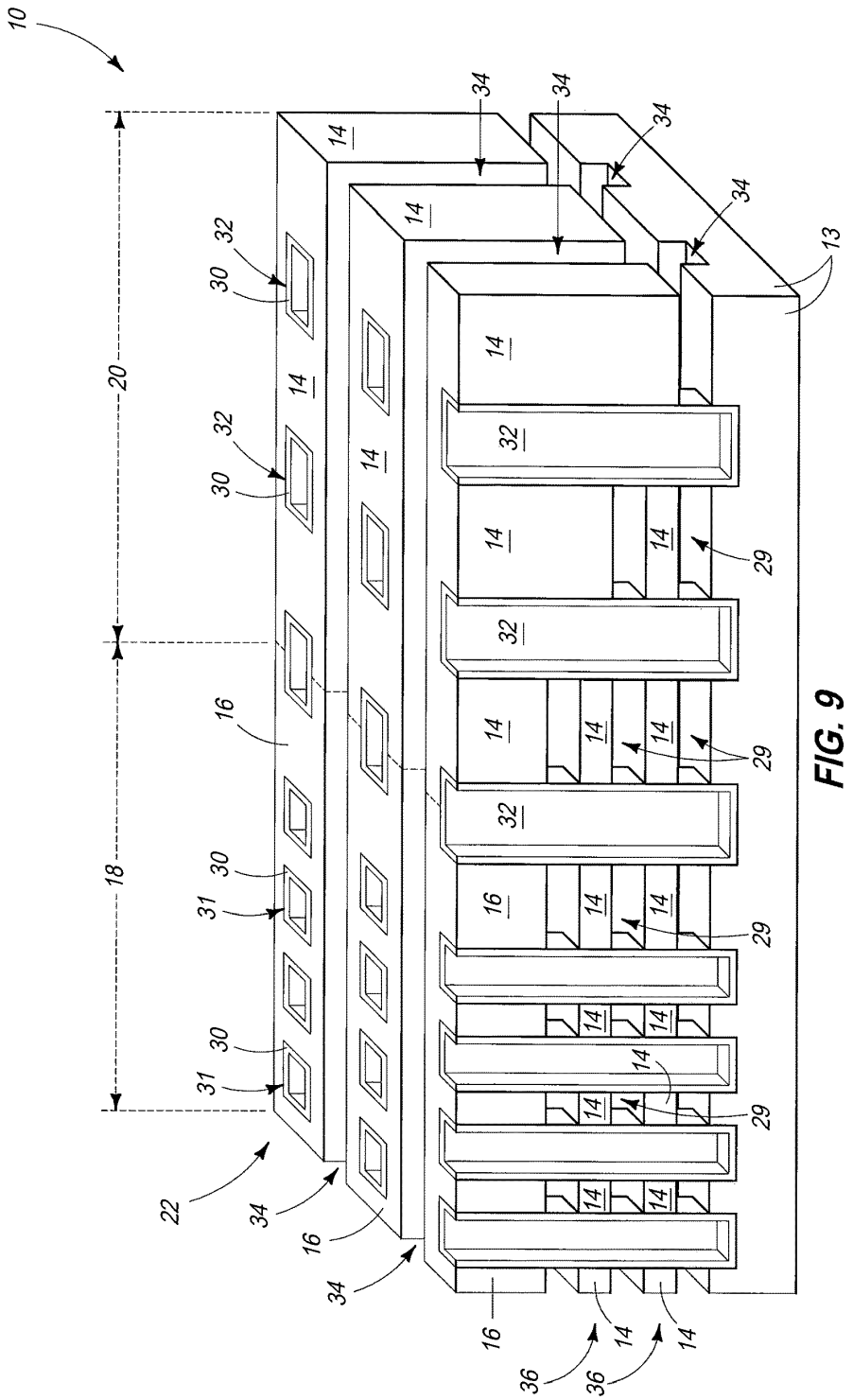


FIG. 9

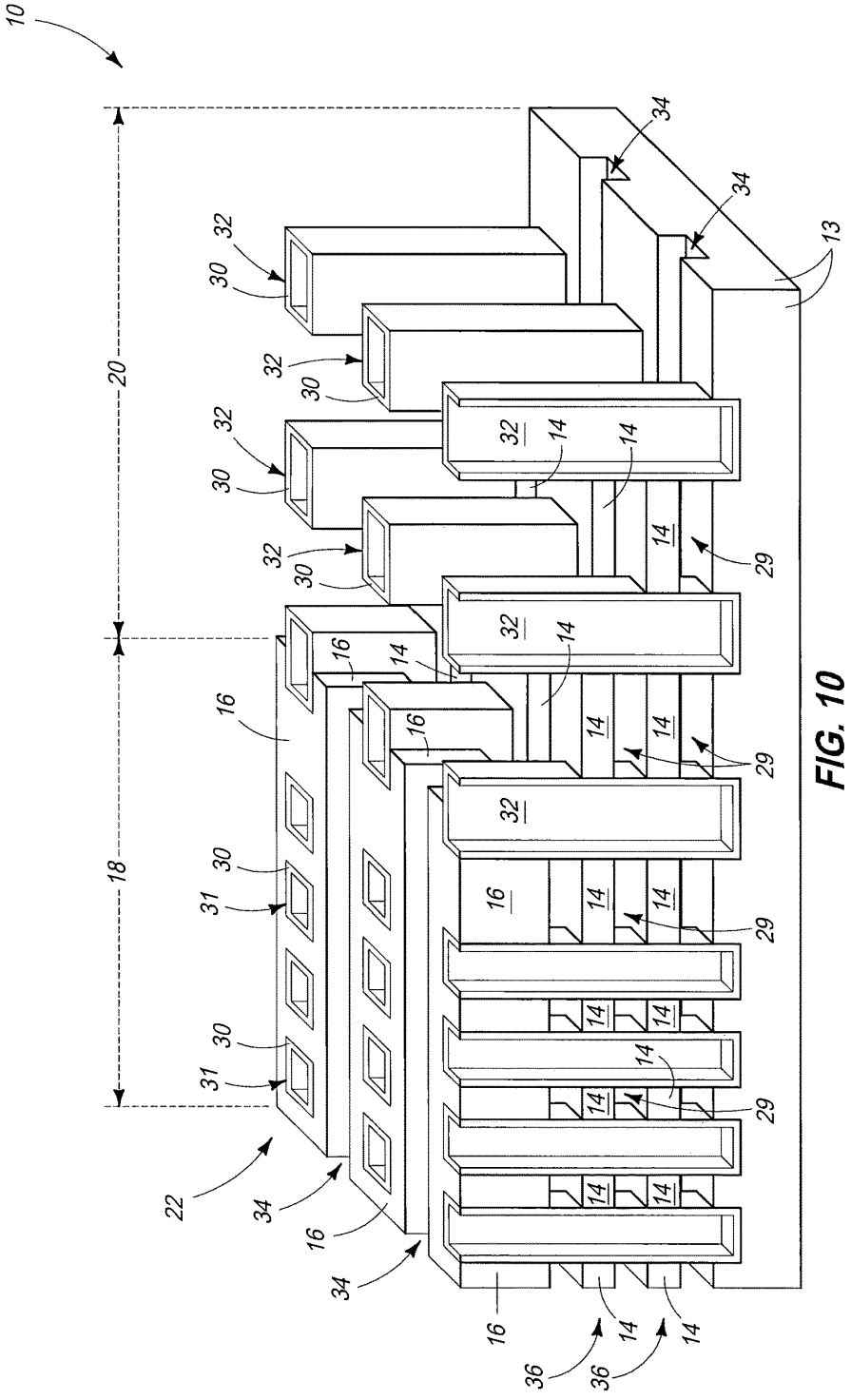


FIG. 10

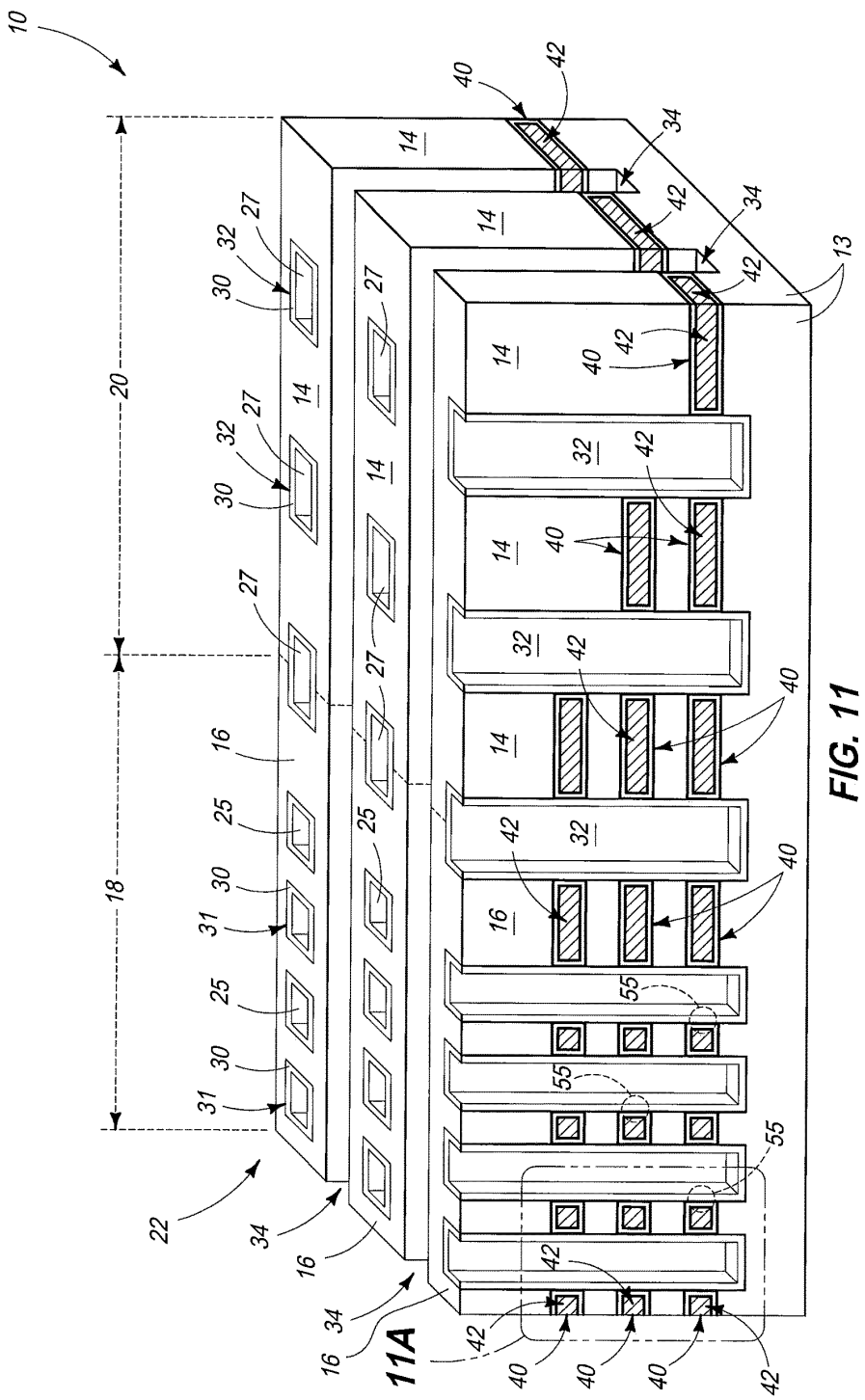


FIG. 11

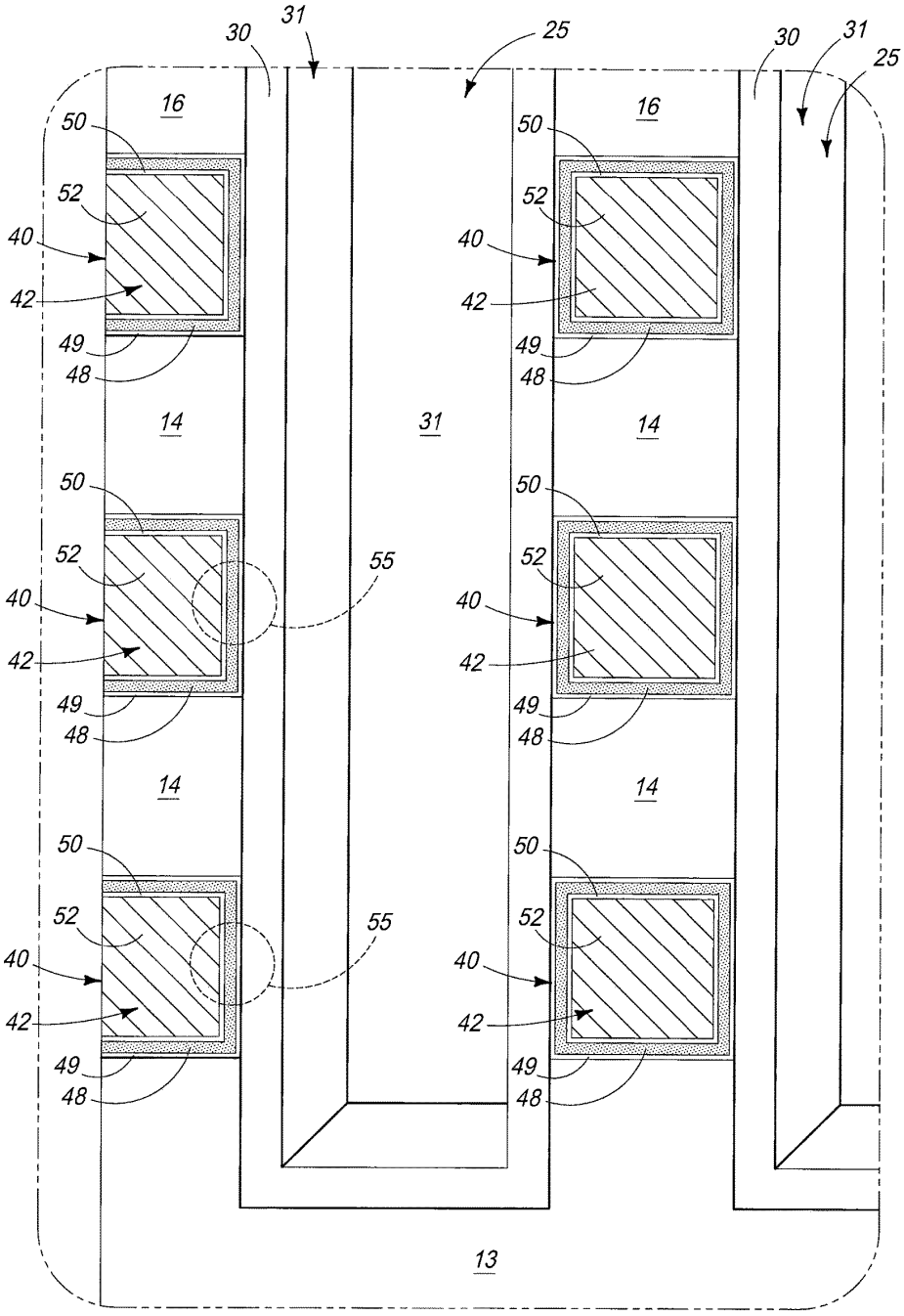


FIG. 11A

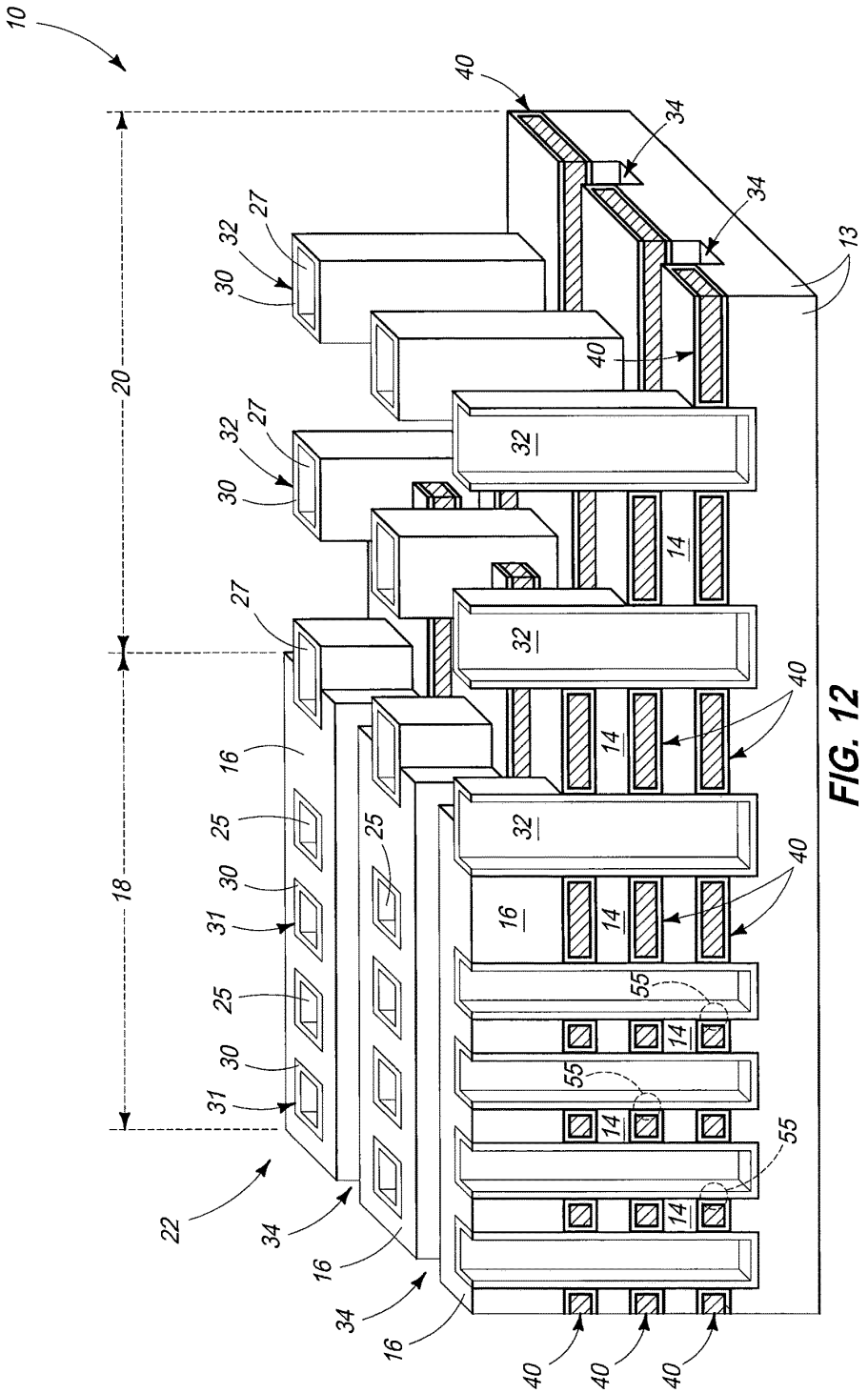


FIG. 12

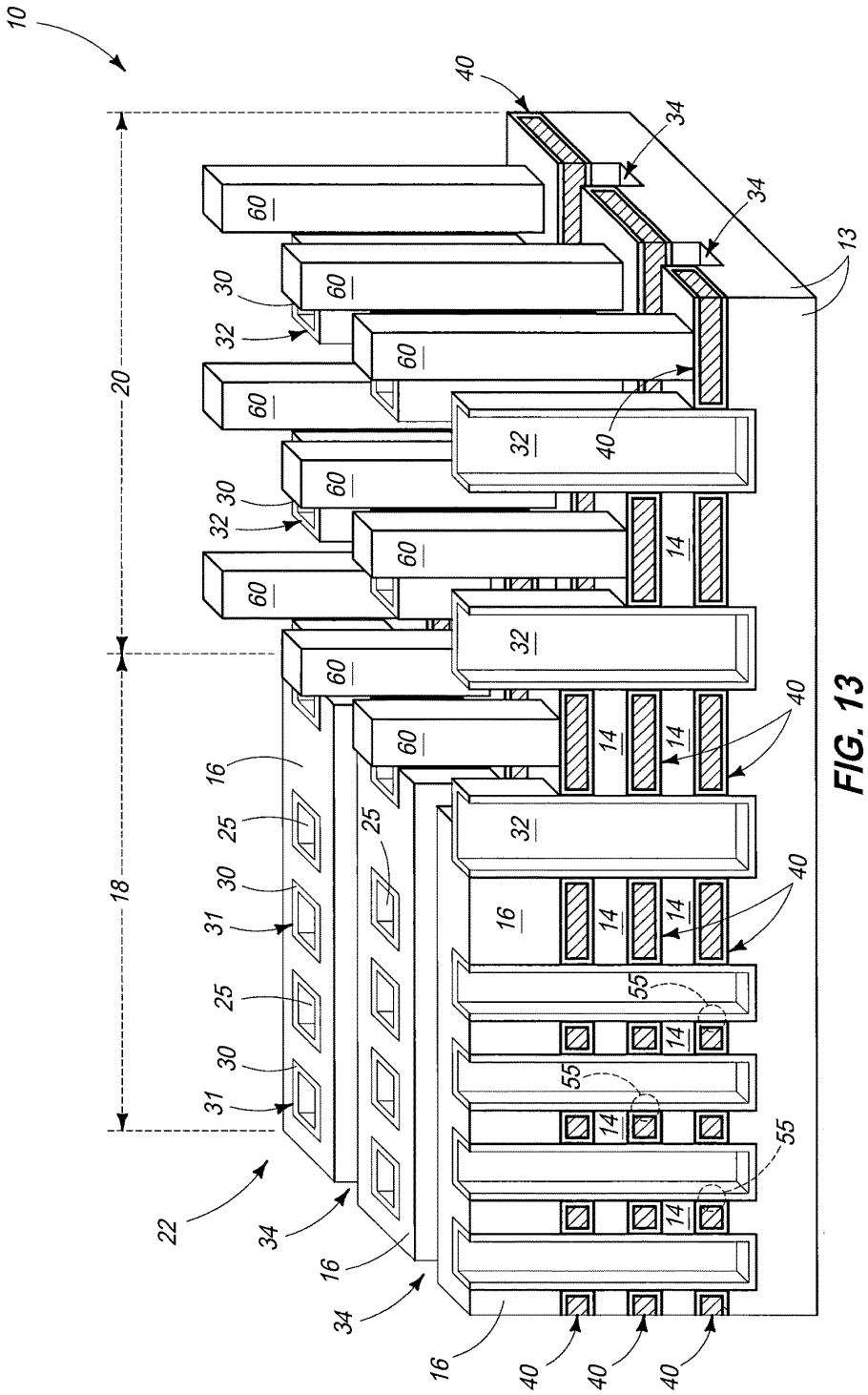


FIG. 13

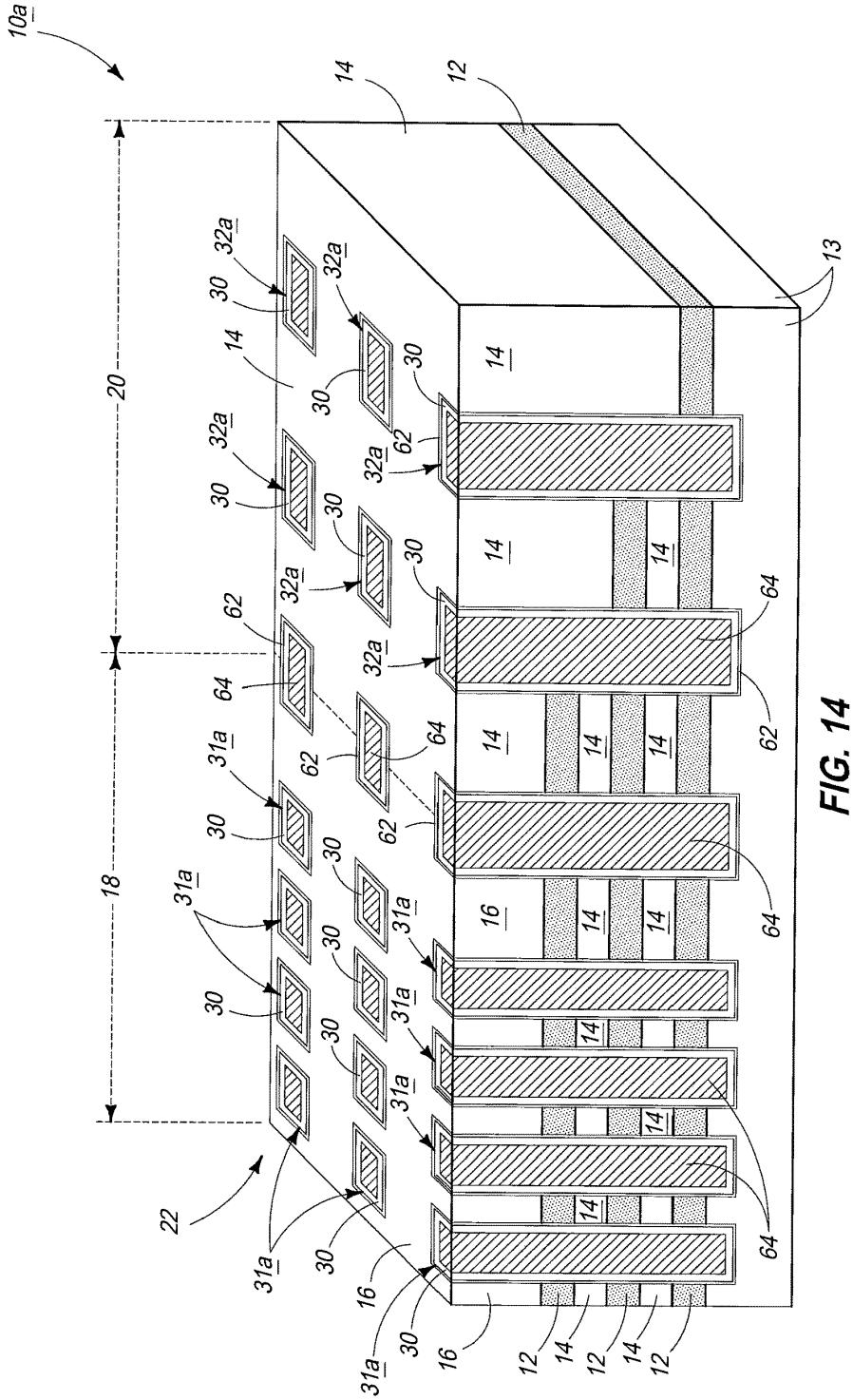


FIG. 14

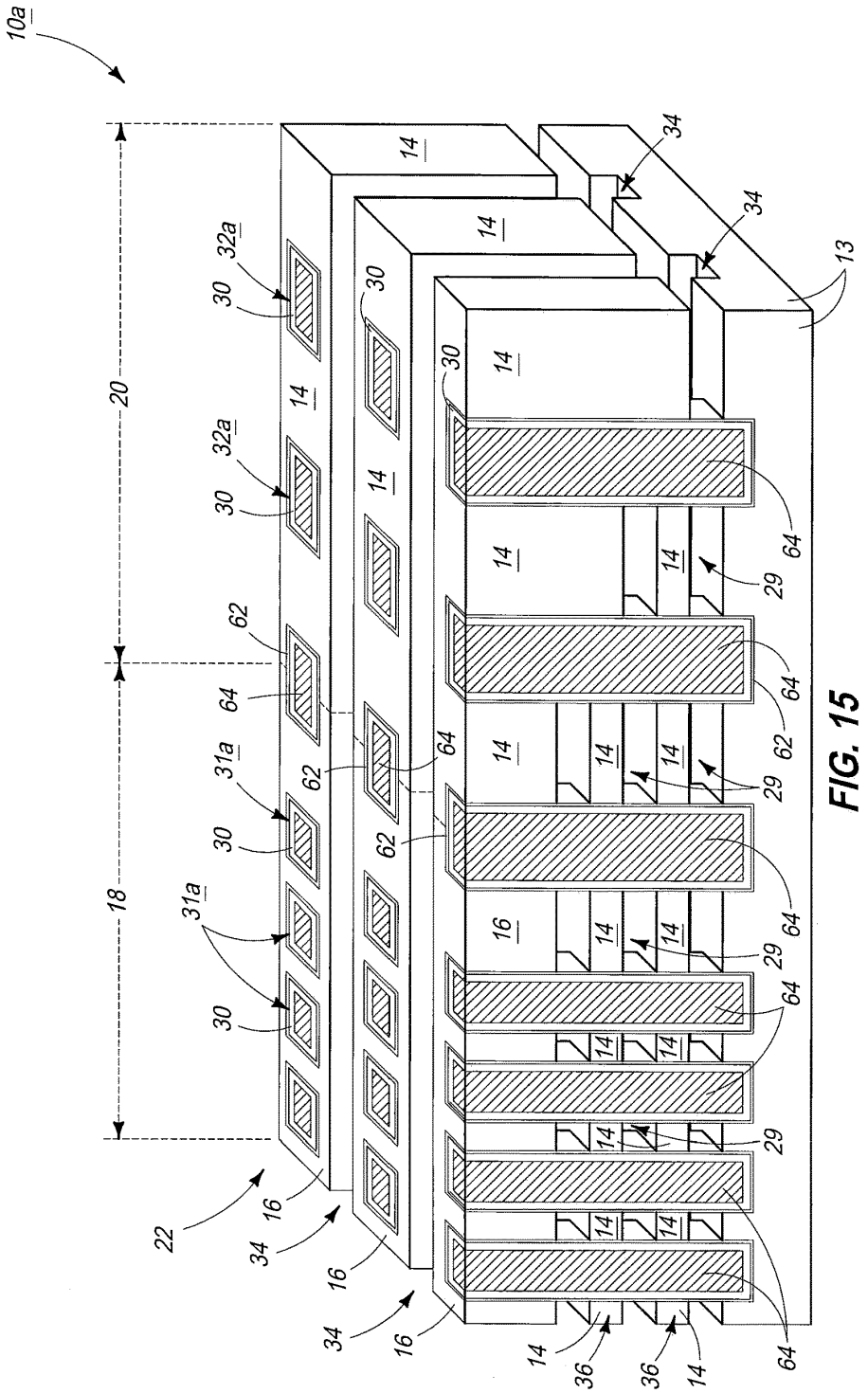


FIG. 15

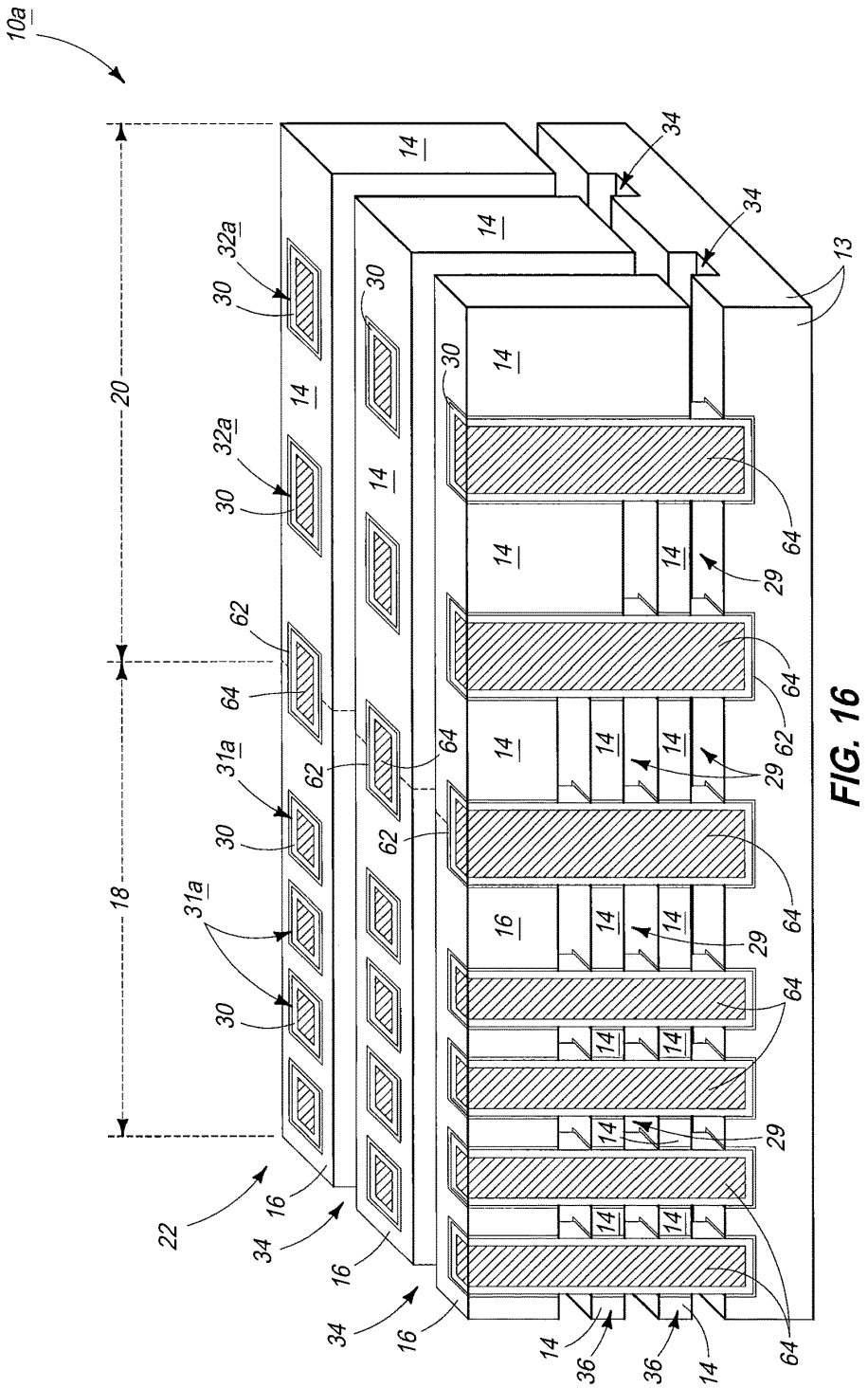


FIG. 16

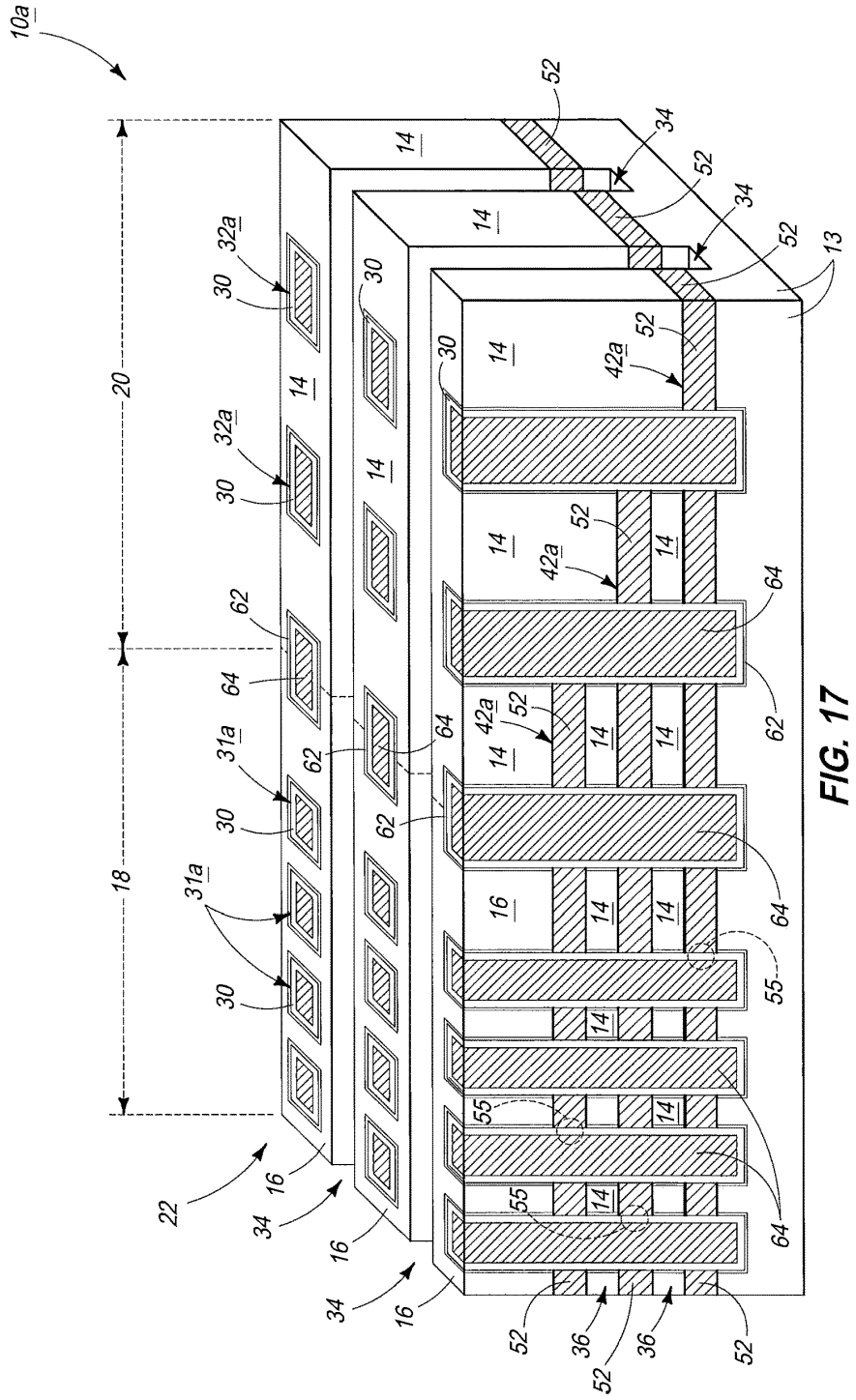


FIG. 17

STACK OF HORIZONTALLY EXTENDING AND VERTICALLY OVERLAPPING FEATURES, METHODS OF FORMING CIRCUITRY COMPONENTS, AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS

RELATED PATENT DATA

This patent resulted from a continuation application of U.S. patent application Ser. No.15/397,919, filed Jan. 4, 2017, entitled "Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells", naming Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat as inventors, which was a continuation application of U.S. patent application Ser. No. 15/095,208, filed Apr. 11, 2016, now US Pat. No. 9,564,471, entitled "Stack Of Horizontally Extending And Vertically Overlapping Features, Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells", naming Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat as inventors, which is a divisional application of U.S. patent application Ser. No. 14/602,559, filed Jan. 22, 2015, now U.S. Pat. No. 9,318,430, which is a divisional application of U.S. patent application Ser. No. 13/085,083, filed Apr. 12, 2011, now U.S. Pat. No. 8,945,996, entitled "Methods Of Forming Circuitry Components, And Methods Of Forming An Array Of Memory Cells", naming Sanh D. Tang, Roger W. Lindsay, and Krishna K. Parat as inventors, the disclosures of which are incorporated by reference.

TECHNICAL FIELD

Embodiments disclosed herein pertain to stacks of horizontally extending and vertically overlapping features, and to methods of forming circuitry components and to methods of forming an array of memory cells.

BACKGROUND

Integrated circuits are often formed on a semiconductor substrate such as a silicon wafer or other semiconductive material. In general, layers of various materials which are semiconductive, conductive, or electrically insulative are utilized to form the integrated circuits. By way of examples, the various materials may be doped, ion implanted, deposited, etched, grown, etc. using various processes. A continuing goal in semiconductive processing is to strive to reduce the size of individual circuitry components, thereby enabling smaller and denser integrated circuitry.

Memory is one type of integrated circuitry, and is used in computer systems for storing data. Such is usually fabricated in one or more arrays of individual memory cells. The memory cells might be volatile, semi-volatile, or nonvolatile. Nonvolatile memory cells can store data for extended periods of time, in many instances including when the computer is turned off. Volatile memory dissipates and therefore requires being refreshed/rewritten, in many instances multiple times per second. Regardless, the smallest unit in each array is termed as a memory cell and is configured to store data as one of at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store data as one of more than two selectable states.

Integrated circuitry fabrication continues to strive to produce smaller and denser integrated circuits. Accordingly, the fewer components an individual circuit device has, the smaller the construction of the finished device can be. A simple memory cell will be comprised of two conductive electrodes having a programmable material there-between. The programmable material is selected or designed to be configured in a selected one of at least two different physical memory states to enable storing of information by an individual memory cell. The reading of the cell comprises determination of which of the states the programmable material is in, and the writing of information to the cell comprises placing the programmable material in a target memory state. Some programmable materials retain a memory state in the absence of refresh, and thus may be incorporated into nonvolatile memory cells.

Some programmable materials may contain mobile charge carriers larger than electrons and holes, for example ions in some example applications. Regardless, the programmable materials may be converted from one memory state to another by moving the mobile charge carriers to alter a distribution of charge density within the programmable materials. Some example memory devices that utilize ions as mobile charge carriers are resistive RAM (RRAM) cells, which can include classes of memory cells containing multivalent oxides, and which can include memristors in some specific applications. Other example memory devices that utilize ions as charge carriers are programmable metallization cells (PMCs); which may be alternatively referred to as a conductive bridging RAM (CBRAM), nanobridge memory, or electrolyte memory.

The RRAM cells may contain programmable material sandwiched between a pair of electrodes. The programming of the RRAM cells may comprise transitioning the programmable material between first a memory state in which charge density is relatively uniformly dispersed throughout the material and a second memory state in which the charge density is concentrated in a specific region of the material (for instance, a region closer to one electrode than the other).

A PMC may similarly have programmable material sandwiched between a pair of current conductive electrodes. The PMC programmable material comprises ion conductive material, for example a suitable chalcogenide or any of various suitable oxides. A suitable voltage applied across the electrodes generates current conductive super-ionic clusters or filaments. Such result from ion transport through the ion conductive material which grows the clusters/filaments from one of the electrodes (the cathode), through the ion conductive material, and toward the other electrode (the anode). The clusters or filaments create current conductive paths between the electrodes. An opposite voltage applied across the electrodes essentially reverses the process and thus removes the current conductive paths. A PMC thus comprises a high resistance state (corresponding to the state lacking a current conductive filament or clusters between the electrodes) and a low resistance state (corresponding to the state having a current conductive filament or clusters between the electrodes), with such states being reversibly interchangeable with one another.

Another type of nonvolatile memory is known as flash memory, a type of EEPROM (electrically-erasable programmable read-only memory) that may be erased and reprogrammed in groups. A typical flash memory array includes a large number of nonvolatile memory cells usually grouped into blocks. Each of the cells within a block may be electrically programmed by charging its programmable gate material. The charge may be removed from the program-

mable gate material by a block erase operation. NAND is a basic architecture of flash memory. A NAND architecture comprises at least one select gate coupled in series to a serial combination of memory cells (with the serial combination being commonly referred to as a NAND string).

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic oblique view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

FIG. **2** is a view of the FIG. **1** substrate at a processing step subsequent to that shown by FIG. **1**.

FIG. **3** is a view of the FIG. **2** substrate at a processing step subsequent to that shown by FIG. **2**.

FIG. **4** is a view of the FIG. **3** substrate at a processing step subsequent to that shown by FIG. **3**.

FIG. **5** is a view of the FIG. **4** substrate at a processing step subsequent to that shown by FIG. **4**.

FIG. **6** is an end view of FIG. **5** relative to line **6**-**6** in FIG. **5**.

FIG. **7** is a view of the FIG. **5** substrate wherein certain material in FIG. **5** is not shown in FIG. **7** solely for clarity.

FIG. **8** is an end view of FIG. **7** relative to line **8**-**8** in FIG. **7**.

FIG. **9** is a view of the FIG. **7** substrate at a processing step subsequent to that shown by FIG. **7**.

FIG. **10** is a view of the FIG. **9** substrate wherein certain material in FIG. **9** is not shown in FIG. **10** solely for clarity.

FIG. **11** is a view of the FIG. **9** substrate at a processing step subsequent to that shown by FIG. **9**.

FIG. **11**A is an enlarged view of a portion of FIG. **11**.

FIG. **12** is view of the FIG. **11** substrate wherein certain material in FIG. **11** is not shown in FIG. **12** solely for clarity.

FIG. **13** is a view of the FIG. **12** substrate at a processing step subsequent to that shown by FIG. **12**.

FIG. **14** is a diagrammatic perspective view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

FIG. **15** is a view of the FIG. **14** substrate at a processing step subsequent to that shown by FIG. **14**.

FIG. **16** is a view of the FIG. **15** substrate at a processing step subsequent to that shown by FIG. **15**.

FIG. **17** is a view of the FIG. **16** substrate at a processing step subsequent to that shown by FIG. **16**.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Example embodiments in accordance with the invention of methods of forming circuitry components are initially described with reference to FIGS. **1**-**10**. In some embodiments, an array of memory cells may be fabricated, for example as described with reference to FIGS. **1**-**13** and with reference to FIGS. **14**-**17**. In one embodiment, such may comprise cross-point memory cells (e.g., as shown in FIG. **17**), and in one embodiment may comprise NAND circuitry (e.g., as shown in FIGS. **11**, **11**A, **12**, and **13**).

Referring to FIG. **1**, a substrate fragment **10** comprises a suitable base substrate **13** over which various materials have been provided. Base substrate **13** may be homogenous or non-homogenous, for example comprising multiple different composition materials and/or layers. As examples, such may comprise bulk monocrystalline silicon and/or a semiconductor-on-insulator substrate. As an additional example, such may comprise dielectric material having contacts (e.g., conductive vias) formed therein which extend vertically or otherwise into communicative contact (e.g., current conductive electrical connection) with device components, regions, or material that is elevationally inward of the dielectric material. In this document, vertical is a direction generally orthogonal to a primary surface relative to which the substrate is processed during fabrication and which may be considered to define a generally horizontal direction. Further, "vertical" and "horizontal" as used herein are generally perpendicular directions relative one another independent of orientation of the substrate in three-dimensional space. Further in this document, "elevational" and "elevationally" are with reference to the vertical direction from a base substrate upon which the circuitry is fabricated.

The base substrate may or may not be a semiconductor substrate. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

In one embodiment, substrate **10** comprises a stack of alternating sacrificial material **12** and dielectric material **14** formed over base substrate **13**. Each material **12** and **14** may be homogenous or non-homogenous. In one embodiment, the respective sacrificial materials **12** are of the same composition relative one another. In one embodiment, the respective dielectric materials **14** are of the same composition relative one another. Regardless, sacrificial material **12** may be selectively etchable, in one embodiment highly selectively etchable, relative to dielectric material **14**. In the context of this document, a "selective" etch requires removal of the stated one material relative to another at a rate of at least 1.5:1, and a highly selective etch at a rate of at least about 10:1. Sacrificial material **12** may be any one or more of conductive (e.g., current conductive), dielectric, or semiconductive. By way of an example only, dielectric material **14** may comprise silicon dioxide (whether doped or undoped), and an example sacrificial material is a conductive or insulative nitride, for example titanium nitride or silicon nitride, respectively. A dielectric material **16** and a hardmask **18** have been provided outwardly of alternating materials **12**, **14**. Each material **16** and **18** may be homogenous or non-homogenous. Dielectric material **16** may be of the same composition as dielectric material **14**, and hardmask material **18** may be of the same composition as sacrificial material **12**. FIG. **1** depicts vertical tiers of three sacrificial materials **12** with two alternating dielectric materials **14**. Additional alternating pairs of sacrificial and dielectric materials may be provided elevationally inward of innermost sacrificial material **12** or elevationally outward of outermost sacrificial material **12**.

Stack of alternating materials **12**, **14** may be considered as comprising a primary portion **18** and an end portion **20**. The end portion in the depicted embodiment has been patterned to form a stair step-like construction. Such may be formed to provide horizontal area for later forming contacts to components, regions, or material in end portion **20** as will be apparent in the continuing discussion. In one embodiment and as shown, end portion **20** comprises individual stairs **21** which at least include sacrificial material **12**.

In one embodiment, materials **12** and **14** may be features (e.g., plates), such as plates or features that are plate-like, whether continuously and/or discontinuously formed. In one

embodiment, a method of forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping plates at least some of which increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Either of collective materials **12** or **14** may be considered in such example embodiment as comprising such plates, or materials **12** and **14** in combination in the depicted embodiment may be considered as such plates. In one embodiment, the horizontally extending and vertically overlapping plates are dielectric, for example plates **14** regardless of the composition of sacrificial material **12**. In one embodiment, all of the plates increase in horizontal extent in the vertical inward direction in the end portion of the stack. For example in the embodiment of FIG. **1**, either of collective plates **12** or collective plates **14** may be considered as plates all of which increase in horizontal extent progressing vertically inward in the end portion of the stack. Alternately, a composite of each immediately adjacent plate pairs **12**, **14** may be considered as respective plates which increase in horizontal extent in the vertical inward direction in end portion **20** of the stack.

In one embodiment, primary portion **18** and end portion **20** comprise a portion of an array area **22** within which a plurality of memory cells will be fabricated. Logic circuitry (not shown) may be fabricated outside of the array area. Control and/or other peripheral circuitry (not shown) for operating the memory array may or may not fully or partially be within the array area, with an example array area as a minimum encompassing all of the memory cells of the given array/sub-array. Further, multiple sub-arrays might also be fabricated and operated independently, in tandem, or otherwise relative one another. As used in this document, a "sub-array" may also be considered as an array.

Referring to FIG. **2**, dielectric material has been formed over substrate **10** and planarized at least to the outermost surface of hardmask **18**. The dielectric material may be homogenous or non-homogenous and, in one embodiment, may be of the same composition as that of material **14** and is so shown and designated in the figures.

Referring to FIG. **3**, first openings **25** have been formed into primary portion **18** of the stack and second openings **27** have been formed into end portion **20** of the stack. Any openings which overlap the primary and end portions may be such first or second openings (i.e., as primary portion openings or end portion openings), with example such openings being shown in FIG. **3** and designated as second openings **27**. Openings **25**, **27** may be formed through each plate **12**, **14**. An example technique for forming openings **25**, **27** is by photolithographic patterning followed by subtractive anisotropic etching. First openings **25** need not be of the same shape and/or density relative one another. Second openings **27** need not be of the same shape and/or density relative one another, or relative to any one or more of first openings **25**. As examples, openings **25** and **27** may be formed to have the same horizontal and vertical cross sections (not shown). Alternately, openings **25** and **27** may be formed to have at least one of different horizontal cross sections (as shown) or different vertical cross sections (as shown). Further and regardless, openings **25** and **27** may be formed at the same time or at different times, and/or may use the same masking step or different masking steps where, for example, photolithographic or other masking is used. In one embodiment and as shown, at least some of openings **27** in end portion **20** are formed to horizontally overlap ends of individual plates **12** and/or **14**.

At least one of conductive material, semiconductive material, and programmable material is/are deposited into the openings. In one embodiment where conductive material is deposited into the openings, such may comprise current conductive material. In the context of this document, current conductive material can include a composition where electric current flow may inherently occur therein predominantly by movement of subatomic positive and/or negative charges when such are generated as opposed to predominantly by movement of ions. Example current conductive materials are elemental metals, alloys of elemental metals, current conductive metal compounds, and conductively doped semiconductive material, including any combinations thereof.

In one embodiment, the depositing of the conductive material, semiconductive material and/or programmable material occurs simultaneously into all of the openings in the primary portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in the end portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in both of the primary and end portions. Operative structures (e.g., circuit components, such as local vertical extensions) are formed therewith within the openings in the primary portion, and dummy structures (e.g. dummy vertical extensions) are formed therewith within the openings in the end portion. In the context of this document, a "dummy" structure is a structure which is used to mimic a physical property of another structure (e.g., load carrying ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive). Openings in which dummy structures are formed may be considered as "dummy openings".

For example referring to FIG. **4**, a material **30** has been deposited within openings **25**, **27**, and then planarized back through hardmask material **18** (not shown). An example thickness for material **30** is from about 100 to about 150 Angstroms. Material **30** may be homogenous or non-homogenous, and may comprise one or more of conductive material (e.g., current conductive material), semiconductive material, and programmable material. In one embodiment, material **30** comprises semiconductive material. Further in such embodiment, the semiconductive material may comprise interconnected channels of a plurality of vertically oriented transistors, and in one embodiment comprises interconnected channels of vertically oriented charge storage transistors as will be apparent from the continuing discussion. Regardless, in one embodiment, material **30** may form operative structures **31** (e.g., operative circuit components **31**) within primary portion openings **25** and form dummy structures **32** (e.g., dummy circuit components) within end portion openings **27**. In one embodiment and as shown, such operative structures **31** and dummy structures **32** are in the form of hollow cylinders. Alternately by way of example, such may be in the form of laterally solid pillars (not shown in FIG. **4**). Regardless, the above processing describes but examples of forming operative structures **31** vertically through plates **12** and/or **14** in primary portion **18** and forming dummy structures **32** vertically through plates **12** and/or **14** in end portion **20**. In one embodiment, the operative and dummy structures may comprise the same material (as shown). In one embodiment, the operative and dummy structures may comprise a plurality of the same materials (not shown in FIG. **4**), and in one such embodiment be arranged in the same lateral order relative one another in the operative and dummy structures. In one

embodiment, the operative and dummy structures may consist essentially of the same material.

Referring to FIGS. **5-8**, horizontally elongated openings **34** (e.g., trenches) have been formed through plates **12** and/or **14**, and laterally between material **30**, to form horizontally elongated and vertically overlapping lines **36** from material of the plates. Lines **36** individually extend from primary portion **18** into end portion **20** and individually laterally about sides of vertically extending portions of both operative structures **31** and dummy structures **32**. FIGS. **7** and **8** are views of FIGS. **5** and **6**, respectively, wherein dielectric material **14** added in FIG. **2** is removed solely for clarity in such drawings. Where either of operative structures **31** or dummy structures **32** are upwardly open (e.g., as shown), such may be partially or wholly filled (not shown) with dielectric and/or other material prior to the forming of horizontally elongated openings **34**.

Referring to FIGS. **9** and **10**, at least some of sacrificial material **12** that is elevationally between lines **36** within primary portion **18** and end portion **20** has been removed from being laterally between horizontally elongated openings **34**. Such thereby, in one embodiment, forms void spaces **29** elevationally between vertically spaced horizontal dielectric lines **36**. An example technique includes etching, for example isotropic dry and/or wet etching. Etching may be conducted selectively (ideally, highly selectively) relative to lines **36**, operative structures **31**, and dummy structures **32**. FIG. **10** is a view of the FIG. **9** substrate wherein dielectric material **14** added in FIG. **2** is removed solely for clarity in such drawing.

The above processing discloses but example embodiments of forming circuitry components in accordance with some aspects of the invention. In one embodiment, a method of forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping features. By way of example only, such features may comprise plates, with the example depicted structure of plates **14** comprising but one example of such plates. Regardless, in such embodiment, the stack comprises a primary portion and an end portion wherein at least some of the features increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Operative structures **31** (e.g., circuit components) are formed vertically through the features in the primary portion and dummy structures **32** (e.g., dummy circuit components) are formed vertically through the features in the end portion. The processing depicted through FIG. **4**, or through FIGS. **5-8**, are examples. The operative and dummy structures may comprise the same material, and in one embodiment may consist essentially of the same material. The dummy structures may support material of the features from vertical movement in the end portion while at least some of sacrificial material that is elevationally between the material of the features in the primary and end portions is removed. The processing depicted in going from that of FIGS. **5-8** to that of FIGS. **9** and **10** is but one such example processing. With respect to a prior art problem, dummy structures heretofore have not been provided in a stair-like end portion of an array. Accordingly, the floors/ceilings that are vertically between the respective void spaces **29** in FIGS. **9** and **10** may be sagged, bent, or broken during processing due to lack of support. In accordance with one embodiment of the invention, dummy structures in the end portion support the features (e.g., the respective ceilings and floors, or plates) from vertical movement, for example by laterally engaging side portions of such floors/ceilings that were created where such dummy structures extend there-through. Regardless, other attributes as described may be employed.

Additional processing may occur in fabricating integrated circuitry, for example in fabricating an array of memory cells as next described with reference to FIGS. **11-13**. Referring to FIGS. **11** and **11**A, material **40** has been isotropically deposited within horizontally elongated openings **34**, former void spaces **29** (not shown in FIGS. **11**, **11**A), and any remaining volume of openings **25**, **27**. Material **40** has subsequently been removed from horizontally elongated openings **34** to form vertically spaced horizontal conductive lines **42** within the void spaces elevationally between horizontal lines **36** of dielectric material **14**. In one embodiment, conductive lines **42** collectively cross a row of the operative and dummy structures at different respective elevations. In one embodiment, individual structures **31**, **32** cross different conductive lines at different respective elevations. In the depicted example, conductive lines **42** extend longitudinally straight linear. Alternately by way of example, some or all of lines **42** may not be straight linear, for example being longitudinally curvilinear (not shown). Material **40** may also be removed from the remaining internal volume of openings **25**, **27** as shown. FIG. **12** depicts the circuitry of FIG. **11** wherein the dielectric material that is shown as being deposited in FIG. **2** is removed solely for clarity.

FIGS. **11**, **11**A, and **12** depict but one example embodiment comprising NAND circuitry wherein operative structures **31** comprise interconnected channel regions of a NAND string. In such example embodiment, material **40** comprises a composite of a suitable tunnel dielectric **49** (FIG. **11**A), floating gate/charge trapping material **48**, dielectric **50**, and conductive control gate material **52**. Thereby, conductive material **52** provides but an example conductive portion of conductive lines **42** that is within the void spaces between the horizontal lines of dielectric material, and which collectively cross a row of the operative and dummy structures at different respective elevations. Individual ones of the memory cells of the example circuitry of FIGS. **11** and **11**A comprise an intersection of an individual horizontal conductive line and an individual operative structure (e.g., in the form of a string of channels of NAND), and some of which are indicated with reference numeral **55**.

In one embodiment, a respective contact may be formed to a stair extension of individual ones of horizontal conductive lines **42** in end portion **20** for making communicative connection to circuitry. One such example is diagrammatically shown in FIG. **13**. The dielectric material **14** of FIG. **2** is again showed removed solely for clarity in depicting certain components. Specifically, FIG. **13** shows example individual contacts **60** (e.g, current conductive contacts) which may be formed through the dielectric material **14** (not shown) of FIG. **2** for making communicative connection to circuitry, such as that elevationally outward of that depicted by FIG. **13** with respect to each conductive line **42**.

Circuitry components other than or in addition to components of memory cells may be fabricated in accordance with embodiments of the invention.

An example embodiment of a method of forming an array of cross-point memory cells is next described with reference to FIGS. **14-17**. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a" or with different numerals. FIG. **14** depicts an alternate embodiment substrate fragment **10***a* to that depicted by FIG. **4**. In FIG. **14**, openings **25**, **27** have been lined with a first

material **62**. In one embodiment, such material is dielectric (i.e., a 15 to 30 Angstroms thick layer of undoped silicon dioxide). Thereafter, a programmable material **30** was deposited to line over first material **62** within openings **25**, **27**. Then, remaining volume of openings **25**, **27** has been filled with conductive material **64**, and materials **62**, **30**, and **64** planarized back to materials **14** and **16**. Horizontally elongated openings (not shown in FIG. **14**) may then be formed analogous to the processing depicted by FIGS. **5-8**.

Programmable material **30** may be solid, gel, amorphous, crystalline, or any other suitable phase. Any existing or yet-to-be developed programmable material may be used, with only some examples being provided below.

One example programmable material is ion conductive material. Example suitable such materials comprise chalcogenide-type (for instance, materials comprising one or more of germanium, selenium, antimony, tellurium, sulfur, copper, etc.; with example chalcogenide-type materials being $Ge_2Sb_2Te_5$, GeS_2, $GeSe_2$, CuS_2, and CuTe) and/or oxides such as zirconium oxide, hafnium oxide, tungsten oxide, copper oxide, niobium oxide, iron oxide, silicon oxide (specifically, silicon dioxide), gadolinium oxide, etc. capable of inherently (or with additive) supporting electrolyte behavior. Such may have silver, copper, cobalt, and/or nickel ions, and/or other suitable ions, diffused therein for ionic conduction, analogously to structures disclosed in U.S. Pat. No. 7,405,967 and U.S. Patent Publication Number 2010/0193758.

Additional example programmable materials include multi-resistive state metal oxide-comprising material. Such may comprise, for example, at least two different layers or regions generally regarded as or understood to be active or passive regions, although not necessarily. Alternately, such may only comprise active material. Example active cell region compositions which comprise metal oxide and can be configured in multi-resistive states include one or a combination of $Sr_xRu_yO_z$, Ru_xO_y, and $In_xSn_yO_z$. Other examples include MgO, Ta_2O_5, $SrTiO_3$, $SrZrO_3$, $BaTiO_3$, $Ba_{(1-x)}Sr_xTiO_3$, ZrO_x (perhaps doped with La), and $CaMnO_3$ (doped with one or more of Pr, La, Sr, or Sm). Example passive cell region compositions include one or a combination of Al_2O_3, TiO_2, and HfO_2. Regardless, a programmable material composite might comprise additional metal oxide or other materials not comprising metal oxide. Example materials and constructions for a multi-resistive state region comprising one or more layers including a programmable metal oxide-comprising material are described and disclosed in U.S. Pat. Nos. 6,753,561; 7,149,108; 7,067,862; and 7,187,201, as well as in U.S. Patent Application Publication Nos. 2006/0171200 and 2007/0173019. Further as is conventional, multi-resistive state metal oxide-comprising materials encompass filament-type metal oxides, ferroelectric metal oxides and others, and whether existing or yet-to-be developed, as long as resistance of the metal oxide-comprising material can be selectively changed.

The programmable material may comprise memristive material. As an example, such material may be statically programmable semiconductive material which comprises mobile dopants that are received within a dielectric such that the material is statically programmable between at least two different resistance states. At least one of the states includes localization or gathering of the mobile dopants such that a dielectric region is formed and thereby provides a higher resistance state. Further, more than two programmable resistance states may be used. In the context of this document, a "mobile dopant" is a component (other than a free electron) of the semiconductive material that is movable to different locations within said dielectric during normal device operation of repeatedly programming the device between at least two different static states by application of voltage differential to the pair of electrodes. Examples include atom vacancies in an otherwise stoichiometric material, and atom interstitials. Specific example mobile dopants include oxygen atom vacancies in amorphous or crystalline oxides or other oxygen-containing material, nitrogen atom vacancies in amorphous or crystalline nitrides or other nitrogen-containing material, fluorine atom vacancies in amorphous or crystalline fluorides or other fluorine-containing material, and interstitial metal atoms in amorphous or crystalline oxides. More than one type of mobile dopant may be used. Example dielectrics in which the mobile dopants are received include suitable oxides, nitrides, and/or fluorides that are capable of localized electrical conductivity based upon sufficiently high quantity and concentration of the mobile dopants. The dielectric within which the mobile dopants are received may or may not be homogenous independent of consideration of the mobile dopants. Specific example dielectrics include TiO_2, AlN, and/or MgF_2. Example programmable materials that comprise oxygen vacancies as mobile dopants may comprise a combination of TiO_2 and TiO_{2-x} in at least one programmed resistance state depending on location of the oxygen vacancies and the quantity of the oxygen vacancies in the locations where such are received. An example programmable material that comprises nitrogen vacancies as mobile dopants is a combination of AlN and AlN_{1-x} in at least one programmed state depending on location of the nitrogen vacancies and the quantity of the nitrogen vacancies in the locations where such are received. An example programmable material that comprises fluorine vacancies as mobile dopants may is a combination of MgF_2 and MgF_{2-x} in at least one programmed resistance state depending on location of the fluorine vacancies and the quantity of the fluorine vacancies in the locations where such are received. As another example, the mobile dopants may comprise aluminum atom interstitials in a nitrogen-containing material.

Still other example programmable materials include polymer materials such as Bengala Rose, AlQ_3Ag, Cu-TCNQ, DDQ, TAPA, and fluorescine-based polymers.

Referring to FIG. **15**, such corresponds in processing sequence to that of FIG. **9** of the above-described embodiments. Sacrificial material **12** (not shown) has been at least partially removed (e.g., by etching) between dielectric lines **36** in primary portion **18** and end portion **20** laterally between horizontally elongated openings **34**. Material **12** may be etched selectively (ideally, highly selectively) relative to dielectric lines **36**, first material lining **62**, and conductive material **64** in openings **25**, **27**. FIGS. **14** and **15** depict an example embodiment wherein the operative and dummy structures comprise a plurality of the same materials, and in such embodiment arranged in the same lateral order relative one another in the operative and dummy structures. Regardless, in one embodiment, first material lining **62** may serve as a protecting barrier from adverse exposure of programmable material **30** to the etching chemistry which etches the sacrificial material.

Referring to FIG. **16**, at least a portion of first material **62** has been removed elevationally between dielectric lines **36** to expose laterally outer sidewalls of programmable material **30** that is elevationally between dielectric lines **36**. An example technique for doing so where material **62** comprises silicon dioxide includes etching with a dilute HF solution.

Referring to FIG. **17**, at least a portion of sacrificial material **12** (not shown) of FIG. **14** has been replaced with

conductor material **52** (e.g., current conductive material) that is in electrical connection with the laterally outer sidewalls of programmable material **30** and to comprise vertically spaced horizontal conductive lines **42***a*. Materials **64** and **52** may be of the same composition or of different compositions. Further and regardless, conductive material **64** within remaining volumes of openings **25**, **27** alternately may be provided subsequent to the etching depicted by FIG. **15**. Regardless, FIG. **17** also depicts conductor material **52** as having been at least partially removed from horizontally elongated openings **34** to form such vertically spaced horizontal conductive lines **42***a*.

Individual ones of the cross-point memory cells comprise crossing ones of the horizontal conductive lines in the primary portion and conductive material in the openings in the primary portion having the programmable material there-between, with some of such example memory cells being indicated with reference numeral **55** in the FIG. **17** example embodiment.

An embodiment of the invention includes a stack of horizontally extending and vertically overlapping features. The stack comprises a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures extend vertically through the features in the primary portion. Dummy structures extend vertically through the features in the end portion. In one embodiment, the features may be horizontally extending lines, for example formed of any one or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s). In one embodiment, the features comprise a combination of horizontally extending conductive and dielectric lines (e.g., overlapping and alternating such lines). In one embodiment, contacts may be in the end portion, for example extending vertically to the lines. Any other attribute as described above may be used, for example as shown and described with respect to FIGS. **1-13** and with respect to FIGS. **14-17**.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

The invention claimed is:

1. Integrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines, the integrated circuitry comprising:

a primary portion and an end portion, at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the gate lines in the primary portion, the operative structures comprising semiconductive material, the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines; and

dummy structures extending vertically through the gate lines in the end portion.

2. The stack of claim **1** further comprising contacts in the end portion that individual extend to the individual gate lines.

3. The integrated circuitry of claim **1** wherein the vertically oriented transistors are charge storage transistors of individual memory cells.

4. The integrated circuitry of claim **3** wherein the memory cells comprise a portion of NAND architecture.

5. The integrated circuitry of claim **1** wherein the operative and dummy structures comprise the same material.

6. The integrated circuitry of claim **5** wherein the operative and dummy structures comprise a plurality of the same materials.

7. The integrated circuitry of claim **6** wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

8. The integrated circuitry of claim **5** wherein the operative and dummy structures consist essentially of the same material.

9. The integrated circuitry of claim **1** wherein the dummy structures comprise semiconductor material.

10. The integrated circuitry of claim **1** wherein the dummy structures comprise the semiconductive material.

11. A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion; and

dummy structures extending vertically through the features in the end portion, the dummy structures individually comprising a cylinder of semiconductive material.

12. The stack of claim **11** comprising solid material filling radially internal regions of individual of the cylinders of semiconductive material.

13. The stack of claim **11** wherein individual of the cylinders of semiconductive material define a radially-outermost horizontal periphery of individual of the dummy structures.

14. The stack of claim **11** wherein the operative structures individually comprise a cylinder of semiconductor material.

15. The stack of claim **11** further comprising vertical contacts in the end portion connecting with conductive material of individual of the features.

16. A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string; and

dummy structures extending vertically through the features in the end portion, some of the dummy structures horizontally overlapping the primary portion and the end portion.

17. The stack of claim **16** wherein the dummy structures comprise a cylinder of semiconductive material.

18. A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion; and

vertical contacts in the end portion connecting with individual of the control gate lines, the contacts and dummy structures having different horizontal cross-sections relative one another.

19. The stack of claim **18** wherein the different horizontal cross-sections are of the same shape and of different sizes relative one another.

20. The stack of claim **18** wherein the different horizontal cross-sections have different values of total horizontal area relative one another.

21. A stack of horizontally extending and vertically overlapping features, the stack comprising:

a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

operative structures extending vertically through the features in the primary portion, the operative structures comprising portions of memory cells, the memory cells comprising a portion of NAND architecture, the operative structures comprising interconnected channel regions of a NAND string, the at least some of the features comprising control gate lines;

dummy structures extending vertically through the control gate lines in the end portion, some of the dummy structures being longitudinally spaced alone a horizontal line; and

vertical contacts in the end portion connecting with individual of the control gate lines, at least one of the vertical contacts being longitudinally between two immediately-longitudinally adjacent of the dummy structures in the horizontal line.

22. The stack of claim **21** wherein the horizontal line is linearly straight.

* * * * *

Exhibit 2

REDACTED

EXHIBIT 2 (02/16/2024)

Micron's Exemplary Infringement Claim Chart for U.S. Patent No. 10,475,737

The following chart provides non-limiting examples, without the benefit of claim construction or discovery, of how YMTC's Accused Products (as that term is defined in the Complaint) meet every limitation, literally or under the doctrine of equivalents, of at least claim 1 of U.S. Patent No. 10,475,737. The referenced images are images from a 232L YMTC 1Tb TLC part. Micron reserves the right to amend, correct, supplement, or otherwise change its explanation of how YMTC's Accused Products meet the following claim limitations, including as the claims are construed, as discovery progresses, or as Micron's investigation continues. Micron takes no position on claim interpretation or scope at this time.

Claim Language	YMTC's Accused Products
1. Integrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines, the integrated circuitry comprising:[1]	YMTC's Accused Products include "[i]ntegrated circuitry comprising a stack of horizontally extending and vertically overlapping conductive transistor gate lines" that includes the following claim elements. Specifically, YMTC's Accused Products include a stack (shown below) of horizontally extending alternating conductive gate lines (e.g., word lines) and dielectric layers, which vertically overlap one another:

[1] By providing this disclosure, Micron does not concede that the preamble is a claim limitation.

EXHIBIT 2 (02/16/2024)

	REDACTED YMTC refers to such layers as forming a "stack." *See, e.g.*, U.S. Pat. No. 10,861,872 at Abstract ("stack").
a primary portion and an end portion, at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;	As shown below, YMTC's Accused Products include "a primary portion and an end portion, at least some of the gate lines extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion." Specifically, as shown below, at least some of the gates lines (e.g., word lines) extend farther in the horizontal direction in the end portion moving deeper into the stack (e.g., towards the substrate):

EXHIBIT 2 (02/16/2024)

	REDACTED YMTC describes that the word lines extend further in the end portion, which it refers to as the "staircase region," then the primary portion, which it refers to as the "core array region." *See, e.g.*, U.S. Pat. No. 10,861,872 at 6:14-25, Figure 1D.
operative structures extending vertically through the gate lines in the primary portion, the operative structures comprising semiconductive material, the	YMTC's Accused Products include "operative structures extending vertically through the gate lines in the primary portion, the operative structures comprising semiconductive material, the semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines." Specifically, the primary portion includes memory strings that are vertically operative transistor structures including memory cells, and these structures extend through the word lines:

EXHIBIT 2 (02/16/2024)

semiconductive material of the operative structures comprising interconnected channels of a plurality of vertically oriented transistors that individually comprise individual of the gate lines; and	REDACTED YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. *See, e.g.*, U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A. The operative structures are depicted in greater detail below and comprise the transistors formed by the four central vertical operative structures of the image:

EXHIBIT 2 (02/16/2024)

	REDACTED
dummy structures extending vertically through the gate lines in the end portion.	YMTC's Accused Products include "dummy structures extending vertically through the gate lines in the end portion." Specifically, as shown below, the end portion includes dummy structures through the gate lines:

EXHIBIT 2 (02/16/2024)

	REDACTED YMTC describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures," which comprise the same semiconductor material as the operative structures. *See, e.g.*, U.S. Pat. No. 10,861,872 at 6:31-50.

Exhibit 3

US008945996B2

(12) **United States Patent**
Tang et al.

(10) **Patent No.: US 8,945,996 B2**
(45) **Date of Patent: Feb. 3, 2015**

(54) **METHODS OF FORMING CIRCUITRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 967 days.

(21) Appl. No.: **13/085,083**

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H01L 21/82 (2006.01)
H01L 27/10 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 27/101*** (2013.01)
USPC **438/128**; 438/261; 438/216; 438/591; 438/639

(58) **Field of Classification Search**
CPC H01L 27/11582; H01L 27/11556; H01L 27/11551; H01L 27/1157; H01L 27/11578; H01L 21/8221
USPC 438/216, 261, 591, 270–273, 639, 438/E21.645, 128
See application file for complete search history.

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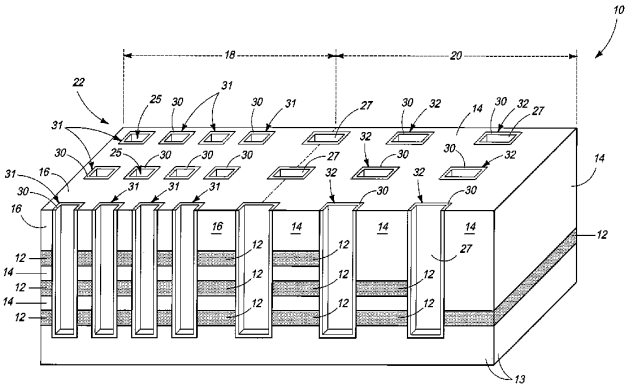
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(57) **ABSTRACT**

A method of forming circuitry components includes forming a stack of horizontally extending and vertically overlapping features. The stack has a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures are formed vertically through the features in the primary portion and dummy structures are formed vertically through the features in the end portion. Horizontally elongated openings are formed through the features to form horizontally elongated and vertically overlapping lines from material of the features. The lines individually extend from the primary portion into the end portion, and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures. Sacrificial material that is elevationally between the lines is at least partially removed in the primary and end portions laterally between the horizontally elongated openings. Other aspects and implementations are disclosed.

32 Claims, 18 Drawing Sheets



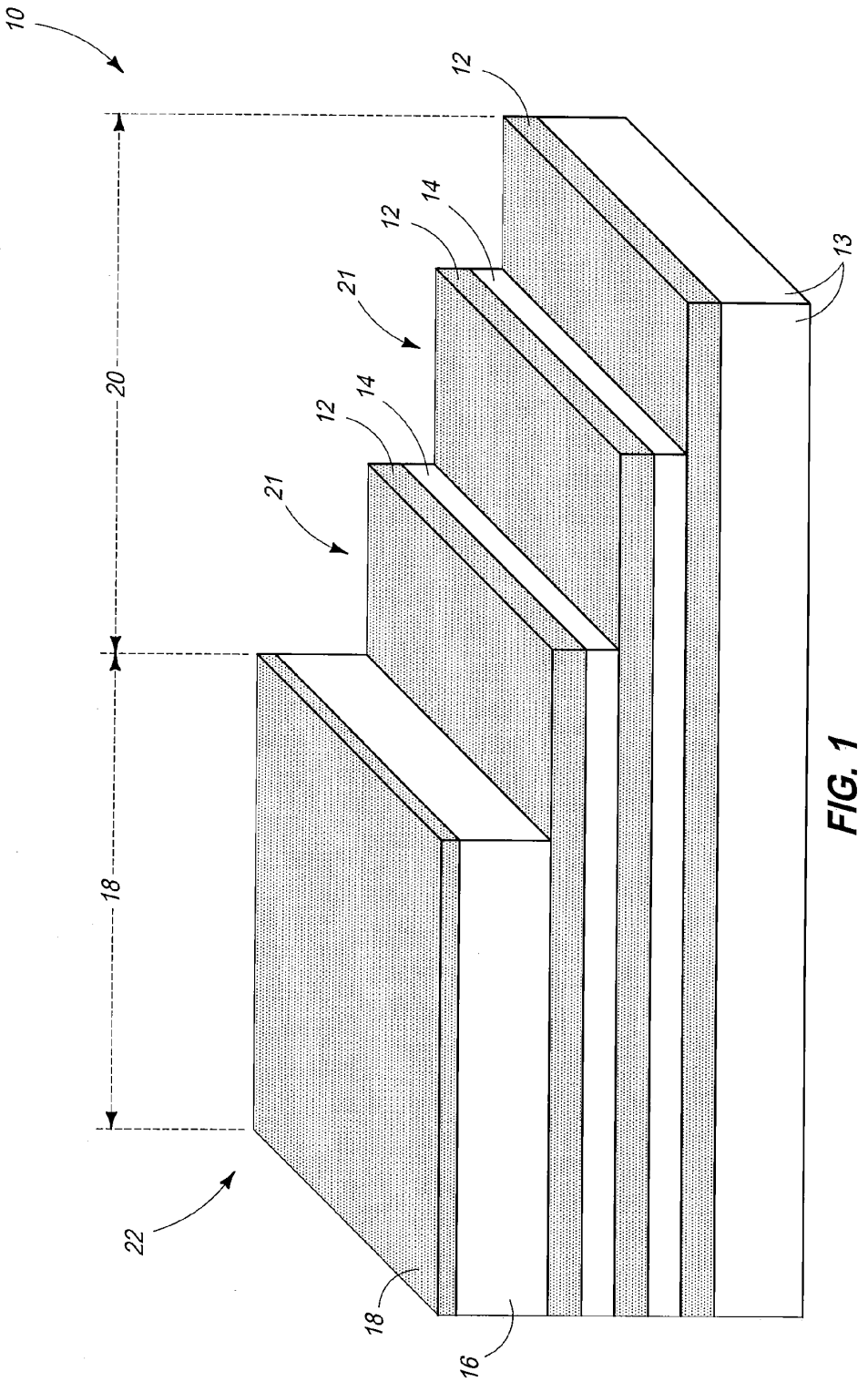


FIG. 1

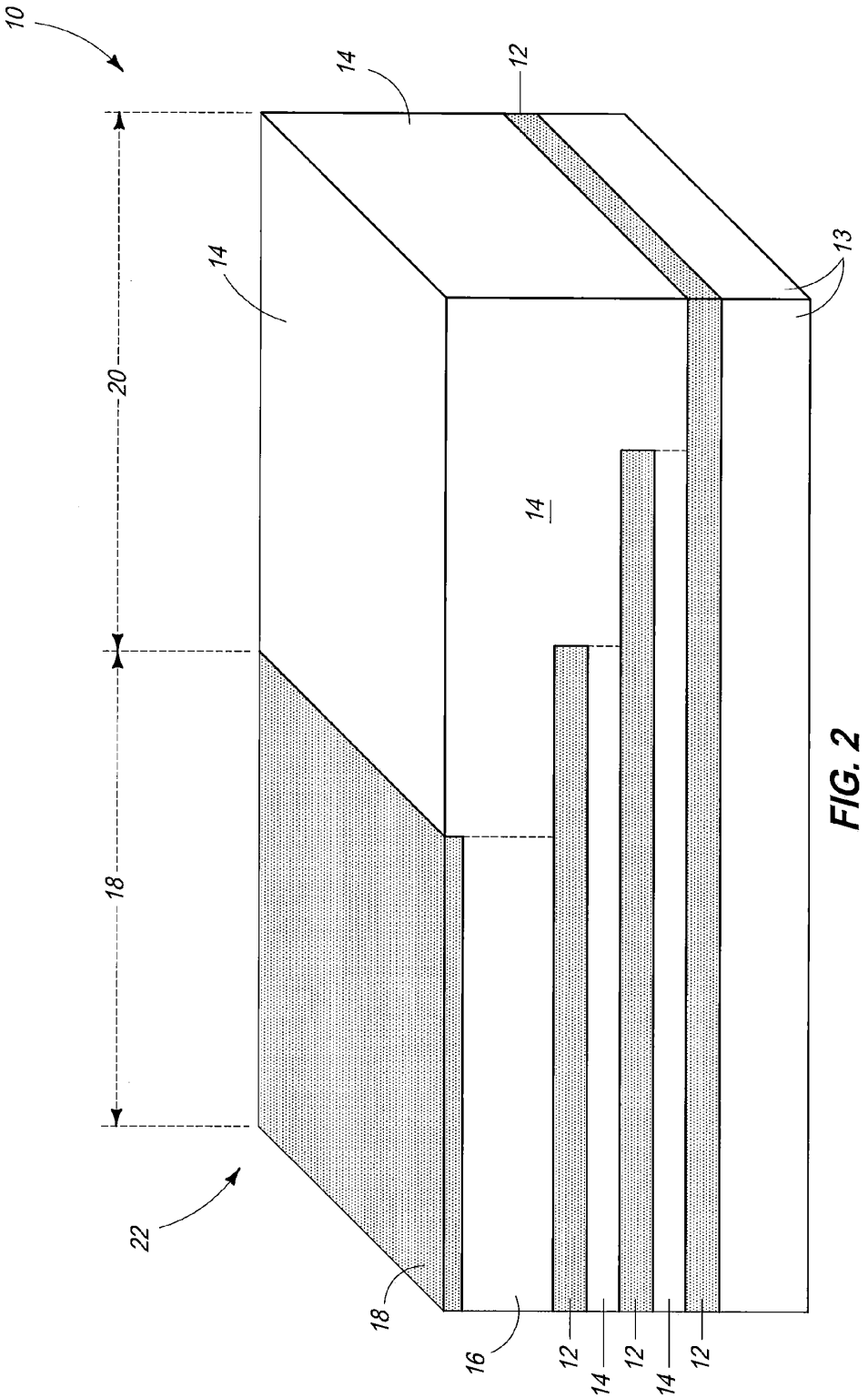


FIG. 2

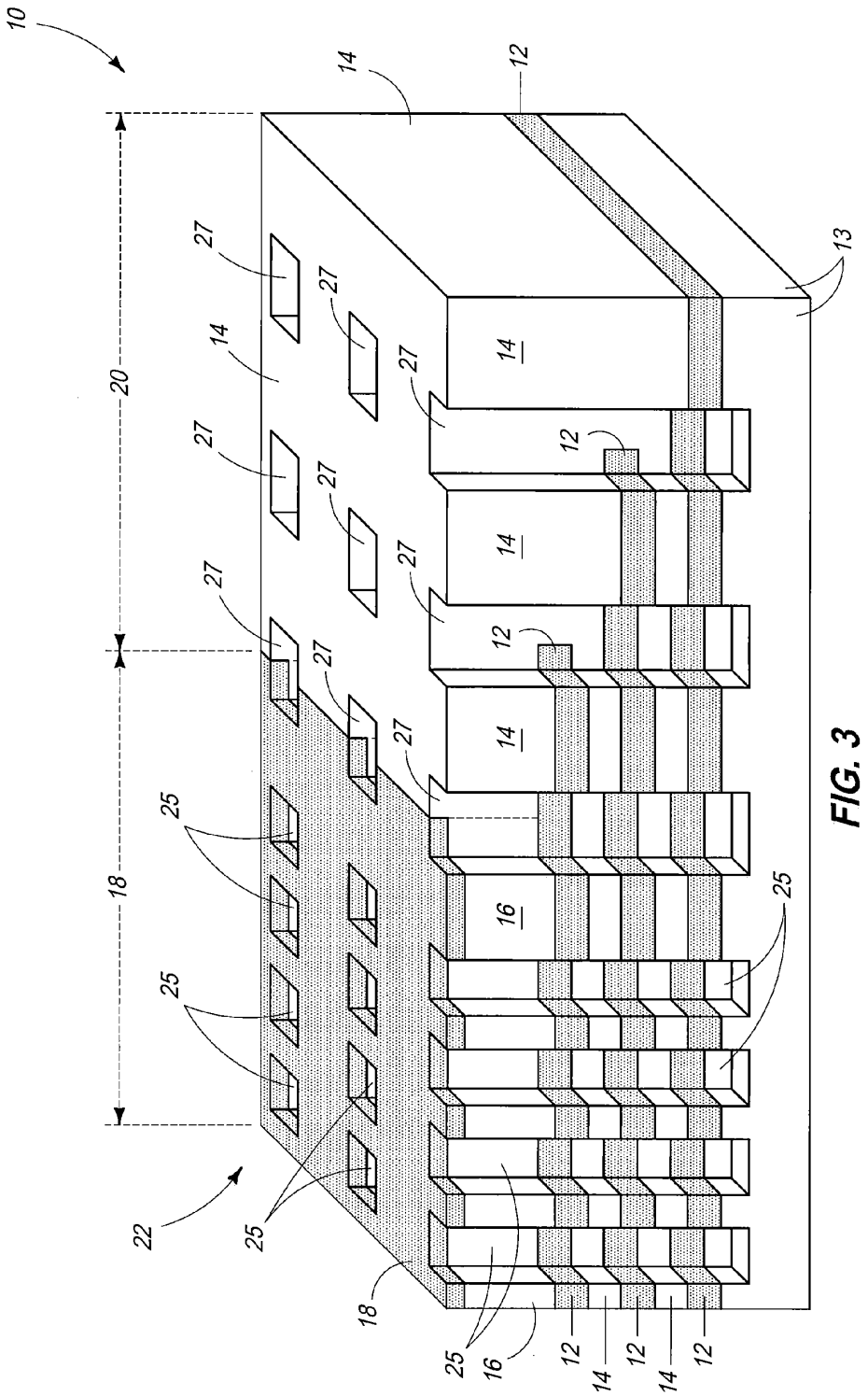


FIG. 3

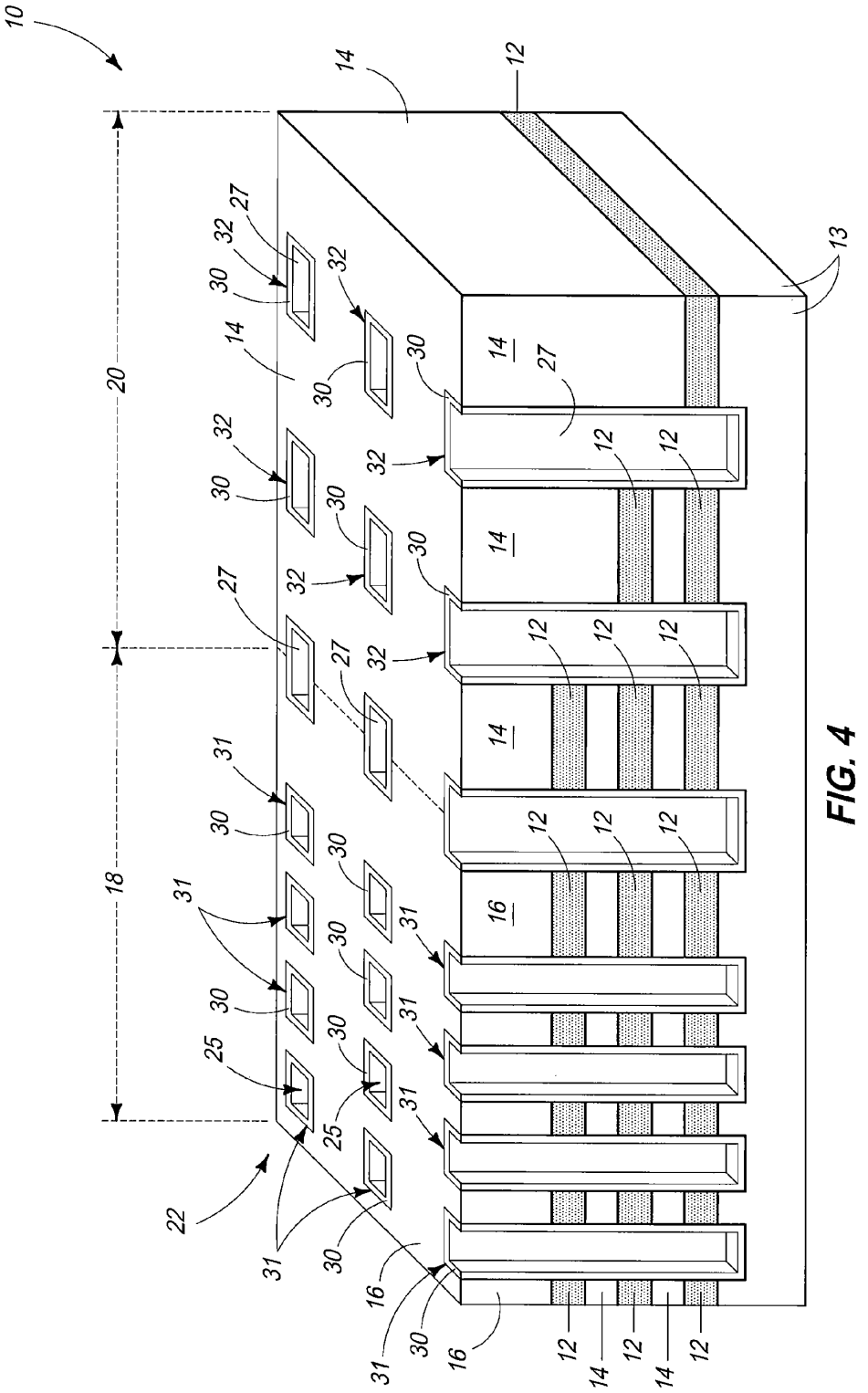


FIG. 4

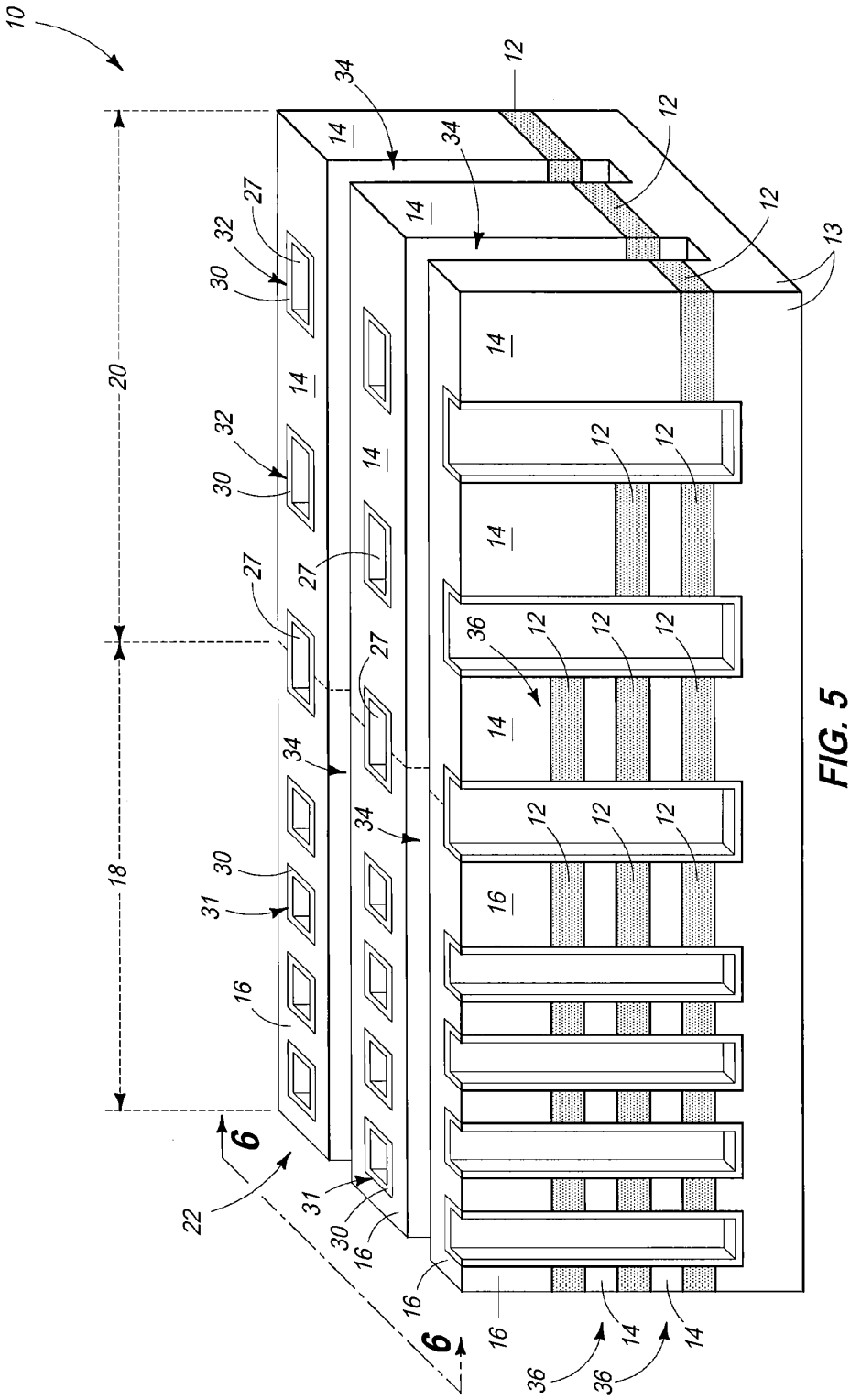


FIG. 5

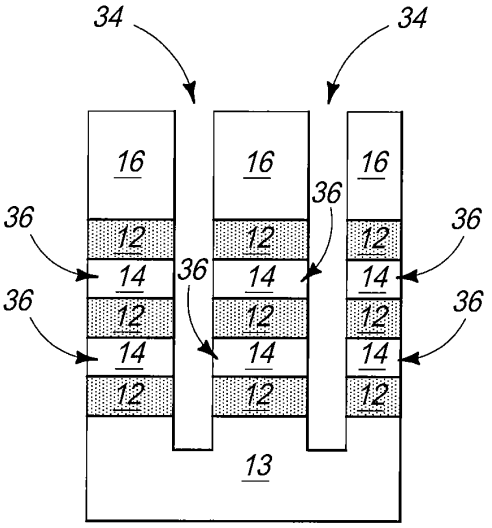

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FIG. 6

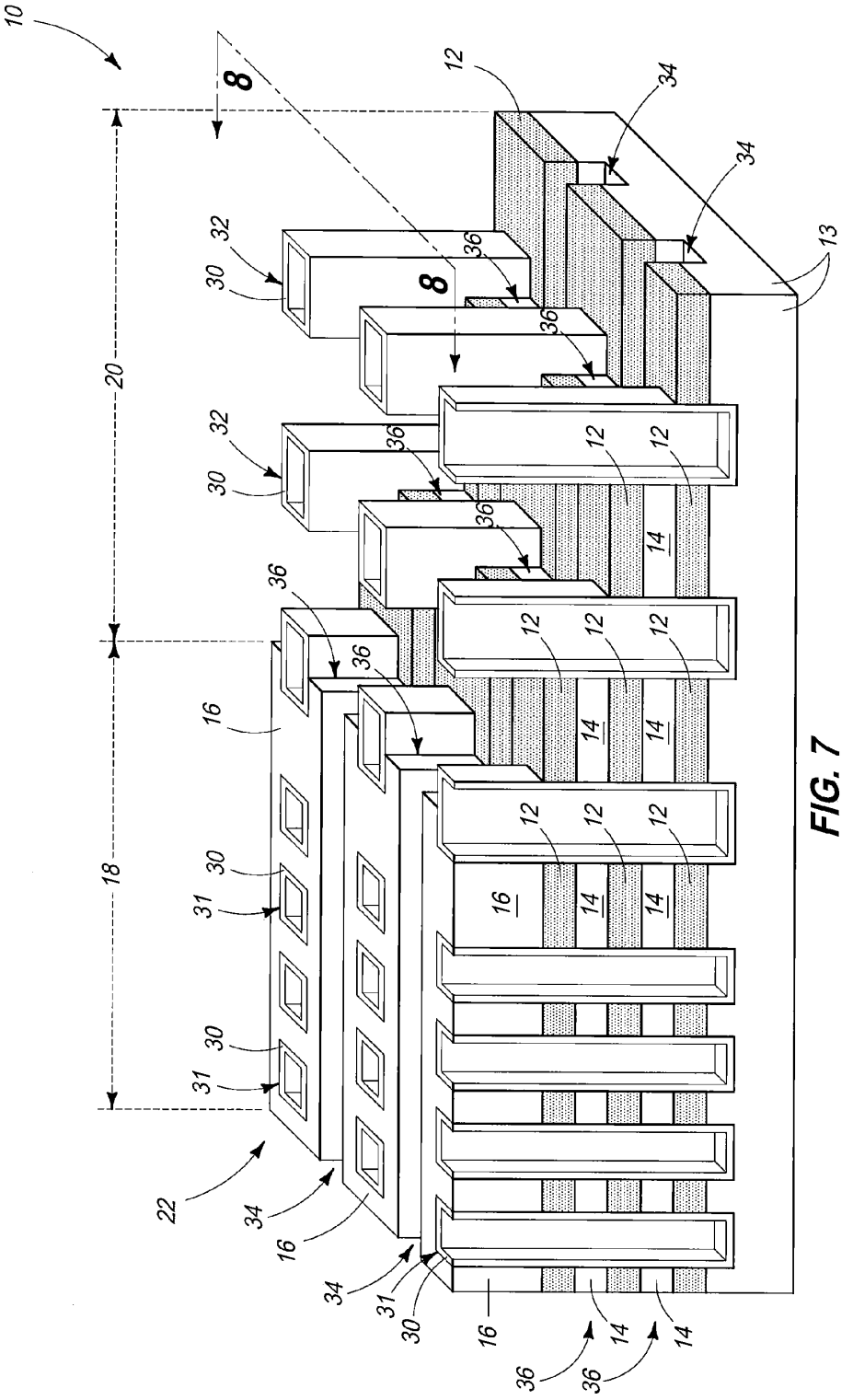

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FIG. 7

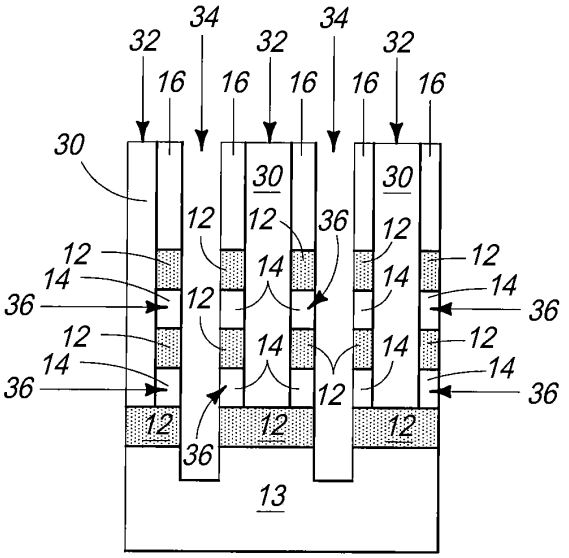

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FIG. 8

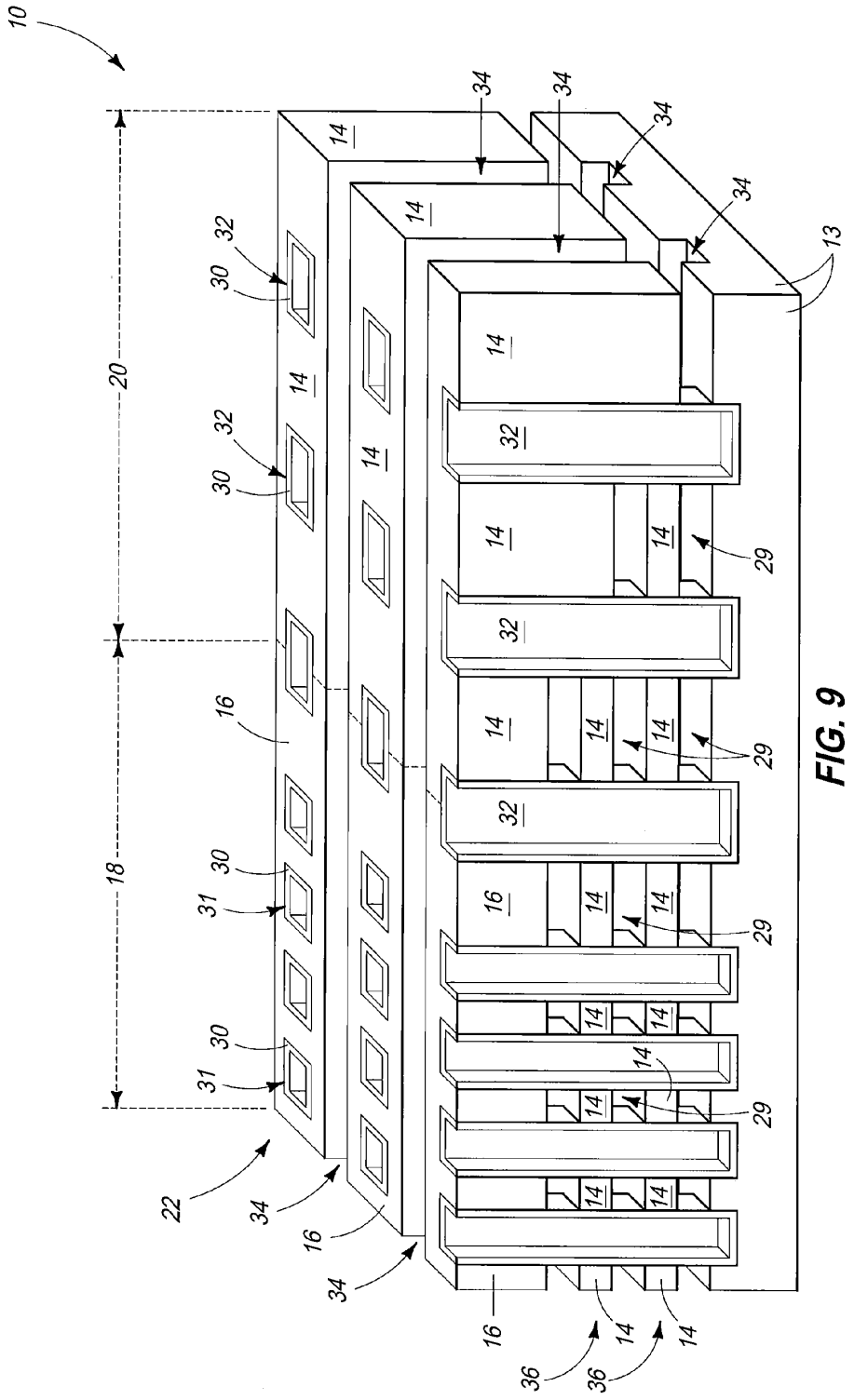


FIG. 9

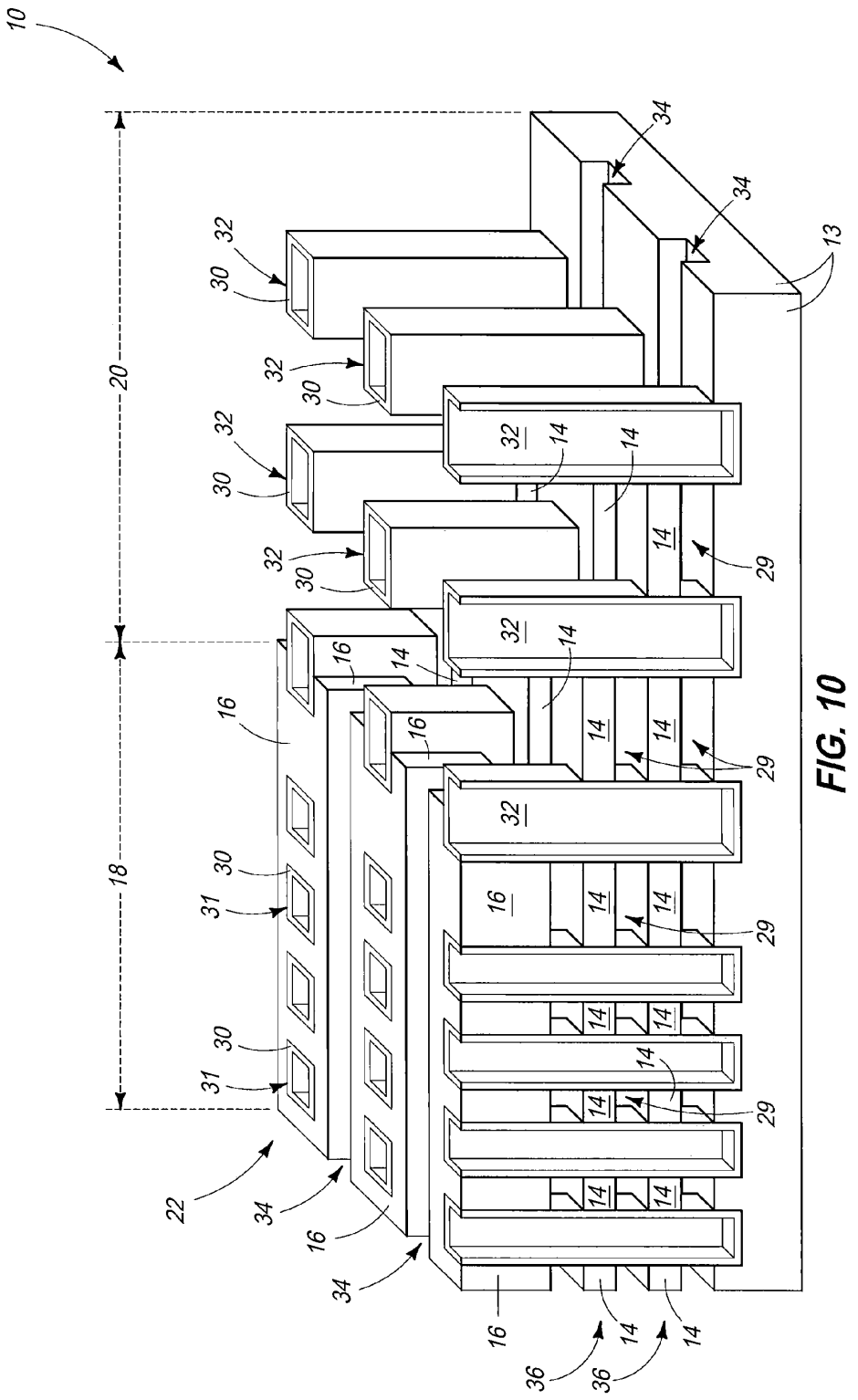


FIG. 10

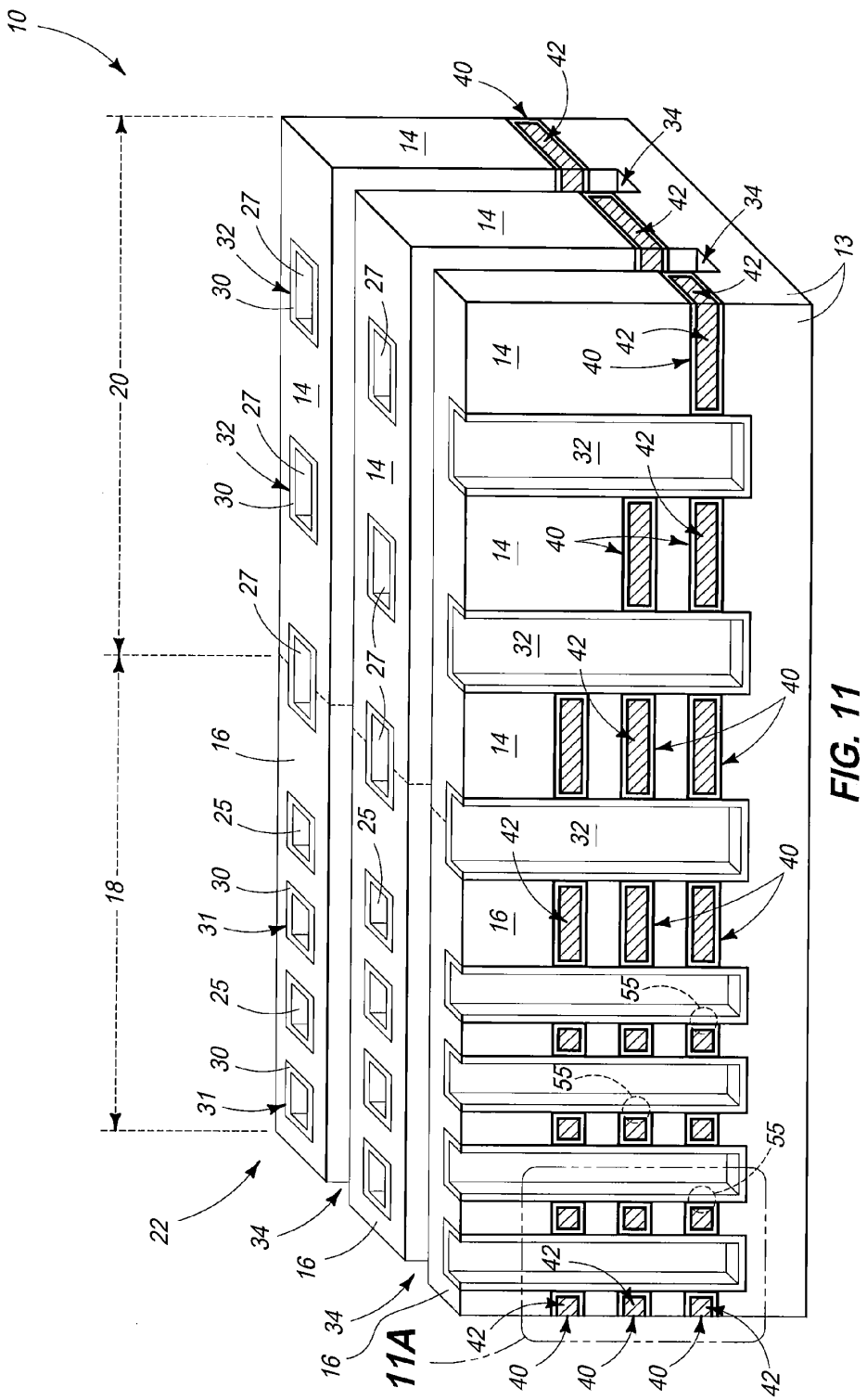


FIG. 11

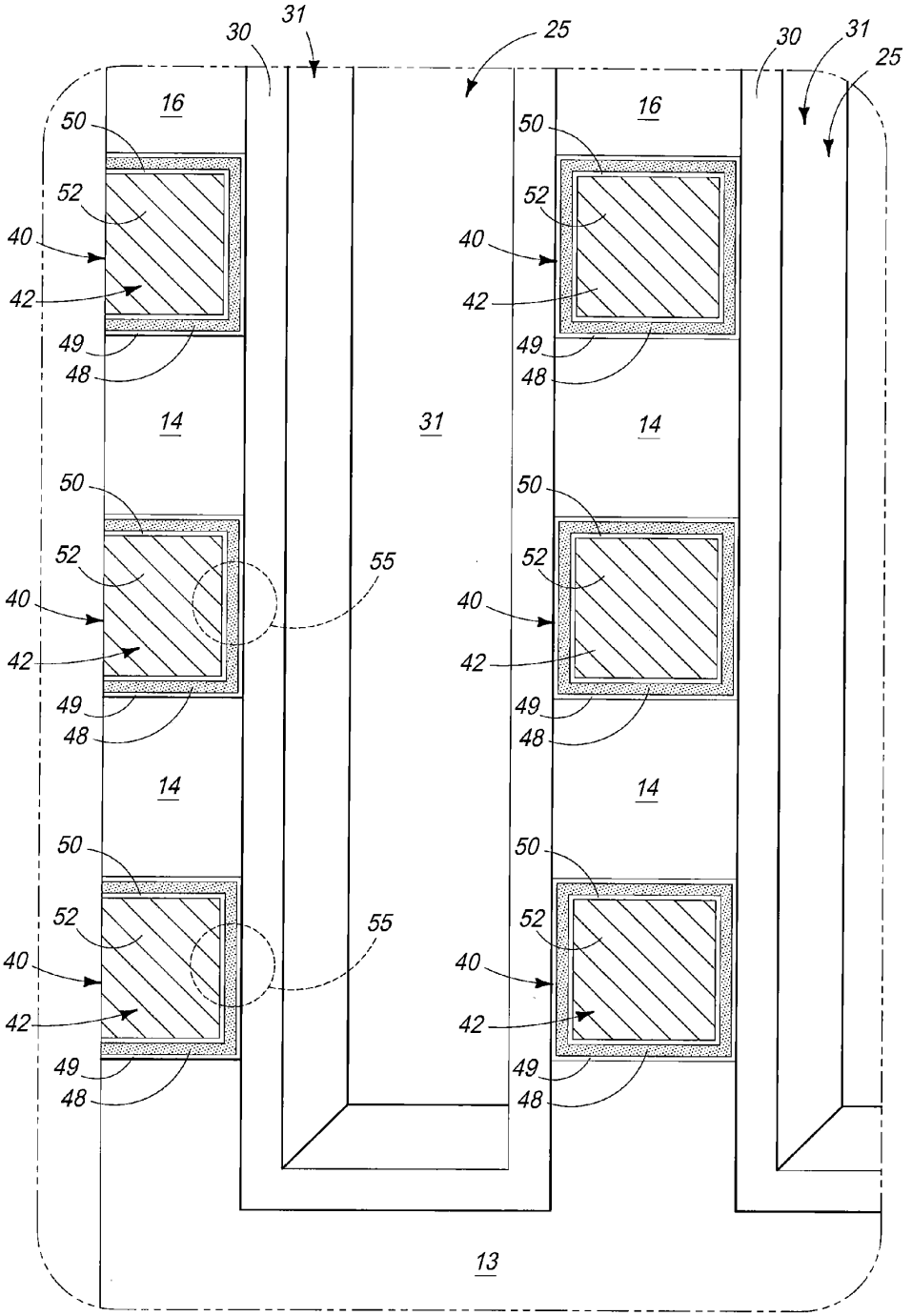


FIG. 11A

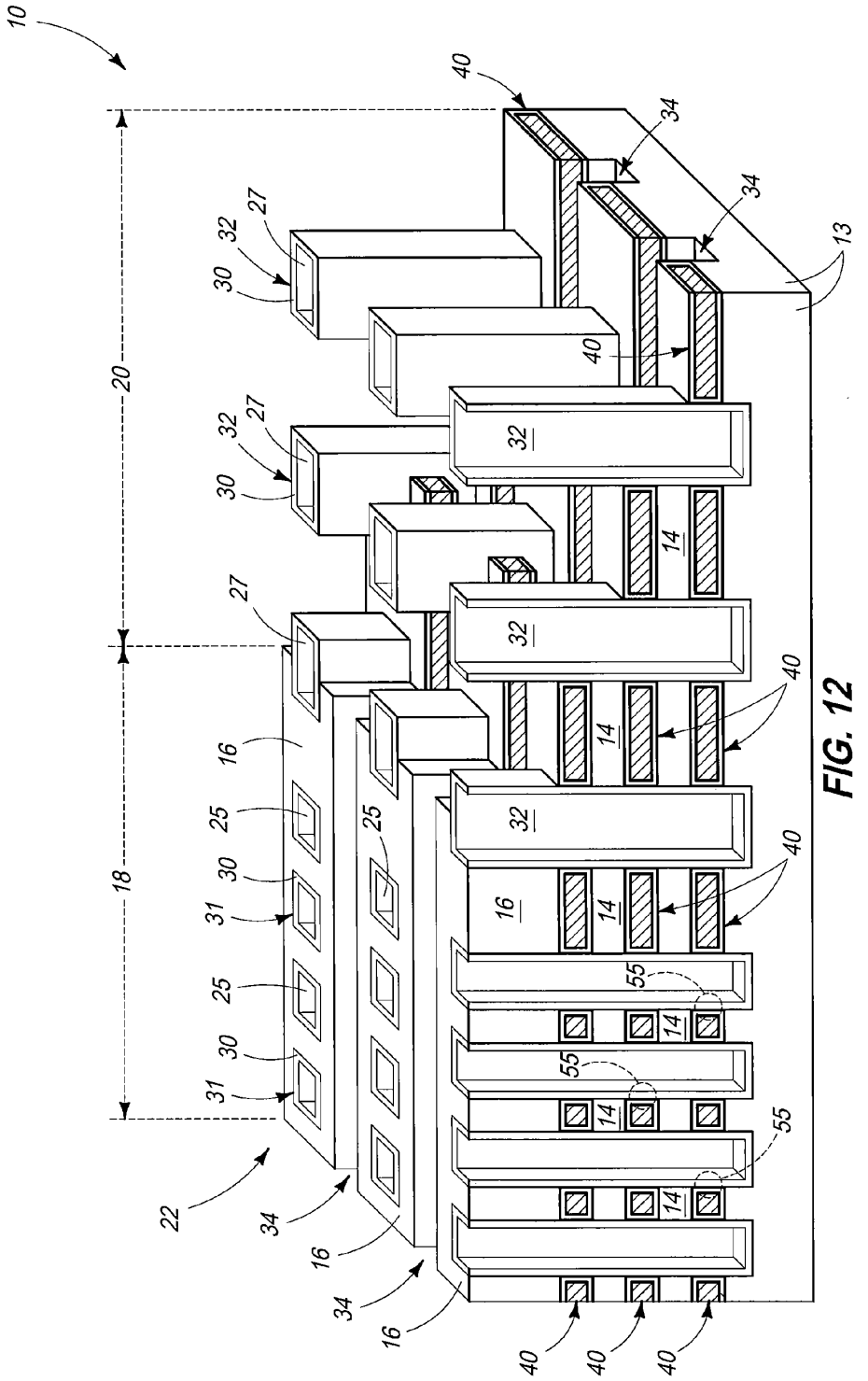


FIG. 12

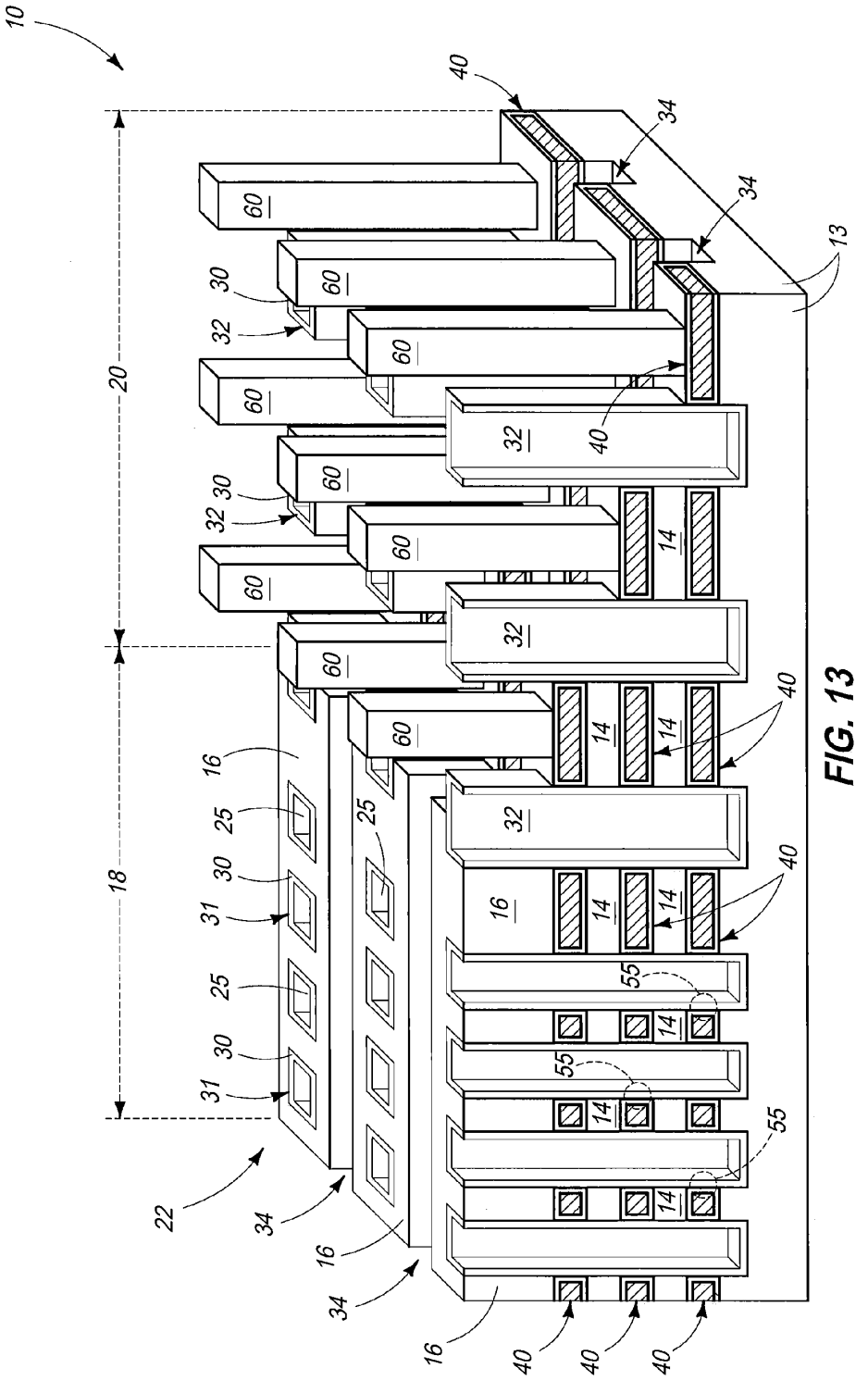


FIG. 13

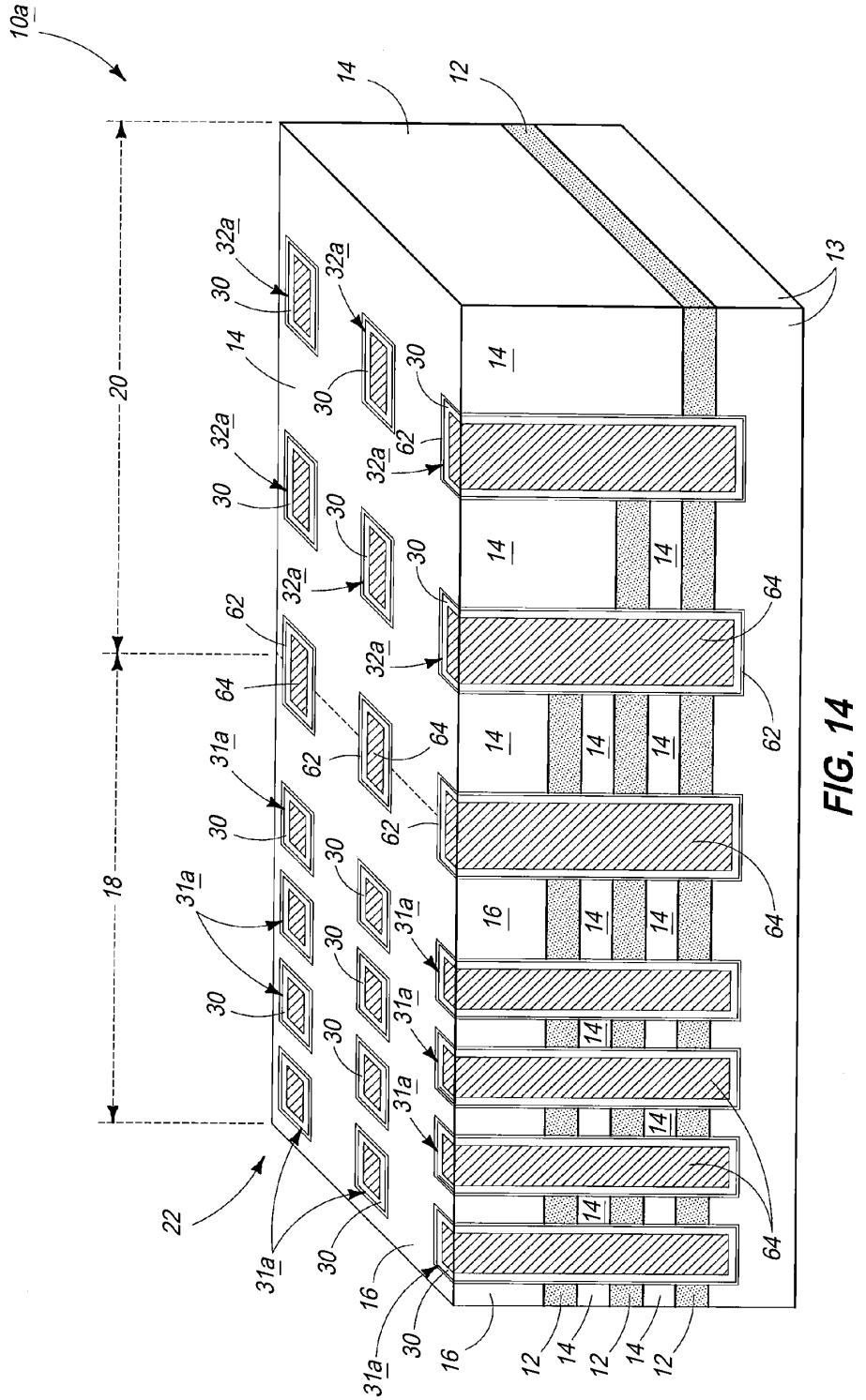


FIG. 14

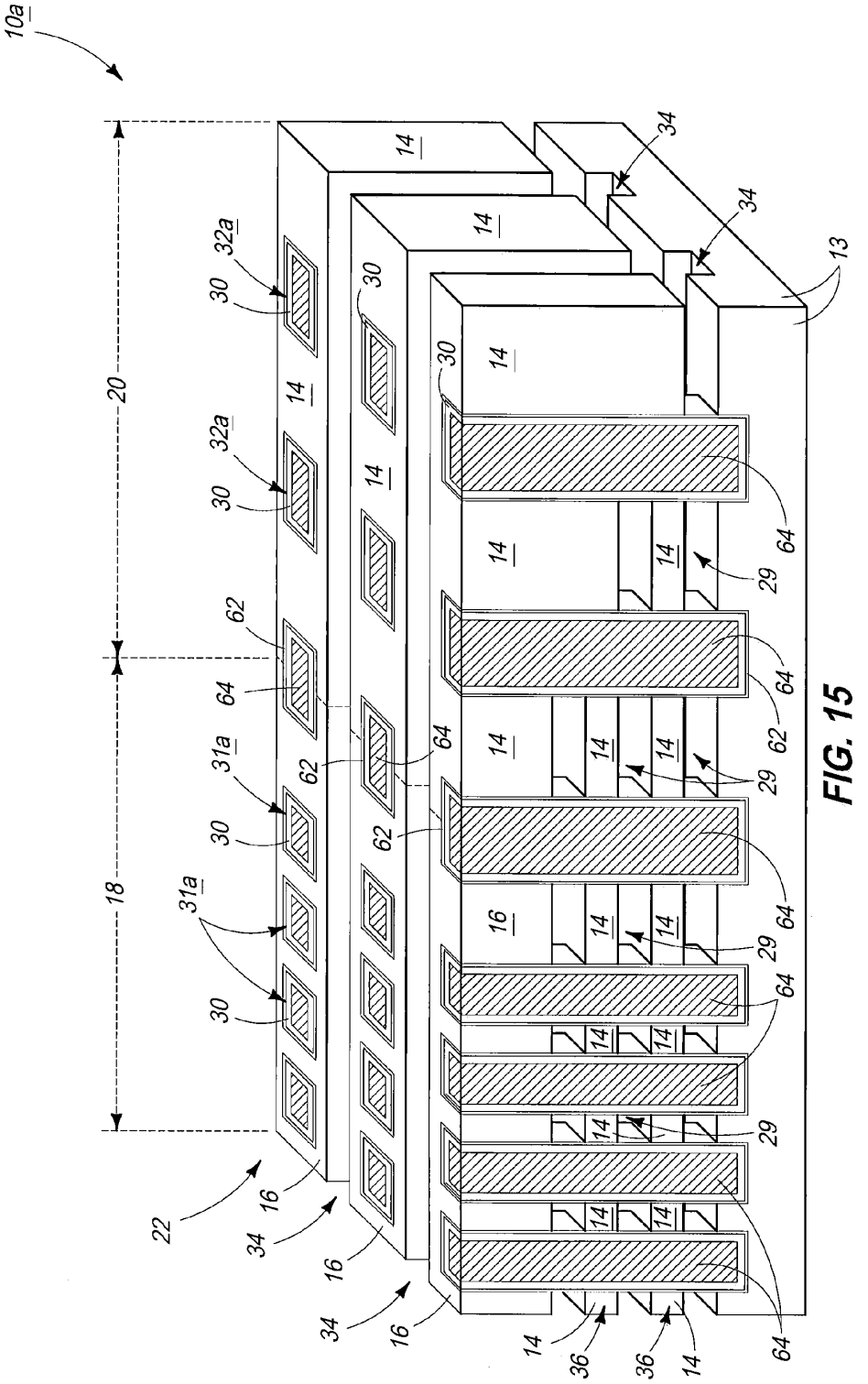


FIG. 15

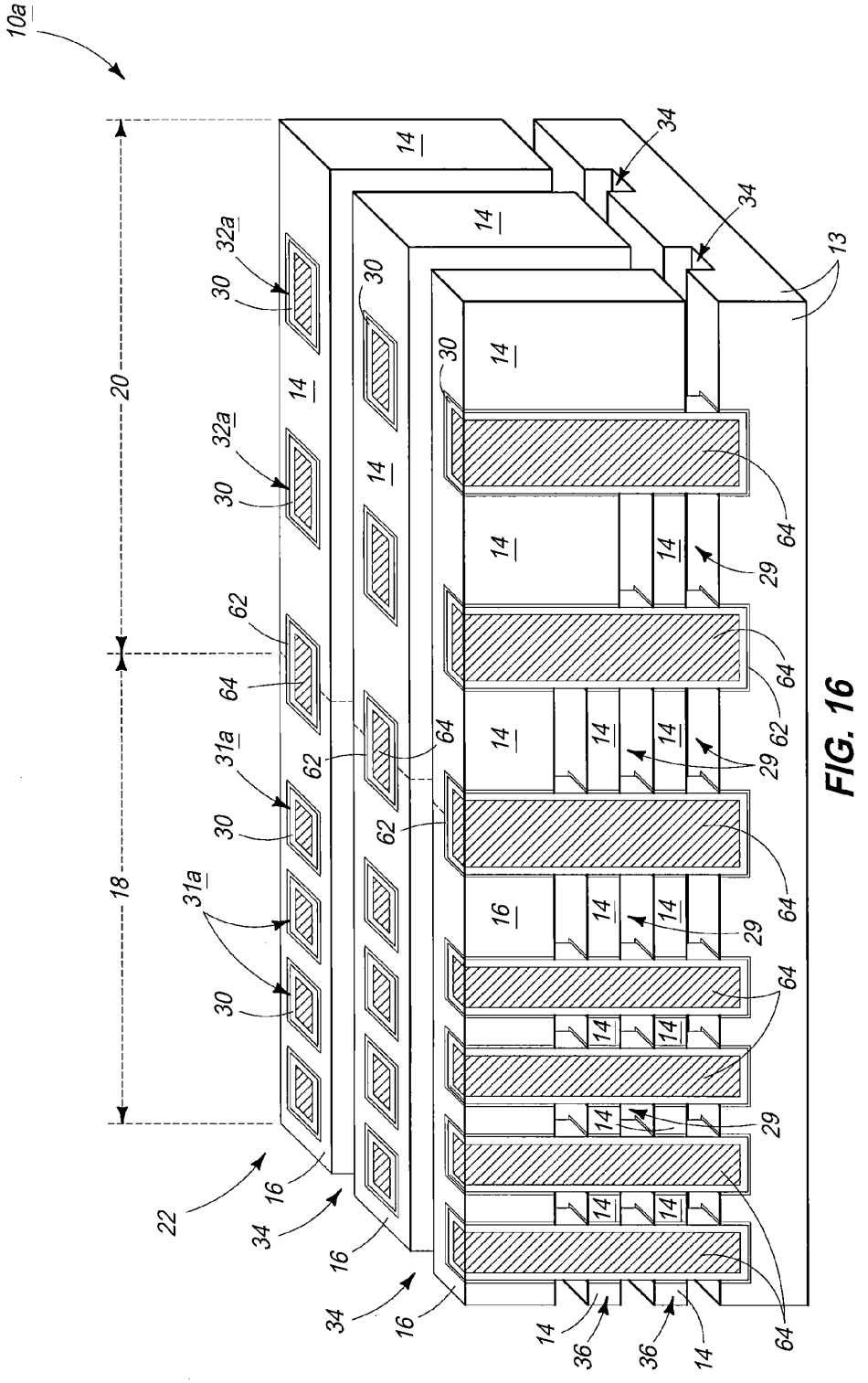


FIG. 16

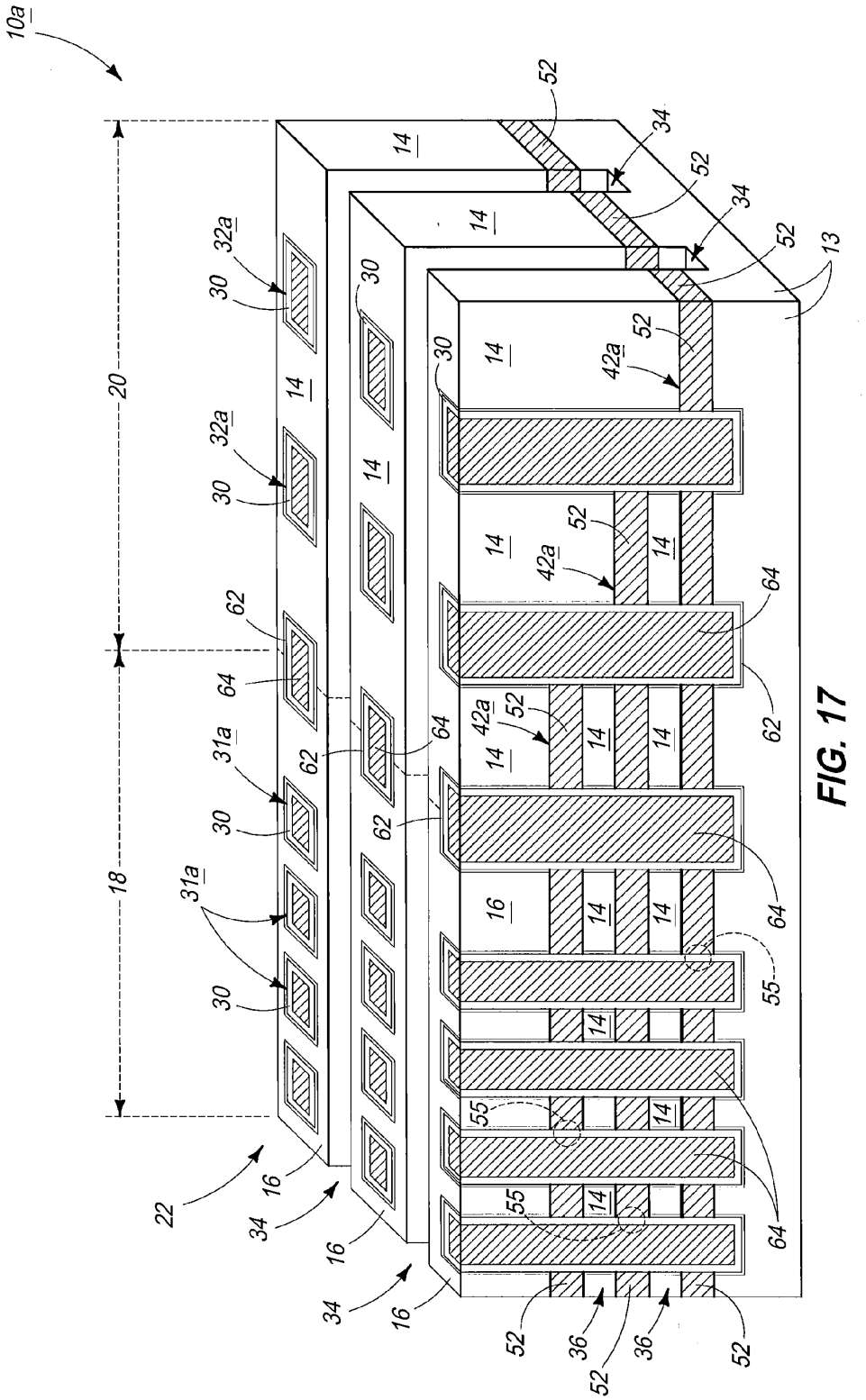


FIG. 17

METHODS OF FORMING CIRCUITRY COMPONENTS AND METHODS OF FORMING AN ARRAY OF MEMORY CELLS

TECHNICAL FIELD

Embodiments disclosed herein pertain to stacks of horizontally extending and vertically overlapping features, and to methods of forming circuitry components and to methods of forming an array of memory cells.

BACKGROUND

Integrated circuits are often formed on a semiconductor substrate such as a silicon wafer or other semiconductive material. In general, layers of various materials which are semiconductive, conductive, or electrically insulative are utilized to form the integrated circuits. By way of examples, the various materials may be doped, ion implanted, deposited, etched, grown, etc. using various processes. A continuing goal in semiconductive processing is to strive to reduce the size of individual circuitry components, thereby enabling smaller and denser integrated circuitry.

Memory is one type of integrated circuitry, and is used in computer systems for storing data. Such is usually fabricated in one or more arrays of individual memory cells. The memory cells might be volatile, semi-volatile, or nonvolatile. Nonvolatile memory cells can store data for extended periods of time, in many instances including when the computer is turned off. Volatile memory dissipates and therefore requires being refreshed/rewritten, in many instances multiple times per second. Regardless, the smallest unit in each array is termed as a memory cell and is configured to store data as one of at least two different selectable states. In a binary system, the states are considered as either a "0" or a "1". In other systems, at least some individual memory cells may be configured to store data as one of more than two selectable states.

Integrated circuitry fabrication continues to strive to produce smaller and denser integrated circuits. Accordingly, the fewer components an individual circuit device has, the smaller the construction of the finished device can be. A simple memory cell will be comprised of two conductive electrodes having a programmable material there-between. The programmable material is selected or designed to be configured in a selected one of at least two different physical memory states to enable storing of information by an individual memory cell. The reading of the cell comprises determination of which of the states the programmable material is in, and the writing of information to the cell comprises placing the programmable material in a target memory state. Some programmable materials retain a memory state in the absence of refresh, and thus may be incorporated into nonvolatile memory cells.

Some programmable materials may contain mobile charge carriers larger than electrons and holes, for example ions in some example applications. Regardless, the programmable materials may be converted from one memory state to another by moving the mobile charge carriers to alter a distribution of charge density within the programmable materials. Some example memory devices that utilize ions as mobile charge carriers are resistive RAM (RRAM) cells, which can include classes of memory cells containing multivalent oxides, and which can include memristors in some specific applications. Other example memory devices that utilize ions as charge carriers are programmable metallization cells (PMCs); which

may be alternatively referred to as a conductive bridging RAM (CBRAM), nanobridge memory, or electrolyte memory.

The RRAM cells may contain programmable material sandwiched between a pair of electrodes. The programming of the RRAM cells may comprise transitioning the programmable material between first a memory state in which charge density is relatively uniformly dispersed throughout the material and a second memory state in which the charge density is concentrated in a specific region of the material (for instance, a region closer to one electrode than the other).

A PMC may similarly have programmable material sandwiched between a pair of current conductive electrodes. The PMC programmable material comprises ion conductive material, for example a suitable chalcogenide or any of various suitable oxides. A suitable voltage applied across the electrodes generates current conductive super-ionic clusters or filaments. Such result from ion transport through the ion conductive material which grows the clusters/filaments from one of the electrodes (the cathode), through the ion conductive material, and toward the other electrode (the anode). The clusters or filaments create current conductive paths between the electrodes. An opposite voltage applied across the electrodes essentially reverses the process and thus removes the current conductive paths. A PMC thus comprises a high resistance state (corresponding to the state lacking a current conductive filament or clusters between the electrodes) and a low resistance state (corresponding to the state having a current conductive filament or clusters between the electrodes), with such states being reversibly interchangeable with one another.

Another type of nonvolatile memory is known as flash memory, a type of EEPROM (electrically-erasable programmable read-only memory) that may be erased and reprogrammed in groups. A typical flash memory array includes a large number of nonvolatile memory cells usually grouped into blocks. Each of the cells within a block may be electrically programmed by charging its programmable gate material. The charge may be removed from the programmable gate material by a block erase operation. NAND is a basic architecture of flash memory. A NAND architecture comprises at least one select gate coupled in series to a serial combination of memory cells (with the serial combination being commonly referred to as a NAND string).

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic oblique view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

FIG. **2** is a view of the FIG. **1** substrate at a processing step subsequent to that shown by FIG. **1**.

FIG. **3** is a view of the FIG. **2** substrate at a processing step subsequent to that shown by FIG. **2**.

FIG. **4** is a view of the FIG. **3** substrate at a processing step subsequent to that shown by FIG. **3**.

FIG. **5** is a view of the FIG. **4** substrate at a processing step subsequent to that shown by FIG. **4**.

FIG. **6** is an end view of FIG. **5** relative to line **6-6** in FIG. **5**.

FIG. **7** is a view of the FIG. **5** substrate wherein certain material in FIG. **5** is not shown in FIG. **7** solely for clarity.

FIG. **8** is an end view of FIG. **7** relative to line **8-8** in FIG. **7**.

FIG. **9** is a view of the FIG. **7** substrate at a processing step subsequent to that shown by FIG. **7**.

FIG. **10** is a view of the FIG. **9** substrate wherein certain material in FIG. **9** is not shown in FIG. **10** solely for clarity.

FIG. **11** is a view of the FIG. **9** substrate at a processing step subsequent to that shown by FIG. **9**.

FIG. **11**A is an enlarged view of a portion of FIG. **11**.

FIG. **12** is view of the FIG. **11** substrate wherein certain material in FIG. **11** is not shown in FIG. **12** solely for clarity.

FIG. **13** is a view of the FIG. **12** substrate at a processing step subsequent to that shown by FIG. **12**.

FIG. **14** is a diagrammatic perspective view of a semiconductor substrate fragment in process in accordance with an embodiment of the invention.

FIG. **15** is a view of the FIG. **14** substrate at a processing step subsequent to that shown by FIG. **14**.

FIG. **16** is a view of the FIG. **15** substrate at a processing step subsequent to that shown by FIG. **15**.

FIG. **17** is a view of the FIG. **16** substrate at a processing step subsequent to that shown by FIG. **16**.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Example embodiments in accordance with the invention of methods of forming circuitry components are initially described with reference to FIGS. **1-10**. In some embodiments, an array of memory cells may be fabricated, for example as described with reference to FIGS. **1-13** and with reference to FIGS. **14-17**. In one embodiment, such may comprise cross-point memory cells (e.g., as shown in FIG. **17**), and in one embodiment may comprise NAND circuitry (e.g., as shown in FIGS. **11**, **11**A, **12**, and **13**).

Referring to FIG. **1**, a substrate fragment **10** comprises a suitable base substrate **13** over which various materials have been provided. Base substrate **13** may be homogenous or non-homogenous, for example comprising multiple different composition materials and/or layers. As examples, such may comprise bulk monocrystalline silicon and/or a semiconductor-on-insulator substrate. As an additional example, such may comprise dielectric material having contacts (e.g., conductive vias) formed therein which extend vertically or otherwise into communicative contact (e.g., current conductive electrical connection) with device components, regions, or material that is elevationally inward of the dielectric material. In this document, vertical is a direction generally orthogonal to a primary surface relative to which the substrate is processed during fabrication and which may be considered to define a generally horizontal direction. Further, "vertical" and "horizontal" as used herein are generally perpendicular directions relative one another independent of orientation of the substrate in three-dimensional space. Further in this document, "elevational" and "elevationally" are with reference to the vertical direction from a base substrate upon which the circuitry is fabricated.

The base substrate may or may not be a semiconductor substrate. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

In one embodiment, substrate **10** comprises a stack of alternating sacrificial material **12** and dielectric material **14** formed over base substrate **13**. Each material **12** and **14** may be homogenous or non-homogenous. In one embodiment, the respective sacrificial materials **12** are of the same composition relative one another. In one embodiment, the respective dielectric materials **14** are of the same composition relative one another. Regardless, sacrificial material **12** may be selectively etchable, in one embodiment highly selectively etchable, relative to dielectric material **14**. In the context of this document, a "selective" etch requires removal of the stated one material relative to another at a rate of at least 1.5:1, and a highly selective etch at a rate of at least about 10:1. Sacrificial material **12** may be any one or more of conductive (e.g., current conductive), dielectric, or semiconductive. By way of an example only, dielectric material **14** may comprise silicon dioxide (whether doped or un-doped), and an example sacrificial material is a conductive or insulative nitride, for example titanium nitride or silicon nitride, respectively. A dielectric material **16** and a hardmask **18** have been provided outwardly of alternating materials **12**, **14**. Each material **16** and **18** may be homogenous or non-homogenous. Dielectric material **16** may be of the same composition as dielectric material **14**, and hardmask material **18** may be of the same composition as sacrificial material **12**. FIG. **1** depicts vertical tiers of three sacrificial materials **12** with two alternating dielectric materials **14**. Additional alternating pairs of sacrificial and dielectric materials may be provided elevationally inward of innermost sacrificial material **12** or elevationally outward of outermost sacrificial material **12**.

Stack of alternating materials **12**, **14** may be considered as comprising a primary portion **18** and an end portion **20**. The end portion in the depicted embodiment has been patterned to form a stair step-like construction. Such may be formed to provide horizontal area for later forming contacts to components, regions, or material in end portion **20** as will be apparent in the continuing discussion. In one embodiment and as shown, end portion **20** comprises individual stairs **21** which at least include sacrificial material **12**.

In one embodiment, materials **12** and **14** may be features (e.g., plates), such as plates or features that are plate-like, whether continuously and/or discontinuously formed. In one embodiment, a method of forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping plates at least some of which increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Either of collective materials **12** or **14** may be considered in such example embodiment as comprising such plates, or materials **12** and **14** in combination in the depicted embodiment may be considered as such plates. In one embodiment, the horizontally extending and vertically overlapping plates are dielectric, for example plates **14** regardless of the composition of sacrificial material **12**. In one embodiment, all of the plates increase in horizontal extent in the vertical inward direction in the end portion of the stack. For example in the embodiment of FIG. **1**, either of collective plates **12** or collective plates **14** may be considered as plates all of which increase in horizontal extent progressing vertically inward in the end portion of the stack. Alternately, a composite of each immediately adjacent plate pairs **12**, **14** may be considered as respective plates which increase in horizontal extent in the vertical inward direction in end portion **20** of the stack.

In one embodiment, primary portion **18** and end portion **20** comprise a portion of an array area **22** within which a plurality of memory cells will be fabricated. Logic circuitry (not shown) may be fabricated outside of the array area. Control and/or other peripheral circuitry (not shown) for operating the

memory array may or may not fully or partially be within the array area, with an example array area as a minimum encompassing all of the memory cells of the given array/sub-array. Further, multiple sub-arrays might also be fabricated and operated independently, in tandem, or otherwise relative one another. As used in this document, a "sub-array" may also be considered as an array.

Referring to FIG. **2**, dielectric material has been formed over substrate **10** and planarized at least to the outermost surface of hardmask **18**. The dielectric material may be homogenous or non-homogenous and, in one embodiment, may be of the same composition as that of material **14** and is so shown and designated in the figures.

Referring to FIG. **3**, first openings **25** have been formed into primary portion **18** of the stack and second openings **27** have been formed into end portion **20** of the stack. Any openings which overlap the primary and end portions may be such first or second openings (i.e., as primary portion openings or end portion openings), with example such openings being shown in FIG. **3** and designated as second openings **27**. Openings **25**, **27** may be formed through each plate **12**, **14**. An example technique for forming openings **25**, **27** is by photolithographic patterning followed by subtractive anisotropic etching. First openings **25** need not be of the same shape and/or density relative one another. Second openings **27** need not be of the same shape and/or density relative one another, or relative to any one or more of first openings **25**. As examples, openings **25** and **27** may be formed to have the same horizontal and vertical cross sections (not shown). Alternately, openings **25** and **27** may be formed to have at least one of different horizontal cross sections (as shown) or different vertical cross sections (as shown). Further and regardless, openings **25** and **27** may be formed at the same time or at different times, and/or may use the same masking step or different masking steps where, for example, photolithographic or other masking is used. In one embodiment and as shown, at least some of openings **27** in end portion **20** are formed to horizontally overlap ends of individual plates **12** and/or **14**.

At least one of conductive material, semiconductive material, and programmable material is/are deposited into the openings. In one embodiment where conductive material is deposited into the openings, such may comprise current conductive material. In the context of this document, current conductive material can include a composition where electric current flow may inherently occur therein predominantly by movement of subatomic positive and/or negative charges when such are generated as opposed to predominantly by movement of ions. Example current conductive materials are elemental metals, alloys of elemental metals, current conductive metal compounds, and conductively doped semiconductive material, including any combinations thereof.

In one embodiment, the depositing of the conductive material, semiconductive material and/or programmable material occurs simultaneously into all of the openings in the primary portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in the end portion. In one embodiment, the depositing of such material occurs simultaneously into all of the openings in both of the primary and end portions. Operative structures (e.g., circuit components, such as local vertical extensions) are formed therewith in the openings in the primary portion, and dummy structures (e.g. dummy vertical extensions) are formed therewith in the openings in the end portion. In the context of this document, a "dummy" structure is a structure which is used to mimic a physical property of another structure (e.g., load carrying ability of an operative structure) and which may comprise a circuit inoperable electrical dead end (e.g., is not part of a current flow path of a circuit even if conductive). Openings in which dummy structures are formed may be considered as "dummy openings".

For example referring to FIG. **4**, a material **30** has been deposited within openings **25**, **27**, and then planarized back through hardmask material **18** (not shown). An example thickness for material **30** is from about 100 to about 150 Angstroms. Material **30** may be homogenous or non-homogenous, and may comprise one or more of conductive material (e.g., current conductive material), semiconductive material, and programmable material. In one embodiment, material **30** comprises semiconductive material. Further in such embodiment, the semiconductive material may comprise interconnected channels of a plurality of vertically oriented transistors, and in one embodiment comprises interconnected channels of vertically oriented charge storage transistors as will be apparent from the continuing discussion. Regardless, in one embodiment, material **30** may form operative structures **31** (e.g., operative circuit components **31**) within primary portion openings **25** and form dummy structures **32** (e.g., dummy circuit components) within end portion openings **27**. In one embodiment and as shown, such operative structures **31** and dummy structures **32** are in the form of hollow cylinders. Alternately by way of example, such may be in the form of laterally solid pillars (not shown in FIG. **4**). Regardless, the above processing describes but examples of forming operative structures **31** vertically through plates **12** and/or **14** in primary portion **18** and forming dummy structures **32** vertically through plates **12** and/or **14** in end portion **20**. In one embodiment, the operative and dummy structures may comprise the same material (as shown). In one embodiment, the operative and dummy structures may comprise a plurality of the same materials (not shown in FIG. **4**), and in one such embodiment be arranged in the same lateral order relative one another in the operative and dummy structures. In one embodiment, the operative and dummy structures may consist essentially of the same material.

Referring to FIGS. **5-8**, horizontally elongated openings **34** (e.g., trenches) have been formed through plates **12** and/or **14**, and laterally between material **30**, to form horizontally elongated and vertically overlapping lines **36** from material of the plates. Lines **36** individually extend from primary portion **18** into end portion **20** and individually laterally about sides of vertically extending portions of both operative structures **31** and dummy structures **32**. FIGS. **7** and **8** are views of FIGS. **5** and **6**, respectively, wherein dielectric material **14** added in FIG. **2** is removed solely for clarity in such drawings. Where either of operative structures **31** or dummy structures **32** are upwardly open (e.g., as shown), such may be partially or wholly filled (not shown) with dielectric and/or other material prior to the forming of horizontally elongated openings **34**.

Referring to FIGS. **9** and **10**, at least some of sacrificial material **12** that is elevationally between lines **36** within primary portion **18** and end portion **20** has been removed from being laterally between horizontally elongated openings **34**. Such thereby, in one embodiment, forms void spaces **29** elevationally between vertically spaced horizontal dielectric lines **36**. An example technique includes etching, for example isotropic dry and/or wet etching. Etching may be conducted selectively (ideally, highly selectively) relative to lines **36**, operative structures **31**, and dummy structures **32**. FIG. **10** is a view of the FIG. **9** substrate wherein dielectric material **14** added in FIG. **2** is removed solely for clarity in such drawing.

The above processing discloses but example embodiments of forming circuitry components in accordance with some aspects of the invention. In one embodiment, a method of

forming circuitry components comprises forming a stack of horizontally extending and vertically overlapping features. By way of example only, such features may comprise plates, with the example depicted structure of plates **14** comprising but one example of such plates. Regardless, in such embodiment, the stack comprises a primary portion and an end portion wherein at least some of the features increase in horizontal extent in the vertical inward direction in the end portion of the stack (i.e., at least some of which extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion). Operative structures **31** (e.g., circuit components) are formed vertically through the features in the primary portion and dummy structures **32** (e.g., dummy circuit components) are formed vertically through the features in the end portion. The processing depicted through FIG. **4**, or through FIGS. **5-8**, are examples. The operative and dummy structures may comprise the same material, and in one embodiment may consist essentially of the same material. The dummy structures may support material of the features from vertical movement in the end portion while at least some of sacrificial material that is elevationally between the material of the features in the primary and end portions is removed. The processing depicted in going from that of FIGS. **5-8** to that of FIGS. **9** and **10** is but one such example processing. With respect to a prior art problem, dummy structures heretofore have not been provided in a stair-like end portion of an array. Accordingly, the floors/ceilings that are vertically between the respective void spaces **29** in FIGS. **9** and **10** may be sagged, bent, or broken during processing due to lack of support. In accordance with one embodiment of the invention, dummy structures in the end portion support the features (e.g., the respective ceilings and floors, or plates) from vertical movement, for example by laterally engaging side portions of such floors/ceilings that were created where such dummy structures extend there-through. Regardless, other attributes as described may be employed.

Additional processing may occur in fabricating integrated circuitry, for example in fabricating an array of memory cells as next described with reference to FIGS. **11-13**. Referring to FIGS. **11** and **11**A, material **40** has been isotropically deposited within horizontally elongated openings **34**, former void spaces **29** (not shown in FIGS. **11**, **11**A), and any remaining volume of openings **25**, **27**. Material **40** has subsequently been removed from horizontally elongated openings **34** to form vertically spaced horizontal conductive lines **42** within the void spaces elevationally between horizontal lines **36** of dielectric material **14**. In one embodiment, conductive lines **42** collectively cross a row of the operative and dummy structures at different respective elevations. In one embodiment, individual structures **31**, **32** cross different conductive lines at different respective elevations. In the depicted example, conductive lines **42** extend longitudinally straight linear. Alternately by way of example, some or all of lines **42** may not be straight linear, for example being longitudinally curvilinear (not shown). Material **40** may also be removed from the remaining internal volume of openings **25**, **27** as shown. FIG. **12** depicts the circuitry of FIG. **11** wherein the dielectric material that is shown as being deposited in FIG. **2** is removed solely for clarity.

FIGS. **11**, **11**A, and **12** depict but one example embodiment comprising NAND circuitry wherein operative structures **31** comprise interconnected channel regions of a NAND string. In such example embodiment, material **40** comprises a composite of a suitable tunnel dielectric **49** (FIG. **11**A), floating gate/charge trapping material **48**, dielectric **50**, and conductive control gate material **52**. Thereby, conductive material **52** provides but an example conductive portion of conductive lines **42** that is within the void spaces between the horizontal lines of dielectric material, and which collectively cross a row of the operative and dummy structures at different respective elevations. Individual ones of the memory cells of the example circuitry of FIGS. **11** and **11**A comprise an intersection of an individual horizontal conductive line and an individual operative structure (e.g., in the form of a string of channels of NAND), and some of which are indicated with reference numeral **55**.

In one embodiment, a respective contact may be formed to a stair extension of individual ones of horizontal conductive lines **42** in end portion **20** for making communicative connection to circuitry. One such example is diagrammatically shown in FIG. **13**. The dielectric material **14** of FIG. **2** is again showed removed solely for clarity in depicting certain components. Specifically, FIG. **13** shows example individual contacts **60** (e.g., current conductive contacts) which may be formed through the dielectric material **14** (not shown) of FIG. **2** for making communicative connection to circuitry, such as that elevationally outward of that depicted by FIG. **13** with respect to each conductive line **42**.

Circuitry components other than or in addition to components of memory cells may be fabricated in accordance with embodiments of the invention.

An example embodiment of a method of forming an array of cross-point memory cells is next described with reference to FIGS. **14-17**. Like numerals from the above-described embodiments have been used where appropriate, with some construction differences being indicated with the suffix "a" or with different numerals. FIG. **14** depicts an alternate embodiment substrate fragment **10***a* to that depicted by FIG. **4**. In FIG. **14**, openings **25**, **27** have been lined with a first material **62**. In one embodiment, such material is dielectric (i.e., a 15 to 30 Angstroms thick layer of undoped silicon dioxide). Thereafter, a programmable material **30** was deposited to line over first material **62** within openings **25**, **27**. Then, remaining volume of openings **25**, **27** has been filled with conductive material **64**, and materials **62**, **30**, and **64** planarized back to materials **14** and **16**. Horizontally elongated openings (not shown in FIG. **14**) may then be formed analogous to the processing depicted by FIGS. **5-8**.

Programmable material **30** may be solid, gel, amorphous, crystalline, or any other suitable phase. Any existing or yet-to-be developed programmable material may be used, with only some examples being provided below.

One example programmable material is ion conductive material. Example suitable such materials comprise chalcogenide-type (for instance, materials comprising one or more of germanium, selenium, antimony, tellurium, sulfur, copper, etc.; with example chalcogenide-type materials being $Ge_2Sb_2Te_5$, GeS_2, $GeSe_2$, CuS_2, and CuTe) and/or oxides such as zirconium oxide, hafnium oxide, tungsten oxide, copper oxide, niobium oxide, iron oxide, silicon oxide (specifically, silicon dioxide), gadolinium oxide, etc. capable of inherently (or with additive) supporting electrolyte behavior. Such may have silver, copper, cobalt, and/or nickel ions, and/or other suitable ions, diffused therein for ionic conduction, analogously to structures disclosed in U.S. Pat. No. 7,405,967 and U.S. Patent Publication Number 2010/0193758.

Additional example programmable materials include multi-resistive state metal oxide-comprising material. Such may comprise, for example, at least two different layers or regions generally regarded as or understood to be active or passive regions, although not necessarily. Alternately, such may only comprise active material. Example active cell region compositions which comprise metal oxide and can be

configured in multi-resistive states include one or a combination of $Sr_xRu_yO_z$, Ru_xO_y, and $In_xSn_yO_z$. Other examples include MgO, Ta_2O_5, $SrTiO_3$, $SrZrO_3$, $BaTiO_3$, $Ba_{(1-x)}Sr_xTiO_3$, ZrO_x (perhaps doped with La), and $CaMnO_3$ (doped with one or more of Pr, La, Sr, or Sm). Example passive cell region compositions include one or a combination of Al_2O_3, TiO_2, and HfO_z. Regardless, a programmable material composite might comprise additional metal oxide or other materials not comprising metal oxide. Example materials and constructions for a multi-resistive state region comprising one or more layers including a programmable metal oxide-comprising material are described and disclosed in U.S. Pat. Nos. 6,753,561; 7,149,108; 7,067,862; and 7,187,201, as well as in U.S. Patent Application Publication Nos. 2006/0171200 and 2007/0173019. Further as is conventional, multi-resistive state metal oxide-comprising materials encompass filament-type metal oxides, ferroelectric metal oxides and others, and whether existing or yet-to-be developed, as long as resistance of the metal oxide-comprising material can be selectively changed.

The programmable material may comprise memristive material. As an example, such material may be statically programmable semiconductive material which comprises mobile dopants that are received within a dielectric such that the material is statically programmable between at least two different resistance states. At least one of the states includes localization or gathering of the mobile dopants such that a dielectric region is formed and thereby provides a higher resistance state. Further, more than two programmable resistance states may be used. In the context of this document, a "mobile dopant" is a component (other than a free electron) of the semiconductive material that is movable to different locations within said dielectric during normal device operation of repeatedly programming the device between at least two different static states by application of voltage differential to the pair of electrodes. Examples include atom vacancies in an otherwise stoichiometric material, and atom interstitials. Specific example mobile dopants include oxygen atom vacancies in amorphous or crystalline oxides or other oxygen-containing material, nitrogen atom vacancies in amorphous or crystalline nitrides or other nitrogen-containing material, fluorine atom vacancies in amorphous or crystalline fluorides or other fluorine-containing material, and interstitial metal atoms in amorphous or crystalline oxides. More than one type of mobile dopant may be used. Example dielectrics in which the mobile dopants are received include suitable oxides, nitrides, and/or fluorides that are capable of localized electrical conductivity based upon sufficiently high quantity and concentration of the mobile dopants. The dielectric within which the mobile dopants are received may or may not be homogenous independent of consideration of the mobile dopants. Specific example dielectrics include TiO_2, AlN, and/or MgF_2. Example programmable materials that comprise oxygen vacancies as mobile dopants may comprise a combination of TiO_2 and TiO_{2-x} in at least one programmed resistance state depending on location of the oxygen vacancies and the quantity of the oxygen vacancies in the locations where such are received. An example programmable material that comprises nitrogen vacancies as mobile dopants is a combination of MN and AlN_{1-x} in at least one programmed state depending on location of the nitrogen vacancies and the quantity of the nitrogen vacancies in the locations where such are received. An example programmable material that comprises fluorine vacancies as mobile dopants may is a combination of MgF_2 and MgF_{2-x} in at least one programmed resistance state depending on location of the fluorine vacancies and the quantity of the fluorine vacancies in the locations where such are received. As another example, the mobile dopants may comprise aluminum atom interstitials in a nitrogen-containing material.

Still other example programmable materials include polymer materials such as Bengala Rose, AlQ_3Ag, Cu-TCNQ, DDQ, TAPA, and fluorescine-based polymers.

Referring to FIG. **15**, such corresponds in processing sequence to that of FIG. **9** of the above-described embodiments. Sacrificial material **12** (not shown) has been at least partially removed (e.g., by etching) between dielectric lines **36** in primary portion **18** and end portion **20** laterally between horizontally elongated openings **34**. Material **12** may be etched selectively (ideally, highly selectively) relative to dielectric lines **36**, first material lining **62**, and conductive material **64** in openings **25**, **27**. FIGS. **14** and **15** depict an example embodiment wherein the operative and dummy structures comprise a plurality of the same materials, and in such embodiment arranged in the same lateral order relative one another in the operative and dummy structures. Regardless, in one embodiment, first material lining **62** may serve as a protecting barrier from adverse exposure of programmable material **30** to the etching chemistry which etches the sacrificial material.

Referring to FIG. **16**, at least a portion of first material **62** has been removed elevationally between dielectric lines **36** to expose laterally outer sidewalls of programmable material **30** that is elevationally between dielectric lines **36**. An example technique for doing so where material **62** comprises silicon dioxide includes etching with a dilute HF solution.

Referring to FIG. **17**, at least a portion of sacrificial material **12** (not shown) of FIG. **14** has been replaced with conductor material **52** (e.g., current conductive material) that is in electrical connection with the laterally outer sidewalls of programmable material **30** and to comprise vertically spaced horizontal conductive lines **42***a*. Materials **64** and **52** may be of the same composition or of different compositions. Further and regardless, conductive material **64** within remaining volumes of openings **25**, **27** alternately may be provided subsequent to the etching depicted by FIG. **15**. Regardless, FIG. **17** also depicts conductor material **52** as having been at least partially removed from horizontally elongated openings **34** to form such vertically spaced horizontal conductive lines **42***a*.

Individual ones of the cross-point memory cells comprise crossing ones of the horizontal conductive lines in the primary portion and conductive material in the openings in the primary portion having the programmable material therebetween, with some of such example memory cells being indicated with reference numeral **55** in the FIG. **17** example embodiment.

An embodiment of the invention includes a stack of horizontally extending and vertically overlapping features. The stack comprises a primary portion and an end portion. At least some of the features extend farther in the horizontal direction in the end portion moving deeper into the stack in the end portion. Operative structures extend vertically through the features in the primary portion. Dummy structures extend vertically through the features in the end portion. In one embodiment, the features may be horizontally extending lines, for example formed of any one or combination of conductive (e.g., current conductive), semiconductive, and/or dielectric material(s). In one embodiment, the features comprise a combination of horizontally extending conductive and dielectric lines (e.g., overlapping and alternating such lines). In one embodiment, contacts may be in the end portion, for example extending vertically to the lines. Any other attribute

as described above may be used, for example as shown and described with respect to FIGS. **1-13** and with respect to FIGS. **14-17**.

In compliance with the statute, the subject matter disclosed herein has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the claims are not limited to the specific features shown and described, since the means herein disclosed comprise example embodiments. The claims are thus to be afforded full scope as literally worded, and to be appropriately interpreted in accordance with the doctrine of equivalents.

The invention claimed is:

1. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and

removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing.

2. The method of claim **1** wherein the operative and dummy structures comprise the same material.

3. The method of claim **2** wherein the operative and dummy structures comprise a plurality of the same materials.

4. The method of claim **3** wherein the same materials are arranged in the same lateral order relative one another in the operative and dummy structures.

5. The method of claim **2** wherein the operative and dummy structures consist essentially of the same material.

6. The method of claim **1** wherein the features comprise plates.

7. The method of claim **1** wherein the operative and dummy structures comprise programmable material.

8. The method of claim **1** wherein the operative and dummy structures comprise semiconductive material.

9. The method of claim **8** wherein the semiconductive material of the operative structures comprises interconnected channels of a plurality of vertically oriented transistors.

10. The method of claim **9** wherein interconnected channels are of vertically oriented charge storage transistors.

11. The method of claim **1** wherein the operative and dummy structures comprise conductive material.

12. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the plates in the end portion;

forming horizontally elongated openings through the structures to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of vertically extending portions of both the operative structures and the dummy structures; and

removing at least some sacrificial material that is elevationally between the lines in the primary and end portions laterally between the openings.

13. The method of claim **12** wherein the removing comprises etching of the sacrificial material selectively relative to material of the lines, the operative structures, and the dummy structures.

14. The method of claim **12** wherein the operative and dummy structures comprise hollow cylinders.

15. The method of claim **12** wherein the operative and dummy structures comprise laterally solid pillars.

16. The method of claim **12** wherein the features comprise plates.

17. A method of forming circuitry components, comprising:

forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;

forming primary portion openings through the features in the primary portion and forming end portion openings through the features in the in the end portion;

forming at least one of conductive material, semiconductive material, and programmable material in the primary portion openings and the end portion openings and forming operative structures therewith within the primary portion openings and forming dummy structures therewith within the end portion openings;

forming horizontally elongated openings through the features to form horizontally elongated and vertically overlapping lines from material of the features, the lines individually extending from the primary portion into the end portion and individually laterally about sides of both the operative structures and the dummy structures; and

removing at least a portion of sacrificial material that is elevationally between the lines in the primary and end portions laterally between the horizontally elongated openings selectively relative to the lines, the operative structures, and the dummy structures.

18. The method of claim **17** comprising forming the primary portion openings and the end portion openings at the same time.

19. The method of claim **17** comprising forming the primary portion openings and the end portion openings at different times.

20. The method of claim **17** comprising forming at least some of the end portion openings horizontally overlap ends of individual ones of the features.

21. The method of claim **17** comprising forming the primary portion openings and the end portion openings to have the same horizontal and vertical cross sections.

22. The method of claim **17** comprising forming the primary portion openings and the end portion openings to have at least one of different horizontal cross sections or different vertical cross sections.

23. The method of claim **17** wherein said at least one of conductive material, semiconductive material, and programmable material is deposited simultaneously into the primary portion openings and the end portion openings.

24. The method of claim **17** wherein the features comprise plates.

25. A method of forming an array of memory cells, comprising:

forming a stack of alternating dielectric material and sacrificial material, the stack comprising a primary portion and an end portion, the end portion having sacrificial material-comprising stairs;

forming a plurality of first openings into the primary portion of the stack;

forming a plurality of second openings into the end portion of the stack;

simultaneously forming at least one of conductive material, semiconductive material, and programmable material in the first and second openings and forming operative structures therewith within the first openings in the primary portion and forming dummy structures therewith within the second openings in the end portion;

forming horizontally elongated openings into the stack which extend from the primary portion into the end portion laterally between the material simultaneously formed to within the first and second openings;

removing at least a portion of the sacrificial material that is laterally between the horizontally elongated openings selectively relative to the dielectric material to form void spaces elevationally between vertically spaced horizontal lines of the dielectric material;

after the removing, forming conductive material into the horizontally elongated openings and the void spaces;

removing at least a portion of the conductive material from the horizontally elongated openings to form vertically spaced horizontal conductive lines from the conductive material within the void spaces elevationally between the horizontal lines of dielectric material, the conductive lines collectively crossing a row of the operative and dummy structures at different respective elevations, individual ones of the memory cells comprising an intersection of an individual horizontal conductive line and an individual operative structure; and

forming a respective communicative contact to a stair extension of individual ones of the horizontal conductive lines in the end portion.

26. The method of claim 25 wherein the memory cells comprise a portion of NAND architecture, the at least one formed material comprises semiconductive material, and the operative structures comprise interconnected channel regions of a NAND string.

27. The method of claim 25 wherein the memory cells comprise cross-point memory cells and the at least one formed material comprises programmable material.

28. The method of claim 25 comprising forming the first and second openings using the same masking step.

29. The method of claim 25 comprising forming the first and second openings using different masking steps.

30. The method of claim 25 wherein the sacrificial material is dielectric.

31. The method of claim 25 wherein the sacrificial material is at least one of semiconductive and conductive.

32. The method of claim 25 wherein the features comprise plates.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

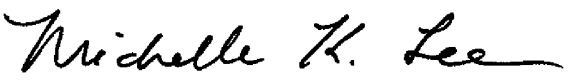
PATENT NO.	: 8,945,996 B2
APPLICATION NO.	: 13/085083
DATED	: February 3, 2015
INVENTOR(S)	: Sanh D. Tang et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In column 12, line 25, in Claim 17, delete “in the in the” and insert -- in the --, therefor.

Signed and Sealed this
Fifth Day of May, 2015



Michelle K. Lee
Director of the United States Patent and Trademark Office

Exhibit 4

REDACTED

EXHIBIT 4 (02/16/2024)

Micron's Exemplary Infringement Claim Chart for U.S. Patent No. 8,945,996

The following chart provides non-limiting examples, without the benefit of claim construction or discovery, of how YMTC's Accused Products (as that term is defined in the Complaint) meet every limitation, literally or under the doctrine of equivalents, of at least claim 1 of U.S. Patent No. 8,945,996, including by how said products made. The referenced images are images from a 232L YMTC 1Tb TLC part. Micron reserves the right to amend, correct, supplement, or otherwise change its explanation of how YMTC's Accused Products meet the following claim limitations, including as the claims are construed, as discovery progresses, or as Micron's investigation continues. Micron takes no position on claim interpretation or scope at this time.

Claim Language	YMTC's Accused Products
1. A method of forming circuitry components, comprising:[1]	YMTC practices "a method of forming circuitry components" that satisfies the subsequent claim limitations. Specifically, as shown below, YMTC manufactures the YMTC Accused Products to include, for example, an end portion, primary portion, dummy structures, and operative structures. REDACTED

[1] By providing this disclosure, Micron does not concede that the preamble is a claim limitation.

EXHIBIT 4 (02/16/2024)

	YMTC refers to such layers as forming a "stack." *See, e.g.*, U.S. Pat. No. 10,861,872 at Abstract ("stack").
forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion;	YMTC practices "forming a stack of horizontally extending and vertically overlapping features, the stack comprising a primary portion and an end portion, at least some of the features extending farther in the horizontal direction in the end portion moving deeper into the stack in the end portion." Specifically, as shown below, forms a stack of alternating gate layers and dielectric layers, which includes a primary portion and end portion. Further, as shown below, at least some of the features (word lines of the stack) extend farther in the horizontal direction in the end portion moving deeper into the stack (e.g., towards the substrate): REDACTED YMTC describes that the word lines extend further in the end portion, which it refers to as the "staircase region," then the primary portion, which it refers to as the "core array region." *See, e.g.*, U.S. Pat. No. 10,861,872 at 6:14-25, Figure 1D.
forming operative structures vertically	YMTC practices "forming operative structures vertically through the features in the primary portion and forming dummy structures vertically through the features in the end portion." Specifically, as shown below, the primary portion includes memory strings that are vertically operative structures including memory cells, and

EXHIBIT 4 (02/16/2024)

through the features in the primary portion and forming dummy structures vertically through the features in the end portion; and	these structures extend through the word line features. Further, as shown below, the end portion includes dummy structures: REDACTED YMTC describes that the primary portion, which it refers to as the "core array region," includes these vertical memory strings. *See, e.g.*, U.S. Pat. No. 10,861,872 at 6:14-30, Figure 1A. YMTC describes that the end portion, which it refers to as the "staircase region," includes "dummy channel structures." *See, e.g.*, U.S. Pat. No. 10,861,872 at 6:31-50.
removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures	YMTC practices "removing at least some sacrificial material that is elevationally between material of the features in the primary and end portions, wherein the dummy structures support material of the features from vertical movement in the end portion during said removing." Specifically, as shown below, YMTC employs depositing sacrificial gate layers that it later removes and replaces with functional gate layers, aka, access line ("features") and employs dummy structures to prevent movement of the stack layers:

EXHIBIT 4 (02/16/2024)

support material of the features from vertical movement in the end portion during said removing.	REDACTED YMTC describes replacing the sacrificial gate layer after forming the dummy channel supporting structures. *See, e.g.*, U.S. Pat. No. 10,861,872 at 2:8-18.

Exhibit 5

US008803214B2

(12) **United States Patent**
Tang et al.

(10) **Patent No.: US 8,803,214 B2**
(45) **Date of Patent: Aug. 12, 2014**

(54) **THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME**

(75) Inventors: **Sanh D. Tang**, Boise, ID (US); **John K. Zahurak**, Eagle, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 312 days.

(21) Appl. No.: **12/825,211**

(22) Filed: **Jun. 28, 2010**

(65) **Prior Publication Data**

US 2011/0316063 A1 Dec. 29, 2011

(51) **Int. Cl.**

H01L 27/06	(2006.01)
H01L 27/10	(2006.01)
H01L 27/115	(2006.01)
H01L 29/66	(2006.01)

(52) **U.S. Cl.**
USPC **257/314**; 257/316; 365/185.26

(58) **Field of Classification Search**
USPC 257/314, E21.602, E29.255, E21.001; 438/128, 309; 365/189.11
See application file for complete search history.

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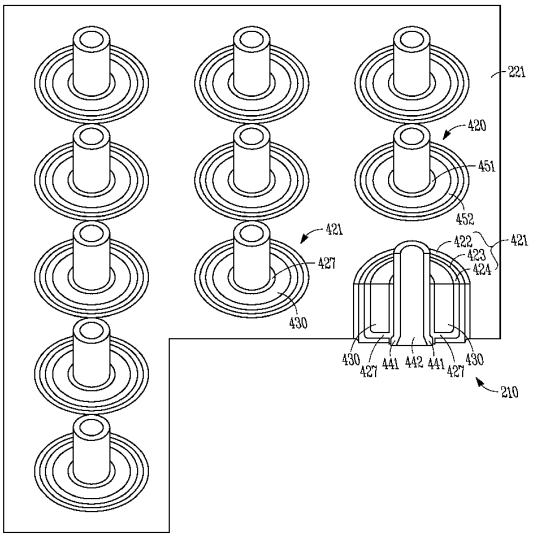
* cited by examiner

Primary Examiner — Olik Chaudhur
Assistant Examiner — Wilner Jean Baptiste
(74) *Attorney, Agent, or Firm* — Schwegman, Lundberg & Woessner, P.A.

(57) **ABSTRACT**

Some embodiments include a memory device and methods of forming the memory device. One such memory device includes a first group of memory cells, each of the memory cells of the first group being formed in a cavity of a first control gate located in one device level of the memory device. The memory device also includes a second group of memory cells, each of the memory cells of the second group being formed in a cavity of a second control gate located in another device level of the memory device. Additional apparatus and methods are described.

21 Claims, 38 Drawing Sheets



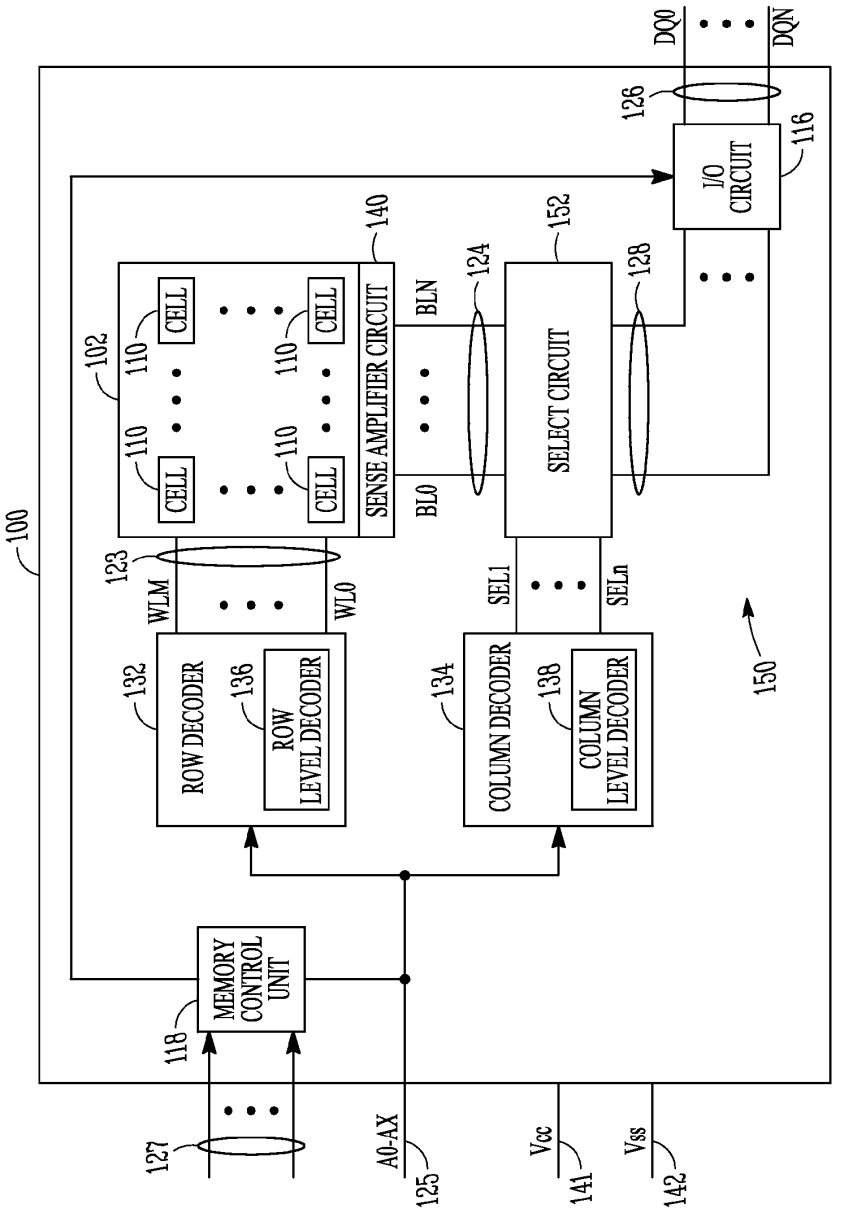

100
102
110
CELL
123
WLM
WL0
132
ROW DECODER
136
ROW LEVEL DECODER
140
SENSE AMPLIFIER CIRCUIT
BLN
BL0
124
152
SELECT CIRCUIT
128
126
DQ0
DQN
116
I/O CIRCUIT
SEL1
SELn
134
COLUMN DECODER
138
COLUMN LEVEL DECODER
150
118
MEMORY CONTROL UNIT
127
A0-AX
125
Vcc
141
Vss
142

FIG. 1

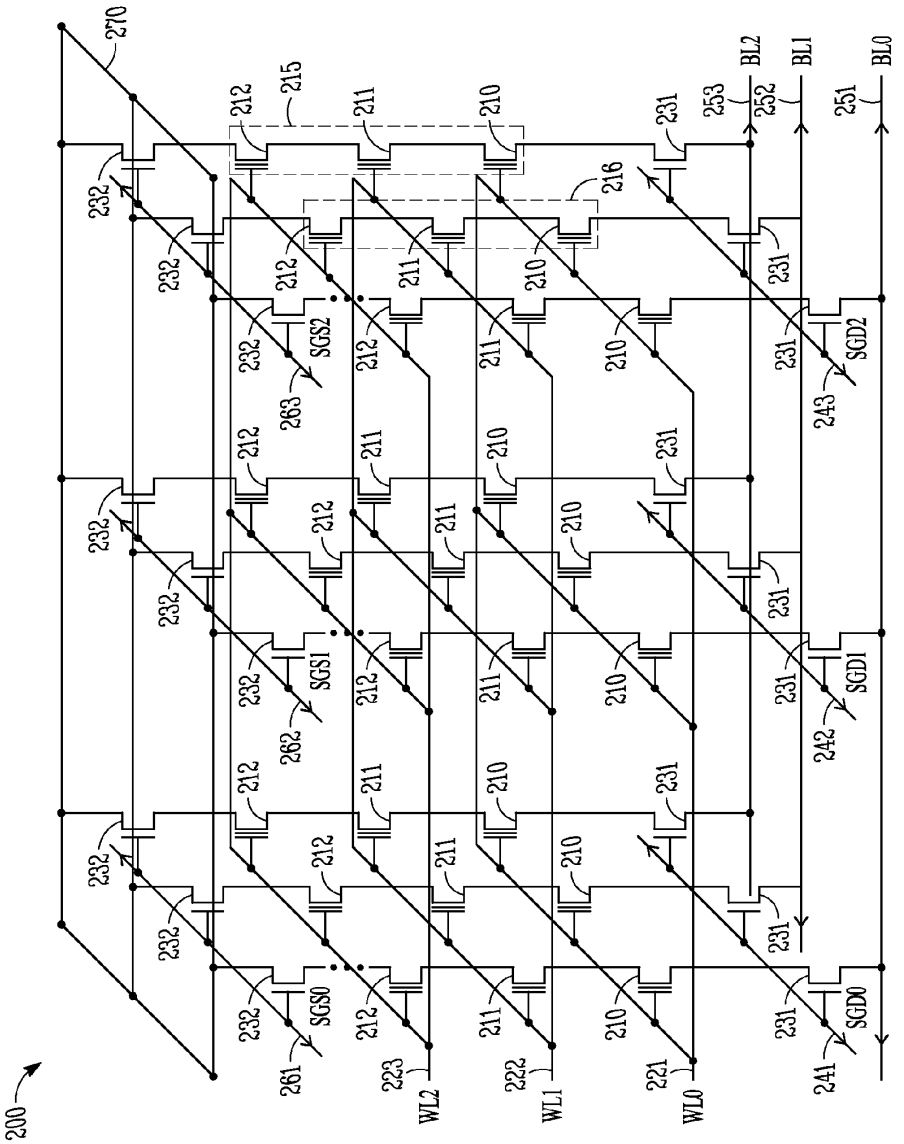

200
270
215
212
211
210
216
231
253
252
251
BL2
BL1
BL0
232
SGS2
SGS1
SGS0
SGD2
SGD1
SGD0
263
262
261
243
242
241
223
222
221
WL2
WL1
WL0

FIG. 2

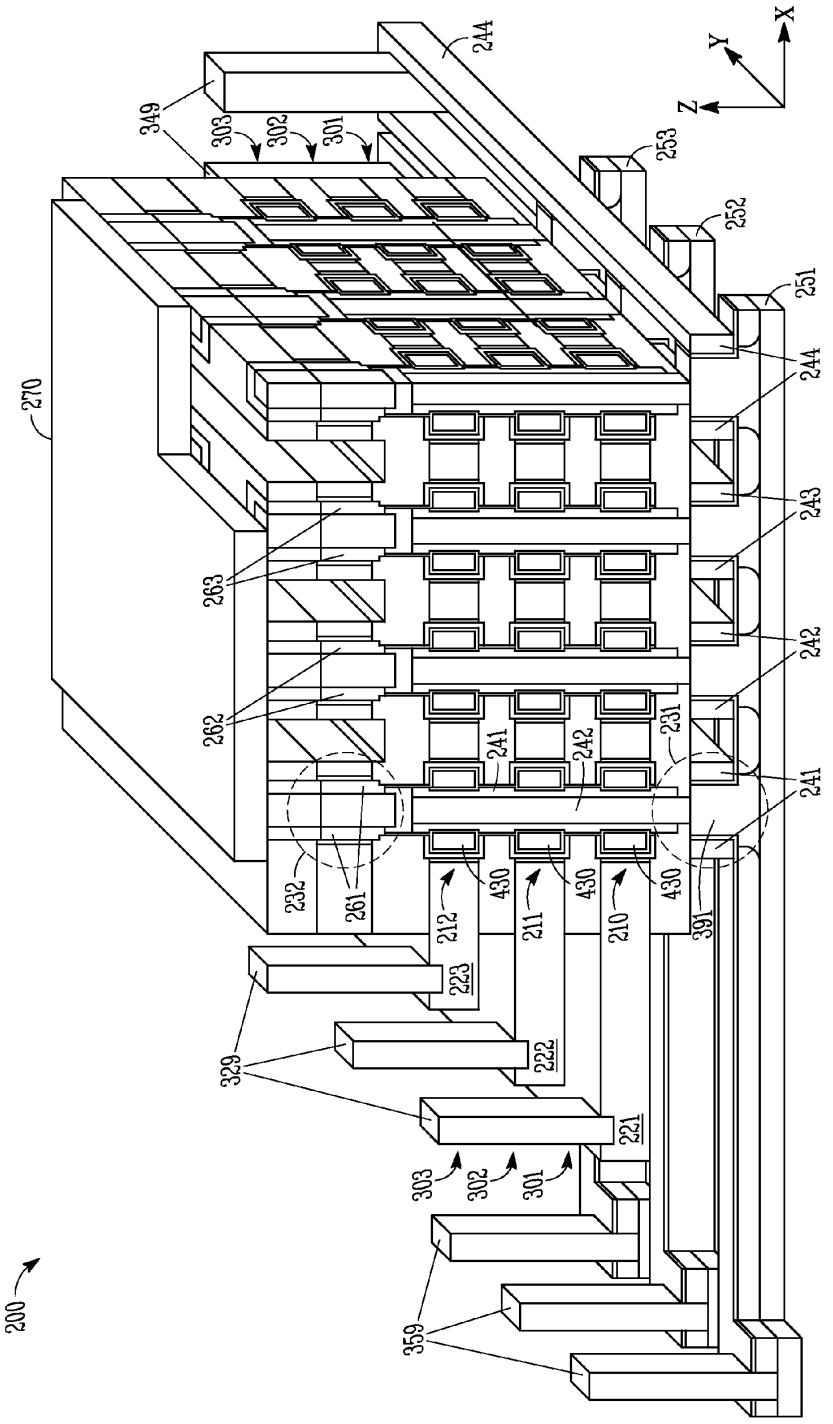

X
Y
Z
244
349
303
302
301
253
252
251
270
263
262
241
242
231
232
261
430
212
211
210
391
223
222
221
329
359
200

FIG. 3

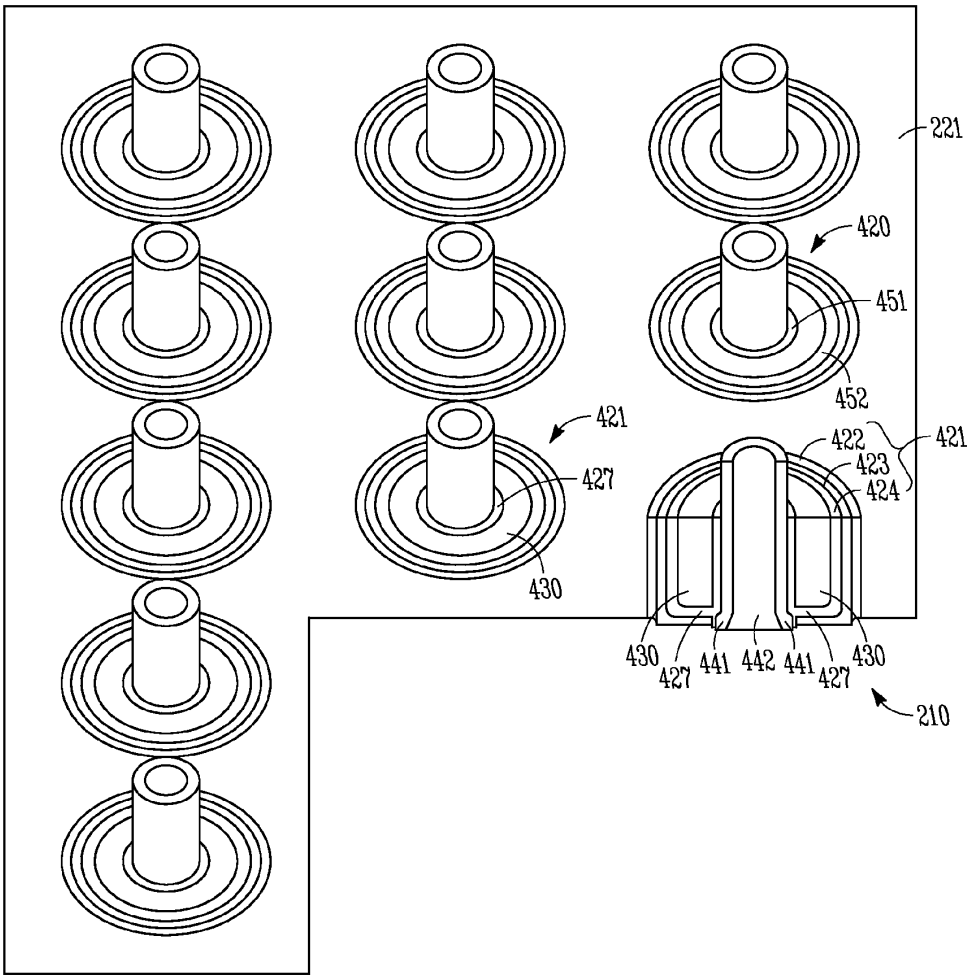

221
420
451
452
421
422
423
424
421
427
430
430
427
441
442
441
427
430
210

FIG. 4

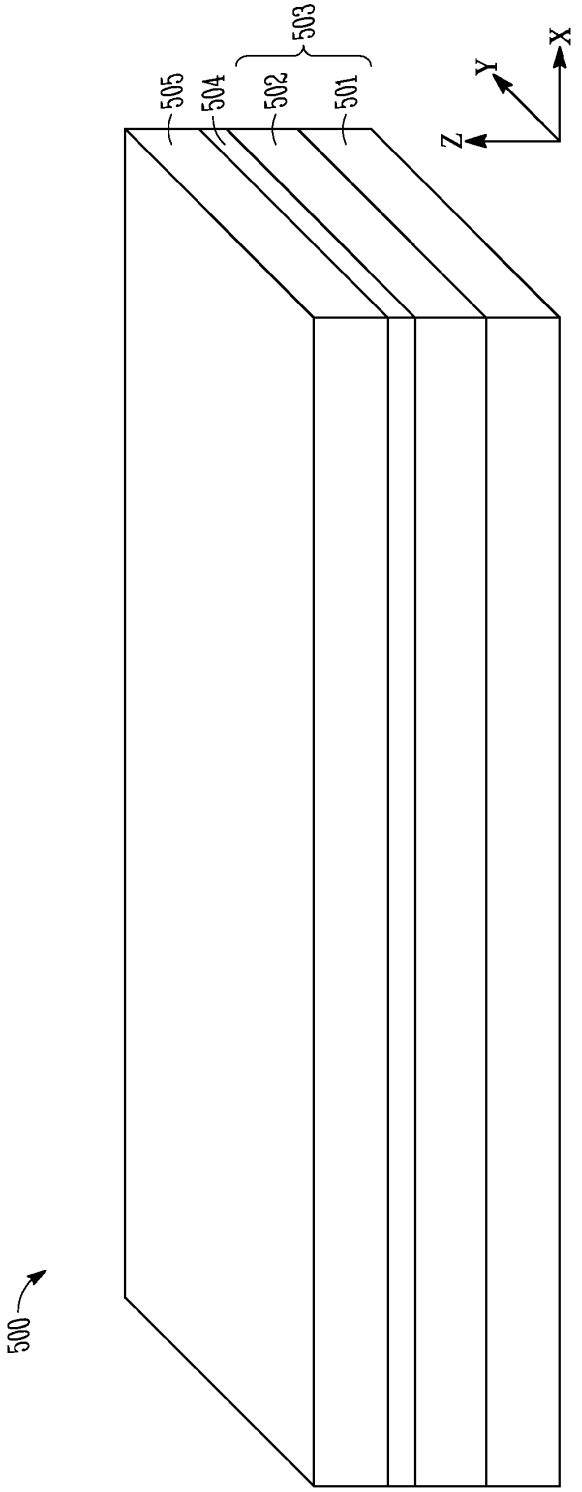


FIG. 5

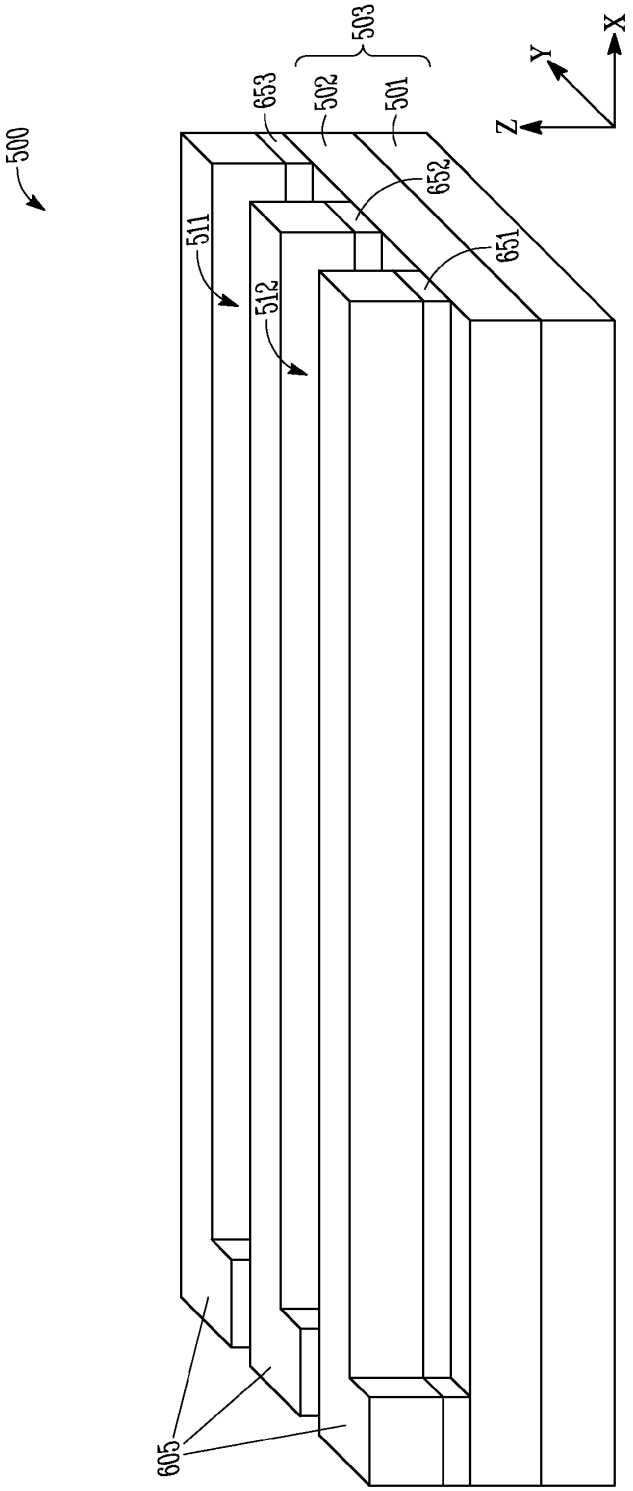


FIG. 6

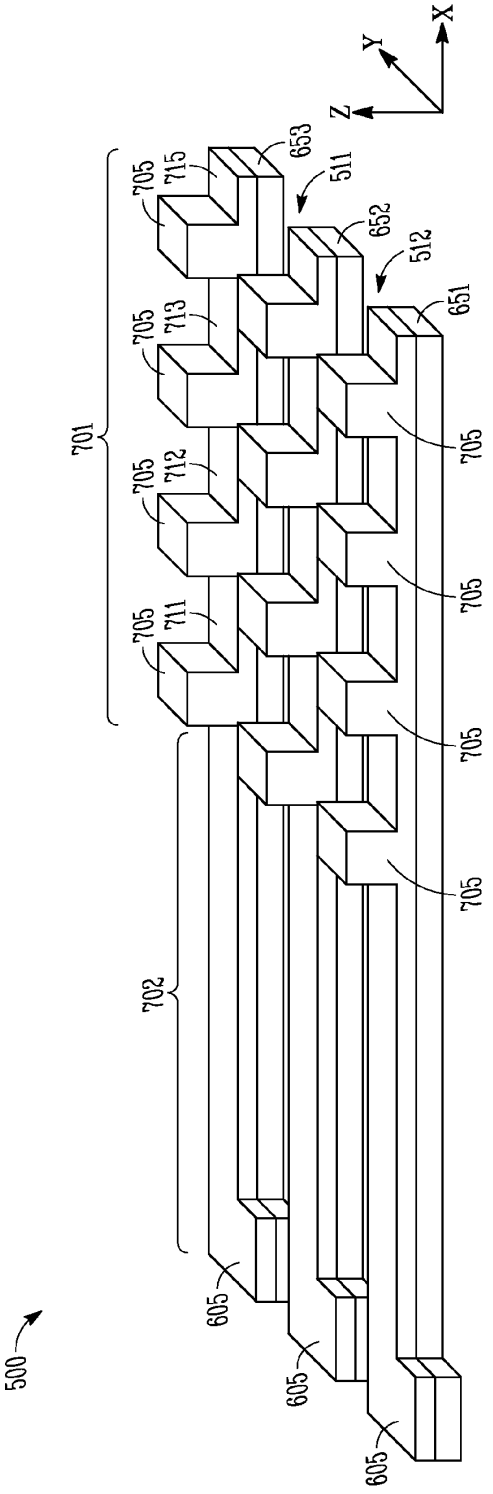


FIG. 7

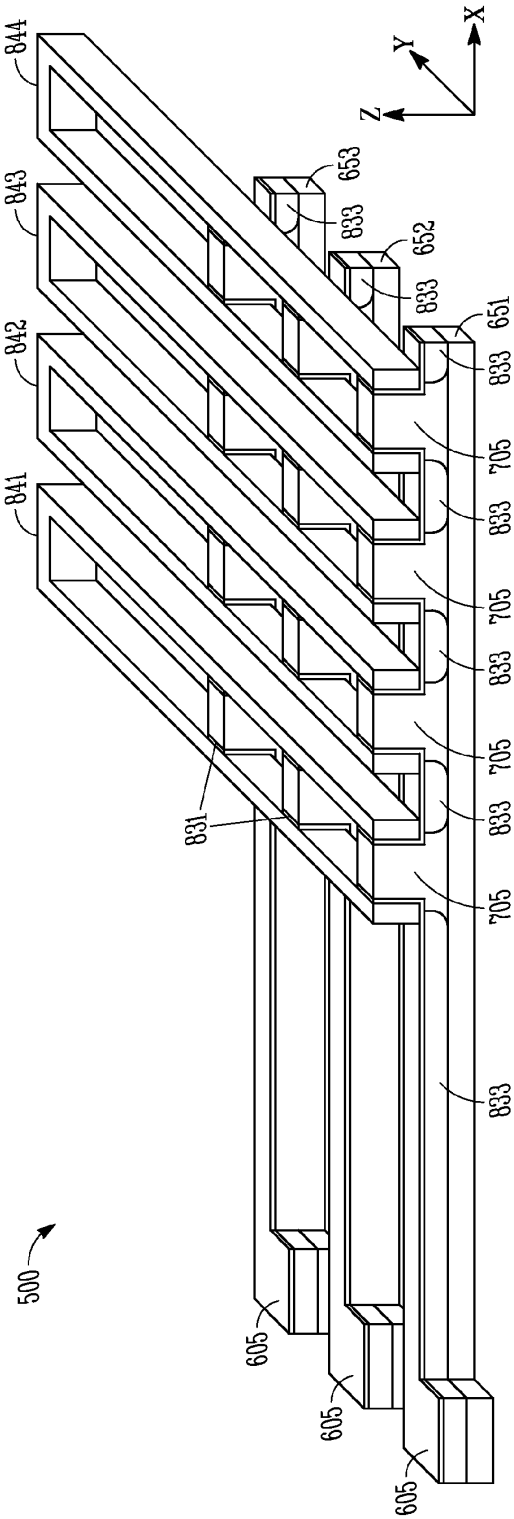


FIG. 8

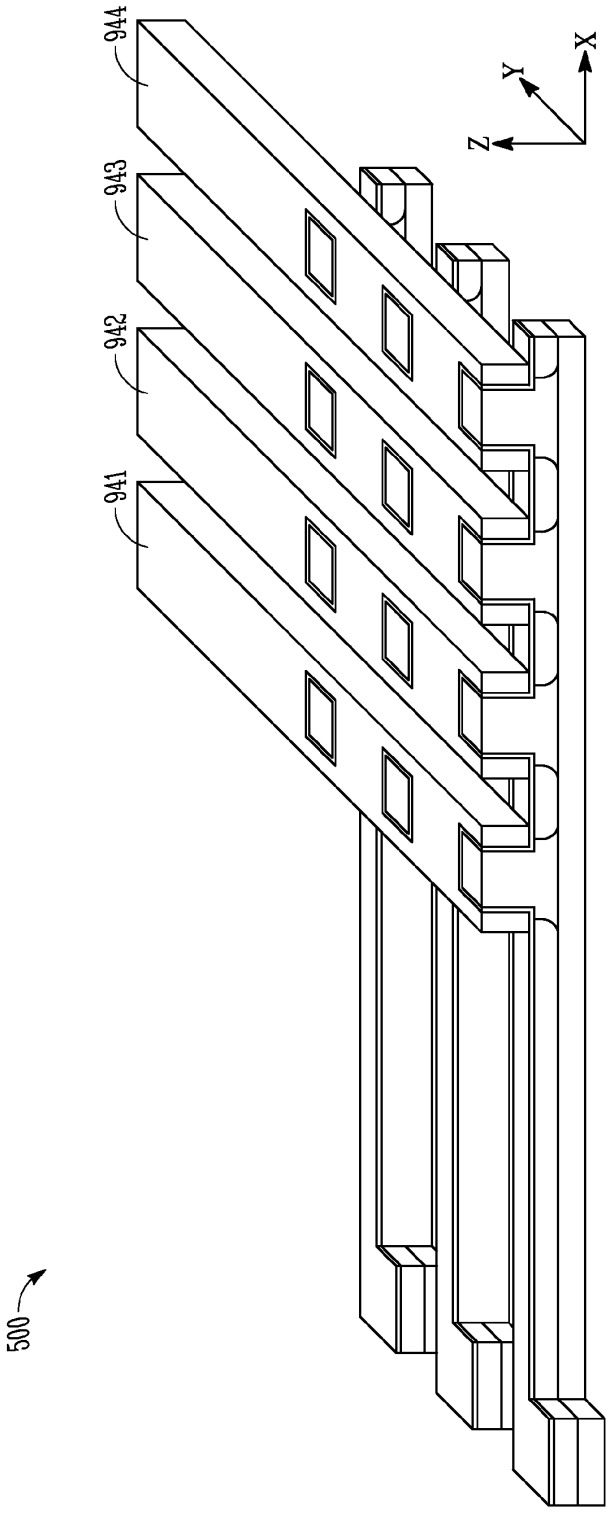


FIG. 9

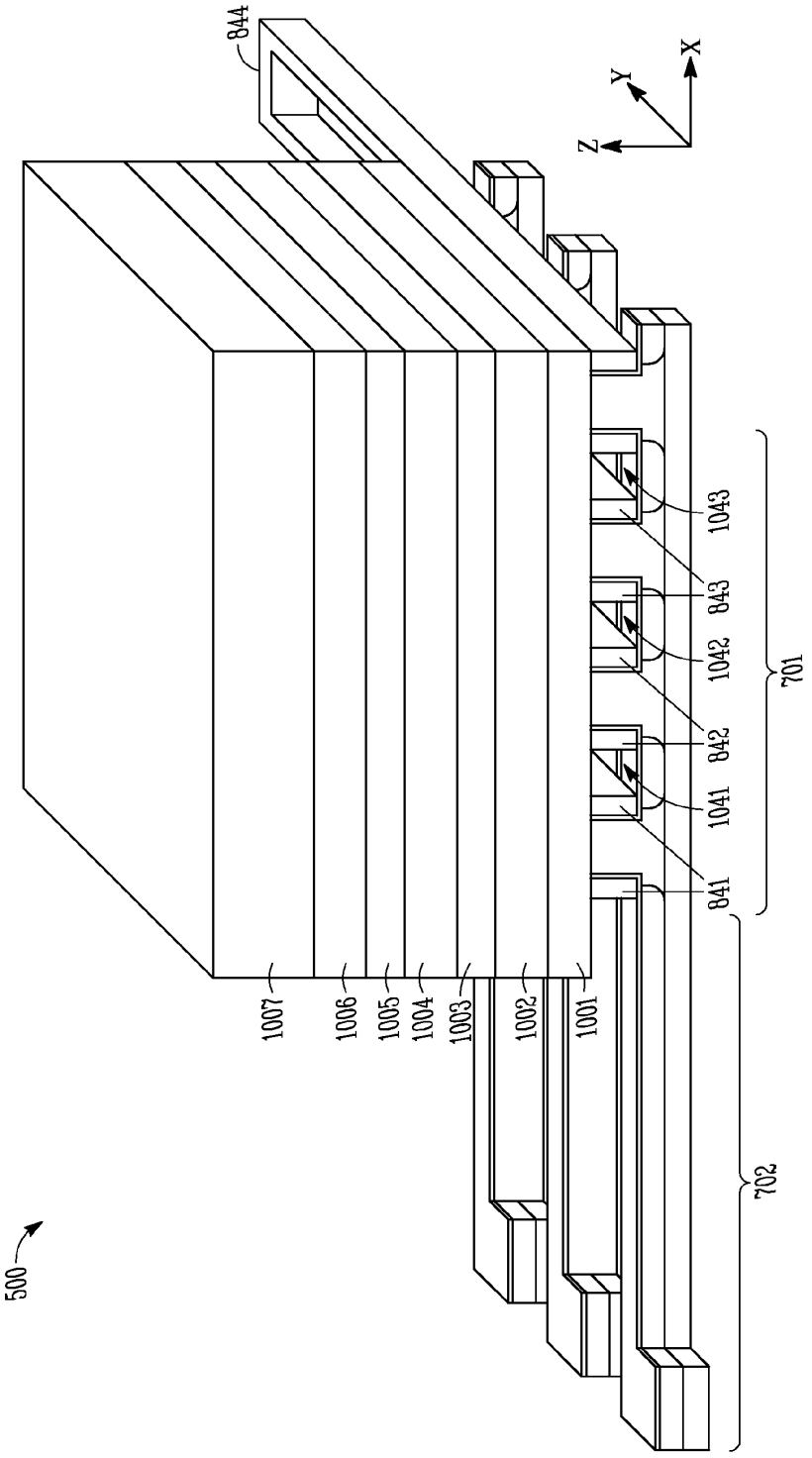

844
Y
X
Z
1043
843
1042
842
1041
841
701
1007
1006
1005
1004
1003
1002
1001
702
500

FIG. 10

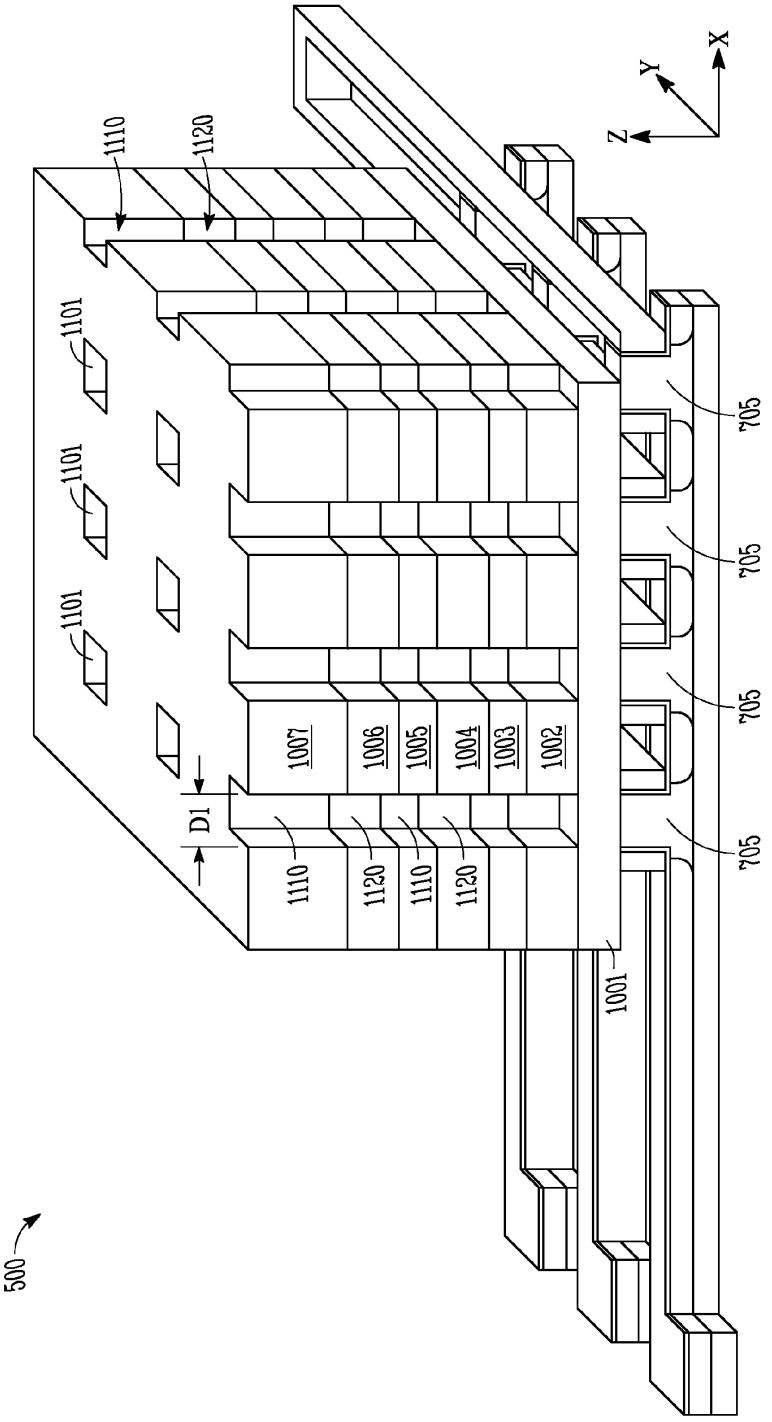

Y
X
Z
1110
1120
1101
1101
1101
705
705
705
705
1007
1006
1005
1004
1003
1002
D1
1110
1120
1110
1120
1001
500

FIG. 11

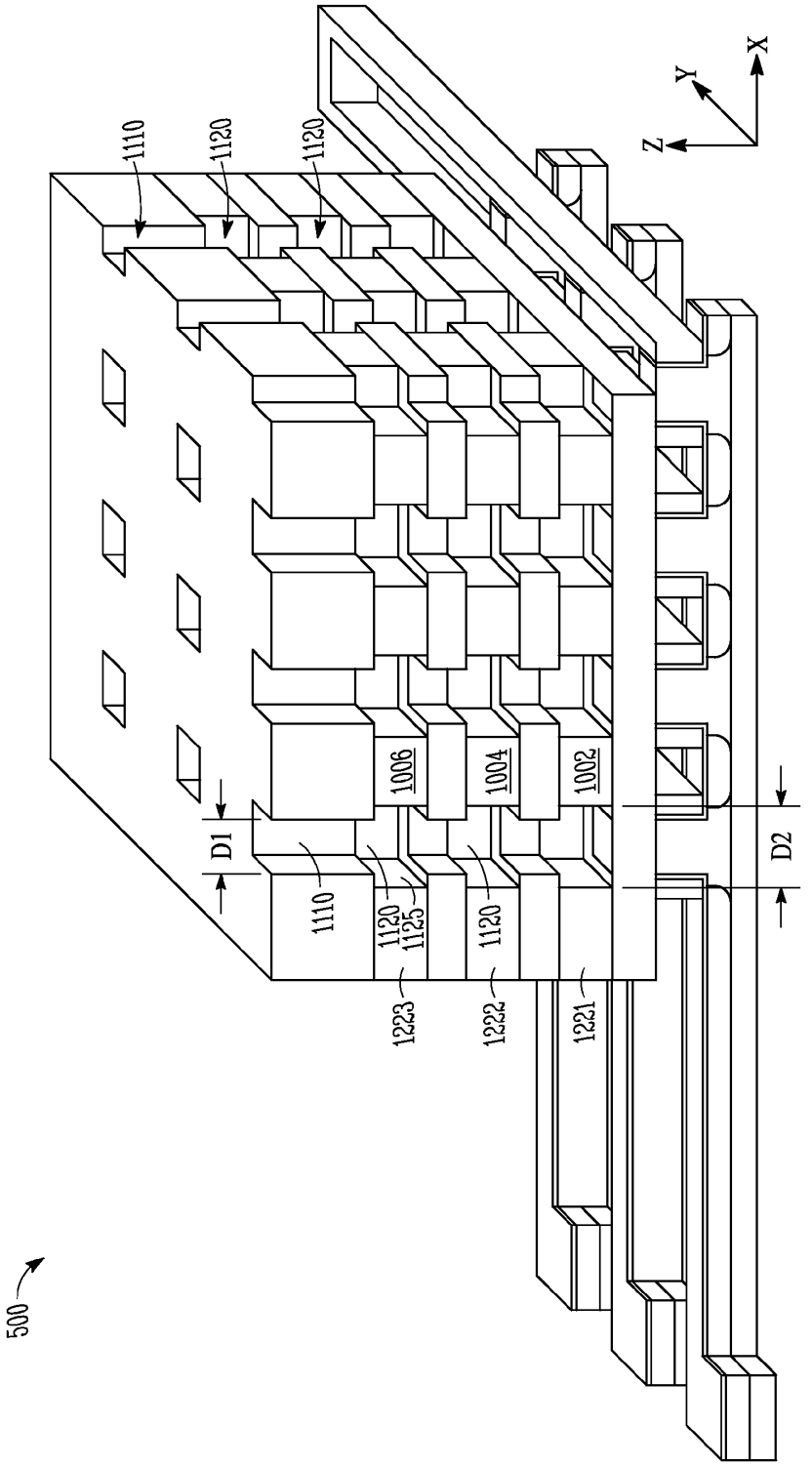

X
Y
Z
1110
1120
1120
1006
1004
1002
D1
D2
1110
1120
1125
1120
1223
1222
1221
500

FIG. 12

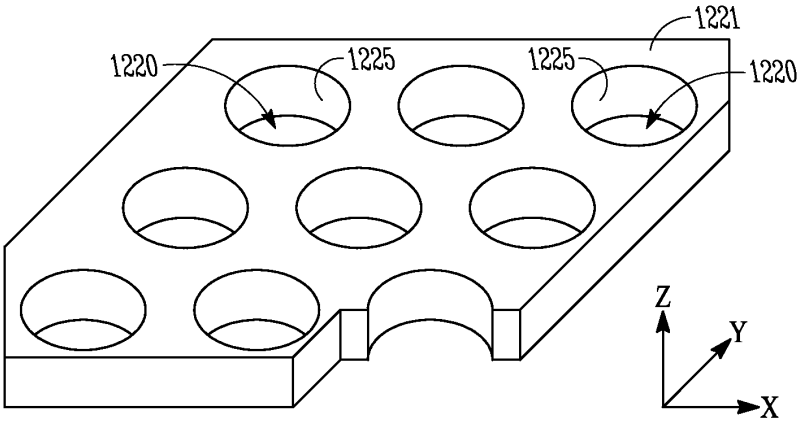


FIG. 13

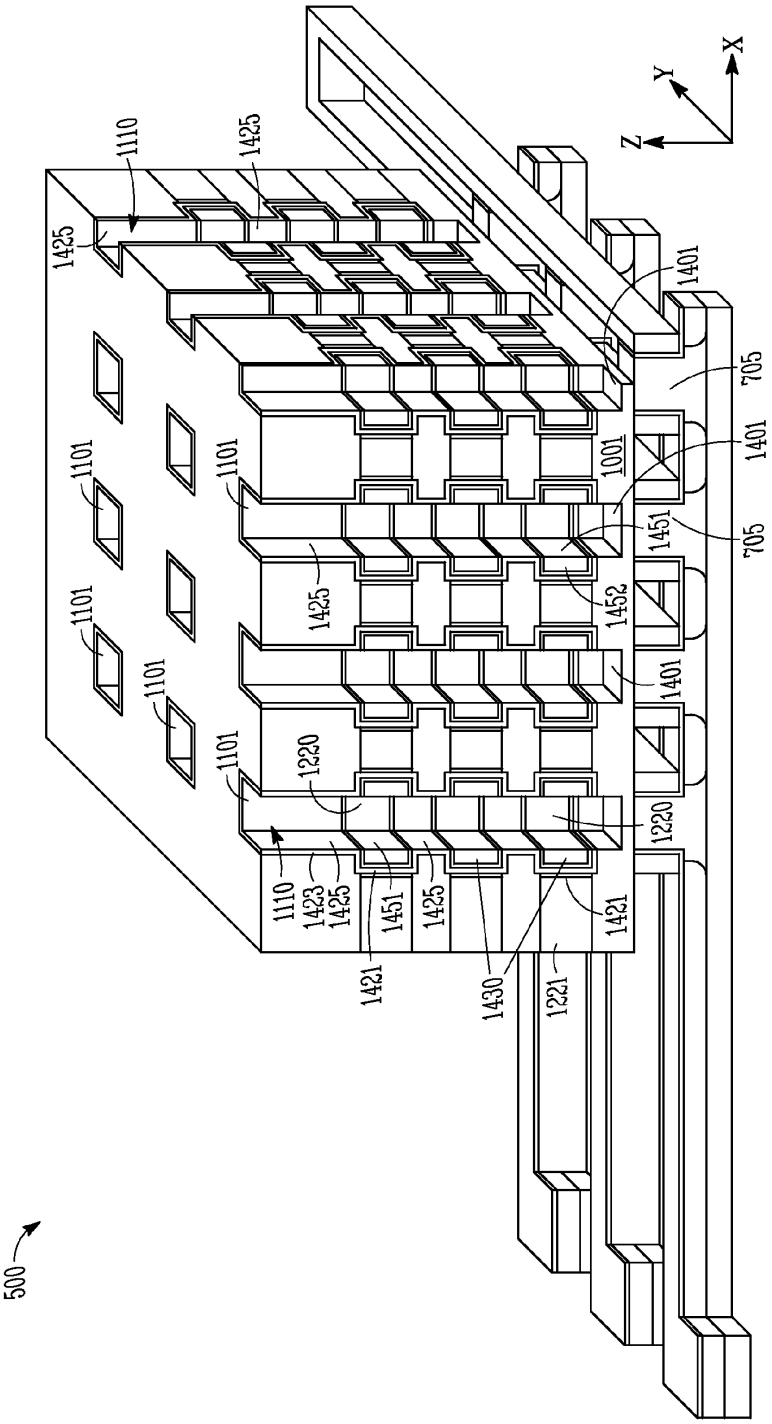

X
Y
Z
1110
1425
1401
705
1001
1451
1452
1101
1220
1423
1421
1430
1221
500

FIG. 14

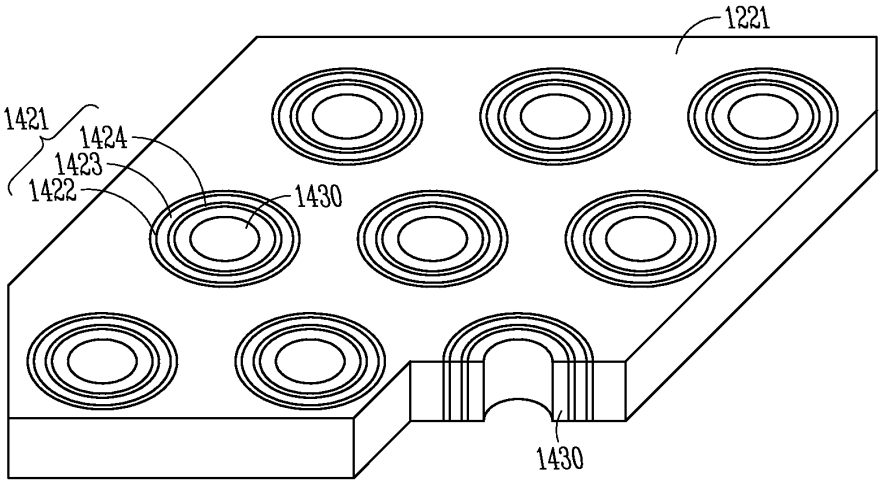


FIG. 15

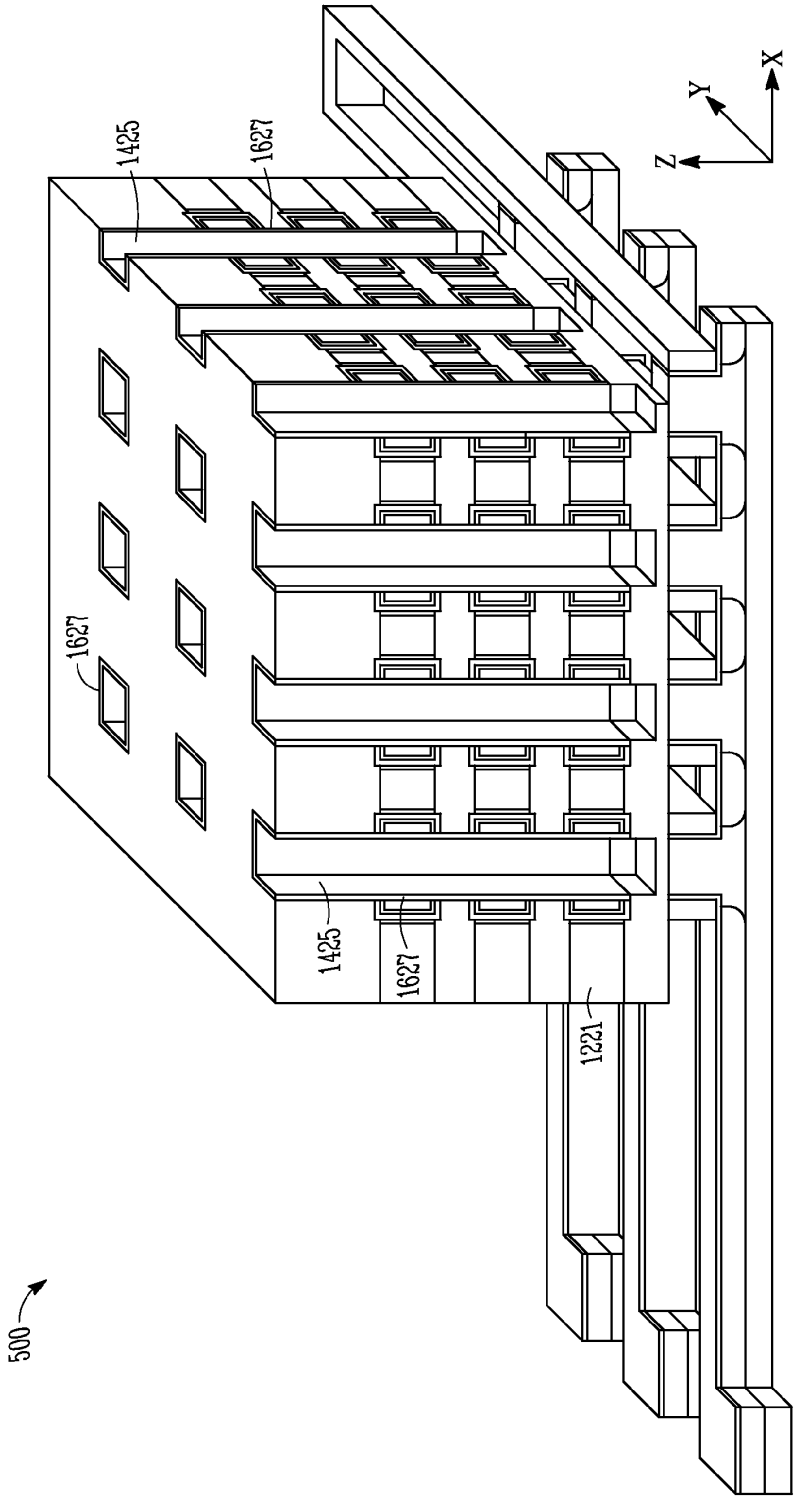


FIG. 16

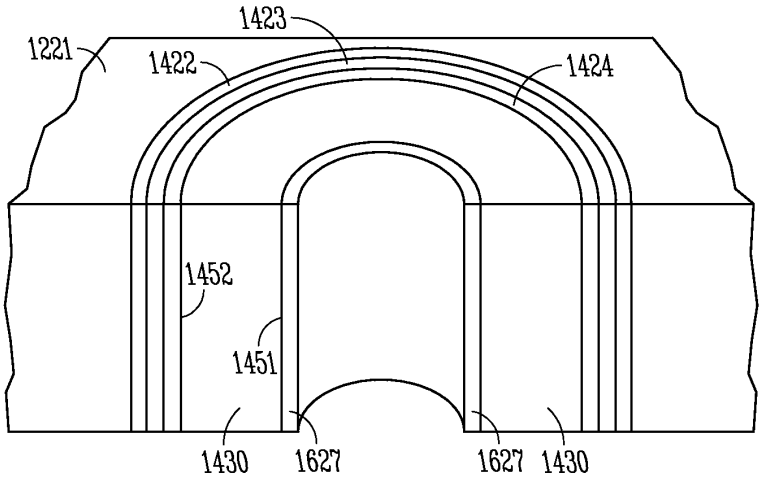


FIG. 17

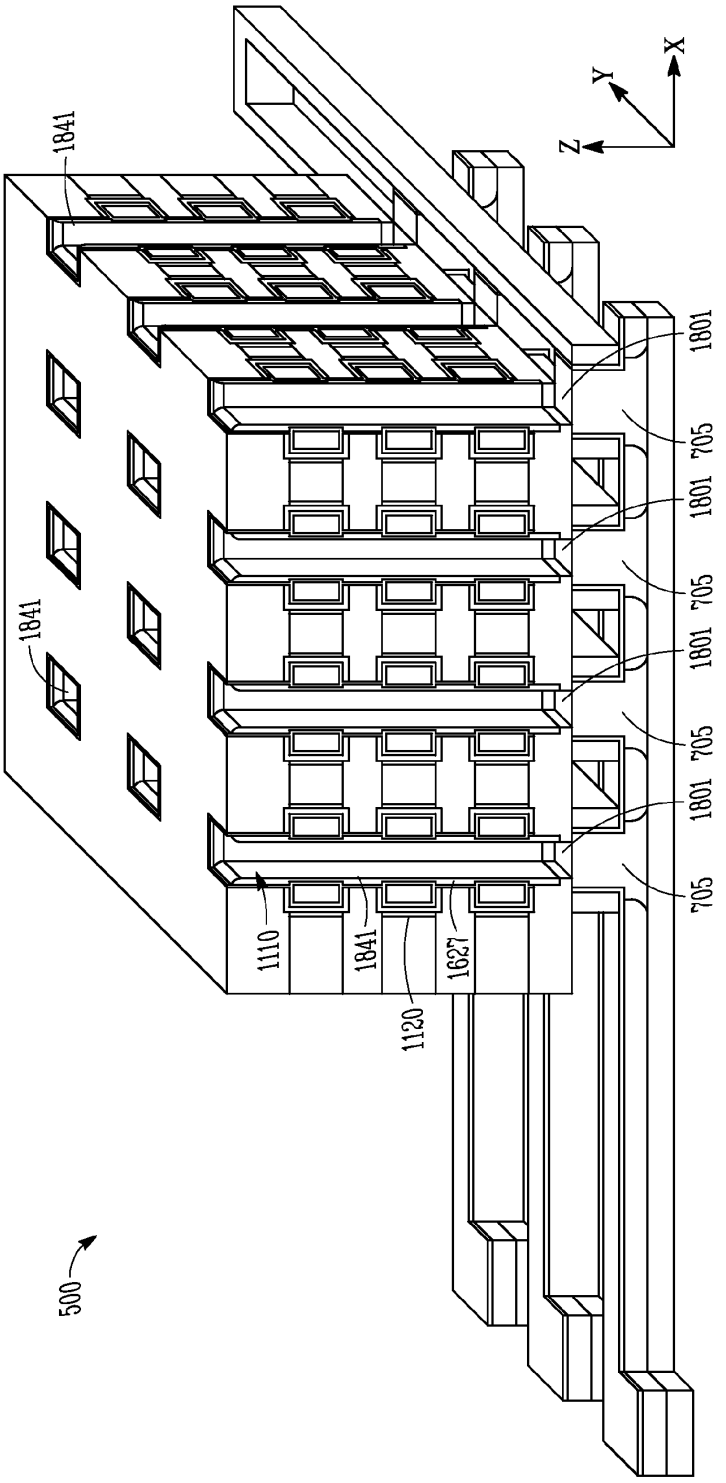

Y
X
Z
1841
1801
705
1801
705
1801
705
1801
705
1841
1110
1841
1627
1120
500

FIG. 18

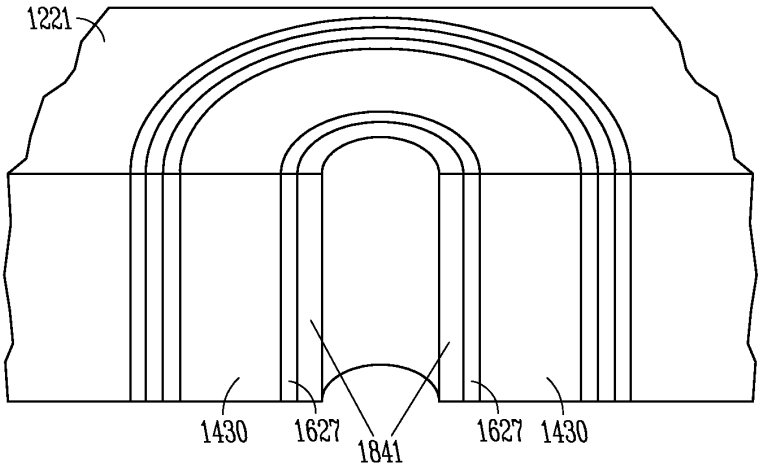


FIG. 19

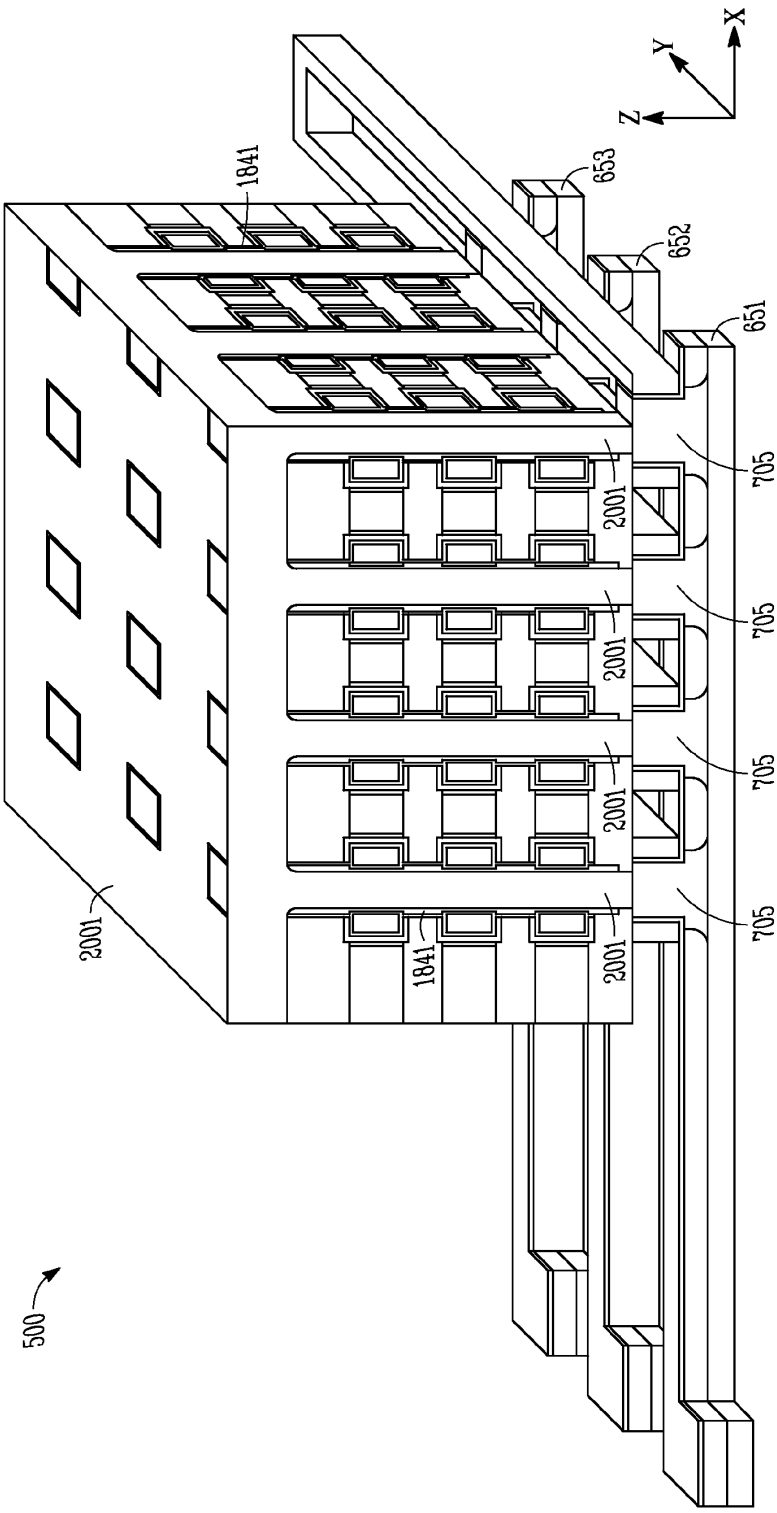


FIG. 20

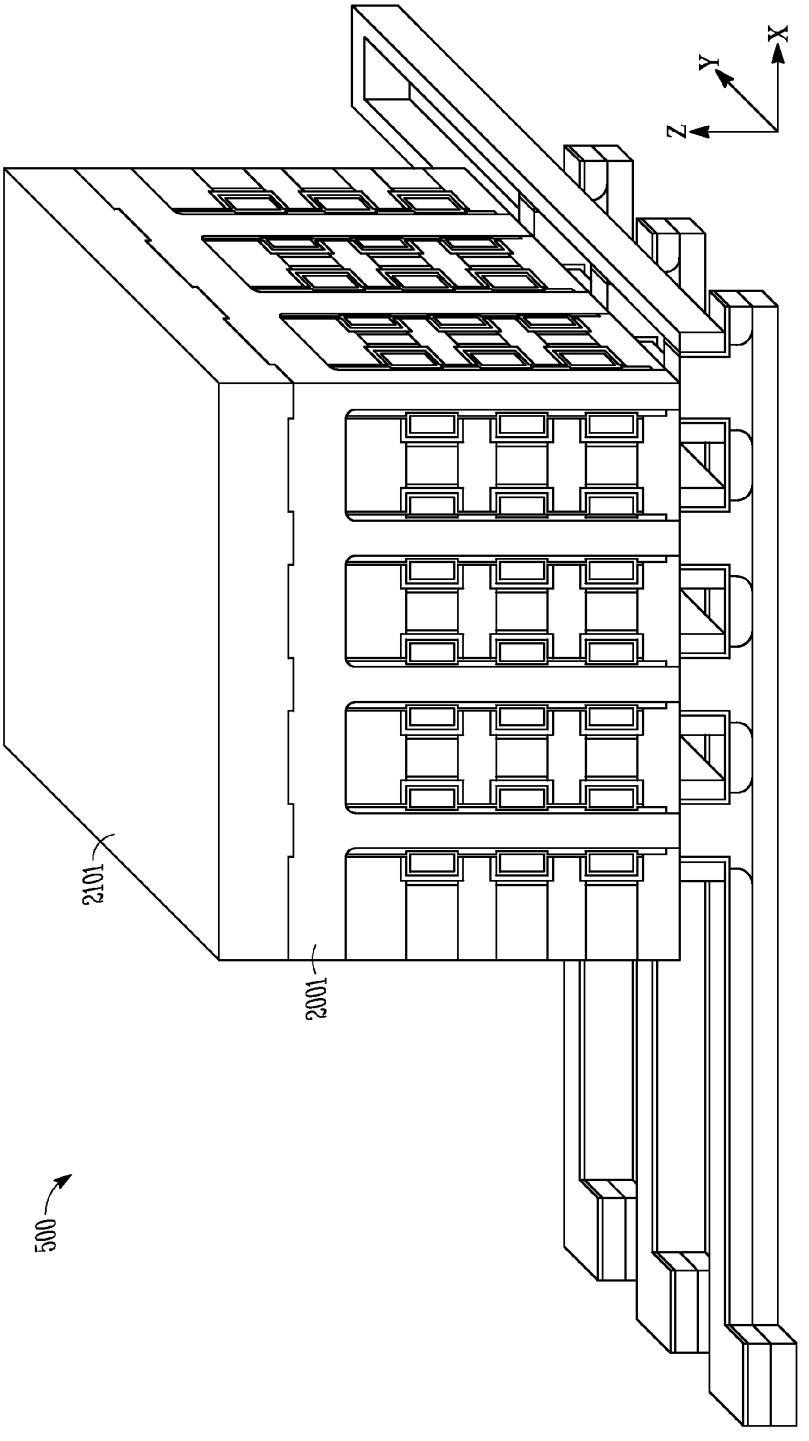


FIG. 21

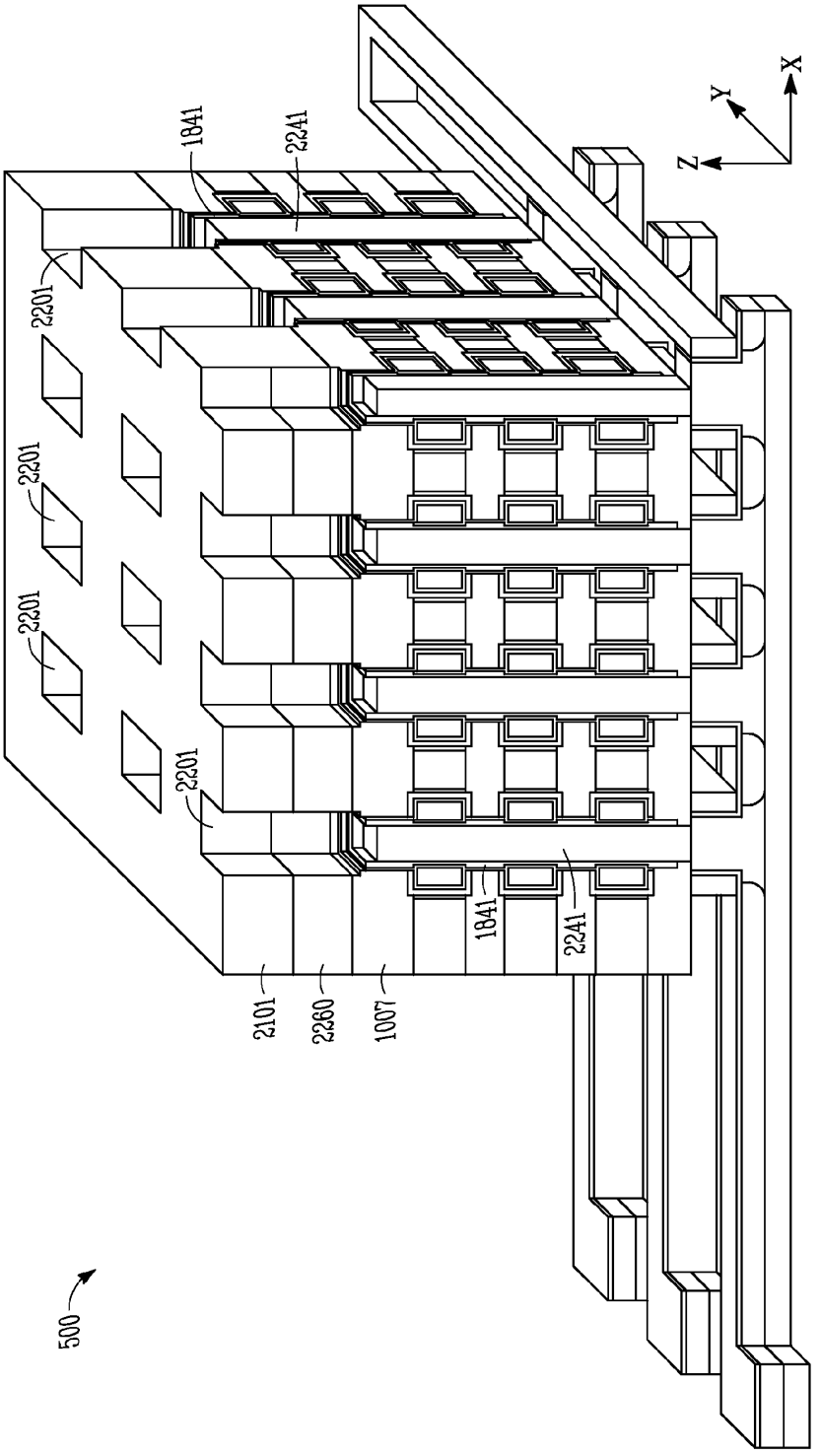

1841
2241
2201
2201
2201
2201
1841
2241
2101
2260
1007
500
Z
Y
X

FIG. 22

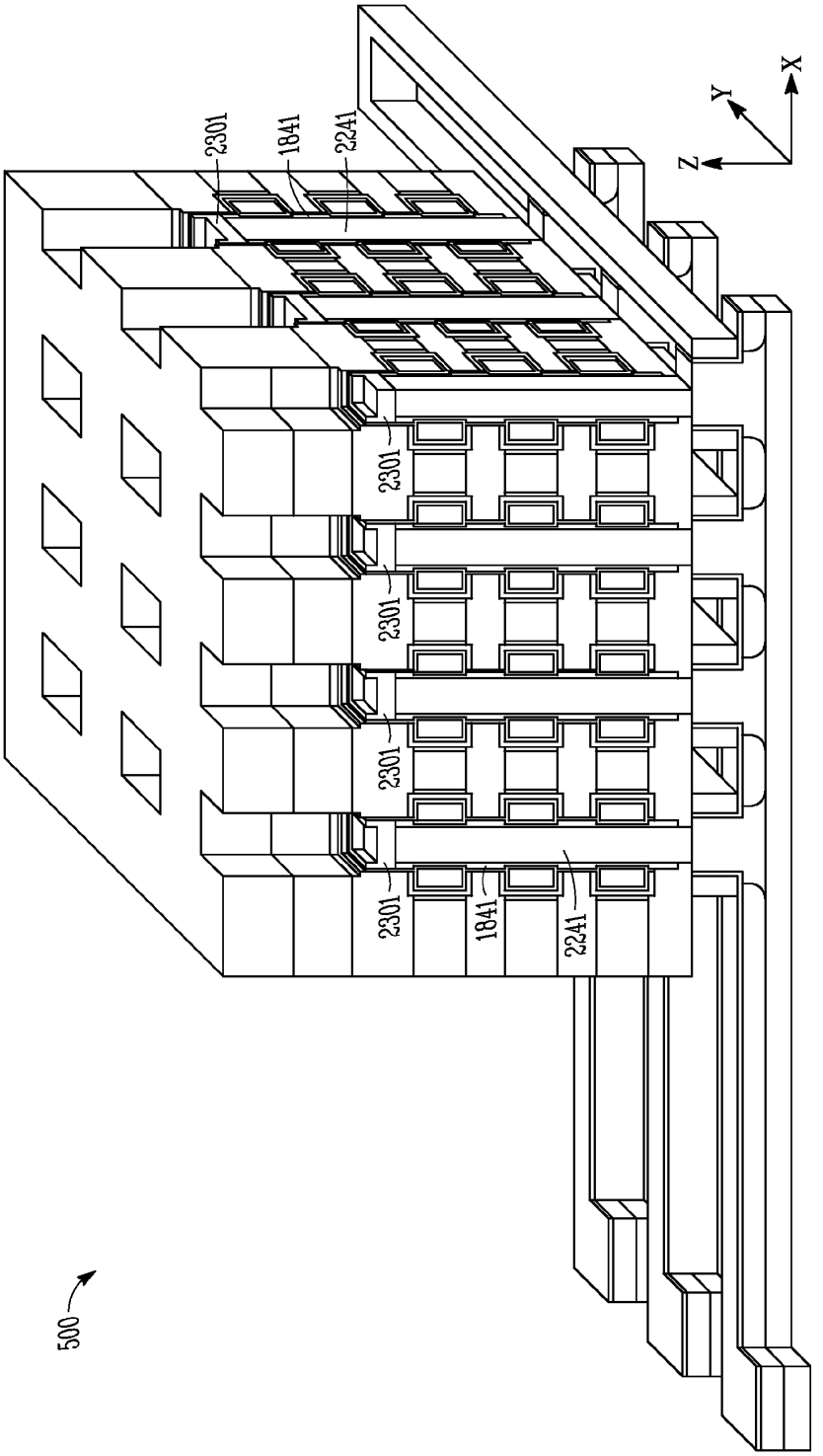


FIG. 23

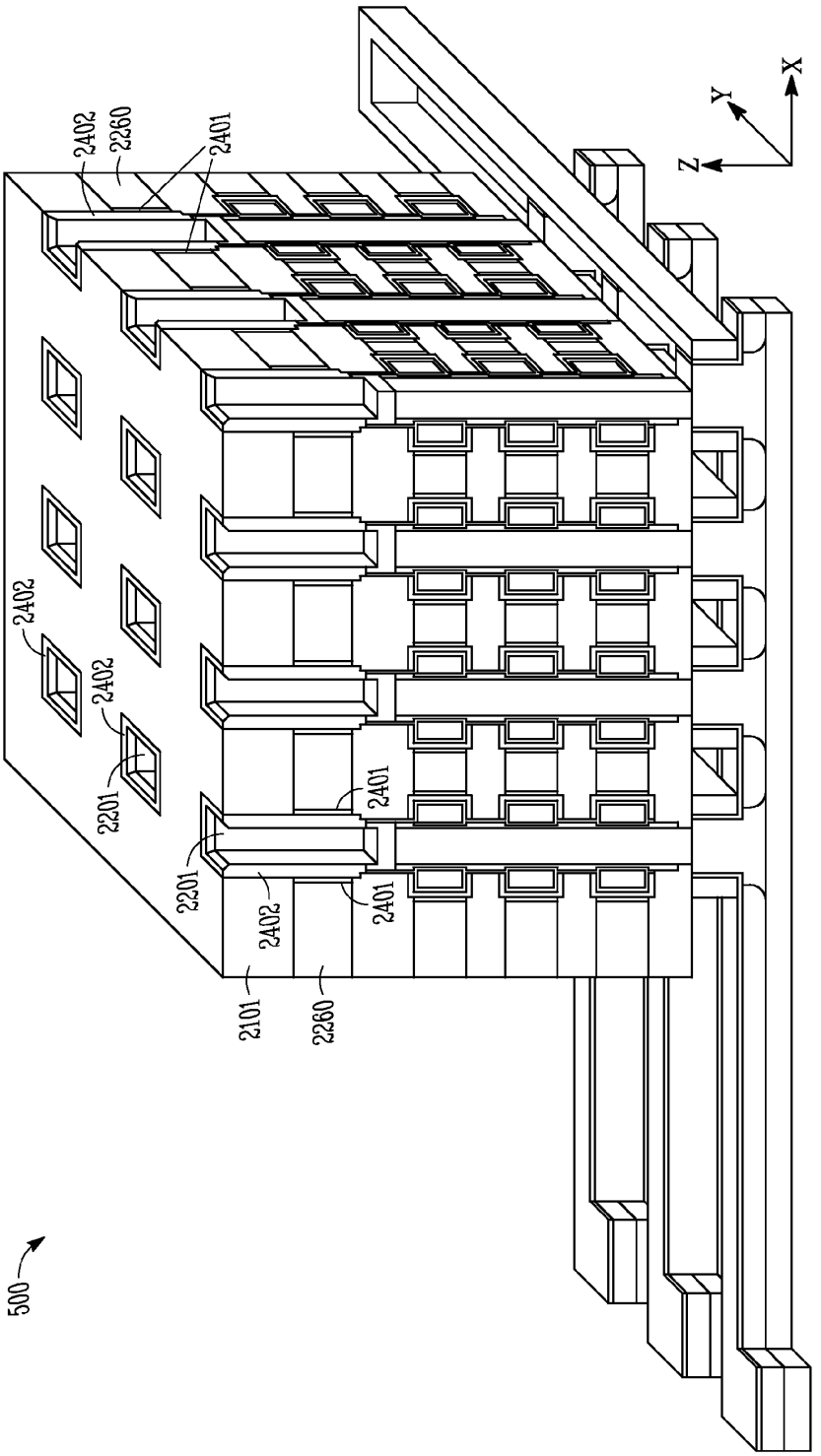

2402
2260
2401
Y
X
Z
2402
2402
2201
2401
2201
2402
2401
2101
2260
500

FIG. 24

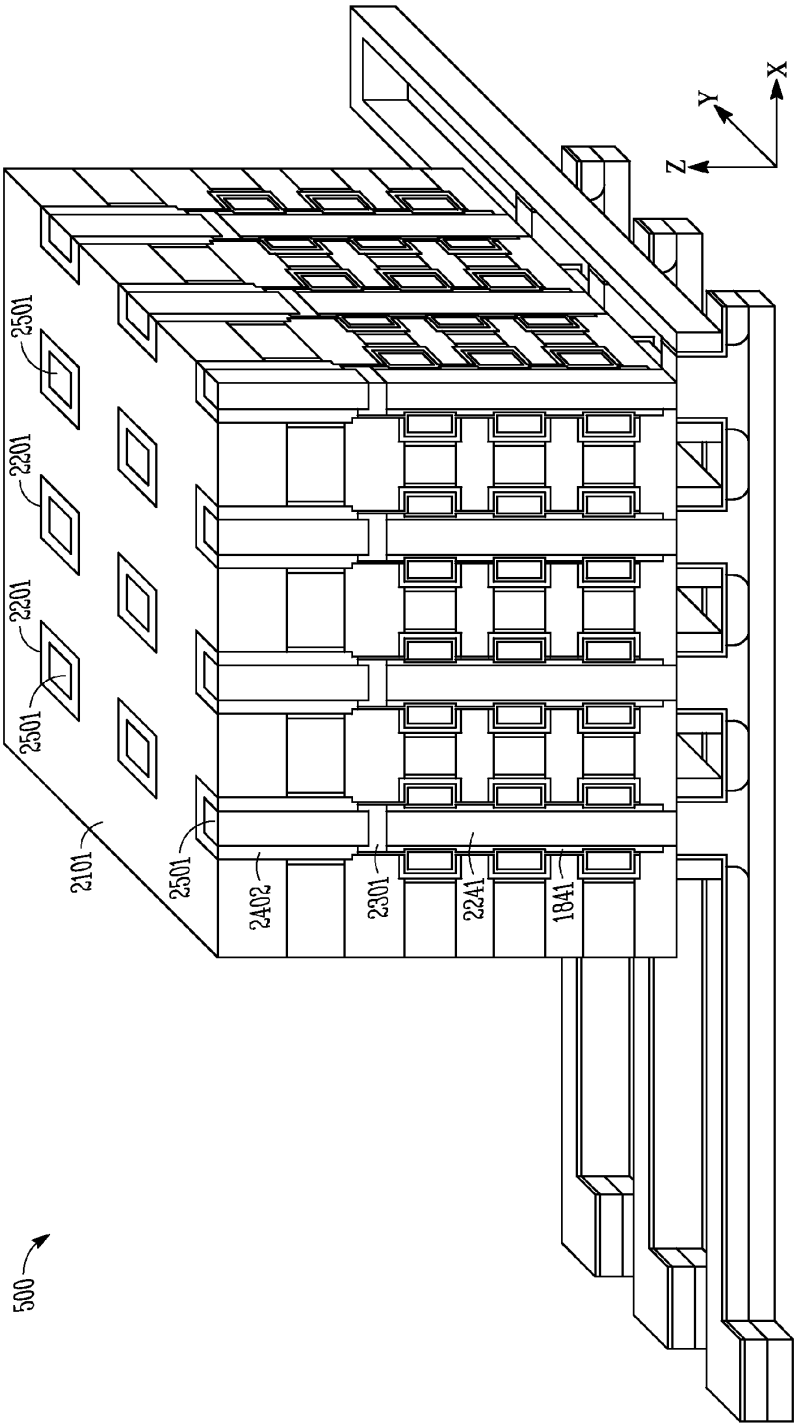


FIG. 25

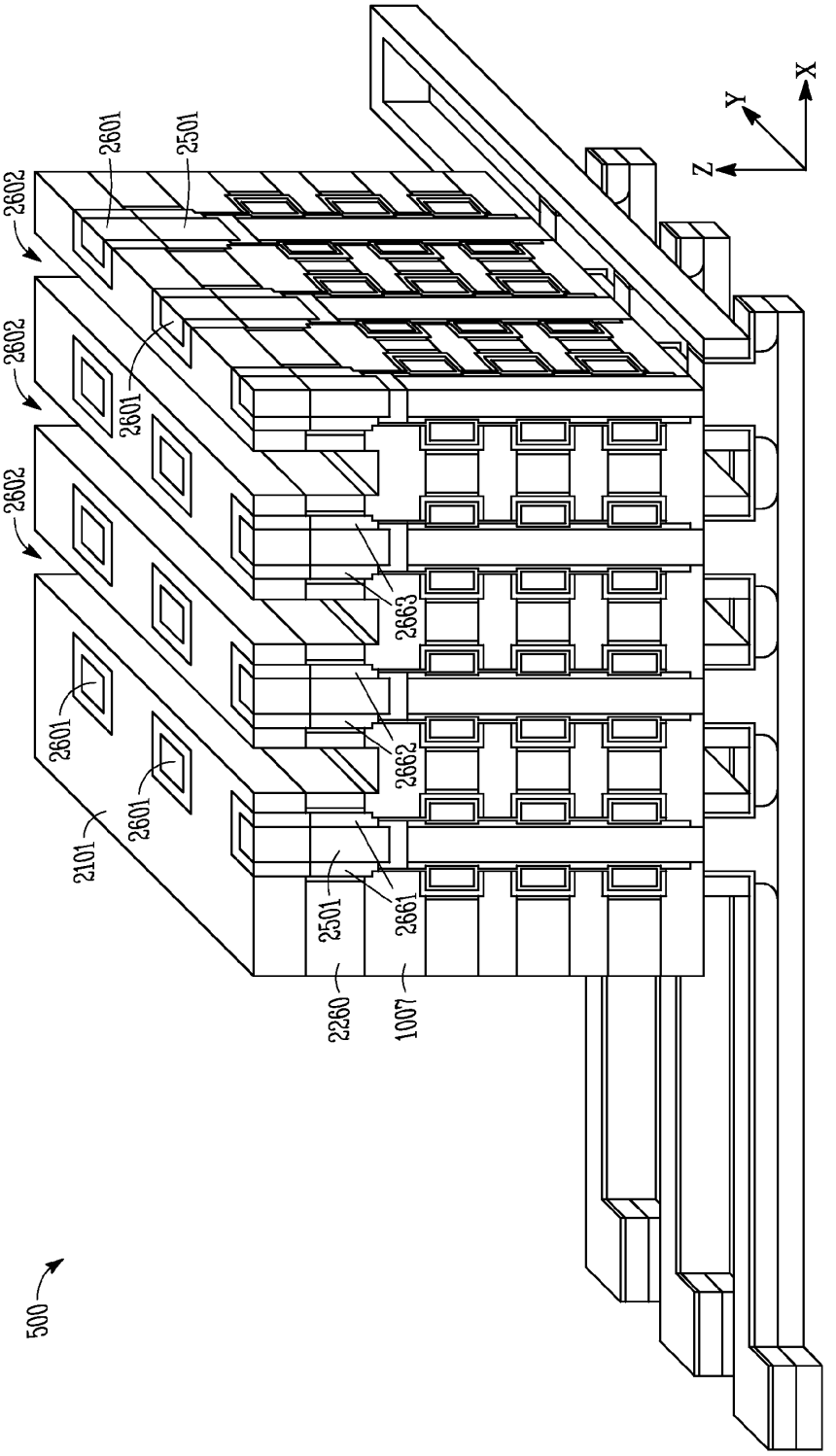

Y
X
Z
2601
2501
2602
2602
2602
2601
2663
2601
2662
2601
2101
2501
2661
2260
1007
500

FIG. 26

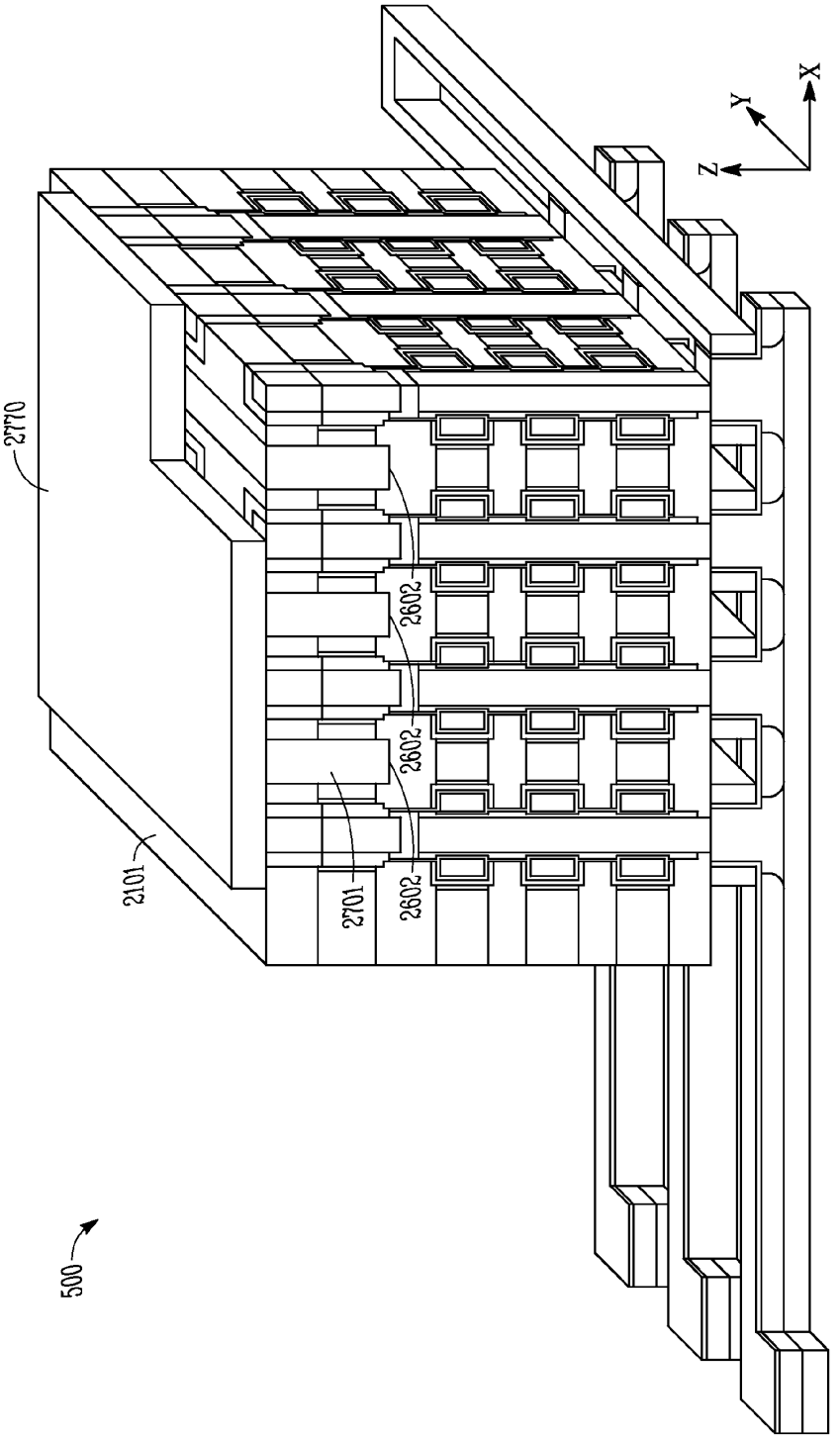


FIG. 27

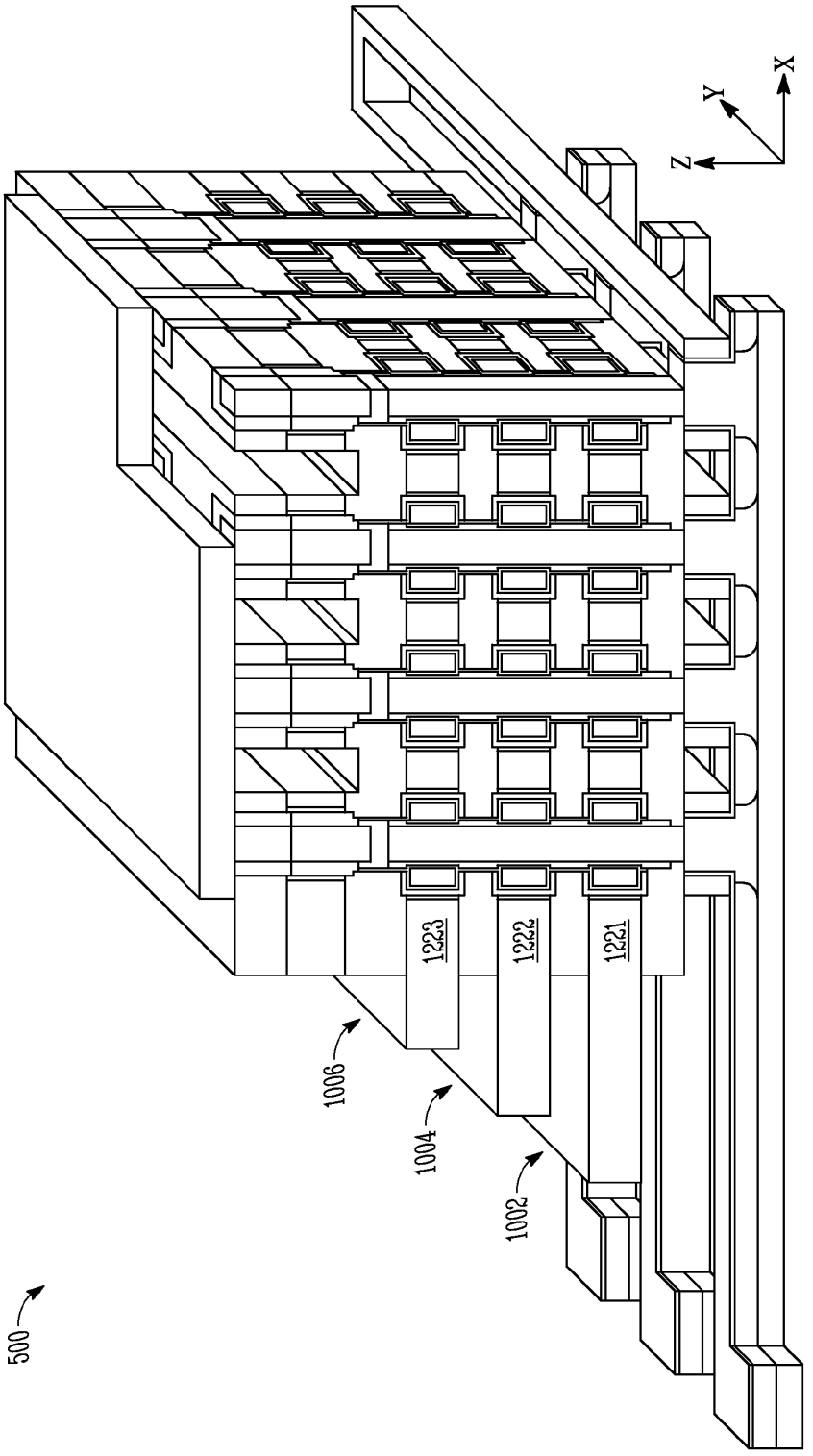


FIG. 28

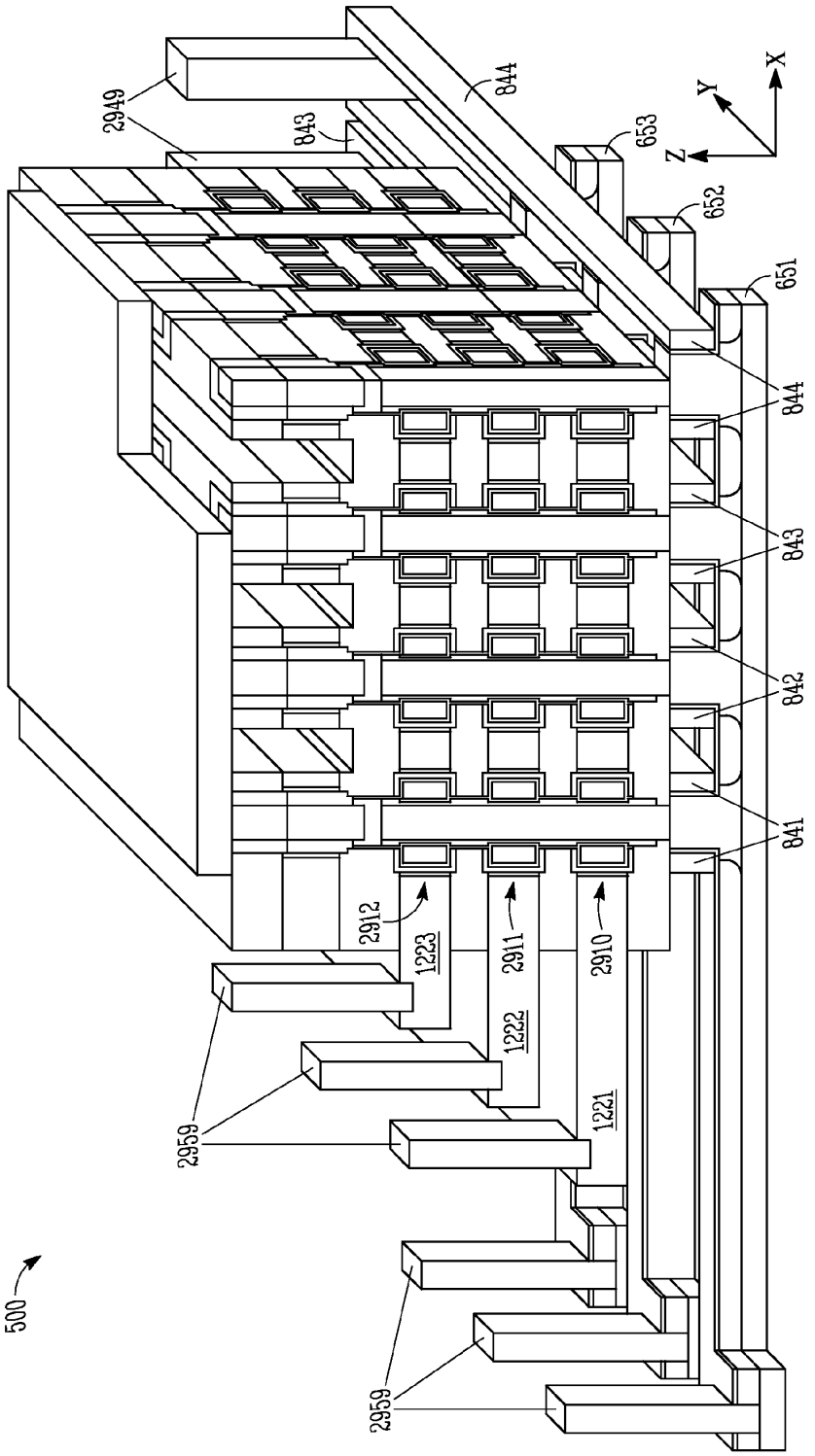

2949
843
844
653
652
651
Y
X
Z
844
843
842
841
2912
1223
2911
2910
1222
1221
2959
2959
500

FIG. 29

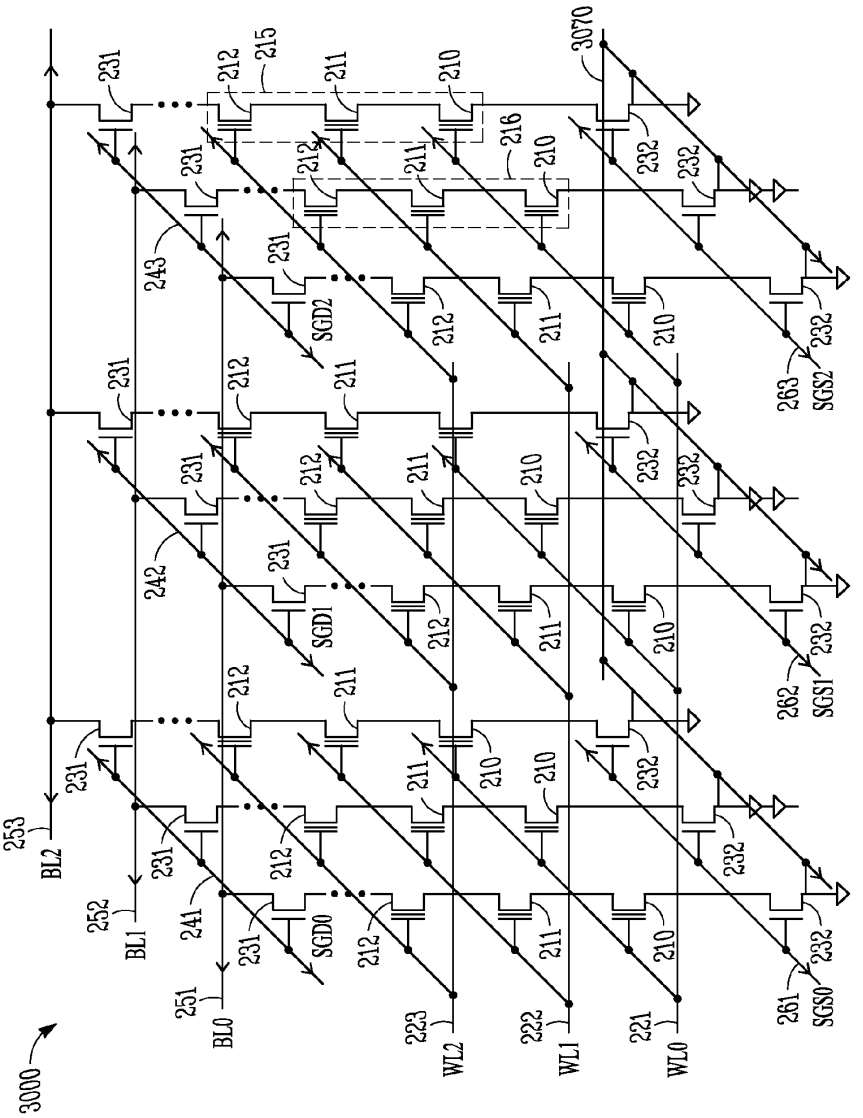

3000
3070
BL2
BL1
BL0
WL2
WL1
WL0
SGD2
SGD1
SGD0
SGS2
SGS1
SGS0

FIG. 30

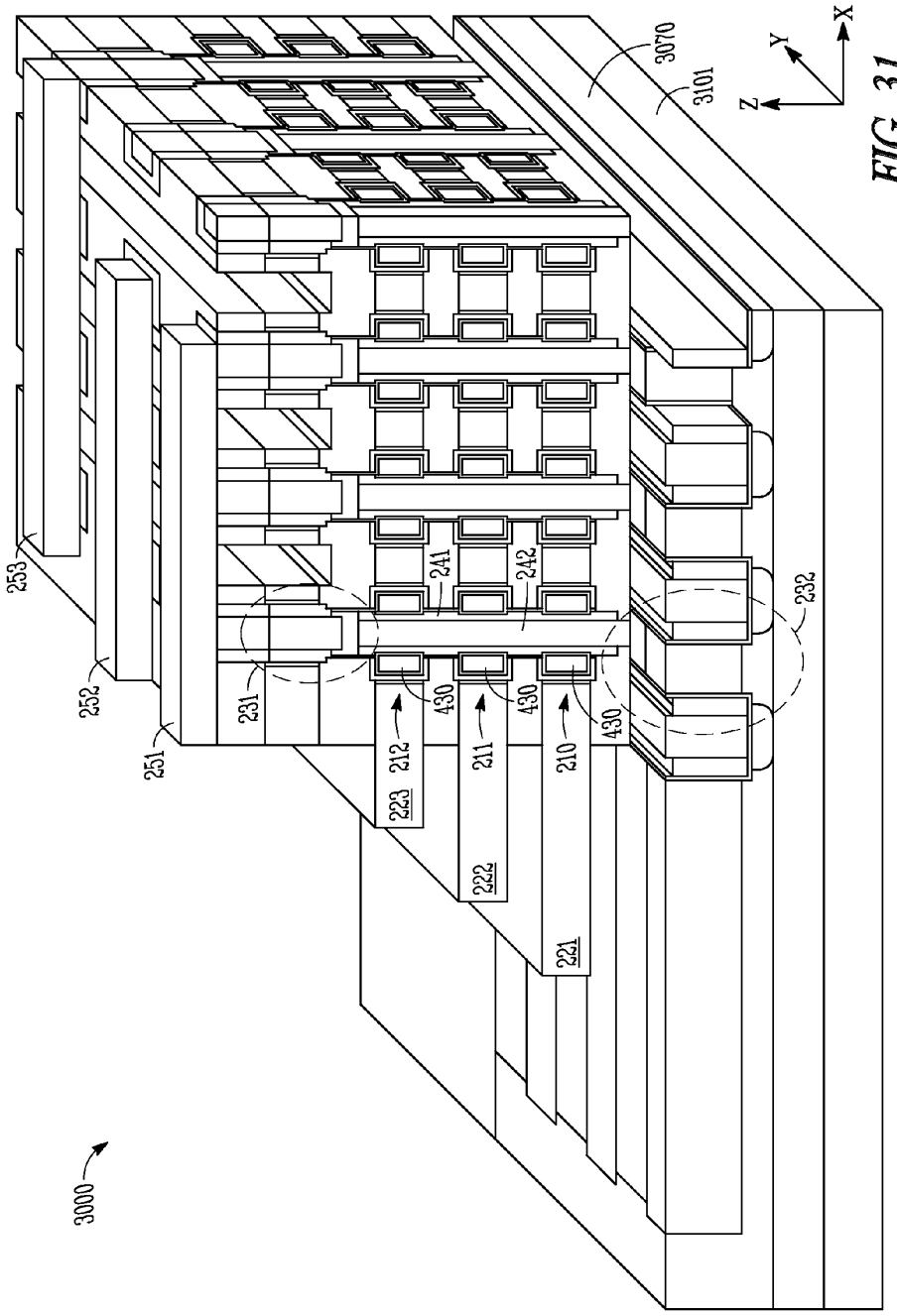

3070
3101
Z
Y
X
253
252
251
231
241
242
232
430
430
430
212
211
210
223
222
221
3000

FIG. 31

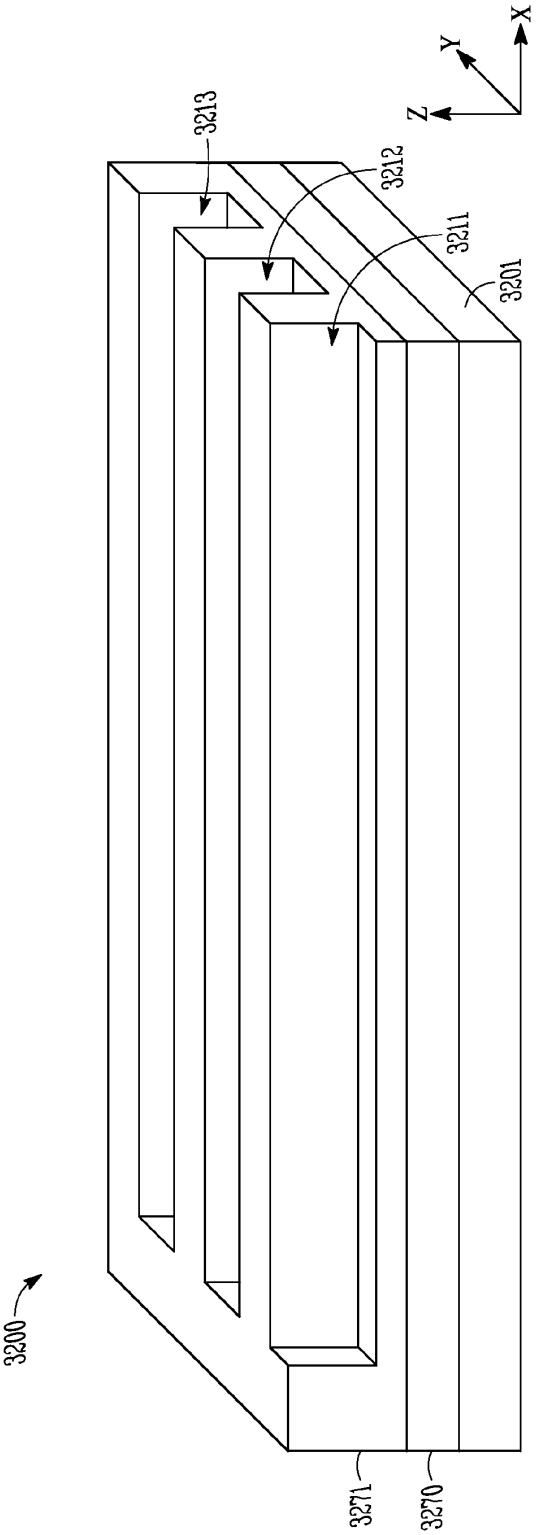


FIG. 32

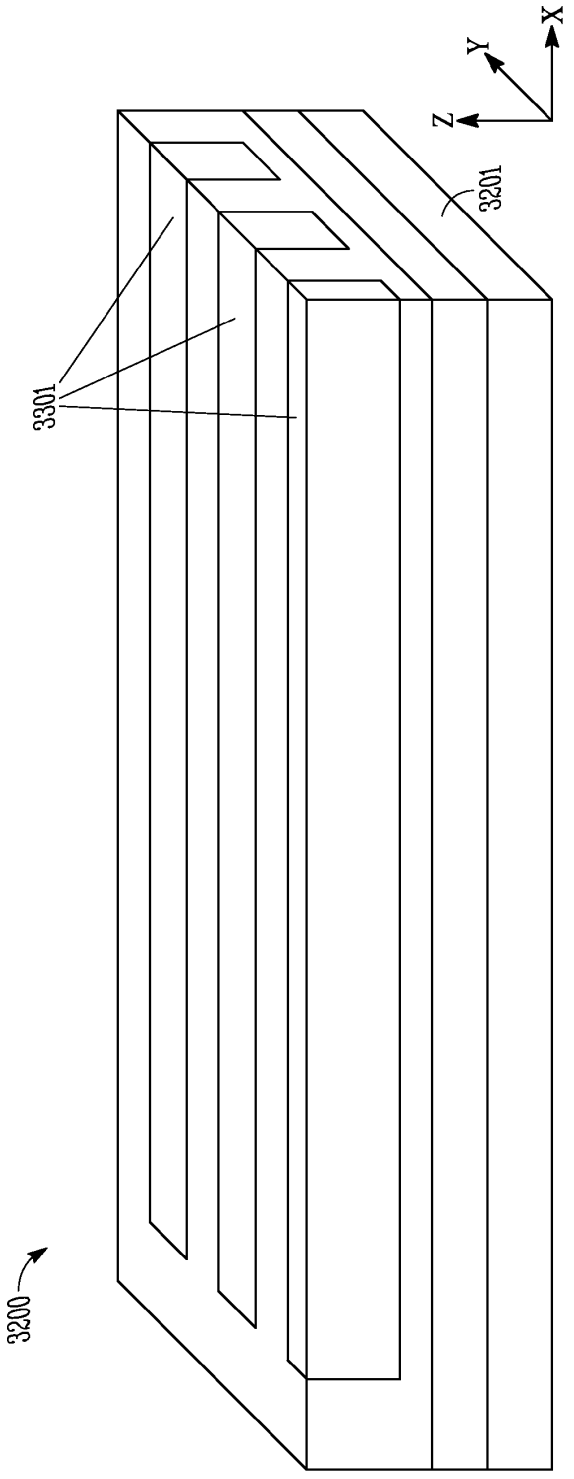


FIG. 33

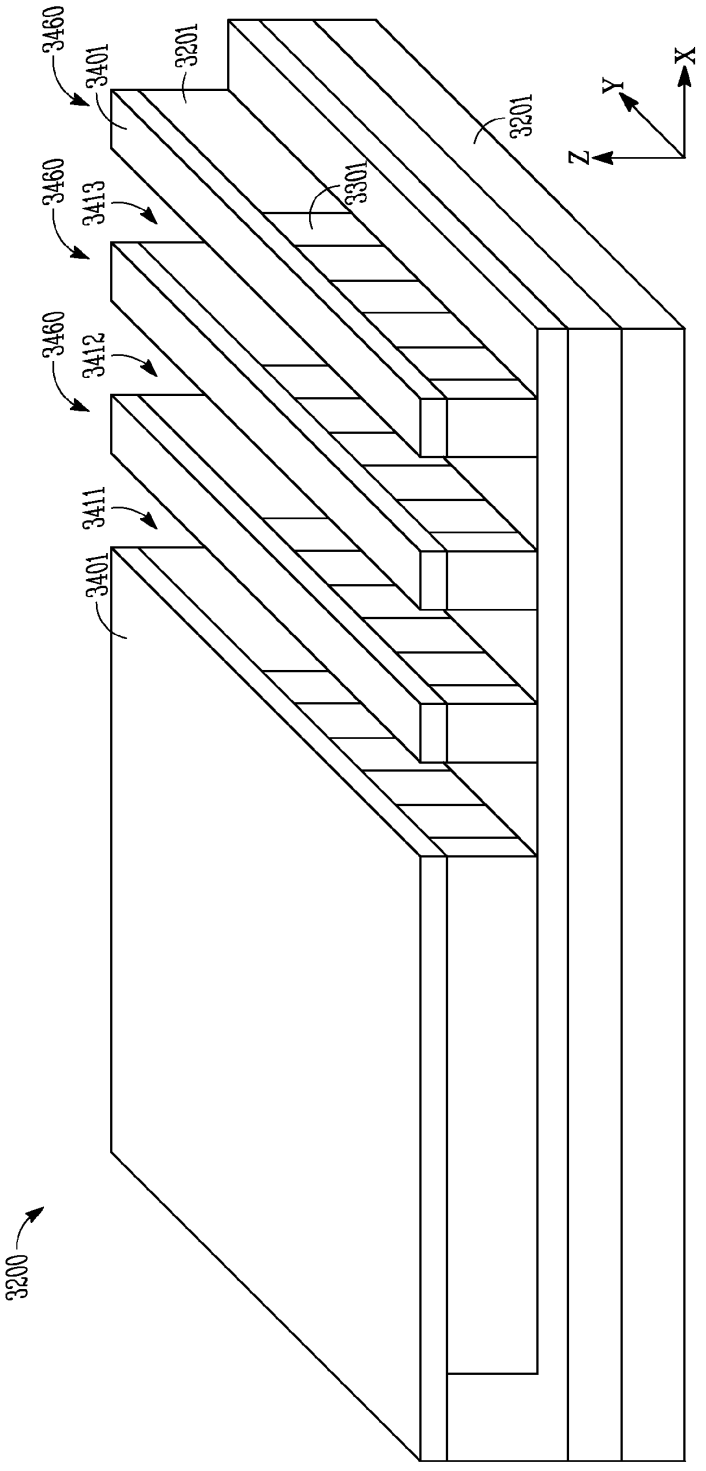

3460
3401
3201
3201
Y
X
Z
3460
3413
3301
3460
3412
3411
3401
3200

FIG. 34

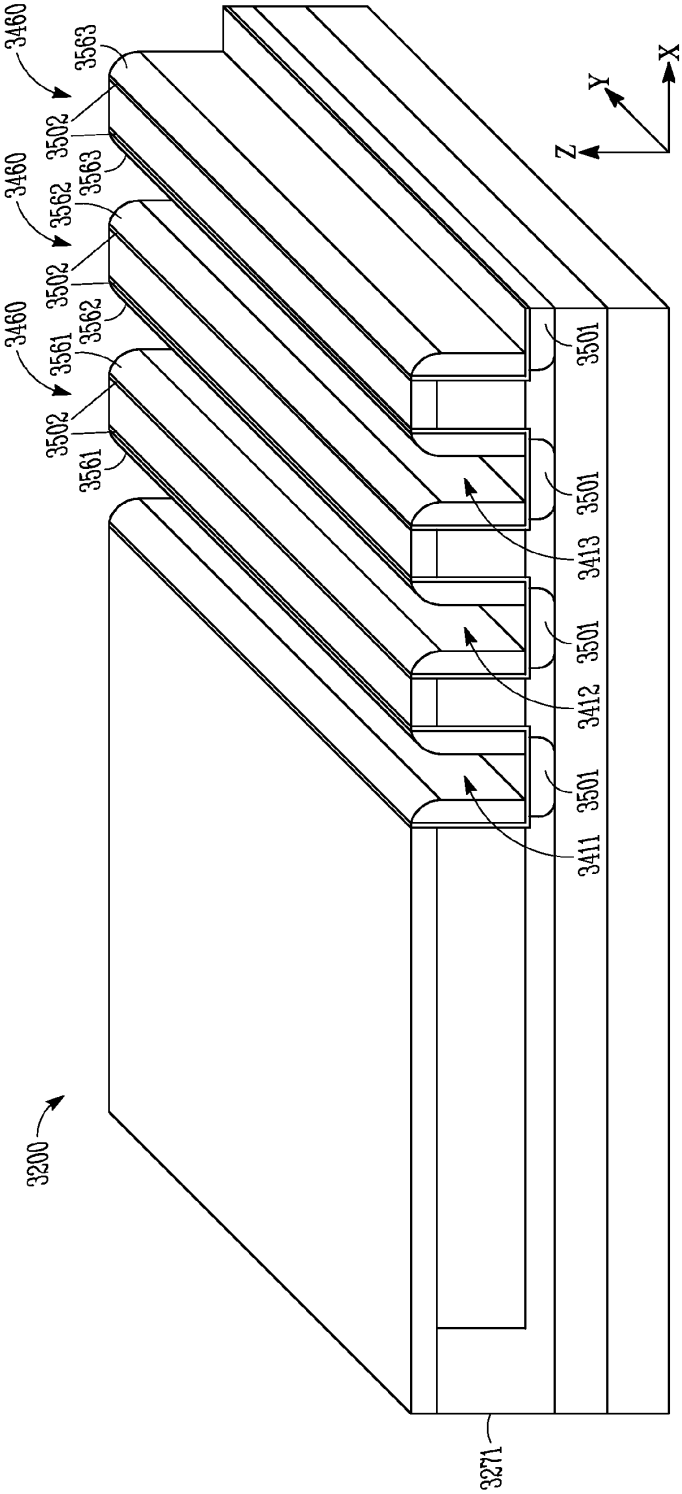

3460
3563
3502
3460
3562
3563
3502
3460
3561
3562
3502
3561
3501
3501
3413
3501
3412
3501
3411
3200
3271
Y
X
Z

FIG. 35

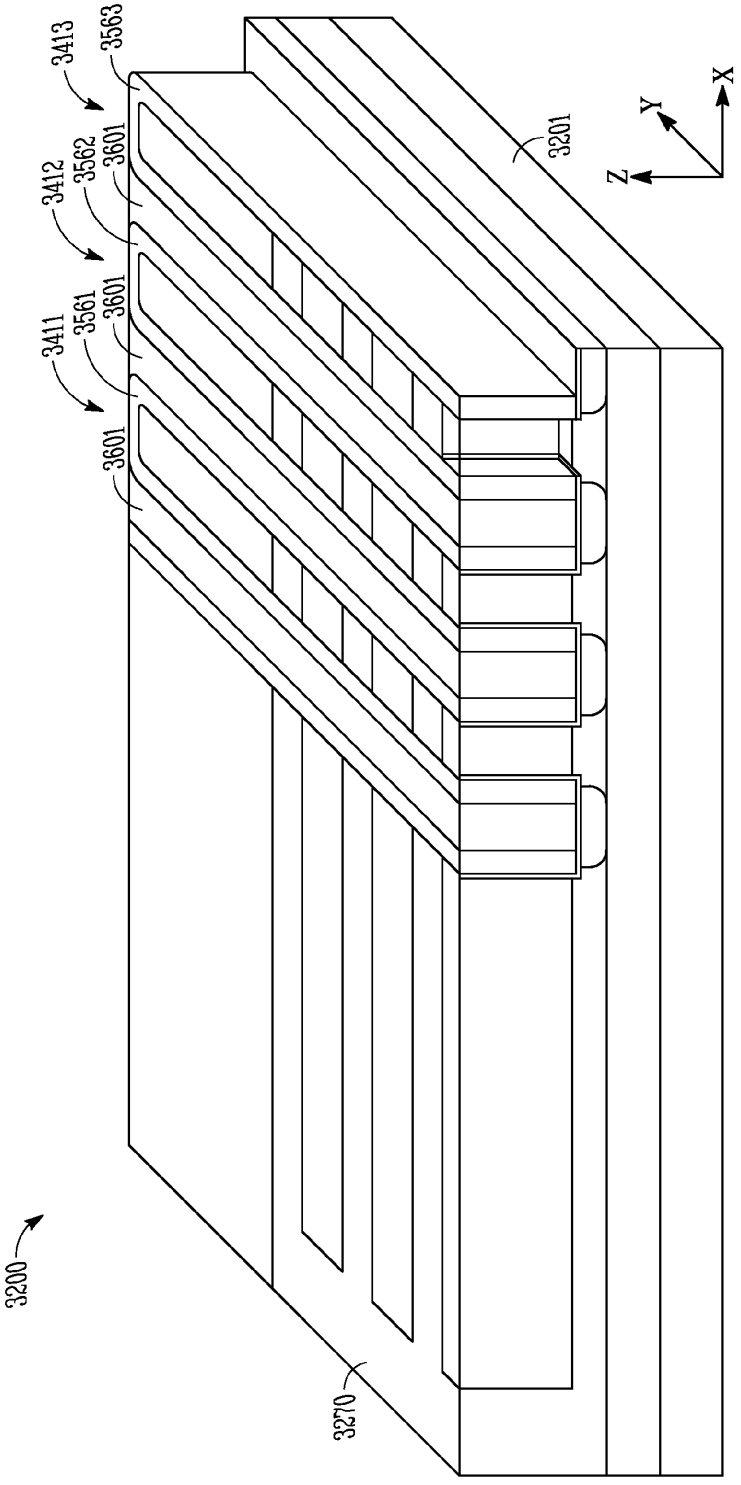

3413
3563
3412
3562
3601
3411
3561
3601
3601
3201
X
Y
Z
3200
3270

FIG. 36

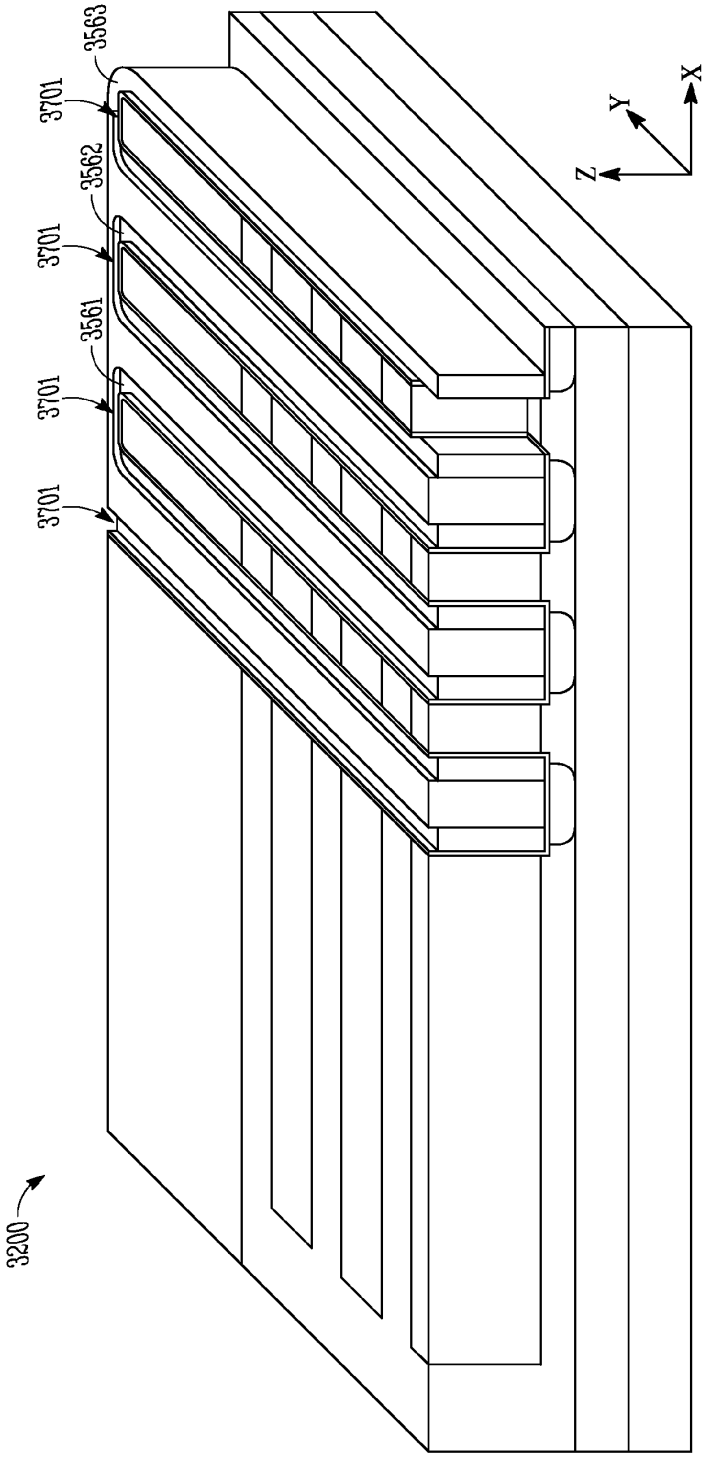


FIG. 37

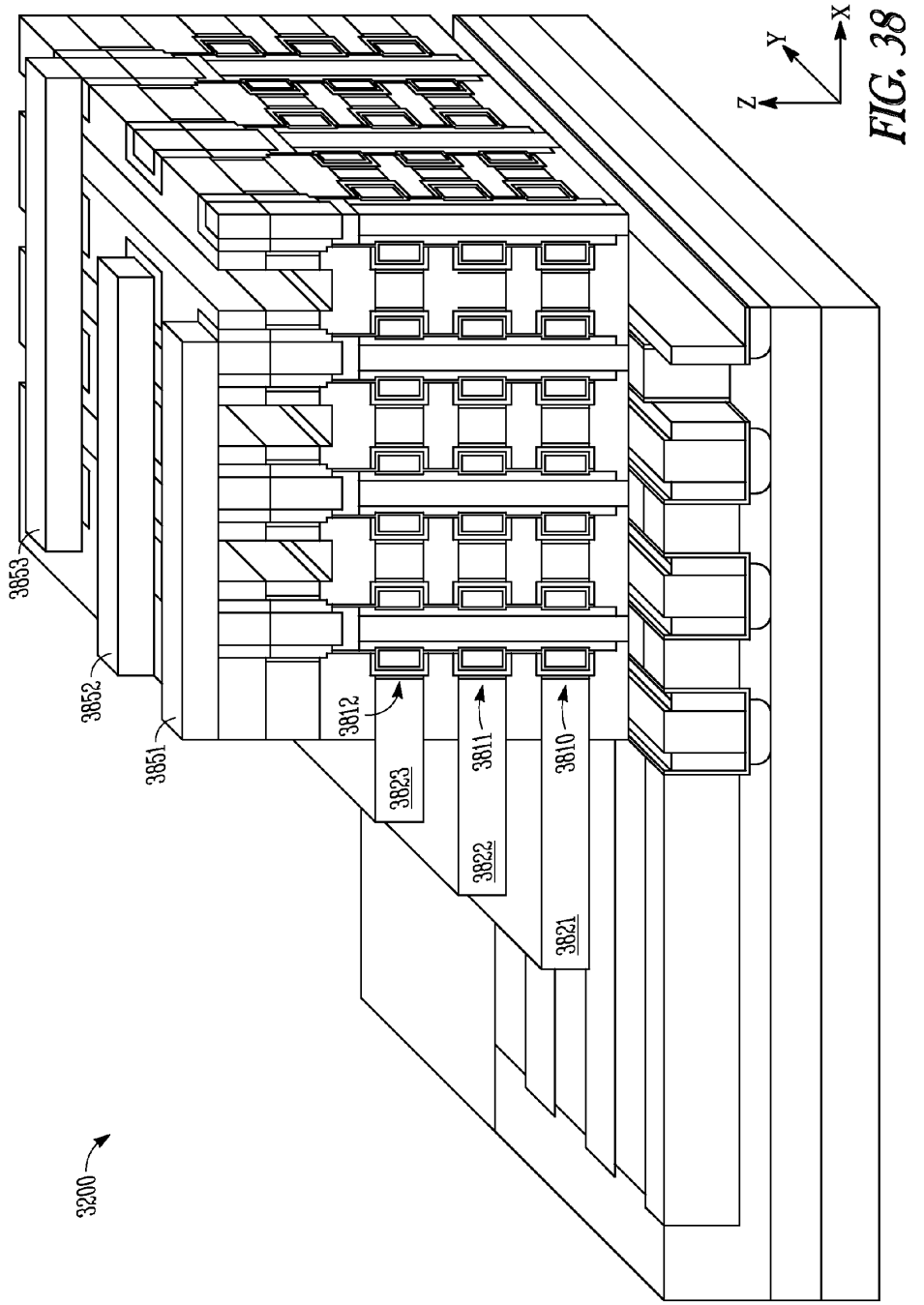


FIG. 38

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

BACKGROUND

Non-volatile memory devices such as flash memory devices are used in many computers and electronic devices to store information. A flash memory device usually has a write operation to store information (e.g., data and instruction codes), a read operation to retrieve the stored information, and an erase operation to clear information from the memory. As demand for higher density memory device increases, three-dimensional (3D) memory devices have been proposed. An example of a conventional 3D memory device is described by Jiyoung Kim et al. in an article titled "Novel 3-D Structure for Ultra High Density Flash Memory with Vertical-Array-Transistor (VRAT) and Planarized Integration on the same Plane (PIPE)", published in the 2008 Symposium on VLSI. Technology Digest of Technical Papers, pages 22-23. Since 3D memory devices are relatively new, manufacturing these devices can pose fabrication process challenges.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a block diagram of a memory device having a memory array with memory cells, according to an embodiment of the invention.

FIG. **2** shows a schematic diagram of a portion of a memory device having data lines located below memory cells, according to an embodiment of the invention.

FIG. **3** shows a three-dimensional view of a portion of the memory device of FIG. **2**, according to an embodiment of the invention.

FIG. **4** shows a portion of a control gate and a memory cell of the memory device of FIG. **3**, according to an embodiment of the invention.

FIG. **5** through FIG. **29** show various processes of forming a memory device having data lines located below memory cells, according to an embodiment of the invention.

FIG. **30** shows a schematic diagram of a portion of a memory device having data lines located above memory cells, according to an embodiment of the invention.

FIG. **31** shows a three-dimensional view of a portion of the memory device of FIG. **30**, according to an embodiment of the invention.

FIG. **32** through FIG. **38** show various processes of forming a memory device with data lines located above memory cells, according to an embodiment of the invention.

DETAILED DESCRIPTION

FIG. **1** shows a block diagram of a memory device **100** having a memory array **102** with memory cells **110** according to an embodiment of the invention. Memory cells **110** can be arranged in rows and columns along with access lines **123** (e.g., wordlines having signals WL**0** through WLM) and lines **124** (e.g., bit lines having signals BL**0** through BLN). Memory device **100** uses lines **124** and **128** to transfer information within memory cells **110**. Memory cells **110** can be physically located in multiple device levels such that one group of memory cells **110** can be stacked on one or more groups of other memory cells **110**. Row decoder **132** and column decoder **134** decode address signals A**0** through AX on lines **125** (e.g., address lines) to determine which memory cells **110** are to be accessed. Row and column level decoders **136** and **138** of row and column decoders **132** and **134**, respectively, determine which of the multiple device levels of memory device **100** that the memory cells **110** to be accessed are located.

A sense amplifier circuit **140** operates to determine the value of information read from memory cells **110** and provide the information in the form of signals to lines **124** and **128**. Sense amplifier circuit **140** can also use the signals on lines **124** and **128** to determine the value of information to be written to memory cells **110**. Memory device **100** can include circuitry **150** to transfer information between memory array **102** and lines (e.g., data lines) **126**. Signals DQ**0** through DQN on lines **126** can represent information read from or written into memory cells **110**. Lines **126** can include nodes within memory device **100** or nodes (e.g., pins or solder balls) on a package where memory device **100** resides. Other devices external to memory device **100** (e.g., a memory controller or a processor) may communicate with memory device **100** through lines **125**, **126**, and **127**.

Memory device **100** performs memory operations such as a read operation to read information from memory cells **110** and a write operation (sometime referred to as a programming operation) to store information into memory cells **110**. A memory control unit **118** controls the memory operations based on control signals on lines **127**. Examples of the control signals on lines **127** include one or more clock signals and other signals to indicate which operation, (e.g., a write or read operation) that memory device **100** performs. Other devices external to memory device **100** (e.g., a processor or a memory controller) may control the values of the control signals on lines **127**. Specific values of a combination of the signals on these lines can produce a command (e.g., a write or read command) that causes memory device **100** to perform a corresponding memory operation (e.g., a write or read operation).

Each of memory cells **110** can store information representing a value of a single bit or a value of multiple bits such as two, three, four, or other numbers of bits. For example, each of memory cells **110** can store information representing a binary value "0" or "1" of a single bit. In another example, each of memory cells **110** can store information representing a value of multiple bits, such as one of four possible values "00", "01", "10", and "11" of two bits, one of eight possible values "000", "001", "010", "011", "100", "101", "110" and "111, or one of other values of other number of multiple bits.

Memory device **100** can receive a supply voltage, including supply voltage signals Vcc and Vss, on lines **141** and **142**, respectively. Supply voltage signal Vss may operate at a ground potential (e.g., having a value of approximately zero volts). Supply voltage signal Vcc may include an external voltage supplied to memory device **100** from an external power source such as a battery or an alternating-current to direct-current (AC-DC) converter circuitry.

Circuitry **150** of memory device **100** can include a select circuit **152** and an input/output (I/O) circuit **116**. Select circuit **152** responds to signals SEL**0** through SELn to select the signals on lines **124** and **128** that can represent the information read from or written into memory cells **110**. Column decoder **134** selectively activates the SEL**0** through SELn signals based on address signals A**0** through AX. Select circuit **152** selects the signals on lines **124** and **128** to provide communication between memory array **102** and I/O circuit **116** during read and write operations.

Memory device **100** can be a non-volatile memory device and memory cells **110** can be non-volatile memory cells such that memory cells **110** can retain information stored thereon when power (e.g., Vcc or Vss, or both) is disconnected from memory device **100**. For example, memory device **100** can be

a flash memory device such as a NAND flash or a NOR flash memory device, or other kinds of memory devices, such as a variable resistance memory device (e.g., phase change random-access-memory (PCRAM), resistive RAM (RRAM), etc.).

One skilled in the art may recognize that memory device **100** may include other features that are not shown in FIG. **1**, to help focus on the embodiments described herein.

Memory device **100** may include at least one of the memory devices and memory cells described below with reference to FIG. **2** through FIG. **38**.

FIG. **2** shows a schematic diagram of a portion of a memory device **200** having data lines **251**, **252**, and **253** located below memory cells **210**, **211**, and **212**, according to an embodiment of the invention. Memory cells **210**, **211**, and **212** can be grouped into groups, such as a group of memory cells **210**, a group of memory cells **211**, and a group of memory cells **212**. As shown in FIG. **2**, the memory cells in each group share the same control gate, such as control gate **221**, **222**, or **223** (with associated signals WL**0**, WL**1**, and WL**2**). The memory cells are coupled in series as strings, such as strings **215** and **216**. Each string can include one of the memory cells from different groups and is coupled between one of transistors **231** and one of transistors **232**.

As shown in FIG. **2**, transistors **231** have gates coupled to select lines **241**, **242**, and **243** (with associated signals SGD**0**, SGD**1**, and SGD**2**). Transistors **231** have nodes (e.g., sources) coupled to data lines **251**, **252**, and **253** (with associated signals BL**0**, BL**1**, and BL**2**). Data lines **251**, **252**, and **253** sometimes correspond to bit lines or sense lines of a non-volatile memory device.

Transistors **232** have gates coupled to select lines **261**, **262**, and **263** (with associated signals SGS**0**, SGS**1**, and SGS**2**). Transistors **232** have nodes (e.g., drains) coupled to a common source **270** of memory cell strings in a non-volatile memory device.

FIG. **2** shows three groups of memory cells with associated components coupled to them, as an example. The number of groups of memory cells and their associated components (e.g., control gates and data lines) can vary.

Memory device **200** uses control gates **221**, **221**, and **223** to control access to memory cells **210**, **211**, and **212** during a read operation to sense (e.g., read) information stored in memory cells **210**, **211**, and **212**, and during a write operation to store information into memory cells **210**, **211**, and **212**. Memory device **200** uses data lines **251**, **252**, and **253** to transfer the information read from these memory cells during a read operation.

Transistors **231** and **232** are responsive to signals SGD**0**, SGD**1**, and SGD**2**, and signals SGS**0**, GS**1**, and SGS**2**, respectively, to selectively couple the memory cells to data lines **251**, **252**, and **253** and common source **270** during a read or write operation.

To help focus on the description herein; the description herein omits detailed description of operations of memory device, such as write, read, and erase operation. One skill in the art would recognize these operations. For example, in an erase operation of memory device **200**, a voltage of approximately 20 volts can be applied to data lines **251**, **252**, and **253** while control gates **221**, **221**, and **223**, select lines **241**, **242**, and **243**, and select lines **261**, **262**, and **263** can be "floated" (e.g., leave unconnected to a voltage). In this erase operation, electrons from memory elements of memory cells **210**, **211**, and **212** may move to data lines **251**, **253**, and **253**.

FIG. **3** shows a 3D view of a portion of memory device **200**, according to an embodiment of the invention. FIG. **3** also shows X, Y, and Z directions, and device levels **301**, **302**, and **303** arranged in the Z-direction. Memory cells **210** of the same group can be arranged in rows and columns in the X-direction and Y-direction. Each group of memory cells is located in different device levels **301**, **302**, or **303**. For example, the group having memory cells **210** is located in device level **301**. The group having memory cells **211** is located in device level **302**. The group having memory cells **212** is located in device level **303**.

As shown in FIG. **3**, memory cells **210**, **211**, and **212** in each string (e.g., memory cells between transistors **231** and **232**) are substantially vertically aligned in the Z-direction with respect to a substrate underneath data lines **251**, **252**, and **253**. The substrate is not shown in FIG. **3**, but can be similar to substrate **503** of FIG. **5** and FIG. **6**. FIG. **3** also shows a channel **241** and a conductive material portion **242** extending vertically in the Z-direction and through memory element **430** of memory cells **210**, **211**, and **212** in the same string between transistors **231** and **232**, which corresponds to transistors **231** and **232** of FIG. **2**. As shown in FIG. **3**, transistor **231** can include a double-gate coupled to a body **391** (e.g., transistor channel) to control (turn on or off) the transistor. The structure of the double-gate can include two segments of the same select line **241** (as shown in FIG. **3**), such that the two segments are located on only two respective sides of body **391**.

Memory device **200** in FIG. **3** also can include contacts **329**, **349**, and **359**. Contacts **329** provide electrical connections to control gates **221**, **222**, and **223**. Contacts **349** provide electrical connections to select lines **241**, **242**, **243**, and **244**. Contacts **359** provide electrical connections to and from data lines **251**, **252**, and **253**. Select line **244** and the memory cell associated with it in the Z-direction are not shown in FIG. **2**.

FIG. **4** shows a portion of control gate **221** and a memory cell **210** of memory device **200** of FIG. **3**. Control gates **222** and **223** and memory cells **211** and **212** of FIG. **2** have structures similar to control gate **221** and memory cell **210**, respectively. As shown in FIG. **4**, control gate **221** can include a homogenous material with cavities **420**, each cavity being filed with various components, including materials different from the homogenous material. The various components include: a memory element **430**; a channel **441**, a conductive material portion **442**, and dielectrics **421** and **427**. Dielectric **421** can include multiple materials **422**, **423**, and **424** arranged as different layers. As shown in FIG. **4**, memory element **430** of each memory cell **210** has a ring shape (e.g., donut shape) with an inner side **451** and an outer side **452**. Each of the other memory cells **211** and **212** shown in FIG. **3** also has a ring shape. As shown in FIG. **3**, within memory cells **210**, **211**, and **212** in the same string (e.g., between transistors **231** and **232**), the entire ring-shape memory element **430** of each memory cell is substantially vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

Each memory element **430** can store information, such as based on the amount of charge (e.g., number of electrons) therein. In each such memory element **430**, the amount of charge corresponds to the value of information store that memory element. The amount of charge can be controlled in a write operation or in erase operation. For example, electrons from channel **441** or conductive material portion **442**, or both, can move to memory element **430** during a write operation due to a tunneling effect known to those skilled in the art. In an erase operation, electrons from memory element **430** can move back to channel **441** or conductive material portion **442**, or both, to data lines **251**, **253**, and **253** (FIG. **2** and FIG. **3**).

Alternative embodiments might use a memory element **430** that can store information, such as based on the resistance of the element **430**, for example.

Memory device **200** of FIG. **3** can be formed using processes similar to or identical to those described below with reference to FIG. **5** through FIG. **29**.

FIG. **5** through FIG. **29** show various processes of forming a memory device **500** having data lines located below memory cells, according to an embodiment of the invention. Memory device **500** (shown in more details in FIG. **29**) can correspond to memory device **300** of FIG. **3**.

FIG. **5** shows memory device **500** having a substrate **503**, which can include materials **501** and **502** arranged as layers. Material **501** can include bulk silicon or could be another semiconductor material. Material **502** can be a dielectric material, for example, silicon oxide. FIG. **5** also shows materials **504** and **505** formed over substrate **503**. Forming materials **504** and **505** can include depositing a conductive material over substrate **503** and then depositing another conductive material over material **504**. Material **504** can include a metal or other conductive materials. Material **505** can include undoped polysilicon or doped polysilicon, such as p-type silicon or another conductive materials.

FIG. **5** also shows an X-direction, a Y-direction perpendicular to the X-direction, and a Z-direction perpendicular to both the X-direction and the Y-direction. As shown in FIG. **5**, materials **504** and **505** can be formed as different layers, one layer over (e.g., on) one or more other layers in the Z-direction.

As used herein, the term "on" used with respect to two or more materials, one "on" the other, means at least some contact between the materials, while "over" or "overlaying" could refer to either a material being "on" another material or where there is one or more additional intervening materials between the materials (e.g., contact is not necessarily required). The term "on", "over", or "overlying" does not imply any directionality as used herein unless otherwise explicitly stated as such.

FIG. **6** shows memory device **500** after data lines **651**, **652**, and **653** and device structures **605** have been formed. A process such as etching (e.g., dry etching) can be used to remove portions of materials **504** and **505** (FIG. **5**) to form trenches **511** and **512**, which have trench bottoms at material **502**. Each of data lines **651**, **652**, and **653** and each of device structures **605** has a greater dimension (e.g., length) extending in the X-direction. A mask (not shown in FIG. **6**) having separate openings extending in the X-direction can be used to form trenches **511** and **512**. As shown in FIG. **6**, trenches **511** and **512** divide material **504** (FIG. **5**) into separate data lines **651**, **652**, and **653**, which can correspond to data lines **251**, **252**, and **253** of FIG. **2**.

FIG. **7** shows memory device **500** after pillars **705** have been formed in area **701** of memory device **500**. Pillars **705** are not formed in area **702** of memory device **500**. For simplicity, FIG. **7** through FIG. **29** do not show substrate **503** of FIG. **6**. In FIG. **7**, a process such as etching (e.g., dry etch) can be used to remove portions of device structures **605** to form trenches **711**, **712**, and **713** in the Y-direction, perpendicular to trenches **511** and **512**, such that pillars **705** can be formed as shown in FIG. **7**. A mask (not shown in FIG. **7**) having separate openings extending in the Y-direction can be used to form trenches **711**, **712**, and **713**. Each pillar **705** can include a height in the Z-direction of approximately 20 to 50 nanometers. As shown in FIG. **7**, pillars **705** are arranged in rows and columns (e.g., in a matrix) in the X-direction and Y-direction. For simplicity, FIG. **7** does not show a dielectric material filled in trenches **511** and **512**. However, forming memory device **500** in FIG. **7** also can include forming a dielectric material (e.g., silicon oxide) to fill trenches **511** and **512** up to a top surface **715** of device structure **605**.

FIG. **8** shows memory device **500** after dielectric **831** and select lines **841**, **842**, **843**, and **844** have been formed. Select lines **841**, **842**, **843**, and **844** can correspond to select lines **241**, **242**, **243**, and **244**, respectively, of FIG. **3**. In FIG. **8**, dielectrics **831** are formed to electrically isolate select lines **841**, **842**, **843**, and **844** from pillars **705**. Dielectrics **831** can be formed by, for example, depositing a dielectric material (e.g., silicon oxide) on at least two sides of each pillar **705** or by oxidizing pillars **705**. After dielectrics **831** are formed, select lines **841**, **842**, **843**, and **844** can be formed by, for example, depositing a conductive material over pillars **705** and trenches **711**, **712**, and **713** (FIG. **7**) and then removing (e.g., etching) a portion of the conductive material to form select lines **841**, **842**, **843**, and **844** having the structure shown in FIG. **8**. Examples of the conductive materials for select lines **841**, **842**, **843**, and **844** include polysilicon, metal, or other conductive materials, such as TiN and TaN.

FIG. **8** also shows doped regions **833**, which can be formed by inserting (e.g., implanting) n-type impurities into selective portions of device structure **605**. Examples of n-type impurities include elements such as phosphorus (P) or arsenic (As). The remaining portion of device structures **605** that has not been inserted with n-type impurities may maintain its original material, such as p-type silicon, as described above with reference to FIG. **5**.

FIG. **9** shows memory device **500** with select lines **941**, **942**, **943**, and **944**, which are alternative structures for select lines **841**, **842**, **843**, and **844** of FIG. **8**. In FIG. **8**, opposite sides of each pillar **705** are associated with two different segments of the same select line **841**, **842**, **843**, or **844**. In FIG. **9**, except for the top surfaces of pillars **705**, each pillar **705** can be completely surrounded by the material of one of the select line **941**, **942**, **943**, or **944** (e.g., four sides of each pillar **705** are associated with four different segments of the same select line). Higher efficient memory device may be achieved with select lines **941**, **942**, **943**, and **944** in comparison to select lines **841**, **842**, **843**, and **844**. Select lines **941**, **942**, **943**, and **944** can also be alternative structures for select lines **241**, **242**, **243**, and **244**, respectively, of FIG. **3**. Thus, each transistor **231** of FIG. **2** and FIG. **3** can include a surrounded gate with a structure shown in FIG. **9**. Thus, instead of a double-gate shown in FIG. **3**, each transistor **231** of FIG. **3** can alternatively include a surrounded gate having four different segments of the same select line (such as select line **941**) surrounding body **391** (FIG. **3**).

FIG. **10** shows memory device **500** after materials **1001** through **1007** are formed over pillars **705** and select lines **841**, **842**, **843**, and **844**. Materials **1001** through **1007** can be formed in both areas **701** and **702** of memory device **500**. However, to focus on the description herein, FIG. **10** does not show some portions of materials **1001** through **1007** in area **702**. The description below with reference to FIG. **28** and FIG. **29** describes forming additional components (e.g., components similar to contacts **329** of FIG. **3**) in area **702** of memory device **500**.

In FIG. **10** through FIG. **29**, for simplicity, some number designations associated with some components of memory device **500** may not be repeated from one figure to another figure. In FIG. **10**, before forming materials **1001** through **1007**, a dielectric material (not shown in FIG. **10**), such as silicon oxide, can be formed to fill gaps **1041**, **1042**, and **1043**. Forming materials **1001** through **1007** can include alternately depositing dielectric material and conductive material in an interleave fashion, such that these materials are alternately

stacked over each other in the Z-direction, as shown in FIG. **10**. Materials **1001**, **1003**, **1005**, and **1007** can include dielectric materials, such as silicon oxide. Materials **1002**, **1004**, and **1006** can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon). As shown in FIG. **10**, materials **1001** through **1007** are formed such that materials **1002**, **1004**, and **1006** are electrically isolated from each other by materials **1001**, **1003**, **1005**, and **1007**.

FIG. **11** shows memory device **500** after openings (e.g., holes) **1101** have been formed in material **1002** through **1107**. Holes **1101** are formed such that each hole **1101** can be aligned substantially directly over a corresponding pillar **705**, as illustrated in FIG. **11**. Forming holes **1101** can include removing (e.g., etching) a portion of each of materials **1002** through **1007**, stopping at material **1001**, such that at least a portion of material **1001** or the entire material **1001** remains to separate holes **1101** from pillars **705**. Forming holes **1101** results in forming cavities **1110** in each of materials **1003**, **1005**, and **1007**, and cavities **1120** in each of materials **1002**, **1004**, and **1006**. As shown in FIG. **12**, cavities **1110** in the materials **1003**, **1005**, and **1007** are substantially aligned directly over cavities **1120** in the other materials **1002**, **1004**, and **1006**. Each cavity **1110** and each cavity **1120** may have substantially the same diameter, D1. Diameter D1 can also be considered the diameter of each hole **1101** at the location of each cavity **1110** and each cavity **1120**.

FIG. **12** shows memory device **500** after cavities **1220** have been formed in materials **1002**, **1004**, and **1006** (used to form control gates **1221**, **1222**, and **1223**). Forming cavities **1220** can include enlarging the size of cavities **1120** (FIG. **11**) while keeping the size of cavities **1110** substantially unchanged (e.g., remaining substantially at diameter D1). For example, enlarging the size of cavities **1120** (FIG. **11**) can include selectively removing (e.g., selective wet or dry etching) a portion of each of materials **1002**, **1004**, and **1006** at each cavity **1120** (FIG. **11**) such that the diameter of each cavity **1220** increases to substantially diameter D2, while the diameter D1 at each cavity **1110** remains substantially unchanged. Diameter D2 is greater than diameter D1. Forming cavities **1120** in materials **1002**, **1004**, and **1006** also form control gates **1221**, **1222**, and **1223**, which can correspond to control gates control gates **221**, **222**, and **223** of FIG. **2**.

FIG. **13** shows more details of control gate **1221** of FIG. **12**. Control gates **1222** and **1223** of FIG. **12** have a similar structure as control gate **1221**. As shown in FIG. **13**, control gate **1221** can include a homogenous material with cavities **1220** of FIG. **11** being arranged in rows and columns in the X-direction and Y-direction. Each cavity **1220** can include a sidewall **1225**.

FIG. **14** and FIG. **15** shows memory device **500** after dielectrics **1421** and memory elements **1430** have been formed in cavities **1220**. For simplicity, FIG. **15** does not show dielectrics **1421** and memory elements **1430** in all cavities **1220**. Each dielectric **1421** can be formed on sidewall **1225**, such that each dielectric **1421** and can be located between the material of control gate **1221** and memory element **1430**, and such that memory element **1430** can be electrically isolated from the material of control gate **1221** by at least a portion of dielectric **1421**. Forming dielectric **1421** can include forming multiple materials **1422**, **1423**, and **1424** (FIG. **15**) at different times, one material after another. Forming material **1422** can include oxidizing a portion (e.g., a surface) of sidewall **1225** to form dielectric material (e.g., silicon oxide) on sidewall **1225**. Alternatively, forming material **1422** can include depositing dielectric material (e.g., silicon oxide) on sidewall **1225**. Forming material **1423** can include depositing dielectric material (e.g., silicon nitride) on material **1422**, wherein a portion of that dielectric material may also form on sidewall **1425** of each cavity **1110**. Forming material **1424** can include depositing dielectric material (e.g., silicon oxide) on material **1423**.

Memory elements **1430** can be formed after dielectrics **1421** are formed. As shown in FIG. **15**, each memory element **1430** has a ring shape (e.g., a donut shape) with an inner side **1451** and an outer side **1452** of FIG. **14**. Forming memory elements **1430** can include depositing a material in holes **1101**. Since cavities **1220** of FIG. **14** are substantially aligned with cavities **1110**, the material (that forms memory element **1430**) may fill both cavities **1110** and **1120**. Then, a portion (e.g., center portion in each hole) of the material that forms memory elements **1430** can be removed (e.g., by etching in the same, single, etching step) such that the material in cavities **1110** can be removed (e.g., completely removed) and the material in cavities **1220** is not completely removed but partially removed. As shown in FIG. **14**, after the material that forms memory elements **1430** is removed from cavities **1110**, a portion of dielectric material **1423** (e.g., silicon nitride, that was formed on material **1422**) may be exposed. As shown in FIG. **14**, after the material that forms memory elements **1430** is partially removed from cavities **1220**, memory element **1430** (formed by the remaining material in a cavity **1220**) associated with the same hole **1101** may have its inner side **1451** substantially aligned with sidewall **1425** (or sidewall **1425** with portions of materials **1422** and **1423** of cavities **1110**) of cavities **1110**.

The material of memory elements **1430** can include, for example, semiconductor material (e.g., polysilicon), dielectric charge trapping material, such as silicon nitride or other dielectric charge trapping materials, or a variable resistance material, such as a phase change material (e.g., GST). During removing (e.g., etching) a portion of the material that forms memory elements **1430**, portions **1401** of material **1001** located over pillars **705** can also be removed to reduce the thickness of portions **1401**.

FIG. **16** and FIG. **17** show memory device **500** after dielectric **1627** has been formed on inner side **1451** of memory element **1430** and in cavities **1110**. Forming dielectric **1627** can include depositing dielectric material (e.g., silicon oxide) on inner side **1451**. Alternatively, forming dielectric **1627** can include oxidizing a portion (e.g., inner side **1451**) of memory element **1430**. Forming dielectric **1627** (e.g., by oxidation) may also consume material **1423** (FIG. **14**) formed on material **1422**, which formed on sidewall **1425** of cavities **1110**. Thus, dielectric **1627** may also form in cavities over material **1422**.

FIG. **18** and FIG. **19** show memory device **500** after channels **1841** have been formed on dielectrics **1627** in both cavities **1110** and **1220**. Forming channels **1841** can include depositing a conductive material on dielectrics **1627**. An etching process can be used to reduce the thickness of the conductive material after it is deposited. The conductive material of channels **1841** can include doped polysilicon, which can have the same material type (e.g., p-type) as pillars **705**. FIG. **18** also shows a formation of openings **1801**, which can be formed by removing (e.g., by etching) portions **1401** (FIG. **14**) located over pillars **705**. As shown in FIG. **19**, channel **1841** is facing memory elements **1430** and is electrically isolated from memory element **1430** by at least a portion of dielectric **1627**.

FIG. **20** shows memory device **500** after a conductive material **2001** has been formed by, for example, depositing undoped or lightly doped polysilicon to place channels **1841** in electrical communication with pillars **705**. As shown in

FIG. **20**, conductive material **2001** forms a continuous conductive path between channels **1841** and data lines **651**, **652**, and **653** through pillars **705**.

FIG. **21** shows memory device **500** after dielectric material **2101** (e.g., silicon oxide) has been formed over conductive material **2001**.

FIG. **22** shows memory device **500** after a formation of openings (e.g., holes **2201**), a conductive material portion **2260**, and conductive material portions **2241**. Holes **2201** are formed such that each hole **2201** can be aligned substantially directly over channels **1841**, as illustrated in FIG. **22**. Forming holes **2201** can include removing (e.g., etching) a portion of dielectric material **2101** and a portion of conductive material **2001** (FIG. **21**), stopping at a location in material **1007**. Holes **2201** can be formed such that after a portion of conductive material **2001** is removed during the formation of holes **2201**, conductive material **2001** is separated into conductive material portion **2260** and conductive material portions **2241**, as illustrated in FIG. **22**.

FIG. **23** shows memory device **500** after doped regions **2301** have been formed. Forming doped regions **2301** can include inserting (e.g., implanting) n-type impurities into top parts of conductive material portions **2241**. Doped regions **2301** can provide a relatively low resistance connection between channels **1841** and other components of memory device **500**.

FIG. **24** shows memory device **500** after dielectrics **2401** and channels **2402** have been formed. Dielectrics **2401** (e.g., silicon oxide) is formed on sidewalls of conductive material portion **2260** at the location of holes **2201**. Channels **2402** are formed on sidewalls of dielectric material **2101** and on dielectrics **2401**.

FIG. **25** shows memory device **500** after conductive material **2501** has been formed in each of holes **2201**, such that channel **2402** can be electrically coupled to channel **1841** through conductive material **2501**, doped region **2301**, and conductive material portion **2241**. Forming conductive material **2501** in each of holes **2201** can include depositing a conductive material (e.g., polysilicon) over material, such that the conductive material fills holes **2201**. Then, a top portion of the conductive material can be removed by, for example, etching back the conductive material or by chemical mechanical planarization (CMP).

FIG. **26** shows memory device **500** after doped regions **2601** and select lines **2661**, **2662**, and **2663** have been formed. Forming doped regions **2601** can include inserting (e.g., implanting) n-type impurities into top portions of conductive material **2501**. Forming select lines **2661**, **2662**, and **2663** can include removing parts of dielectric material **2101** and conductive material portion **2260** to form trenches **2602**, which have trench bottoms partially extending into material **1007**. As shown in FIG. **26**, trenches **2602** separate conductive material portion **2260** into select lines **2661**, **2662**, and **2663**, which can correspond to select lines **261**, **262**, and **263** of FIG. **2**.

FIG. **27** shows memory device **500** after material **2701** and a common source **2770** have been formed. Forming material **2701** can include depositing a dielectric material (e.g., silicon dioxide) over material **2101**, such that the dielectric material fills trenches **2602**. Then, a top portion of the dielectric material can be removed by, for example, etching back the dielectric material or by CMP. Forming common source **2770** can include depositing a conductive material (e.g., metal) over materials **2701** and **2101**.

FIG. **28** shows memory device **500** after materials **1001** through **1007** in area **702** (FIG. **10**) are processed (e.g., by patterning) to form a stair like pattern with material between the stairs are not shown in FIG. **28**. As mentioned above in the description of FIG. **10**, some portions of materials **1001** through **1007** are omitted from area **702** of FIG. **10** through FIG. **27** for clarity. FIG. **28** shows material **1001** through **1007** in area **702** after they have been processed to form the stair like pattern. As shown in FIG. **28**, control gates **1221**, **1222**, and **1223** are formed from materials **1002**, **1004**, and **1006**, respectively, which are formed in the stair like pattern.

FIG. **29** shows memory device **500** after contacts **2929**, **2949**, and **2959** have been formed. Contacts **2929** provide electrical connections to control gates **1221**, **1222**, and **1223**. Contacts **2949** provide electrical connections to select lines **841**, **842**, **843**, and **844**. Contacts **2959** provide electrical connections to and from data lines **651**, **652**, and **653**.

As shown in FIG. **29**, memory device **500** can include components and memory cells **2910**, **2911**, and **2912** similar to or identical to components and memory cells **210**, **211**, and **212** of memory device **300** described above with reference to FIG. **2** and FIG. **3**.

One skilled in the art may readily recognize that additional processes may be performed to form additional features of a memory device, such as memory device **500** described above. Thus, to help focus on the embodiments described herein, FIG. **5** through FIG. **29** described above and FIG. **30** through FIG. **38** described below show only some of the features of a memory device, such as memory device **500**.

FIG. **30** shows a schematic diagram of a portion of a memory device **300** having data lines **251**, **252**, and **253** located above memory cells **210**, **211**, and **212**, according to an embodiment of the invention. Memory device **300** can include components similar to those of memory device **200** of FIG. **3**. Thus, for simplicity, similar or same components between memory device **200** and memory device **3000** are given the same number designations. The detailed description of these similar components is not repeated in FIG. **30**. Main differences between memory device **3000** and memory device **200** include the locations of data lines **251**, **252**, and **253** and common source **3070** of memory device **3000** to enable global erase operation. As shown in FIG. **30**, data lines **251**, **252**, and **253** are located above memory cells **210**, **211**, and **212**. Common source **3070** is located below memory cells **210**, **211**, and **212** and can couple directly to at least a portion of a substrate of memory device **3000** (e.g., substrate **3101** in FIG. **31**). This main difference may allow voltages to be applied to various components of memory device **3000** in a different way during an erase operation and memory device **3000** function differently (e.g., during the global erase operation) in comparison with the erase operation (e.g., local erase operation) of memory device **200**. For example, in an erase operation of memory device **3000**, a voltage of approximately 20 volts can be applied to common source **3070**, while control gates **221**, **221**, and **223**, data lines **251**, **252**, and **253**, select lines **241**, **242**, and **243**, and select lines **261**, **262**, and **26** can be "floated". In this erase operation, electrons from memory elements of memory cells **210**, **211**, and **212** may move (e.g., by tunneling) to common source **3070** (e.g., global erase). In memory **200**, as described above with reference to FIG. **2**, FIG. **3**, and FIG. **4**, during an erase operation, electrons from memory elements of memory cells **210**, **211**, and **212** may move to data lines **251**, **253**, and **253** (e.g., local erase)

FIG. **31** shows a 3D view of a portion of the memory device **3000** of FIG. **30**, according to an embodiment of the invention. As shown in FIG. **31**, data lines **251**, **252**, and **253** are located above memory cells **210**, **211**, and **212**, common source **3070** is located below memory cells **210**, **211**, and **212** and is coupled to a substrate **3101**. Substrate **3101** can include semiconductor material, such as p-type silicon.

As shown in FIG. **31**, memory cells **210**, **211**, and **212** in each string (e.g., memory cells between transistors **231** and **232**) are substantially vertically aligned in the Z-direction with respect to substrate **3101**. Transistor **232** can include a double-gate or surrounded gate similar to the double-gate (FIG. **3**) or surrounded gate (FIG. **9**) of transistor **231** of FIG. **3**. FIG. **31** also shows a channel **441** and a conductive material portion **442** extending vertically in the Z-direction and through memory element **430** of memory cells **210**, **211**, and **212** in the same string between transistors **231** and **232**, which corresponds to transistors **231** and **232** of FIG. **30**.

Memory element **430** in each of memory cells **210**, **211**, and **212** has a ring shape. As shown in FIG. **31**, within memory cells **210**, **211**, and **212** in the same string, the entire ring-shape memory element **430** of each memory cell is substantially vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

FIG. **32** through FIG. **38** show various processes of forming a memory device **3200** having data lines located above memory cells, according to an embodiment of the invention. Memory device **3200** (shown in more details in FIG. **38**) can correspond to memory device **3000** of FIG. **31**.

FIG. **32** shows memory device **3200** having a substrate **3201** and trenches **3211**, **3212**, and **3213**, and substrate portions **3270** and **3271** formed on a top portion of substrate **3201**. Substrate **3201** can include semiconductor material, such as bulk silicon. Top substrate portions **3270** and **3271** can be formed by inserting (e.g., implanting) p-type impurities into a top portion of substrate **3201**. Thus, substrate portions **3270** and **3271** can include p-type silicon. Forming trenches **3211**, **3212**, and **3213** and substrate portion **3270** can include removing (e.g., etching) a portion of substrate portion **3271**. During a write or read operation of memory device **3200**, substrate portion **3270** can be coupled to a potential, such as to ground. During an erase operation of memory device **3200**, substrate portion **3270** can be coupled to a voltage, for example, approximately 20 volts.

FIG. **33** shows memory device **3200** after material **3301** has been formed in trenches **3211**, **3212**, and **3213** (FIG. **32**). Forming material **3301** can include depositing dielectric material (e.g., silicon oxide) over substrate **3201** to fill trenches **3211**, **3212**, and **3213**. Then, a top portion of the dielectric material can be removed by, for example, CMP.

FIG. **34** shows memory device **3200** after material **3401** and trenches **3411**, **3412**, and **3413**, and device structures **3460** have been formed. Forming material **3401** can include depositing dielectric material (e.g., silicon oxide, or silicon nitride) over substrate **3201** and material **3301**. Forming trenches **3411**, **3412**, and **3413** can include removing (e.g., etching) portions of substrate **3201**, material **3301**, and material **3401**. Device structures **3460** are formed as a result of the formation of trenches **3411**, **3412**, and **3413**.

FIG. **35** shows memory device **3200** after a formation of doped regions **3501**, material **3502**, and select lines **3561**, **3562**, and **3563**. Forming doped regions **3501** can include inserting (e.g., implanting) n-type impurities into selective portions of substrate portion **3271**. Material **3502** (e.g., silicon oxide) can be formed on both sides of each device structure **3460** to electrically isolate select lines **3561**, **3562**, and **3563** from device structures **3460**. Materials of select lines **3561**, **3562**, and **3563** can include one or more conductive materials, such as one or more metals, alloys, other conductive materials, or a combination thereof. Select lines **3561**, **3562**, and **3563** can correspond to select lines **261**, **262**, and **263** of memory device **3000** of FIG. **30**.

FIG. **36** shows memory device **3200** after material **3601** have been formed in trenches **3411**, **3412**, and **3413**. Forming material **3601** can include depositing dielectric material (e.g., silicon dioxide) to fill trenches **3411**, **3412**, and **3413**. Then, a top portion of the dielectric material can be removed by, for example, etching back the conductive material or by CMP, stopping at substrate portion **3270**.

FIG. **37** shows memory device **3200** after grooves **3701** have been formed by removing (e.g., by wet etching) a top portion of the material used to form select lines **3561**, **3562**, and **3563**. Alternatively, forming grooves **3701** can be omitted.

FIG. **38** shows memory device **3200** after other components have been formed. The processes for forming the components of memory device **3200** in FIG. **38** can include similar or identical processes for forming the component of memory device **500** described above with reference to FIG. **10** through FIG. **29**. For example, control gates **3821**, **3822**, and **3823** of FIG. **38** can be formed using processes similar to or identical to those of forming control gates **1221**, **1222**, and **1223** of memory device **500** described above with described above with reference to FIG. **5** through FIG. **29**. Data lines **3851**, **3852**, and **3853** of FIG. **38**, can correspond to data lines **251**, **252**, and **253** of FIG. **30** and FIG. **31**. As shown in FIG. **38**, memory device **3200** can include memory cells **3810**, **3811**, and **3812**, which can be formed using processes similar to or identical to those of forming memory cells **2910**, **2911**, and **2912** of memory device **500** described above with reference to FIG. **5** through FIG. **29**.

One or more embodiments described herein include a memory device and methods of forming the memory device. One such memory device can include a first group of memory cells, each cell of the first group being formed in a respective cavity of a first control gate located in one device level of the memory device. The memory device also can include a second group of memory cells, each cell of the second group being formed in a cavity of in a second control gate located in another device level of the memory device. Additional apparatus and methods are described. Other embodiments including additional apparatus and methods are described above with reference to FIG. **1** through FIG. **38**.

The illustrations of apparatus such as memory devices **100**, **200**, **500**, **3000**, and **3200**, and memory cells **210**, **211**, **212**, **2910**, **2911**, **2912**, **3010**, **3811**, and **3812** are intended to provide a general understanding of the structure of various embodiments and not a complete description of all the elements and features of the apparatus that might make use of the structures described herein.

The apparatus of various embodiments may include or be included in electronic circuitry used in high-speed computers, communication and signal processing circuitry, memory modules, portable memory storage devices (e.g., thumb drives), single or multi-processor modules, single or multiple embedded processors, multi-core processors, data switches, and application-specific modules including multilayer, multichip modules. Such apparatus may further be included as sub-components within a variety of electronic systems, such as televisions, cellular telephones, personal computers (e.g., laptop computers, desktop computers, handheld computers, tablet computers, etc.), workstations, radios, video players, audio players (e.g., MP3 (Motion Picture Experts Group, Audio Layer 3) players), vehicles, medical devices (e.g., heart monitor, blood pressure monitor, etc.), set top boxes, and others.

The above description and the drawings illustrate some embodiments of the invention to enable those skilled in the art to practice the embodiments of the invention. Other embodi-

ments may incorporate structural, logical, electrical, process, and other changes. Examples merely typify possible variations. Portions and features of some embodiments may be included in, or substituted for, those of others. Many other embodiments will be apparent to those of skill in the art upon studying and understanding the above description.

The Abstract is provided to comply with 37 C.F.R. §1.72(b) requiring an abstract that will allow the reader to quickly ascertain the nature and gist of the technical disclosure. The Abstract of the Disclosure is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

What is claimed is:

1. An apparatus comprising:
- a substrate of a memory device;
- a plurality of first memory cells located in a first device level of the memory device over the substrate;
- a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level;
- a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;
- a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate; and
- data lines configured to be selectively coupled to a common source and the memory cells through conductive material.

2. The apparatus of claim **1**, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction,
- the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions.

3. The apparatus of claim **2**, wherein the common source is formed over a substrate of the memory device, such that the common source is between the first and second memory cells and the substrate to allow electrons from the memory element of at least one of the first and second memory cells to move to the common source during an erase operation.

4. The apparatus of claim **1**, wherein the first memory cells are substantially vertically aligned with the second memory cells.

5. The apparatus of claim **1**, wherein the memory element of each of the first memory cells is substantially vertically aligned with the memory element of one of the second memory cells.

6. The apparatus of claim **1**, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a double-gate.

7. The apparatus of claim **1**, further comprising transistors to selectively couple the first and second memory cells to the data lines associated with the first and second memory cells during a memory operation of the memory device, wherein at least one of the transistors comprises a surrounded gate.

8. An apparatus comprising:
- a plurality of first memory cells located in a first device level of a memory device;
- a plurality of second memory cells located in a second device level of the memory device;
- a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate;
- a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate, wherein the first and second memory cells include multiple memory cells arranged in a first direction and multiple memory cells arranged in a second direction;
- a common source; and
- data lines configured to be selectively coupled to the common source and the first and second memory cells through conductive material, the conductive material extending through the first and second memory cells in a third direction, the third direction being substantially perpendicular to the first and second directions, wherein the common source is formed over a substrate of the memory device, such that the first and second memory cells are between the common source and the substrate.

9. An apparatus comprising:
- a first non-volatile memory cell including a first memory element, the first memory element having a ring shape, the first memory element located in a first device level of a memory device;
- a second non-volatile memory cell including a second memory element, the second memory element having a ring shape, the second memory element located in a second device level of the memory device, wherein the first device level is different from the second device level;
- a conductive material extending through the first and second memory elements; and
- a data line configured to be selectively coupled to a common source and the first and second memory cells through the conductive material.

10. The apparatus of claim **9**, further comprising:
- a first additional conductive material configured to operate as a control gate to access the first memory cell, wherein the first memory element and the first additional conductive material are located in the first device level of the memory device; and
- a second additional conductive material configured to operate as a control gate to access the second memory cell, wherein the second memory element and the second additional conductive material are located in the second device level of the memory device.

11. The apparatus of claim **10**, wherein each of the first and second memory cells further includes a first dielectric between the respective memory element and the conductive material.

12. The apparatus of claim **11**, wherein each of the first and second memory cells further includes a second dielectric between the respective memory element and the respective additional conductive material.

13. The apparatus of claim **9**, wherein the data line is located between the substrate and the first memory cell.

14. The apparatus of claim **9**, wherein the first and second memory cells are located between the substrate and the data line.

15. An apparatus comprising:

a substrate of a memory device;

a first conductive material located in a first device level of the memory device over the substrate, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device over the first device level and over the substrate, the second conductive material including a second cavity, the second cavity having a second sidewall, wherein the first device level is different from the second device level;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element; and

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric.

16. The apparatus of claim **15**, wherein the first and second memory elements comprise polysilicon.

17. The apparatus of claim **15**, wherein the first and second memory elements comprise a dielectric material.

18. The apparatus of claim **17**, wherein the dielectric material comprises silicon nitride.

19. The apparatus of claim **15**, further comprising dielectric material between the first and second conductive materials.

20. The apparatus of claim **15**, further comprising:

a data line configured to be selectively coupled to the conductive channel, wherein the first and second memory elements are located between the data line and the substrate.

21. An apparatus comprising:

a first conductive material located in a first device level of a memory device, the first conductive material including a first cavity, the first cavity having a first sidewall;

a second conductive material located in a second device level of the memory device, the second conductive material including a second cavity, the second cavity having a second sidewall;

a first dielectric formed on the first sidewall and the second sidewall;

a first memory element located in the first cavity and electrically isolated from the first conductive material by a first portion of the first dielectric;

a second memory element located in the second cavity and electrically isolated from the second conductive material by a second portion of the first dielectric;

a second dielectric formed on a side of the first memory element and on a side of the second memory element;

a conductive channel extending from the first device level to the second device level and facing the first and second memory elements, such that the conductive channel is electrically isolated from the first and second memory elements by at least a respective portion of the second dielectric;

a substrate; and

a data line configured to be selectively coupled to the conductive channel, wherein the data line is located between the second conductive material and the substrate.

* * * * *

Exhibit 6

REDACTED

EXHIBIT 6 (02/16/2024)

Micron's Exemplary Infringement Claim Chart for U.S. Patent No. 8,803,214

The following chart provides non-limiting examples, without the benefit of claim construction or discovery, of how YMTC's Accused Products (as that term is defined in the Complaint) meet every limitation, literally or under the doctrine of equivalents, of at least claim 1 of U.S. Patent No. 8,803,214. The referenced images are images from a 232L YMTC 1Tb TLC part. Micron reserves the right to amend, correct, supplement, or otherwise change its explanation of how YMTC's Accused Products meet the following claim limitations, including as the claims are construed, as discovery progresses, or as Micron's investigation continues. Micron takes no position on claim interpretation or scope at this time.

Claim Language	YMTC's Accused Products
1. An apparatus comprising:[1]	YMTC's Accused Products includes "an apparatus." Specifically, as shown below, the products include a semiconductor apparatus: REDACTED

[1] By providing this disclosure, Micron does not concede that the preamble is a claim limitation.

EXHIBIT 6 (02/16/2024)

a substrate of a memory device;	YMTC's Accused Products include "a substrate of a memory device." Specifically, as shown below, YMTC's Accused Products include a substrate that supports multiple memory strings: REDACTED
a plurality of first memory cells located in a first device level of the memory device over the substrate;	YMTC's Accused Products include "a plurality of first memory cells located in a first device level of the memory device over the substrate." Specifically, as shown below, YMTC's Accused Products include multiple device levels (each control gate (e.g., word line) with memory cells in the cavities):

EXHIBIT 6 (02/16/2024)

	REDACTED Note that the 214 Patent explains that: "The term 'on', 'over', or 'overlying' does not imply any directionality as used herein unless otherwise explicitly stated as such." 8,803,214 Patent at 5:30-38.
a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from	YMTC's Accused Products include "a plurality of second memory cells located in a second device level of the memory device over the first device level and over the substrate, wherein the first device level is different from the second device level." Specifically, as shown below, YMTC's Accused Products include multiple device levels (each control gate (e.g., word line) with memory cells in the cavities):

EXHIBIT 6 (02/16/2024)

the second device level;	REDACTED Note that the 214 Patent explains that: "The term 'on', 'over', or 'overlying' does not imply any directionality as used herein unless otherwise explicitly stated as such." 8,803,214 Patent at 5:30-38.
a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a	YMTC's Accused Products include "a first control gate formed in the first device level, the first control gate to control access to the first memory cells, wherein each of the first memory cells includes a memory element formed in a cavity of the first control gate." Specifically, as shown below, YMTC's Accused Products include in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):

EXHIBIT 6 (02/16/2024)

cavity of the first control gate;	REDACTED
a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate; and	YMTC's Accused Products include "a second control gate formed in the second device level, the second control gate to control access to the second memory cells, wherein each of the second memory cells includes a memory element formed in a cavity of the second control gate." Specifically, as shown below, YMTC's Accused Products include in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):

EXHIBIT 6 (02/16/2024)

	REDACTED
data lines configured to be selectively coupled to a common source and the memory cells through conductive material.	YMTC's Accused Products include "data lines configured to be selectively coupled to a common source and the memory cells through conductive material." Specifically, as shown below, YMTC's Accused Products include data lines that selectively couples, e.g., through select gate transistor devices (e.g., shown below on top and bottom of stack), through conductive material (e.g., semiconductor pillar and metal material interconnects) to both a common source and memory cells, e.g., during accesses to the memory cells:

EXHIBIT 6 (02/16/2024)

	REDACTED YMTC describes the connections between the data lines, common source, and memory array in U.S. Pat. No. 10,937,806 at 6:36-56.

Exhibit 7

US010872903B2

(12) **United States Patent**
Tang et al.

(10) **Patent No.: US 10,872,903 B2**
(45) **Date of Patent: Dec. 22, 2020**

(54) **THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/716,177**

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H01L 27/11565 (2017.01)
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(52) **U.S. Cl.**
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(Continued)

(58) **Field of Classification Search**
CPC ... H01L 27/11517–27/1156; H01L 2924/1438; H01L 29/42324–29/42336;
(Continued)

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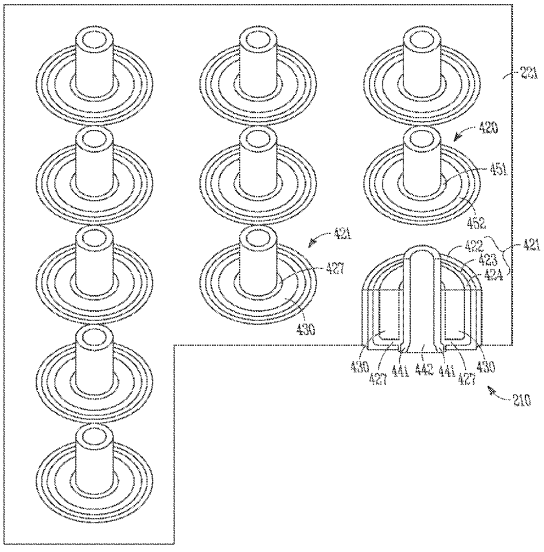
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(57) **ABSTRACT**

Some embodiments include a memory device and methods of forming the memory device. One such memory device includes a first group of memory cells, each of the memory cells of the first group being formed in a cavity of a first control gate located in one device level of the memory device. The memory device also includes a second group of memory cells, each of the memory cells of the second group being formed in a cavity of a second control gate located in another device level of the memory device. Additional apparatus and methods are described.

20 Claims, 38 Drawing Sheets



Related U.S. Application Data

continuation of application No. 15/722,580, filed on Oct. 2, 2017, now Pat. No. 10,090,324, which is a continuation of application No. 15/188,273, filed on Jun. 21, 2016, now Pat. No. 9,780,115, which is a continuation of application No. 14/041,928, filed on Sep. 30, 2013, now Pat. No. 9,379,005, which is a division of application No. 12/825,211, filed on Jun. 28, 2010, now Pat. No. 8,803,214.

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H01L 21/28	(2006.01)
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CPC ***G11C 13/0097*** (2013.01); ***G11C 16/10*** (2013.01); ***G11C 16/14*** (2013.01); ***G11C 16/26*** (2013.01); ***H01L 21/76838*** (2013.01); ***H01L 23/528*** (2013.01); ***H01L 27/0688*** (2013.01); ***H01L 27/11519*** (2013.01); ***H01L 27/11548*** (2013.01); ***H01L 27/11551*** (2013.01); ***H01L 27/11556*** (2013.01); ***H01L 27/11565*** (2013.01); ***H01L 27/11575*** (2013.01); ***H01L 27/11578*** (2013.01); ***H01L 27/249*** (2013.01); ***H01L 27/2454*** (2013.01); ***H01L 29/40114*** (2019.08); ***H01L 29/66825*** (2013.01); ***H01L 29/66833*** (2013.01); ***H01L 29/7889*** (2013.01); ***H01L 29/7926*** (2013.01); *G11C 2213/71* (2013.01); *H01L 45/06* (2013.01)

(58) **Field of Classification Search**

CPC H01L 29/788–29/7889; H01L 27/11582; H01L 27/11519; H01L 23/528

See application file for complete search history.

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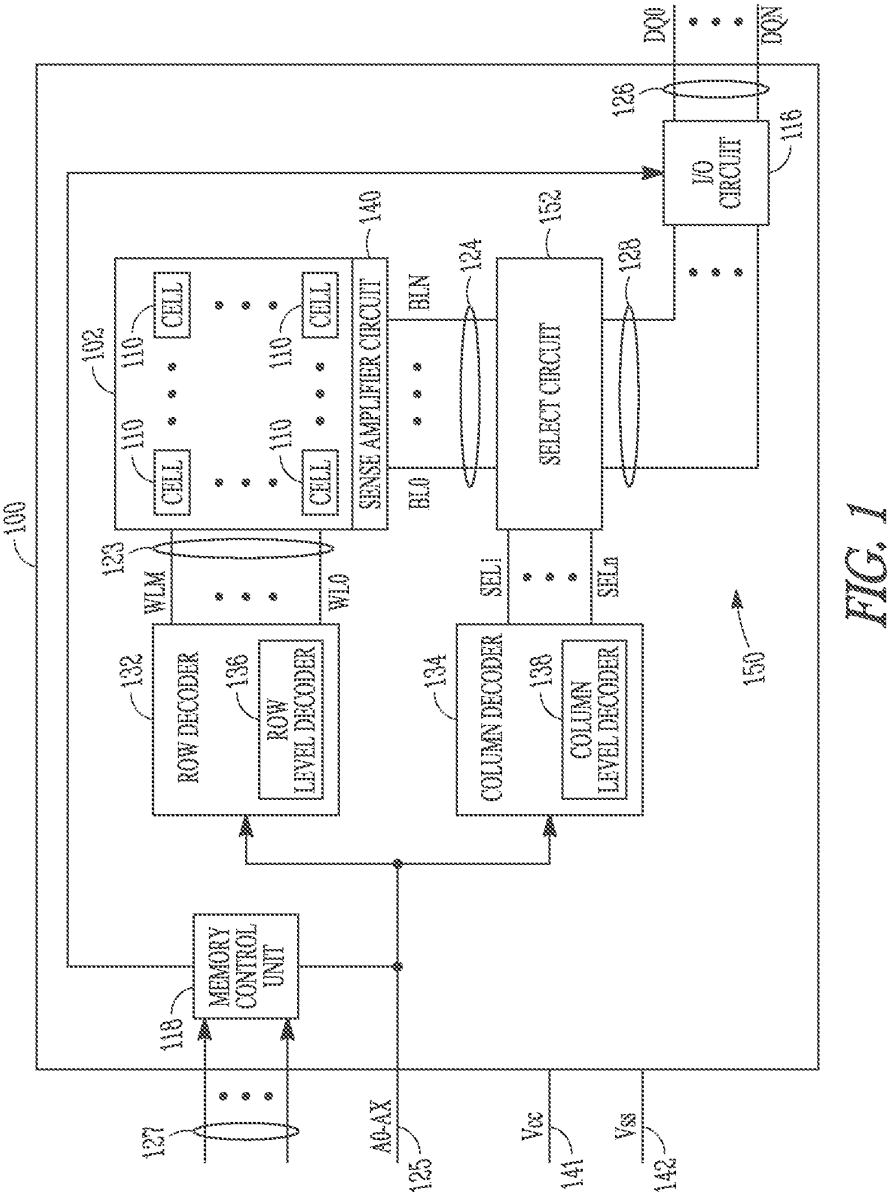

100
102
110
CELL
SENSE AMPLIFIER CIRCUIT
140
BL0
BLN
124
SELECT CIRCUIT
152
128
I/O CIRCUIT
116
126
DQ0
DQN
123
WL0
WLM
ROW DECODER
132
ROW LEVEL DECODER
136
SEL1
SELn
COLUMN DECODER
134
COLUMN LEVEL DECODER
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150
MEMORY CONTROL UNIT
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127
A0-AX
125
Vcc
141
Vss
142

FIG. 1

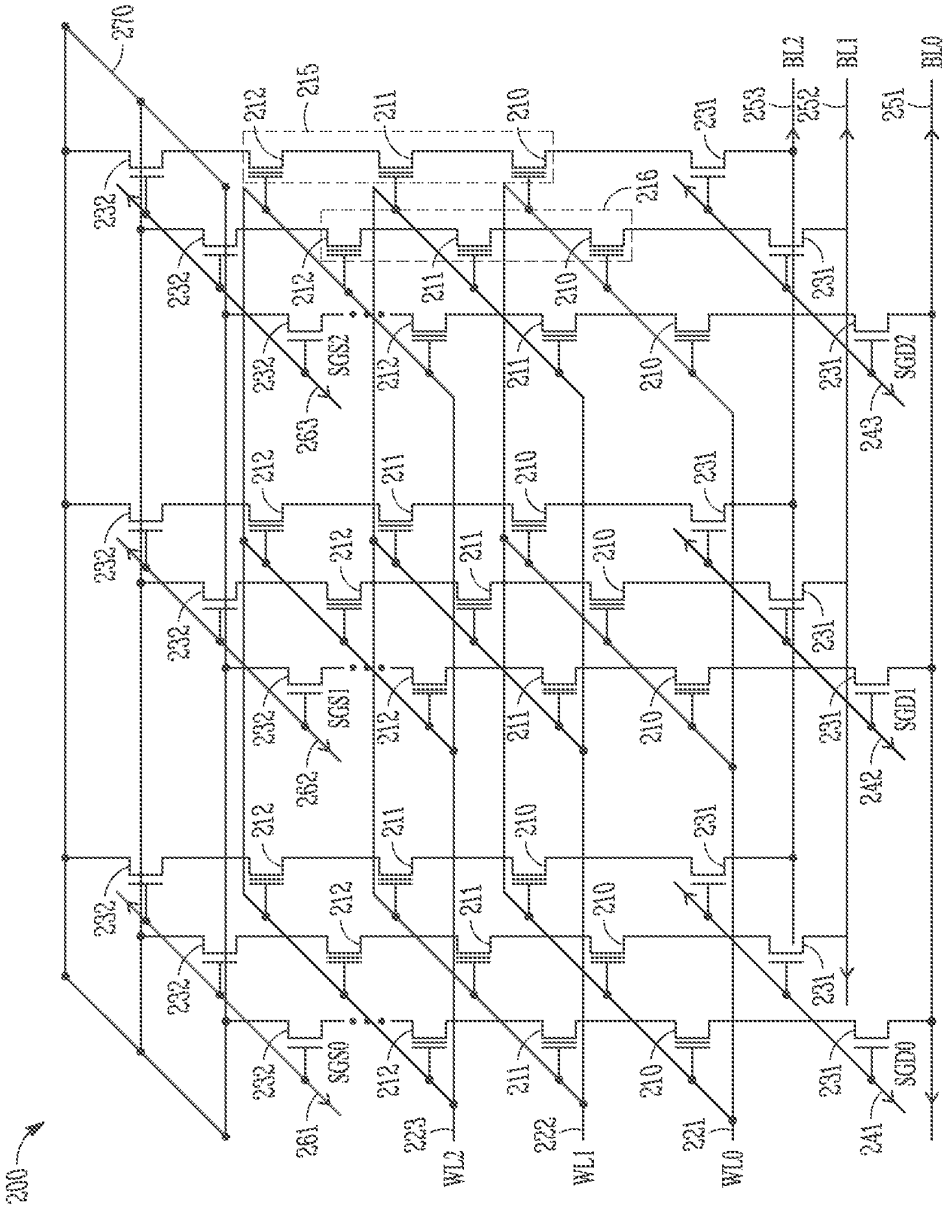

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270
215
216
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BL1
BL0
WL2
WL1
WL0
SGS2
SGS1
SGS0
SGD2
SGD1
SGD0

FIG. 2

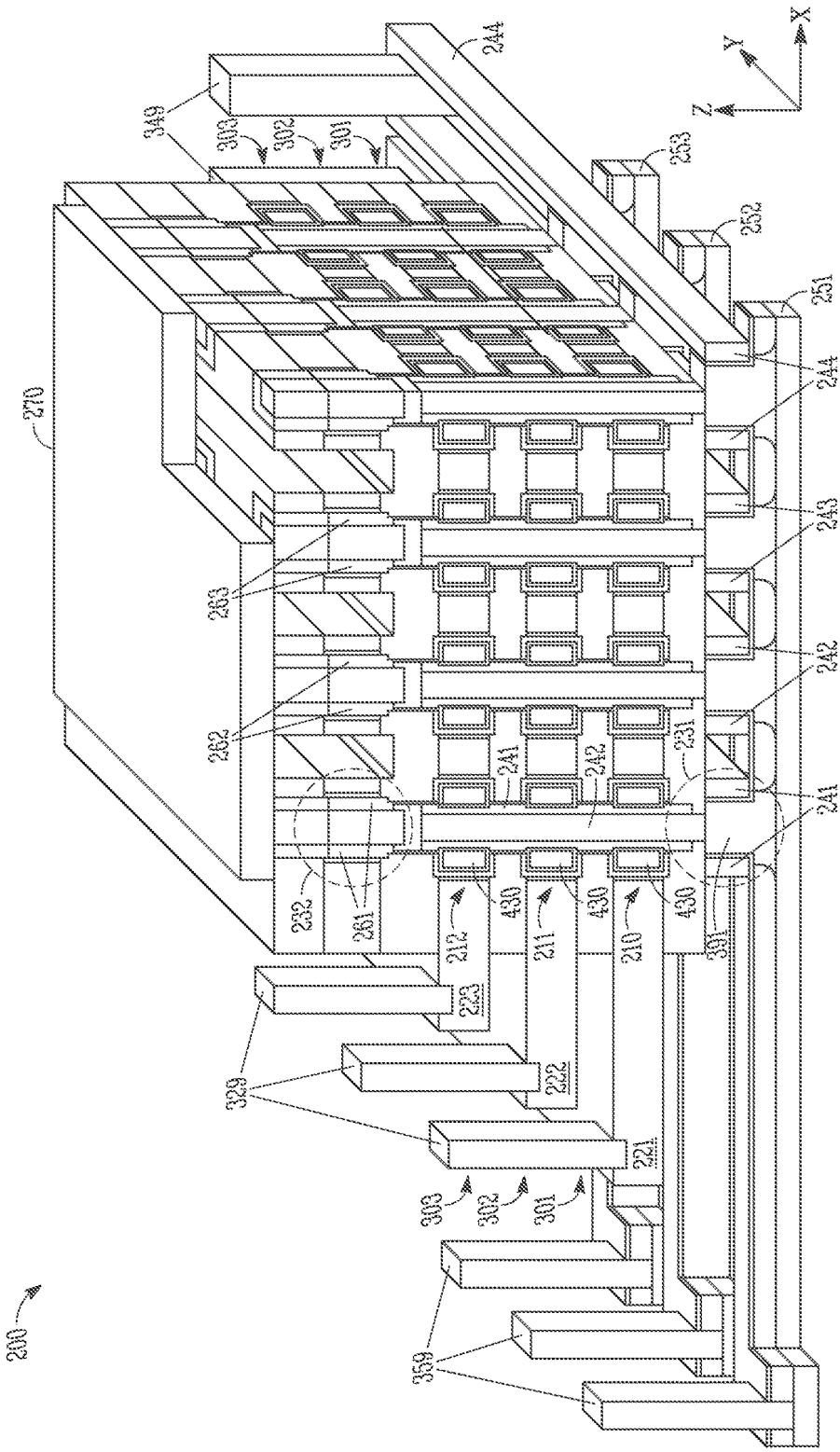

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Y
Z
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349
303
302
301
253
252
251
270
244
243
263
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262
231
241
242
241
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391
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329
221
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302
301
359
200

FIG. 3

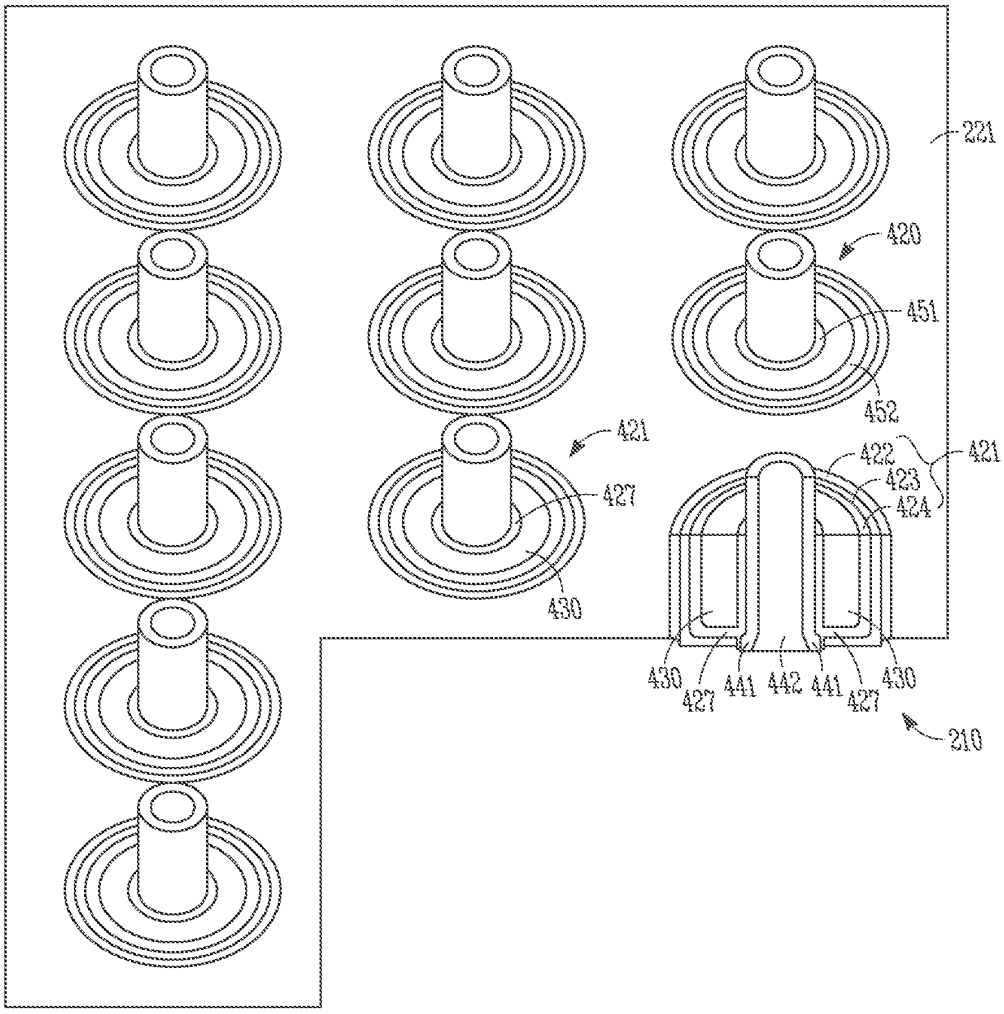

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427
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210

FIG. 4

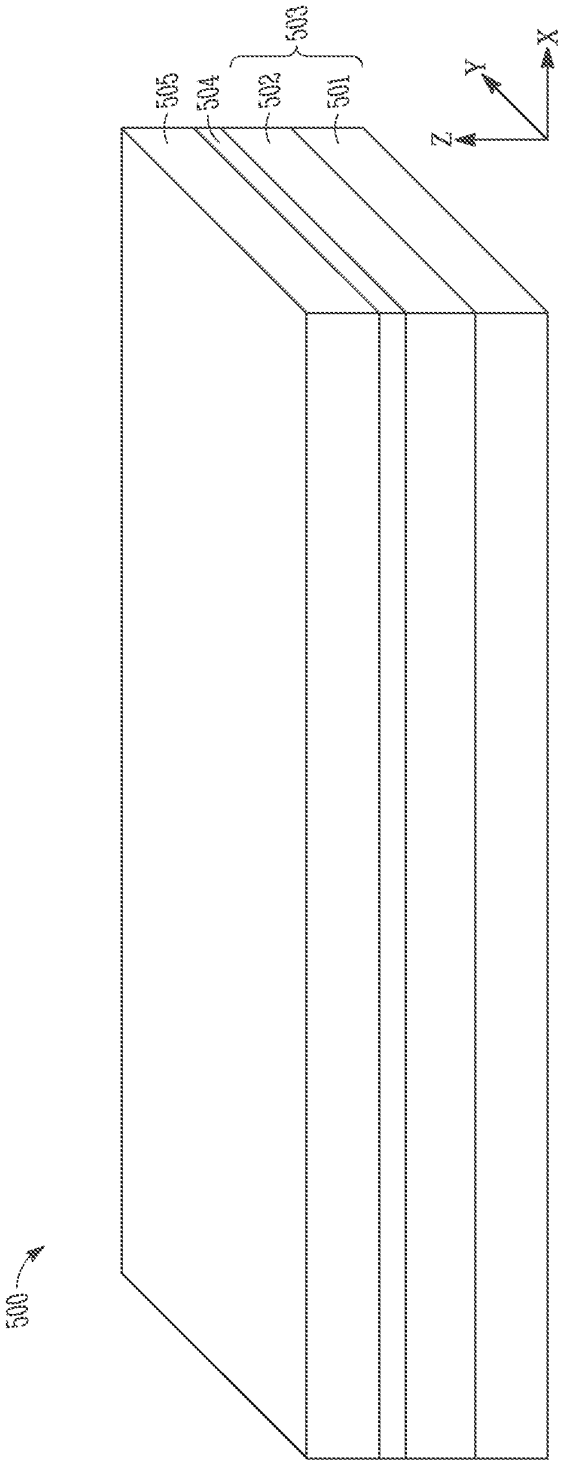


FIG. 5

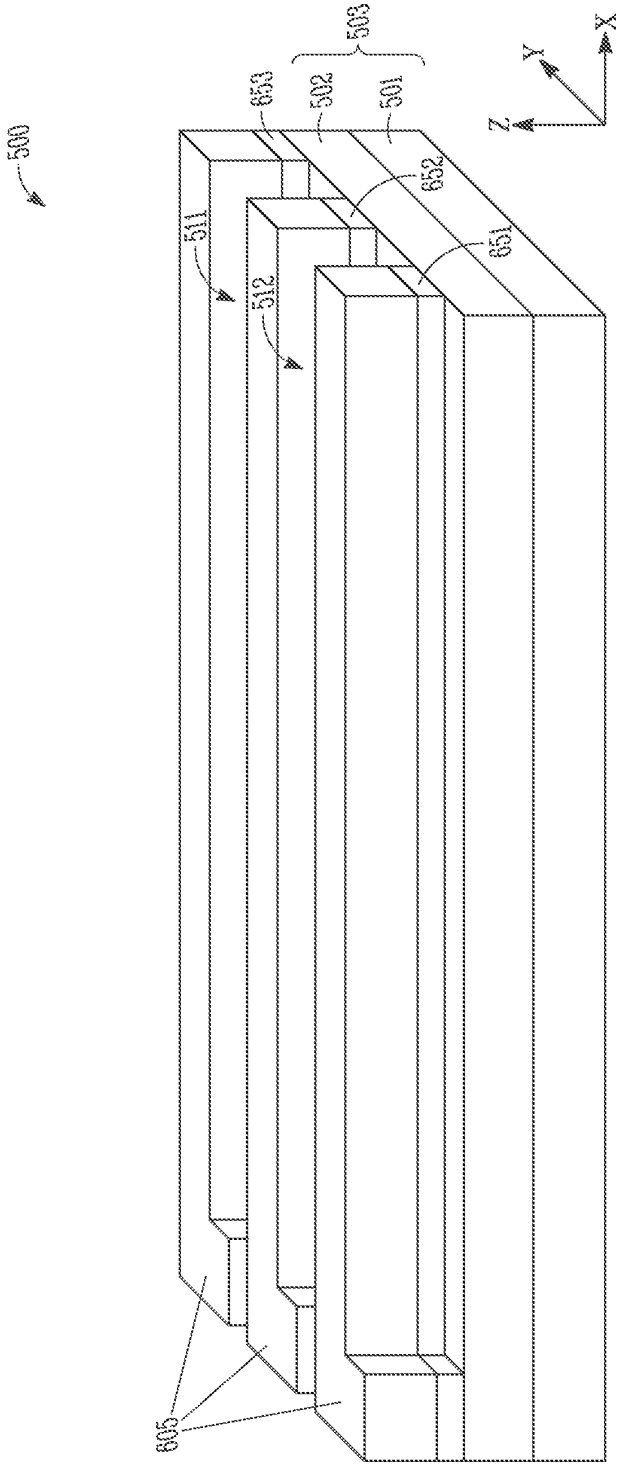


FIG. 6

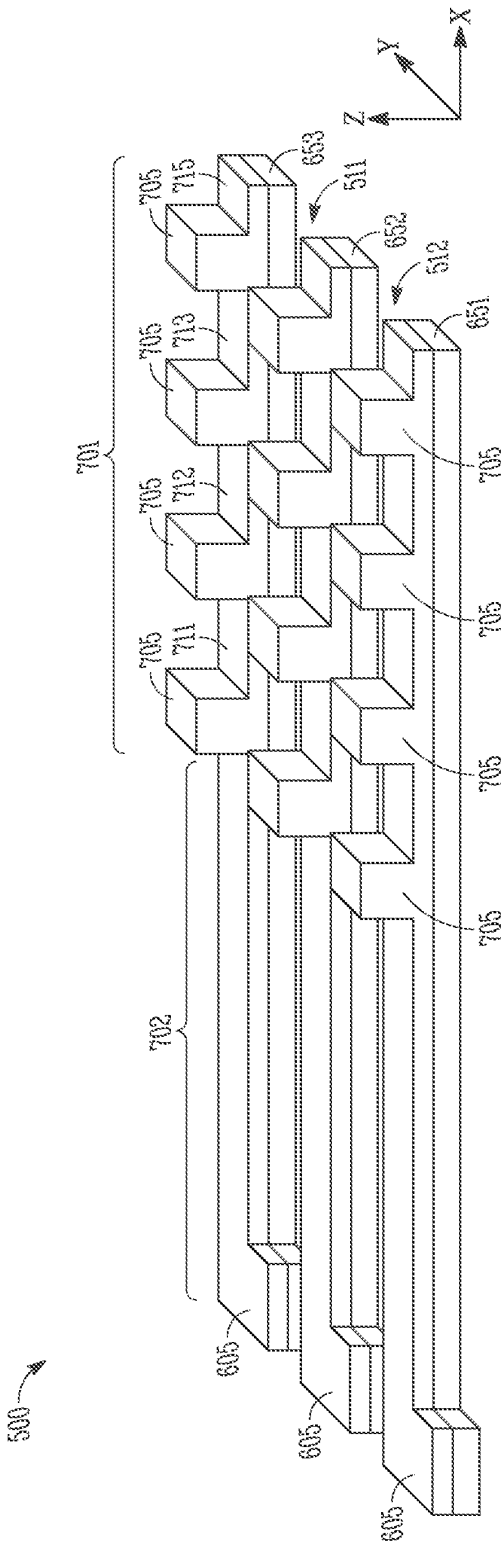


FIG. 7

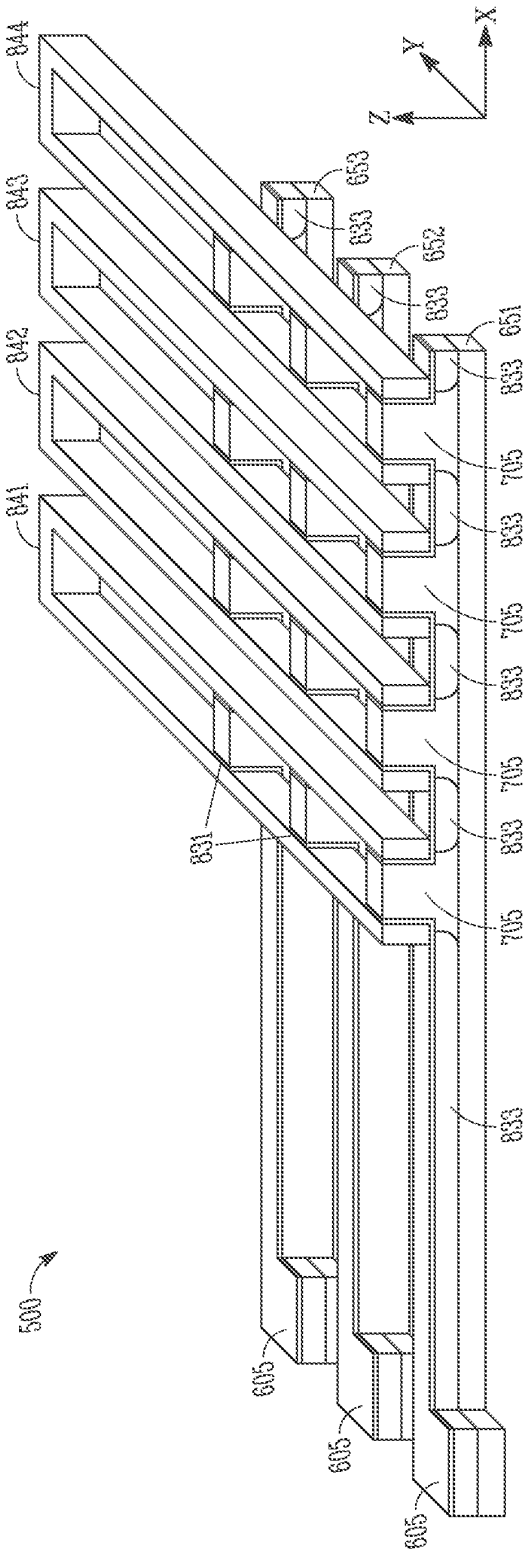


FIG. 8

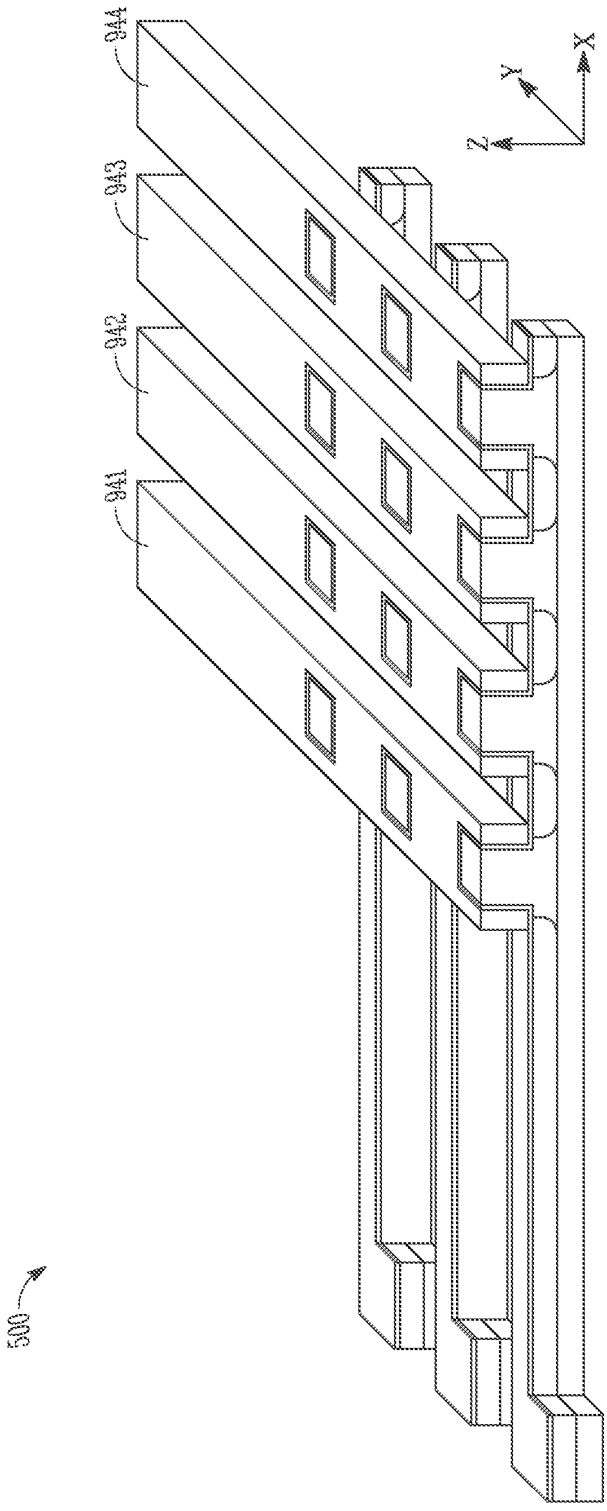


FIG. 9

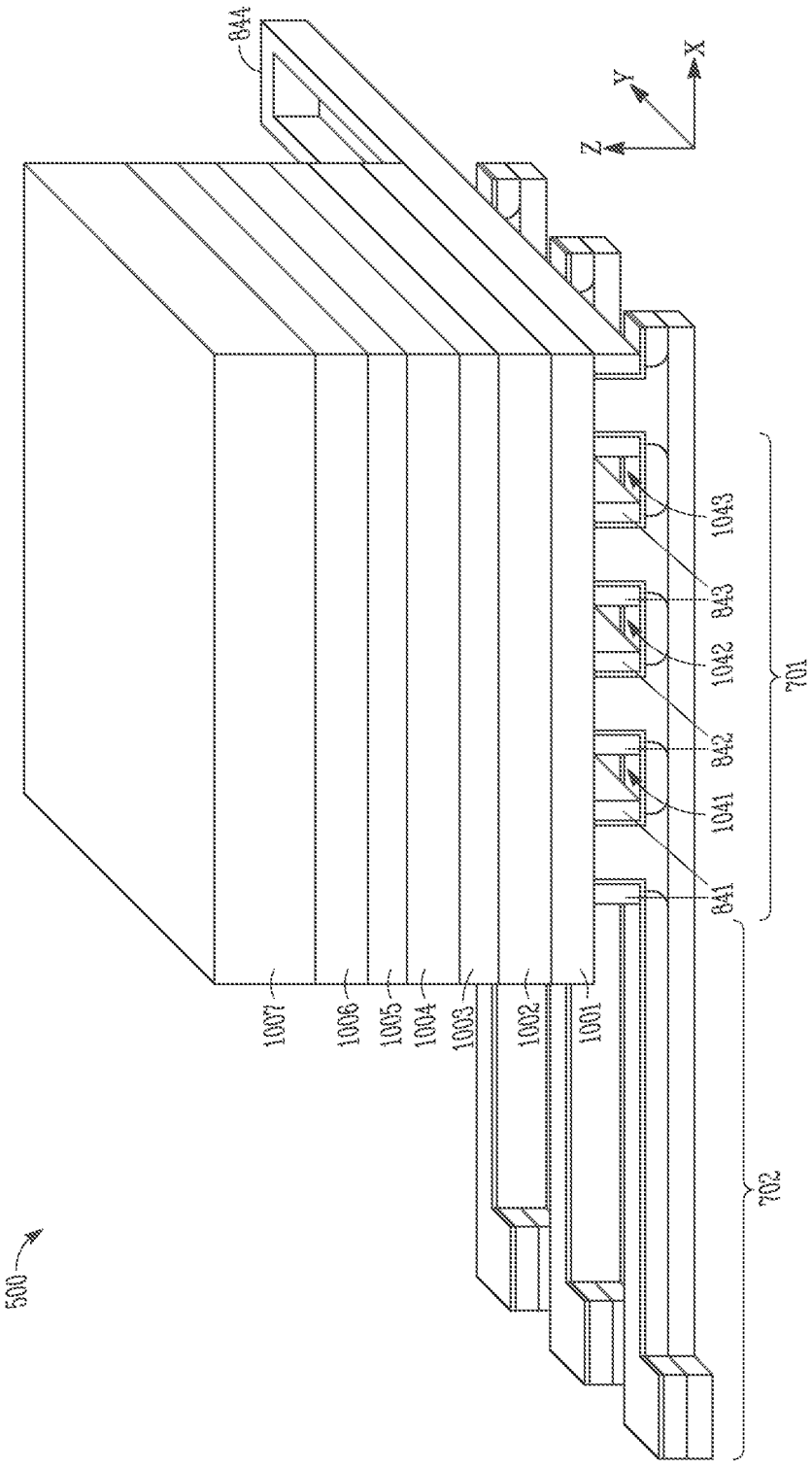

844
Y
X
Z
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843
1042
842
1041
841
701
1007
1006
1005
1004
1003
1002
1001
702
500

FIG. 10

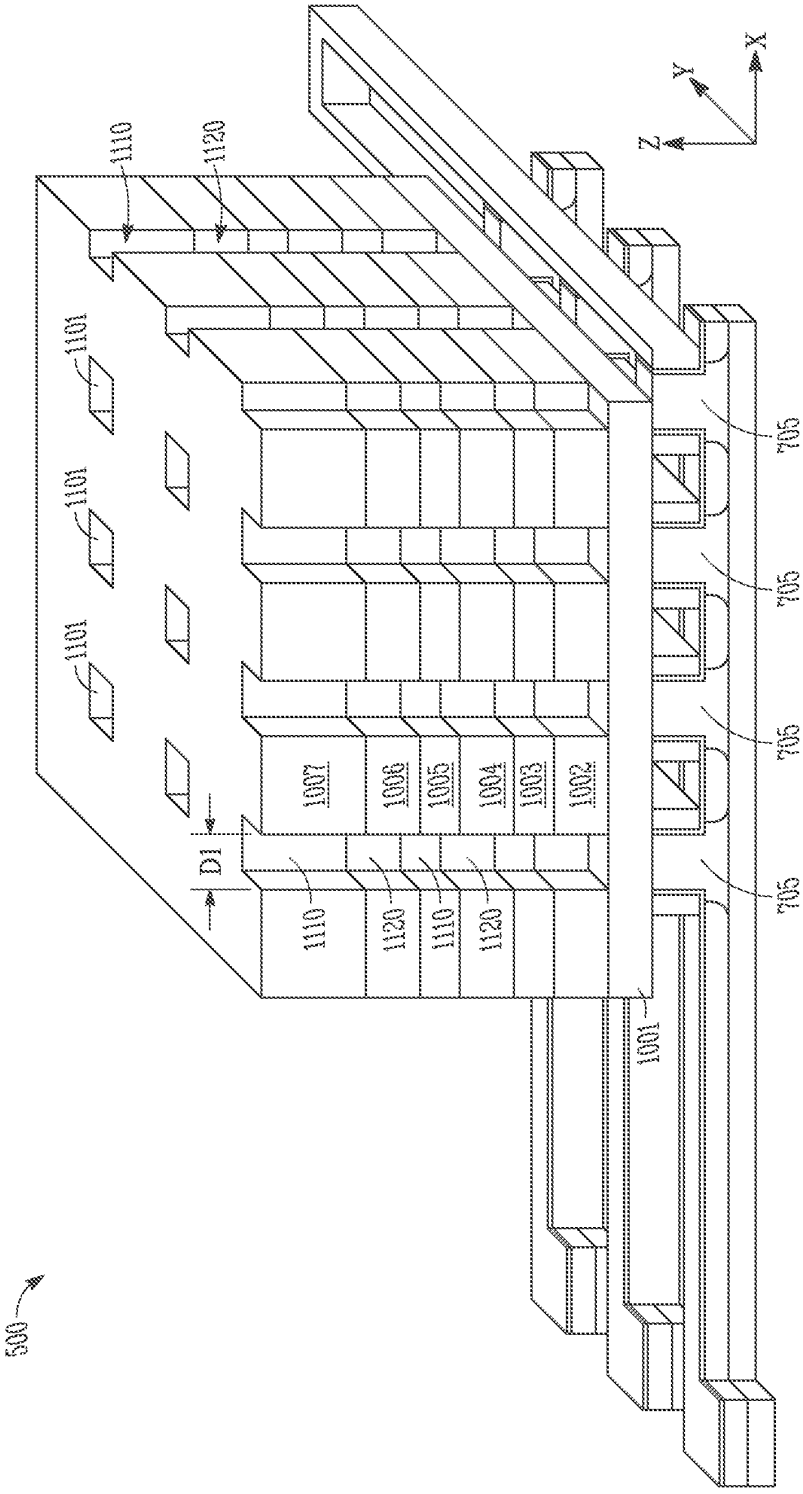

X
Y
Z
1110
1120
1101
1101
1101
705
705
705
705
1007
1006
1005
1004
1003
1002
D1
1110
1120
1110
1120
1001
500

FIG. 11

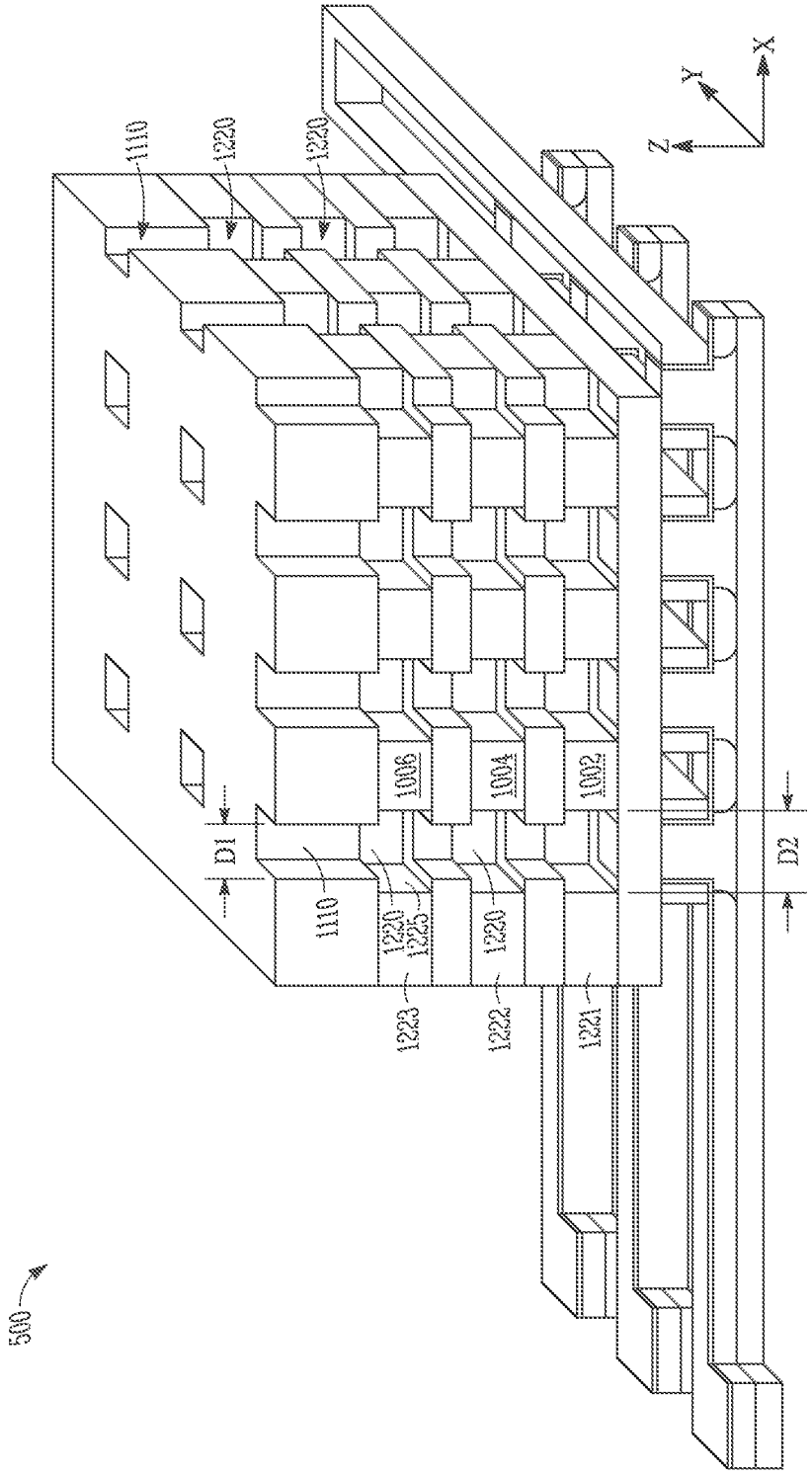

X
Y
Z
1110
1220
1220
1006
1004
1002
D1
D2
1110
1220
1225
1220
1223
1222
1221
500

FIG. 12

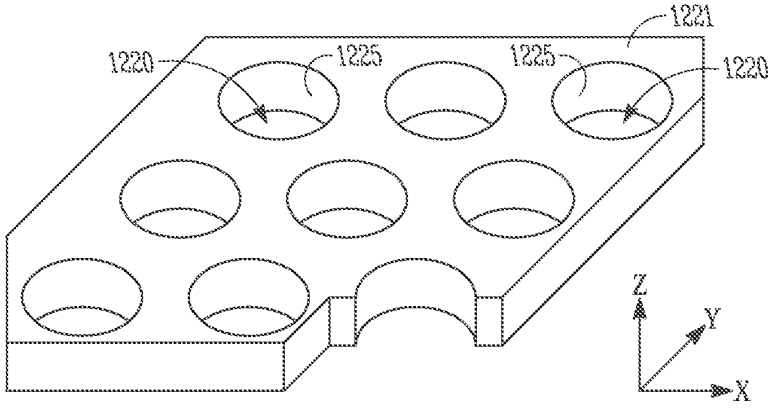


FIG. 13

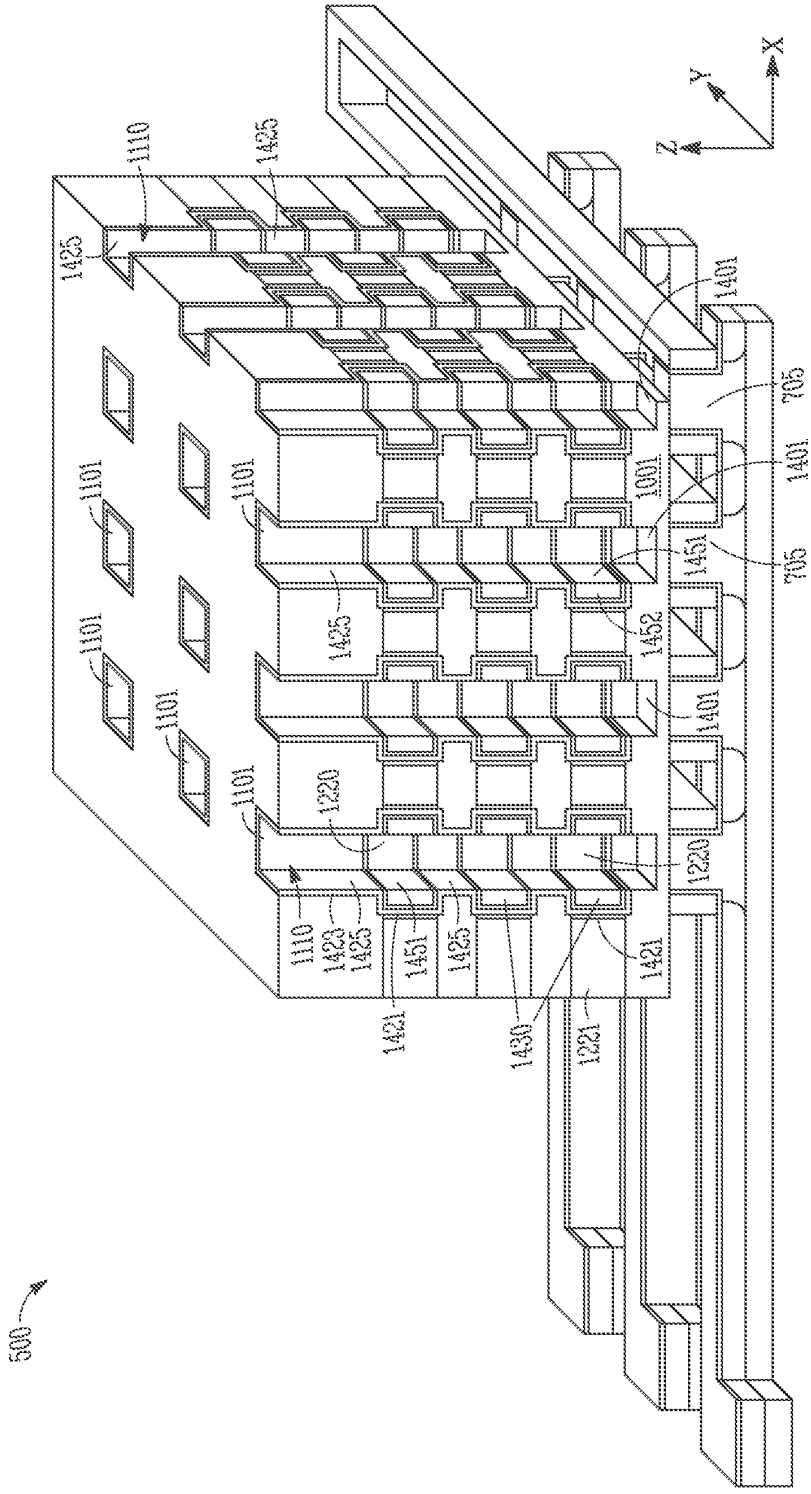

X
Y
Z
1110
1425
1401
705
1101
1001
1451
1452
1220
1423
1421
1430
1221
500

FIG. 14

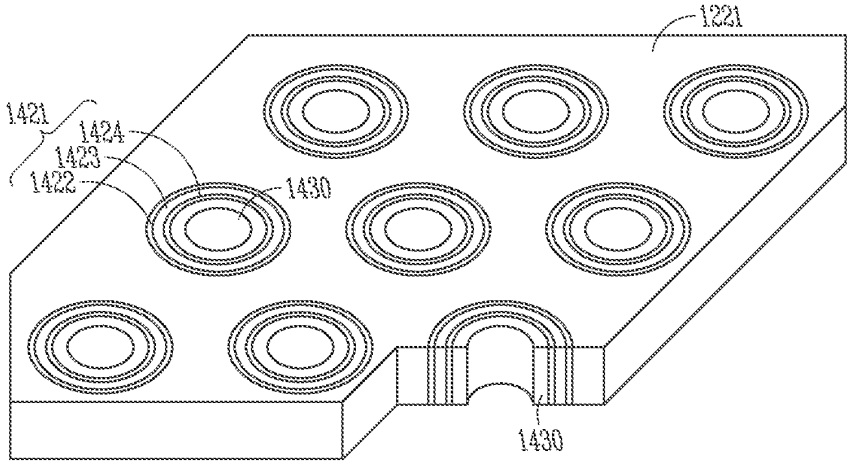


FIG. 15

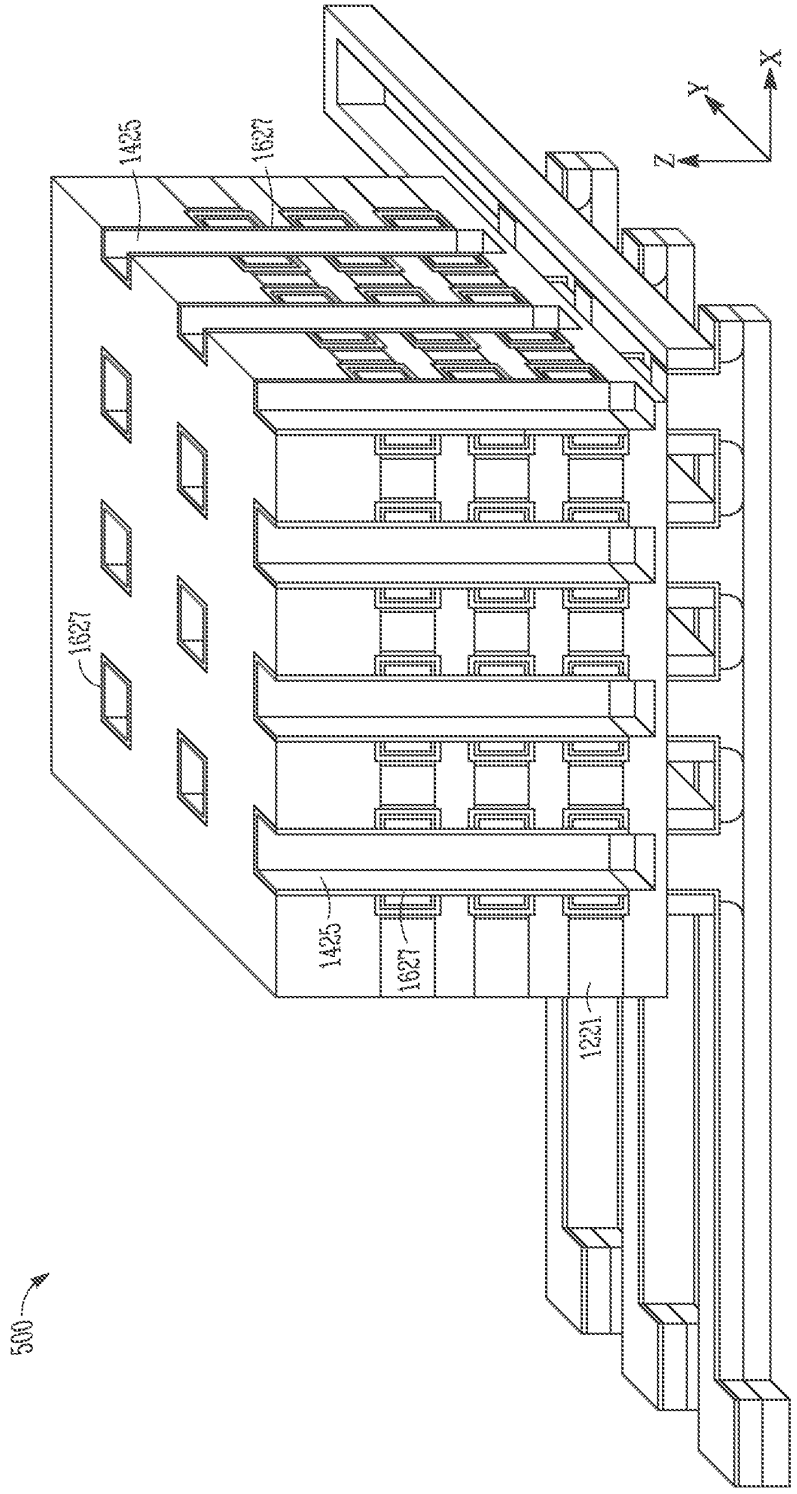


FIG. 16

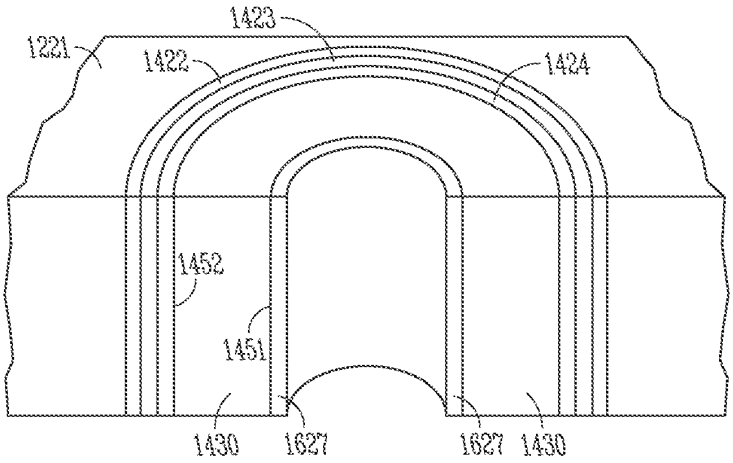


FIG. 17

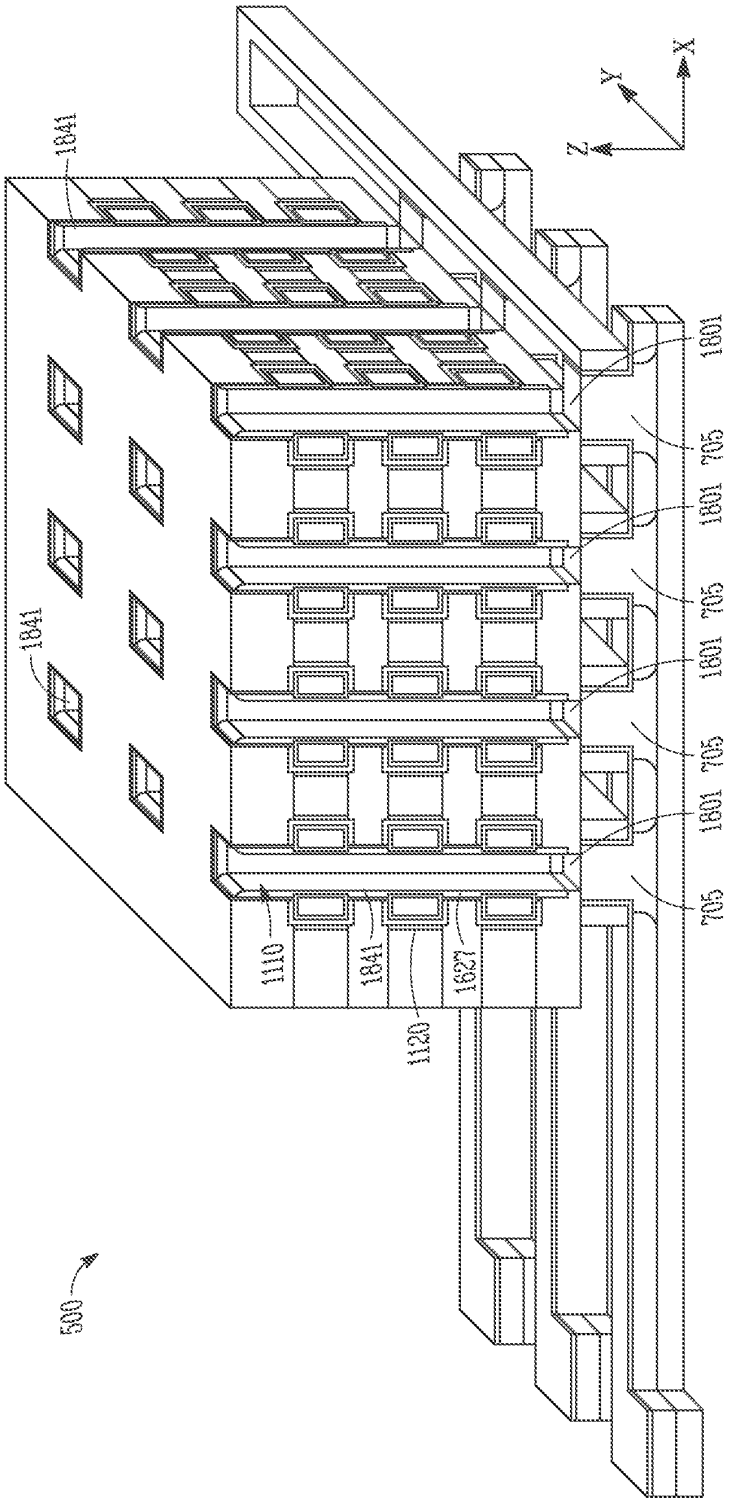

X
Y
Z
1841
1801
705
1801
705
1801
705
1801
705
1841
1110
1841
1827
1120
500

FIG. 18

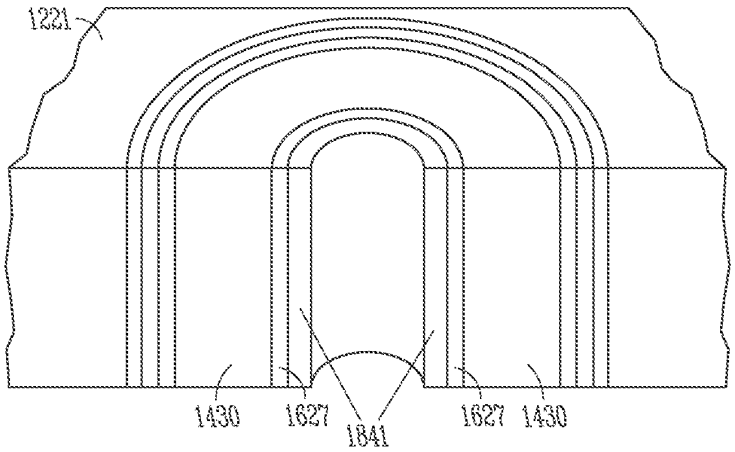


FIG. 19

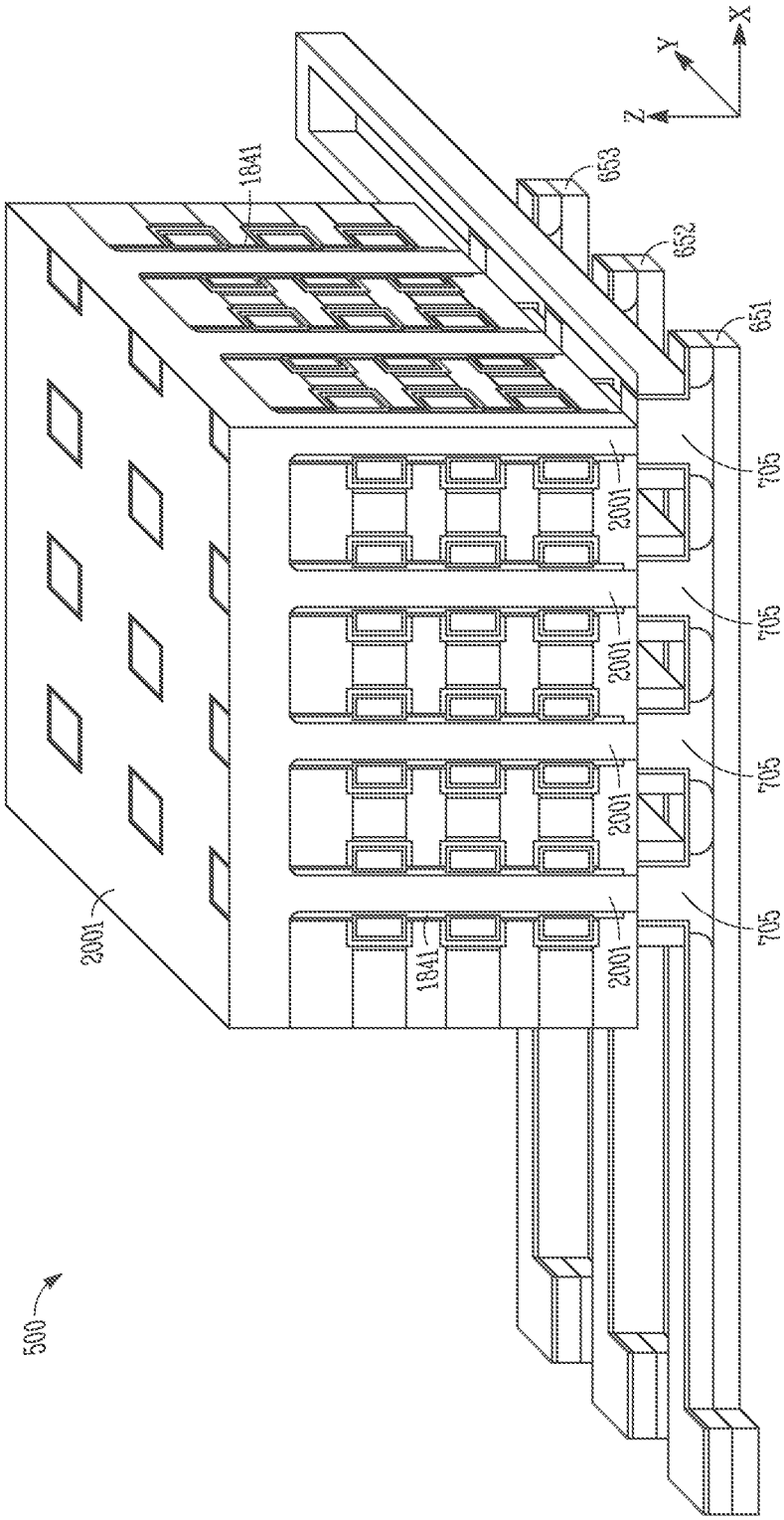


FIG. 20

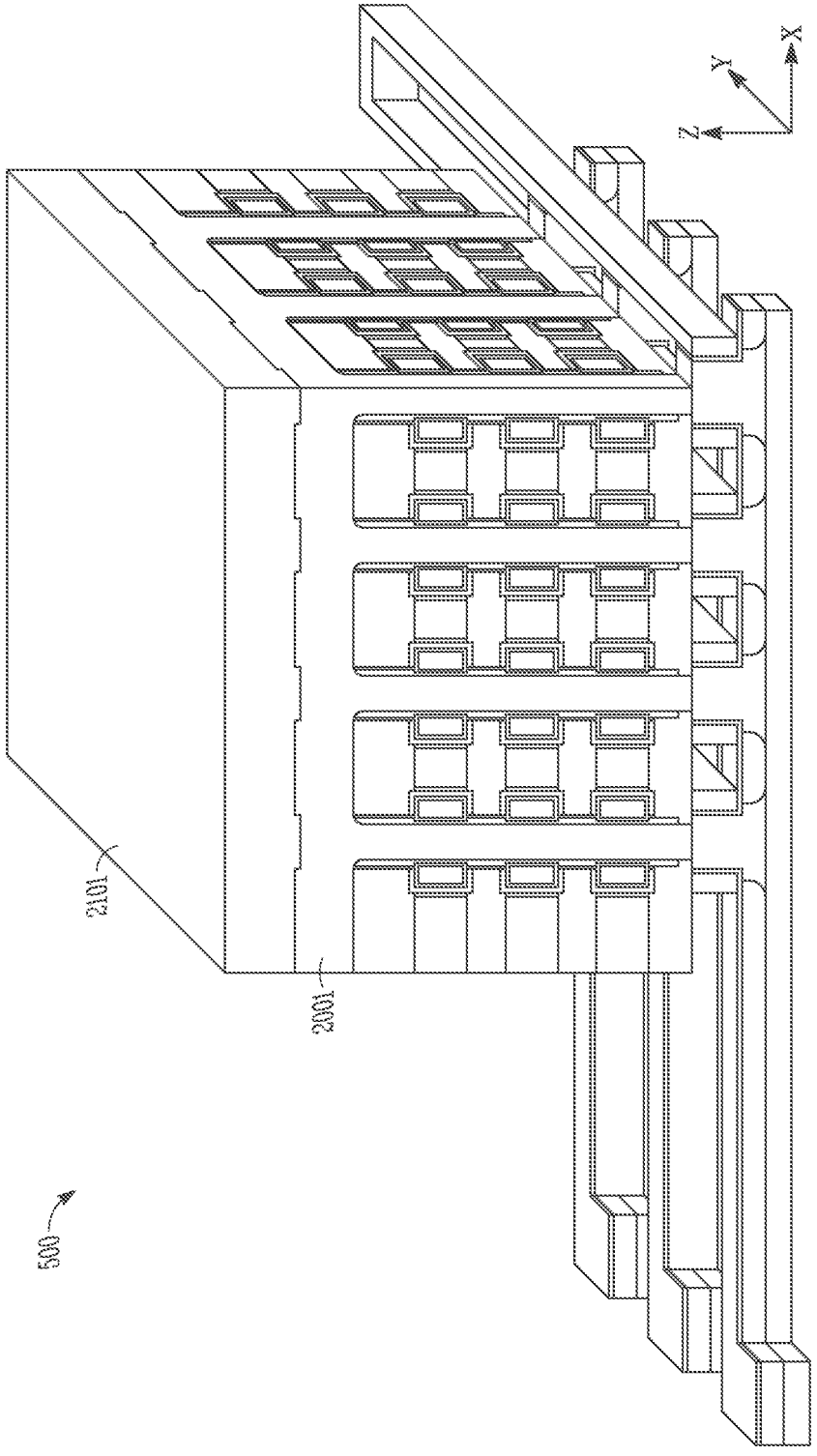


FIG. 21

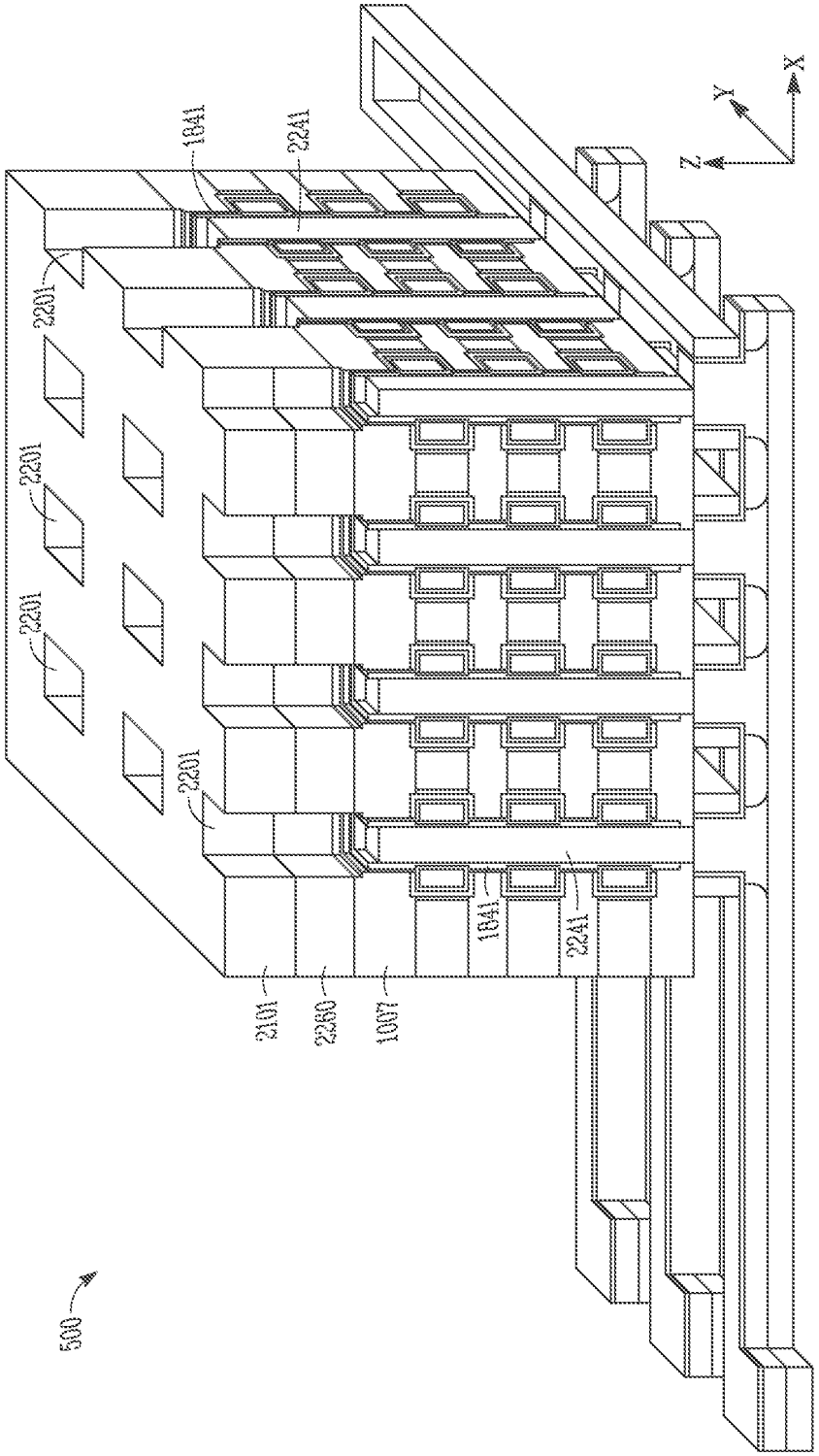

1041
2241
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2201
2201
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1041
2241
3101
2380
1007
500
X
Y
Z

FIG. 22

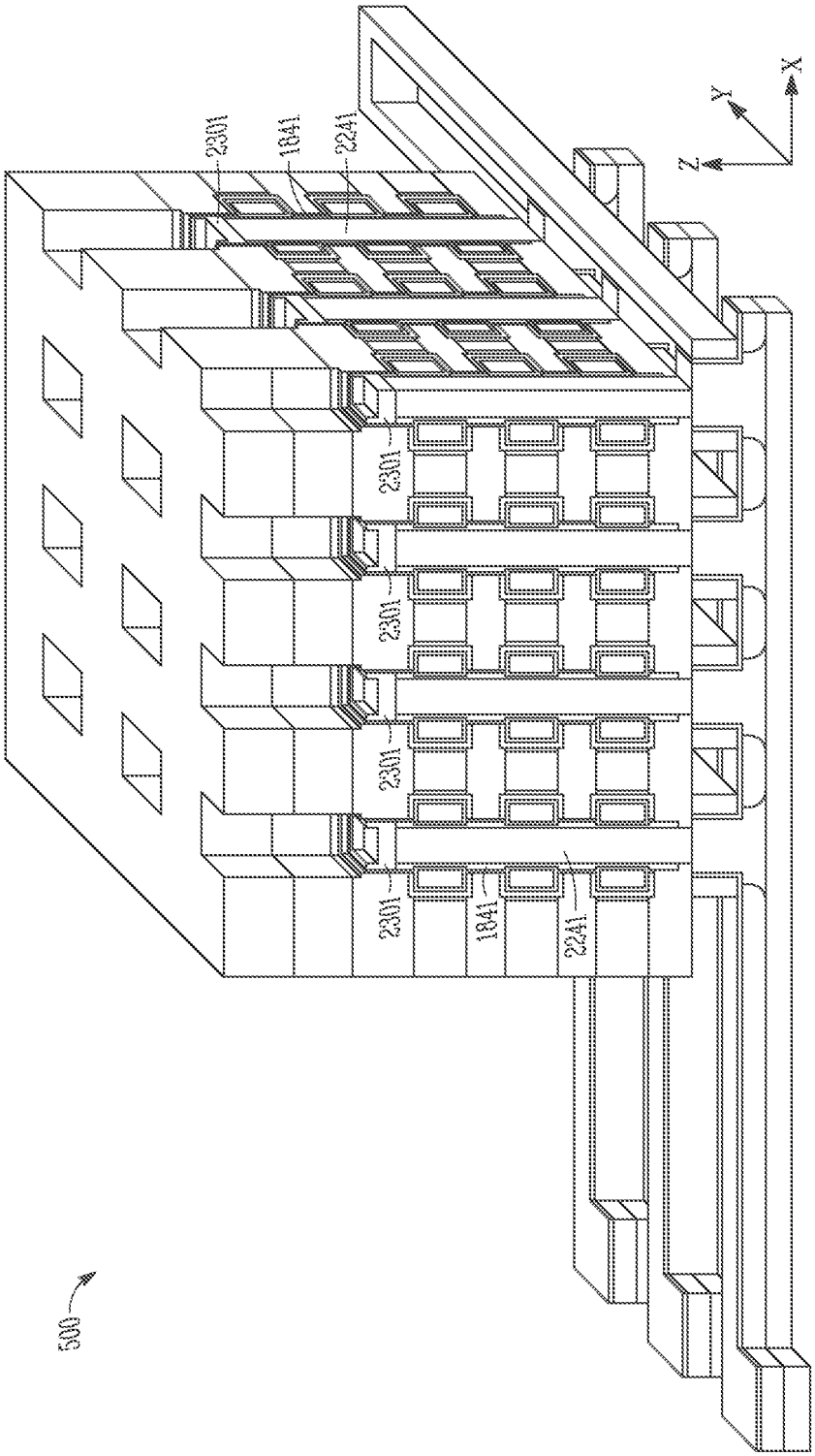


FIG. 23

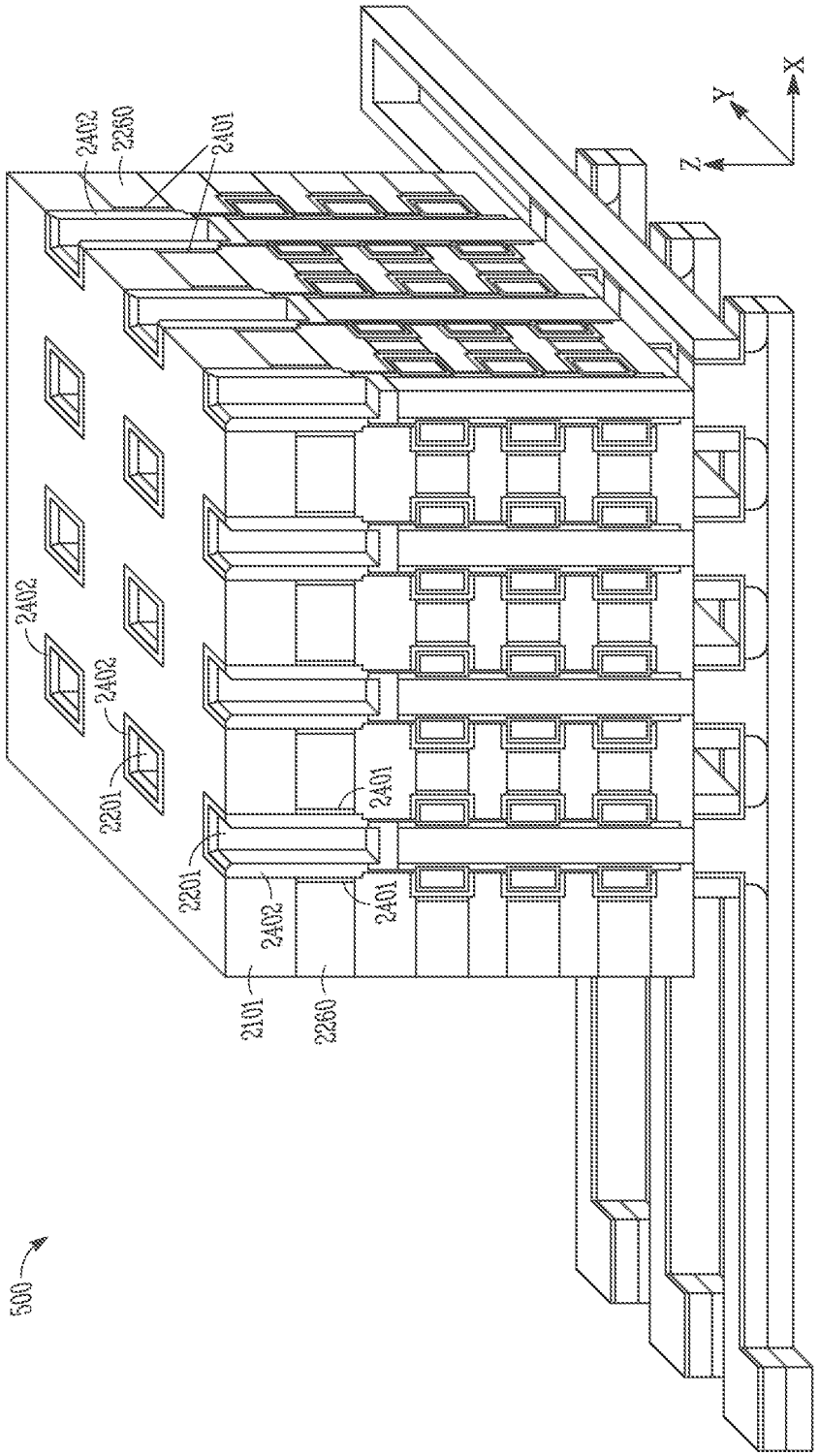

X
Y
Z
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2260
2401
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2402
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2101
2260
500

FIG. 24

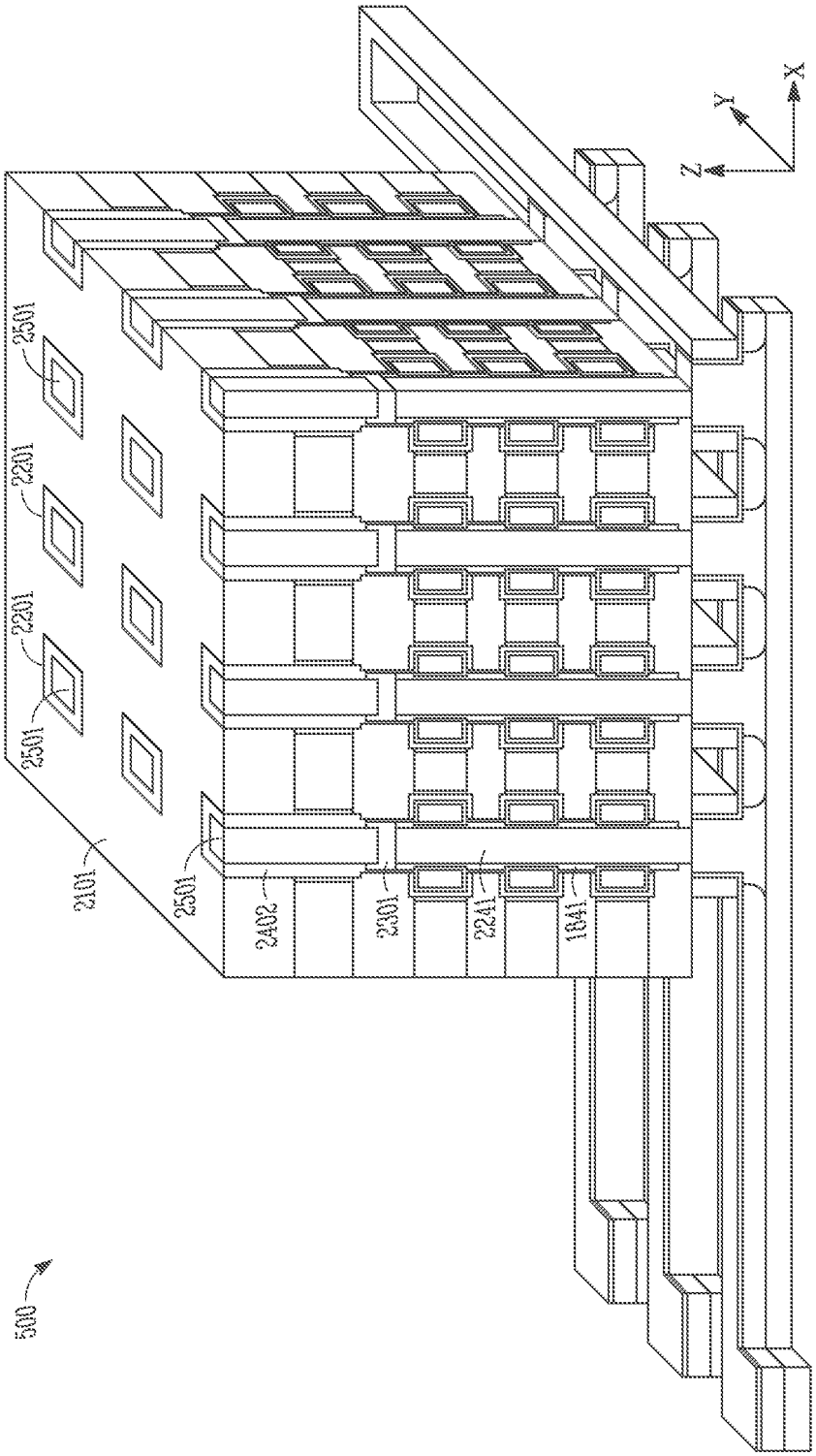


FIG. 25

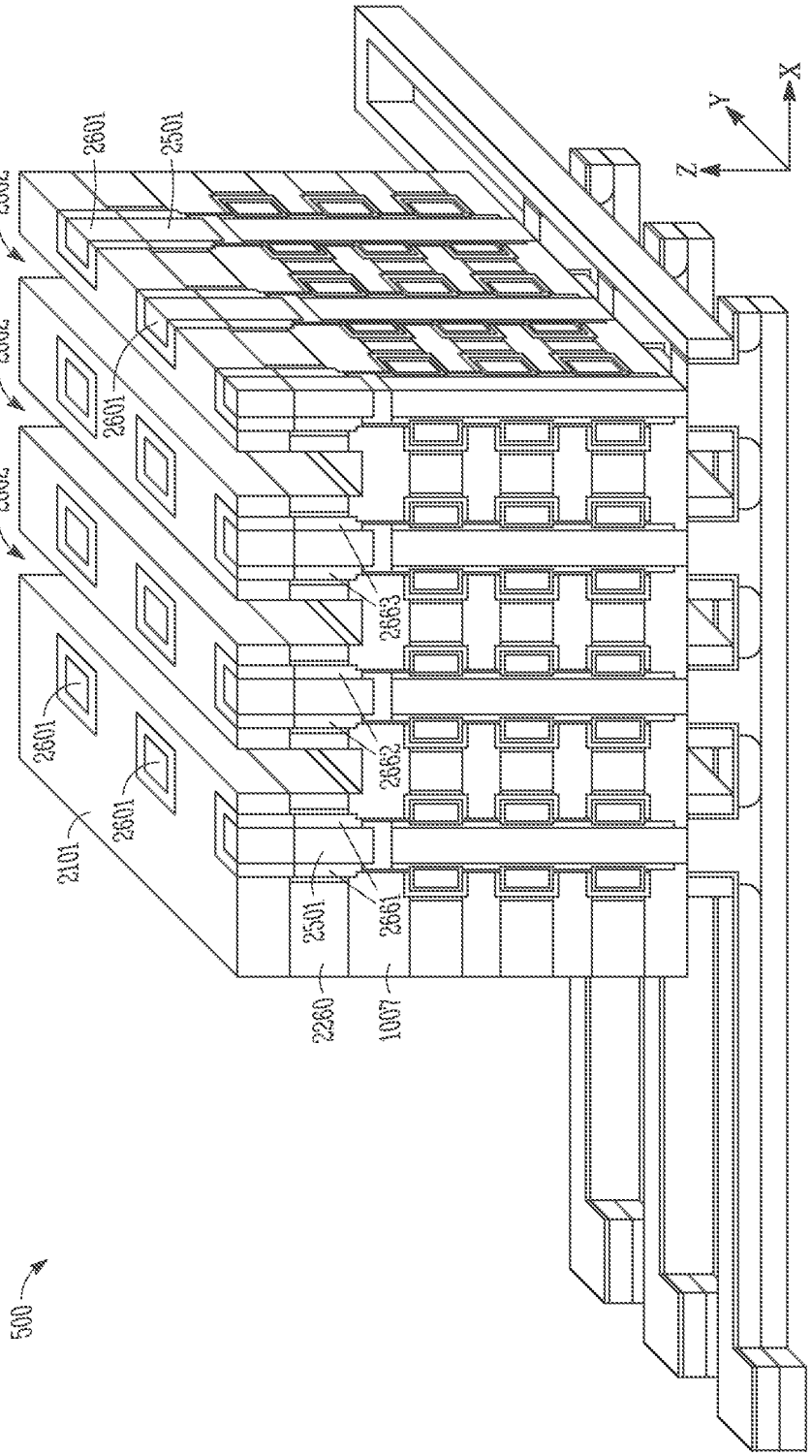

X
Y
Z
2601
2501
2602
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2501
2661
2260
1007
500

FIG. 26

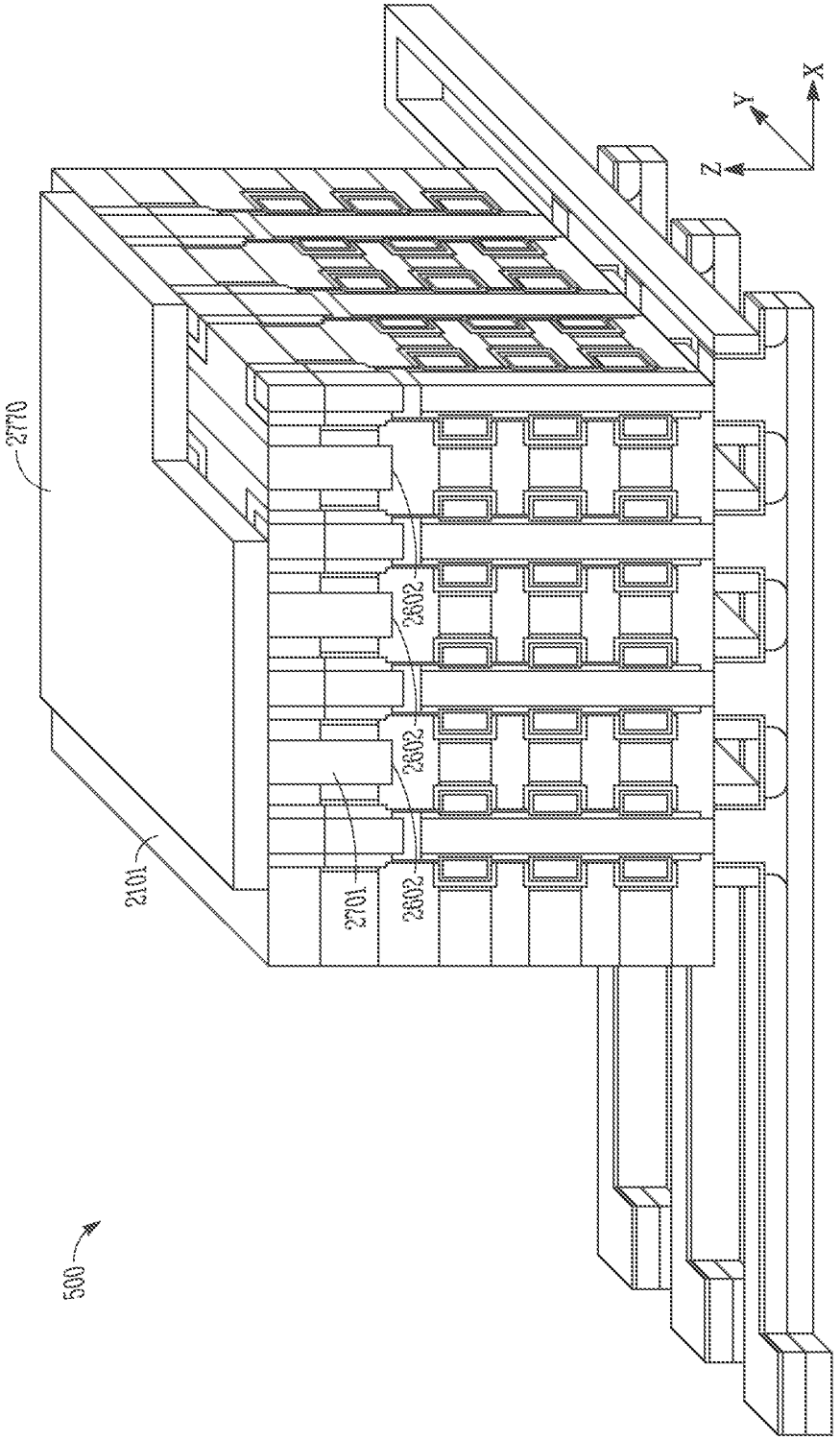


FIG. 27

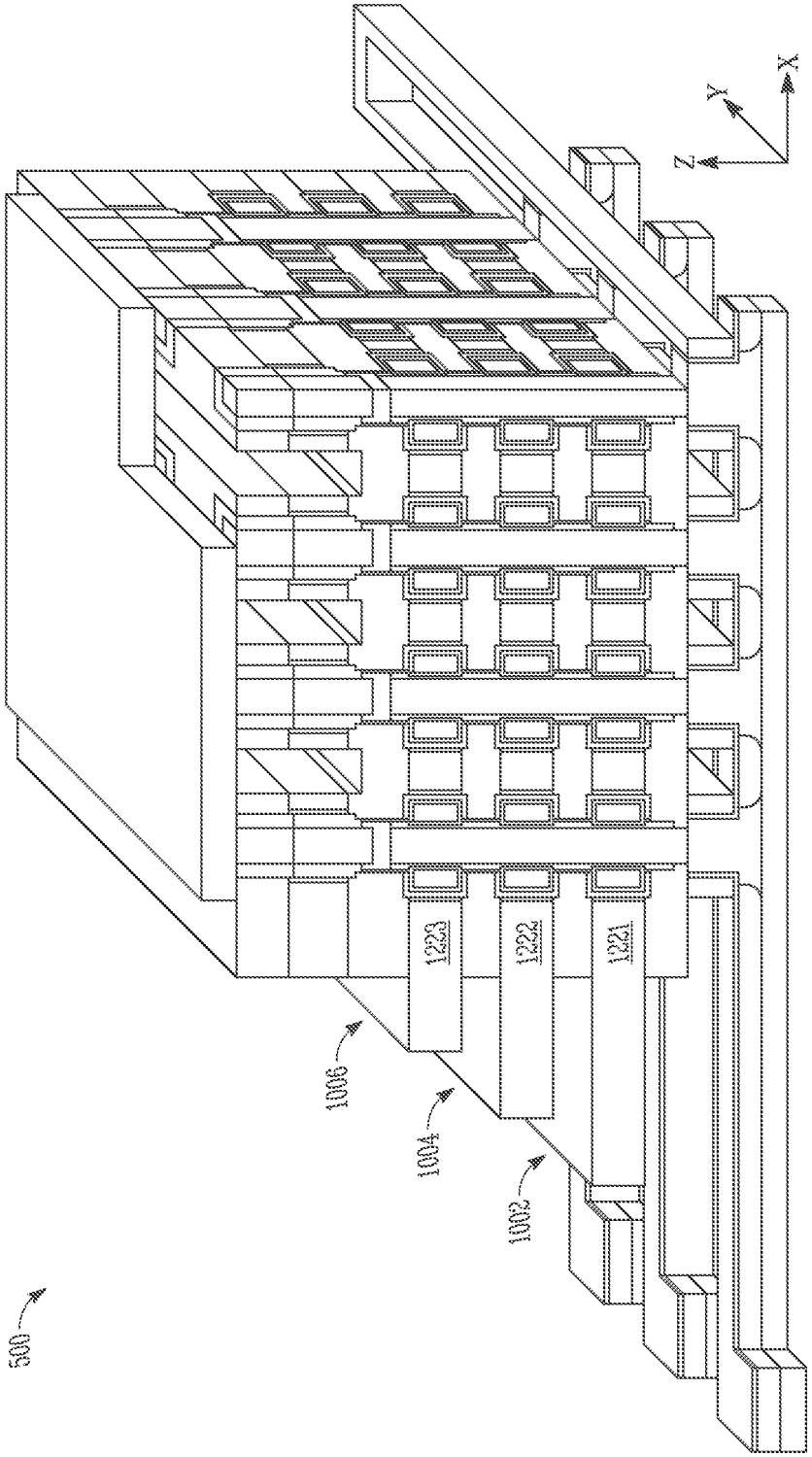


FIG. 28

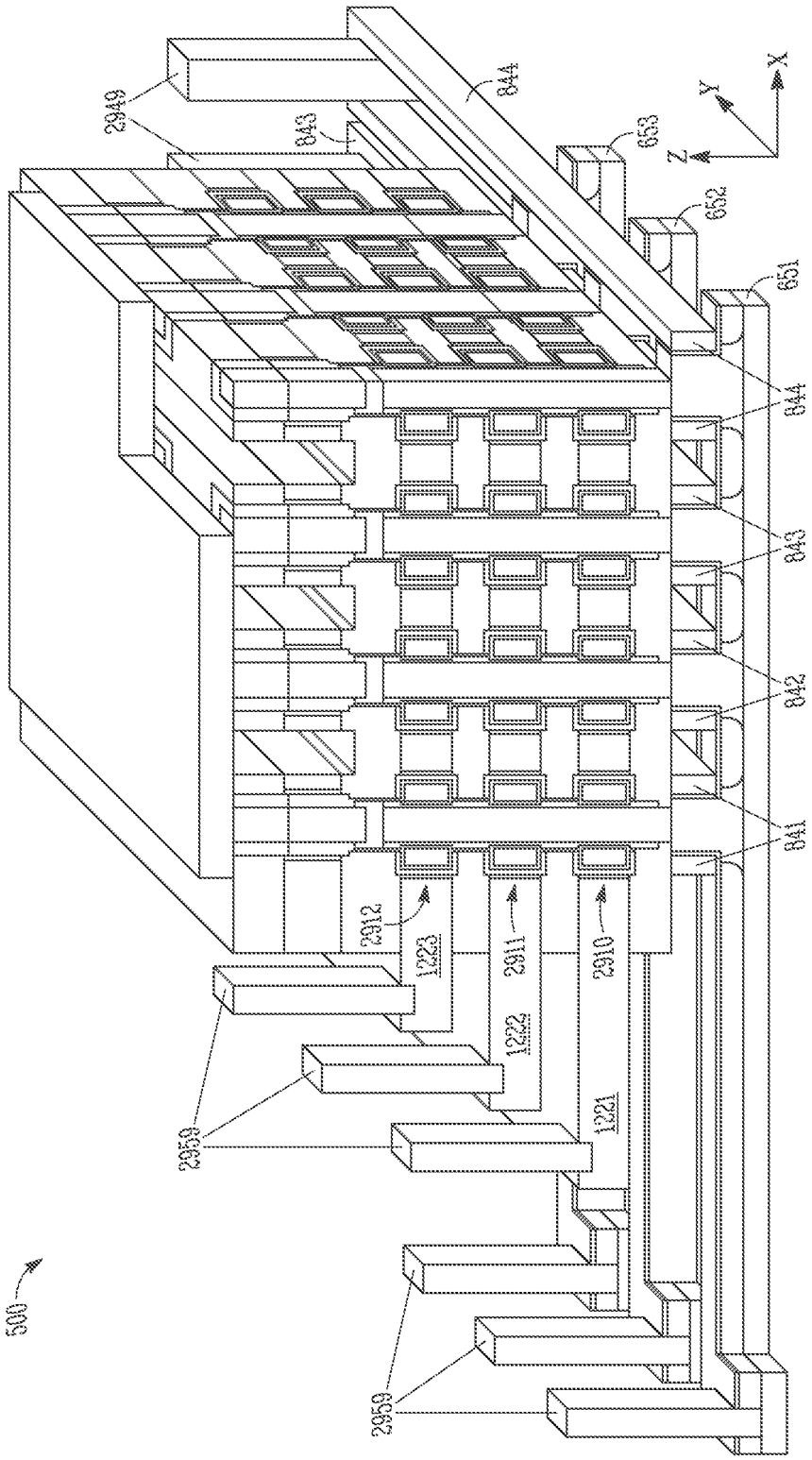

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651
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2939
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6982

FIG. 29

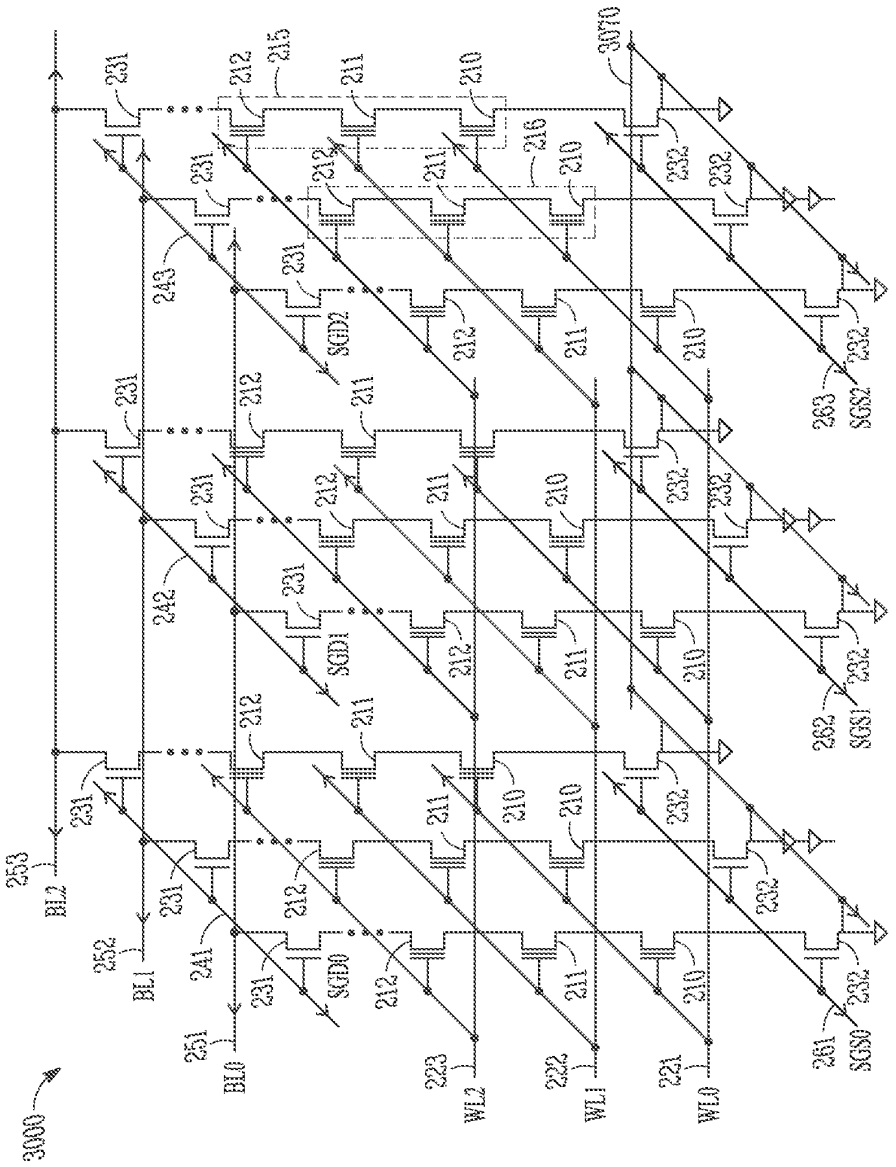

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263
SGS2
262
SGS1
261
SGS0
253
BL2
252
BL1
251
BL0
223
WL2
222
WL1
221
WL0

FIG. 30

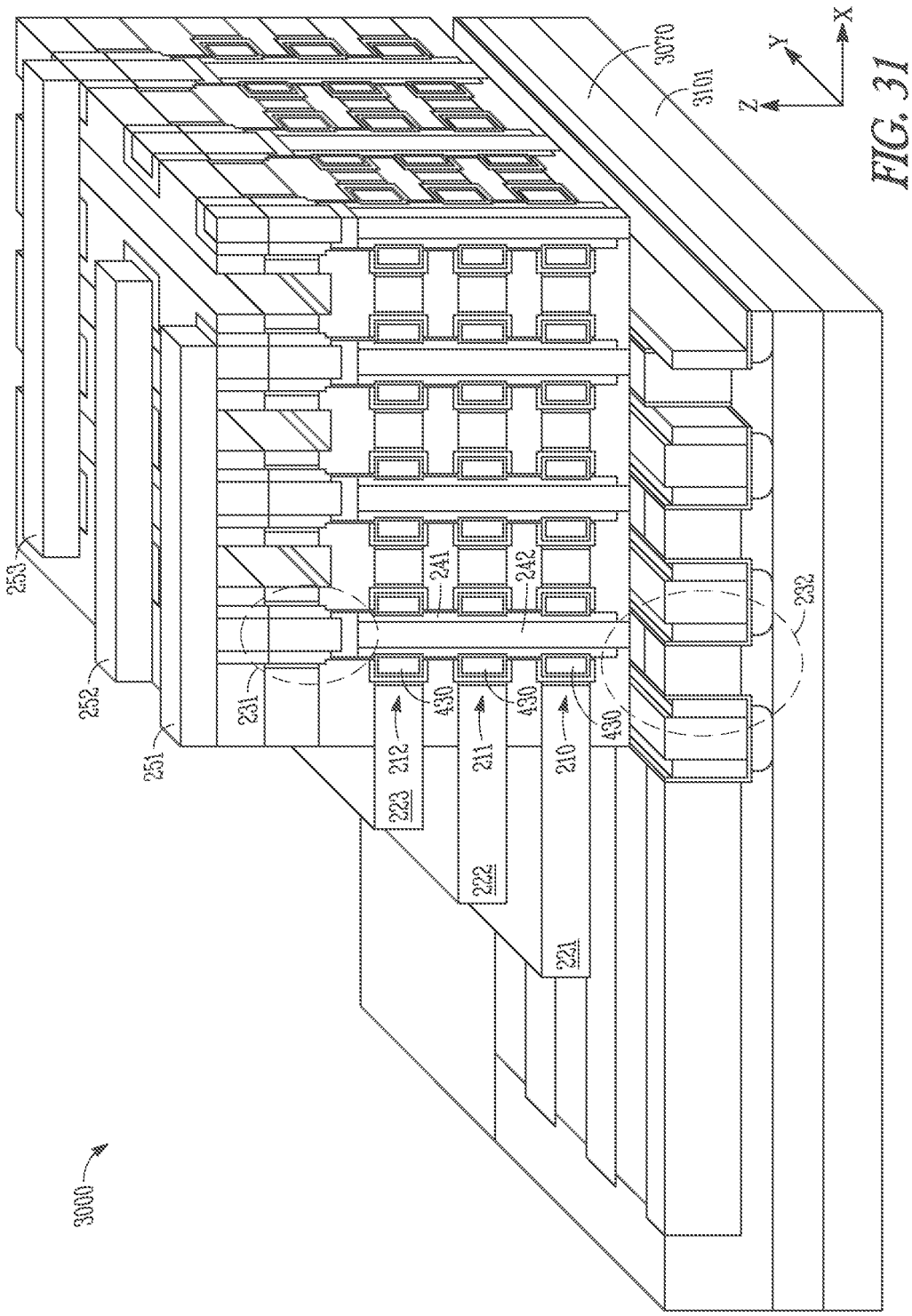

3070
3101
Y
X
Z
253
252
251
241
242
232
231
430
430
430
212
211
210
223
222
221
3000

FIG. 31

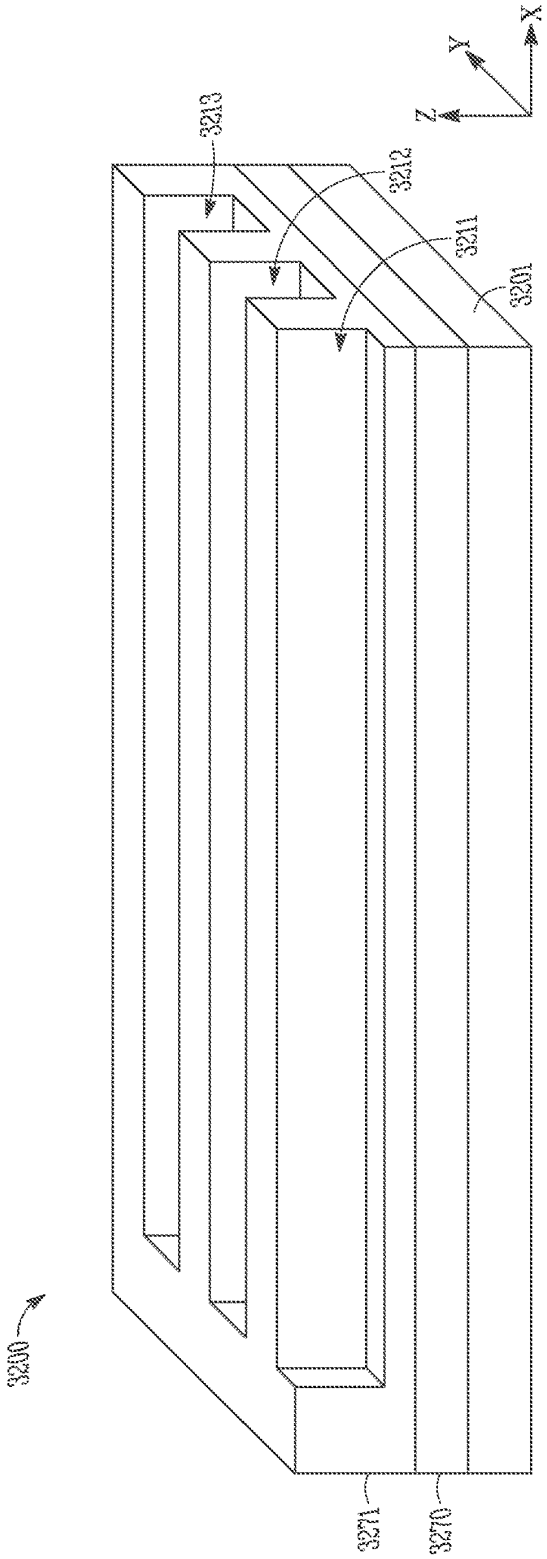


FIG. 32

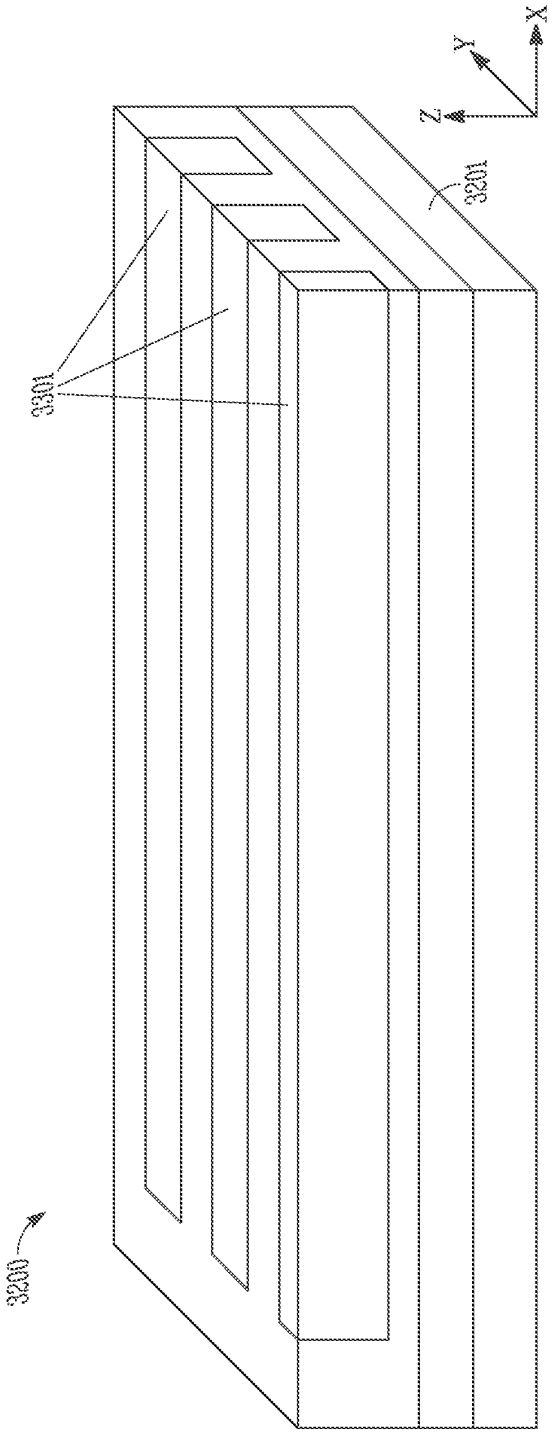


FIG. 33

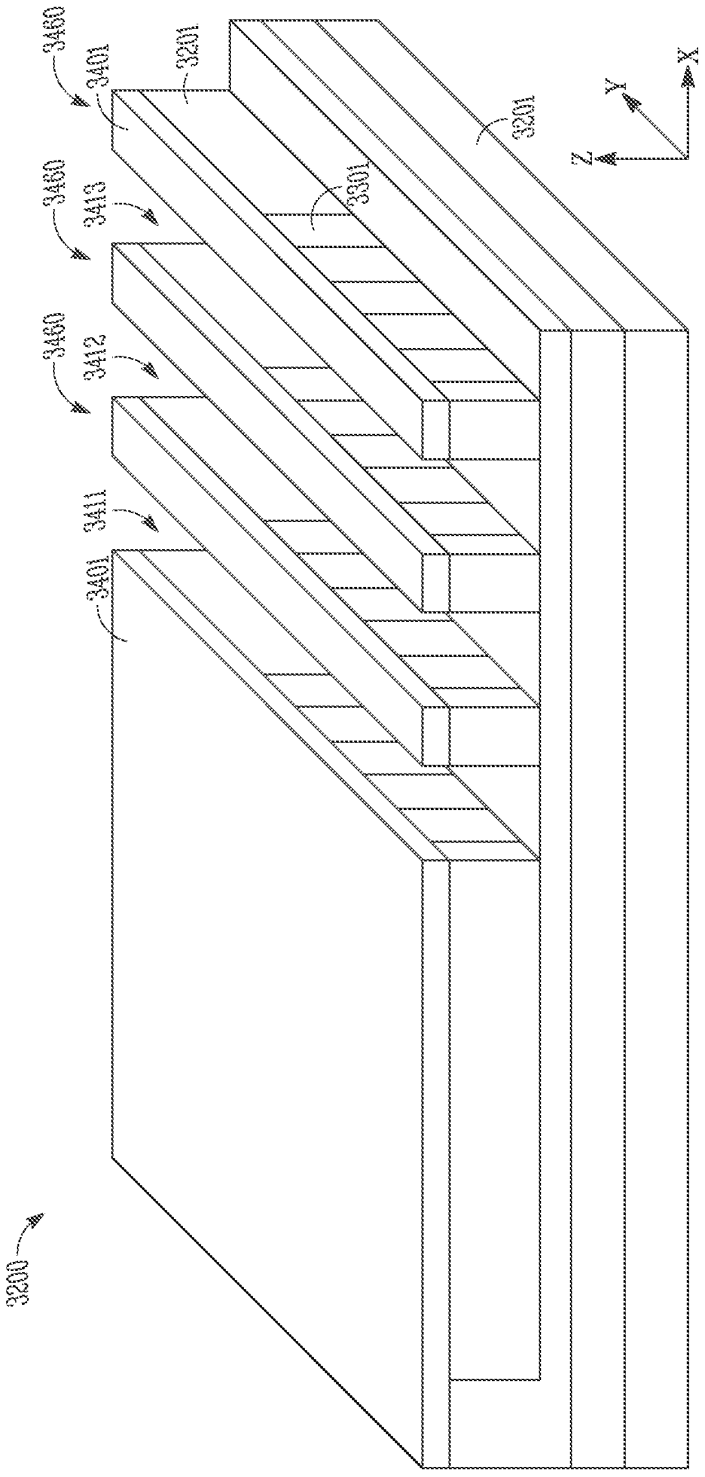

3460
3401
3201
3201
Y
X
Z
3460
3413
3301
3460
3412
3411
3401
3200

FIG. 34

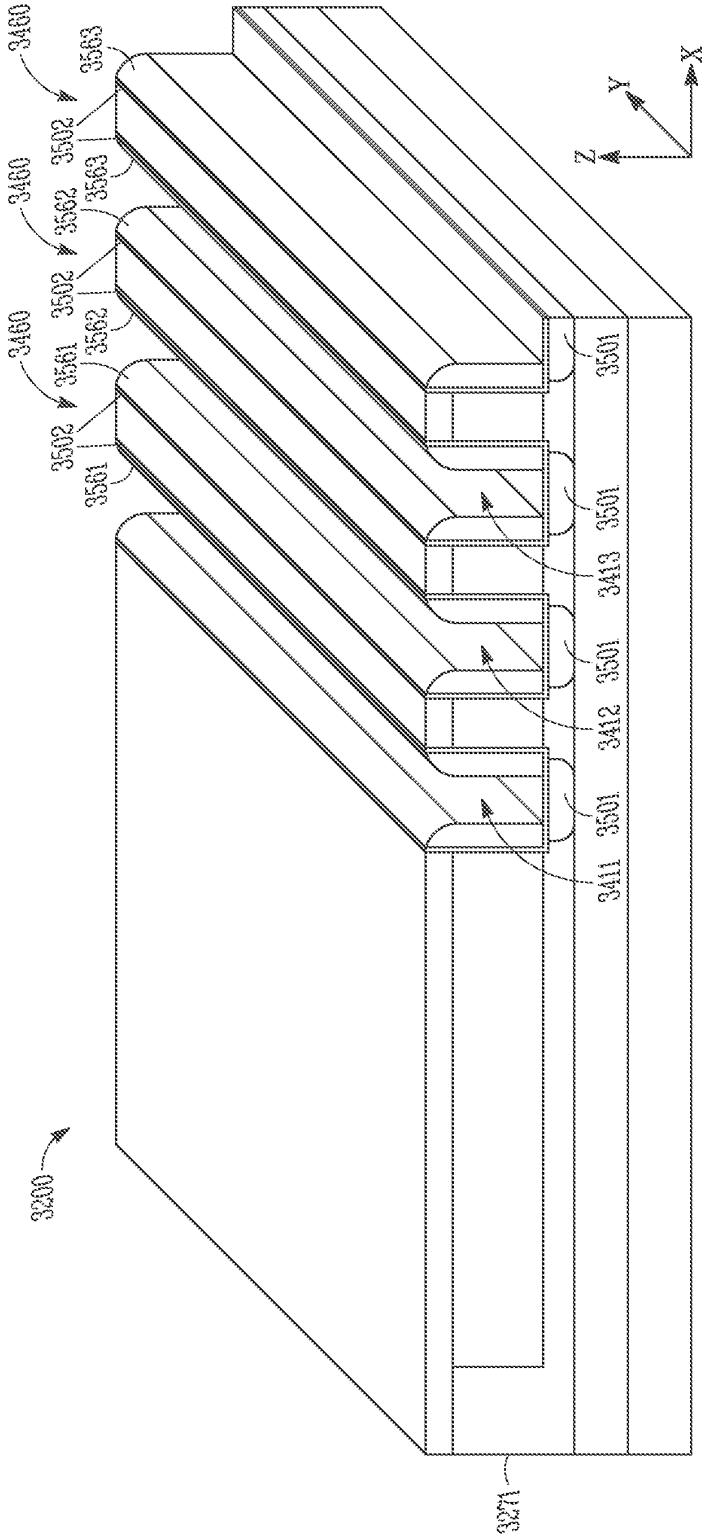

3460
3563
3502
3460
3562
3563
3502
3460
3561
3562
3502
3561
3501
3501
3413
3501
3412
3501
3411
3200
3271
Y
X
Z

FIG. 35

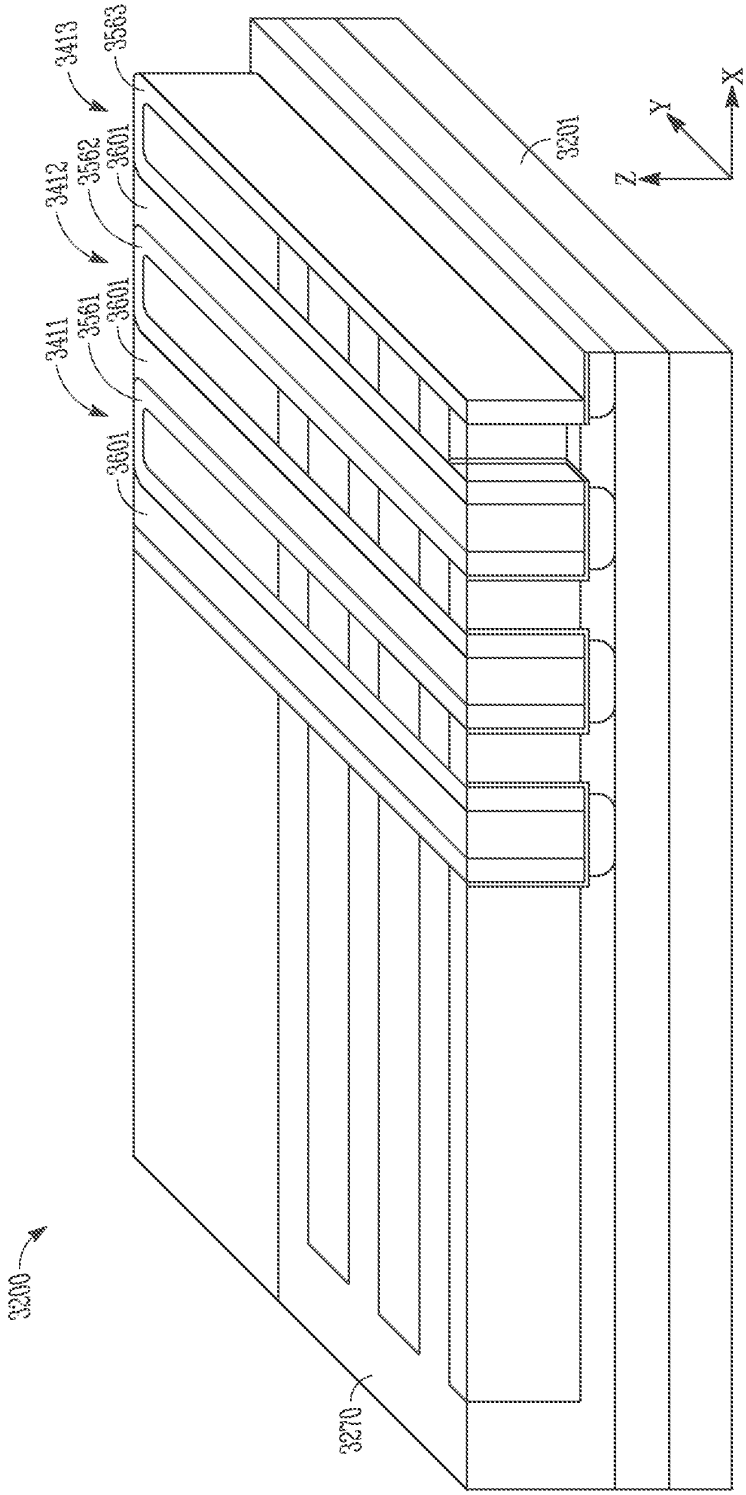


FIG. 36

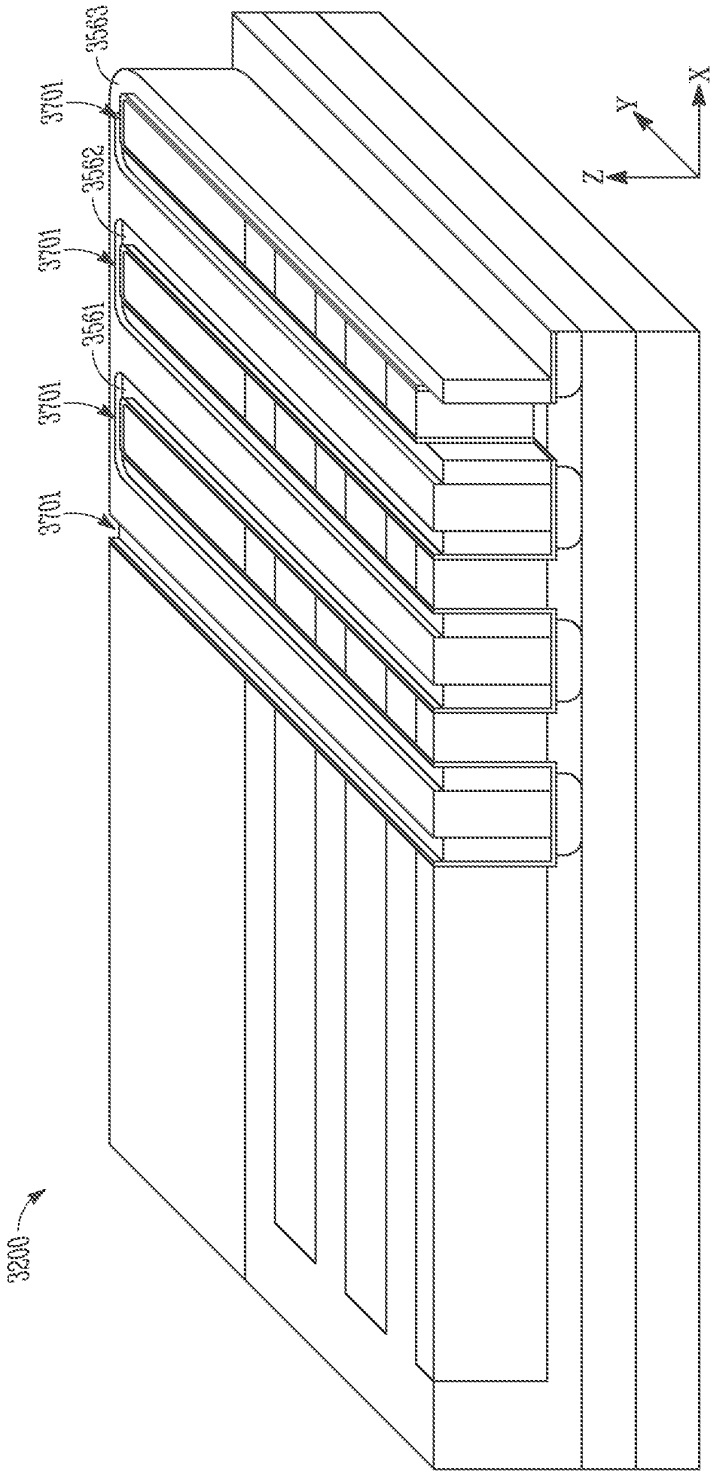


FIG. 37

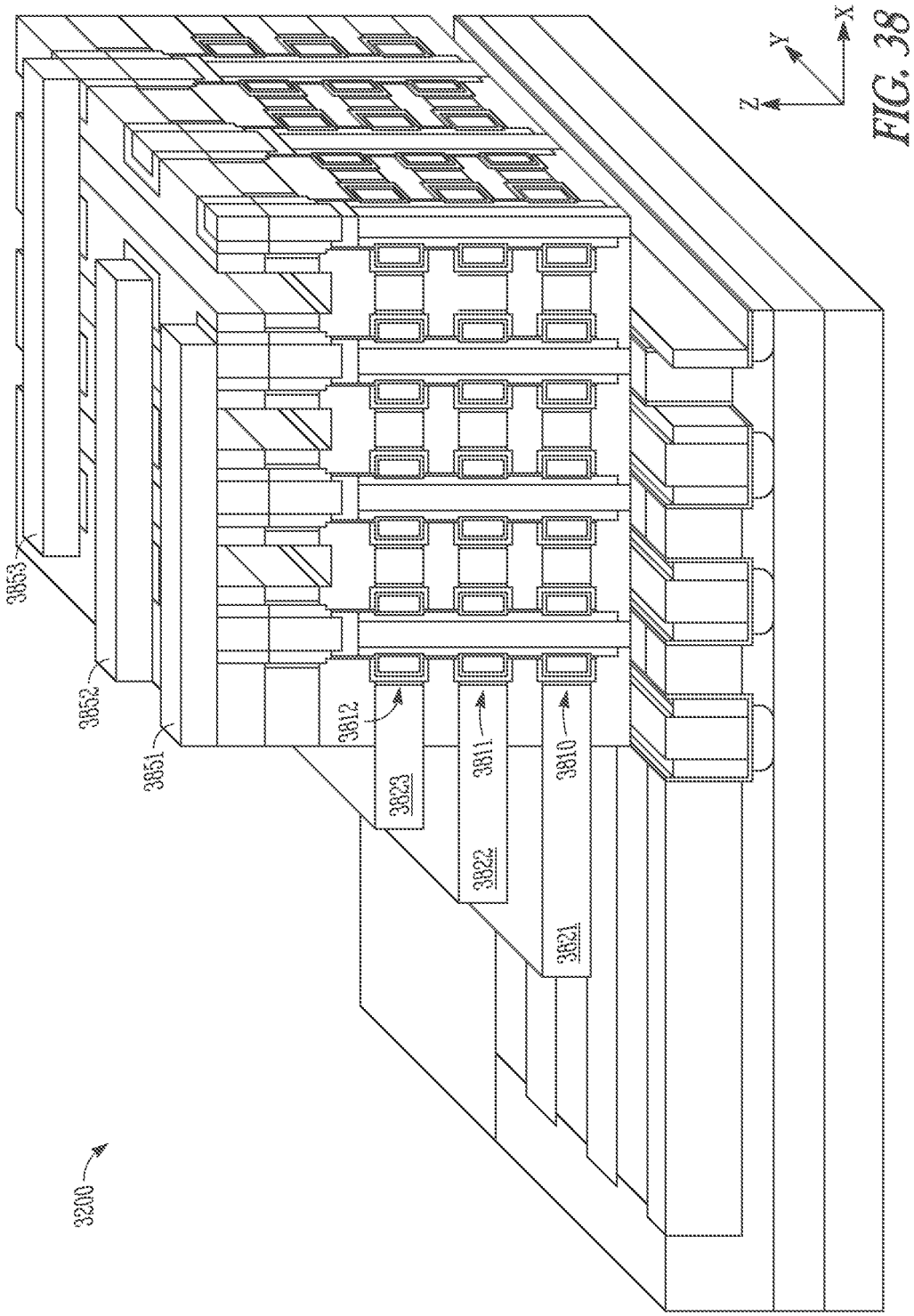


FIG. 38

THREE DIMENSIONAL MEMORY AND METHODS OF FORMING THE SAME

PRIORITY APPLICATION

This application is a continuation of U.S. application Ser. No. 16/125,242, filed Sep. 7, 2018, which is a continuation of U.S. application Ser. No. 15/722,580, filed Oct. 2, 2017, now issued as U.S. Pat. No. 10,090,324, which is a continuation of U.S. application Ser. No. 15/188,273, filed Jun. 21, 2016, now issued as U.S. Pat. No. 9,780,115, which is a continuation of U.S. application Ser. No. 14/041,928, filed Sep. 30, 2013, now issued as U.S. Pat. No. 9,379,005, which is a divisional of U.S. application Ser. No. 12/825,211, filed Jun. 28, 2010, now issued as U.S. Pat. No. 8,803,214, all of which are incorporated herein by reference in their entireties.

BACKGROUND

Non-volatile memory devices such as flash memory devices are used in many computers and electronic devices to store information. A flash memory device usually has a write operation to store information (e.g., data and instruction codes), a read operation to retrieve the stored information, and an erase operation to clear information from the memory. As demand for higher density memory device increases, three-dimensional (3D) memory devices have been proposed. An example of a conventional 3D memory device is described by Jiyoung Kim et al. in an article titled "Novel 3-D Structure for Ultra High Density Flash Memory with Vertical-Array-Transistor (VRAT) and Planarized Integration on the same Plane (PIPE)", published in the 2008 Symposium on VLSI Technology Digest of Technical Papers, pages 22-23. Since 3D memory devices are relatively new, manufacturing these devices can pose fabrication process challenges.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a block diagram of a memory device having a memory array with memory cells, according to an embodiment of the invention.

FIG. **2** shows a schematic diagram of a portion of a memory device having data lines located below memory cells, according to an embodiment of the invention.

FIG. **3** shows a three-dimensional view of a portion of the memory device of FIG. **2**, according to an embodiment of the invention.

FIG. **4** shows a portion of a control gate and a memory cell of the memory device of FIG. **3**, according to an embodiment of the invention.

FIG. **5** through FIG. **29** show various processes of forming a memory device having data lines located below memory cells, according to an embodiment of the invention.

FIG. **30** shows a schematic diagram of a portion of a memory device having data lines located above memory cells, according to an embodiment of the invention.

FIG. **31** shows a three-dimensional view of a portion of the memory device of FIG. **30**, according to an embodiment of the invention.

FIG. **32** through FIG. **38** show various processes of forming a memory device with data lines located above memory cells, according to an embodiment of the invention.

DETAILED DESCRIPTION

FIG. **1** shows a block diagram of a memory device **100** having a memory array **102** with memory cells **110** according to an embodiment of the invention. Memory cells **110** can be arranged in rows and columns along with access lines **123** (e.g., wordlines having signals WL**0** through WLM) and lines **124** (e.g., bit lines having signals BL**0** through BLN). Memory device **100** uses lines **124** and **128** to transfer information within memory cells **110**. Memory cells **110** can be physically located in multiple device levels such that one group of memory cells **110** can be stacked on one or more groups of other memory cells **110**. Row decoder **132** and column decoder **134** decode address signals A**0** through AX on lines **125** (e.g., address lines) to determine which memory cells **110** are to be accessed. Row and column level decoders **136** and **138** of row and column decoders **132** and **134**, respectively, determine which of the multiple device levels of memory device **100** that the memory cells **110** to be accessed are located.

A sense amplifier circuit **140** operates to determine the value of information read from memory cells **110** and provide the information in the form of signals to lines **124** and **128**. Sense amplifier circuit **140** can also use the signals on lines **124** and **128** to determine the value of information to be written to memory cells **110**. Memory device **100** can include circuitry **150** to transfer information between memory array **102** and lines (e.g., data lines) **126**. Signals DQ**0** through DQN on lines **126** can represent information read from or written into memory cells **110**. Lines **126** can include nodes within memory device **100** or nodes (e.g., pins or solder balls) on a package where memory device **100** resides. Other devices external to memory device **100** (e.g., a memory controller or a processor) may communicate with memory device **100** through lines **125**, **126**, and **127**.

Memory device **100** performs memory operations such as a read operation to read information from memory cells **110** and a write operation (sometime referred to as a programming operation) to store information into memory cells **110**. A memory control unit **118** controls the memory operations based on control signals on lines **127**. Examples of the control signals on lines **127** include one or more clock signals and other signals to indicate which operation, (e.g., a write or read operation) that memory device **100** performs. Other devices external to memory device **100** (e.g., a processor or a memory controller) may control the values of the control signals on lines **127**. Specific values of a combination of the signals on these lines can produce a command (e.g., a write or read command) that causes memory device **100** to perform a corresponding memory operation (e.g., a write or read operation).

Each of memory cells **110** can store information representing a value of a single bit or a value of multiple bits such as two, three, four, or other numbers of bits. For example, each of memory cells **110** can store information representing a binary value "0" or "1" of a single bit. In another example, each of memory cells **110** can store information representing a value of multiple bits, such as one of four possible values "00", "01", "10", and "11" of two bits, one of eight possible values "000", "001", "010", "011", "100", "101", "110" and "111, or one of other values of other number of multiple bits.

Memory device **100** can receive a supply voltage, including supply voltage signals Vcc and Vss, on lines **141** and **142**, respectively. Supply voltage signal Vss may operate at a ground potential (e.g., having a value of approximately zero volts). Supply voltage signal Vcc may include an external voltage supplied to memory device **100** from an external power source such as a battery or an alternating-current to direct-current (AC-DC) converter circuitry.

Circuitry **150** of memory device **100** can include a select circuit **152** and an input/output (I/O) circuit **116**. Select

circuit **152** responds to signals SEL**0** through SELn to select the signals on lines **124** and **128** that can represent the information read from or written into memory cells **110**. Column decoder **134** selectively activates the SEL**0** through SELn signals based on address signals A**0** through AX. Select circuit **152** selects the signals on lines **124** and **128** to provide communication between memory array **102** and I/O circuit **116** during read and write operations.

Memory device **100** can be a non-volatile memory device and memory cells **110** can be non-volatile memory cells such that memory cells **110** can retain information stored thereon when power (e.g., Vcc or Vss, or both) is disconnected from memory device **100**. For example, memory device **100** can be a flash memory device such as a NAND flash or a NOR flash memory device, or other kinds of memory devices, such as a variable resistance memory device (e.g., phase change random-access-memory (PCRAM), resistive RAM (RRAM), etc.).

One skilled in the art may recognize that memory device **100** may include other features that are not shown in FIG. **1**, to help focus on the embodiments described herein.

Memory device **100** may include at least one of the memory devices and memory cells described below with reference to FIG. **2** through FIG. **38**.

FIG. **2** shows a schematic diagram of a portion of a memory device **200** having data lines **251**, **252**, and **253** located below memory cells **210**, **211**, and **212**, according to an embodiment of the invention. Memory cells **210**, **211**, and **212** can be grouped into groups, such as a group of memory cells **210**, a group of memory cells **211**, and a group of memory cells **212**. As shown in FIG. **2**, the memory cells in each group share the same control gate, such as control gate **221**, **222**, or **223** (with associated signals WL**0**, WL**1**, and WL**2**). The memory cells are coupled in series as strings, such as strings **215** and **216**. Each string can include one of the memory cells from different groups and is coupled between one of transistors **231** and one of transistors **232**.

As shown in FIG. **2**, transistors **231** have gates coupled to select lines **241**, **242**, and **243** (with associated signals SGD**0**, SGD**1**, and SGD**2**). Transistors **231** have nodes (e.g., sources) coupled to data lines **251**, **252**, and **253** (with associated signals BL**0**, BL**1**, and BL**2**). Data lines **251**, **252**, and **253** sometimes correspond to bit lines or sense lines of a non-volatile memory device.

Transistors **232** have gates coupled to select lines **261**, **262**, and **263** (with associated signals SGS**0**, SGS**1**, and SGS**2**). Transistors **232** have nodes (e.g., drains) coupled to a common source **270** of memory cell strings in a non-volatile memory device.

FIG. **2** shows three groups of memory cells with associated components coupled to them, as an example. The number of groups of memory cells and their associated components (e.g., control gates and data lines) can vary.

Memory device **200** uses control gates **221**, **221**, and **223** to control access to memory cells **210**, **211**, and **212** during a read operation to sense (e.g., read) information stored in memory cells **210**, **211**, and **212**, and during a write operation to store information into memory cells **210**, **211**, and **212**. Memory device **200** uses data lines **251**, **252**, and **253** to transfer the information read from these memory cells during a read operation.

Transistors **231** and **232** are responsive to signals SGD**0**, SGD**1**, and SGD**2**, and signals SGS**0**, GS**1**, and SGS**2**, respectively, to selectively couple the memory cells to data lines **251**, **252**, and **253** and common source **270** during a read or write operation.

To help focus on the description herein, the description herein omits detailed description of operations of memory device, such as write, read, and erase operation. One skill in the art would recognize these operations. For example, in an erase operation of memory device **200**, a voltage of approximately 20 volts can be applied to data lines **251**, **252**, and **253** while control gates **221**, **221**, and **223**, select lines **241**, **242**, and **243**, and select lines **261**, **262**, and **263** can be "floated" (e.g., leave unconnected to a voltage). In this erase operation, electrons from memory elements of memory cells **210**, **211**, and **212** may move to data lines **251**, **253**, and **253**.

FIG. **3** shows a 3D view of a portion of memory device **200**, according to an embodiment of the invention. FIG. **3** also shows X, Y, and Z directions, and device levels **301**, **302**, and **303** arranged in the Z-direction. Memory cells **210** of the same group can be arranged in rows and columns in the X-direction and Y-direction. Each group of memory cells is located in different device levels **301**, **302**, or **303**. For example, the group having memory cells **210** is located in device level **301**. The group having memory cells **211** is located in device level **302**. The group having memory cells **212** is located in device level **303**.

As shown in FIG. **3**, memory cells **210**, **211**, and **212** in each string (e.g., memory cells between transistors **231** and **232**) are substantially vertically aligned in the Z-direction with respect to a substrate underneath data lines **251**, **252**, and **253**. The substrate is not shown in FIG. **3**, but can be similar to substrate **503** of FIG. **5** and FIG. **6**. FIG. **3** also shows a channel **241** and a conductive material portion **242** extending vertically in the Z-direction and through memory element **430** of memory cells **210**, **211**, and **212** in the same string between transistors **231** and **232**, which corresponds to transistors **231** and **232** of FIG. **2**. As shown in FIG. **3**, transistor **231** can include a double-gate coupled to a body **391** (e.g., transistor channel) to control (turn on or off) the transistor. The structure of the double-gate can include two segments of the same select line **241** (as shown in FIG. **3**), such that the two segments are located on only two respective sides of body **391**.

Memory device **200** in FIG. **3** also can include contacts **329**, **349**, and **359**. Contacts **329** provide electrical connections to control gates **221**, **222**, and **223**. Contacts **349** provide electrical connections to select lines **241**, **242**, **243**, and **244**. Contacts **359** provide electrical connections to and from data lines **251**, **252**, and **253**. Select line **244** and the memory cell associated with it in the Z-direction are not shown in FIG. **2**.

FIG. **4** shows a portion of control gate **221** and a memory cell **210** of memory device **200** of FIG. **3**. Control gates **222** and **223** and memory cells **211** and **212** of FIG. **2** have structures similar to control gate **221** and memory cell **210**, respectively. As shown in FIG. **4**, control gate **221** can include a homogenous material with cavities **420**, each cavity being filed with various components, including materials different from the homogenous material. The various components include: a memory element **430**; a channel **441**, a conductive material portion **442**, and dielectrics **421** and **427**. Dielectric **421** can include multiple materials **422**, **423**, and **424** arranged as different layers. As shown in FIG. **4**, memory element **430** of each memory cell **210** has a ring shape (e.g., donut shape) with an inner side **451** and an outer side **452**. Each of the other memory cells **211** and **212** shown in FIG. **3** also has a ring shape. As shown in FIG. **3**, within memory cells **210**, **211**, and **212** in the same string (e.g., between transistors **231** and **232**), the entire ring-shape memory element **430** of each memory cell is substantially

vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

Each memory element **430** can store information, such as based on the amount of charge (e.g., number of electrons) therein. In each such memory element **430**, the amount of charge corresponds to the value of information store that memory element. The amount of charge can be controlled in a write operation or in erase operation. For example, electrons from channel **441** or conductive material portion **442**, or both, can move to memory element **430** during a write operation due to a tunneling effect known to those skilled in the art. In an erase operation, electrons from memory element **430** can move back to channel **441** or conductive material portion **442**, or both, to data lines **251**, **253**, and **253** (FIG. **2** and FIG. **3**). Alternative embodiments might use a memory element **430** that can store information, such as based on the resistance of the element **430**, for example.

Memory device **200** of FIG. **3** can be formed using processes similar to or identical to those described below with reference to FIG. **5** through FIG. **29**.

FIG. **5** through FIG. **29** show various processes of forming a memory device **500** having data lines located below memory cells, according to an embodiment of the invention. Memory device **500** (shown in more details in FIG. **29**) can correspond to memory device **300** of FIG. **3**.

FIG. **5** shows memory device **500** having a substrate **503**, which can include materials **501** and **502** arranged as layers. Material **501** can include bulk silicon or could be another semiconductor material. Material **502** can be a dielectric material, for example, silicon oxide. FIG. **5** also shows materials **504** and **505** formed over substrate **503**. Forming materials **504** and **505** can include depositing a conductive material over substrate **503** and then depositing another conductive material over material **504**. Material **504** can include a metal or other conductive materials. Material **505** can include undoped polysilicon or doped polysilicon, such as p-type silicon or another conductive materials.

FIG. **5** also shows an X-direction, a Y-direction perpendicular to the X-direction, and a Z-direction perpendicular to both the X-direction and the Y-direction. As shown in FIG. **5**, materials **504** and **505** can be formed as different layers, one layer over (e.g., on) one or more other layers in the Z-direction.

As used herein, the term "on" used with respect to two or more materials, one "on" the other, means at least some contact between the materials, while "over" or "overlaying" could refer to either a material being "on" another material or where there is one or more additional intervening materials between the materials (e.g., contact is not necessarily required). The term "on", "over", or "overlying" does not imply any directionality as used herein unless otherwise explicitly stated as such.

FIG. **6** shows memory device **500** after data lines **651**, **652**, and **653** and device structures **605** have been formed. A process such as etching (e.g., dry etching) can be used to remove portions of materials **504** and **505** (FIG. **5**) to form trenches **511** and **512**, which have trench bottoms at material **502**. Each of data lines **651**, **652**, and **653** and each of device structures **605** has a greater dimension (e.g., length) extending in the X-direction. A mask (not shown in FIG. **6**) having separate openings extending in the X-direction can be used to form trenches **511** and **512**. As shown in FIG. **6**, trenches **511** and **512** divide material **504** (FIG. **5**) into separate data lines **651**, **652**, and **653**, which can correspond to data lines **251**, **252**, and **253** of FIG. **2**.

FIG. **7** shows memory device **500** after pillars **705** have been formed in area **701** of memory device **500**. Pillars **705** are not formed in area **702** of memory device **500**. For simplicity, FIG. **7** through FIG. **29** do not show substrate **503** of FIG. **6**. In FIG. **7**, a process such as etching (e.g., dry etch) can be used to remove portions of device structures **605** to form trenches **711**, **712**, and **713** in the Y-direction, perpendicular to trenches **511** and **512**, such that pillars **705** can be formed as shown in FIG. **7**. A mask (not shown in FIG. **7**) having separate openings extending in the Y-direction can be used to form trenches **711**, **712**, and **713**. Each pillar **705** can include a height in the Z-direction of approximately 20 to 50 nanometers. As shown in FIG. **7**, pillars **705** are arranged in rows and columns (e.g., in a matrix) in the X-direction and Y-direction. For simplicity, FIG. **7** does not show a dielectric material filled in trenches **511** and **512**. However, forming memory device **500** in FIG. **7** also can include forming a dielectric material (e.g., silicon oxide) to fill trenches **511** and **512** up to a top surface **715** of device structure **605**.

FIG. **8** shows memory device **500** after dielectric **831** and select lines **841**, **842**, **843**, and **844** have been formed. Select lines **841**, **842**, **843**, and **844** can correspond to select lines **241**, **242**, **243**, and **244**, respectively, of FIG. **3**. In FIG. **8**, dielectrics **831** are formed to electrically isolate select lines **841**, **842**, **843**, and **844** from pillars **705**. Dielectrics **831** can be formed by, for example, depositing a dielectric material (e.g., silicon oxide) on at least two sides of each pillar **705** or by oxidizing pillars **705**. After dielectrics **831** are formed, select lines **841**, **842**, **843**, and **844** can be formed by, for example, depositing a conductive material over pillars **705** and trenches **711**, **712**, and **713** (FIG. **7**) and then removing (e.g., etching) a portion of the conductive material to form select lines **841**, **842**, **843**, and **844** having the structure shown in FIG. **8**. Examples of the conductive materials for select lines **841**, **842**, **843**, and **844** include polysilicon, metal, or other conductive materials, such as TiN and TaN.

FIG. **8** also shows doped regions **833**, which can be formed by inserting (e.g., implanting) n-type impurities into selective portions of device structure **605**. Examples of n-type impurities include elements such as phosphorus (P) or arsenic (As). The remaining portion of device structures **605** that has not been inserted with n-type impurities may maintain its original material, such as p-type silicon, as described above with reference to FIG. **5**.

FIG. **9** shows memory device **500** with select lines **941**, **942**, **943**, and **944**, which are alternative structures for select lines **841**, **842**, **843**, and **844** of FIG. **8**. In FIG. **8**, opposite sides of each pillar **705** are associated with two different segments of the same select line **841**, **842**, **843**, or **844**. In FIG. **9**, except for the top surfaces of pillars **705**, each pillar **705** can be completely surrounded by the material of one of the select line **941**, **942**, **943**, or **944** (e.g., four sides of each pillar **705** are associated with four different segments of the same select line). Higher efficient memory device may be achieved with select lines **941**, **942**, **943**, and **944** in comparison to select lines **841**, **842**, **843**, and **844**. Select lines **941**, **942**, **943**, and **944** can also be alternative structures for select lines **241**, **242**, **243**, and **244**, respectively, of FIG. **3**. Thus, each transistor **231** of FIG. **2** and FIG. **3** can include a surrounded gate with a structure shown in FIG. **9**. Thus, instead of a double-gate shown in FIG. **3**, each transistor **231** of FIG. **3** can alternatively include a surrounded gate having four different segments of the same select line (such as select line **941**) surrounding body **391** (FIG. **3**).

FIG. **10** shows memory device **500** after materials **1001** through **1007** are formed over pillars **705** and select lines **841**, **842**, **843**, and **844**. Materials **1001** through **1007** can be

formed in both areas **701** and **702** of memory device **500**. However, to focus on the description herein, FIG. **10** does not show some portions of materials **1001** through **1007** in area **702**. The description below with reference to FIG. **28** and FIG. **29** describes forming additional components (e.g., components similar to contacts **329** of FIG. **3**) in area **702** of memory device **500**.

In FIG. **10** through FIG. **29**, for simplicity, some number designations associated with some components of memory device **500** may not be repeated from one figure to another figure. In FIG. **10**, before forming materials **1001** through **1007**, a dielectric material (not shown in FIG. **10**), such as silicon oxide, can be formed to fill gaps **1041**, **1042**, and **1043**. Forming materials **1001** through **1007** can include alternately depositing dielectric material and conductive material in an interleave fashion, such that these materials are alternately stacked over each other in the Z-direction, as shown in FIG. **10**. Materials **1001**, **1003**, **1005**, and **1007** can include dielectric materials, such as silicon oxide. Materials **1002**, **1004**, and **1006** can include conductive materials, such as metal or polysilicon (e.g., n-type silicon for p-type silicon). As shown in FIG. **10**, materials **1001** through **1007** are formed such that materials **1002**, **1004**, and **1006** are electrically isolated from each other by materials **1001**, **1003**, **1005**, and **1007**.

FIG. **11** shows memory device **500** after openings (e.g., holes) **1101** have been formed in material **1002** through **1107**. Holes **1101** are formed such that each hole **1101** can be aligned substantially directly over a corresponding pillar **705**, as illustrated in FIG. **11**. Forming holes **1101** can include removing (e.g., etching) a portion of each of materials **1002** through **1007**, stopping at material **1001**, such that at least a portion of material **1001** or the entire material **1001** remains to separate holes **1101** from pillars **705**. Forming holes **1101** results in forming cavities **1110** in each of materials **1003**, **1005**, and **1007**, and cavities **1120** in each of materials **1002**, **1004**, and **1006**. As shown in FIG. **12**, cavities **1110** in the materials **1003**, **1005**, and **1007** are substantially aligned directly over cavities **1120** in the other materials **1002**, **1004**, and **1006**. Each cavity **1110** and each cavity **1120** may have substantially the same diameter, D**1**. Diameter D**1** can also be considered the diameter of each hole **1101** at the location of each cavity **1110** and each cavity **1120**.

FIG. **12** shows memory device **500** after cavities **1220** have been formed in materials **1002**, **1004**, and **1006** (used to form control gates **1221**, **1222**, and **1223**). Forming cavities **1220** can include enlarging the size of cavities **1120** (FIG. **11**) while keeping the size of cavities **1110** substantially unchanged (e.g., remaining substantially at diameter D**1**). For example, enlarging the size of cavities **1120** (FIG. **11**) can include selectively removing (e.g., selective wet or dry etching) a portion of each of materials **1002**, **1004**, and **1006** at each cavity **1120** (FIG. **11**) such that the diameter of each cavity **1220** increases to substantially diameter D**2**, while the diameter D**1** at each cavity **1110** remains substantially unchanged. Diameter D**2** is greater than diameter D**1**. Forming cavities **1120** in materials **1002**, **1004**, and **1006** also form control gates **1221**, **1222**, and **1223**, which can correspond to control gates control gates **221**, **222**, and **223** of FIG. **2**.

FIG. **13** shows more details of control gate **1221** of FIG. **12**. Control gates **1222** and **1223** of FIG. **12** have a similar structure as control gate **1221**. As shown in FIG. **13**, control gate **1221** can include a homogenous material with cavities **1220** of FIG. **11** being arranged in rows and columns in the X-direction and Y-direction. Each cavity **1220** can include a sidewall **1225**.

FIG. **14** and FIG. **15** shows memory device **500** after dielectrics **1421** and memory elements **1430** have been formed in cavities **1220**. For simplicity, FIG. **15** does not show dielectrics **1421** and memory elements **1430** in all cavities **1220**. Each dielectric **1421** can be formed on sidewall **1225**, such that each dielectric **1421** and can be located between the material of control gate **1221** and memory element **1430**, and such that memory element **1430** can be electrically isolated from the material of control gate **1221** by at least a portion of dielectric **1421**. Forming dielectric **1421** can include forming multiple materials **1422**, **1423**, and **1424** (FIG. **15**) at different times, one material after another. Forming material **1422** can include oxidizing a portion (e.g., a surface) of sidewall **1225** to form dielectric material (e.g., silicon oxide) on sidewall **1225**. Alternatively, forming material **1422** can include depositing dielectric material (e.g., silicon oxide) on sidewall **1225**. Forming material **1423** can include depositing dielectric material (e.g., silicon nitride) on material **1422**, wherein a portion of that dielectric material may also form on sidewall **1425** of each cavity **1110**. Forming material **1424** can include depositing dielectric material (e.g., silicon oxide) on material **1423**.

Memory elements **1430** can be formed after dielectrics **1421** are formed. As shown in FIG. **15**, each memory element **1430** has a ring shape (e.g., a donut shape) with an inner side **1451** and an outer side **1452** of FIG. **14**. Forming memory elements **1430** can include depositing a material in holes **1101**. Since cavities **1220** of FIG. **14** are substantially aligned with cavities **1110**, the material (that forms memory element **1430**) may fill both cavities **1110** and **1120**. Then, a portion (e.g., center portion in each hole) of the material that forms memory elements **1430** can be removed (e.g., by etching in the same, single, etching step) such that the material in cavities **1110** can be removed (e.g., completely removed) and the material in cavities **1220** is not completely removed but partially removed. As shown in FIG. **14**, after the material that forms memory elements **1430** is removed from cavities **1110**, a portion of dielectric material **1423** (e.g., silicon nitride, that was formed on material **1422**) may be exposed. As shown in FIG. **14**, after the material that forms memory elements **1430** is partially removed from cavities **1220**, memory element **1430** (formed by the remaining material in a cavity **1220**) associated with the same hole **1101** may have its inner side **1451** substantially aligned with sidewall **1425** (or sidewall **1425** with portions of materials **1422** and **1423** of cavities **1110**) of cavities **1110**.

The material of memory elements **1430** can include, for example, semiconductor material (e.g., polysilicon), dielectric charge trapping material, such as silicon nitride or other dielectric charge trapping materials, or a variable resistance material, such as a phase change material (e.g., GST). During removing (e.g., etching) a portion of the material that forms memory elements **1430**, portions **1401** of material **1001** located over pillars **705** can also be removed to reduce the thickness of portions **1401**.

FIG. **16** and FIG. **17** show memory device **500** after dielectric **1627** has been formed on inner side **1451** of memory element **1430** and in cavities **1110**. Forming dielectric **1627** can include depositing dielectric material (e.g., silicon oxide) on inner side **1451**. Alternatively, forming dielectric **1627** can include oxidizing a portion (e.g., inner side **1451**) of memory element **1430**. Forming dielectric **1627** (e.g., by oxidation) may also consume material **1423**

(FIG. **14**) formed on material **1422**, which formed on sidewall **1425** of cavities **1110**. Thus, dielectric **1627** may also form in cavities over material **1422**.

FIG. **18** and FIG. **19** show memory device **500** after channels **1841** have been formed on dielectrics **1627** in both cavities **1110** and **1220**. Forming channels **1841** can include depositing a conductive material on dielectrics **1627**. An etching process can be used to reduce the thickness of the conductive material after it is deposited. The conductive material of channels **1841** can include doped polysilicon, which can have the same material type (e.g., p-type) as pillars **705**. FIG. **18** also shows a formation of openings **1801**, which can be formed by removing (e.g., by etching) portions **1401** (FIG. **14**) located over pillars **705**. As shown in FIG. **19**, channel **1841** is facing memory elements **1430** and is electrically isolated from memory element **1430** by at least a portion of dielectric **1627**.

FIG. **20** shows memory device **500** after a conductive material **2001** has been formed by, for example, depositing undoped or lightly doped polysilicon to place channels **1841** in electrical communication with pillars **705**. As shown in FIG. **20**, conductive material **2001** forms a continuous conductive path between channels **1841** and data lines **651**, **652**, and **653** through pillars **705**.

FIG. **21** shows memory device **500** after dielectric material **2101** (e.g., silicon oxide) has been formed over conductive material **2001**.

FIG. **22** shows memory device **500** after a formation of openings (e.g., holes **2201**), a conductive material portion **2260**, and conductive material portions **2241**. Holes **2201** are formed such that each hole **2201** can be aligned substantially directly over channels **1841**, as illustrated in FIG. **22**. Forming holes **2201** can include removing (e.g., etching) a portion of dielectric material **2101** and a portion of conductive material **2001** (FIG. **21**), stopping at a location in material **1007**. Holes **2201** can be formed such that after a portion of conductive material **2001** is removed during the formation of holes **2201**, conductive material **2001** is separated into conductive material portion **2260** and conductive material portions **2241**, as illustrated in FIG. **22**.

FIG. **23** shows memory device **500** after doped regions **2301** have been formed. Forming doped regions **2301** can include inserting (e.g., implanting) n-type impurities into top parts of conductive material portions **2241**. Doped regions **2301** can provide a relatively low resistance connection between channels **1841** and other components of memory device **500**.

FIG. **24** shows memory device **500** after dielectrics **2401** and channels **2402** have been formed. Dielectrics **2401** (e.g., silicon oxide) is formed on sidewalls of conductive material portion **2260** at the location of holes **2201**. Channels **2402** are formed on sidewalls of dielectric material **2101** and on dielectrics **2401**.

FIG. **25** shows memory device **500** after conductive material **2501** has been formed in each of holes **2201**, such that channel **2402** can be electrically coupled to channel **1841** through conductive material **2501**, doped region **2301**, and conductive material portion **2241**. Forming conductive material **2501** in each of holes **2201** can include depositing a conductive material (e.g., polysilicon) over material, such that the conductive material fills holes **2201**. Then, a top portion of the conductive material can be removed by, for example, etching back the conductive material or by chemical mechanical planarization (CMP).

FIG. **26** shows memory device **500** after doped regions **2601** and select lines **2661**, **2662**, and **2663** have been formed. Forming doped regions **2601** can include inserting (e.g., implanting) n-type impurities into top portions of conductive material **2501**. Forming select lines **2661**, **2662**, and **2663** can include removing parts of dielectric material **2101** and conductive material portion **2260** to form trenches **2602**, which have trench bottoms partially extending into material **1007**. As shown in FIG. **26**, trenches **2602** separate conductive material portion **2260** into select lines **2661**, **2662**, and **2663**, which can correspond to select lines **261**, **262**, and **263** of FIG. **2**.

FIG. **27** shows memory device **500** after material **2701** and a common source **2770** have been formed. Forming material **2701** can include depositing a dielectric material (e.g., silicon dioxide) over material **2101**, such that the dielectric material fills trenches **2602**. Then, a top portion of the dielectric material can be removed by, for example, etching back the dielectric material or by CMP. Forming common source **2770** can include depositing a conductive material (e.g., metal) over materials **2701** and **2101**.

FIG. **28** shows memory device **500** after materials **1001** through **1007** in area **702** (FIG. **10**) are processed (e.g., by patterning) to form a stair like pattern with material between the stairs are not shown in FIG. **28**. As mentioned above in the description of FIG. **10**, some portions of materials **1001** through **1007** are omitted from area **702** of FIG. **10** through FIG. **27** for clarity. FIG. **28** shows material **1001** through **1007** in area **702** after they have been processed to form the stair like pattern. As shown in FIG. **28**, control gates **1221**, **1222**, and **1223** are formed from materials **1002**, **1004**, and **1006**, respectively, which are formed in the stair like pattern.

FIG. **29** shows memory device **500** after contacts **2929**, **2949**, and **2959** have been formed. Contacts **2929** provide electrical connections to control gates **1221**, **1222**, and **1223**. Contacts **2949** provide electrical connections to select lines **841**, **842**, **843**, and **844**. Contacts **2959** provide electrical connections to and from data lines **651**, **652**, and **653**.

As shown in FIG. **29**, memory device **500** can include components and memory cells **2910**, **2911**, and **2912** similar to or identical to components and memory cells **210**, **211**, and **212** of memory device **300** described above with reference to FIG. **2** and FIG. **3**.

One skilled in the art may readily recognize that additional processes may be performed to form additional features of a memory device, such as memory device **500** described above. Thus, to help focus on the embodiments described herein, FIG. **5** through FIG. **29** described above and FIG. **30** through FIG. **38** described below show only some of the features of a memory device, such as memory device **500**.

FIG. **30** shows a schematic diagram of a portion of a memory device **300** having data lines **251**, **252**, and **253** located above memory cells **210**, **211**, and **212**, according to an embodiment of the invention. Memory device **300** can include components similar to those of memory device **200** of FIG. **3**. Thus, for simplicity, similar or same components between memory device **200** and memory device **3000** are given the same number designations. The detailed description of these similar components is not repeated in FIG. **30**. Main differences between memory device **3000** and memory device **200** include the locations of data lines **251**, **252**, and **253** and common source **3070** of memory device **3000** to enable global erase operation. As shown in FIG. **30**, data lines **251**, **252**, and **253** are located above memory cells **210**, **211**, and **212**. Common source **3070** is located below memory cells **210**, **211**, and **212** and can couple directly to at least a portion of a substrate of memory device **3000** (e.g., substrate **3101** in FIG. **31**). This main difference may allow voltages to be applied to various components of memory

device **3000** in a different way during an erase operation and memory device **3000** function differently (e.g., during the global erase operation) in comparison with the erase operation (e.g., local erase operation) of memory device **200**. For example, in an erase operation of memory device **3000**, a voltage of approximately 20 volts can be applied to common source **3070**, while control gates **221**, **221**, and **223**, data lines **251**, **252**, and **253**, select lines **241**, **242**, and **243**, and select lines **261**, **262**, and **26** can be "floated". In this erase operation, electrons from memory elements of memory cells **210**, **211**, and **212** may move (e.g., by tunneling) to common source **3070** (e.g., global erase). In memory **200**, as described above with reference to FIG. **2**, FIG. **3**, and FIG. **4**, during an erase operation, electrons from memory elements of memory cells **210**, **211**, and **212** may move to data lines **251**, **253**, and **253** (e.g., local erase)

FIG. **31** shows a 3D view of a portion of the memory device **3000** of FIG. **30**, according to an embodiment of the invention. As shown in FIG. **31**, data lines **251**, **252**, and **253** are located above memory cells **210**, **211**, and **212**, common source **3070** is located below memory cells **210**, **211**, and **212** and is coupled to a substrate **3101**. Substrate **3101** can include semiconductor material, such as p-type silicon.

As shown in FIG. **31**, memory cells **210**, **211**, and **212** in each string (e.g., memory cells between transistors **231** and **232**) are substantially vertically aligned in the Z-direction with respect to substrate **3101**. Transistor **232** can include a double-gate or surrounded gate similar to the double-gate (FIG. **3**) or surrounded gate (FIG. **9**) of transistor **231** of FIG. **3**. FIG. **31** also shows a channel **441** and a conductive material portion **442** extending vertically in the Z-direction and through memory element **430** of memory cells **210**, **211**, and **212** in the same string between transistors **231** and **232**, which corresponds to transistors **231** and **232** of FIG. **30**.

Memory element **430** in each of memory cells **210**, **211**, and **212** has a ring shape. As shown in FIG. **31**, within memory cells **210**, **211**, and **212** in the same string, the entire ring-shape memory element **430** of each memory cell is substantially vertically aligned (in the Z-direction) with the entire ring-shape memory element of each of the other memory cells in the same string.

FIG. **32** through FIG. **38** show various processes of forming a memory device **3200** having data lines located above memory cells, according to an embodiment of the invention. Memory device **3200** (shown in more details in FIG. **38**) can correspond to memory device **3000** of FIG. **31**.

FIG. **32** shows memory device **3200** having a substrate **3201** and trenches **3211**, **3212**, and **3213**, and substrate portions **3270** and **3271** formed on a top portion of substrate **3201**. Substrate **3201** can include semiconductor material, such as bulk silicon. Top substrate portions **3270** and **3271** can be formed by inserting (e.g., implanting) p-type impurities into a top portion of substrate **3201**. Thus, substrate portions **3270** and **3271** can include p-type silicon. Forming trenches **3211**, **3212**, and **3213** and substrate portion **3270** can include removing (e.g., etching) a portion of substrate portion **3271**. During a write or read operation of memory device **3200**, substrate portion **3270** can be coupled to a potential, such as to ground. During an erase operation of memory device **3200**, substrate portion **3270** can be coupled to a voltage, for example, approximately 20 volts.

FIG. **33** shows memory device **3200** after material **3301** has been formed in trenches **3211**, **3212**, and **3213** (FIG. **32**). Forming material **3301** can include depositing dielectric material (e.g., silicon oxide) over substrate **3201** to fill trenches **3211**, **3212**, and **3213**. Then, a top portion of the dielectric material can be removed by, for example, CMP.

FIG. **34** shows memory device **3200** after material **3401** and trenches **3411**, **3412**, and **3413**, and device structures **3460** have been formed. Forming material **3401** can include depositing dielectric material (e.g., silicon oxide, or silicon nitride) over substrate **3201** and material **3301**. Forming trenches **3411**, **3412**, and **3413** can include removing (e.g., etching) portions of substrate **3201**, material **3301**, and material **3401**. Device structures **3460** are formed as a result of the formation of trenches **3411**, **3412**, and **3413**.

FIG. **35** shows memory device **3200** after a formation of doped regions **3501**, material **3502**, and select lines **3561**, **3562**, and **3563**. Forming doped regions **3501** can include inserting (e.g., implanting) n-type impurities into selective portions of substrate portion **3271**. Material **3502** (e.g., silicon oxide) can be formed on both sides of each device structure **3460** to electrically isolate select lines **3561**, **3562**, and **3563** from device structures **3460**. Materials of select lines **3561**, **3562**, and **3563** can include one or more conductive materials, such as one or more metals, alloys, other conductive materials, or a combination thereof. Select lines **3561**, **3562**, and **3563** can correspond to select lines **261**, **262**, and **263** of memory device **3000** of FIG. **30**.

FIG. **36** shows memory device **3200** after material **3601** have been formed in trenches **3411**, **3412**, and **3413**. Forming material **3601** can include depositing dielectric material (e.g., silicon dioxide) to fill trenches **3411**, **3412**, and **3413**. Then, a top portion of the dielectric material can be removed by, for example, etching back the conductive material or by CMP, stopping at substrate portion **3270**.

FIG. **37** shows memory device **3200** after grooves **3701** have been formed by removing (e.g., by wet etching) a top portion of the material used to form select lines **3561**, **3562**, and **3563**. Alternatively, forming grooves **3701** can be omitted.

FIG. **38** shows memory device **3200** after other components have been formed. The processes for forming the components of memory device **3200** in FIG. **38** can include similar or identical processes for forming the component of memory device **500** described above with reference to FIG. **10** through FIG. **29**. For example, control gates **3821**, **3822**, and **3823** of FIG. **38** can be formed using processes similar to or identical to those of forming control gates **1221**, **1222**, and **1223** of memory device **500** described above with described above with reference to FIG. **5** through FIG. **29**. Data lines **3851**, **3852**, and **3853** of FIG. **38**, can correspond to data lines **251**, **252**, and **253** of FIG. **30** and FIG. **31**. As shown in FIG. **38**, memory device **3200** can include memory cells **3810**, **3811**, and **3812**, which can be formed using processes similar to or identical to those of forming memory cells **2910**, **2911**, and **2912** of memory device **500** described above with reference to FIG. **5** through FIG. **29**.

One or more embodiments described herein include a memory device and methods of forming the memory device. One such memory device can include a first group of memory cells, each cell of the first group being formed in a respective cavity of a first control gate located in one device level of the memory device. The memory device also can include a second group of memory cells, each cell of the second group being formed in a cavity of in a second control gate located in another device level of the memory device. Additional apparatus and methods are described. Other embodiments including additional apparatus and methods are described above with reference to FIG. **1** through FIG. **38**.

The illustrations of apparatus such as memory devices **100**, **200**, **500**, **3000**, and **3200**, and memory cells **210**, **211**, **212**, **2910**, **2911**, **2912**, **3010**, **3811**, and **3812** are intended to

provide a general understanding of the structure of various embodiments and not a complete description of all the elements and features of the apparatus that might make use of the structures described herein.

The apparatus of various embodiments may include or be included in electronic circuitry used in high-speed computers, communication and signal processing circuitry, memory modules, portable memory storage devices (e.g., thumb drives), single or multi-processor modules, single or multiple embedded processors, multi-core processors, data switches, and application-specific modules including multilayer, multi-chip modules. Such apparatus may further be included as sub-components within a variety of electronic systems, such as televisions, cellular telephones, personal computers (e.g., laptop computers, desktop computers, handheld computers, tablet computers, etc.), workstations, radios, video players, audio players (e.g., MP3 (Motion Picture Experts Group, Audio Layer 3) players), vehicles, medical devices (e.g., heart monitor, blood pressure monitor, etc.), set top boxes, and others.

The above description and the drawings illustrate some embodiments of the invention to enable those skilled in the art to practice the embodiments of the invention. Other embodiments may incorporate structural, logical, electrical, process, and other changes. Examples merely typify possible variations. Portions and features of some embodiments may be included in, or substituted for, those of others. Many other embodiments will be apparent to those of skill in the art upon studying and understanding the above description.

The Abstract is provided to comply with 37 C.F.R. § 1.72(b) requiring an abstract that will allow the reader to quickly ascertain the nature and gist of the technical disclosure. The Abstract of the Disclosure is submitted with the understanding that it will not be used to interpret or limit the scope or meaning of the claims.

What is claimed is:

1. An apparatus comprising:

conductive pillars extending outward from a substrate;

memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars;

a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate;

a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and

a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.

2. The apparatus of claim **1**, further comprising:

a first conductive region located on a first side of the conductive pillar and separated from the conductive pillar by a first dielectric material; and

a second conductive region located on a second side opposite from the first side of the conductive pillar and separated from the conductive pillar by a second dielectric material.

3. The apparatus of claim **2**, wherein the first conductive region is coupled to the second conductive region.

4. The apparatus of claim **2**, wherein each of the first and second conductive regions comprises polysilicon.

5. The apparatus of claim **2**, wherein each of the first and second conductive regions comprises metal.

6. The apparatus of claim **1**, further comprising a data line coupled to the conductive channel, wherein the data line is located between the substrate and the first and second memory cells.

7. The apparatus of claim **1**, further comprising a data line coupled to the conductive channel, wherein the first and second memory cells are located between the data line and the substrate.

8. The apparatus of claim **1**, wherein the memory element comprises polysilicon.

9. The apparatus of claim **1**, wherein the memory element comprises a dielectric material.

10. An apparatus comprising:

a first conductive pillar and a second conductive pillar extending outward from a substrate;

a first data line coupled to the first and second conductive pillars, the first data line located between the first and second conductive pillars and the substrate;

a third conductive pillar and a fourth conductive pillars extending outward from the substrate;

a second data line coupled to the third and fourth conductive pillars, the second data line located between the third and fourth conductive pillars and the substrate;

a first memory cell string formed over the first conductive pillar;

a second memory cell string formed over the second conductive pillar;

a third memory cell string formed over the third conductive pillar;

a fourth memory cell string formed over the fourth conductive pillar;

a first control gate formed in a first device level;

a second control gate formed in a second device level, wherein,

the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;

the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate;

the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and

the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

11. The apparatus of claim **10**, further comprising:

a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells;

a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells;

a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and

a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.

12. The apparatus of claim 10, further comprising a first conductive gate including a first segment and a second segment coupled to the first segment, wherein:

the first segment is located on a first side of each of the first and third conductive pillars and separated from the first and third conductive pillars by a first dielectric material; and

the second segment is located on a second side of each of the first and third conductive pillars and separated from the first and third conductive pillars by a second dielectric material.

13. The apparatus of claim 12, further comprising a second conductive gate including a third a segment and a fourth segment coupled to the third segment, wherein:

the third segment is located on a first side of each of the second and fourth conductive pillars and separated from the second and fourth conductive pillars by a third dielectric material; and

the fourth segment is located on a second side of each of the second and fourth conductive pillars and separated from the second and fourth conductive pillars by a fourth dielectric material.

14. The apparatus of claim 13, wherein each of the first and second conductive gates comprises polysilicon.

15. The apparatus of claim 13, wherein each of the first and second conductive gates comprises metal.

16. The apparatus of claim 10, wherein the memory element of each of the first, second, third, and fourth memory cells comprises one of polysilicon and a dielectric material.

17. An apparatus comprising:

a first conductive pillar and a second conductive pillar extending outward from a substrate;

a third conductive pillar and a fourth conductive pillars extending outward from the substrate;

a region including a conductive material, the region coupled to the first, second, third, and fourth conductive pillars, the region located between substrate and the first, second, third, and fourth conductive pillars;

a first memory cell string formed over the first conductive pillar;

a second memory cell string formed over the second conductive pillar;

a third memory cell string formed over the third conductive pillar;

a fourth memory cell string formed over the fourth conductive pillar;

a first data line coupled to the first and second memory cell strings, the first and second memory cell strings located between the first data line and the substrate;

a second data line coupled to the third and fourth memory cell strings, the third and fourth memory cell strings located between the second data line and the substrate;

a first control gate formed in a first device level;

a second control gate formed in a second device level, wherein,

the first memory cell string includes a first memory cell having a memory element formed in a first cavity of the first control gate, and a second memory cell having a memory element formed in a first cavity of the second control gate;

the second memory cell string includes a third memory cell having a memory element formed in a second cavity of the first control gate, and a fourth memory cell having a memory element formed in a second cavity of the second control gate;

the third memory cell string includes a fifth memory cell having a memory element formed in a third cavity of the first control gate, and a sixth memory cell having a memory element formed in a third cavity of the second control gate; and

the fourth memory cell string includes a seventh memory cell having a memory element formed in a fourth cavity of the first control gate, and an eighth memory cell having a memory element formed in a fourth cavity of the second control gate.

18. The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises polysilicon.

19. The apparatus of claim 17, wherein the memory element of each of the first, second, third, and fourth memory cells comprises a silicon nitride.

20. The apparatus of claim 17, further comprising:

a first conductive channel coupled to the first conductive pillar and extending between the first and second memory cells;

a second conductive channel coupled to the second conductive pillar and extending between the third and fourth memory cells;

a third conductive channel coupled to the third conductive pillar and extending between the fifth and sixth memory cells; and

a fourth conductive channel coupled to the fourth conductive pillar and extending between the seventh and eighth memory cells.

* * * * *

Exhibit 8

REDACTED

EXHIBIT 8 (02/16/2024)

Micron's Exemplary Infringement Claim Chart for U.S. Patent No. 10,872,903

The following chart provides non-limiting examples, without the benefit of claim construction or discovery, of how YMTC's Accused Products (as that term is defined in the Complaint) meet every limitation, literally or under the doctrine of equivalents, of at least claim 1 of U.S. Patent No. 10,872,903. The referenced images are images from a 232L YMTC 1Tb TLC part. Micron reserves the right to amend, correct, supplement, or otherwise change its explanation of how YMTC's Accused Products meet the following claim limitations, including as the claims are construed, as discovery progresses, or as Micron's investigation continues. Micron takes no position on claim interpretation or scope at this time.

Claim Language	YMTC's Accused Products
1. An apparatus comprising:[1]	YMTC's Accused Products includes "an apparatus." Specifically, as shown below, the products include a semiconductor apparatus:

[1] By providing this disclosure, Micron does not concede that the preamble is a claim limitation.

EXHIBIT 8 (02/16/2024)

	REDACTED
conductive pillars extending outward from a substrate;	YMTC's Accused Products include "conductive pillars extending outward from a substrate." Specifically, as shown below, YMTC's Accused Products include a substrate with conductive pillars that extend out from the substrate:

EXHIBIT 8 (02/16/2024)

	REDACTED
memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars;	YMTC's Accused Products include "memory cell strings, each of the memory cell strings is formed over a respective conductive pillar of the conductive pillars." Specifically, as shown below, YMTC's Accused Products include memory cell strings (with memory cells in cavities of the control gates) over the conductive pillars:

EXHIBIT 8 (02/16/2024)

	REDACTED Note that the '903 Patent explains that: "The term 'on', 'over', or 'overlying' does not imply any directionality as used herein unless otherwise explicitly stated as such." 10,872,903 Patent at 5:46-54.
a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a	YMTC's Accused Products include "a first control gate formed in a first device level, the memory cell strings including a memory cell string, the memory cell string including a first memory cell having a memory element formed in a cavity of the first control gate." Specifically, as shown below, YMTC's Accused Products include in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):

EXHIBIT 8 (02/16/2024)

memory element formed in a cavity of the first control gate;	REDACTED
a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the	YMTC's Accused Products include "a second control gate formed in a second device level, the memory cell string including a second memory cell having a memory element formed in a cavity of the second control gate; and." Specifically, as shown below, YMTC's Accused Products include in each device level, a control gate (e.g., word line) that is used to select memory cells, wherein in cavities of the control gate (e.g., word line) are memory elements (e.g., respective memory cells for that level of the memory strings):

EXHIBIT 8 (02/16/2024)

second control gate; and	REDACTED
a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars.	YMTC's Accused Products include "a conductive channel extending between the first memory cell and the second memory cell and electrically coupled to a conductive pillar of the conductive pillars." Specifically, as shown below, YMTC's Accused Products include memory strings that comprise the memory elements in respective device levels (in respective cavities of control gates), wherein the memory string forms a conductive channel that extends between the respective memory cells and forms a conductive path through the conductive pillar. The conductive channel runs through the memory cell string in the vertical direction and is electrically coupled to the conductive pillar.

EXHIBIT 8 (02/16/2024)

	REDACTED

Exhibit 9

US010373974B2

(12) **United States Patent**
Freeman et al.

(10) **Patent No.: US 10,373,974 B2**
(45) **Date of Patent: *Aug. 6, 2019**

(54) **MICROELECTRONIC DEVICES AND RELATED METHODS**

(71) Applicant: **Micron Technology, Inc.**, Boise, ID (US)

(72) Inventors: **Eric H. Freeman**, Kuna, ID (US); **Justin B. Dorhout**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **16/051,886**

(22) Filed: **Aug. 1, 2018**

(65) **Prior Publication Data**

US 2018/0350836 A1 Dec. 6, 2018

Related U.S. Application Data

(63) Continuation of application No. 15/666,064, filed on Aug. 1, 2017, now Pat. No. 10,062,708, which is a continuation of application No. 14/942,573, filed on Nov. 16, 2015, now Pat. No. 9,728,548.

(51) **Int. Cl.**
H01L 27/11573 (2017.01)
H01L 27/11575 (2017.01)
H01L 27/11582 (2017.01)

(52) **U.S. Cl.**
CPC .. ***H01L 27/11582*** (2013.01); ***H01L 27/11573*** (2013.01); ***H01L 27/11575*** (2013.01)

(58) **Field of Classification Search**
CPC H01L 27/11526; H01L 27/11551; H01L 27/11573; H01L 27/11578; H01L 27/11582
See application file for complete search history.

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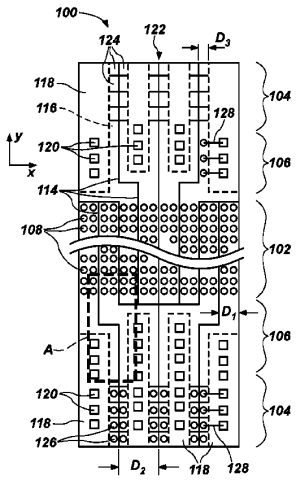
(Continued)

Primary Examiner — Allison Bernstein
(74) *Attorney, Agent, or Firm* — TraskBritt

(57) **ABSTRACT**

Vertical memory blocks for semiconductor devices include a memory cell region including an array of memory cell pillars and at least one via region including a dielectric stack of alternating dielectric materials and at least one conductive via extending through the dielectric stack. Semiconductor devices including a vertical memory block include at least one vertical memory block, which includes slots extending between adjacent memory cells of a three-dimensional array. The slots are separated by a first distance in a first portion of the block, and by a second, greater distance in a second portion of the block. Methods of forming vertical memory blocks include forming slots separated by a first distance in a memory array region and by a second, greater distance in a via region. At least one conductive via is formed through a stack of alternating first and second dielectric materials in the via region.

20 Claims, 8 Drawing Sheets



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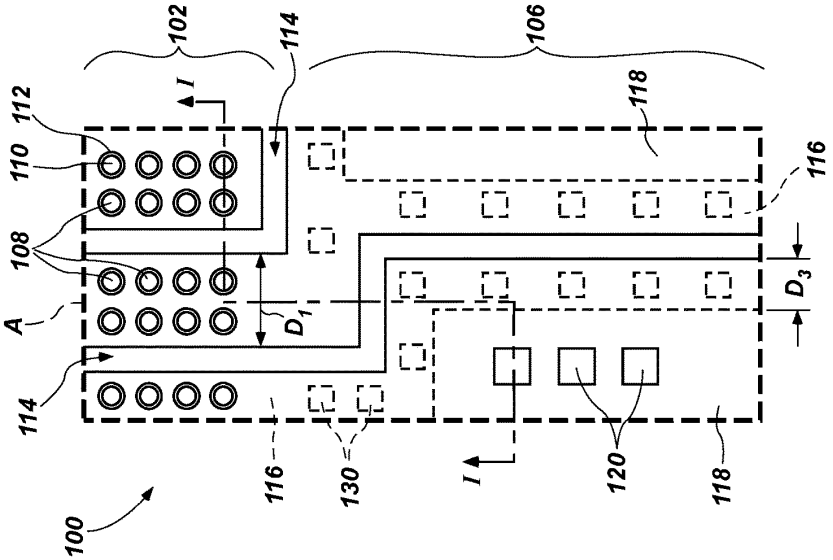

102
114
106
I
112
118
110
116
108
A
D_1
D_3
114
116
130
I
120
118
100

FIG. 2

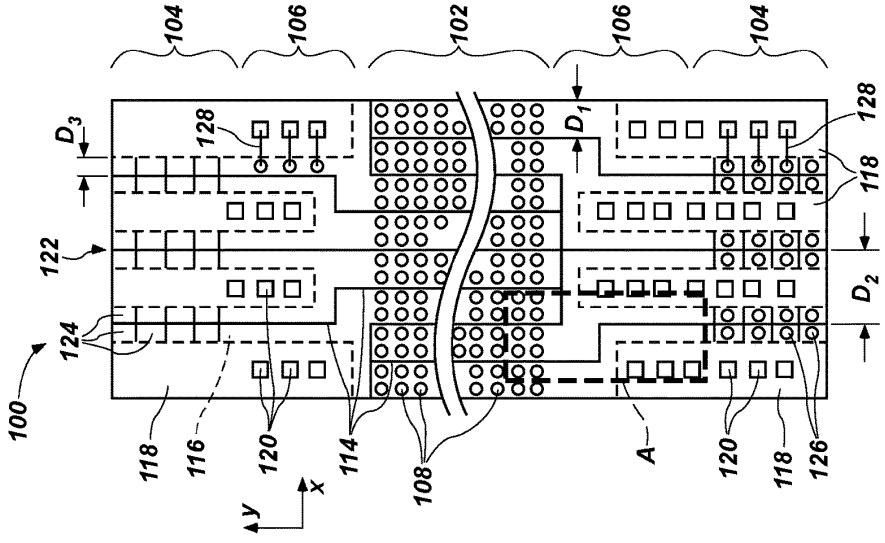

104
106
102
106
104
D_3
128
D_1
128
118
122
D_2
124
100
118
116
120
114
108
A
120
118
126
y
x

FIG. 1

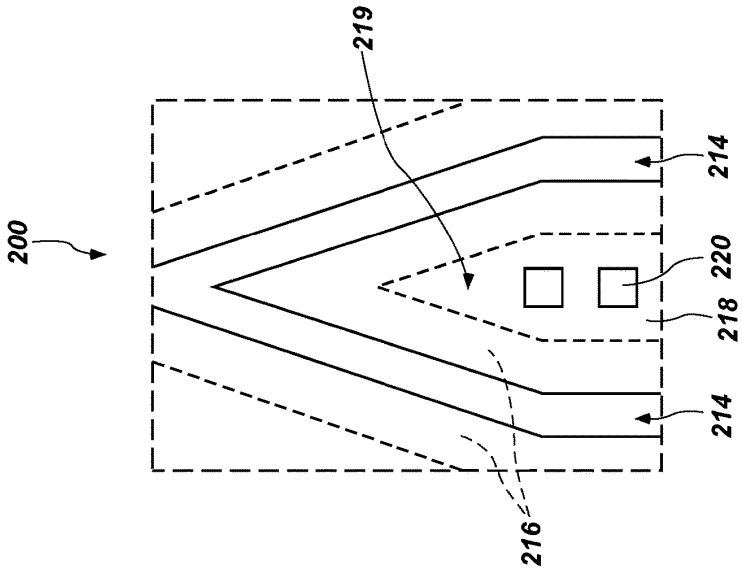

219
214
200
220
218
214
216

FIG. 4

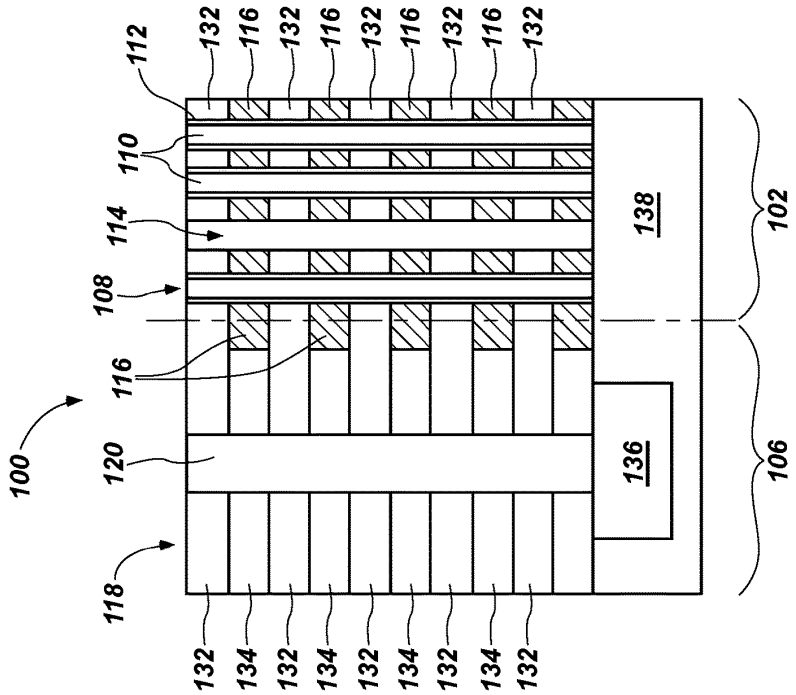

112
132
116
132
116
132
116
132
116
132
110
114
108
116
120
118
138
136
102
106
100
132
134
132
134
132
134
132
134
132

FIG. 3

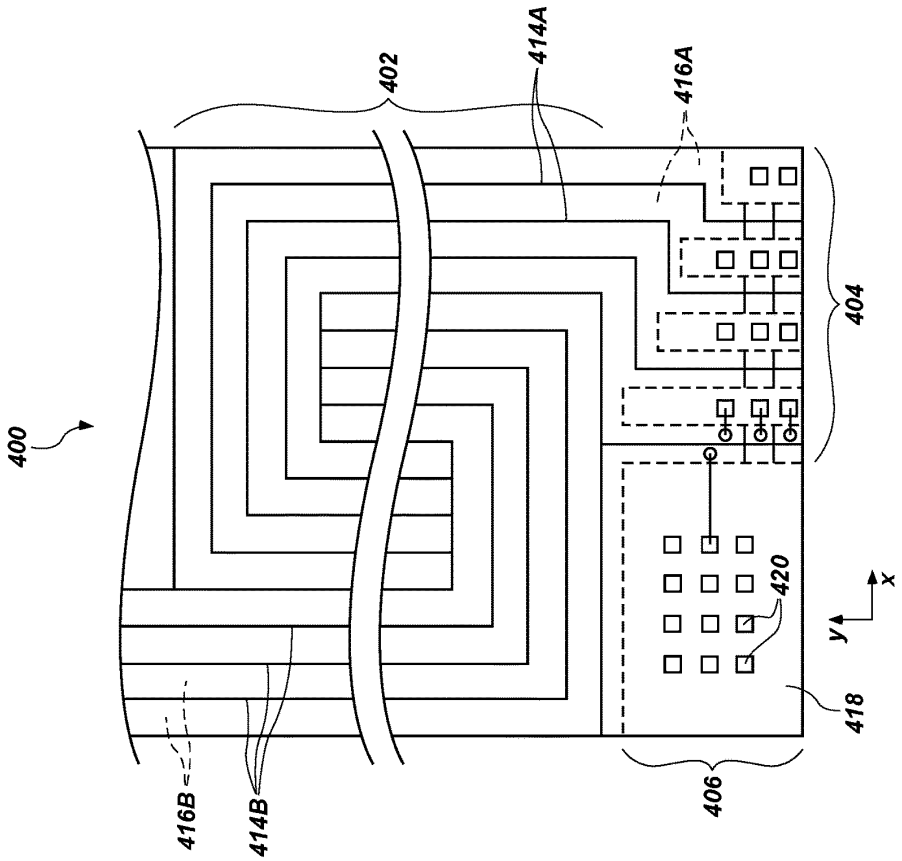

400
402
414A
416A
404
420
418
406
416B
414B
x
y

FIG. 6

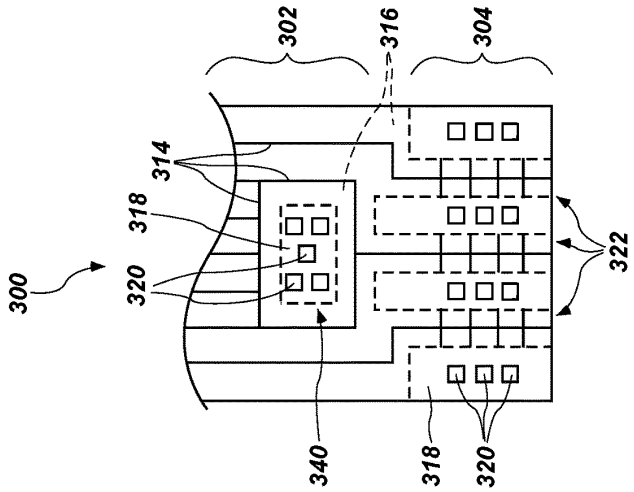

300
302
316
304
314
318
320
322
340
318
320

FIG. 5

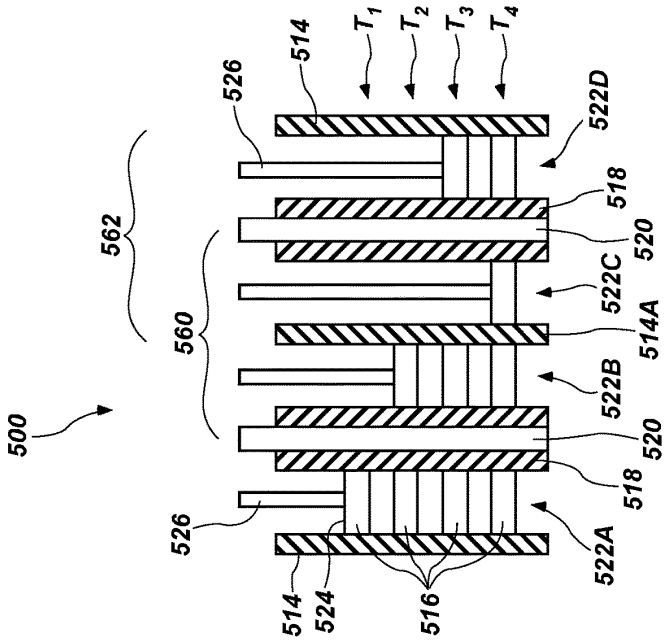

T_1
T_2
T_3
T_4
514
526
522D
518
520
522C
514A
522B
520
518
522A
562
560
500
526
514
524
516

FIG. 8

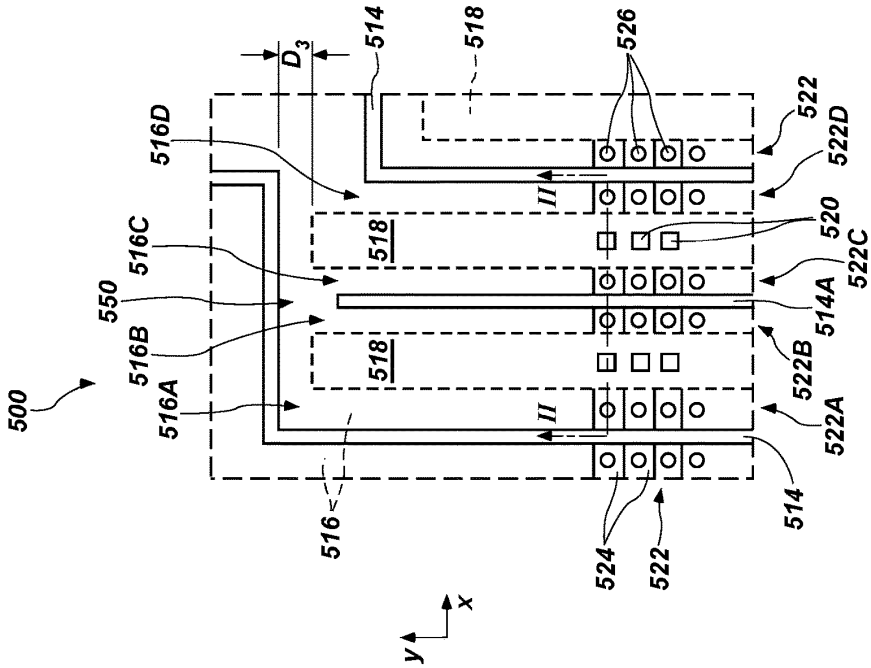

D_3
514
518
526
516D
522
522D
520
522C
514A
522B
522A
516C
550
516B
516A
518
518
500
II
II
516
524
522
514
x
y

FIG. 7

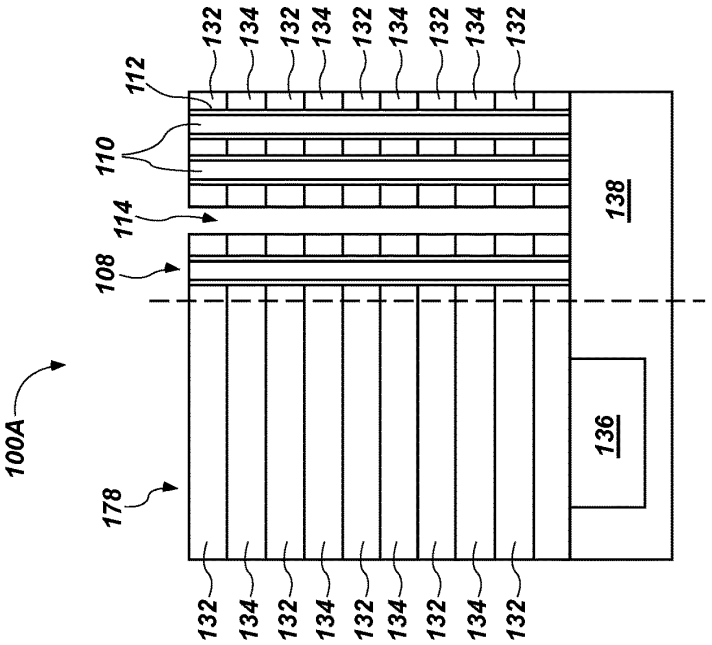

132
134
112
110
114
108
138
136
100A
178

FIG. 9B

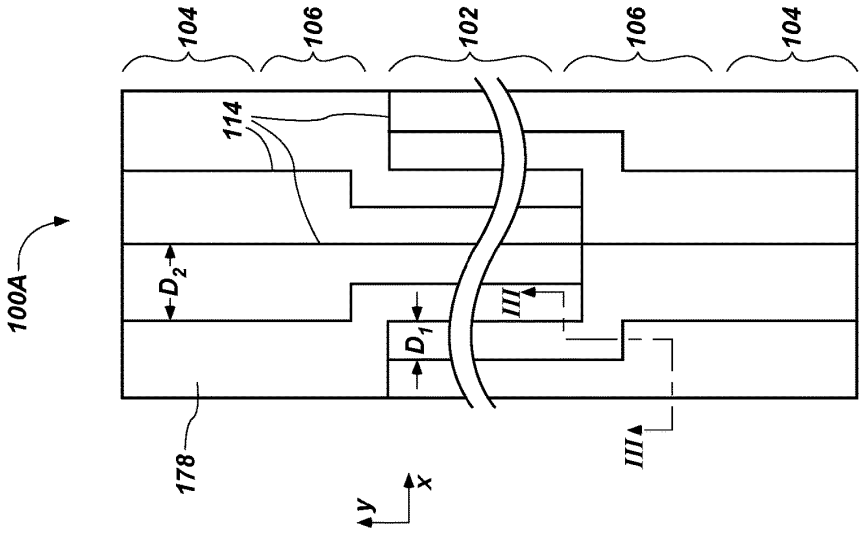

104
106
102
114
100A
D_2
D_1
III
178
y
x

FIG. 9A

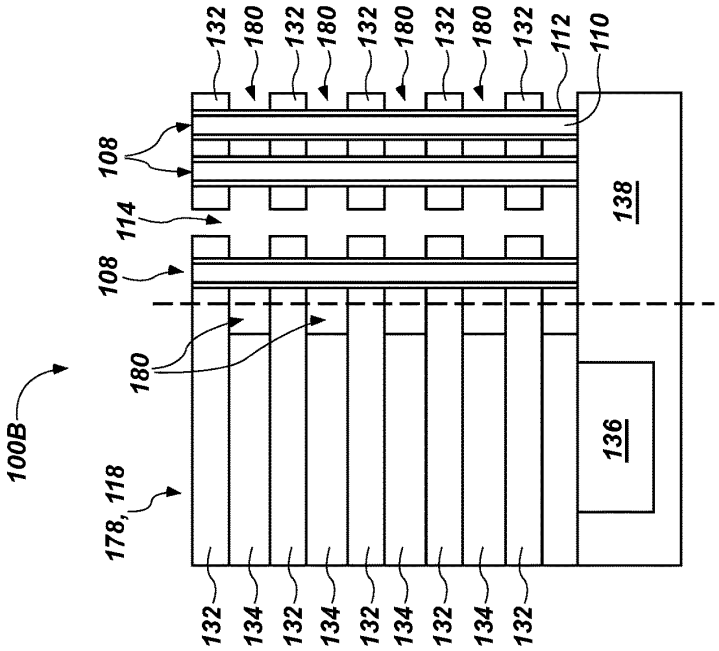


FIG. 10B

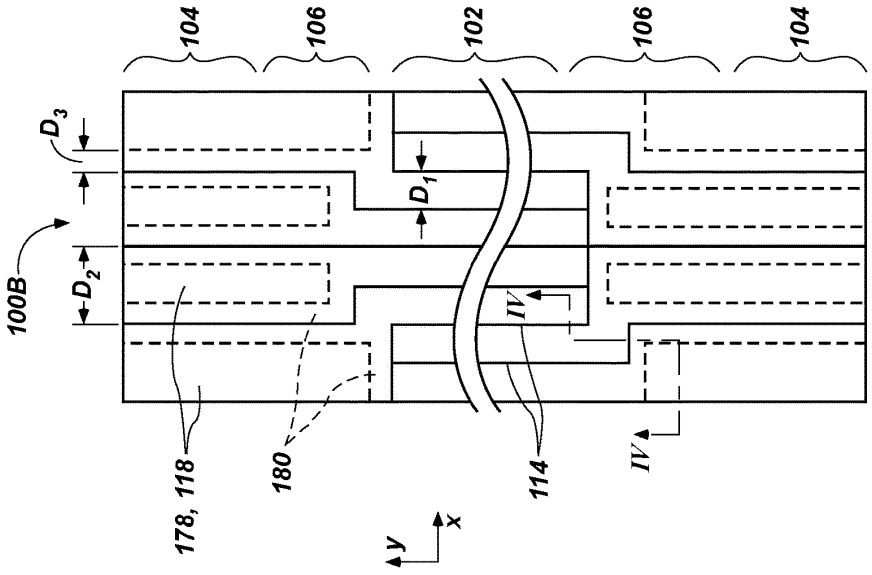


FIG. 10A

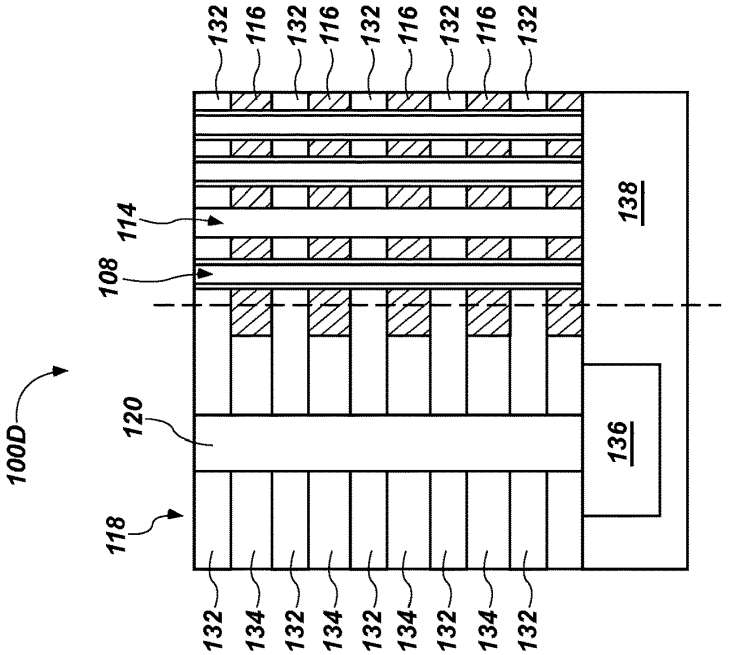

132
116
132
116
132
116
132
116
132
138
114
108
120
136
100D
118
132
134
132
134
132
134
132
134
132

FIG. 12

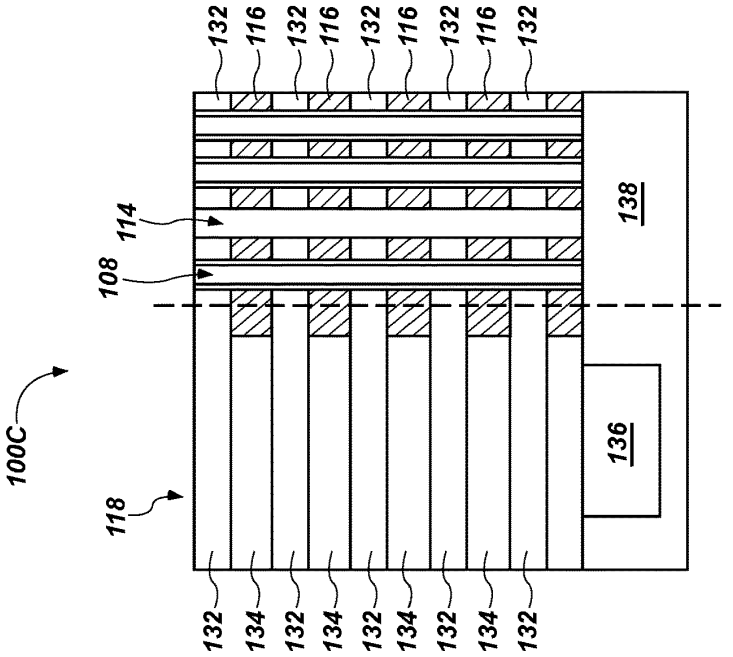

132
116
132
116
132
116
132
116
132
138
114
108
136
100C
118
132
134
132
134
132
134
132
134
132

FIG. 11

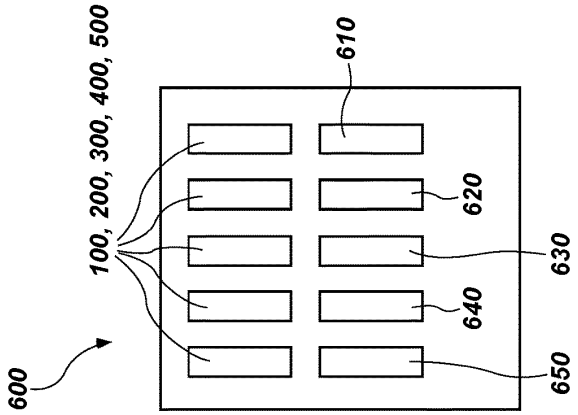

100, 200, 300, 400, 500
610
620
630
640
650
600

FIG. 14

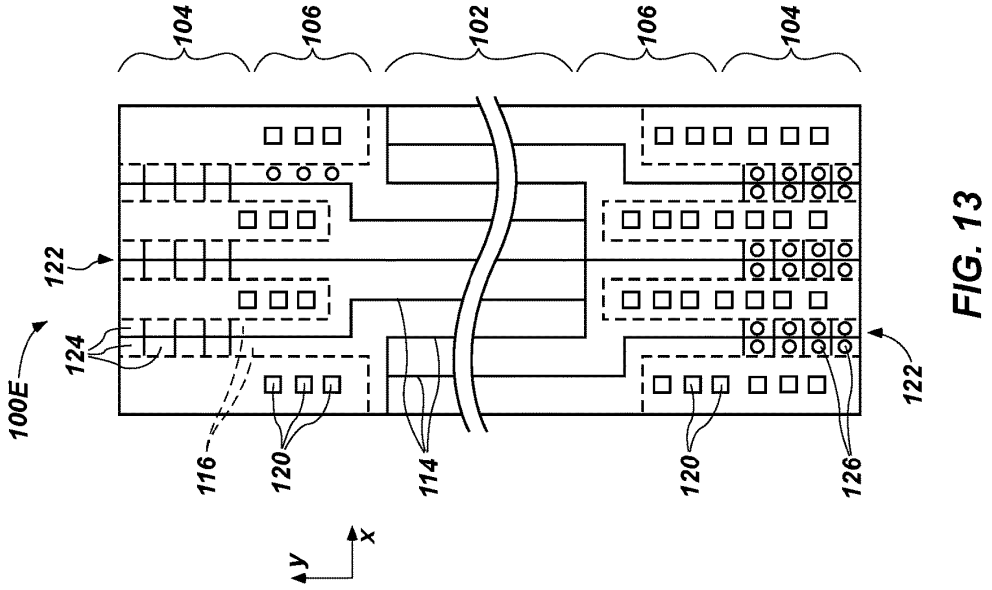

104
106
102
106
104
122
124
100E
116
120
114
120
126
122
y
x

FIG. 13

MICROELECTRONIC DEVICES AND RELATED METHODS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 15/666,064, filed Aug. 1, 2017, now U.S. Pat. No. 10,062,708, issued Aug. 28, 2018, which is a continuation of U.S. patent application Ser. No. 14/942,573, filed Nov. 16, 2015, now U.S. Pat. No. 9,728,548, issued Aug. 8, 2017, the disclosure of each of which is hereby incorporated herein in its entirety by this reference.

FIELD

Embodiments of the present disclosure relate to semiconductor devices including vertical memory block constructions that include slots for forming conductive elements within the vertical memory block. Embodiments of the present disclosure also relate to vertical memory blocks that include conductive through-array vias.

BACKGROUND

A continuing goal of the semiconductor industry has been to increase the memory density (e.g., the number of memory cells per memory die) of memory devices, such as non-volatile memory devices (e.g., NAND Flash memory devices). One way of increasing memory density in non-volatile memory devices is to utilize vertical memory array (also referred to as a "three-dimensional (3D) memory array") architectures. A conventional vertical memory array includes semiconductor pillars extending through openings in tiers of conductive structures (e.g., word line plates, control gate plates, access lines, word lines) and dielectric materials at each junction of the semiconductor pillars and the conductive structures. Such a configuration permits a greater number of transistors to be located in a unit of die area by building the array upwards (e.g., vertically) on a die, as compared to structures with conventional planar (e.g., two-dimensional) arrangements of transistors.

Conventional vertical memory arrays include tiers of conductive structures (e.g., access lines, word lines) separated by dielectric materials. One such vertical memory array is a so-called "MONOS" type memory array, which stands for metal-oxide-nitride-oxide-semiconductor, referring to the materials forming each individual memory cell. Conventional MONOS type memory arrays may be formed by forming the semiconductor pillars through a stack of alternating first and second dielectric materials, forming slots through the stack adjacent to the semiconductor pillars, removing the second dielectric materials through the slots, and replacing the second dielectric materials with a conductive material to form word line plates. During such a process, all or substantially all of the second dielectric material is replaced by the conductive material, such that a body of the vertical memory array includes alternating layers of the first dielectric material and the conductive word line plates.

Some conventional vertical memory arrays include so-called "through-array vias," which are conductive vias that extend through the vertical memory array to a sub-array feature. Through-array vias potentially reduce an area that the vertical memory array and associated circuitry covers on a semiconductor device, compared to vias or other contacts that are formed outside of an area of the vertical memory array. However, the formation of the through-array vias

requires additional processing acts and cost. For example, to conventionally form such through-array vias that are electrically isolated from the conductive word line materials, a portion of the alternating layers of the first dielectric material and the conductive word line material is removed and replaced with a dielectric material, through which the through-array vias are formed.

It would, therefore, be desirable to develop improved structures and methods of forming vertical memory arrays with through-array vias for semiconductor devices (e.g., vertical memory devices, such as NAND Flash memory devices) that reduce the number and complexity of additional processing acts practiced in conventional methods and structures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a schematic top view of a vertical memory block including via regions laterally adjacent to conductive word lines according to an embodiment of the present disclosure.

FIG. **2** shows a detailed top view of a portion of the vertical memory block of FIG. **1**, taken from dashed box A of FIG. **1**.

FIG. **3** shows a partial cross-sectional view taken of the vertical memory block of FIGS. **1** and **2**, taken from section line I-I of FIG. **2**.

FIG. **4** shows a top view of a portion of a vertical memory block with diverging slots and a via region having a variable width according to an embodiment of the present disclosure.

FIG. **5** shows a partial top view of a vertical memory block having a via region in a memory array region of the vertical memory block according to an embodiment of the present disclosure.

FIG. **6** shows a partial top view of a vertical memory block including an enlarged via region according to an embodiment of the present disclosure.

FIG. **7** shows a top view of a stair step region of a vertical memory block according to an embodiment of the present disclosure.

FIG. **8** shows a partial cross-sectional view of the stair step region of the vertical memory array block of FIG. **7**, taken from section line II-II of FIG. **7**.

FIGS. **9**A through **13** illustrate different views of a vertical memory block at progressive stages of forming the vertical memory block according to an embodiment of the present disclosure.

FIG. **14** shows a memory device including at least one vertical memory block according to an embodiment of the present disclosure.

DETAILED DESCRIPTION

The following description provides specific details, such as material types and processing conditions in order to provide a thorough description of embodiments of the present disclosure. However, a person of ordinary skill in the art will understand that the embodiments of the present disclosure may be practiced without employing these specific details. Indeed, the embodiments of the present disclosure may be practiced in conjunction with conventional fabrication techniques and materials employed in the industry, which are known to one of ordinary skill in the art.

The fabrication processes described herein do not describe a complete process flow for processing semiconductor structures. The remainder of the process flow is known to those of ordinary skill in the art. Accordingly, only

the methods and memory device structures necessary to understand embodiments of the present disclosure are described herein.

In the following detailed description, reference is made to the accompanying drawings, which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the present disclosure may be practiced. These embodiments are described in sufficient detail to enable a person of ordinary skill in the art to practice the present disclosure. However, other embodiments may be utilized, and structural, material, and electrical changes may be made without departing from the scope of the disclosure. The illustrations presented herein are not meant to be actual views of any particular system, device, structure, or process, but are idealized representations that are employed to describe the embodiments of the present disclosure. The drawings presented herein are not necessarily drawn to scale.

Similar structures or components in the various drawings may retain the same or similar numbering for the convenience of the reader; however, the similarity in numbering does not mean that the structures or components are necessarily identical in size, composition, configuration, or other property.

As used herein, the term "substantially" in reference to a given parameter, property, or condition means and includes to a degree that one skilled in the art would understand that the given parameter, property, or condition is met with a small degree of variance, such as within acceptable manufacturing tolerances. For example, a parameter that is substantially met may be at least about 90% met, at least about 95% met, or even at least about 99% met.

As used herein, any relational term, such as "first," "second," "over," "top," "bottom," "underlying," etc., is used for clarity and convenience in understanding the disclosure and accompanying drawings and does not connote or depend on any specific preference, orientation, or order, except where the context clearly indicates otherwise.

As used herein, the term "forming" means and includes any method of creating, building, or depositing a material. For example, forming may be accomplished by atomic layer deposition (ALD), chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering, co-sputtering, spin-coating, diffusing, depositing, growing, or any other technique known in the art of semiconductor fabrication. Depending on the specific material to be formed, the technique for forming the material may be selected by a person of ordinary skill in the art.

Embodiments of the present disclosure include memory devices including a vertical memory block that has one or more conductive vias extending through alternating dielectric materials in a via region thereof. The vertical memory block may include a three-dimensional (3D) array of MONOS-type memory cells having conductive access lines (e.g., metal word lines) extending through the 3D array adjacent to slots formed vertically through the 3D array. The slots may be separated from one another by a first distance in a memory array region of the vertical memory block. The slots may be separated by a second, greater distance in a via region of the vertical memory block, in which the one or more conductive vias are located and vertically extend. The via region may be located laterally adjacent to a stair step structure of the vertical memory block, longitudinally adjacent to the stair step structure, or in the memory array region of the vertical memory block.

FIG. **1** shows a top view of a vertical memory block **100** (also simply "memory block **100**") of a memory device (e.g., a semiconductor memory device) according to an embodiment of the present disclosure. Portions of the vertical memory block **100** depicted in FIG. **1** do not show all features, so that underlying structures and elements can be seen more clearly. FIG. **2** shows a detailed top view of a portion of the vertical memory block **100** of FIG. **1**, taken from dashed box A of FIG. **1**. FIG. **3** shows a partial cross-sectional view taken of the vertical memory block **100** of FIGS. **1** and **2**, taken from section line I-I of FIG. **2**.

Referring to FIG. **1**, the vertical memory block **100** may be elongated in a longitudinal direction y, may have a width in a lateral direction x, and may also have a height in a vertical direction in and out of the page from the perspective of FIG. **1**. By way of example and not limitation, the width of the vertical memory block **100** in the lateral direction x may be between about 3 μm and about 5 μm. In some embodiments, the width of the vertical memory block **100** in the lateral direction x may be about 3.4 μm. A memory array region **102** may be generally centrally located in the vertical memory block in the longitudinal direction y. The vertical memory block **100** may include a stair step region **104** at one or both longitudinal ends of the vertical memory block **100**. As shown in FIG. **1**, a via region **106** may be located longitudinally between the array region **102** and each of the stair step regions **104**.

FIG. **2** illustrates a detailed view, marked by dashed box A in FIG. **1**, of a portion of the memory array region **102** and the via region **106** of the vertical memory block **100** of FIG. **1**. Referring to FIGS. **1** and **2**, in the memory array region **102**, an array of memory cell pillars **108** may each extend vertically through the vertical memory block **100**. Each of the memory cell pillars **108** may include a central region **110** of a semiconductor material, such as a polysilicon or silicon-germanium material, at least partially surrounded by a charge trapping material **112**, such as an oxide-nitride-oxide ("ONO") material. Slots **114** (shown in FIG. **1** as solid lines), filled with a dielectric material (e.g., a silicon oxide material), may extend through the memory array region **102** proximate to and between adjacent memory cell pillars **108**.

As shown in FIGS. **1** and **2**, the slots **114** may be separated from each other by a first distance D_1 in the memory array region **102**. In some embodiments, the first distance D_1 may be between about 400 nm and about 1000 nm. As shown in FIG. **1**, in the via region **106**, at least some of the slots **114** may be separated from each other by a second distance D_2 that is greater than the first distance D_1. In some embodiments, the second distance D_2 is at least about twice the first distance D_1, such as about four times the first distance D_1. The slots **114** may be provided for the introduction of an electrically conductive (e.g., metal) material to be coupled to (e.g., into contact with) the memory cell pillars **108** throughout the memory array region **102** to form conductive word lines **116**, as will be explained below. The conductive word lines **116** are conductive word lines **116** in the embodiments shown herein, although the present disclosure is not so limited. As shown by dashed lines in FIGS. **1** and **2**, the conductive word lines **116** may extend along the slots **114** and be coupled to the memory cell pillars **108**. In some embodiments, the conductive word lines **116** may include a metal, such as titanium, tantalum, tantalum nitride, tungsten, or tungsten nitride. The conductive word lines **116** and memory cell pillars **108** may form an array of so-called "MONOS" (metal-oxide-nitride-oxide-semiconductor) memory cells. In some embodiments, the memory cells may be so-called "TANOS" (tantalum nitride-aluminum oxide-nitride-oxide-semiconductor) or "BETANOS" (band/barrier

engineered TANOS) memory cells, which are subsets of the general category of MONOS memory cells.

Where the slots **114** are sufficiently distant from each other, such as the slots **114** in the via region **106** separated by the second distance D_2, the conductive word lines **116** may have a width from the slots **114** of at least a third distance D_3. On the other hand, where the slots **114** are sufficiently close to one another, such as the slots **114** in the memory array region **102** separated by the first distance D_1 that is about twice the third distance D_3 or less, the conductive material may form a conductive word line **116** having a width greater than the third distance D_3 (e.g., a width of the first distance D_1).

In the via region **106**, adjacent conductive word lines **116** may be separated by dielectric stacks **118** of at least two different alternating dielectric materials (e.g., alternating oxide and nitride materials). Conductive vias **120** may extend through the vertical memory block **100** within the dielectric stacks **118**. Since the conductive vias **120** extend through the vertical memory block **100**, the conductive vias **120** are also referred to as "through-array vias" or "TAVs." Thus, the slots **114** being separated by the second distance D_2 in the via region **106** provides space for the conductive vias **120** to be positioned through the vertical memory block **100**, without having to use space beyond the footprint of the vertical memory block **100**.

Referring again to FIG. **1**, the stair step region **104** may include one or more stair step structures **122** for electrically contacting and accessing different overlapping conductive word lines **116**. The stair step structures **122** may include contact regions **124** (e.g., "stairs") (for clarity, labeled at the top portion of FIG. **1**, but also present in the bottom portion of FIG. **1**) arranged like a staircase. Word line contacts **126** (for clarity, shown and labeled at the bottom portion of FIG. **1**, but also present in the top portion of the vertical memory block shown in FIG. **1**) may physically and electrically contact the contact regions **124** of the stair step structures **122** to provide electrical access to the conductive word lines **116**.

In some embodiments, electrical connections **128** may connect the word line contacts **126** to respective conductive vias **120**, as shown near the bottom of FIG. **1**. In some embodiments, the electrical connections **128** may connect the conductive vias **120** to other portions of one or more of the conductive word lines **116**, as shown near the top of FIG. **1**. In some embodiments, the conductive vias **120** may be electrically connected to other features or elements within the vertical memory block **100** or external to the vertical memory block **100**.

Although FIG. **1** illustrates adjacent stair step structures **122** that are separated by dielectric stacks **118** of at least two different alternating dielectric materials in the via region **106**, the present disclosure is not so limited. For example, rather than splitting a single conductive word line **116** into two adjacent stair step structures **122**, two or more adjacent conductive word lines **116** may be merged into a single stair step structure **122**. Thus, the present disclosure includes various embodiments of vertical memory blocks with split and merged word lines **116** in different regions of the vertical memory blocks, depending upon the arrangement and proximity of the slots **114**.

Referring to FIG. **2**, dielectric support pillars **130** (shown as dashed squares) may, optionally, be located to support dielectric materials (e.g., oxide materials) in the vertical memory block **100** during fabrication. The memory cell pillars **108** may support the dielectric materials in the memory array region **102** during fabrication. However, in portions of the vertical memory block **100** that may lack memory cell pillars **108**, such as in the via region **106** or in the stair step region **104**, the dielectric support pillars **130** may be used to support the dielectric materials during fabrication of the vertical memory block **100**. The dielectric support pillars **130** may include a dielectric material, such as an oxide material (e.g., silicon dioxide).

FIG. **3** illustrates a partial cross-sectional view of the vertical memory block **100**, taken from section line I-I of FIG. **2**. In the memory array region **102**, the memory cell pillars **108** (each including the central region **110** of a semiconductor material at least partially surrounded by the charge trapping material **112**) and the slots **114** may vertically extend through a stack of alternating conductive word lines **116** and first dielectric materials **132**. An individual memory cell (e.g., a MONOS memory cell) may be formed at each junction between the respective conductive word lines **116** and memory cell pillars **108**. FIG. **3** illustrates five overlying conductive word lines **116** and five overlying first dielectric materials **132** between the conductive word lines **116**. Thus, the vertical memory block **100** shown in FIG. **3** has five tiers. However, the present disclosure is not limited to vertical memory blocks **100** with five tiers. Rather, vertical memory blocks according to the present disclosure may have any number of tiers, such as at least 16, 32, 36, or 72 tiers, by way of non-limiting examples.

In the via region **106**, conductive vias **120** (only one shown in FIG. **3**) vertically extend through the dielectric stack **118**. The dielectric stack **118** may include alternating first dielectric materials **132** and second dielectric materials **134**. By way of example and not limitation, the first dielectric materials **132** may include an oxide (e.g., silicon dioxide) material, and the second dielectric materials **134** may include a nitride (e.g., silicon nitride) material. To form the conductive word lines **116**, a portion of the second dielectric material **134** along the slots **114** may be selectively removed, while the first dielectric material **132** remains. A conductive material may then be formed to replace the second dielectric material **134** that was removed. Both the first and second dielectric materials **132**, **134** may be present in the dielectric stack **118** because the slots **114** are sufficiently far away from each other in the via region **106** that the second dielectric material **134** is not removed in the dielectric stack **118**. Thus, the first and second dielectric materials **132**, **134** remain and form the dielectric stack **118**, through which the conductive vias **120** may be formed to electrically isolate the conductive vias **120** from the conductive word lines **116**. The conductive vias **120** may be electrically coupled to sub-array circuitry **136**, such as a driver circuit, in or on a substrate **138**. For example, at least one of the conductive vias **120** may operatively couple the sub-array circuitry **136** to the vertical memory block **100**.

Vertical memory blocks **100** having the features and configurations described in the present disclosure may enable dense wiring with no exit channel for wires from a group of sub-blocks.

Although the present disclosure describes, by way of example, vertical memory blocks including arrays of MONOS memory cells, the present disclosure is not so limited. For example, the present disclosure may be applicable to any vertical memory block or device that is fabricated by forming memory cell materials prior to forming associated conductive materials (e.g., word lines, gate materials) coupled to the memory cell materials, such as through slots formed according to this disclosure. For example, the

present disclosure also applies to so-called "floating gate" memory cells including a metal control gate as a charge trapping material **112**.

Accordingly, vertical memory blocks are disclosed including a memory cell region and at least one via region. The memory cell region includes an array of memory cell pillars extending vertically through the vertical memory block. The at least one via region includes a dielectric stack of alternating dielectric materials and at least one conductive via extending through the dielectric stack.

Additionally, semiconductor devices including a vertical memory block are disclosed. The semiconductor devices include at least one driver circuit on or in a substrate and at least one vertical memory block having a longitudinal length and a lateral width on the substrate and operatively coupled to the at least one driver circuit. The at least one vertical memory block includes a three-dimensional array of memory cells, slots extending vertically through the at least one memory block laterally between adjacent memory cells of the three-dimensional array, and conductive access lines extending along and adjacent to the slots. The slots are separated by a first lateral distance in a first portion of the vertical memory block along the three-dimensional array of memory cells, and by a second, greater lateral distance in a second portion of the at least one vertical memory block adjacent to the three-dimensional array of memory cells.

Referring again to FIGS. **1** and **2**, rectangular (when viewed from the top as in FIGS. **1** and **2**) dielectric stacks **118** may be formed by routing the slots **114** from the first distance D_1 apart from each other to the second distance D_2 apart from each other in a step-wise fashion (i.e., by forming the slots **114** with 90 degree angles). However, the present disclosure is not so limited.

As shown in FIG. **4**, in some embodiments, a vertical memory block **200** may include slots **214** that gradually diverge from each other at an acute angle. Such diverging slots **214** may result in conductive word lines **216** and dielectric stacks **218** that are not rectangular. Rather, the dielectric stacks **218** between adjacent conductive word lines **216** (or adjacent portions of a single conductive word line **216**) may have a shape that includes a narrow end region **219** corresponding to the adjacent diverging slots **214**.

Referring to FIG. **5**, in some embodiments, a vertical memory block **300** may include a dielectric stack **318** through which conductive vias **320** extend that is positioned in a memory array region **302** of the vertical memory block **300** rather than in a separate via region. For example, an area **340** of the memory array region **302** may be left free of slots **314**, such that the dielectric stack **318** is between conductive word lines **316** along the slots **314** within the memory array region **302**.

Additionally or alternatively, one or more dielectric stacks **318** and associated conductive vias **320** may be positioned in a stair step region **304** of the vertical memory array **300**, such as adjacent to stair step structures **322**.

Accordingly, the dielectric stack **318** and associated conductive vias **320** may be located at any desired location (depending on, e.g., a location of sub-array circuitry to which the conductive vias **320** are to be connected) in the vertical memory block **300**. To locate the dielectric stack **318** and associated conductive vias **320** in a desired location, a sufficiently large space between adjacent slots **314** is provided at the desired location, such that adjacent conductive word lines **316** (or adjacent portions of a single conductive word line **316**) do not extend all the way across the space.

Referring to FIG. **6**, a vertical memory block **400** may include a relatively large (compared to the embodiments described above) dielectric stack **418** in a via region **406** adjacent to a stair step region **404**. A relatively wider (compared to the embodiments described above) memory array region **402** in the lateral direction x may be formed to provide additional lateral space for the dielectric stack **418** and associated conductive vias **420** in the via region **406**. The additional lateral space for the dielectric stack **418** may be utilized by spacing the conductive vias **420** farther apart, by forming additional conductive vias **420** therein, or both.

The width of the memory array region **402** may be increased without reducing a density of memory cells by routing slots **414**A, **414**B to fill the extra width. By way of example and not limitation, the slots **414**A, **414**B may be routed in an interlocking-J pattern. Thus, first slots **414**A for forming first conductive word lines **416**A associated with a first stair step region **404** (e.g., at the bottom of the memory array block **400** depicted in FIG. **6**) may extend away from the first stair step region **404** in a longitudinal direction y, laterally across a portion of the memory array block **400**, and longitudinally back towards the first stair step region **404**. Complementary, second slots **414**B for forming conductive word lines **416**B associated with another stair step region **404** (not shown in FIG. **6**, but in a direction toward the top of the memory array block **400** depicted in FIG. **6**) may extend away from the associated stair step region **404** in a longitudinal direction y, laterally across a portion of the memory array block **400**, and longitudinally back towards the second stair step region **404**. Thus, the width of the memory array region **402** and, consequently, of the vertical memory block **400**, may be enlarged while substantially filling the memory array region **402** with slots **414**A, **414**B and corresponding conductive word lines **416**A, **416**B, to maintain a density of memory cells coupled to the word lines **416**A, **416**B within the memory array region **402**.

Embodiments including slots **414**A, **414**B arranged in an interlocking-J pattern may enable each word line contact to connect to two or more conductive word lines **416**A, **416**B, such that the stair step region **404** may exhibit up to about four times the pitch between the slots **414**A, **414**B. The extra space may be used for a large array region **406** (as shown in FIG. **6**) or for multiple dielectric stacks **418** positioned throughout the stair step region **404**.

FIG. **7** shows a top view of a stair step region of a vertical memory block **500** according to an embodiment of the present disclosure. FIG. **8** shows a partial cross-sectional view of the stair step portion of the vertical memory block **500** of FIG. **7**, taken from section line II-II of FIG. **7**. The vertical memory block **500** of FIGS. **7** and **8** includes many features and elements that are similar to the vertical memory block **100** described above with reference to FIGS. **1** through **3**. For example, the vertical memory block **500** of FIGS. **7** and **8** includes slots **514**, conductive word lines **516**, dielectric stacks **518** of alternating dielectric materials, conductive vias **520** extending through the vertical memory block **500** within the dielectric stacks **518**, and stair step structures **522** including contact regions **524** for electrically contacting and accessing different overlapping conductive word lines **516** using word line contacts **526**. The conductive word lines **516** extend along the slots **514**. As discussed above, the conductive word lines **516** may have a width from the corresponding slots **514** that is the third distance D_3 in locations where the slots **514** are sufficiently far apart from each other (e.g., more than twice the third distance D_3). In locations where the slots **514** are apart from each other about twice the third distance D_3 or less, the conductive word lines

516 may have a greater width than the third distance D_3, as the material of the conductive word lines **516** formed from adjacent slots **514** contact or are integrally formed with each other.

However, compared to the vertical memory block **100** of FIGS. **1** through **3**, the vertical memory block **500** of FIGS. **7** and **8** includes an additional slot **514**A in the stair step region that splits one area of the conductive word lines **516** into four distinct word line portions **516**A, **516**B, **516**C, and **516**D that terminate in respective stair step structures **522**A, **522**B, **522**C, and **522**D. The additional slot **514**A may extend from the stair step structures **522**A, **522**B, **522**C, and **522**D in a longitudinal direction y to proximate (e.g., within about twice the third distance D_3 or less), but not connecting with, another one of the slots **514**. A word line connection region **550** may remain between the additional slot **514**A and the proximate slot **514**. As shown in FIG. **8**, multiple conductive word lines **516** may be vertically positioned over each other in tiers T_1, T_2, T_3, and T_4. Referring to a single conductive word line **516** (i.e., a conductive word line **516** at a particular tier T_1, T_2, T_3, or T_4), the four word line portions **516**A, **516**B, **516**C, and **516**D are physically and electrically connected to each other at the word line connection region **550**. Thus, due to the presence of the additional slot **514**A and the word line connection region **550** (FIG. **7**), the four word line portions **516**A, **516**B, **516**C, and **516**D at any one of the tiers T_1, T_2, T_3, or T_4 are physically and electrically connected fingers of the same conductive word line **516**.

As is known by those of ordinary skill in the art, stair step structures for electrical connection to conductive word lines (or word line plates) at the tiers of vertical memory blocks may be formed by utilizing a so-called "stair step mask" and, optionally, one or more so-called "chop masks." A stair step mask may be formed over the vertical memory block while leaving one step-width (e.g., a width of one contact region **524** measured in the longitudinal direction y) exposed. One or more tiers of conductive material (e.g., of the conductive word lines **516**) exposed through the stair step mask may be removed, such as by a first cycle of anisotropic material removal (e.g., etching). An edge of the stair step mask may be removed to recess the edge of the stair step mask and to expose another step-width, in addition to the original exposed step-width. Another cycle of material removal may be performed to remove another one or more tiers of conductive material exposed through the recessed stair step mask. The process may be repeated to form a desired number of contact regions (e.g., contact regions **524**, also referred to as "stairs").

A chop mask may be used cover one or more particular stair step structures or portions thereof (e.g., one or more of the stair step structures **522**, **522**A, **522**B, **522**C, **522**D), while leaving one or more other stair step structures or portions thereof exposed through the chop mask. The entire exposed one or more other stair step structures or portions thereof is vertically recessed, such that one or more exposed tiers is removed. Thus, the one or more stair step structures exposed through the chop mask may be vertically recessed from the one or more stair step structures that is covered by the chop mask, such that the one or more exposed stair step structures defines contact regions ("stairs") for tiers that are lower than the tiers having contact regions ("stairs") for the one or more stair step structures covered by the chop mask. A chop mask may be used before or after the stair step mask is used. Chop masks are used to provide contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover. In addition, process control of removing material utilizing a stair step mask to form a stair step structure, as described above, may be difficult to maintain for a large number of cycles (e.g., more than about 12 cycles) and tiers. A single chop mask may be used to double the number of contact regions ("stairs") of a stair step structure formed using a single stair step mask. By way of a non-limiting example, a stair step mask may be used to form a stair step structure of 12 contact regions, for accessing 12 respective tiers. A chop mask may be used to expose and access 12 additional tiers underlying the 12 tiers formed by the stair step mask alone.

Returning to methods and structures of the present disclosure, as shown in FIG. **8**, after (or, alternatively, before) a stair step mask is used to form an initial stair step structure, a first chop mask may be positioned to cover the first and fourth stair step structures **522**A, **522**D, while leaving the second and third stair step structures **522**B, **522**C exposed, as indicated under a first bracket **560** in FIG. **8**. One material removal cycle may be performed to remove exposed portions of the topmost conductive word line **516** in a first tier T_1. The first chop mask may be removed, and a second chop mask may be positioned to cover the first and second stair step structures **522**A, **522**B, while leaving the third and fourth stair step structures **522**C, **522**D exposed, as indicated under a second bracket **562** in FIG. **8**. Two material removal cycles may be performed to remove exposed portions of the conductive word lines **516** in a second tier T_2 and third tier T_3 in the third stair step structure **522**C, and to remove exposed portions of the two conductive word lines **516** in the first tier T_1 and a second tier T_2 of the fourth stair step structure **522**D. In this manner, a contact region **524** for the first tier T_1 may be defined in the first stair step structure **522**A, a contact region **524** for the second tier T_2 may be defined in the second stair step structure **522**B, a contact region **524** for the third tier T_3 may be defined in the fourth stair step structure **522**D, and a contact region **524** for the fourth tier T_4 may be defined in the third stair step structure **522**C.

In the embodiment shown in FIGS. **7** and **8**, four cycles of material removal may be performed in connection with each time a corresponding stair step mask is recessed, such that successively lower "stairs" in a single stair step structure **522**, **522**A, **522**B, **522**C, **522**D are four tiers lower than a successively higher "stair" in the same stair step structure **522**, **522**A, **522**B, **522**C, **522**D.

In some embodiments, a single material removal cycle may be performed in connection with each time a corresponding stair step mask is recessed to form "stairs." In such embodiments, assuming S number of stairs are formed using the stair step mask alone, a first chop mask may be used to remove exposed portions of the same S number of conductive word lines **516** from the second and third stair step structures **522**B, **522**C, and a second chop mask may be used to remove exposed portions of twice the S number of eight conductive word lines **516** from the third and fourth stair step structures **522**C, **522**D. The embodiment shown in FIGS. **7** and **8** is an example of such embodiments, in which the S number of stairs formed using the stair step mask alone is four.

Thus, in embodiments employing the additional slot **514**A and including a word line connection region **550**, as shown by way of example in FIGS. **7** and **8**, a single stair step mask and two chop masks may be sufficient to form distinct contact regions **524** for a quantity of tiers up to four times the number of contact regions **524** exposed by the single stair step mask alone.

FIGS. **9**A through **13** illustrate a method of forming a vertical memory block, such as the vertical memory block **100** of FIG. **1**. FIG. **9**A shows a top view of a vertical memory block structure **100**A, and FIG. **9**B shows a cross-sectional view of the vertical memory block structure **100**A taken from section line of FIG. **9**A. Referring to FIG. **9**B, a stack **178** of alternating first and second dielectric materials **132**, **134** is formed over the substrate **138**, which may include the sub-array circuitry **136**. The first dielectric material **132** may be, for example, an oxide material such as silicon dioxide. The second dielectric material **134** may be, for example, a nitride material such as silicon nitride. The memory cell pillars **108** may be formed in the memory array region **102** (FIG. **9**A), each of which may include the central region **110** of a semiconductor material at least partially surrounded by a charge trapping material **112**. By way of example, the memory cell pillars **108** may be formed by anisotropically removing portions of the first dielectric material **132** and second dielectric material **134** to form holes through the stack **178**, after which an oxide, nitride, and oxide material is formed along sidewalls defining the holes through the stack **178** to form the charge trapping material **112**. A semiconductor material may be formed to fill the remaining holes to form the central region **110** of the memory cell pillars **108**. Optionally, dielectric support pillars **130** (FIG. **2**) of a dielectric material (e.g., an oxide material, such as silicon dioxide) may additionally be formed in locations lacking memory cell pillars **108**, to provide support for the first dielectric materials **132** in those locations during subsequent operations.

Referring to FIGS. **9**A and **9**B, the slots **114** may be formed by anisotropically removing portions of the first dielectric material **132** and second dielectric material **134**. The slots **114** may be formed to be separated from adjacent slots **114** by a first distance D_1 in the memory array region **102** of the stack **178**, and at least some of the slots **114** in the stair step region **104** and the via region **106** may be separated by a second distance D_2 greater than the first distance D_1.

FIG. **10**A shows a top view of a vertical memory block structure **100**B formed from the vertical memory block structure **100**A of FIGS. **9**A and **9**B after additional processing. FIG. **10**B shows a cross-sectional view of the vertical memory block structure **100**B taken from section line IV-IV of FIG. **10**A.

Referring to FIGS. **10**A and **10**B, portions of the second dielectric material **134** of the stack **178** adjacent to the slots **114** may be removed through the slots **114**, such as by an isotropic material removal process that selectively removes the second dielectric material **134** relative to the first dielectric material **132** and the charge trapping material **112** of the memory cell pillars **108**. One of ordinary skill in the art is familiar with such isotropic removal processes. The material removal process may form access line gaps **180** (referred to below as "word line gaps **180**") between the first dielectric materials **132**. Based on the amount of time and chemistry used to remove the portions of the second dielectric material **134** and to form the word line gaps **180**, the word line gaps **180** may have a width from the slots **114** of the third distance D_3. The third distance D_3 may be about half the first distance D_1 between the slots **114** in the array region **102** or more, such that the word line gaps **180** extend from one slot **114** to an adjacent slot **114** in locations where the slots **114** are separated by the first distance D_1, such as in the memory array region **102**. The second distance D_2 may be about twice the first distance D_1 or more, such that portions of the stack **178** of alternating dielectric materials remains between adjacent slots **114** in locations where the slots **114** are separated by the second distance D_2, such as in the stair step region **104** and the via region **106**, to define the dielectric stacks **118** in those locations.

FIG. **11** shows a cross-sectional view of a vertical memory block structure **100**C formed from the vertical memory block structure **100**B of FIGS. **10**A and **10**B after additional processing. Referring to FIG. **11**, the word line gaps **180** (FIG. **10**B) may be filled with a conductive material (e.g., titanium, tantalum, tantalum nitride, tungsten, or tungsten nitride) to form the conductive word lines **116**. Any residual conductive material within the slots **114** may be removed, and the slots **114** may be filled with a dielectric material (e.g., an oxide material, a nitride material).

FIG. **12** shows a cross-sectional view of a vertical memory block structure **100**D formed from the vertical memory block structure **100**C of FIG. **11** after additional processing. Referring to FIG. **12**, conductive vias **120** may be formed to extend through the dielectric stacks **118** of the alternating first and second dielectric materials **132**, **134** to electrically contact the sub-array circuitry **136** in or on the substrate **138**. To form the conductive vias **120**, portions of the first and second dielectric materials **132**, **134** in the dielectric stacks **118** may be anisotropically removed to form through holes, which may be at least partially filed with a conductive via material (e.g., titanium, tantalum, tantalum nitride, tungsten, or tungsten nitride).

FIG. **13** is a top view of a vertical memory block structure **100**E formed from the vertical memory block structure **100**D of FIG. **12** after additional processing. As shown in FIG. **13**, ends of the conductive word lines **116** proximate longitudinal ends of the vertical memory block structure **100**E may be processed to form the stair step structures **122**, defining the contact regions **124** for electrically contacting and accessing the conductive word lines **116** of different tiers. As generally described above with reference to FIGS. **7** and **8**, the stair step structures **122** may be formed using a stair step mask and, optionally, one or more chop masks, as is known to one of ordinary skill in the art. After the stair step structures **122** are formed to define the contact regions **124**, the word line contacts **126** may be formed to physically and electrically contact the respective conductive word lines **116**. Electrical connections **128** (FIG. **1**) may be formed between the conductive vias **120** and other conductive elements, such as the word line contacts, for example.

Although the formation of the conductive vias **120** has been explained and illustrated as occurring subsequent to the formation of the conductive word lines **116** and the filling of the slots **114** with a dielectric material, the present disclosure is not so limited. For example, the conductive vias **120** may be formed prior to, during, or after the formation of the conductive word lines **116** and the filling of the slots **114** with a dielectric material. In some embodiments, the conductive vias **120** may be formed after forming the stair step structures **122**, such as during a same process in which the word line contacts **126** are formed.

The methods described herein enable the formation of through-array vias **120** without the need for removing conductive material **116** and other portions of the vertical memory block **100** in a separate material removal act to form the conductive vias **120**. Rather, the methods of the present disclosure utilize dielectric materials (e.g., the first and second dielectric materials **132**, **134**) that are already present during the formation of the vertical memory block **100** as a location for forming the conductive vias **120**. Such methods provide efficient use of the materials and processes used to form the vertical memory block **100**.

Accordingly, the present disclosure includes methods of forming a vertical memory block of a semiconductor device. In accordance with such methods, a stack of alternating first dielectric materials and second dielectric materials is formed. Portions of the first dielectric materials and second dielectric materials are removed to form slots extending through the stack. The slots are separated by a first distance in a memory array region of the vertical memory block and by a second, greater distance in a via region of the vertical memory array block. Portions of the second dielectric materials adjacent to the slots are removed to form access line gaps extending along the slots. Portions of the second dielectric material are left in the via region. A conductive material is formed within the access line gaps to form conductive access lines. At least one conductive via is formed to extend through the first dielectric materials and the second dielectric materials in the via region.

The present disclosure also includes devices and systems that include one or more of the vertical memory blocks **100**, **200**, **300**, **400**, **500** described above. As shown in FIG. **14**, a semiconductor memory device **600** may include one or more of the vertical memory blocks **100**, **200**, **300**, **400**, **500** described above. The semiconductor memory device **600** may also include additional elements, such as communication circuitry **610**, drivers **620**, a memory controller **630**, an amplifier **640**, and a decoder **650**, for example. In some embodiments, one or more of the additional elements may be formed under the vertical memory blocks **100**, **200**, **300**, **400**, **500** and electrically contacted using through-array vias (e.g., the conductive vias **120**, **220**, **320**, **420**, **520** described above). A semiconductor system may include a semiconductor memory device **600** as described herein.

The embodiments of the disclosure described above and illustrated in the accompanying drawing figures do not limit the scope of the invention, since these embodiments are merely examples of embodiments of the disclosure. The invention is encompassed by the appended claims and their legal equivalents. Any equivalent embodiments lie within the scope of this disclosure. Indeed, various modifications of the present disclosure, in addition to those shown and described herein, such as other combinations and modifications of the elements described, will become apparent to those of ordinary skill in the art from the description. Such embodiments, combinations, and modifications also fall within the scope of the appended claims and their legal equivalents.

What is claimed is:

1. A microelectronic device comprising:

at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:

an array of memory cells in a memory cell region;

stair step structures in at least one stair step region;

conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region;

access lines extending through the at least one memory block; and

a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.

2. The microelectronic device of claim **1**, wherein the at least one memory block comprises a connection region physically and operatively connecting the adjacent access line portions of the individual access lines to one another, each of the adjacent access line portions separated from one another by the dielectric material.

3. The microelectronic device of claim **2**, wherein four access line portions of a single access line are connected to one another through the connection region, at least two of the four access line portions separated from one another by the dielectric material within an additional slot terminating at the connection region.

4. The microelectronic device of claim **1**, wherein at least some of the stair step structures comprise:

individual tiers aligned at different vertical levels from one another within a respective stair step structure; and

contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.

5. The microelectronic device of claim **1**, wherein the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region.

6. The microelectronic device of claim **1**, wherein a pitch between adjacent access lines in the at least one stair step region is about four times greater than a pitch between the adjacent access lines in the memory cell region.

7. A method of forming a microelectronic device, the method comprising:

forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region;

forming an array of memory cells in the memory cell region;

forming stair step structures in the stair step region;

forming conductive vias in the via region;

forming access lines extending through the memory block;

forming slots extending between adjacent portions of individual access lines within the stair step region; and

forming a dielectric material within the slots.

8. The method of claim **7**, further comprising forming a connection region within at least some of the access lines, wherein forming the access lines comprises connecting the portions of the individual access lines to one another within the connection region.

9. The method of claim **7**, wherein forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.

10. The method of claim **7**, wherein forming the slots comprises dividing at least some of the individual access lines into four distinct portions.

11. The method of claim **7**, wherein forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots.

12. The method of claim **7**, wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.

13. The method of claim **7**, wherein:

forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials; and

forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

14. A method of forming a microelectronic device, the method comprising:

forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials;

forming access lines coupled to memory cells of the array of memory cells;

forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;

forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and

removing at least a portion of the stair step structures using at least one chop mask.

15. The method of claim **14**, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.

16. The method of claim **14**, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.

17. The method of claim **14**, wherein forming the at least one stair step region comprises:

forming the stair step mask over the stack while exposing a width of a first step;

removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask;

recessing an edge of the stair step mask to expose a width of a second step; and

removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.

18. The method of claim **14**, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises:

covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask; and

vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed.

19. The method of claim **14**, wherein forming the conductive vias comprises forming at least some of the conductive vias between the array of memory cells and the at least one stair step region.

20. The method of claim **14**, wherein forming the conductive vias comprises forming at least some of the conductive vias between adjacent stair step structures.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 10,373,974 B2
APPLICATION NO. : 16/051886
DATED : August 6, 2019
INVENTOR(S) : Eric H. Freeman and Justin B. Dorhout

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification
Column 11, Line 6, change "section line of" to --section line III-III of--

Signed and Sealed this
Tenth Day of September, 2019

Andrei Iancu
Director of the United States Patent and Trademark Office

Exhibit 10

REDACTED

EXHIBIT 10 (02/16/2024)

Micron's Exemplary Infringement Claim Chart for U.S. Patent No. 10,373,974

The following chart provides non-limiting examples, without the benefit of claim construction or discovery, of how YMTC's Accused Products (as that term is defined in the Complaint) meet every limitation, literally or under the doctrine of equivalents, of at least claim 1 of U.S. Patent No. 10,373,974. The referenced images are images from a 232L YMTC 1Tb TLC part. Micron reserves the right to amend, correct, supplement, or otherwise change its explanation of how YMTC's Accused Products meet the following claim limitations, including as the claims are construed, as discovery progresses, or as Micron's investigation continues. Micron takes no position on claim interpretation or scope at this time.

Claim Language	YMTC's Accused Products
A microelectronic device comprising:[1]	YMTC's Accused Products include "a microelectronic device" that includes the subsequent claim limitations. Specifically, as the below demonstrates, the YMTC Accused Products are microelectronic memory devices that include, for example, a memory array and access circuity (e.g., in the sub-array circuity): REDACTED

[1] By providing this disclosure, Micron does not concede that the preamble is a claim limitation.

EXHIBIT 10 (02/16/2024)

at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:	YMTC's Accused Products include "at least one memory block operatively coupled to sub-array circuitry" that includes the subsequent claim limitations. Specifically, as shown below, the memory block includes an array of memory cells, a staircase structure, and a contact area with conductive vias. Further, as shown below, sub-array circuitry interfaces to the memory block (e.g., CMOS access circuitry below and above the memory block): REDACTED
an array of memory cells in a memory cell region;	YMTC's Accused Products include "an array of memory cells in a memory cell region." REDACTED

EXHIBIT 10 (02/16/2024)

stair step structures in at least one stair step region;	YMTC's Accused Products include "stair step structures in at least one stair step region." Specifically, as shown below, YMTC's Accused Products include a staircase region with word line contacts that connect to respective control gates of the staircase structure: REDACTED
conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region;	YMTC's Accused Products include "conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region." Specifically, as shown below, YMTC's Accused Products include conductive vias through the alternating stack of word line gates and dielectric layers. REDACTED

EXHIBIT 10 (02/16/2024)

access lines extending through the at least one memory block; and	YMTC's Accused Products include "access lines extending through the at least one memory block." Specifically, as shown below, YMTC's Accused Products include an alternating stack of access lines (conductive word lines) and dielectric: REDACTED
a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.	YMTC's Accused Products include "a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region." Specifically, as shown below, there exists dielectric material within slots, wherein the slots extend through the stack (between portions of individual access lines, i.e., the word lines) within the staircase region:

	REDACTED Further, additional dielectric material is within slots as shown by the yellow lines below in a pan view of the staircase region:

EXHIBIT 10 (02/16/2024)

	REDACTED

Exhibit 11

UNITED STATES
SECURITIES AND EXCHANGE COMMISSION
Washington, D.C. 20549

FORM 10-K

(Mark One)

☒ **ANNUAL REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the fiscal year ended August 31, 2023

OR

☐ **TRANSITION REPORT PURSUANT TO SECTION 13 OR 15(d) OF THE SECURITIES EXCHANGE ACT OF 1934**

For the transition period from to
Commission file number 1-10658

Micron Technology, Inc.

(Exact name of registrant as specified in its charter)

Delaware	**75-1618004**
(State or other jurisdiction of incorporation or organization)	(IRS Employer Identification No.)
Address of principal executive offices, including zip code	**8000 S. Federal Way, Boise, Idaho 83716-9632**
Registrant's telephone number, including area code	**(208) 368-4000**

Securities registered pursuant to Section 12(b) of the Act:

Title of each class	**Trading Symbol**	**Name of each exchange on which registered**
Common Stock, par value $0.10 per share	MU	Nasdaq Global Select Market

Securities registered pursuant to Section 12(g) of the Act: **None**

Indicate by check mark if the registrant is a well-known seasoned issuer, as defined in Rule 405 of the Securities Act. Yes ☒ No ☐

Indicate by check mark if the registrant is not required to file reports pursuant to Section 13 or Section 15(d) of the Act. Yes ☐ No ☒

Indicate by check mark whether the registrant (1) has filed all reports required to be filed by Section 13 or 15(d) of the Securities Exchange Act of 1934 during the preceding 12 months (or for such shorter period that the registrant was required to file such reports), and (2) has been subject to such filing requirements for the past 90 days. Yes ☒ No ☐

Indicate by check mark whether the registrant has submitted electronically every Interactive Data File required to be submitted pursuant to Rule 405 of Regulation S-T (§ 232.405 of this chapter) during the preceding 12 months (or for such shorter period that the registrant was required to submit such files). Yes ☒ No ☐

Indicate by check mark whether the registrant is a large accelerated filer, an accelerated filer, a non-accelerated filer, a smaller reporting company, or an emerging growth company. See the definitions of "large accelerated filer," "accelerated filer," "smaller reporting company," and "emerging growth company" in Rule 12b-2 of the Exchange Act.

Large Accelerated Filer	Accelerated Filer	Non-Accelerated Filer	Smaller Reporting Company	Emerging Growth Company
☒	☐	☐	☐	☐

If an emerging growth company, indicate by check mark if the registrant has elected not to use the extended transition period for complying with any new or revised financial accounting standards provided pursuant to Section 13(a) of the Exchange Act. ☐

Indicate by check mark whether the registrant has filed a report on and attestation to its management's assessment of the effectiveness of its internal control over financial reporting under Section 404(b) of the Sarbanes-Oxley Act (15 U.S.C. 7262(b)) by the registered public accounting firm that prepared or issued its audit report. ☒

If securities are registered pursuant to Section 12(b) of the Act, indicate by check mark whether the financial statements of the registrant included in the filing reflect the correction of an error to previously issued financial statements. ☐

Indicate by check mark whether any of those error corrections are restatements that required a recovery analysis of incentive-based compensation received by any of the registrant's executive officers during the relevant recovery period pursuant to §240.10D-1(b). ☐

Indicate by check mark whether the registrant is a shell company (as defined in Rule 12b-2 of the Exchange Act). Yes ☐ No ☒

The aggregate market value of the voting and non-voting common equity held by non-affiliates was $47.9 billion based on the closing price reported on the Nasdaq Global Select Market on March 2, 2023. Shares of common stock held by each executive officer and director and by each person who owns 5% or more of the outstanding common stock were excluded as they may be deemed to be affiliates. This determination of affiliate status is not necessarily a conclusive determination for other purposes.

The number of outstanding shares of the registrant's common stock as of September 29, 2023 was 1,098,034,471.

DOCUMENTS INCORPORATED BY REFERENCE

Portions of the Proxy Statement for the registrant's Fiscal 2023 Annual Meeting of Shareholders to be held on January 18, 2024 are incorporated by reference into Part II and Part III of this Annual Report on Form 10-K.

Micron corporate profile

It's all about data

Data is today's new business currency, and memory and storage are a critical foundation for the data economy. Memory and storage innovations will help transform society and enable significant value *for all*.

Who we are

Micron designs, develops and manufactures industry-leading memory and storage products. By providing foundational capability for AI and 5G across data center, the intelligent edge, and consumer devices, we unlock innovation across industries including healthcare, automotive and communications. Our technology and expertise are central to maximizing value from cutting-edge computing applications and new business models which disrupt and advance the industry.

Our vision

As a global leader in memory and storage solutions, we are transforming how the world uses information to enrich life *for all*. By advancing technologies to collect, store and manage data with unprecedented speed and efficiency, we lead the transformation of data to intelligence. In a world of change, we remain nimble, delivering products that help inspire the world to learn, communicate and advance faster than ever.

Our commitment

Our customers depend on our innovative solutions every day. We dedicate ourselves to demonstrating our environmental conscience, an inclusive team culture where all voices are heard and respected, and engaging in our communities to enrich life *for all*.

Global product portfolio

DRAM | NAND | NOR | Solid-State Drives | Graphics and High Bandwidth Memory (HBM) | Managed NAND and Multichip Packages

Founded on October 5, 1978

Headquartered in
Boise, Idaho, USA

$15.5B
FY23 annual revenue

5th
Largest semiconductor company in the world*

136
On the 2023 Fortune 500

~54,000
Patents granted and growing**

17
Countries**

11
Manufacturing sites and 15 customer labs**

~43,000
Team members**

*Based on Gartner Market Share: Semiconductors by End Market Worldwide 2022 (April 2023), excluding IP/software revenue.
**Micron data as of August 31, 2023

Media inquiries
mediarelations@micron.com

Government inquiries
govaffairs@micron.com

Investor inquiries
investorrelations@micron.com

Connect with us on micron.com

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Micron's Global Presence



Micron's global presence map highlights locations that include our manufacturing sites, centers of excellence, customer labs, and large offices. Not all Micron locations are represented on this map.

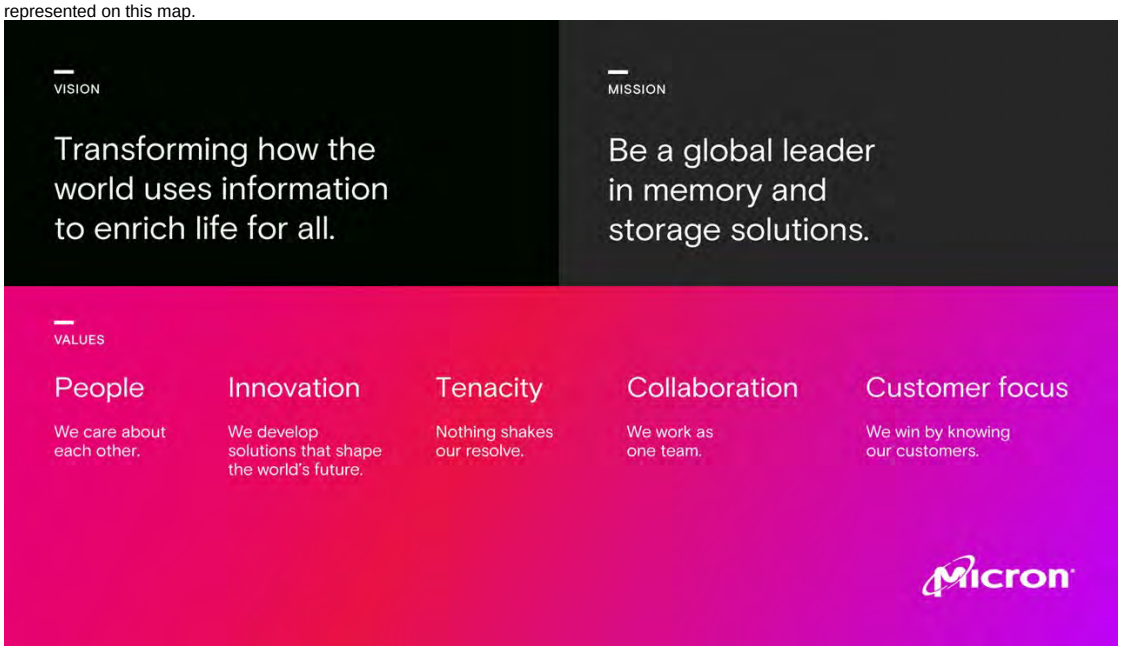


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Definitions of Commonly Used Terms

As used herein, “we,” “our,” “us,” and similar terms include Micron Technology, Inc. and its consolidated subsidiaries, unless the context indicates otherwise. Abbreviations, terms, or acronyms are commonly used or found in multiple locations throughout this report and include the following:

Term	Definition	Term	Definition
2023 Notes	2.497% Senior Notes due April 2023, repaid November 2021	GDDR	Graphics double data rate
2024 Notes	4.640% Senior Notes due February 2024, repaid November 2021	HBM	High-bandwidth memory, a stacked DRAM technology optimized for memory-bandwidth intensive applications
2024 Term Loan A	Senior Term Loan A due October 2024	Inotera	Inotera Memories, Inc.
2025 Term Loan A	Senior Term Loan A due November 2025	LIBOR	London Interbank Offered Rate
2026 Term Loan A	Senior Term Loan A due November 2026	LPDDR	Low-power double data rate DRAM
2027 Term Loan A	Senior Term Loan A due November 2027	LPDRAM	Low-power DRAM
2026 Notes	4.975% Senior Notes due February 2026	MCP	Multichip packaged solutions with managed NAND and LPDRAM
2027 Notes	4.185% Senior Notes due February 2027	Micron	Micron Technology, Inc. (Parent Company)
2028 Notes	5.375% Senior Notes due April 2028	MTU	Micron Technology Utah, LLC
2029 A Notes	5.327% Senior Notes due February 2029	Multi-Tranche Term Loan Agreement	Borrowing agreement executed November 3, 2022 that governs the 2025 Term Loan A, 2026 Term Loan A, and 2027 Term Loan A
2029 B Notes	6.750% Senior Notes due November 2029	NRV	Net realizable value
2030 Notes	4.663% Senior Notes due February 2030	OEM	Original equipment manufacturer
2032 Green Bonds	2.703% Senior Notes due April 2032	PCIe	High-speed motherboard connection for peripheral devices such as storage drives
2032D Notes	3.125% Convertible Senior Notes due May 2032, settled August 2021	Qimonda	Qimonda AG
2033 A Notes	5.875% Senior Notes due February 2033	QLC	Quad-level cell (four bits per cell)
2033 B Notes	5.875% Senior Notes due September 2033	Revolving Credit Facility	$2.5 billion Revolving Credit Facility due May 2026
2041 Notes	3.366% Senior Notes due November 2041	SATA	Hardware interface for connecting to storage devices such as hard disk drives and SSDs
2051 Notes	3.477% Senior Notes due November 2051	SLC	Single-level cell (one bit per cell)
AI	Artificial intelligence	SOFR	Secured Overnight Financing Rate
CAC	China’s Cyberspace Administration	SSD	Solid state drive
DDR	Double data rate DRAM	TI	Texas Instruments Incorporated
EBITDA	Earnings before interest, taxes, depreciation, and amortization	TLC	Triple-level cell (three bits per cell)
eMCP	Embedded multichip packaged solutions with embedded multimedia card storage and LPDDR	UFS	Universal flash storage
EUV	Extreme ultraviolet lithography	uMCP	UFS-based MCP
Extinguished 2024 Term Loan A	Senior Term Loan A due October 2024, repaid May 2021		

Micron, Crucial, any associated logos, and all other Micron trademarks are the property of Micron. 3D XPoint is a trademark of Intel Corporation or its subsidiaries. Other product names or trademarks that are not owned by Micron are for identification purposes only and may be the trademarks of their respective owners.

All period references are to our fiscal periods unless otherwise indicated. Our fiscal year is the 52 or 53-week period ending on the Thursday closest to August 31. Fiscal 2023, 2022, and 2021 each contained 52 weeks.

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Forward-Looking Statements

This Form 10-K contains trend information and other forward-looking statements that involve a number of risks and uncertainties. Such forward-looking statements may be identified by words such as "anticipate," "expect," "intend," "pledge," "committed," "plan," "opportunities," "future," "believe," "target," "on track," "estimate," "continue," "likely," "may," "will," "would," "should," "could," and variations of such words and similar expressions. However, the absence of these words or similar expressions does not mean that a statement is not forward-looking. Specific forward-looking statements include, but are not limited to, statements such as those made regarding expected production ramp of certain products; plans to implement EUV lithography; restructure plans and expected related savings; potential increases in our effective tax rate; the timing for construction and ramping of production for new memory manufacturing fabs in the United States; intent to make investments at our backend facility in Xi'an, China and build a new assembly and test facility in Gujarat, India; the receipt of government grants and investment tax credits; estimates of tax expense for 2024; the payment of future cash dividends; market conditions and profitability in our industry; potential write-downs of inventories in future quarters; the impact of the Cyberspace Administration of China decision; capital spending in 2024; the sufficiency of our cash and investments; allocation and dispersal of the net proceeds of our 2032 Green Bonds; and results of tax return examinations. Our actual results could differ materially from our historical results and those discussed in the forward-looking statements. Factors that could cause actual results to differ materially include, but are not limited to, those identified in "Part I – Item 1A. Risk Factors."

PART I
ITEM 1. BUSINESS

Overview

We are an industry leader in innovative memory and storage solutions transforming how the world uses information to enrich life *for all*. With a relentless focus on our customers, technology leadership, and manufacturing and operational excellence, Micron delivers a rich portfolio of high-performance DRAM, NAND, and NOR memory and storage products through our Micron® and Crucial® brands. Every day, the innovations that our people create fuel the data economy, enabling advances in artificial intelligence and 5G applications that unleash opportunities — from the data center to the intelligent edge and across the client and mobile user experience.

We manufacture our products at wholly-owned facilities and also utilize subcontractors for certain manufacturing processes. Our global network of manufacturing centers of excellence not only allows us to benefit from scale while streamlining processes and operations, but it also brings together some of the world's brightest talent to work on the most advanced memory technology. Centers of excellence bring expertise together in one location, providing an efficient support structure for end-to-end manufacturing, with quicker cycle times, in partnership with teams such as research and development ("R&D"), product engineering, human resources, procurement, and supply chain. For our locations in Singapore and Taiwan, this is also a combination of bringing fabrication and back-end manufacturing together. We make significant investments to develop proprietary product and process technology, which generally increases bit density per wafer and reduces per-bit manufacturing costs of each generation of product. We continue to introduce new generations of products that offer improved performance characteristics, including higher data transfer rates, advanced packaging solutions, lower power consumption, improved read/write reliability, and increased memory density.

We face intense competition in the semiconductor memory and storage markets and to remain competitive we must continuously develop and implement new products and technologies and decrease manufacturing costs in spite of ongoing inflationary cost pressures. Our success is largely dependent on obtaining returns on our R&D investments, efficient utilization of our manufacturing infrastructure, development and integration of advanced product and process technologies, market acceptance of our diversified portfolio of semiconductor-based memory and storage solutions, and efficient capital spending.

Sales, Markets, and Products

Product Technologies

Our product portfolio of memory and storage solutions, advanced solutions, and storage platforms is based on our high-performance semiconductor memory and storage technologies, including DRAM, NAND, and NOR. We sell our products into various markets through our business units in numerous forms, including components, modules, SSDs, managed NAND, MCPs, and wafers. Our system-level solutions, including SSDs and managed NAND, combine NAND, a controller, firmware, and in some cases DRAM.

***DRAM*:** DRAM products are dynamic random access memory semiconductor devices with low latency that provide high-speed data retrieval with a variety of performance characteristics. DRAM products lose content when power is turned off ("volatile") and are most commonly used in client, cloud server, enterprise, networking, graphics, industrial, and automotive markets. LPDRAM products, which are engineered to meet standards for performance and power consumption, are sold into smartphone and other mobile-device markets (including client markets for Chromebooks and notebook PCs), as well as into the automotive, industrial, and consumer markets.

***NAND*:** NAND products are non-volatile, re-writeable semiconductor storage devices that provide high-capacity, low-cost storage with a variety of performance characteristics. NAND is used in SSDs for the enterprise and cloud, client, and consumer markets and in removable storage markets. Managed NAND is used in smartphones and other mobile devices, and in consumer, automotive, and embedded markets. Low-density NAND is ideal for applications like automotive, surveillance, machine-to-machine, automation, printer, and home networking.

***NOR*:** NOR products are non-volatile re-writable semiconductor memory devices that provide fast read speeds. NOR is most commonly used for reliable code storage (e.g., boot, application, operating system, and execute-in-place code in an embedded system) and for frequently changing small data storage and is ideal for automotive, industrial, and consumer applications.

Products by Business Unit and Market

Compute and Networking Business Unit ("CNBU")

CNBU includes memory products and solutions sold into client, cloud server, enterprise, graphics, and networking markets. CNBU reported revenue of $5.71 billion in 2023, $13.69 billion in 2022, and $12.28 billion in 2021. CNBU sales in 2023 consisted primarily of DRAM products produced on 1x, 1y, 1z, and 1α (1-alpha) technology nodes. In 2023, we achieved several important product qualifications on our industry-leading 1ß (1-beta) DRAM node and are well positioned to ramp manufacturing of CNBU products in 2024.

Client: CNBU sales to the client market in 2023 consisted primarily of DDR4, DDR5, LPDDR5, and LPDDR4 DRAM products. Our products sold to the client market support both commercial and consumer PC unit growth.

Cloud Server: CNBU sales to the cloud market in 2023 consisted primarily of our DDR4 and DDR5 DRAM products. Overall cloud growth continues to be driven by the shift of both infrastructure and workloads from on-premises to the cloud. Cloud-native workloads are drivers of growth through use-cases like intelligent edge devices capable of AI and augmented reality that store and access data in the cloud or rely on the cloud for compute capability. Cloud servers supporting AI and data-centric workloads require significantly increasing quantities of DRAM, HBM, and NAND as the task of turning data into insight becomes increasingly memory-centric. As modern servers pack more processing cores into CPUs, the memory bandwidth per CPU core has been decreasing. Our DDR5 alleviates this bottleneck by providing higher bandwidth compared to previous generations, enabling improved performance and scaling. We expect that our new server DDR5 memory will be a key enabler of CPU core count growth and the bandwidth that DDR5 delivers will be central to unlocking overall server system performance gains for data-intensive workloads like AI and high-performance computing. HBM, used in high performance computing, had very strong demand this year, driven by demand for generative AI. We are working closely with our customers and have begun sampling our industry-leading HBM3E product offering. We expect to begin a mass production ramp for HBM3E in early calendar 2024. In 2023, we announced the introduction of 128GB and 256GB Compute Express Link ("CXL") 2.0 memory expansion modules. By leveraging a unique dual-channel memory architecture, we are able to deliver higher module capacity and increased bandwidth.

Enterprise: CNBU sales to the enterprise market in 2023 consisted primarily of our DDR4 and DDR5 DRAM products. In 2023, we announced volume shipments of our 96GB DDR5 high-density module built on 1α technology, using 24Gb die, which delivers equivalent performance for the majority of workloads versus the more expensive through-silicon via ("TSV") dual-die package-based 128GB modules. The enterprise market continues to grow beyond the mature OEM-sourced server consumption model with the further maturing of hybrid cloud and edge solutions as part of the digital transformation.

Graphics: CNBU sales to the graphics market in 2023 consisted primarily of GDDR6 graphics products. The graphics market is driven by the need for high-performance and HBM solutions. Our GDDR6 and GDDR6X DRAM graphics products are incorporated into gaming consoles, PC graphics cards, and graphics processing unit-based data center solutions, which are the driving force behind applications such as AI, virtual and augmented reality, 4K and 8K gaming, and professional design.

Networking: CNBU sales to the networking market in 2023 consisted primarily of DDR4 and DDR5 DRAM products. In 2023, demand was driven by 5G infrastructure deployments, data center networking growth, and increasing data transfer requirements across multiple industries.

Mobile Business Unit ("MBU")

MBU includes memory and storage products sold into the mobile market including discrete NAND, DRAM, and managed NAND products. MBU managed NAND includes embedded multi-media controller ("e.MMC") and universal flash storage ("UFS") solutions, each of which combine high-capacity NAND with a high-speed controller and firmware, and eMCP/uMCP products, which combine an e.MMC/UFS solution with LPDRAM. MBU reported revenue of $3.63 billion in 2023, $7.26 billion in 2022, and $7.20 billion in 2021. In 2023, we achieved key mobile customer qualifications on our 1ß based LPDDR5X and started high-volume revenue shipments to tier-1 OEMs. In addition, we achieved significant milestones in UFS with the qualification and ramp of a high-capacity uMCP5 featuring 16GB of DRAM and 512GB of NAND. We also started to sample a new UFS 4.0 product based on our latest 232-layer NAND technology, which enables industry-leading performance for flagship handsets.

Mobile: MBU sales to the mobile market in 2023 consisted primarily of LPDDR4 and LPDDR5 DRAM and managed NAND solutions. 5G-enabled products require higher DRAM and NAND content per device and the market penetration rate for 5G continued to increase. Our smartphone, tablet, and mobile PC products are utilized by OEMs to enable AI, augmented reality, and life-like virtual reality capabilities into high-end phones, including facial and voice recognition, real-time translation, fast image search, and scene detection.

Embedded Business Unit ("EBU")

EBU includes memory and storage products and solutions sold into automotive, industrial, and consumer markets and includes discrete and module DRAM, discrete NAND, managed NAND, SSDs, and NOR. EBU reported revenue of $3.64 billion in 2023, $5.24 billion in 2022, and $4.21 billion in 2021. The embedded market has traditionally been characterized by long life-cycle DRAM and non-volatile products manufactured on mature process technologies. Strong trends of digitization, connectivity, and intelligence in every device, are driving increasing demand in embedded markets for memory and storage products that incorporate leading process technologies. Our embedded products enable edge devices to store, connect, and transform information in the internet of things ("IoT") market and are utilized in a diverse set of applications in the automotive, industrial, and consumer markets.

Automotive: EBU sales to the automotive market in 2023 consisted primarily of LPDDR4 and LPDDR5 DRAM, DDR3 and DDR4 DRAM, and e.MMC managed NAND. Advancements in autonomous driving, advanced driver-assistance systems, and in-vehicle infotainment systems continue to increase the requirements for high-performing memory and storage products, with higher reliability requirements for leading-edge products. Automotive memory and storage products enable connected, advanced infotainment systems with increasingly larger and higher definition displays and support improved voice and gesture control. In addition, our products enable increasingly advanced vision and sensor based automated systems to support driver assistance solutions and vehicle safety. Our comprehensive and expanding portfolio of DRAM, NAND, and NOR solutions to the automotive market, as well as our extensive customer support network, enable us to maintain our strong leadership position in this market.

Industrial: EBU sales to the industrial market in 2023 consisted primarily of DDR3 and DDR4 DRAM, LPDDR4 DRAM, NAND MCPs, and SLC NAND. Our products enable applications in the growing industrial IoT market, including machine-to-machine communication, factory automation, transportation, surveillance, retail, and smart infrastructure.

Consumer: EBU sales to the consumer market in 2023 consisted primarily of our LPDDR4 and LPDDR5 DRAM, DDR4 and DDR3 DRAM, and SLC NAND. These embedded memory and storage solutions are used in a diverse set of consumer products, including service provider and IP set-top boxes, digital home assistants, digital still and video cameras, home networking, ultra-high definition televisions, augmented reality and virtual reality ("AR/VR") headsets, and many more applications. Our embedded memory and storage solutions enable edge devices in the consumer products market to store, connect, and transform information in the IoT.

Storage Business Unit ("SBU")

SBU includes SSDs and component-level solutions sold into enterprise and cloud, client, and consumer storage markets. SBU reported revenue of $2.55 billion in 2023, $4.55 billion in 2022, and $3.97 billion in 2021. In 2023, 176-layer NAND comprised the largest portion of SBU's NAND bit shipments. In 2023, we also began shipping client, consumer, and data center SSDs featuring 232-layer NAND technology. It features higher areal density and delivers higher capacity and improved energy efficiency over previous generations of our NAND, to enable best-in-class support of the most data-intensive use cases from client to cloud.

SSDs: SSD storage products incorporate NAND, a controller, and firmware and offer significant performance and features over hard disk drives, including smaller form factors, faster read and write speeds, higher reliability, and lower power consumption. We offer SSD solutions utilizing our NAND technology to the enterprise and cloud, client, and consumer markets.

Enterprise and Cloud SSDs: SBU sales to the enterprise and cloud SSD markets in 2023 consisted primarily of our 5300, 7450, 5400, 9400, and 6500 series SSDs. In data center SSDs, our entire portfolio is now on 176-layer or 232-layer NAND, demonstrating our product and technology leadership. We are in a strong position to serve AI demand for fast storage as these data-intensive applications proliferate. In 2023, we launched our first 200+ layer NAND data center SSD, and qualification has completed at some customers and is in progress at other customers largely to support AI cluster installations. The enterprise and cloud storage markets are driven by the growth of applications that store, access, and analyze data in the cloud. Applications such as machine learning servers require fast access to data with low latency, predictable performance, and high storage capacities.

Client SSDs: SBU sales to the client SSD market in 2023 consisted primarily of our 2450, 2400, and 3400 series client SSDs. Our client SSDs, targeted for leading personal computer OEMs, have mostly replaced hard disk drives used in notebooks, desktops, workstations, and other consumer applications, and deliver high performance, power efficiency, security, and capacity.

Consumer SSDs: SBU sales to the consumer SSD market in 2023 consisted primarily of our Crucial-branded MX500 and BX500 SATA SSDs and our P3, P3 Plus, and P5 Plus PCIe SSDs, which utilize our NAND QLC and TLC technologies. In 2023, we began production shipments of Crucial T700, a Gen5 PCIe consumer SSD built with our 232-layer NAND. Our consumer SSD solutions have mostly replaced hard disk drives as end users and system builders and integrators seek the higher performance, power savings, and reliability of SSDs.

Components: SBU sales of components in 2023 consisted primarily of our 96-layer, 176-layer, and 232-layer TLC and QLC NAND products.

Marketing and Customers

We seek to build collaborative relationships with our customers to understand their unique opportunities and challenges. By engaging with our customers early in the product life-cycle to identify and design features and performance characteristics into our products, we are able to manufacture products that anticipate and address our customers' changing needs. Collaborating with our customers on their design needs in changing end markets and meeting their timelines for qualifying new products allows us to differentiate our memory and storage solutions, which provides greater value to our customers.

Our semiconductor memory and storage products are offered under our Micron and Crucial brand names and through private labels. We market our semiconductor memory and storage products primarily through our own direct sales force and maintain sales or representative offices to support our worldwide customer base. Our products are also offered through distributors, retailers, and independent sales representatives. Our distributors carry our products in inventory and typically sell a variety of other semiconductor products, including our competitors' products. Our independent sales representatives obtain orders, subject to final acceptance by us, and we then make shipments against these orders directly to customers or through our distributors. We sell our Crucial-branded products through a web-based customer-direct sales channel as well as through channel and distribution partners. We maintain inventory at locations in close proximity to certain key customers to facilitate rapid delivery of products.

Due to volatile industry conditions, our customers are generally reluctant to enter into long-term, fixed-price purchase contracts. We typically enter into long-term agreements with our customers with acknowledgment that pricing, quantity, and other terms will be periodically negotiated to reflect market conditions and our customer's demand for our products.

In each of the last three years, approximately one-half of our total revenue was from our top ten customers. For other information regarding our concentrations and customers, see "Part II – Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Certain Concentrations."

Competitive Conditions

We face intense competition in the semiconductor memory and storage markets from a number of companies, including Kioxia Holdings Corporation; Samsung Electronics Co., Ltd.; SK hynix Inc.; and Western Digital Corporation. Our competitors may use aggressive pricing to obtain market share. Some of our competitors are large corporations or conglomerates that may have a larger market share and greater resources to invest in technology, capitalize on growth opportunities, and withstand downturns in the semiconductor markets in which we compete. Consolidation of industry competitors could put us at a competitive disadvantage as our competitors may benefit from increased manufacturing scale and a stronger product portfolio. We operate in different jurisdictions than our competitors and may be impacted by unfavorable changes in currency exchange rates.

In addition, some governments may provide, or have provided and may continue to provide, significant assistance, financial or otherwise, to some of our competitors or to new entrants and may intervene in support of national industries and/or competitors. In particular, we face the threat of increasing competition as a result of significant investment in the semiconductor industry by the Chinese government and various state-owned or affiliated entities, in companies such as Yangtze Memory Technologies Co., Ltd. ("YMTC") and ChangXin Memory Technologies, Inc. ("CXMT"). In addition, the May 21, 2023 decision by China's Cyberspace Administration (the "CAC") that critical information infrastructure operators in China may not purchase Micron products had an impact on our ability to compete effectively in China and elsewhere.

We and our competitors generally seek to increase wafer output, improve yields, and reduce die size, which could result in significant increases in worldwide supply and downward pressure on prices. During periods of supply overcapacity, the industry may experience a temporary interruption in increased wafer output due to curtailed capital expenditures. Increases in worldwide supply of semiconductor memory and storage also result from fabrication capacity expansions, either by way of new facilities, increased capacity utilization, or reallocation of other semiconductor production to semiconductor memory and storage production. Our competitors may increase capital expenditures resulting in future increases in worldwide supply. We, and some of our competitors, have plans to ramp, or are constructing or ramping, production at new fabrication facilities. Increases in worldwide supply of semiconductor memory and storage, if not accompanied by commensurate increases in demand, could lead to declines in average selling prices for our products and could materially adversely affect our business, results of operations, or financial condition. If competitors are more successful at developing or implementing new product or process technology, their products could have cost or performance advantages.

Manufacturing

We manufacture our products within our own facilities located in Taiwan, Singapore, Japan, the United States, Malaysia, and China, and also utilize subcontractors to perform certain manufacturing processes. Our products are manufactured on 300mm wafers in facilities that generally operate 24 hours per day, seven days per week. Semiconductor manufacturing is capital intensive, requiring large investments in sophisticated facilities and equipment. Our DRAM, NAND, and NOR products share a number of common manufacturing processes, enabling us to leverage our product and process technology and certain resources and manufacturing infrastructure across these product lines.

Our process for manufacturing semiconductor products is complex and involves numerous precise steps, including wafer fabrication, post fabrication processing, assembly, and test. Efficient production of semiconductor products requires utilization of advanced semiconductor manufacturing techniques and effectively deploying those techniques across multiple facilities. The primary determinants of manufacturing cost are process line-width, 3D non-volatile layers, NAND cell levels, process complexity (including the number of mask layers and fabrication steps), and manufacturing yield. Other factors include the cost and sophistication of manufacturing equipment, equipment utilization, cost of raw materials, labor productivity, package type, cleanliness of our manufacturing environment, and utilization of subcontractors to perform certain manufacturing processes. As we continue to increase our production of high value products and solutions, manufacturing costs are increasingly affected by the costs of application-specific integrated circuit ("ASIC") controllers and other semiconductors, advanced and complex packaging configurations, and testing at progressively higher performance speeds and quality levels. We continuously enhance our production processes, increase bits per wafer, transition to higher density products, and utilize advanced testing and assembly processes.

Wafer fabrication occurs in a highly-controlled clean environment to minimize yield loss from contaminants. Despite stringent manufacturing controls, individual circuits may be nonfunctional or wafers may be scrapped due to equipment errors, minute impurities in materials, defects in photomasks, circuit design marginalities or defects, or contamination from airborne particles, among other factors. Success of our manufacturing operations depends largely on minimizing defects and improving process margin to maximize yield of high-quality circuits. In this regard, we employ rigorous quality controls throughout the manufacturing, screening, and testing processes. We continue to heighten quality control as our product offerings expand into higher-end segments that require increasing performance targets.

Our products are manufactured and sold in both packaged form and as unpackaged bare die. Our packaged products include packaged die, memory modules, and system-level solutions, such as SSDs, managed NAND, and MCPs. We assemble many products in-house and, in some cases, outsource assembly services for certain packaged die, memory modules, SSDs, and MCPs. We test our products at various stages in the manufacturing process, conduct numerous quality control inspections throughout the entire production flow, and perform high temperature burn-in on finished products. In addition, we use our proprietary AMBYX™ line of intelligent test and burn-in systems to perform simultaneous circuit tests of semiconductor die, capturing quality and reliability data and reducing testing time and cost.

In recent years, we have produced an increasingly broad portfolio of products and system solutions, which enhances our ability to allocate resources to our most profitable products but also increases the complexity of our manufacturing and supply chain operations. Although our product lines generally use similar manufacturing processes, our costs can be affected by frequent conversions to new products; the allocation of manufacturing capacity to more complex, smaller-volume products; and the reallocation of manufacturing capacity across various product lines.

Resources

Supply Chain, Materials, and Third-Party Service Providers

Our supply chain and operations are dependent on the availability of materials that meet exacting standards and the use of third parties to provide us with components and services. We generally have multiple sources of supply for our materials and services. However, only a limited number of suppliers are capable of delivering certain materials, components, and services that meet our standards and, in some cases, materials, components, or services are provided by a single or sole source, and we may be unable to qualify new suppliers on a timely basis. The availability of materials or components such as chemicals, silicon wafers, gases, photoresist, controllers, substrates, lead frames, printed circuit boards, targets, and reticle glass blanks is impacted by various factors. These factors could include a shortage of raw materials or a disruption in the processing or purification of those raw materials into finished goods. Shortages or increases in lead times have occurred in the past, are currently occurring with respect to some materials and components, and may occur from time to time in the future. Constraints within our supply chain for certain materials and integrated circuit components could limit our bit shipments, which could have a material adverse effect on our business, results of operations, or financial condition.

Our manufacturing processes are also dependent on our relationships with third-party manufacturers of controllers, analog integrated circuits, and other components used in some of our products and with outsourced semiconductor foundries, assembly and test providers, contract manufacturers, logistics carriers, and other service providers, including providers of electricity and other utilities. Although we have certain long-term contracts with some of our suppliers, many of these contracts do not provide for long-term capacity or pricing commitments. To the extent we do not have firm commitments from our third-party suppliers over a specific time period or for any specific capacity, quantity, and/or pricing, our suppliers may allocate capacity to their other customers and capacity and/or materials may not be available when needed or at reasonable prices. Inflationary pressures have increased, and may continue to increase costs for materials, supplies, and services. Regardless of contract structure, large swings in demand may exceed our contracted supply and/or our suppliers' capacity to meet those demand changes resulting in a shortage of parts, materials, or capacity needed to manufacture our products. In addition, if any of our suppliers was to cease operations or become insolvent, this could impact their ability to provide us with necessary supplies, and we may not be able to obtain the needed supply in a timely way or at all from other providers.

Certain materials are primarily available in a limited number of countries, including rare earth elements, minerals, and metals. Trade disputes, geopolitical tensions, economic circumstances, political conditions, or public health issues may limit our ability to obtain such materials. Although these rare earth and other materials are generally available from multiple suppliers, China is the predominant producer of certain of these materials. If China were to restrict or stop exporting these materials, our suppliers' ability to obtain such supply may be constrained and we may be unable to obtain sufficient quantities, or obtain supply in a timely manner, or at a commercially reasonable cost. Constrained supply of rare earth elements, minerals, and metals may restrict our ability to manufacture certain of our products and make it difficult or impossible to compete with other semiconductor memory and storage manufacturers who are able to obtain sufficient quantities of these materials from China.

We and/or our suppliers and service providers could be affected by regional conflicts, civil unrest, labor disruptions, sanctions, tariffs, embargoes, or other trade restrictions, as well as laws and regulations enacted in response to concerns regarding climate change, conflict minerals, responsible sourcing practices, public health crises, or other matters, which could limit the supply of our materials and/or increase the cost. Environmental regulations could limit our ability to procure or use certain chemicals or materials in our operations or products. In addition, disruptions in transportation lines could delay our receipt of materials. Our ability to procure components to repair equipment essential for our manufacturing processes could also be negatively impacted by various restrictions or disruptions in supply chains, among other items. The disruption of our supply of materials, components, or services, or the extension of our lead times could have a material adverse effect on our business, results of operations, or financial condition.

Our inability to source materials, supplies, capital equipment, or third-party services could affect our overall production output and our ability to fulfill customer demand. Significant or prolonged shortages of our products could halt customer manufacturing and damage our relationships with these customers. Any damage to our customer relationships as a result of a shortage of our products could have a material adverse effect on our business, results of operations, or financial condition.

Similarly, if our customers experience disruptions to their supplies, materials, components, or services, or the extension of their lead times, they may reduce, cancel, or alter the timing of their purchases with us, which could have a material adverse effect on our business, results of operations, or financial condition.

Patents and Licenses

As of August 31, 2023, we owned approximately 13,100 active U.S. patents and 6,300 active foreign patents. In addition, we have thousands of U.S. and foreign patent applications pending. Our patents have various terms expiring through 2042.

From time to time, we sell and/or license our technology to other parties and continue to pursue opportunities to monetize our investments in our intellectual property through partnering and other arrangements. We have also jointly developed memory and storage product and process technology with third parties on a limited basis.

We have a number of patent and intellectual property license agreements and have, from time to time, licensed or sold our intellectual property to third parties. Some of these license agreements require us to make one-time or periodic payments while others have resulted in us receiving payments. We may need to obtain additional licenses or renew existing license agreements in the future, and we may enter into additional sales or licenses of intellectual property and partnering arrangements. We are unable to predict whether these license agreements can be obtained or renewed on terms acceptable to us.

Research and Development

Our R&D efforts are focused primarily on development of memory and storage solutions, including our industry-leading DRAM and NAND technology, that enable continuous improvement in performance and cost structure for our products. In DRAM, our 1ß node was introduced ahead of the industry and we ramped our manufacturing of it during 2023. We plan to implement EUV lithography on the DRAM node after 1ß. In NAND, the introduction of our 232-layer node was also ahead of the industry and we ramped our manufacturing of it during 2023. We are also focused on developing new fundamentally different memory structures, materials, and packages designed to facilitate our transition to next generation products. Additional R&D efforts are concentrated on the enablement of advanced computing, storage, and mobile memory architectures and the investigation of new opportunities that leverage our core semiconductor expertise. Product design and development efforts include high-density DDR5, LPDDR5, HBM, CXL based products, and advanced graphics DRAM; 3D NAND (including TLC and QLC technologies); mobile and storage solutions (including firmware and controllers); managed NAND; SSDs; and other memory technologies and systems.

To compete in the semiconductor memory and storage markets, we must continue to develop technologically advanced products and processes. The continued evolution of our semiconductor product offerings is necessary to meet expected customer requirements for memory and storage products and solutions. Our process, design, firmware, controller, package, and system development efforts occur at multiple locations across the world. Our primary R&D centers are located in Boise, Idaho; India; Japan; Taiwan; China; Italy; Singapore; Germany; Malaysia; and other sites in the United States.

R&D expenses vary primarily with the number of development and pre-qualification wafers processed and end-product solutions developed, personnel costs, and the cost of advanced equipment dedicated to new product and process development, such as investments in EUV lithography equipment. Because of the lead times necessary to manufacture our products, we typically begin to process wafers before completion of performance and reliability testing. Development of a product is deemed complete when it is qualified through internal reviews and tests for performance, functionality, and reliability. R&D expenses can vary significantly depending on the timing of product qualification.

Human Capital

We depend on a highly educated and experienced workforce to design, develop, and manufacture high-quality, cutting-edge memory and storage solutions. As of August 31, 2023, we had approximately 43,000 employees located in the following regions:

Region	Percent All	Percent Women
Asia	78 %	34 %
Americas	20 %	20 %
Europe, Middle East, and Africa	2 %	21 %
Total	100 %	31 %

As of August 31, 2023 and September 1, 2022, 31% of our global workforce were women. As of August 31, 2023, 25% of our technical or engineering roles were held by women, as compared to 24% as of September 1, 2022. Women comprised 17% of our senior leaders as of August 31, 2023 and September 1, 2022.

Our Board of Directors was comprised of four men and four women as of August 31, 2023. In addition, as of August 31, 2023, based on self-identification, one member of our Board of Directors is Asian, one member is African-American, and six members are White. One member of our Board of Directors is a veteran of the U.S. military.

Talent Acquisition, Development, and Engagement

Finding and retaining the best and brightest people in an extremely competitive industry environment is a strategic imperative for our business. We partner with our communities, institutions, governments, and associations to expand the pipeline of diverse, highly skilled STEM talent globally. Our partnerships with K-12 and post-secondary education systems are key to training and inspiring the next generation to consider STEM careers in the semiconductor industry. We use AI to reduce or eliminate the potential for bias from resumes, allowing us to focus on individual merit over personal characteristics. We are committed to developing team members at all stages of their careers, including on-the-job training, continuing education, a robust mentoring program, and numerous internal certifications and training. In addition, we develop and accelerate our leaders' careers through targeted learning that helps them move to higher-level positions or across functions.

We use a research-based, people-centric approach to understanding and improving team member engagement. Periodically, we invite all team members to participate in our internal engagement survey, which covers questions that measure and provide insight into three driving factors: meaningfulness, availability, and psychological safety. In April 2023, 82% of our team members participated in the survey. The results of the survey are shared with all team members and management uses feedback from the survey to identify and implement continuous improvements to our culture and workplace practices.

Compensation and Benefits

Our compensation programs are designed to support our team members' financial and personal wellbeing by providing a valuable return for their contributions to the company. Our total compensation strategy includes base salary, annual bonuses, equity awards, a discounted stock purchase plan, and a comprehensive benefits package.

Diversity, Equality, and Inclusion

We have five diversity, equality, and inclusion ("DEI") commitments that serve as the roadmap of our DEI work internally, within our industry, and in the community at large. To hold ourselves accountable, each commitment is assigned an executive sponsor who is responsible for its strategy and execution. Our five DEI commitments are summarized as follows:

- Increase representation of underrepresented groups
- Drive equitable pay and inclusive benefits
- Champion advocacy and strengthen our culture of inclusion
- Engage with diverse financial institutions for cash management
- Increase diverse supplier representation and spending

We have a regular review of pay globally, including base pay and stock awards, to drive compensation equitably. In 2023, due to challenging industry conditions, base pay increases were suspended, however we achieved global pay equity for all underrepresented employees in compensation across bonuses and stock rewards. In 2022 and 2021, we achieved comprehensive global pay equity for all employees in total compensation across base pay, bonuses, and stock rewards. A pay equity analysis will be conducted in 2024 with our base pay merit review. We also continually assess our global leave, medical, and financial benefits to ensure inclusiveness. In addition, a portion of our company-wide annual bonus program is based on the achievement of DEI-related goals.

Health, Safety, and Wellbeing

Proactive efforts to prevent occupational illnesses and injuries allow us to maintain a safe, healthy, and secure workplace. Each of our sites have health and safety committees, which are designed to promote overall operations and communications regarding safety and to help lead and implement secure and compliant work areas. Our safety program creates a unified corporate safety culture by establishing a formal training structure and common safety practices across our global facilities.

In addition to our proactive efforts on safety, our team member wellness program offers resources across our five pillars of wellbeing (physical, mental, social, career, and financial). We provide services to our team members including free mental health and counseling support, on-site and near-site fitness centers, wellness spaces and health clinics at certain Micron sites, money management and other financial education tools, and encouraging team members to form healthy habits, reduce stress and reinforce mindfulness solutions by participating in wellbeing challenges and measuring their personal progress. We also provide exclusive access to near-site, company-sponsored childcare centers, financial subsidies to help families with cost, and partnerships with community centers.

We are a member of the Responsible Business Alliance (“RBA”), a group of leading companies focused on promoting responsible working conditions, ethical business practices, and environmental stewardship throughout our global supply chain. We strive to adhere to both our Code of Business Conduct and Ethics (available on our website, www.micron.com) and the RBA code of conduct, which is a demonstration of our commitment to integrity and responsible practices.

Additional information about our human capital is included in our 2023 Sustainability Report and our 2022 DEI Annual Report, each available on our website. Information contained or referenced on our website is not incorporated by reference and does not form a part of this Annual Report on Form 10-K.

Government Regulations

Our worldwide business activities are subject to various federal, state, local, and foreign laws and our products are governed by a number of rules and regulations and customer expectations. The efforts and expenditures needed to comply with these laws, rules, and regulations do not presently have a material impact on our results of operations, capital expenditures, or competitive position. Nevertheless, compliance with existing or future government laws, including, but not limited to, our operations, products, global trade, business acquisitions, employee health and safety, and taxes could have a material adverse effect on our future results of operations, capital expenditures, or competitive position. See “Item 1A. Risk Factors” for a discussion of these potential impacts.

Environmental Compliance

Manufacturing of our products is subject to complex and evolving federal, state, local, and foreign environmental, health, safety and product laws and regulations and expectations. We approach environmental compliance and sustainability proactively to ensure we meet applicable government regulations regarding use of raw materials and chemicals, discharges, emissions, climate change and energy use, and waste disposal and management from our manufacturing processes. Our approach also considers the expectations of our investors, customers, team members, community members, and other stakeholders. Compliance with the law and other obligations is a minimum environmental expectation at Micron. Our wafer fabrication facilities continued to conform to the requirements of the ISO 14001:2015 environmental management systems standard to ensure we are continuously improving our performance. As part of the ISO 14001 framework, we have established a global environmental policy and meet requirements, such as environmental aspects evaluation and control, compliance obligations, commitment, training, communication, document control, operational control, emergency preparedness and response, and management review. While we have not experienced any material adverse effects to our operations from environmental regulations, changes in regulations could necessitate additional capital expenditures, modification of our operations or chemical usage, or other compliance actions.

Trade Regulations

Sales of our memory and storage products, and the transfer of related technical information and know-how, including support, are subject to laws and regulations governing international trade, including, but not limited to, export control, customs, and sanctions regulations administered by U.S. government agencies such as the Bureau of Industry and Security ("BIS") of the U.S. Department of Commerce and the Office of Foreign Asset Control of the U.S. Department of the Treasury. Other jurisdictions, such as the European Union or China, also maintain, or may implement, similar laws and regulations with which we must comply. Any such laws or regulations may require that we either obtain licenses or other authorizations to export certain of our products or sell them to certain countries, companies, or individuals, or, in the absence of such licenses or authorizations, not export or sell the applicable products or transfer the related technical information and know-how to the affected countries, companies, or individuals. In addition, increased tariffs imposed by the countries in which our products are sold can increase the cost of our product to our customers. The laws and regulations that govern international trade change frequently, sometimes without advance notice. See "Item 1A. Risk Factors – Risks Related to Laws and Regulations – Government actions and regulations, such as export restrictions, tariffs and trade protection measures, may limit our ability to sell our products to certain customers or markets, or could otherwise restrict our ability to conduct operations" and " – Risks Related to Our Business, Operations, and Industry – We face geopolitical and other risks associated with our international operations that could materially adversely affect our business, results of operations, or financial condition."

We and/or our suppliers and service providers could be affected by tariffs, embargoes, or other trade restrictions, as well as laws and regulations enacted in response to concerns regarding climate change, conflict minerals, responsible sourcing practices, public health crises, or other matters, which could limit the supply of our materials and/or increase the cost. Environmental regulations could limit our ability to procure or use certain chemicals or materials in our operations or products. In addition, disruptions in transportation lines could delay our receipt of materials. Lead times for the supply of materials have been extended in the past. Our ability to procure components to repair equipment essential for our manufacturing processes could also be negatively impacted by various restrictions or disruptions in supply chains, among other items. The disruption of our supply of materials, components, or services, or the extension of our lead times could have a material adverse effect on our business, results of operations, or financial condition. Similarly, if our customers experience disruptions to their supplies, materials, components, or services, or the extension of their lead times, they may reduce, cancel, or alter the timing of their purchases with us, which could have a material adverse effect on our business, results of operations, or financial condition.

Information About Our Executive Officers

Our executive officers are appointed annually by our Board of Directors and our directors are elected annually by our shareholders. All officers serve until their successors are duly chosen or elected and qualified, except in the case of earlier death, resignation, or removal.

The following presents information, as of August 31, 2023, about our executive officers:



Scott R. Allen

Corporate Vice President and Chief Accounting Officer

Mr. Allen, 55, joined us in September 2020 as Corporate Vice President of Accounting. Mr. Allen was named Corporate Vice President and Chief Accounting Officer in October 2020. From August 2016 to September 2020, Mr. Allen held several executive roles at NetApp, Inc. including Senior Vice President, Chief Accounting Officer. Mr. Allen holds a Bachelor of Business Administration in Accounting from Siena College.



April S. Arnzen

Senior Vice President and Chief People Officer

Ms. Arnzen, 52, joined us in December 1996 and has served in various leadership positions since that time. Ms. Arnzen was named Senior Vice President, Human Resources in June 2017 and named Senior Vice President and Chief People Officer in October 2020. Ms. Arnzen holds a BS in Human Resource Management and Marketing from the University of Idaho and is a graduate of the Stanford Graduate School of Business Executive Program.



Manish Bhatia

Executive Vice President, Global Operations

Mr. Bhatia, 51, joined us in October 2017 as our Executive Vice President, Global Operations. From May 2016 to October 2017, Mr. Bhatia served as the Executive Vice President of Silicon Operations at Western Digital Corporation. From March 2010 to May 2016, Mr. Bhatia held several executive roles at SanDisk Corporation including Executive Vice President of Worldwide Operations until it was acquired by Western Digital in May 2016. Mr. Bhatia holds a BS and MS in Mechanical Engineering and an MBA, each from the Massachusetts Institute of Technology.



Michael W. Bokan

Senior Vice President, Worldwide Sales

Mr. Bokan, 62, joined us in 1996 and has served in various leadership positions since that time. Mr. Bokan was named Senior Vice President, Worldwide Sales in October 2018. Mr. Bokan holds a BS in Business Administration from Colorado State University.



Scott J. DeBoer

Executive Vice President, Technology & Products

Dr. DeBoer, 57, joined us in February 1995 and has served in various leadership positions since that time. Dr. DeBoer was named Executive Vice President, Technology Development in June 2017 and named Executive Vice President, Technology & Products in September 2019. Dr. DeBoer holds a PhD in Electrical Engineering and an MS in Physics from Iowa State University. He completed his undergraduate degree at Hastings College.



Sanjay Mehrotra

President, Chief Executive Officer, and Director

Mr. Mehrotra, 65, joined us in May 2017 as our President, Chief Executive Officer, and Director. Mr. Mehrotra co-founded and led SanDisk Corporation as a start-up in 1988 until its eventual sale in May 2016, serving as its President and Chief Executive Officer from January 2011 to May 2016, and as a member of its Board of Directors from July 2010 to May 2016. Mr. Mehrotra served as a member of the Board of Directors for Cavium, Inc. from July 2009 until July 2018 and for Western Digital Corp. from May 2016 to February 2017 and has served since March 2021 as a member of the Board of Directors of CDW Corporation. Mr. Mehrotra holds a BS and an MS in Electrical Engineering and Computer Science from the University of California, Berkeley and is a graduate of the Stanford Graduate School of Business Executive Program.



Mark J. Murphy

Executive Vice President and Chief Financial Officer

Mr. Murphy, 55, joined us in April 2022 as Executive Vice President and Chief Financial Officer. From June 2016 to April 2022, Mr. Murphy served as the Chief Financial Officer of Qorvo, Inc. Prior to Qorvo, Mr. Murphy served as Executive Vice President and Chief Financial Officer of Delphi Automotive PLC, and prior to Delphi, held executive roles at Praxair, Inc. and MEMC Electronic Materials, Inc. Mr. Murphy currently serves on the Board of Directors of Albany International Corp. Mr. Murphy is a veteran of the U.S. Marine Corps and holds an MBA from Harvard University and BS in Business from Marquette University.



Sumit Sadana

Executive Vice President and Chief Business Officer

Mr. Sadana, 54, joined us in June 2017 as our Executive Vice President and Chief Business Officer. From April 2010 to May 2016, Mr. Sadana served in various roles at SanDisk Corporation, including Executive Vice President, Chief Strategy Officer, and General Manager, Enterprise Solutions until it was acquired by Western Digital in May 2016. Mr. Sadana currently serves on the Board of Directors of Silicon Laboratories, Inc. Mr. Sadana holds a B.Tech. in Electrical Engineering from the Indian Institute of Technology, Kharagpur, India and an MS in Electrical Engineering from Stanford University.

There are no family relationships between any of our directors or executive officers.

Available Information

Our executive offices are located at 8000 South Federal Way, Boise, Idaho 83716-9632 and our telephone number is (208) 368-4000. Information about us is available on our website, www.micron.com. Also available on our website are our Corporate Governance Guidelines, Governance and Sustainability Committee Charter, Compensation Committee Charter, Audit Committee Charter, Finance Committee Charter, Security Committee Charter, and Code of Business Conduct and Ethics. We intend to satisfy the disclosure requirement under Item 5.05 of Form 8-K regarding any amendments to, or waivers from, our Code of Business Conduct and Ethics by posting such information on our website within four business days of the amendment or waiver. Copies of these documents are available to shareholders upon request. Information contained or referenced on our website is not incorporated by reference and does not form a part of this Annual Report on Form 10-K.

Investors and others should note that we announce material financial information about our business and products through a variety of means, including our investor relations website (investors.micron.com), filings with the U.S. Securities and Exchange Commission ("SEC"), press releases, public conference calls, blog posts (micron.com/about/blog), and webcasts. We use these channels to achieve broad, non-exclusionary distribution of information to the public and for complying with our disclosure obligations under Regulation FD. Therefore, we encourage investors, the media, and others interested in our company to review the information we post on such channels.

Our filings are available free of charge on our website as soon as reasonably practicable after they are electronically filed with, or furnished to, the SEC, including our annual and quarterly reports on Forms 10-K and 10-Q and current reports on Form 8-K, our proxy statements, and any amendments to those reports or statements. The SEC's website, www.sec.gov, contains reports, proxy and information statements, and other information regarding issuers that file electronically with the SEC. The content on any website referred to in this Form 10-K is not incorporated by reference in this Form 10-K unless expressly noted.

ITEM 1A. RISK FACTORS

In addition to the factors discussed elsewhere in this Form 10-K, this section discusses important factors which could cause actual results or events to differ materially from those contained in any forward-looking statements made by us. The order of presentation is not necessarily indicative of the level of risk that each factor poses to us. Any of these factors could have a material adverse effect on our business, results of operations, financial condition, or stock price. Our operations could also be affected by other factors that are presently unknown to us or not considered significant.

Risk Factor Summary

Risks Related to Our Business, Operations, and Industry

- volatility in average selling prices of our products;
- a range of factors that may adversely affect our gross margins;
- our international operations, including geopolitical risks;
- the highly competitive nature of our industry;
- our ability to develop and produce new and competitive memory and storage technologies and products;
- realizing expected returns from capacity expansions;
- achieving or maintaining certain performance or other obligations associated with incentives from various governments;
- availability and quality of materials, supplies, and capital equipment and dependency on third-party service providers;
- a downturn in regional or worldwide economies;
- disruptions to our manufacturing process from operational issues, natural disasters, or other events;
- dependency on a select number of key customers, including international customers;
- products that fail to meet specifications, are defective, or are incompatible with end uses;
- breaches of our security systems or products, or those of our customers, suppliers, or business partners;
- attracting, retaining, and motivating highly skilled employees;
- responsible sourcing requirements and related regulations;
- environmental, social, and governance considerations;
- acquisitions and/or alliances; and
- restructure plans may not realize expected savings or other benefits.

Risks Related to Intellectual Property and Litigation

- protecting our intellectual property and retaining key employees who are knowledgeable of and develop our intellectual property;
- legal proceedings and claims; and
- claims that our products or manufacturing processes infringe or otherwise violate the intellectual property rights of others or failure to obtain or renew license agreements covering such intellectual property.

Risks Related to Laws and Regulations

- impacts of government actions and compliance with tariffs, trade restrictions, and/or trade regulations;
- tax expense and tax laws in key jurisdictions; and
- compliance with laws, regulations, or industry standards, including environmental considerations.

Risks Related to Capitalization and Financial Markets

- our ability to generate sufficient cash flows or obtain access to external financing;
- our debt obligations;
- changes in foreign currency exchange rates;
- counterparty default risk;
- volatility in the trading price of our common stock; and
- fluctuations in the amount and frequency of our common stock repurchases and payment of cash dividends and resulting impacts.

Risks Related to Our Business, Operations, and Industry

Volatility in average selling prices for our semiconductor memory and storage products may adversely affect our business.

We have experienced significant volatility in our average selling prices and may continue to experience such volatility in the future. For example, average selling prices for DRAM declined in the high-40s percent range and NAND declined in the low-50s percent range for 2023 as compared to 2022. Since 2017, annual percentage changes in DRAM average selling prices have ranged from approximately plus 35% to a minus high-40s percent range. Since 2017, annual percentage changes in NAND average selling prices have ranged from nearly flat to a minus low-50s percent range. In current and recent periods, average selling prices for our products have been below our manufacturing costs and we may experience such circumstances in the future. Average selling prices for our products that decline faster than our costs have recently had an adverse effect on our business and results of operations, and in future periods could have a material adverse effect on our business, results of operations, or financial condition.

Our gross margins may be adversely affected by a range of factors.

Our gross margins are dependent, in part, upon continuing decreases in per gigabit manufacturing costs achieved through improvements in our manufacturing processes and product designs. Factors that may limit our ability to reduce our per gigabit manufacturing costs at sufficient levels to prevent deterioration of or improve gross margins include, but are not limited to:

- strategic product diversification decisions affecting product mix;
- increasing complexity of manufacturing processes;
- difficulties in transitioning to smaller line-width process technologies or additional 3D memory layers or NAND cell levels;
- process complexity including number of mask layers and fabrication steps;
- manufacturing yield;
- technological barriers;
- changes in process technologies;
- new products that may require relatively larger die sizes;
- start-up or other costs associated with capacity expansions;
- higher costs of goods and services due to inflationary pressures or market conditions; and
- higher manufacturing costs per gigabit due to fabrication facility underutilization, lower wafer output, and insufficient volume to run new technology nodes to achieve cost optimization.

Many factors may result in a reduction of our output or a delay in ramping production, which could lead to underutilization of our production assets. These factors may include, among others, a weak demand environment, industry oversupply, inventory surpluses, difficulties in ramping emerging technologies, supply chain disruptions, and delays from equipment suppliers. See “Part II – Item 7. Management’s Discussion and Analysis of Financial Condition and Results of Operations – Overview – Industry Conditions” for information regarding our current underutilization. A significant portion of our manufacturing costs are fixed and do not vary proportionally with changes in production output. As a result, lower utilization, lower wafer output, and corresponding increases in our per gigabit manufacturing costs have resulted in higher inventory carrying costs, and have had, and may continue to have, an adverse effect on our gross margins, business, results of operations, or financial condition.

We have a broad portfolio of products to address our customers' needs, which span multiple market segments and are subject to rapid technological changes. Our manufacturing costs on a per gigabit basis vary across our portfolio as they are largely influenced by the technology node in which the solution was developed. We strive to balance our demand and supply for each technology node, but the dynamics of our markets and our customers can create periods of imbalance, which can lead us to carry elevated inventory levels. Consequently, we may incur charges in connection with obsolete or excess inventories, or we may not fully recover our costs, which would reduce our gross margins. For example, in 2023, we recorded aggregate charges of $1.83 billion to write down the carrying value of our inventories to their estimated net realizable value. In addition, due to the customized nature of certain products we manufacture, we may be unable to sell certain finished goods inventories to alternative customers or manufacture in-process inventory to different specifications, which may result in excess and obsolescence charges in future periods.

In addition, if we are unable to supply products that meet customer design and performance specifications, we may be required to sell such products at lower average selling prices, which may reduce our gross margins. Our gross margins may also be impacted by shifts in product mix, driven by our strategy to optimize our portfolio to best respond to changing market dynamics.

Our inability to prevent deterioration of or improve gross margins could have a material adverse effect on our business, results of operations, or financial condition.

We face geopolitical and other risks associated with our international operations that could materially adversely affect our business, results of operations, or financial condition.

In addition to our U.S. operations, a substantial portion of our operations are conducted in Taiwan, Singapore, Japan, Malaysia, China, and India, and many of our customers, suppliers, and vendors also operate internationally. In 2023, nearly half of our revenue was from sales to customers who have headquarters located outside the United States, while over 80% of our revenue in 2023 was from products shipped to customer locations outside the United States.

Our international operations are subject to a number of risks, including:

- restrictions on sales of goods or services to one or more of our significant foreign customers;
- export and import duties, changes to import and export regulations, customs regulations and processes, and restrictions on the transfer of funds, including currency controls in China, which could negatively affect the amount and timing of payments from certain of our customers and, as a result, our cash flows;
- compliance with U.S. and international laws involving international operations, including the Foreign Corrupt Practices Act of 1977, as amended, sanctions and anti-corruption laws, export and import laws, and similar rules and regulations;
- theft of intellectual property;
- political and economic instability, including instability resulting from domestic and international conflicts;
- government actions or civil unrest preventing the flow of products and materials, including delays in shipping and obtaining products and materials, cancellation of orders, or loss or damage of products;
- problems with the transportation or delivery of products and materials;
- issues arising from cultural or language differences and labor unrest;
- longer payment cycles and greater difficulty in collecting accounts receivable;
- compliance with trade, technical standards, and other laws in a variety of jurisdictions;
- contractual and regulatory limitations on the ability to maintain flexibility with staffing levels;
- disruptions to manufacturing or R&D activities as a result of actions imposed by foreign governments;
- changes in economic policies of foreign governments;
- difficulties in staffing and managing international operations; and
- public health issues.

If we or our customers, suppliers, or vendors are impacted by any of these risks, it could have a material adverse effect on our business, results of operations, or financial condition.

Following the May 21, 2023 decision of its cybersecurity review of our products sold in China, the CAC determined that critical information infrastructure operators in China may not purchase Micron products, impacting our revenue with companies headquartered in mainland China and Hong Kong, including direct sales as well as indirect sales through distributors. Some revenue with customers headquartered outside of China has also been impacted. As we try to mitigate possible impacts due to the CAC decision, revenue may come at lower prices or gross margins due to product or customer mix changes, which may impact our business results. Further actions by the Chinese government could impact additional revenue inside or outside China, or our operations in China, or our ability to ship products to our customers, any of which could have a material adverse effect on our business, results of operations, or financial condition.

Political, economic, or other actions may adversely affect our operations in Taiwan. A majority of our DRAM production output in 2023 was from our fabrication facilities in Taiwan and any loss of output could have a material adverse effect on us. Any political, economic, or other actions may also adversely affect our customers and the technology industry supply chain, for which Taiwan is a central hub, and as a result, could have a material adverse impact on us.

In addition, the U.S. government has in the past restricted American firms from selling products and software to certain of our customers and may in the future impose similar restrictions on one or more of our significant customers. These restrictions may not prohibit our competitors from selling similar products to our customers, which may result in our loss of sales and market share. Even as such restrictions are lifted, financial or other penalties or continuing export restrictions imposed with respect to our customers could have a continuing negative impact on our future revenue and results of operations, and we may not be able to recover any customers or market share we lose, or make such recoveries at acceptable average selling prices, while complying with such restrictions.

The semiconductor memory and storage markets are highly competitive.

We face intense competition in the semiconductor memory and storage markets from a number of companies, including Kioxia Holdings Corporation; Samsung Electronics Co., Ltd.; SK hynix Inc.; and Western Digital Corporation. Our competitors may use aggressive pricing to obtain market share. Some of our competitors are large corporations or conglomerates that may have a larger market share and greater resources to invest in technology, capitalize on growth opportunities, and withstand downturns in the semiconductor markets in which we compete. Consolidation of industry competitors could put us at a competitive disadvantage as our competitors may benefit from increased manufacturing scale and a stronger product portfolio. We operate in different jurisdictions than our competitors and may be impacted by unfavorable changes in currency exchange rates.

In addition, some governments may provide, or have provided and may continue to provide, significant assistance, financial or otherwise, to some of our competitors or to new entrants and may intervene in support of national industries and/or competitors. In particular, we face the threat of increasing competition as a result of significant investment in the semiconductor industry by the Chinese government and various state-owned or affiliated entities, in companies such as Yangtze Memory Technologies Co., Ltd. (“YMTC”) and ChangXin Memory Technologies, Inc. (“CXMT”). In addition, the CAC’s decision that critical information infrastructure operators in China may not purchase Micron products had an impact on our ability to compete effectively in China and elsewhere.

We and our competitors generally seek to increase wafer output, improve yields, and reduce die size, which could result in significant increases in worldwide supply and downward pressure on prices. Increases in worldwide supply of semiconductor memory and storage also result from fabrication capacity expansions, either by way of new facilities, increased capacity utilization, or reallocation of other semiconductor production to semiconductor memory and storage production. Our competitors may increase capital expenditures resulting in future increases in worldwide supply. We, and some of our competitors, have plans to ramp, or are constructing or ramping, production at new fabrication facilities. Increases in worldwide supply of semiconductor memory and storage, if not accompanied by commensurate increases in demand, could lead to declines in average selling prices for our products and could materially adversely affect our business, results of operations, or financial condition. If competitors are more successful at developing or implementing new product or process technology, their products could have cost or performance advantages.

The competitive nature of our industry could have a material adverse effect on our business, results of operations, or financial condition.

Our future success depends on our ability to develop and produce new and competitive memory and storage technologies and products.

Our key semiconductor memory and storage technologies face technological barriers to continue to meet long-term customer needs. These barriers include potential limitations on stacking additional 3D memory layers, increasing bits per cell (i.e., cell levels), meeting higher density requirements, improving power consumption and reliability, and delivering advanced features and higher performance. We may face technological barriers to continue to shrink our products at our current or historical rate, which has generally reduced per gigabit cost. We have invested and expect to continue to invest in R&D for new and existing products and process technologies, such as EUV lithography, to continue to deliver advanced product requirements. Such new technologies can add complexity and risk to our schedule and may affect our costs and production output. We may be unable to recover our investment in R&D or otherwise realize the economic benefits of reducing die size or increasing memory and storage densities. Our competitors are working to develop new memory and storage technologies that may offer performance and/or cost advantages to existing technologies and render existing technologies obsolete. Accordingly, our future success may depend on our ability to develop and produce viable and competitive new memory and storage technologies.

We are developing new products, including system-level memory and storage products and solutions, which complement our traditional products or leverage their underlying design or process technology. We have invested and expect to continue to invest in new semiconductor product and system-level solution development. We are increasingly differentiating our products and solutions to meet the specific demands of our customers, which increases our reliance on our customers' ability to accurately forecast the needs and preferences of their customers. As a result, our product demand forecasts may be impacted significantly by the strategic actions of our customers. In addition, our ability to successfully introduce new products often requires us to make product specification decisions multiple years in advance of when new products enter the market.

It is important that we deliver products in a timely manner with increasingly advanced performance characteristics at the time our customers are designing and evaluating samples for their products. If we do not meet their product design schedules, our customers may exclude us from further consideration as a supplier for those products. The process to develop new products requires us to demonstrate advanced functionality, performance, and reliability, often well in advance of a planned ramp of production, in order to secure design wins with our customers. Many factors may negatively impact our ability to meet anticipated timelines and/or expected or required quality standards with respect to the development of certain of our products. In addition, some of our components have long lead-times, requiring us to place orders up to a year in advance of anticipated demand. Such long lead-times increase the risk of excess inventory or loss of sales in the event our forecasts vary substantially from actual demand.

There can be no assurance of the following:

- we will be successful in developing competitive new semiconductor memory and storage technologies and products;
- we will be able to cost-effectively manufacture new products;
- we will be able to successfully market these technologies;
- margins generated from sales of these products will allow us to recover costs of development efforts;
- we will be able to establish or maintain key relationships with customers, or that we will not be prohibited from working with certain customers, for specific chip set or design requirements;
- we will accurately predict and design products that meet our customers' specifications; or
- we will be able to introduce new products into the market and qualify them with our customers on a timely basis.

Unsuccessful efforts to develop new memory and storage technologies and products could have a material adverse effect on our business, results of operations, or financial condition.

We may not be able to achieve expected returns from capacity expansions.

We have announced our intent to expand our production capacity and/or make capital investments in the United States and in other regions where we operate.

These expansions involve several risks including the following:

- capital expenditure requirements for capacity expansions during periods of relatively low free cash flow generation, resulting from challenging memory and storage industry conditions;
- availability of necessary funding, which may include external sources;
- ability to realize expected grants, investment tax credits, and other government incentives, including through the U.S. CHIPS and Science Act of 2022 ("CHIPS Act") and other national, international, state, and local grants;
- potential changes in laws or provisions of grants, investment tax credits, and other government incentives;
- potential restrictions on expanding in certain geographies;
- availability of equipment and construction materials;
- ability to complete construction as scheduled and within budget;
- availability of the necessary workforce;
- ability to timely ramp production in a cost-effective manner;
- increases to our cost structure until new production is ramped to adequate scale; and
- sufficient customer demand to utilize our increased capacity.

We invest our capital in areas that we believe best align with our business strategy and optimize future returns. Investments in capital expenditures may not generate expected returns or cash flows. Significant judgment is required to determine which capital investments will result in optimal returns, and we could invest in projects that are ultimately less profitable than those projects we do not select. Delays in completion and ramping of new production facilities, or failure to optimize our investment choices, could significantly impact our ability to realize expected returns on our capital expenditures.

Any of the above factors could have a material adverse effect on our business, results of operations, or financial condition.

Our incentives from various governments are conditional upon achieving or maintaining certain performance or other obligations and are subject to reduction, termination, clawback, or could impose certain limitations on our business.

We have received, and may in the future continue to receive, benefits and incentives from national, state, and local governments in various regions of the world designed to encourage us to establish, maintain, or increase investment, workforce, or production in those regions. These incentives may take various forms, including grants, loan subsidies, and tax arrangements, and typically require us to achieve or maintain certain levels of investment, capital spending, employment, technology deployment, or research and development activities to qualify for such incentives or could restrict us from undertaking certain activities. We may be unable to obtain significant future incentives to continue to fund a portion of our capital expenditures and operating costs, without which our cost structure would be adversely impacted. We also cannot guarantee that we will successfully achieve performance or other obligations required to qualify for these incentives or that the granting agencies will provide such funding. These incentive arrangements typically provide the granting agencies with rights to audit our compliance with their terms and obligations. Such audits could result in modifications to, or termination of, the applicable incentive program. The incentives we receive could be subject to reduction, termination, or clawback, and any decrease or clawback of government incentives could have a material adverse effect on our business, results of operations, or financial condition.

Our business, results of operations, or financial condition could be adversely affected by the availability and quality of materials, supplies, and capital equipment, or dependency on third-party service providers.

Our supply chain and operations are dependent on the availability of materials that meet exacting standards and the use of third parties to provide us with components and services. We generally have multiple sources of supply for our materials and services. However, only a limited number of suppliers are capable of delivering certain materials, components, and services that meet our standards and, in some cases, materials, components, or services are provided by a single or sole source, and we may be unable to qualify new suppliers on a timely basis. The availability of materials or components such as chemicals, silicon wafers, gases, photoresist, controllers, substrates, lead frames, printed circuit boards, targets, and reticle glass blanks is impacted by various factors. These factors could include a shortage of raw materials or a disruption in the processing or purification of those raw materials into finished goods. Shortages or increases in lead times have occurred in the past, are currently occurring with respect to some materials and components, and may occur from time to time in the future. Constraints within our supply chain for certain materials and integrated circuit components could limit our bit shipments, which could have a material adverse effect on our business, results of operations, or financial condition.

Our manufacturing processes are also dependent on our relationships with third-party manufacturers of controllers, analog integrated circuits, and other components used in some of our products and with outsourced semiconductor foundries, assembly and test providers, contract manufacturers, logistics carriers, and other service providers, including providers of electricity and other utilities. Although we have certain long-term contracts with some of our suppliers, many of these contracts do not provide for long-term capacity or pricing commitments. To the extent we do not have firm commitments from our third-party suppliers over a specific time period or for any specific capacity, quantity, and/or pricing, our suppliers may allocate capacity to their other customers and capacity and/or materials may not be available when needed or at reasonable prices. Inflationary pressures have increased, and may continue to increase costs for materials, supplies, and services. Regardless of contract structure, large swings in demand may exceed our contracted supply and/or our suppliers' capacity to meet those demand changes resulting in a shortage of parts, materials, or capacity needed to manufacture our products. In addition, if any of our suppliers was to cease operations or become insolvent, this could impact their ability to provide us with necessary supplies, and we may not be able to obtain the needed supply in a timely way or at all from other providers.

Certain materials are primarily available in a limited number of countries, including rare earth elements, minerals, and metals. Trade disputes, geopolitical tensions, economic circumstances, political conditions, or public health issues may limit our ability to obtain such materials. Although these rare earth and other materials are generally available from multiple suppliers, China is the predominant producer of certain of these materials. If China were to restrict or stop exporting these materials, our suppliers' ability to obtain such supply may be constrained and we may be unable to obtain sufficient quantities, or obtain supply in a timely manner, or at a commercially reasonable cost. Constrained supply of rare earth elements, minerals, and metals may restrict our ability to manufacture certain of our products and make it difficult or impossible to compete with other semiconductor memory and storage manufacturers who are able to obtain sufficient quantities of these materials from China.

We and/or our suppliers and service providers could be affected by regional conflicts, civil unrest, labor disruptions, sanctions, tariffs, embargoes, or other trade restrictions, as well as laws and regulations enacted in response to concerns regarding climate change, conflict minerals, responsible sourcing practices, public health crises, or other matters, which could limit the supply of our materials and/or increase the cost. Environmental regulations could limit our ability to procure or use certain chemicals or materials in our operations or products. In addition, disruptions in transportation lines could delay our receipt of materials. Our ability to procure components to repair equipment essential for our manufacturing processes could also be negatively impacted by various restrictions or disruptions in supply chains, among other items. The disruption of our supply of materials, components, or services, or the extension of our lead times could have a material adverse effect on our business, results of operations, or financial condition.

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Our operations are dependent on our ability to procure advanced semiconductor manufacturing equipment that enables the transition to lower cost manufacturing processes. For certain key types of equipment, including photolithography tools, we are sometimes dependent on a single supplier. From time to time, we have experienced difficulties in obtaining some equipment on a timely basis due to suppliers' limited capacity. Our inability to obtain equipment on a timely basis could adversely affect our ability to transition to next generation manufacturing processes and reduce our costs. Delays in obtaining equipment could also impede our ability to ramp production and could increase our overall costs of a ramp. Our inability to obtain advanced semiconductor manufacturing equipment in a timely manner could have a material adverse effect on our business, results of operations, or financial condition.

Our construction projects to expand production and R&D capacity are highly dependent on available sources of labor, materials, equipment, and services. Increasing demand, supply constraints, inflation, and other market conditions could result in increasing shortages and higher costs for these items. Difficulties in obtaining these resources could result in significant delays in completion of our construction projects and cost increases, which could have a material adverse effect on our business, results of operations, or financial condition.

Our inability to source materials, supplies, capital equipment, or third-party services could affect our overall production output and our ability to fulfill customer demand. Significant or prolonged shortages of our products could halt customer manufacturing and damage our relationships with these customers. Any damage to our customer relationships as a result of a shortage of our products could have a material adverse effect on our business, results of operations, or financial condition.

Similarly, if our customers experience disruptions to their supplies, materials, components, or services, or the extension of their lead times, they may reduce, cancel, or alter the timing of their purchases with us, which could have a material adverse effect on our business, results of operations, or financial condition.

Downturns in regional or worldwide economies may harm our business.

Downturns in regional or worldwide economies, due to inflation, geopolitics, major central bank policy actions including interest rate increases, public health crises, or other factors, have harmed our business in the past and current and future downturns could also adversely affect our business. Adverse economic conditions affect demand for devices that incorporate our products, such as personal computers, smartphones, automobiles, and servers. Reduced demand for these or other products could result in significant decreases in our average selling prices and product sales. In addition, to the extent our customers or distributors have elevated inventory levels or are impacted by a deterioration in credit markets, we may experience a decrease in short-term and/or long-term demand resulting in industry oversupply and declines in pricing for our products.

A deterioration of conditions in regional or worldwide credit markets could limit our ability to obtain external financing to fund our operations and capital expenditures. In addition, we may experience losses on our holdings of cash and investments due to failures of financial institutions and other parties. Difficult economic conditions may also result in a higher rate of losses on our accounts receivable due to credit defaults. As a result, downturns in regional or worldwide economies could have a material adverse effect on our business, results of operations, or financial condition.

If our manufacturing process is disrupted by operational issues, natural disasters, or other events, our business, results of operations, or financial condition could be materially adversely affected.

We and our subcontractors manufacture products using highly complex processes that require technologically advanced equipment and continuous modification to improve yields and performance. Difficulties in the manufacturing process or the effects from a shift in product mix can reduce yields or disrupt production and may increase our per gigabit manufacturing costs. We and our subcontractors maintain operations and continuously implement new product and process technology at manufacturing facilities, which are widely dispersed in multiple locations in several countries including the United States, Singapore, Taiwan, Japan, Malaysia, and China. As a result of the necessary interdependence within our network of manufacturing facilities, an operational disruption at one of our or a subcontractor's facilities may have a disproportionate impact on our ability to produce many of our products.

From time to time, there have been disruptions in our manufacturing operations as a result of power outages, improperly functioning equipment, disruptions in supply of raw materials or components, or equipment failures. We have manufacturing and other operations in locations subject to natural occurrences and possible climate changes, such as severe and variable weather and geological events resulting in increased costs, or disruptions to our manufacturing operations or those of our suppliers or customers. In addition, climate change may pose physical risks to our manufacturing facilities or our suppliers' facilities, including increased extreme weather events that could result in supply delays or disruptions. Other events, including political or public health crises, such as an outbreak of contagious diseases, may also affect our production capabilities or that of our suppliers, including as a result of quarantines, closures of production facilities, lack of supplies, or delays caused by restrictions on travel or shipping. Events of the types noted above have occurred from time to time and may occur in the future. As a result, in addition to disruptions to operations, our insurance premiums may increase or we may not be able to fully recover any sustained losses through insurance.

If production is disrupted for any reason, manufacturing yields may be adversely affected, or we may be unable to meet our customers' requirements and they may purchase products from other suppliers. This could result in a significant increase in manufacturing costs, loss of revenue, or damage to customer relationships, any of which could have a material adverse effect on our business, results of operations, or financial condition.

A significant portion of our revenue is concentrated with a select number of customers.

In each of the last three years, approximately one-half of our total revenue was from our top ten customers. A disruption in our relationship with any of these customers could adversely affect our business. We could experience fluctuations in our customer base or the mix of revenue by customer as markets and strategies evolve. Our customers' demand for our products may fluctuate due to factors beyond our control. In addition, any consolidation of our customers could reduce the number of customers to whom our products may be sold. Our inability to meet our customers' requirements or to qualify our products with them could adversely impact our revenue. A meaningful change in the inventory strategy of our customers could impact our industry bit demand growth outlook. The loss of, or restrictions on our ability to sell to, one or more of our major customers, or any significant reduction in orders from, or a shift in product mix by, customers could have a material adverse effect on our business, results of operations, or financial condition.

Increases in sales of system solutions may increase our dependency upon specific customers and our costs to develop, qualify, and manufacture our system solutions.

Our development of system-level memory and storage products is dependent, in part, upon successfully identifying and meeting our customers' specifications for those products. Developing and manufacturing system-level products with specifications unique to a customer increases our reliance upon that customer for purchasing our products at sufficient volumes and prices in a timely manner. Even if our products meet customer specifications, our sales of system-level solutions are dependent upon our customers choosing our products over those of our competitors and purchasing our products at sufficient volumes and prices. Our competitors' products may be less costly, provide better performance, or include additional features when compared to our products. Our long-term ability to sell system-level memory and storage products is reliant upon our customers' ability to create, market, and sell their products containing our system-level solutions at sufficient volumes and prices in a timely manner. If we fail to successfully develop and market system-level products, our business, results of operations, or financial condition may be materially adversely affected.

Manufacturing system-level solutions, such as SSDs, managed NAND, and HBM, typically results in higher per-unit manufacturing costs as compared to other products. Even if we are successful in selling system-level solutions to our customers in sufficient volume, we may be unable to generate sufficient profit if our per-unit manufacturing costs are not offset by higher per-unit selling prices. Manufacturing system-level solutions to customer specifications requires a longer development cycle, as compared to discrete products, to design, test, and qualify, which may increase our costs. Some of our system solutions are increasingly dependent on sophisticated firmware that may require significant customization to meet customer specifications, which increases our costs and time to market. Additionally, we may need to update our controller and hardware design as well as our firmware or develop new firmware as a result of new product introductions or changes in customer specifications and/or industry standards, which increases our costs. System complexities and extended warranties for system-level products could also increase our warranty costs. Our failure to cost-effectively manufacture system-level solutions and/or controller, hardware design, and firmware in a timely manner may result in reduced demand for our system-level products and could have a material adverse effect on our business, results of operations, or financial condition.

Products that fail to meet specifications, are defective, or are otherwise incompatible with end uses could impose significant costs on us.

Products that do not meet specifications or that contain, or are perceived by our customers to contain, defects or that are otherwise incompatible with end uses could impose significant costs on us or otherwise materially adversely affect our business, results of operations, or financial condition. From time to time, we experience problems with nonconforming, defective, or incompatible products after we have shipped such products. In recent periods, we have further diversified and expanded our product offerings, which could potentially increase the chance that one or more of our products could fail to meet specifications in a particular application. Our products and solutions may be deemed fully or partially responsible for functionality in our customers' products and may result in sharing or shifting of product or financial liability from our customers to us for costs incurred by the end user as a result of our customers' products failing to perform as specified. In addition, if our products and solutions perform critical functions in our customers' products or are used in high-risk consumer end products, such as autonomous driver assistance programs, home and enterprise security, smoke and noxious gas detectors, medical monitoring equipment, or wearables for child and elderly safety, our potential liability may increase. We could be adversely affected in several ways, including the following:

- we may be required or agree to compensate customers for costs incurred or damages caused by defective or incompatible products and to replace products;
- we could incur a decrease in revenue or adjustment to pricing commensurate with the reimbursement of such costs or alleged damages; and
- we may encounter adverse publicity, which could cause a decrease in sales of our products or harm our reputation or relationships with existing or potential customers.

Any of the foregoing items could have a material adverse effect on our business, results of operations, or financial condition.

Breaches of our security systems or products, or those of our customers, suppliers, or business partners, could expose us to losses.

We maintain a system of controls over the physical security of our facilities. We also manage and store various proprietary information and sensitive or confidential data relating to our operations. In addition, we process, store, and transmit large amounts of data relating to our customers and employees, including sensitive personal information. Unauthorized persons, employees, former employees, nation states, or other parties may gain access to our facilities or technology infrastructure and systems to steal trade secrets or other proprietary information, compromise confidential information, create system disruptions, or cause shutdowns. This risk is exacerbated as competitors for talent, particularly engineering talent, attempt to hire our employees. Through cyberattacks on technology infrastructure and systems, unauthorized parties may obtain access to computer systems, networks, and data, including cloud-based platforms. The technology infrastructure and systems of our suppliers, vendors, service providers, cloud solution providers, and partners have in the past experienced, and may in the future experience, such attacks, which could impact our operations. Cyberattacks can include ransomware, computer denial-of-service attacks, worms, supply chain attacks, social engineering, open source vulnerabilities, and other malicious software programs or other attacks, including those using techniques that change frequently or may be disguised or difficult to detect, or designed to remain dormant until a triggering event, impersonation of authorized users, and efforts to discover and exploit any design flaws, “bugs,” security vulnerabilities, as well as intentional or unintentional acts by employees or other insiders with access privileges. Additionally, some actors are using artificial intelligence technology to launch more automated, targeted and coordinated attacks. Globally, cyberattacks are increasing in number and the attackers are increasingly organized and well-financed, or supported by state actors, and are developing increasingly sophisticated systems to not only attack, but also to evade detection. In addition, geopolitical tensions or conflicts may create a heightened risk of cyberattacks. Breaches of our physical security, attacks on our technology infrastructure and systems, or breaches or attacks on our customers, suppliers, or business partners who have confidential or sensitive information regarding us and our customers and suppliers, could result in significant losses and damage our reputation with customers and suppliers and may expose us to litigation if the confidential information of our customers, suppliers, or employees is compromised.

Our products are also targets for cyberattacks, including those products utilized in cloud-based environments. While some of our products contain encryption or security algorithms to protect third-party content or user-generated data stored on our products, these products could still be hacked or the encryption schemes could be compromised, breached, or circumvented by motivated and sophisticated attackers. Further, our products contain sophisticated hardware and firmware and applications that may contain security vulnerabilities or defects in design or manufacture, including “bugs” and other problems that could interfere with the intended operation of our products. To the extent our products are hacked, or the encryption schemes are compromised or breached, this could harm our business by requiring us to employ additional resources to fix the errors or defects, exposing us to litigation, claims, and harm to our reputation.

Any of the foregoing security risks could have a material adverse effect on our business, results of operations, or financial condition.

We must attract, retain, and motivate highly skilled employees.

To remain competitive, we must attract, retain, and motivate executives and other highly skilled, diverse employees, as well as effectively manage succession for key employees. Competition for experienced employees in our industry can be intense. Hiring and retaining qualified executives and other employees is critical to our business. If our total compensation programs, employment benefits, and workplace culture are not viewed as competitive and inclusive, our ability to attract, retain, and motivate employees could be compromised.

At times, we experience higher levels of attrition, increasing compensation costs, and more intense competition for talent across our industry. To the extent we experience significant attrition and are unable to timely replace employees, we could experience a loss of critical skills and reduced employee morale, potentially resulting in business disruptions or increased expenses to address any disruptions. Additionally, changes to immigration policies in the countries in which we operate, as well as restrictions on travel due to public health crises or other causes, may limit our ability to hire and/or retain talent in, or transfer talent to, specific locations.

Our inability to attract, retain, and motivate executives and other employees or effectively manage succession of key roles may inhibit our ability to maintain or expand our business operations.

Compliance with responsible sourcing requirements and any related regulations could increase our operating costs, or limit the supply and increase the cost of certain materials, supplies, and services, and if we fail to comply, customers may reduce purchases from us or disqualify us as a supplier.

We and many of our customers have adopted responsible sourcing programs that require us to meet certain environmental, social and governance criteria, and to periodically report on our performance against these requirements, including that we source the materials, supplies, and services we use and incorporate into the products we sell as prescribed by these programs. Many customer programs require us to remove a supplier within a prescribed period if such supplier ceases to comply with prescribed criteria, and our supply chain may at any time contain suppliers at risk of being removed due to non-compliance with responsible sourcing requirements. Some of our customers may elect to disqualify us as a supplier (resulting in a permanent or temporary loss of sales to such customer) or reduce purchases from us if we are unable to verify that our performance or products (including the underlying supply chain) meet the specifications of our customers' responsible sourcing programs on a continuous basis. Meeting responsible sourcing requirements may increase operating requirements and costs or limit the sourcing and availability of some of the materials, supplies, and services we use, particularly when the availability of such materials, supplies, and services is concentrated to a limited number of suppliers. From time to time, we remove suppliers or require our suppliers to remove suppliers from their supply chains based on our responsible sourcing requirements or customer requirements, and we or our suppliers may be unable to replace such removed suppliers in a timely or cost-effective manner. Any inability to replace removed suppliers in a timely or cost effective manner may affect our ability and/or the cost to obtain sufficient quantities of materials, supplies, and services necessary for the manufacture of our products. Our inability to replace suppliers we have removed in a timely or cost-effective manner or comply with customers' responsible sourcing requirements or with any related regulations could have a material adverse effect on our business, results of operations, or financial condition.

Failure to meet environmental, social, and governance expectations or standards or achieve our related goals could adversely affect our business, results of operations, financial condition, or stock price.

In recent years, there has been an increased focus from stakeholders on environmental, social, and governance matters, including greenhouse gas emissions and climate-related risks, sustainability, renewable energy, water stewardship, waste management, diversity, equality and inclusion, responsible sourcing and supply chain, human rights, and social responsibility. Given our commitment to relevant social and environmental issues as it relates to our business, we actively manage these issues and have established and publicly announced certain goals, commitments, and targets which we may refine or even expand further in the future. These goals, commitments, and targets reflect our current plans and aspirations and are not guarantees that we will be able to achieve them. Achieving these goals may entail significant costs, for example we have entered into several virtual power purchase agreements to obtain renewable energy credits at a cost that will vary based on future prices for electrical power. Evolving stakeholder expectations and our efforts to manage these issues, report on them, and accomplish our goals present numerous operational, regulatory, reputational, financial, legal, and other risks, any of which could have a material adverse impact, including on our reputation and stock price.

Such risks and uncertainties include:

- reputational harm, including damage to our relationships with customers, suppliers, investors, governments, or other stakeholders;
- adverse impacts on our ability to manufacture and sell products and maintain our market share;
- the success of our collaborations with third parties;
- increased risk of litigation, investigations, or regulatory enforcement action;
- unfavorable environmental, social, and governance ratings or investor sentiment;
- diversion of resources and increased costs to control, assess, and report on environmental, social, and governance metrics;
- our ability to achieve our goals, commitments, and targets within timeframes announced;
- increased costs to achieve our goals, commitments, and targets;
- unforeseen operational and technological difficulties;
- access to and increased cost of capital; and
- adverse impacts on our stock price.

Any failure, or perceived failure, to meet evolving stakeholder expectations and industry standards or achieve our environmental, social, and governance goals, commitments, and targets could have an adverse effect on our business, results of operations, financial condition, or stock price.

Acquisitions and/or alliances involve numerous risks.

Acquisitions and the formation or operation of alliances, such as joint ventures and other partnering arrangements, involve numerous risks, including the following:

- integrating the operations, technologies, and products of acquired or newly formed entities into our operations;
- increasing capital expenditures to upgrade and maintain facilities;
- increased debt levels;
- the assumption of unknown or underestimated liabilities;
- the use of cash to finance a transaction, which may reduce the availability of cash to fund working capital, capital expenditures, R&D expenditures, and other business activities;
- diverting management's attention from daily operations;
- managing larger or more complex operations and facilities and employees in separate and diverse geographic areas;
- hiring and retaining key employees;
- requirements imposed by government authorities in connection with the regulatory review of a transaction, which may include, among other things, divestitures or restrictions on the conduct of our business or the acquired business;
- underestimating the costs or overestimating the benefits, including product, revenue, cost and other synergies and growth opportunities that we expect to realize, and we may not achieve those benefits;
- failure to maintain customer, vendor, and other relationships;
- inadequacy or ineffectiveness of an acquired company's internal financial controls, disclosure controls and procedures, compliance programs, and/or environmental, health and safety, anti-corruption, human resource, or other policies or practices; and
- impairment of acquired intangible assets, goodwill, or other assets as a result of changing business conditions or technological advancements.

The global memory and storage industry has experienced consolidation and may continue to consolidate. We engage, from time to time, in discussions regarding potential acquisitions and similar opportunities. To the extent we are successful in completing any such transactions, we could be subject to some or all of the risks described above. Acquisitions of, or alliances with, technology companies are inherently risky and may not be successful and could have a material adverse effect on our business, results of operations, or financial condition.

We have incurred restructure charges and may incur restructure charges in future periods and may not realize expected savings or other benefits from restructure plans.

In 2023, we initiated a restructure plan in response to current market conditions. See "Part II – Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Restructure and Asset Impairments" and "Part II – Item 7. Management's Discussion and Analysis of Financial Condition and Results of Operations – Overview." In addition, we may in the future enter into other restructure initiatives in order to, among other items, streamline our operations, respond to changes in business conditions, our markets, or product offerings, or to centralize certain key functions.

We may not realize expected savings or other benefits from our current or future restructure activities and may incur additional restructure charges or other losses in future periods associated with other initiatives. In connection with any restructure initiatives, we could incur restructure charges, loss of production output, loss of key personnel, disruptions in our operations, and difficulties in the timely delivery of products, which could have a material adverse effect on our business, results of operations, or financial condition.

Risks Related to Intellectual Property and Litigation

We may be unable to protect our intellectual property or retain key employees who are knowledgeable of and develop our intellectual property.

We maintain a system of controls over our intellectual property, including U.S. and foreign patents, trademarks, copyrights, trade secrets, licensing arrangements, confidentiality procedures, non-disclosure agreements with employees, consultants, and vendors, and a general system of internal controls. Despite our system of controls over our intellectual property, it may be possible for our current or future competitors to obtain, copy, use, or disclose, illegally or otherwise, our product and process technology or other proprietary information. The laws of some foreign countries may not protect our intellectual property to the same degree as do U.S. laws, and our confidentiality, non-disclosure, and non-compete agreements may be unenforceable or difficult and costly to enforce.

Additionally, our ability to maintain and develop intellectual property is dependent upon our ability to attract, develop, and retain highly skilled employees. If our competitors or future entrants into our industry are successful in hiring our employees, they may directly benefit from the knowledge these employees gained while they were under our employment, and this may also negatively impact our ability to maintain and develop intellectual property.

Our inability to protect our intellectual property or retain key employees who are knowledgeable of and develop our intellectual property could have a material adverse effect on our business, results of operations, or financial condition.

Legal proceedings and claims could have a material adverse effect on our business, results of operations, or financial condition.

From time to time, we are subject to various legal proceedings and claims that arise out of the ordinary conduct of our business or otherwise, both domestically and internationally. Such claims include, but are not limited to, allegations of anticompetitive conduct and infringement of intellectual property. See “Part II – Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Contingencies.”

Any claim, with or without merit, could result in significant legal fees that could negatively impact our financial results, disrupt our operations, and require significant attention from our management. We may be associated with and subject to litigation, claims, or arbitration disputes arising from, or as a result of:

- our relationships with vendors or customers, supply agreements, or contractual obligations with our subcontractors or business partners;
- the actions of our vendors, subcontractors, or business partners;
- our indemnification obligations, including obligations to defend our customers against third-party claims asserting infringement of certain intellectual property rights, which may include patents, trademarks, copyrights, or trade secrets; and
- the terms of our product warranties or from product liability claims.

As we continue to focus on developing system solutions with manufacturers of consumer products, including autonomous driving, augmented reality, and others, we may be exposed to greater potential for personal liability claims against us as a result of consumers’ use of those products. We, our officers, or our directors could also be subject to claims of alleged violations of securities laws. There can be no assurance that we are adequately insured to protect against all claims and potential liabilities, and we may elect to self-insure with respect to certain matters. Exposures to various legal proceedings and claims could lead to significant costs and expenses as we defend claims, are required to pay damage awards, or enter into settlement agreements, any of which could have a material adverse effect on our business, results of operations, or financial condition.

Claims that our products or manufacturing processes infringe or otherwise violate the intellectual property rights of others, or failure to obtain or renew license agreements covering such intellectual property, could materially adversely affect our business, results of operations, or financial condition.

As is typical in the semiconductor and other high technology industries, from time to time others have asserted, and may in the future assert, that our products or manufacturing processes infringe upon, misappropriate, misuse, or otherwise violate their intellectual property rights. We are unable to predict the outcome of these assertions made against us. Any of these types of claims, regardless of the merits, could subject us to significant costs to defend or resolve such claims and may consume a substantial portion of management's time and attention. As a result of these claims, we may be required to:

- pay significant monetary damages, fines, royalties, or penalties;
- enter into license or settlement agreements covering such intellectual property rights;
- make material changes to or redesign our products and/or manufacturing processes; and/or
- cease manufacturing, having made, selling, offering for sale, importing, marketing, or using products and/or manufacturing processes in certain jurisdictions.

We may not be able to take any of the actions described above on commercially reasonable terms and any of the foregoing results could have a material adverse effect on our business, results of operations, or financial condition. See "Part II – Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Contingencies."

We have a number of intellectual property license agreements. Some of these license agreements require us to make one-time or periodic payments. We may need to obtain additional licenses or renew existing license agreements in the future. We are unable to predict whether these license agreements can be obtained or renewed on terms acceptable to us. The failure to obtain or renew licenses as necessary could have a material adverse effect on our business, results of operations, or financial condition.

Risks Related to Laws and Regulations

Government actions and regulations, such as export restrictions, tariffs, and trade protection measures, may limit our ability to sell our products to certain customers or markets, or could otherwise restrict our ability to conduct operations.

International trade disputes, geopolitical tensions, and military conflicts have led, and continue to lead, to new and increasing export restrictions, trade barriers, tariffs, and other trade measures that can increase our manufacturing costs, make our products less competitive, reduce demand for our products, limit our ability to sell to certain customers or markets, limit our ability to procure, or increase our costs for, components or raw materials, impede or slow the movement of our goods across borders, impede our ability to perform R&D activities, or otherwise restrict our ability to conduct operations. Increasing protectionism, economic nationalism, and national security concerns may lead to further changes in trade policy, domestic sourcing initiatives, or other formal and informal measures that could make it more difficult to sell our products in, or restrict our access to, some markets and/or customers. For example, following the May 21, 2023 decision of its cybersecurity review of our products sold in China, the CAC determined that critical information infrastructure operators in China may not purchase Micron products, impacting our revenue with companies headquartered in mainland China and Hong Kong, including direct sales as well as indirect sales through distributors. Some revenue with customers headquartered outside of China has also been impacted. Further actions by the Chinese government could impact additional revenue inside or outside China, or our operations in China, or our ability to ship products to our customers, any of which could have a material adverse effect on our business, results of operations, or financial condition.

We cannot predict what further actions may ultimately be taken with respect to export regulations, tariffs, or other trade regulations between the United States and other countries, what products or companies may be subject to such actions, or what actions may be taken by other countries in retaliation. Further changes in trade policy, tariffs, restrictions on exports or other trade barriers, or restrictions on supplies, equipment, and raw materials including rare earth minerals, may limit our ability to produce products, increase our selling and/or manufacturing costs, decrease margins, reduce the competitiveness of our products, or inhibit our ability to sell products or purchase necessary equipment and supplies. Such changes may also result in reputational harm to us, the development or adoption of technologies that compete with our products, long-term changes in global trade and technology supply chains, or negative impacts on our customers' products which incorporate our solutions. Any of the effects described in this risk factor could have a material adverse effect on our business, results of operations, or financial condition.

The technology industry is subject to intense media, political, and regulatory scrutiny, which can increase our exposure to government investigations, legal actions, and penalties. Although we have policies, controls, and procedures designed to help ensure compliance with applicable laws, there can be no assurance that our employees, contractors, suppliers, or agents will not violate such laws or our policies. Violations of trade laws, restrictions, or regulations can result in fines; criminal sanctions against us or our officers, directors, or employees; prohibitions on the conduct of our business; and damage to our reputation.

Tax-related matters could have a material adverse effect on our business, results of operations, or financial condition.

We are subject to income taxes in the United States and many foreign jurisdictions. Our provision for income taxes and cash tax liabilities in the future could be adversely affected by numerous factors, including changes in the geographic mix of our earnings among jurisdictions, challenges by tax authorities to our tax positions and intercompany transfer pricing arrangements, failure to meet performance obligations with respect to tax incentive agreements, expanding our operations in various countries, fluctuations in foreign currency exchange rates, adverse resolution of audits and examinations of previously filed tax returns, and changes in tax laws and regulations.

Changes to income tax laws and regulations, or the interpretation of such laws, in any of the jurisdictions in which we operate could significantly increase our effective tax rate and ultimately reduce our cash flows from operating activities and otherwise have a material adverse effect on our financial condition. Beginning in 2024, the Inflation Reduction Act of 2022 imposes a 15% book minimum tax on corporations with three-year average annual adjusted financial statement income exceeding $1 billion. The impact of this tax will depend on our facts in each year, anticipated guidance from the U.S. Department of the Treasury, and other developing global tax legislation. Further changes in the tax laws of foreign jurisdictions could arise as a result of the base erosion and profit shifting project undertaken by the Organisation for Economic Co-operation and Development ("OECD"). In December 2022, the European Union ("EU") member states reached an agreement to implement the minimum tax component ("Pillar Two") of the OECD's tax reform initiative. The directive is expected to be enacted into the national law of the EU member states by December 31, 2023. If similar directives under Pillar Two are adopted by taxing authorities in other countries where we do business, such changes could have a material adverse effect on our business, results of operations, or financial condition.

We and others are subject to a variety of complex and evolving laws, regulations, or industry standards, including with respect to environmental, health, safety, and product considerations, which may have a material adverse effect on our business, results of operations, or financial condition.

The manufacture of our products requires the use of facilities, equipment, chemicals, and materials that are subject to a broad array of laws and regulations in numerous jurisdictions in which we operate. Additionally, we are subject to a variety of other laws and regulations relative to the construction, maintenance, and operations of our facilities. Any changes in laws, regulations, or industry standards could cause us to incur additional direct costs, as well as increased indirect costs related to our relationships with our customers and suppliers, and otherwise harm our operations and financial condition. Any failure to comply with laws, regulations, or industry standards could adversely impact our reputation and our financial results. Additionally, we engage various third parties as sales channel partners or to represent us or otherwise act on our behalf who are also subject to a broad array of laws, regulations, and industry standards. Our engagement with these third parties may also expose us to risks associated with their respective compliance with laws and regulations.

New and evolving environmental health, safety, and product considerations, including those related to greenhouse gas emissions and climate change, the purchase, use and disposal of regulated and/or hazardous chemicals, and the potential resulting environmental, health or safety impacts, may result in new laws, regulations, or industry standards that may affect us, our suppliers, and our customers. Such laws, regulations, or industry standards could cause us to incur additional direct costs for compliance, as well as increased indirect costs resulting from our customers, suppliers, or both incurring additional compliance costs that are passed on to us. These costs may adversely impact our results of operations and financial condition.

As a result of the considerations detailed in this risk factor, we could experience the following:

- suspension of production or sales of our products;
- limited supplies of chemicals or materials used to make our products;
- remediation costs;
- increased compliance costs;
- alteration of our manufacturing processes;
- regulatory penalties, fines, civil or criminal sanctions, and other legal liabilities; and
- reputational challenges.

Compliance with, or our failure, or the failure of our third-party sales channel partners or agents, to comply with, laws, regulations, or industry standards could have a material adverse effect on our business, results of operations, or financial condition.

Risks Related to Capitalization and Financial Markets

We may be unable to generate sufficient cash flows or obtain access to external financing necessary to fund our operations, make scheduled debt payments, pay our dividend, and make adequate capital investments.

Our cash flows from operations depend primarily on the volume of semiconductor memory and storage products sold, average selling prices, and manufacturing costs. To develop new product and process technology, support future growth, achieve operating efficiencies, and maintain product quality, we must make significant capital investments in manufacturing technology, capital equipment, facilities, R&D, and product and process technology. We estimate capital expenditures in 2024 for property, plant, and equipment, net of partner contributions, to be slightly above $7 billion.

In the past, we have utilized external sources of financing when needed. As a result of our debt levels, expected debt amortization, prevailing interest rates, and general capital market and other economic conditions, it may be difficult for us to obtain financing on terms acceptable to us or at all. We have experienced volatility in our cash flows and operating results and we expect to continue to experience such volatility in the future, which may negatively affect our credit rating. Our credit rating may also be affected by our liquidity, financial results, economic risk, or other factors, which may increase the cost of borrowings and make it difficult for us to obtain financing on terms acceptable to us or at all. There can be no assurance that we will be able to generate sufficient cash flows, access capital or credit markets, or find other sources of financing to fund our operations, make debt payments, refinance our debt, pay our quarterly dividend, and make adequate capital investments to remain competitive in terms of technology development and cost efficiency. Our inability to do any of the foregoing could have a material adverse effect on our business, results of operations, or financial condition.

Debt obligations could adversely affect our financial condition.

We have incurred in the past, and expect to incur in the future, debt to finance our capital investments, business acquisitions, and to realign our capital structure. As of August 31, 2023, we had debt with a carrying value of $13.33 billion and may incur additional debt, including under our $2.50 billion Revolving Credit Facility. Our debt obligations could adversely impact us as follows:

- require us to use a large portion of our cash flow to pay principal and interest on debt, which will reduce the amount of cash flow available to fund our business activities;
- adversely impact our credit rating, which could increase borrowing costs;
- limit our future ability to raise funds for capital expenditures, strategic acquisitions or business opportunities, R&D, and other general corporate requirements;
- restrict our ability to incur specified indebtedness, create or incur certain liens, and enter into sale-leaseback financing transactions;
- increase our vulnerability to adverse economic and industry conditions;
- increase our exposure to rising interest rates from variable rate indebtedness; and
- result in certain of our debt instruments becoming immediately due and payable or being deemed to be in default if applicable cross default, cross-acceleration and/or similar provisions are triggered.

Our ability to meet our payment obligations under our debt instruments depends on our ability to generate significant cash flows or obtain external financing in the future. This, to some extent, is subject to market, economic, financial, competitive, legislative, and regulatory factors as well as other factors that are beyond our control. There can be no assurance that our business will generate cash flow from operations, or that additional capital will be available to us, in amounts sufficient to enable us to meet our debt payment obligations and to fund other liquidity needs. Additionally, events and circumstances may occur which would cause us to not be able to satisfy applicable draw-down conditions and utilize our Revolving Credit Facility. In light of industry conditions, in 2023, we amended the financial covenants in our Revolving Credit Facility and term loan agreements. See “Part II – Item 7. Management’s Discussion and Analysis of Financial Condition and Results of Operations – Overview – Industry Conditions” and “Part II - Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Debt.” If we are unable to generate sufficient cash flows to service our debt payment obligations or satisfy our debt covenants, we may need to refinance, restructure, or amend the terms of our debt, sell assets, reduce or delay capital investments, or seek to raise additional capital. If we are unable to implement one or more of these alternatives, we may be unable to meet our debt payment obligations, which could have a material adverse effect on our business, results of operations, or financial condition.

Changes in foreign currency exchange rates could materially adversely affect our business, results of operations, or financial condition.

Across our global operations, significant transactions and balances are denominated in currencies other than the U.S. dollar (our reporting currency), primarily the Chinese yuan, euro, Indian rupee, Japanese yen, Malaysian ringgit, New Taiwan dollar, and Singapore dollar. In addition, a significant portion of our manufacturing costs are denominated in foreign currencies. Exchange rates for some of these currencies against the U.S. dollar have been volatile and may be volatile in future periods. If these currencies strengthen against the U.S. dollar, our manufacturing costs could significantly increase. Exchange rates for the U.S. dollar that adversely change against our foreign currency exposures could have a material adverse effect on our business, results of operations, or financial condition.

We are subject to counterparty default risks.

We have numerous arrangements with financial institutions that subject us to counterparty default risks, including cash deposits, investments, and derivative instruments. Additionally, we are subject to counterparty default risk from our customers for amounts receivable from them. As a result, we are subject to the risk that the counterparty will default on its performance obligations. A counterparty may not comply with its contractual commitments which could then lead to its defaulting on its obligations with little or no notice to us, which could limit our ability to mitigate our exposure. Additionally, our ability to mitigate our exposures may be constrained by the terms of our contractual arrangements or because market conditions prevent us from taking effective action. If one of our counterparties becomes insolvent or files for bankruptcy, our ability to recover any losses suffered as a result of that counterparty's default may be limited by the liquidity of the counterparty or the applicable laws governing the bankruptcy proceedings. In the event of such default, we could incur significant losses, which could have a material adverse effect on our business, results of operations, or financial condition.

The trading price of our common stock has been and may continue to be volatile.

Our common stock has experienced substantial price volatility in the past and may continue to do so in the future. Additionally, we, the technology industry, and the stock market as a whole have on occasion experienced extreme stock price and volume fluctuations that have affected stock prices in ways that may have been unrelated to the specific operating performance of individual companies. The trading price of our common stock may fluctuate widely due to various factors, including, but not limited to, actual or anticipated fluctuations in our financial condition and operating results, changes in financial forecasts or estimates by us or financial or other market estimates and ratings by securities and other analysts, changes in our capital structure, including issuance of additional debt or equity to the public, interest rate changes, regulatory changes, news regarding our products or products of our competitors, and broad market and industry fluctuations.

For these reasons, investors should not rely on recent or historical trends to predict future trading prices of our common stock, financial condition, results of operations, or cash flows. Investors in our common stock may not realize any return on their investment in us and may lose some or all of their investment. Volatility in the trading price of our common stock could also result in the filing of securities class action litigation matters, which could result in substantial costs and the diversion of management time and resources.

The amount and frequency of our share repurchases may fluctuate, and we cannot guarantee that we will fully consummate our share repurchase authorization, or that it will enhance long-term shareholder value. Share repurchases could also increase the volatility of the trading price of our stock and will diminish our cash reserves.

The amount, frequency, and execution of our share repurchases pursuant to our share repurchase authorization may fluctuate based on our operating results, cash flows, and priorities for the use of cash for other purposes. Our expenditures for share repurchases were $425 million in 2023, $2.43 billion in 2022, $1.20 billion in 2021. These other purposes include, but are not limited to, operational spending, capital spending, acquisitions, and repayment of debt. Other factors, including changes in tax laws, could also impact our share repurchases. Although our Board of Directors has authorized share repurchases of up to $10 billion of our outstanding common stock, the authorization does not obligate us to repurchase any common stock.

We cannot guarantee that our share repurchase authorization will be fully consummated or that it will enhance long-term shareholder value. The repurchase authorization could affect the trading price of our stock and increase volatility, and any announcement of a pause in, or termination of, this program may result in a decrease in the trading price of our stock. In addition, this program will diminish our cash reserves.

There can be no assurance that we will continue to declare cash dividends in any particular amounts or at all.

Our Board of Directors has adopted a dividend policy pursuant to which we currently pay a cash dividend on our common shares on a quarterly basis. The declaration and payment of any dividend is subject to the approval of our Board of Directors and our dividend may be discontinued or reduced at any time. There can be no assurance that we will declare cash dividends in the future in any particular amounts, or at all.

Future dividends, if any, and their timing and amount, may be affected by, among other factors: our financial condition, results of operations, capital requirements, business conditions, debt service obligations, contractual restrictions, industry practice, legal requirements, regulatory constraints, and other factors that our Board of Directors may deem relevant. A reduction in or elimination of our dividend payments could have a negative effect on the trading price of our stock.

ITEM 1B. UNRESOLVED STAFF COMMENTS

None.

ITEM 2. PROPERTIES

Our corporate headquarters are located in Boise, Idaho. In addition to our principal facilities described below, we own or lease numerous other facilities in locations throughout the world used for design, R&D, and sales and marketing activities. The following is a summary of our principal facilities as of August 31, 2023:



Location	Principal Operations
Taiwan	R&D, wafer fabrication, component assembly and test, module assembly and test
Singapore	R&D, wafer fabrication, component assembly and test, module assembly and test
Japan	R&D, wafer fabrication
United States	R&D, wafer fabrication, reticle manufacturing
Malaysia	Component assembly and test, module assembly and test
China	Component assembly and test, module assembly and test

We believe that our existing facilities are suitable and adequate for our present purposes. We generally utilize all of our manufacturing capacity; however, a portion of our facilities were underutilized for 2023 due to industry conditions. See “Part II – Item 7. Management’s Discussion and Analysis of Financial Condition and Results of Operations – Overview – Industry Conditions” for information regarding our current underutilization.

To support expected memory demand in the second half of the decade, we will need to add new DRAM wafer capacity. Following the enactment of the CHIPS Act in 2022, we announced plans to invest in two leading-edge memory manufacturing fabs in the United States, contingent on CHIPS Act support through grants and investment tax credits. As part of this plan, in September 2022, we broke ground on a leading-edge memory manufacturing fab in Boise, Idaho. Construction of the fab began in October 2023 with DRAM production targeted to start in calendar 2025 and first output in early calendar 2026. In addition, in October 2022, we announced plans to build a second leading-edge DRAM manufacturing fab in Clay, New York. We expect construction to begin in calendar 2024, with production anticipated to ramp in the latter half of the decade. We expect these new fabs to fulfill our requirements for additional wafer capacity starting in the second half of the decade and beyond, in line with industry demand trends. On August 21, 2023 we announced that two of our subsidiaries had each submitted full applications on August 18, 2023 for federal funding in the form of grants under the CHIPS Act for both of these projects.

We are also advancing our global back-end assembly and test network in order to support our product portfolio and extend our ability to deliver on global customer demand in the future. We intend to make investments at our backend facility in Xi'an, China, including a new building to provide space to add more product capability, to allow us over time to serve more of the demand from our customers in China from the Xi'an facility. We also intend to build a new assembly and test facility in Gujarat, India to address demand in the latter half of this decade.
We do not identify or allocate assets by operating segment, other than goodwill. For a breakout of the carrying value of our long-lived assets by geographic area see "Part II – Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Geographic Information."

ITEM 3. LEGAL PROCEEDINGS

For a discussion of legal proceedings, see "Part II – Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Contingencies" and "Item 1A. Risk Factors" of this Annual Report on Form 10-K.

SEC regulations require disclosure of certain proceedings related to environmental matters unless we reasonably believe that the related monetary sanctions, if any, will be less than a specified threshold. We use a threshold of $1 million for this purpose.

ITEM 4. MINE SAFETY DISCLOSURES

Not applicable.

PART II

ITEM 5. MARKET FOR REGISTRANT'S COMMON EQUITY, RELATED STOCKHOLDER MATTERS, AND ISSUER PURCHASES OF EQUITY SECURITIES

Market Information

Our common stock is listed on The Nasdaq Global Select Market under the trading symbol "MU."

Holders of Record

As of September 29, 2023, there were approximately 1,719 shareholders of record of our common stock. A substantially greater number of holders of our common stock are "street name" or beneficial holders, whose shares are held of record by banks, brokers, and other financial institutions.

Dividends

On September 27, 2023, our Board of Directors declared a quarterly dividend of $0.115 per share, payable in cash on October 25, 2023, to shareholders of record as of the close of business on October 10, 2023.

We currently expect quarterly dividends to continue in future periods and aim to grow our dividend payments over time. However, the declaration and payment of any future cash dividends are at the discretion and subject to the approval of our Board of Directors. Our Board of Directors' decisions regarding the amount and payment of dividends will depend on many factors, such as our financial condition, results of operations, capital requirements, business conditions, debt service obligations, contractual restrictions, industry practice, legal requirements, regulatory constraints, and other factors that our Board of Directors may deem relevant. We cannot guarantee that we will continue to pay a dividend in any future period.

Equity Compensation Plan Information

The information required by this item is incorporated by reference from the information to be included in our 2023 Proxy Statement under the section entitled “Equity Compensation Plan Information,” which will be filed with the SEC within 120 days after August 31, 2023.

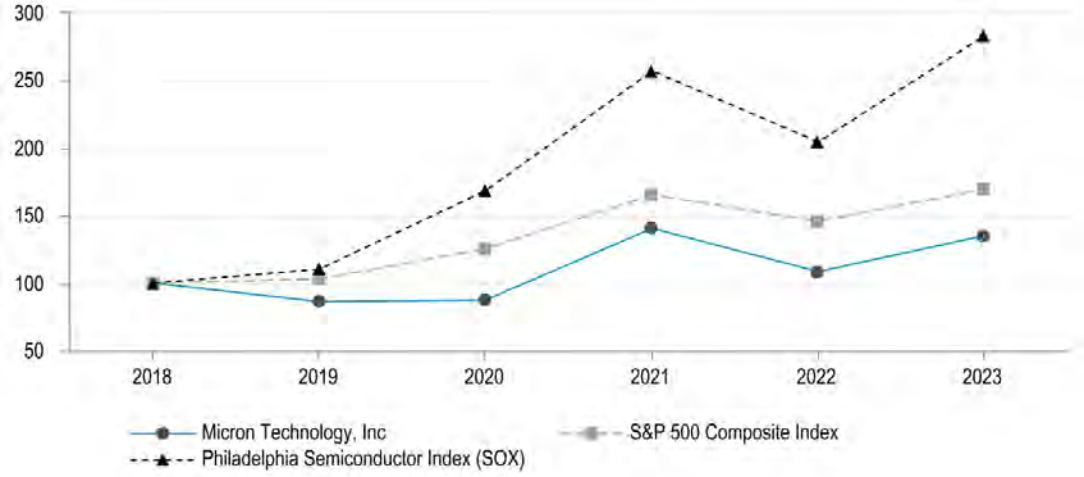
Issuer Purchase of Equity Securities

Common Stock Repurchase Authorization

In 2018, we announced that our Board of Directors authorized the discretionary repurchase of up to $10 billion of our outstanding common stock through open-market purchases, block trades, privately-negotiated transactions, derivative transactions, and/or pursuant to Rule 10b5-1 trading plans. The repurchase authorization has no expiration date, does not obligate us to acquire any common stock, and is subject to market conditions and our ongoing determination of the best use of available cash. During the quarter ended August 31, 2023, we did not repurchase any common stock under the authorization and as of August 31, 2023, $3.11 billion of the authorization remained available for the repurchase of our common stock.
Shares of common stock withheld as payment of withholding taxes and exercise prices in connection with the vesting or exercise of equity awards are also treated as common stock repurchases. Those withheld shares of common stock are not required to be disclosed under Item 703 of Regulation S-K and accordingly are excluded from this Item 5.

Performance Graph

The following graph illustrates a five-year comparison of cumulative total returns for our common stock, the S&P 500 Composite Index, and the Philadelphia Semiconductor Index (SOX) from August 31, 2018, through August 31, 2023. We operate on a 52 or 53-week fiscal year which ends on the Thursday closest to August 31. Accordingly, the last day of our fiscal year varies. For consistent presentation and comparison to the industry indices shown herein, we have calculated our stock performance graph assuming an August 31 year end.



Note: Management cautions that the stock price performance information shown in the graph above may not be indicative of current stock price levels or future stock price performance.

The performance graph above assumes $100 was invested on August 31, 2018 in common stock of Micron Technology, Inc., the S&P 500 Composite Index, and the Philadelphia Semiconductor Index (SOX). Any dividends paid during the period presented were assumed to be reinvested. The performance was plotted using the following data:

	2018	2019	2020	2021	2022	2023
Micron Technology, Inc.	$ 100	$ 86	$ 87	$ 140	$ 108	$ 135
S&P 500 Composite Index	100	103	125	165	146	169
Philadelphia Semiconductor Index (SOX)	100	110	168	257	204	283

ITEM 6. [RESERVED]

ITEM 7. MANAGEMENT'S DISCUSSION AND ANALYSIS OF FINANCIAL CONDITION AND RESULTS OF OPERATIONS

This discussion should be read in conjunction with the consolidated financial statements and accompanying notes for the year ended August 31, 2023. All period references are to our fiscal periods unless otherwise indicated. Our fiscal year is the 52 or 53-week period ending on the Thursday closest to August 31. Fiscal 2023, 2022, and 2021 each contained 52 weeks. All tabular dollar amounts are in millions, except per share amounts.

Overview

For an overview of our business, see "Part I – Item 1. Business – Overview."

Industry Conditions

The memory and storage industry environment deteriorated sharply in the fourth quarter of 2022 and throughout 2023 due to weak demand in many end markets combined with global and macroeconomic challenges and lower demand resulting from customer actions to reduce inventory levels. This led to significant reductions in average selling prices for both DRAM and NAND and bit shipments for DRAM, resulting in declines in revenue across all our business segments and nearly all our end markets. Due to the challenging pricing environment, we recognized charges of $1.83 billion in 2023 to write down inventories to their estimated net realizable value. Ongoing demand growth, customer inventory normalization, and industry-wide supply discipline have set the stage for increased revenue, and improved pricing and profitability throughout fiscal 2024. As a result, pricing trends have started to improve and there were no write downs of inventories to net realizable value in the fourth quarter of 2023. However, further write-downs of inventories in future quarters could occur if pricing expectations deteriorate. Given the challenging pricing environment, elevated levels of inventories for suppliers and customers, and significant supply-demand mismatch, we expect industry profitability will remain challenged into 2024.

As a result of these conditions and increases in our inventory levels, we have reduced capital expenditures and also significantly reduced wafer starts in 2023 for both DRAM and NAND. We expect wafer starts will remain significantly below peak capacity levels for the foreseeable future as we remain focused on managing down our inventories and controlling our supply. We recognized period costs from fabrication facility underutilization of $382 million in 2023 due to wafer start reductions. We estimate that we will recognize approximately $200 million of period costs from underutilization due to wafer start reductions in the first quarter of 2024. We have also taken significant steps to reduce our costs and operating expenses. These actions include the 2023 Restructure Plan discussed below and additional reductions in external spending, including implementing productivity programs across the business, suspension of our 2023 bonus company-wide, reductions in select product programs, lower discretionary spending, and cuts to 2023 executive salaries across the company.

Impact of China Cyberspace Administration Decision

On March 31, 2023, China's Cyberspace Administration (the "CAC") notified us that it was conducting a cybersecurity review of our products sold in China. On May 21, 2023, we received notice that the CAC had concluded its review and decided that our products presented a cybersecurity risk. As such, the CAC determined that critical information infrastructure operators in China may not purchase Micron products. There is no list of the companies that have been designated as critical information infrastructure operators published by the Chinese government or otherwise available to us. Therefore, the full impact of the CAC decision on our business remains uncertain.

The CAC decision has impacted our business, particularly in the domestic data center and networking markets in China. In addition, although demand for DRAM and NAND is improving as customer inventory levels continue to normalize and secular growth drivers remain intact, the CAC decision continues to impact our revenue opportunity in China. This significant headwind is impacting our outlook and slowing our recovery. We are working to mitigate this impact over time and expect quarter-to-quarter revenue variability. Our revenue with companies headquartered in mainland China and Hong Kong, including direct sales as well as indirect sales through distributors, is approximately a quarter of our worldwide revenue and remains our principal exposure to the CAC decision. Although the impact of the CAC decision remains uncertain, we believe that approximately half of that China-headquartered customer revenue, which equates to a low-double-digit percentage of our worldwide revenue, is at risk of being impacted. Despite the near-term impact to our demand as a result of the CAC decision, our long-term goal is to retain our worldwide DRAM and NAND market share.

2023 Restructure Plan

We initiated a restructure plan in response to challenging industry conditions (the “2023 Restructure Plan”). Under the plan, we expect our headcount reduction to approach 15% by the end of calendar 2023, through a combination of voluntary attrition and personnel reductions. In connection with the plan, we incurred restructure charges of $171 million in 2023 primarily related to employee severance costs. The 2023 Restructure Plan was substantially completed in 2023. As a result of the 2023 Restructure Plan, we expect to realize cost savings of approximately $130 million per quarter (approximately 60% in cost of goods sold, 30% in R&D, and 10% in SG&A) subsequent to 2023. Further information on restructure activities can be found in “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Restructure and Asset Impairments.”

Lehi, Utah Fab and 3D XPoint

In 2021, we updated our portfolio strategy to further strengthen our focus on memory and storage innovations for the data center market. In connection therewith, we determined that there was insufficient market validation to justify the ongoing investments required to commercialize 3D XPoint at scale. Accordingly, we ceased development of 3D XPoint technology and engaged in discussions for the sale of our facility located in Lehi, Utah that was dedicated to 3D XPoint production. As a result, we classified the property, plant, and equipment as held for sale in 2021, ceased depreciating the assets, and recognized a $435 million restructure and asset impairment charge and a $104 million tax benefit.

We closed the sale of our Lehi facility to TI in 2022 for $893 million and disposed of $918 million of net assets, consisting primarily of property, plant, and equipment, resulting in a $23 million loss, net of selling expenses and other adjustments.

Results of Operations

Consolidated Results

For the year ended	2023		2022		2021	
Revenue	$ 15,540	100 %	$ 30,758	100 %	$ 27,705	100 %
Cost of goods sold	16,956	109 %	16,860	55 %	17,282	62 %
Gross margin	(1,416)	(9)%	13,898	45 %	10,423	38 %
Research and development	3,114	20 %	3,116	10 %	2,663	10 %
Selling, general, and administrative	920	6 %	1,066	3 %	894	3 %
Restructure and asset impairments	171	1 %	48	— %	488	2 %
Other operating (income) expense, net	124	1 %	(34)	— %	95	— %
Operating income (loss)	(5,745)	(37)%	9,702	32 %	6,283	23 %
Interest income (expense), net	80	1 %	(93)	— %	(146)	(1)%
Other non-operating income (expense), net	7	— %	(38)	— %	81	— %
Income tax (provision) benefit	(177)	(1)%	(888)	(3)%	(394)	(1)%
Equity in net income (loss) of equity method investees	2	— %	4	— %	37	— %
Net income (loss)	$ (5,833)	(38)%	$ 8,687	28 %	$ 5,861	21 %

Total Revenue: Total revenue for 2023 was adversely impacted by the factors described in the section titled “Industry Conditions” above. Total revenue for 2023 decreased 49% as compared to 2022 primarily due to decreases in sales of both DRAM and NAND products.

- Sales of DRAM products decreased 51% primarily due to a high-40s percent range decline in average selling prices and decreases in bit shipments in the high-single-digit percent range.
- Sales of NAND products decreased 46% primarily due to a low-50s percent range decline in average selling prices partially offset by increases in bit shipments in the high-single-digit percent range.

Total revenue for 2022 increased 11% as compared to 2021 primarily due to increases in sales of both DRAM and NAND products.

- Sales of DRAM products increased 12% primarily due to increases in bit shipments of slightly over 10%.
- Sales of NAND products increased 11% primarily due to a high-single-digit percent increase in bit shipments and a low-single-digit percent increase in average selling prices.

***Consolidated Gross Margin*:** Our consolidated gross margin has been adversely impacted by the factors described in the section titled “Industry Conditions” above. Our consolidated gross margin percentage decreased to negative 9% for 2023 from 45% for 2022 primarily due to declines in average selling prices for both DRAM and NAND and charges to write down inventories (as detailed in “Inventory NRV write-downs” below), and $382 million of facility underutilization costs in 2023.

Inventory NRV write-downs: Our consolidated gross margin was impacted by charges to write down inventories to their estimated net realizable value as a result of declines in average selling prices for both DRAM and NAND. As charges to write down inventories are recorded in advance of when inventories are sold, costs of goods sold in subsequent periods are lower than they otherwise would be. The impact of inventory NRV write-downs for each period reflects (1) inventory write-downs in that period, offset by (2) lower costs in that period on the sale of inventory written down in prior periods. The impacts of inventory NRV write-downs are summarized below:

For the year ended	2023	2022	2021
Provision to write down inventory to NRV	$ (1,831)	$ —	$ —
Lower costs from sale of inventory written down in prior periods	844	—	—
	$ (987)	$ —	$ —

Our consolidated gross margin percentage increased to 45% for 2022 from 38% for 2021, as a result of improvements in margins for both DRAM and NAND products, primarily due to reductions in manufacturing costs. Manufacturing cost reductions were driven by strong execution in ramping our 1α DRAM and 176-layer NAND technology nodes. For 2021, our gross margins included the impact of underutilization costs at MTU of $335 million. See “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Lehi, Utah Fab and 3D XPoint.” Also, effective as of the beginning of the second quarter of 2021, we changed our method of inventory costing from average cost to first-in, first-out (“FIFO”). Concurrently, as of the beginning of the second quarter of 2021, we modified our inventory cost absorption processes used to estimate inventory values, which affects the timing of when costs are recognized. These changes resulted in a one-time increase to cost of goods sold of approximately $293 million in 2021.

Revenue by Business Unit

For the year ended	2023		2022		2021	
CNBU	$ 5,710	37 %	$ 13,693	45 %	$ 12,280	44 %
MBU	3,630	23 %	7,260	24 %	7,203	26 %
EBU	3,637	23 %	5,235	17 %	4,209	15 %
SBU	2,553	16 %	4,553	15 %	3,973	14 %
All Other	10	— %	17	— %	40	— %
	$ 15,540		$ 30,758		$ 27,705	

Percentages of total revenue may not total 100% due to rounding.

Changes in revenue for each business unit for 2023 as compared to 2022 were as follows:

- CNBU revenue decreased 58% primarily due to declines in average selling prices for DRAM and decreases in bit shipments.
- MBU revenue decreased 50% primarily due to declines in average selling prices for both DRAM and NAND and decreases in NAND bit shipments.
- EBU revenue decreased 31% primarily due to declines in average selling prices for both DRAM and NAND and decreases in bit shipments.
- SBU revenue decreased 44% primarily due to declines in average selling prices for NAND partially offset by increases in bit shipments.

Changes in revenue for each business unit for 2022 as compared to 2021 were as follows:

- CNBU revenue increased 12% primarily due to increases in bit shipments to cloud, enterprise, and networking markets.
- MBU revenue was relatively unchanged as both DRAM and NAND revenue was relatively flat.
- EBU revenue increased 24% primarily due to strong demand growth in industrial and automotive markets.
- SBU revenue increased 15% primarily due to higher average selling prices and increases in shipments of SSD products.

Operating Income (Loss) by Business Unit

For the year ended	2023		2022		2021	
CNBU	$ (585)	(10)%	$ 5,844	43 %	$ 4,295	35 %
MBU	(1,750)	(48)%	2,160	30 %	2,173	30 %
EBU	382	11 %	1,752	33 %	1,006	24 %
SBU	(1,887)	(74)%	513	11 %	173	4 %
All Other	8	80 %	12	71 %	20	50 %
	$ (3,832)		$ 10,281		$ 7,667	

Percentages reflect operating income (loss) as a percentage of revenue for each business unit.

Changes in operating income or loss for each business unit for 2023 as compared to 2022 were as follows:

- CNBU operating income (loss) deteriorated primarily due to declines in average selling prices and lower bit shipments.
- MBU operating income (loss) deteriorated primarily due to declines in average selling prices and lower NAND bit shipments.
- EBU operating income decreased primarily due to declines in average selling prices and lower bit shipments.
- SBU operating income (loss) deteriorated primarily due to declines in average selling prices.

Changes in operating income or loss for each business unit for 2022 as compared to 2021 were as follows:

- CNBU operating income increased primarily due to higher bit shipments and manufacturing cost reductions.
- MBU operating income was relatively unchanged as slight increases in gross margins were offset by higher operating expenses.
- EBU operating income increased primarily due to manufacturing cost reductions from an increasing mix of leading-edge bits, higher bit shipments, and improved DRAM pricing in industrial and consumer markets, partially offset by higher R&D expenses.
- SBU operating income increased primarily due to improved product mix driving increases in average selling prices, increases in SSD shipments, and manufacturing cost reductions, partially offset by higher R&D expenses.

Operating Expenses and Other

Research and Development: R&D expenses vary primarily with the number of development and pre-qualification wafers processed, the cost of advanced equipment dedicated to new product and process development, and personnel costs. Because of the lead times necessary to manufacture our products, we typically begin to process wafers before completion of performance and reliability testing. Development of a product is deemed complete when it is qualified through internal reviews and tests for performance and reliability. R&D expenses can vary significantly depending on the timing of product qualification.

R&D expenses for 2023 were relatively unchanged as compared to 2022 as decreases in employee compensation were offset by higher depreciation expense. R&D expenses for 2022 increased 17% as compared to 2021 primarily due to higher employee compensation from increases in headcount, higher volumes of development and prequalification wafers, and higher depreciation expense.

Selling, General, and Administrative: SG&A expenses for 2023 were 14% lower as compared to 2022 primarily due to decreases in employee compensation, legal fees, advertising, and professional services. SG&A expenses for 2022 were 19% higher as compared to 2021 primarily due to increases in employee compensation, professional services, and legal fees.

Restructure and Asset Impairments: For a discussion of restructure and asset impairments, see the Overview sections above titled “2023 Restructure Plan” and “Lehi, Utah Fab and 3D XPoint.”

***Interest Income (Expense), Net*:** Interest income (expense) improved for 2023 as compared to 2022 primarily as a result of increases in interest income due to higher interest rates on our cash and investments, partially offset by increases in interest expense due to higher debt balances and interest rates. Interest income (expense) improved for 2022 as compared to 2021 primarily due to an increase of $59 million in interest income as a result of increases in interest rates on our cash and investments.

Income Taxes: Our income tax (provision) benefit consisted of the following:

For the year ended	2023	2022	2021
Income (loss) before taxes	$ (5,658)	$ 9,571	$ 6,218
Income tax (provision) benefit	(177)	(888)	(394)
Effective tax rate	(3.1)%	9.3 %	6.3 %

The change in our effective tax rate for 2023 as compared to 2022 was primarily due to a pre-tax loss in 2023. Despite a consolidated pre-tax loss on a worldwide basis, we have taxes payable in certain geographies due to minimum taxable income reportable in those geographies. Our effective tax rate increased in 2022 as compared to 2021 primarily due to the geographic mix of our earnings and a valuation allowance recorded against our Idaho deferred tax assets of $189 million, partially offset by tax impacts of changes in foreign currency exchange rates.

We operate in a number of jurisdictions outside the United States, including Singapore, where we have tax incentive arrangements. These incentives expire, in whole or in part, at various dates through 2034 and are conditional, in part, upon meeting certain business operations and employment thresholds. As a result of a loss before taxes and geographical mix of income, the benefit from tax incentive arrangements was not material for 2023. The effect of tax incentive arrangements reduced our tax provision by $1.12 billion (benefiting our diluted earnings per share by $1.00) for 2022 and by $758 million ($0.66 per diluted share) for 2021.

Beginning in 2024, the Inflation Reduction Act of 2022 imposes a 15% book minimum tax on corporations with three-year average annual adjusted financial statement income exceeding $1 billion. The impact of this tax will depend on our facts in each year, anticipated guidance from the U.S. Department of the Treasury, and other developing global tax legislation.

Various tax reforms are being considered in multiple jurisdictions that, if enacted, contain provisions that could materially impact our tax expense. We continue to monitor the potential impact of these various tax reform proposals to our overall global effective tax rate and financial statements.

Other: Further information can be found in the following notes contained in “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements”:

- Lehi, Utah Fab and 3D XPoint
- Goodwill
- Equity Plans
- Restructure and Asset Impairments
- Other Operating (Income) Expense, Net
- Other Non-Operating Income (Expense), Net
- Income Taxes

Liquidity and Capital Resources

Our primary sources of liquidity are cash generated from operations and financing obtained from capital markets and financial institutions. Cash generated from operations is highly dependent on selling prices for our products, which can vary significantly from period to period. Cash and marketable investments totaled $10.44 billion as of August 31, 2023, and $10.98 billion as of September 1, 2022. Our cash and investments consist primarily of bank deposits, money market funds, and liquid investment-grade, fixed-income securities, which are diversified among industries and individual issuers. To mitigate credit risk, we invest through high-credit-quality financial institutions and by policy generally limit the concentration of credit exposure by restricting the amount of investments with any single obligor. As of August 31, 2023, $2.45 billion of our cash and marketable investments was held by our foreign subsidiaries.

We continuously evaluate alternatives for efficiently funding our capital expenditures and ongoing operations. We expect, from time to time, to engage in a variety of financing transactions for such purposes, including the issuance of securities. As of August 31, 2023, $2.50 billion was available to draw under our Revolving Credit Facility. On March 27, 2023, we entered into amendments to the Multi-Tranche Term Loan Agreement and the agreements governing the Revolving Credit Facility and the 2024 Term Loan A to revise the leverage ratio covenant in each such agreement, as further described in “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Debt.” Funding of certain significant capital projects is also dependent on the receipt of government incentives, which are subject to conditions and may not be obtained.

To develop new product and process technology, support future growth, achieve operating efficiencies, and maintain product quality, we must continue to invest in manufacturing technologies, facilities and equipment, and R&D. We estimate capital expenditures in 2024 for property, plant, and equipment, net of partner contributions, to be slightly above $7 billion. Actual amounts for 2024 will vary depending on market conditions. As of August 31, 2023, we had purchase obligations of approximately $915 million for the acquisition of property, plant, and equipment, of which approximately $812 million is expected to be paid within one year. For a description of other contractual obligations, such as leases, debt, and commitments, see “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Leases,” “ – Debt,” and “ – Commitments.”

To support expected memory demand in the second half of the decade, we will need to add new DRAM wafer capacity. Following the enactment of the CHIPS Act in 2022, we announced plans to invest in two leading-edge memory manufacturing fabs in the United States, contingent on CHIPS Act support through grants and investment tax credits. As part of this plan, in September 2022, we broke ground on a leading-edge memory manufacturing fab in Boise, Idaho. Construction of the fab began in October 2023 with DRAM production targeted to start in calendar 2025 and first output in early calendar 2026. In addition, in October 2022, we announced plans to build a second leading-edge DRAM manufacturing fab in Clay, New York. We expect construction to begin in calendar 2024, with production anticipated to ramp in the latter half of the decade. We expect these new fabs to fulfill our requirements for additional wafer capacity starting in the second half of the decade and beyond, in line with industry demand trends. On August 21, 2023 we announced that two of our subsidiaries had each submitted full applications on August 18, 2023 for federal funding in the form of grants under the CHIPS Act for both of these projects.

We are also advancing our global back-end assembly and test network in order to support our product portfolio and extend our ability to deliver on global customer demand in the future. We intend to make investments at our backend facility in Xi’an, China, including a new building to provide space to add more product capability, to allow us over time to serve more of the demand from our customers in China from the Xi’an facility. We also intend to build a new assembly and test facility in Gujarat, India to address demand in the latter half of this decade.

Our Board of Directors has authorized the discretionary repurchase of up to $10 billion of our outstanding common stock through open-market purchases, block trades, privately-negotiated transactions, derivative transactions, and/or pursuant to Rule 10b5-1 trading plans. The repurchase authorization has no expiration date, does not obligate us to acquire any common stock, and is subject to market conditions and our ongoing determination of the best use of available cash. Through August 31, 2023, we had repurchased an aggregate of $6.89 billion of the authorized amount. See “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Equity.”

On September 27, 2023, our Board of Directors declared a quarterly dividend of $0.115 per share, payable in cash on October 25, 2023, to shareholders of record as of the close of business on October 10, 2023. The declaration and payment of any future cash dividends are at the discretion and subject to the approval of our Board of Directors. Our Board of Directors' decisions regarding the amount and payment of dividends will depend on many factors, including, but not limited to, our financial condition, results of operations, capital requirements, business conditions, debt service obligations, contractual restrictions, industry practice, legal requirements, regulatory constraints, and other factors that our Board of Directors may deem relevant.

We expect that our cash and investments, cash flows from operations, and available financing will be sufficient to meet our requirements at least through the next 12 months and thereafter for the foreseeable future.

Cash Flows

For the year ended	2023	2022	2021
Net cash provided by operating activities	$ 1,559	$ 15,181	$ 12,468
Net cash provided by (used for) investing activities	(6,191)	(11,585)	(10,589)
Net cash provided by (used for) financing activities	4,983	(2,980)	(1,781)
Effect of changes in currency exchange rates on cash, cash equivalents, and restricted cash	(34)	(106)	41
Net increase (decrease) in cash, cash equivalents, and restricted cash	$ 317	$ 510	$ 139

Operating Activities: Cash provided by operating activities reflects net income (loss) adjusted for certain non-cash items, including depreciation expense, amortization of intangible assets, inventory write-downs, asset impairments, and stock-based compensation, and the effects of changes in operating assets and liabilities. The decrease in cash provided by operating activities for 2023 as compared to 2022 was primarily due to a net loss in the current year adjusted for non-cash items and the effect of an increase in inventories and a decline in accounts payable and accrued expenses, partially offset by a decrease in receivables.

The increase in cash provided by operating activities for 2022 as compared to 2021 was primarily due to higher net income adjusted for non-cash items and the effect of lower receivables, partially offset by an increase in inventories.

Investing Activities: For 2023, net cash used for investing activities consisted primarily of $7.68 billion of expenditures for property, plant, and equipment; contributions of $710 million received from partners to offset capital expenditures; and $868 million of net inflows from maturities, sales, and purchases of available-for-sale securities.

For 2022, net cash used for investing activities consisted primarily of $12.07 billion of expenditures for property, plant, and equipment; contributions of $115 million received from partners to offset capital expenditures; $888 million of net inflows from the sale of the Lehi, Utah fab; and $155 million of net outflows from purchases, sales, and maturities of available-for-sale securities.

For 2021, net cash used for investing activities consisted primarily of $10.03 billion of expenditures for property, plant, and equipment, partially offset by contributions of $502 million received from partners to offset capital expenditures, and $1.06 billion of net outflows from purchases, sales, and maturities of available-for-sale securities.

Financing Activities: For 2023, net cash provided by financing activities consisted primarily of $3.20 billion of proceeds from our 2025, 2026, and 2027 Term Loan A borrowings, $1.27 billion from the issuance of the 2029 B Notes, $896 million from the issuance of the 2033 B Notes, $749 million from the issuance of the 2033 A Notes, and $599 million from the issuance of the 2028 Notes. Cash used for financing activities included $761 million for repayments of debt, $504 million for payments of dividends to shareholders, $425 million for the acquisition of 8.6 million shares of our common stock under our share repurchase authorization, and $138 million of payments on equipment purchase contracts.

For 2022, net cash used for financing activities included $2.43 billion for the acquisition of 35.4 million shares of our common stock under our share repurchase authorization, $2.03 billion of repayments of debt primarily to redeem the 2023 Notes and 2024 Notes, $461 million of cash payments of dividends to shareholders, and $141 million of payments on equipment purchase contracts. Cash used for financing activities was partially offset by aggregate proceeds of $2.00 billion from the issuance of the unsecured 2032 Green Bonds, 2041 Notes, and 2051 Notes.

For 2021, net cash used for financing activities consisted primarily of $1.20 billion for the acquisition of 15.6 million shares of our common stock under our share repurchase authorization, $295 million of payments on equipment purchase contracts, $185 million of cash payments to settle conversions of our 2032D Notes, and $147 million of repayments of finance leases and other debt. In addition, we received proceeds of $1.19 billion under an unsecured 2024 Term Loan A and used the proceeds to repay the $1.19 billion Extinguished 2024 Term Loan A.

See “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Debt.”

Critical Accounting Estimates

The preparation of financial statements and related disclosures in conformity with U.S. GAAP requires management to make estimates and judgments that affect the reported amounts of assets, liabilities, revenues, expenses, and related disclosures. Estimates and judgments are based on historical experience, forecasted events, and various other assumptions that we believe to be reasonable under the circumstances. Estimates and judgments may vary under different assumptions or conditions and involve a significant level of uncertainty. We evaluate our estimates and judgments on an ongoing basis. Our management believes the accounting policies below are critical in the portrayal of our financial condition and results of operations and require management’s most difficult, subjective, or complex judgments.

***Contingencies*:** We are subject to the possibility of losses from various contingencies. Significant judgment is necessary to estimate the probability and amount of a loss, if any, from such contingencies. An accrual is made when it is probable that a liability has been incurred or an asset has been impaired, and the amount of loss can be reasonably estimated. In accounting for the resolution of contingencies, significant judgment may be necessary to estimate amounts pertaining to periods prior to the resolution that are charged to operations in the period of resolution and amounts related to future periods.

***Goodwill*:** We test goodwill for impairment in our fourth quarter each year, or more frequently if indicators of an impairment exist, to determine whether it is more likely than not that the fair value of the reporting unit with goodwill is less than its carrying value. For reporting units for which this assessment concludes that it is more likely than not that the fair value is more than its carrying value, goodwill is considered not impaired, and we are not required to perform the goodwill impairment test. Qualitative factors considered in this assessment include industry and market considerations, overall financial performance, and other relevant events and factors affecting the fair value of the reporting unit. For reporting units for which this assessment concludes that it is more likely than not that the fair value is below the carrying value, goodwill is tested for impairment by determining the fair value of each reporting unit and comparing it to the carrying value of the net assets assigned to the reporting unit. If the fair value of the reporting unit exceeds its carrying value, goodwill is considered not impaired. If the carrying value of the reporting unit exceeds its fair value, we recognize an impairment loss up to the difference between the carrying value and implied fair value. We recognized a charge of $101 million in 2023 to impair all of the goodwill assigned to our SBU reporting unit based on our quantitative assessment for impairment in the current year. The quantitative assessment indicated that the fair value for all of our other reporting units substantially exceeded their carrying value.

Determining when to test for impairment, the reporting units, the assets and liabilities of the reporting unit, and the fair value of the reporting unit requires significant judgment and involves the use of significant estimates and assumptions. These estimates and assumptions include revenue growth rates, forecasted manufacturing costs, and other expenses and are developed as part of our long-range planning process. The same estimates are used in business planning, forecasting, and capital budgeting as part of our long-term manufacturing capacity analysis. These estimates and assumptions are used to calculate projected future cash flows for the reporting unit, which are discounted using a risk-adjusted rate to estimate a fair value. The discount rate requires determination of appropriate market comparables. We base fair value estimates on assumptions we believe to be reasonable but that are unpredictable and inherently uncertain. Actual future results may differ from those estimates. We assess the reasonableness of our methodology, forecasts, and assumptions by comparing the aggregate calculated fair value for our reporting units to our market capitalization.

***Income taxes*:** We are required to estimate our provision for income taxes and amounts ultimately payable or recoverable in numerous tax jurisdictions around the world. These estimates involve significant judgment and interpretations of regulations and are inherently complex. Resolution of income tax treatments in individual jurisdictions may not be known for many years after completion of the applicable year. We are also required to evaluate the realizability of our deferred tax assets on an ongoing basis in accordance with U.S. GAAP, which requires the assessment of our performance and other relevant factors. Realization of deferred tax assets is dependent on our ability to generate future taxable income. Our income tax provision or benefit is dependent, in part, on our ability to forecast future taxable income in Japan, Malaysia, the United States, Taiwan, and other jurisdictions. Such forecasts are inherently difficult and involve significant judgments including, among others, projecting future average selling prices and sales volumes, manufacturing and overhead costs, levels of capital spending, and other factors that significantly impact our analyses of the amount of net deferred tax assets that are more likely than not to be realized.

***Inventories*:** Inventories are stated at the lower of cost or net realizable value, with cost being determined on a first-in, first-out (“FIFO”) basis. Cost includes depreciation, labor, material, and overhead costs, including product and process technology costs. Determining net realizable value of finished goods and work in process inventories involves significant judgments, including projecting future average selling prices, future sales volumes, and future cost per part. To project average selling prices and sales volumes, we review recent sales volumes, existing customer orders, current contract prices, industry analyses of supply and demand, and general economic trends. To project cost per part, we review trends with historical results and consider known changes in our cost structure as applicable. Actual selling prices may vary significantly from projected prices due to the volatile nature of the semiconductor memory and storage markets. When these analyses reflect estimated net realizable values below our manufacturing costs, we record a charge to cost of goods sold in advance of when inventories are actually sold. As a result, the timing of when product costs are charged to costs of goods sold can vary significantly. Differences in future average selling prices used in calculating lower of cost or net realizable value adjustments can result in significant changes in the estimated net realizable value of finished goods and work in process inventories and accordingly the amount of write-down recorded. For example, a 5% decrease in future average selling prices would have changed the estimated net realizable value of our finished goods and work in process inventories by approximately $600 million as of August 31, 2023.

U.S. GAAP provides for products to be grouped into categories in order to compare costs to net realizable values. The amount of any inventory write-down can vary significantly depending on the determination of inventory categories. We review the major characteristics of product type and markets in determining the unit of account for which we perform the lower of cost or net realizable value analysis and categorize all inventories (including DRAM, NAND, and other memory) as a single group.

***Property, plant, and equipment*:** We periodically assess the estimated useful lives of our property, plant, and equipment based on technology node transitions, capital spending, and equipment re-use rates. We also review the carrying value of property, plant, and equipment for impairment when events and circumstances indicate that the carrying value of an asset or group of assets may not be recoverable from the estimated future cash flows expected to result from its use and/or disposition. In cases where undiscounted expected future cash flows are less than the carrying value, an impairment loss is recognized equal to the amount by which the carrying value exceeds the estimated fair value of the assets. The estimate of future cash flows involves numerous assumptions which require significant judgment by us, including, but not limited to, future use of the assets for our operations versus sale or disposal of the assets, future selling prices for our products, and future production and sales volumes.

***Revenue recognition*:** Revenue is primarily recognized at a point in time when control of the promised goods is transferred to our customers in an amount that reflects the consideration we expect to be entitled to in exchange for those goods. Contracts with our customers are generally short-term in duration at fixed, negotiated prices with payment generally due shortly after delivery. We estimate a liability for returns using the expected value method based on historical returns. In addition, we generally offer price protection to our distributors, which is a form of variable consideration that decreases the transaction price. We use the expected value method, based on historical price adjustments and current pricing trends, to estimate the amount of revenue recognized from sales to distributors. Differences between the estimated and actual amounts are recognized as adjustments to revenue.

Recently Adopted Accounting Standards

No material items.

Recently Issued Accounting Standards

No material items.

ITEM 7A. QUANTITATIVE AND QUALITATIVE DISCLOSURES ABOUT MARKET RISK

Interest Rate Risk

We are exposed to interest rate risk related to our indebtedness and our investment portfolio. As of August 31, 2023 and September 1, 2022, we had fixed-rate debt with an aggregate carrying value of $7.52 billion and $4.03 billion, respectively, and as a result, the fair value of our debt fluctuates with changes in market interest rates. We estimate that, as of August 31, 2023 and September 1, 2022, a hypothetical 1% decrease in market interest rates would increase the fair value of our fixed-rate debt by approximately $475 million and $275 million, respectively.

Interest rate risk related to our investment portfolio is managed by primarily investing in shorter term securities. We estimate that, as of August 31, 2023 and September 1, 2022, a hypothetical 1% increase in interest rates would decrease the fair value of our portfolio by approximately $20 million and $30 million, respectively. Such impact would only be realized if investments were sold prior to maturity.

As of August 31, 2023 and September 1, 2022, we had floating-rate debt, including fixed-rate debt that is swapped to floating-rate debt, with an aggregate principal amount of $4.63 billion and $2.09 billion, respectively. A hypothetical 1% increase in the interest rates of this floating-rate debt would result in an increase in annual interest expense of $46 million and $21 million as of August 31, 2023 and September 1, 2022, respectively.

Foreign Currency Exchange Rate Risk

The information in this section should be read in conjunction with the information related to changes in the currency exchange rates in “Part I – Item 1A. Risk Factors.” Changes in foreign currency exchange rates could materially adversely affect our business, results of operations, or financial condition.

The functional currency for all of our operations is the U.S. dollar. The substantial majority of our sales are transacted in the U.S. dollar; however, significant amounts of our operating expenses and capital expenditures, and certain assets and liabilities, are incurred in or exposed to other currencies, primarily the Chinese yuan, euro, Indian rupee, Japanese yen, Malaysian ringgit, New Taiwan dollar, and Singapore dollar. We have established currency risk management programs for our monetary assets and liabilities denominated in foreign currencies to hedge against fluctuations in the fair value and volatility of future cash flows caused by changes in currency exchange rates. We generally utilize currency forward contracts in these hedging programs, which reduce, but do not always entirely eliminate, the impact of currency exchange rate movements. We do not use derivative financial instruments for trading or speculative purposes.

Based on monetary assets and liabilities denominated in foreign currencies, we estimate that a hypothetical 10% adverse change in exchange rates versus the U.S. dollar would result in losses of approximately $129 million as of August 31, 2023 and $186 million as of September 1, 2022. We hedge our exposure to changes in currency exchange rates by utilizing a rolling hedge strategy for our primary currency exposures with currency forward contracts that generally mature within three months. The effectiveness of our hedges is dependent, among other factors, upon our ability to accurately measure exposures on a timely basis. To hedge the exposure of changes in cash flows from changes in currency exchange rates for certain capital expenditures and manufacturing costs, we may utilize currency forward contracts that generally mature within two years. See “Item 8. Financial Statements and Supplementary Data – Notes to Consolidated Financial Statements – Derivative Instruments.”

ITEM 8. FINANCIAL STATEMENTS AND SUPPLEMENTARY DATA

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Micron Technology, Inc.
Consolidated Statements of Operations

(In millions, except per share amounts)

For the year ended	August 31, 2023	September 1, 2022	September 2, 2021
Revenue	$ 15,540	$ 30,758	$ 27,705
Cost of goods sold	16,956	16,860	17,282
Gross margin	(1,416)	13,898	10,423
Research and development	3,114	3,116	2,663
Selling, general, and administrative	920	1,066	894
Restructure and asset impairments	171	48	488
Other operating (income) expense, net	124	(34)	95
Operating income (loss)	(5,745)	9,702	6,283
Interest income	468	96	37
Interest expense	(388)	(189)	(183)
Other non-operating income (expense), net	7	(38)	81
	(5,658)	9,571	6,218
Income tax (provision) benefit	(177)	(888)	(394)
Equity in net income (loss) of equity method investees	2	4	37
Net income (loss)	$ (5,833)	$ 8,687	$ 5,861
Earnings (loss) per share			
Basic	$ (5.34)	$ 7.81	$ 5.23
Diluted	(5.34)	7.75	5.14
Number of shares used in per share calculations			
Basic	1,093	1,112	1,120
Diluted	1,093	1,122	1,141

See accompanying notes to consolidated financial statements.

Micron Technology, Inc.
Consolidated Statements of Comprehensive Income (Loss)

(In millions)

For the year ended	August 31, 2023	September 1, 2022	September 2, 2021
Net income (loss)	$ (5,833)	$ 8,687	$ 5,861
Other comprehensive income (loss), net of tax			
Gains (losses) on derivative instruments	234	(516)	(67)
Pension liability adjustments	11	3	3
Unrealized gains (losses) on investments	6	(48)	(7)
Foreign currency translation adjustments	(3)	(1)	2
Other comprehensive income (loss)	248	(562)	(69)
Total comprehensive income (loss)	$ (5,585)	$ 8,125	$ 5,792

See accompanying notes to consolidated financial statements.

Micron Technology, Inc.
Consolidated Balance Sheets

(In millions, except par value amounts)

As of	August 31, 2023	September 1, 2022
Assets		
Cash and equivalents	$ 8,577	$ 8,262
Short-term investments	1,017	1,069
Receivables	2,443	5,130
Inventories	8,387	6,663
Other current assets	820	657
Total current assets	21,244	21,781
Long-term marketable investments	844	1,647
Property, plant, and equipment	37,928	38,549
Operating lease right-of-use assets	666	678
Intangible assets	404	421
Deferred tax assets	756	702
Goodwill	1,150	1,228
Other noncurrent assets	1,262	1,277
Total assets	$ 64,254	$ 66,283
Liabilities and equity		
Accounts payable and accrued expenses	$ 3,958	$ 6,090
Current debt	278	103
Other current liabilities	529	1,346
Total current liabilities	4,765	7,539
Long-term debt	13,052	6,803
Noncurrent operating lease liabilities	603	610
Noncurrent unearned government incentives	727	589
Other noncurrent liabilities	987	835
Total liabilities	20,134	16,376
Commitments and contingencies		
Shareholders' equity		
Common stock, $0.10 par value, 3,000 shares authorized, 1,239 shares issued and 1,098 outstanding (1,226 shares issued and 1,094 outstanding as of September 1, 2022)	124	123
Additional capital	11,036	10,197
Retained earnings	40,824	47,274
Treasury stock, 141 shares held (132 shares as of September 1, 2022)	(7,552)	(7,127)
Accumulated other comprehensive income (loss)	(312)	(560)
Total equity	44,120	49,907
Total liabilities and equity	$ 64,254	$ 66,283

See accompanying notes to consolidated financial statements.

Micron Technology, Inc.
Consolidated Statements of Changes in Equity

(In millions, except per share amounts)

	Common Stock						
	Number of Shares	Amount	Additional Capital	Retained Earnings	Treasury Stock	Accumulated Other Comprehensive Income (Loss)	Total Shareholders' Equity
Balance at September 3, 2020	1,194	$ 119	$ 8,917	$ 33,384	$ (3,495)	$ 71	$ 38,996
Net income (loss)	—	—	—	5,861	—	—	5,861
Other comprehensive income (loss), net	—	—	—	—	—	(69)	(69)
Stock issued under stock plans	13	2	223	—	—	—	225
Stock-based compensation expense	—	—	378	—	—	—	378
Repurchase of stock - repurchase program	—	—	—	—	(1,200)	—	(1,200)
Repurchase of stock - withholdings on employee equity awards	(2)	—	(12)	(82)	—	—	(94)
Stock issued for convertible notes	11	1	(1)	—	—	—	—
Cash settlement of convertible notes	—	—	(52)	—	—	—	(52)
Dividends and dividend equivalents declared ($0.10 per share)	—	—	—	(112)	—	—	(112)
Balance at September 2, 2021	1,216	$ 122	$ 9,453	$ 39,051	$ (4,695)	$ 2	$ 43,933
Net income (loss)	—	—	—	8,687	—	—	8,687
Other comprehensive income (loss), net	—	—	—	—	—	(562)	(562)
Stock issued under stock plans	12	1	244	—	—	—	245
Stock-based compensation expense	—	—	514	—	—	—	514
Repurchase of stock - repurchase program	—	—	—	—	(2,432)	—	(2,432)
Repurchase of stock - withholdings on employee equity awards	(2)	—	(14)	(112)	—	—	(126)
Dividends and dividend equivalents declared ($0.315 per share)	—	—	—	(352)	—	—	(352)
Balance at September 1, 2022	1,226	$ 123	$ 10,197	$ 47,274	$ (7,127)	$ (560)	$ 49,907
Net income (loss)	—	—	—	(5,833)	—	—	(5,833)
Other comprehensive income (loss), net	—	—	—	—	—	248	248
Stock issued under stock plans	15	1	262	—	—	—	263
Stock-based compensation expense	—	—	596	—	—	—	596
Repurchase of stock - repurchase program	—	—	—	—	(425)	—	(425)
Repurchase of stock - withholdings on employee equity awards	(2)	—	(19)	(108)	—	—	(127)
Dividends and dividend equivalents declared ($0.460 per share)	—	—	—	(509)	—	—	(509)
Balance at August 31, 2023	1,239	$ 124	$ 11,036	$ 40,824	$ (7,552)	$ (312)	$ 44,120

See accompanying notes to consolidated financial statements.

Micron Technology, Inc.
Consolidated Statements of Cash Flows

(In millions)

For the year ended	August 31, 2023	September 1, 2022	September 2, 2021
Cash flows from operating activities			
Net income (loss)	$ (5,833)	$ 8,687	$ 5,861
Adjustments to reconcile net income (loss) to net cash provided by operating activities:			
Depreciation expense and amortization of intangible assets	7,756	7,116	6,214
Provision to write down inventories to net realizable value	1,831	—	—
Stock-based compensation	596	514	378
Goodwill impairment	101	—	—
Restructure and asset impairments	11	44	454
Loss on debt repurchases and conversions	—	83	1
Change in operating assets and liabilities:			
Receivables	2,763	190	(1,446)
Inventories	(3,555)	(2,179)	866
Accounts payable and accrued expenses	(2,104)	744	210
Other	(7)	(18)	(70)
Net cash provided by operating activities	1,559	15,181	12,468
Cash flows from investing activities			
Expenditures for property, plant, and equipment	(7,676)	(12,067)	(10,030)
Purchases of available-for-sale securities	(723)	(1,770)	(3,163)
Proceeds from maturities of available-for-sale securities	1,566	1,321	1,250
Proceeds from government incentives	710	115	495
Proceeds from sales of available-for-sale securities	25	294	856
Proceeds from sale of Lehi, Utah fab	—	888	—
Other	(93)	(366)	3
Net cash provided by (used for) investing activities	(6,191)	(11,585)	(10,589)
Cash flows from financing activities			
Proceeds from issuance of debt	6,716	2,000	1,188
Repayments of debt	(761)	(2,032)	(1,520)
Payments of dividends to shareholders	(504)	(461)	—
Repurchases of common stock - repurchase program	(425)	(2,432)	(1,200)
Payments on equipment purchase contracts	(138)	(141)	(295)
Other	95	86	46
Net cash provided by (used for) financing activities	4,983	(2,980)	(1,781)
Effect of changes in currency exchange rates on cash, cash equivalents, and restricted cash	(34)	(106)	41
Net increase (decrease) in cash, cash equivalents, and restricted cash	317	510	139
Cash, cash equivalents, and restricted cash at beginning of period	8,339	7,829	7,690
Cash, cash equivalents, and restricted cash at end of period	$ 8,656	$ 8,339	$ 7,829
Supplemental disclosures			
Income taxes paid, net	$ (532)	$ (493)	$ (361)
Interest paid, net of amounts capitalized	(323)	(154)	(171)
Noncash equipment acquisitions on contracts payable	165	157	289

See accompanying notes to consolidated financial statements.

Micron Technology, Inc.

NOTES TO CONSOLIDATED FINANCIAL STATEMENTS

(All tabular amounts in millions, except per share amounts)

Significant Accounting Policies

Basis of Presentation

We are an industry leader in innovative memory and storage solutions transforming how the world uses information to enrich life *for all*. With a relentless focus on our customers, technology leadership, and manufacturing and operational excellence, Micron delivers a rich portfolio of high-performance DRAM, NAND, and NOR memory and storage products through our Micron® and Crucial® brands. Every day, the innovations that our people create fuel the data economy, enabling advances in artificial intelligence and 5G applications that unleash opportunities — from the data center to the intelligent edge and across the client and mobile user experience.

The accompanying consolidated financial statements include the accounts of Micron Technology, Inc. and our consolidated subsidiaries and have been prepared in accordance with accounting principles generally accepted in the United States of America. Intercompany balances and transactions have been eliminated in consolidation. Certain reclassifications have been made to prior period amounts to conform to current period presentation. See “Inventories” below for changes to our significant accounting policies, and the “Inventories” note for additional information.

Our fiscal year is the 52 or 53-week period ending on the Thursday closest to August 31. Fiscal 2023, 2022, and 2021 each contained 52 weeks. All period references are to our fiscal periods unless otherwise indicated.

Derivative and Hedging Instruments

We use derivative instruments to manage our exposure to changes in currency exchange rates from (1) our monetary assets and liabilities denominated in currencies other than the U.S. dollar and (2) forecasted cash flows for certain capital expenditures and manufacturing costs. We also use derivative instruments to manage our exposure to changes in commodity prices for manufacturing supplies and to minimize certain exposures to changes in the fair value of fixed-rate debt that result from fluctuations in benchmark interest rates. Derivative instruments are measured at their fair values and recognized as either assets or liabilities.

The accounting for changes in the fair value of derivative instruments is based on the intended use of the derivative and the resulting designation. For derivative instruments that are not designated for hedge accounting, gains or losses from changes in fair values are recognized in other non-operating income (expense) and cash flows are classified as investing activities in the statement of cash flows. For derivative instruments designated as cash flow hedges, gains or losses are included as a component of accumulated other comprehensive income and reclassified into earnings in the same line items and in the same periods in which the underlying transactions affect earnings. For derivative instruments designated as cash flow hedges, time value is excluded from the assessment of effectiveness and the gains and losses attributable to time value are recognized in earnings through an amortization approach. For derivative instruments designated as fair value hedges, changes in the fair values of the derivative instruments and the offsetting changes in the fair values of the underlying hedged items are both recognized in earnings. Cash flows from derivative instruments designated as cash flow hedges or fair value hedges are classified in the same category as the items being hedged.

We enter into master netting arrangements with our counterparties to mitigate credit risk in derivative hedge transactions. These master netting arrangements allow us and our counterparties to net settle amounts owed to each other. Derivative assets and liabilities that can be net settled with each counterparty have been presented in our consolidated balance sheet on a net basis.

Financial Instruments

Cash equivalents include highly liquid short-term investments with original maturities to us of three months or less that are readily convertible to known amounts of cash. Other investments with remaining maturities of less than one year are included in short-term investments. Investments with remaining maturities greater than one year are included in long-term marketable investments. The carrying value of investment securities sold is determined using the specific identification method.

Functional Currency

The U.S. dollar is the functional currency for us and all of our consolidated subsidiaries.

Goodwill

We perform an annual impairment assessment for goodwill in our fourth quarter each year.

Government Incentives

We receive incentives from governmental entities related to capital expenditures, expenses, and other activities. Our government incentives may require that we meet or maintain specified spending levels and other operational metrics and may be subject to reimbursement if such conditions are not met or maintained. Government incentives are recorded in the financial statements in accordance with their purpose: as a reduction of asset costs or a reduction of expenses. Incentives related to the acquisition or construction of fixed assets are recognized as a reduction in the carrying amounts of the related assets and reduce depreciation expense over the useful lives of the assets. Incentives related to specific operating activities are offset against the related expense in the period the expense is incurred. Government incentives received prior to being earned are recognized in current or noncurrent deferred income or restricted cash, whereas government incentives earned prior to being received are recognized in current or noncurrent receivables. Cash received from government incentives related to operating expenses is included as an operating activity in the statement of cash flows, whereas cash received from incentives related to the acquisition of property, plant, and equipment is included as an investing activity.

Inventories

Effective as of the beginning of the second quarter of 2021, we changed the method of inventory costing from average cost to FIFO. The difference between average cost and FIFO was not material to any previously reported financial statements. Therefore, we have recognized the cumulative effect of the change as a reduction of inventories and a charge to cost of goods sold of $133 million as of the beginning of the second quarter of 2021.

Inventories are stated at the lower of cost or net realizable value, with cost being determined on a FIFO basis. Cost includes depreciation, labor, material, and overhead costs, including product and process technology costs. Determining net realizable value of finished goods and work in process inventories requires projecting future average selling prices, sales volumes, and costs per part. When net realizable value is below cost, we record a charge to cost of goods sold to write down inventories to their estimated net realizable value in advance of when inventories are actually sold. We review the major characteristics of product type and markets in determining the unit of account for which we perform the lower of cost or net realizable value analysis and categorize all inventories (including DRAM, NAND, and other memory) as a single group.

Leases

We determine if an arrangement is a lease, or contains a lease, at the inception of the arrangement and evaluate whether the lease is an operating lease or a finance lease at the commencement date. We recognize right-of-use assets and lease liabilities for operating and finance leases with terms greater than 12 months. Right-of-use assets represent our right to use an asset for the lease term, while lease liabilities represent our obligation to make lease payments. We do not separate lease and non-lease components for real-estate and gas plant leases. Sublease income is included within lease expense.

Product and Process Technology

Costs incurred to (1) acquire product and process technology, (2) patent technology, and (3) maintain patent technology, are capitalized and amortized on a straight-line basis over periods ranging up to 12.5 years. We capitalize a portion of costs incurred to patent technology based on historical data of patents issued as a percent of patents we file. Product and process technology costs are amortized over the shorter of (1) the estimated useful life of the technology, (2) the patent term, or (3) the term of the technology agreement. Fully-amortized assets are removed from product and process technology and accumulated amortization.

Product Warranty

We generally provide a limited warranty that our products are in compliance with applicable specifications existing at the time of delivery. Under our standard terms and conditions of sale, liability for certain failures of product during a stated warranty period is usually limited to repair or replacement of defective items or return of, or a credit with respect to, amounts paid for such items. Under certain circumstances, we provide more extensive limited warranty coverage than that provided under our standard terms and conditions. Our warranty obligations are not material.

Property, Plant, and Equipment

Property, plant, and equipment is stated at cost and depreciated using the straight-line method over estimated useful lives of generally 10 to 30 years for buildings, 7 years for production equipment, up to 7 years for other equipment, and 3 to 5 years for software. Assets held for sale are carried at the lower of estimated fair value or carrying value and are included in current assets. When property, plant, or equipment is retired or otherwise disposed, the net book value is removed and we recognize any gain or loss in results of operations.

We capitalize interest on borrowings during the period of time we carry out the activities necessary to bring assets to the condition of their intended use and location. Capitalized interest becomes part of the cost of assets.

Research and Development

Costs related to the conceptual formulation and design of products and processes are charged to R&D expense as incurred. Development of a product is deemed complete when it is qualified through reviews and tests for performance and reliability. Subsequent to product qualification, product costs are included in cost of goods sold. Amounts from cost-sharing arrangements are reflected as a reduction of R&D expense.

Revenue Recognition

Revenue is primarily recognized at a point in time when control of the promised goods is transferred to our customers in an amount that reflects the consideration we expect to be entitled to in exchange for those goods. Contracts with our customers are generally short-term in duration at fixed, negotiated prices with payment generally due shortly after delivery. We estimate a liability for returns using the expected value method based on historical returns. In addition, we generally offer price protection to our distributors, which is a form of variable consideration that decreases the transaction price. We use the expected value method, based on historical price adjustments and current pricing trends, to estimate the amount of revenue recognized from sales to distributors. Differences between the estimated and actual amounts are recognized as adjustments to revenue.

Stock-based Compensation

Stock-based compensation is measured at the grant date, based on the fair value of the award, and recognized as expense under the straight-line attribution method over the requisite service period. We account for forfeitures as they occur. We issue new shares upon the exercise of stock options, conversion of share units, or issuance of shares under our ESPP.

Treasury Stock

Treasury stock is carried at cost. When we retire our treasury stock, any excess of the repurchase price paid over par value is allocated between additional capital and retained earnings.

Use of Estimates

The preparation of financial statements and related disclosures in conformity with accounting principles generally accepted in the United States of America requires our management to make estimates and judgments that affect the reported amounts of assets, liabilities, revenues, expenses, and related disclosures. Estimates and judgments are based on historical experience, forecasted events, and various other assumptions that we believe to be reasonable under the circumstances. Estimates and judgments may differ under different assumptions or conditions. We evaluate our estimates and judgments on an ongoing basis. Actual results could differ from estimates.

Lehi, Utah Fab and 3D XPoint

In 2021, we updated our portfolio strategy to further strengthen our focus on memory and storage innovations for the data center market. In connection therewith, we determined that there was insufficient market validation to justify the ongoing investments required to commercialize 3D XPoint at scale. Accordingly, we ceased development of 3D XPoint technology and engaged in discussions for the sale of our facility located in Lehi, Utah that was dedicated to 3D XPoint production. As a result, we classified the property, plant, and equipment as held for sale in 2021, ceased depreciating the assets, and recognized a $435 million restructure and asset impairment charge and a $104 million tax benefit.

We closed the sale of our Lehi facility to TI in 2022 for $893 million and disposed of $918 million of net assets, consisting primarily of property, plant, and equipment, resulting in a $23 million loss, net of selling expenses and other adjustments.

Variable Interest Entities

A number of special purpose entities (the "Lease SPEs") were created by a third-party to facilitate equipment lease financing transactions between us and financial institutions that fund the lease financing transactions ("Financing Entities"). Neither we nor the Financing Entities have an equity interest in the Lease SPEs. The Lease SPEs are variable interest entities because their equity is not sufficient to permit them to finance their activities without additional support from the Financing Entities and because the third-party equity holder lacks characteristics of a controlling financial interest. By design, the arrangements with the Lease SPEs are merely financing vehicles and we do not bear any significant risks from variable interests with the Lease SPEs. We have determined that we do not have the power to direct the activities of the Lease SPEs that most significantly impact their economic performance and we do not consolidate the Lease SPEs.

Cash and Investments

All of our short-term investments and long-term marketable investments were classified as available-for-sale as of the dates noted below. Cash and equivalents and the fair values of our available-for-sale investments, which approximated amortized costs, were as follows:

	As of August 31, 2023				As of September 1, 2022			
	Cash and Equivalents	Short-term Investments	Long-term Marketable Investments[1]	Total Fair Value	Cash and Equivalents	Short-term Investments	Long-term Marketable Investments[1]	Total Fair Value
Cash	$ 5,771	$ —	$ —	$ 5,771	$ 6,055	$ —	$ —	$ 6,055
Level 1[2]								
Money market funds	1,629	—	—	1,629	1,196	—	—	1,196
Level 2[3]								
Certificates of deposit	1,172	25	—	1,197	976	50	—	1,026
Corporate bonds	—	737	437	1,174	—	759	995	1,754
Asset-backed securities	—	15	387	402	—	20	608	628
Government securities	5	131	20	156	2	155	44	201
Commercial paper	—	109	—	109	33	85	—	118
	8,577	$ 1,017	$ 844	$ 10,438	8,262	$ 1,069	$ 1,647	$ 10,978
Restricted cash[4]	79				77			
Cash, cash equivalents, and restricted cash	$ 8,656				$ 8,339			

(1) *The maturities of long-term marketable investments primarily range from one to five years, except for asset-backed securities which are not due at a single maturity date.*

(2) *The fair value of Level 1 securities is measured based on quoted prices in active markets for identical assets.*

(3) *The fair value of Level 2 securities is measured using information obtained from pricing services, which obtain quoted market prices for similar instruments, non-binding market consensus prices that are corroborated by observable market data, or various other methodologies, to determine the appropriate value at the measurement date. We perform supplemental analysis to validate information obtained from these pricing services. No adjustments were made to the fair values indicated by such pricing information as of August 31, 2023 or September 1, 2022.*

(4) *Restricted cash is included in other current assets and other noncurrent assets and primarily relates to certain government incentives received prior to being earned and for which restrictions lapse upon achieving certain performance conditions or which will be returned if performance conditions are not met.*

Gross realized gains and losses from sales of available-for-sale securities were not significant for any period presented.

Non-marketable Equity Investments

In addition to the amounts included in the table above, we had $218 million and $222 million of non-marketable equity investments without a readily determinable fair value that were included in other noncurrent assets as of August 31, 2023 and September 1, 2022, respectively. For non-marketable investments, we recognized in other non-operating income (expense) a net loss of $7 million for 2023 and net gains of $36 million for 2022 and $70 million for 2021. Our non-marketable equity investments are recorded at fair value on a non-recurring basis and classified as Level 3.

Receivables

As of	August 31, 2023	September 1, 2022
Trade receivables	$ 2,048	$ 4,765
Income and other taxes	194	251
Other	201	114
	$ 2,443	$ 5,130

Inventories

As of	August 31, 2023	September 1, 2022
Finished goods	$ 1,616	$ 1,028
Work in process	6,111	4,830
Raw materials and supplies	660	805
	$ 8,387	$ 6,663

In 2023, we recorded charges of $1.83 billion to cost of goods sold to write down the carrying value of work in process and finished goods inventories to their estimated net realizable value.

Effective as of the beginning of the second quarter of 2021, we changed our method of inventory costing from average cost to FIFO. This change in accounting principle is preferable because in an environment with continuously changing production costs FIFO more closely matches the actual cost of goods sold with the revenues from sales of those specific units, better represents the actual cost of inventories remaining on hand at any period-end, and improves comparability with our semiconductor industry peers. The change to FIFO was not material to any prior periods, nor was the cumulative effect of $133 million material to the second quarter of 2021. As such, prior periods were not retrospectively adjusted, and the cumulative effect was reported as an increase to cost of goods sold for the second quarter of 2021 of $133 million, with an offsetting reduction to beginning inventories. This charge resulted in a corresponding reduction to operating income (loss), a $128 million reduction to net income (loss), and an $0.11 reduction to diluted earnings per share for both the second quarter and the year ended 2021.

Property, Plant, and Equipment

As of	August 31, 2023	September 1, 2022
Land	$ 283	$ 280
Buildings	17,967	16,676
Equipment[1]	65,555	61,354
Construction in progress[2]	2,464	1,897
Software	1,316	1,124
	87,585	81,331
Accumulated depreciation	(49,657)	(42,782)
	$ 37,928	$ 38,549

(1) *Includes costs related to equipment not placed into service of $2.91 billion as of August 31, 2023 and $3.35 billion as of September 1, 2022.*

(2) *Includes building-related construction, tool installation, and software costs for assets not placed into service.*

Depreciation expense was $7.67 billion, $7.03 billion, and $6.13 billion for 2023, 2022, and 2021, respectively. Interest capitalized as part of the cost of property, plant, and equipment was $208 million, $77 million, and $66 million for 2023, 2022, and 2021, respectively.

Intangible Assets

	As of August 31, 2023			As of September 1, 2022		
	Gross Amount	Accumulated Amortization	Net Carrying Amount	Gross Amount	Accumulated Amortization	Net Carrying Amount
Product and process technology	$ 613	$ (209)	$ 404	$ 742	$ (321)	$ 421

In 2023, 2022, and 2021, we capitalized $87 million, $158 million, and $106 million, respectively, for product and process technology with weighted-average useful lives of 9 years. Amortization expense was $86 million, $85 million, and $82 million for 2023, 2022, and 2021, respectively. Expected amortization expense is $75 million for 2024, $51 million for 2025, $47 million for 2026, $43 million for 2027, and $42 million for 2028.

Goodwill

As of	August 31, 2023	September 1, 2022
Goodwill	$ 1,150	$ 1,228

In the fourth quarter of 2023, we recognized a charge of $101 million included in other operating income (loss) to impair all of the goodwill assigned to our SBU reporting unit based on a quantitative assessment for impairment. We evaluated the fair value of our reporting units for the assessment based on an income approach, which uses a discounted cash flow methodology. The impairment of SBU goodwill reflects lower forecasted cash flows for SBU as a result of adverse conditions in the storage industry environment due to weak demand in many end markets combined with global and macroeconomic challenges and lower demand resulting from customer actions to reduce elevated inventory levels. These conditions led to significant reductions in SBU's average selling prices and bit shipments, driving declines in revenue and cash flows. The quantitative assessment for impairment indicated that the fair value for all of our other reporting units substantially exceeded their carrying value.

As of August 31, 2023, CNBU, MBU, and EBU had goodwill of $855 million, $198 million, and $97 million, respectively. As of September 1, 2022, CNBU, MBU, SBU, and EBU had goodwill of $832 million, $198 million, $101 million, and $97 million, respectively. The Company added $23 million of goodwill to CNBU from an acquisition in the third quarter of 2023.

Leases

We have finance and operating leases through which we obtain the right to use facilities, land, and equipment that support our business operations. Our finance leases consist primarily of (i) gas and other supply agreements that are deemed to contain embedded leases and (ii) equipment leases. Our operating leases consist primarily of offices, laboratories, other facilities, and land. Certain of our operating leases include one or more options to extend the lease term for periods from one year to 10 years for real estate and one year to 99 years for land.

Certain supply or service agreements require us to exercise significant judgment to determine whether the agreement contains a lease. Our assessment includes determining whether we or the supplier control the assets used to fulfill the agreements by identifying whether we or the supplier have the right to change the type, quantity, timing, or location of the output of the assets. Our gas supply arrangements generally are deemed to contain a lease because we have the right to substantially all of the output of the assets used to produce the supply and we have the right to change the quantity and timing of the output of those assets. In determining the lease term, we assess whether we are reasonably certain to exercise any options to renew or terminate a lease or to purchase the right-of-use asset. Measuring the present value of the initial lease liability requires judgment to determine the discount rate, which we base on interest rates for borrowings with similar terms and collateral issued by entities with credit ratings similar to ours.

The components of lease cost are presented below:

For the year ended	2023	2022	2021
Finance lease cost			
Amortization of right-of-use asset	$ 105	$ 99	$ 69
Interest on lease liability	24	24	20
Operating lease cost[1]	137	125	108
	$ 266	$ 248	$ 197

[1] *Operating lease cost includes short-term and variable lease expenses, which were not material for the periods presented.*

Supplemental cash flow information related to leases was as follows:

For the year ended	2023	2022	2021
Cash flows used for operating activities			
Finance leases	$ 24	$ 23	$ 21
Operating leases	139	110	106
Cash flows used for financing activities – Finance leases	109	103	85
Noncash acquisitions of right-of-use assets			
Finance leases	508	309	395
Operating leases	57	197	27

Supplemental balance sheet information related to leases was as follows:

As of	August 31, 2023	September 1, 2022
Finance lease right-of-use assets (included in property, plant, and equipment)	$ 1,311	$ 904
Current operating lease liabilities (included in accounts payable and accrued expenses)	66	60
Weighted-average remaining lease term (in years)		
Finance leases	9	12
Operating leases	11	12
Weighted-average discount rate		
Finance leases	3.86 %	2.65 %
Operating leases	3.21 %	2.90 %

As of August 31, 2023, maturities of lease liabilities by fiscal year were as follows:

For the year ending	Finance Leases	Operating Leases
2024	$ 219	$ 62
2025	200	77
2026	190	76
2027	185	76
2028	178	74
2029 and thereafter	506	453
Less imputed interest	(197)	(149)
	$ 1,281	$ 669

The table above excludes obligations for leases that have been executed but have not yet commenced. As of August 31, 2023, excluded obligations consisted of $170 million of finance lease obligations over a weighted-average period of 12 years for gas supply arrangements deemed to contain embedded leases and equipment leases. We will recognize right-of-use assets and associated lease liabilities at the time such assets become available for our use.

Accounts Payable and Accrued Expenses

As of	August 31, 2023	September 1, 2022
Accounts payable	$ 1,725	$ 2,142
Property, plant, and equipment	1,419	2,170
Salaries, wages, and benefits	367	877
Income and other taxes	67	420
Other	380	481
	$ 3,958	$ 6,090

Debt

	As of August 31, 2023						As of September 1, 2022			
				Net Carrying Amount				Net Carrying Amount		
	Stated Rate	Effective Rate	Principal	Current	Long-Term	Total	Principal	Current	Long-Term	Total
2024 Term Loan A	6.146 %	6.18 %	$ 588	$ —	$ 587	$ 587	$ 1,188	$ —	$ 1,187	$ 1,187
2025 Term Loan A	6.681 %	6.82 %	1,052	—	1,050	1,050	—	—	—	—
2026 Term Loan A	6.806 %	6.94 %	971	49	921	970	—	—	—	—
2027 Term Loan A	6.931 %	7.07 %	1,123	57	1,063	1,120	—	—	—	—
2026 Notes	4.975 %	5.07 %	500	—	499	499	500	—	498	498
2027 Notes[(1)]	4.185 %	4.27 %	900	—	798	798	900	—	806	806
2028 Notes	5.375 %	5.52 %	600	—	596	596	—	—	—	—
2029 A Notes	5.327 %	5.40 %	700	—	697	697	700	—	697	697
2029 B Notes	6.750 %	6.54 %	1,250	—	1,263	1,263	—	—	—	—
2030 Notes	4.663 %	4.73 %	850	—	846	846	850	—	846	846
2032 Green Bonds	2.703 %	2.77 %	1,000	—	995	995	1,000	—	994	994
2033 A Notes	5.875 %	5.96 %	750	—	745	745	—	—	—	—
2033 B Notes	5.875 %	6.01 %	900	—	890	890	—	—	—	—
2041 Notes	3.366 %	3.41 %	500	—	497	497	500	—	496	496
2051 Notes	3.477 %	3.52 %	500	—	496	496	500	—	496	496
Finance lease obligations	N/A	3.86 %	1,281	172	1,109	1,281	886	103	783	886
			$ 13,465	$ 278	$ 13,052	$ 13,330	$ 7,024	$ 103	$ 6,803	$ 6,906

[(1)] *In 2021, we entered into fixed-to-floating interest rate swaps on the 2027 Notes with an aggregate $900 million notional amount equal to the principal amount of the 2027 Notes. The resulting variable interest paid is at a rate equal to SOFR plus approximately 3.33%. The fixed-to-floating interest rate swaps are accounted for as fair value hedges, and as a result, the carrying values of our 2027 Notes reflect adjustments in fair value.*

As of August 31, 2023, all of our debt, other than finance lease obligations, were unsecured obligations that rank equally in right of payment with all of our other existing and future unsecured indebtedness and were effectively subordinated to all future secured indebtedness, to the extent of the value of the assets securing such indebtedness. All our unsecured debt were obligations of our parent company, Micron, and were structurally subordinated to all liabilities of its subsidiaries, including trade payables. The terms of our indebtedness generally contain cross payment default and cross acceleration provisions. Micron's guarantees of certain liabilities of its subsidiaries are unsecured obligations ranking equally in right of payment with all of Micron's other existing and future unsecured indebtedness.

Debt Activity

The table below presents the effects of debt financing and prepayment activities in 2023:

	Transaction Date	Increase (Decrease) in Principal	Increase (Decrease) in Carrying Value	Increase (Decrease) in Cash
Issuances				
2029 B Notes	October 31, 2022	$ 750	$ 744	$ 744
2025 Term Loan A	November 3, 2022	927	925	925
2026 Term Loan A	November 3, 2022	746	745	745
2027 Term Loan A	November 3, 2022	927	924	924
2025 Term Loan A	January 5, 2023	125	125	125
2026 Term Loan A	January 5, 2023	250	249	249
2027 Term Loan A	January 5, 2023	225	225	225
2029 B Notes	February 9, 2023	500	520	520
2033 A Notes	February 9, 2023	750	745	745
2028 Notes	April 11, 2023	600	596	596
2033 B Notes	April 11, 2023	900	890	890
Prepayments				
2024 Term Loan A	April 13, 2023	(600)	(600)	(600)
		$ 6,100	$ 6,088	$ 6,088

In 2022, we issued $2.00 billion of senior unsecured notes and received cash of $1.99 billion. The approximate $1.00 billion of net proceeds from the issuance of the 2032 Green Bonds are being used to fund eligible sustainability-focused projects. The remaining proceeds, along with cash on hand, were used to repay $1.85 billion of principal amount of notes (carrying value of $1.85 billion) for $1.93 billion in cash. We recognized losses of $83 million in connection with these repayments.

In 2021, substantially all holders of our 2032D Notes converted their notes. We settled these conversions and all remaining 2032D Notes with $185 million in cash and 11.1 million shares of our stock, which approximated the carrying value of debt and equity for those notes.

Senior Unsecured Notes

We may redeem our 2026 Notes, 2027 Notes, 2028 Notes, 2029 A Notes, 2029 B Notes, 2030 Notes, 2032 Green Bonds, 2033 A Notes, 2033 B Notes, 2041 Notes, and 2051 Notes (the "Senior Unsecured Notes"), in whole or in part, at our option prior to their respective maturity dates at a redemption price equal to the greater of (i) 100% of the principal amount of the notes to be redeemed and (ii) the present value of the remaining scheduled payments of principal and interest, in each case plus accrued interest. We may also redeem any series of our Senior Unsecured Notes, in whole or in part, at a price equal to par between one and six months prior to maturity in accordance with the respective terms of such series.

Each series of Senior Unsecured Notes contains covenants that, among other things, limit, in certain circumstances, our ability and/or the ability of our restricted subsidiaries (which are generally domestic subsidiaries in which we own at least 80% of the voting stock and which own principal property, as defined in the indenture governing such series) to (1) create or incur certain liens; (2) enter into certain sale and lease-back transactions; and (3) consolidate with or merge with or into, or convey, transfer, or lease all or substantially all of our properties and assets, to another entity. These covenants are subject to a number of limitations and exceptions. Additionally, if a change of control triggering event, as defined in the indentures governing our Senior Unsecured Notes, occurs with respect to a series of Senior Unsecured Notes, we will be required to offer to purchase such Senior Unsecured Notes at 101% of the outstanding aggregate principal amount plus accrued interest up to the purchase date.

2032 Green Bonds: We plan to allocate an amount equal to the approximate $1.00 billion of net proceeds of our unsecured 2032 Green Bonds by November 1, 2023, to fund eligible sustainability-focused projects involving renewable energy, green buildings, energy efficiency, water management, waste abatement, and a circular economy.

Multi-Tranche Term Loan A

In 2023, we entered into a term loan agreement consisting of three tranches (the “Multi-Tranche Term Loan Agreement”) and borrowed $3.20 billion in aggregate principal amount. The tranches mature on November 3, 2025 (“2025 Term Loan A”); November 3, 2026 (“2026 Term Loan A”); and November 3, 2027 (“2027 Term Loan A”).

The 2026 Term Loan A and 2027 Term Loan A each require equal quarterly installment payments in an amount equal to 1.25% of the original principal amount. The 2025 Term Loan A does not require quarterly installment payments. Borrowings under the Multi-Tranche Term Loan Agreement will generally bear interest at adjusted term SOFR plus an applicable interest rate margin ranging from 1.00% to 2.00%, varying by tranche and depending on our corporate credit ratings. Adjusted term SOFR for the Multi-Tranche Term Loan Agreement is the SOFR benchmark plus 0.10%.

The Multi-Tranche Term Loan Agreement requires us to maintain, on a consolidated basis, a leverage ratio of total indebtedness to adjusted EBITDA, as defined in the Multi-Tranche Term Loan Agreement and calculated as of the last day of each fiscal quarter, not to exceed 3.25 to 1.00. On March 27, 2023, we amended the Multi-Tranche Term Loan Agreement to provide that in lieu of the foregoing leverage ratio, during the fourth quarter of 2023 and each quarter of 2024, we will be required to maintain, on a consolidated basis, a net leverage ratio of total net indebtedness to adjusted EBITDA, as defined in the Multi-Tranche Term Loan Agreement and calculated as of the last day of each fiscal quarter, not to exceed 3.25 to 1.00. Alternatively, for up to three of such five quarters, we may elect to comply with a requirement of minimum liquidity, as defined in the Multi-Tranche Term Loan Agreement, of not less than $5.0 billion. In the fourth quarter of 2023, we complied with the net leverage ratio. Each of the leverage ratio and net leverage ratio maximums, as applicable, is subject to a temporary four quarter increase in such ratio to 3.75 to 1.00 following certain material acquisitions.

The Multi-Tranche Term Loan Agreement contains other covenants that, among other things, limit, in certain circumstances, our ability and/or the ability of our restricted subsidiaries to (1) create or incur certain liens and enter into sale and lease-back transactions, (2) create, assume, incur, or guarantee certain additional secured indebtedness and unsecured indebtedness of our restricted subsidiaries, and (3) consolidate with or merge with or into, or convey, transfer, lease, or otherwise dispose of all or substantially all of our assets, to another entity. These covenants are subject to a number of limitations, exceptions, and qualifications. Our obligations under the Multi-Tranche Term Loan Agreement are unsecured.

2024 Term Loan A

On April 13, 2023, we used a portion of the proceeds from our April 2023 issuance of senior unsecured notes to prepay $600 million principal amount of our 2024 Term Loan A.

On June 7, 2023, the 2024 Term Loan A agreement was amended, pursuant to its transition provisions, to replace LIBOR-based benchmark rates with SOFR-based benchmark rates effective July 1, 2023. Subsequent to this amendment, borrowings under the 2024 Term Loan Agreement generally bear interest at adjusted term SOFR plus an applicable interest rate margin ranging from 0.625% to 1.375% depending on our corporate credit ratings. Adjusted term SOFR for the 2024 Term Loan A is the SOFR benchmark plus a credit spread adjustment ranging from approximately 0.11% to 0.43% depending on the applicable interest period selected. Prior to July 1, 2023, the 2024 Term Loan A bore interest at a rate equal to LIBOR plus 0.625% to 1.375% based on our corporate credit ratings.

The 2024 Term Loan A agreement contains the same leverage ratio, as amended, and substantially the same other covenants as the Multi-Tranche Term Loan Agreement. Our obligations under the 2024 Term Loan A agreement are unsecured.

Revolving Credit Facility

As of August 31, 2023, no amounts were outstanding under the Revolving Credit Facility and $2.50 billion was available to us. Under the Revolving Credit Facility, borrowings would generally bear interest at a rate equal to adjusted term SOFR plus 1.00% to 1.75%, depending on our corporate credit ratings. Adjusted term SOFR for the Revolving Credit Facility agreement is the SOFR benchmark plus a credit spread adjustment ranging from approximately 0.11% to 0.43% depending on the applicable interest period selected. Any amounts outstanding under the Revolving Credit Facility would mature in May 2026 and amounts borrowed may be prepaid without penalty.

The Revolving Credit Facility contains the same leverage ratio, as amended, and substantially the same other covenants as the Multi-Tranche Term Loan Agreement.

Maturities of Notes Payable

As of August 31, 2023, maturities of notes payable by fiscal year were as follows:

2024	$	107
2025		695
2026		1,659
2027		1,780
2028		1,493
2029 and thereafter		6,450
Unamortized issuance costs, discounts, and premium, net		(35)
Hedge accounting fair value adjustment		(100)
	$	12,049

Commitments

As of August 31, 2023, we had noncancelable commitments with remaining contractual terms in excess of one year of approximately $6.7 billion for purchase obligations, of which approximately $1.2 billion will be due in 2024, $1.4 billion due in 2025, $1.0 billion due in 2026, $1.0 billion due in 2027, $700 million due in 2028, and $1.4 billion due in 2029 and thereafter. Purchase obligations primarily include payments for goods or services with either a fixed or minimum quantity and price, which includes payments for the acquisition of property, plant, and equipment. Payments for leases that have been executed but have not yet commenced are excluded.

In 2023, we entered into an 18-year power purchase agreement in Singapore to purchase up to 450 megawatts of power at predominantly variable prices. This contract is expected to supply the majority of our power consumption needs in Singapore with more favorable pricing than our previous supply arrangements.

Contingencies

We are currently a party to legal actions other than those described below arising from the normal course of business, none of which are expected to have a material adverse effect on our business, results of operations, or financial condition.

Patent Matters

As is typical in the semiconductor and other high-tech industries, from time to time, others have asserted, and may in the future assert, that our products or manufacturing processes infringe upon their intellectual property rights.

On March 19, 2018, Micron Semiconductor (Xi'an) Co., Ltd. ("MXA") was served with a patent infringement complaint filed by Fujian Jinhua Integrated Circuit Co., Ltd. ("Jinhua") in the Fuzhou Intermediate People's Court in Fujian Province, China (the "Fuzhou Court"). On April 3, 2018, Micron Semiconductor (Shanghai) Co. Ltd. ("MSS") was served with the same complaint. The complaint alleges that MXA and MSS infringed one Chinese patent by manufacturing and selling certain Crucial DDR4 DRAM modules. The complaint seeks an order requiring MXA and MSS to destroy inventory of the accused products and equipment for manufacturing the accused products in China; to stop manufacturing, using, selling, and offering for sale the accused products in China; and to pay damages of 98 million Chinese yuan plus court fees incurred.

On March 21, 2018, MXA was served with a patent infringement complaint filed by United Microelectronics Corporation ("UMC") in the Fuzhou Court. On April 3, 2018, MSS was served with the same complaint. The complaint alleges that MXA and MSS infringed one Chinese patent by manufacturing and selling certain Crucial DDR4 DRAM modules. The complaint seeks an order requiring MXA and MSS to destroy inventory of the accused products and equipment for manufacturing the accused products in China; to stop manufacturing, using, selling, and offering for sale the accused products in China; and to pay damages of 90 million Chinese yuan plus court fees incurred. On November 26, 2021, pursuant to a settlement agreement between UMC and Micron, UMC filed an application to the Fuzhou Court to withdraw its complaints against MXA and MSS.

On April 3, 2018, MSS was served with another patent infringement complaint filed by Jinhua and an additional complaint filed by UMC in the Fuzhou Court. The additional complaints allege that MSS infringes two Chinese patents by manufacturing and selling certain Crucial MX300 SSDs. The complaint filed by UMC seeks an order requiring MSS to destroy inventory of the accused products and equipment for manufacturing the accused products in China; to stop manufacturing, using, selling, and offering for sale the accused products in China; and to pay damages of 90 million Chinese yuan plus court fees incurred. The complaint filed by Jinhua seeks an order requiring MSS to destroy inventory of the accused products and equipment for manufacturing the accused products in China; to stop manufacturing, using, selling, and offering for sale the accused products in China; and to pay damages of 98 million Chinese yuan plus court fees incurred. On November 26, 2021, pursuant to a settlement agreement between UMC and Micron, UMC filed an application to the Fuzhou Court to withdraw its complaint against MSS.

On July 5, 2018, MXA and MSS were notified that the Fuzhou Court granted a preliminary injunction against those entities that enjoins them from manufacturing, selling, or importing certain Crucial and Ballistix-branded DRAM modules and solid-state drives in China. We are complying with the ruling and have requested the Fuzhou Court to reconsider or stay its decision.

On April 28, 2021, Netlist, Inc. (“Netlist”) filed two patent infringement actions against Micron, Micron Semiconductor Products, Inc. (“MSP”), and Micron Technology Texas, LLC (“MTEC”) in the U.S. District Court for the Western District of Texas. The first complaint alleges that one U.S. patent is infringed by certain of our non-volatile dual in-line memory modules. The second complaint alleges that three U.S. patents are infringed by certain of our load-reduced dual in-line memory modules (“LRDIMMs”). Each complaint seeks injunctive relief, damages, attorneys’ fees, and costs. On March 31, 2022, Netlist filed a patent infringement complaint against Micron and Micron Semiconductor Germany, GmbH in Dusseldorf Regional Court alleging that two German patents are infringed by certain of our LRDIMMs. The complaint seeks damages, costs, and injunctive relief. On June 10, 2022, Netlist filed a patent infringement complaint against Micron, MSP, and MTEC in the U.S. District Court for the Eastern District of Texas (“E.D. Tex.”) alleging that six U.S. patents are infringed by certain of our memory modules and HBM products. On August 1, 2022, Netlist filed a second patent infringement complaint against the same defendants in E.D. Tex. alleging that one U.S. patent is infringed by certain of our LRDIMMs. On August 15, 2022, Netlist amended the second complaint to assert that two additional U.S. patents are infringed by certain of our LRDIMMs. The complaints in E.D. Tex. seek injunctive relief, damages, and attorneys’ fees.

On August 16, 2022, Sonrai Memory Ltd. filed a patent infringement action against Micron in the U.S. District Court for the Western District of Texas. The complaint alleges that two U.S. patents are infringed by certain SSD and NAND flash products. The complaint seeks damages, attorneys’ fees, and costs.

On January 23, 2023, Besang Inc. filed a patent infringement complaint against Micron in the U.S. District Court for the Eastern District of Texas. The complaint alleges that one U.S. patent is infringed by certain of our 3D NAND and SSD products. The complaint seeks an injunction, damages, attorneys’ fees, and costs.

Among other things, the above lawsuits pertain to substantially all of our DRAM, NAND, and other memory and storage products we manufacture, which account for substantially all of our revenue.

Qimonda

On January 20, 2011, Dr. Michael Jaffé, administrator for Qimonda’s insolvency proceedings, filed suit against Micron and Micron Semiconductor B.V. (“Micron B.V.”), in the District Court of Munich, Civil Chamber. The complaint sought to void, under Section 133 of the German Insolvency Act, a share purchase agreement between Micron B.V. and Qimonda signed in fall 2008, pursuant to which Micron B.V. purchased substantially all of Qimonda’s shares of Inotera (the “Inotera Shares”), representing approximately 18% of Inotera’s outstanding shares at that time, and sought an order requiring us to re-transfer those shares to the Qimonda estate. The complaint also sought, among other things, to recover damages for the alleged value of the joint venture relationship with Inotera and to terminate, under Sections 103 or 133 of the German Insolvency Code, a patent cross-license between us and Qimonda entered into at the same time as the share purchase agreement.

Following a series of hearings with pleadings, arguments, and witnesses on behalf of the Qimonda estate, on March 13, 2014, the court issued judgments: (1) ordering Micron B.V. to pay approximately $1 million in respect of certain Inotera Shares sold in connection with the original share purchase; (2) ordering Micron B.V. to disclose certain information with respect to any Inotera Shares sold by it to third parties; (3) ordering Micron B.V. to disclose the benefits derived by it from ownership of the Inotera Shares, including in particular, any profits distributed on the Inotera Shares and all other benefits; (4) denying Qimonda’s claims against Micron for any damages relating to the joint venture relationship with Inotera; and (5) determining that Qimonda’s obligations under the patent cross-license agreement are canceled. In addition, the court issued interlocutory judgments ordering, among other things: (1) that Micron B.V. transfer to the Qimonda estate the Inotera Shares still owned by Micron B.V. and pay to the Qimonda estate compensation in an amount to be specified for any Inotera Shares sold to third parties; and (2) that Micron B.V. pay the Qimonda estate as compensation an amount to be specified for benefits derived by Micron B.V. from ownership of the Inotera Shares. The interlocutory judgments had no immediate, enforceable effect and Micron, accordingly, was able to continue to operate with full control of the Inotera Shares subject to further developments in the case. Micron and Micron B.V. appealed the judgments to the German Appeals Court, which thereafter appointed an independent expert to perform an evaluation of Dr. Jaffé’s claims that the amount Micron paid for Qimonda was less than fair market value. On March 31, 2020, the expert presented an opinion to the Appeals Court concluding that the amount paid by Micron was within an acceptable range of fair value. On October 5, 2022, the Appeals Court ruled that the relevant issue to be addressed is whether Qimonda's creditors were prejudiced such that the original transaction should be voided.

On May 9, 2023, Micron and Dr. Jaffé reached an agreement to dismiss the case in exchange for a one-time payment by Micron to the Qimonda estate and a waiver of each party's claims. The agreement was formally entered by the Appeals Court in July 2023 and the case was dismissed.

Antitrust Matters

Six cases have been filed against Micron alleging price fixing of DRAM products in the following Canadian courts on the dates indicated: Superior Court of Quebec (April 30, 2018 and May 3, 2018), the Federal Court of Canada (May 2, 2018), the Ontario Superior Court of Justice (May 15, 2018), and the Supreme Court of British Columbia (May 10, 2018). The plaintiffs in these cases are individuals seeking certification of class actions on behalf of direct and indirect purchasers of DRAM in Canada (or regions of Canada) between June 1, 2016 and February 1, 2018.

On May 15, 2018, the Chinese State Administration for Market Regulation ("SAMR") notified Micron that it was investigating potential collusion and other anticompetitive conduct by DRAM suppliers in China. On May 31, 2018, SAMR made unannounced visits to our sales offices in Beijing, Shanghai, and Shenzhen to seek certain information as part of its investigation. We are cooperating with SAMR in its investigation.

Securities Matters

On February 9, 2021, a derivative complaint was filed by a shareholder against Sanjay Mehrotra and other current and former directors of Micron, allegedly on behalf of and for the benefit of Micron, in the U.S. District Court for the District of Delaware alleging violations of securities laws, breaches of fiduciary duties, and other violations of law involving allegedly false and misleading statements about Micron's commitment to diversity and progress in diversifying its workforce, executive leadership, and Board of Directors. The complaint seeks damages, fees, interest, costs, and an order requiring Micron to take various actions to allegedly improve its corporate governance and internal procedures.

Other Matters

In the normal course of business, we are a party to a variety of agreements pursuant to which we may be obligated to indemnify another party. It is not possible to predict the maximum potential amount of future payments under these types of agreements due to the conditional nature of our obligations and the unique facts and circumstances involved in each particular agreement. Historically, our payments under these types of agreements have not had a material adverse effect on our business, results of operations, or financial condition.

Contingency Assessment

We are unable to predict the outcome of any of the matters noted above and cannot make a reasonable estimate of the potential loss or range of possible losses. A determination that our products or manufacturing processes infringe the intellectual property rights of others or entering into a license agreement covering such intellectual property could result in significant liability and/or require us to make material changes to our products and/or manufacturing processes. Any of the foregoing, as well as the resolution of any other legal matter noted above, could have a material adverse effect on our business, results of operations, or financial condition.

Equity

Common Stock Repurchases

Our Board of Directors has authorized the discretionary repurchase of up to $10 billion of our outstanding common stock through open-market purchases, block trades, privately-negotiated transactions, derivative transactions, and/or pursuant to Rule 10b5-1 trading plans. The repurchase authorization has no expiration date, does not obligate us to acquire any common stock, and is subject to market conditions and our ongoing determination of the best use of available cash. We repurchased 8.6 million shares of our common stock for $425 million in 2023 and 35.4 million shares for $2.43 billion in 2022. Through August 31, 2023, we had repurchased an aggregate of $6.89 billion under the authorization. Amounts repurchased are included in treasury stock.

Dividends

In each quarter of 2023, we declared and paid dividends of $126 million ($0.115 per share). On September 27, 2023, our Board of Directors declared a quarterly dividend of $0.115 per share, payable in cash on October 25, 2023, to shareholders of record as of the close of business on October 10, 2023.

Accumulated Other Comprehensive Income (Loss)

Changes in accumulated other comprehensive income (loss) by component for the year ended August 31, 2023 were as follows:

	Gains (Losses) on Derivative Instruments	Unrealized Gains (Losses) on Investments	Pension Liability Adjustments	Cumulative Foreign Currency Translation Adjustment	Total
As of September 1, 2022	$ (538)	$ (47)	$ 25	$ —	$ (560)
Other comprehensive income (loss) before reclassifications	19	18	17	(3)	51
Amount reclassified out of accumulated other comprehensive income (loss)	261	1	(2)	—	260
Tax effects	(46)	(13)	(4)	—	(63)
Other comprehensive income (loss)	234	6	11	(3)	248
As of August 31, 2023	$ (304)	$ (41)	$ 36	$ (3)	$ (312)

Fair Value Measurements

The estimated fair values and carrying values of our outstanding debt instruments were as follows:

	As of August 31, 2023		As of September 1, 2022	
	Fair Value	Carrying Value	Fair Value	Carrying Value
Notes	$ 11,549	$ 12,049	$ 5,472	$ 6,020

The fair values of our debt instruments were estimated based on Level 2 inputs, including the trading price of our notes when available, discounted cash flows, and interest rates based on similar debt issued by parties with credit ratings similar to ours.

Derivative Instruments

	Notional or Contractual Amount	Fair Value of Assets[1]	Fair Value of Liabilities[2]
As of August 31, 2023			
Derivative instruments with hedge accounting designation			
Cash flow currency hedges	$ 3,873	$ 16	$ (180)
Cash flow commodity hedges	331	45	—
Fair value interest rate hedges	900	—	(100)
Derivative instruments without hedge accounting designation			
Non-designated currency hedges	1,839	2	(17)
		$ 63	$ (297)
As of September 1, 2022			
Derivative instruments with hedge accounting designation			
Cash flow currency hedges	$ 5,427	$ —	$ (330)
Cash flow commodity hedges	97	1	(6)
Fair value interest rate hedges	900	—	(91)
Derivative instruments without hedge accounting designation			
Non-designated currency hedges	2,821	7	(13)
		$ 8	$ (440)

(1) *Included in receivables and other noncurrent assets.*
(2) *Included in accounts payable and accrued expenses and other noncurrent liabilities.*

Derivative Instruments with Hedge Accounting Designation

***Cash Flow Hedges*:** We utilize forward and swap contracts that generally mature within two years designated as cash flow hedges to minimize our exposure to changes in currency exchange rates or commodity prices for certain capital expenditures and manufacturing costs. Forward and swap contracts are measured at fair value based on market-based observable inputs including market spot and forward rates, interest rates, and credit-risk spreads (Level 2). We recognized gains from cash flow hedges of $30 million for 2023, and losses of $735 million and $52 million for 2022 and 2021, respectively, in accumulated other comprehensive income (loss). We recognized losses related to amounts excluded from hedge effectiveness testing on our cash flow hedges of $101 million in 2023 in cost of goods sold through an amortization approach. The amounts recognized in 2022 and 2021 were not significant. We reclassified losses of $261 million and $53 million in 2023 and 2022, respectively, and gains of $41 million in 2021, from accumulated other comprehensive income (loss) to earnings, primarily to cost of goods sold. As of August 31, 2023, we expect to reclassify $177 million of pre-tax losses related to cash flow hedges from accumulated other comprehensive income (loss) into earnings in the next 12 months.

***Fair Value Hedges*:** We utilize fixed-to-floating interest rate swaps designated as fair value hedges to minimize certain exposures to changes in the fair value of fixed-rate debt that result from fluctuations in benchmark interest rates. Interest rate swaps are measured at fair value based on market-based observable inputs including interest rates and credit-risk spreads (Level 2). The changes in the fair values of derivatives designated as fair value hedges and the offsetting changes in the underlying fair values of the hedged items are both recognized in earnings. When a derivative is no longer designated as a fair value hedge for any reason, including termination and maturity, the remaining unamortized difference between the carrying value of the hedged item at that time and the face value of the hedged item is amortized to earnings over the remaining life of the hedged item, or immediately if the hedged item has matured or been extinguished. We recognized interest expense of $96 million for changes in the fair value of our interest rate swaps in 2022 and the impact to interest expense was not significant for 2023 or 2021. We also recognized offsetting reductions in interest expense of the same amounts related to the changes in the fair value of the hedged portion of the underlying debt for these periods.

Derivative Instruments without Hedge Accounting Designation

***Currency Derivatives*:** We generally utilize a rolling hedge strategy with currency forward contracts that mature within three months to hedge our exposures of monetary assets and liabilities from changes in currency exchange rates. At the end of each reporting period, monetary assets and liabilities denominated in currencies other than the U.S. dollar are remeasured into U.S. dollars and the associated outstanding forward contracts are marked to market. Currency forward contracts are valued at fair values based on the middle of bid and ask prices of dealers or exchange quotations (Level 2). Realized and unrealized gains and losses on derivative instruments without hedge accounting designation as well as the changes in the underlying monetary assets and liabilities from changes in currency exchange rates are included in other non-operating income (expense), net. The amounts recognized for derivative instruments without hedge accounting designation were not significant for the periods presented. We do not use derivative instruments for speculative purposes.

Derivative Counterparty Credit Risk and Master Netting Arrangements

Our derivative instruments expose us to credit risk to the extent counterparties may be unable to meet the terms of the contracts. Our maximum exposure to loss due to credit risk if counterparties fail completely to perform according to the terms of the contracts would generally equal the fair value of assets for these contracts as listed in the tables above. We seek to mitigate such risk by limiting our counterparties to major financial institutions and by spreading risk across multiple financial institutions. As of August 31, 2023 and September 1, 2022, amounts netted under our master netting arrangements were not significant.

Equity Plans

As of August 31, 2023, 95 million shares of our common stock were available for future awards under our equity plans, including 14 million shares approved for issuance under our employee stock purchase plan (“ESPP”).

Restricted Stock and Restricted Stock Units (“Restricted Stock Awards”)

As of August 31, 2023, there were 29 million shares of Restricted Stock Awards outstanding, 26 million of which contained only service conditions. For service-based Restricted Stock Awards granted through October 2021, restrictions generally lapse in one-fourth or one-third increments during each year of employment after the grant date. For service-based Restricted Stock Awards granted beginning in November 2021, restrictions generally lapse on 25% or 33% of the units granted after the first year and on 6.25% or 8.33% each quarter thereafter over the remaining three or two years of employment. Restrictions generally lapse on Restricted Stock with performance or market conditions as conditions are met over a 3-year period. At the end of the performance period, the number of actual shares to be awarded will vary between 0% and 200% of target amounts, depending upon the achievement level. In 2022, our Board of Directors approved dividend equivalent rights for unvested restricted stock units awarded on or after October 13, 2021.

Restricted Stock Awards activity for 2023 is summarized as follows:

	Number of Shares	Weighted-Average Grant Date Fair Value Per Share
Outstanding as of September 1, 2022	23	$ 60.93
Granted	17	55.99
Restrictions lapsed	(9)	58.23
Canceled	(2)	58.00
Outstanding as of August 31, 2023	29	59.11

For the year ended	2023	2022	2021
Restricted stock award shares granted	17	13	11
Weighted-average grant-date fair value per share	$ 55.99	$ 70.81	$ 53.58
Aggregate vesting-date fair value of shares vested	$ 514	$ 498	$ 385

Employee Stock Purchase Plan ("ESPP")

Our ESPP is offered to substantially all employees and permitted eligible employees to purchase shares of our common stock through payroll deductions of up to 10% of their eligible compensation, subject to certain limitations prior to August 2021. Beginning in August 2021, employees are permitted to deduct up to 15% of their eligible compensation to purchase shares under the ESPP. The purchase price of the shares under the ESPP equals 85% of the lower of the fair market value of our common stock on either the first or last day of each six-month offering period. Compensation expense is calculated as of the beginning of the offering period as the fair value of the employees' purchase rights utilizing the Black-Scholes option valuation model and is recognized over the offering period. Grant-date fair value and assumptions used in the Black-Scholes option valuation model were as follows:

For the year ended	2023	2022	2021
Weighted-average grant-date fair value per share	$ 17.06	$ 18.87	$ 20.71
Average expected life in years	0.5	0.5	0.5
Weighted-average expected volatility (based on implied volatility)	37 %	43 %	41 %
Weighted-average risk-free interest rate	5.1 %	2.0 %	0.1 %
Expected dividend yield	0.7 %	0.6 %	0.3 %

Under the ESPP, employees purchased 5 million, 4 million, and 3 million shares of common stock in 2023, 2022, and 2021, respectively, at a per share weighted average price of $51.93, $58.52, and $51.42, respectively.

Stock Options

As of August 31, 2023, stock options of 2 million shares were outstanding, all of which were fully exercisable. Stock options expire 8 years from the date of grant. We did not grant any stock options in 2023, 2022, or 2021. Stock options of 1 million shares were exercised in 2023. The total intrinsic value for options exercised was $30 million, $54 million, and $143 million in 2023, 2022, and 2021, respectively.

Stock-based Compensation Expense

For the year ended	2023	2022	2021
Stock-based compensation expense by caption			
Research and development	$ 226	$ 175	$ 110
Cost of goods sold	201	193	186
Selling, general, and administrative	137	133	99
Restructure	(7)	(5)	—
	$ 557	$ 496	$ 395
Stock-based compensation expense by type of award			
Restricted stock awards	$ 488	$ 429	$ 333
ESPP	69	66	52
Stock options	—	1	10
	$ 557	$ 496	$ 395

Income tax benefits related to the tax deductions for share-based awards are recognized only upon the settlement of the related share-based awards. Income tax benefits for share-based awards were $68 million, $77 million, and $83 million for 2023, 2022, and 2021, respectively. Stock-based compensation expense of $88 million and $48 million was capitalized and remained in inventory as of August 31, 2023 and September 1, 2022, respectively. As of August 31, 2023, $1.26 billion of total unrecognized compensation costs for unvested awards, before the effect of any future forfeitures, was expected to be recognized through the fourth quarter of 2027, resulting in a weighted-average period of 1.3 years.

Employee Benefit Plans

We have employee retirement plans at our U.S. and international sites. Details of significant plans are as follows:

Employee Savings Plan for U.S. Employees

We have a 401(k) retirement plan under which U.S. employees may contribute up to 75% of their eligible pay, subject to Internal Revenue Service annual contribution limits, to various savings alternatives, none of which include direct investment in our stock. We match in cash eligible contributions from employees up to 5% of the employee's annual eligible earnings. Contribution expense for the 401(k) plan was $59 million, $66 million, and $77 million in 2023, 2022, and 2021, respectively.

Retirement Plans

We have pension plans available to employees at various foreign sites. As of August 31, 2023, the projected benefit obligations of our plans were $175 million and plan assets were $232 million. As of September 1, 2022, the projected benefit obligations of our plans were $186 million and plan assets were $221 million. Pension expense was not material for 2023, 2022, or 2021.

Government Incentives

We receive incentives from governmental entities primarily in India, Japan, Singapore, Taiwan, and the United States principally in the form of cash grants and tax credits. These incentives primarily relate to capital expenditures, have initial terms ranging from one year to 15 years, and may be subject to reimbursement if certain conditions are not met or maintained. The conditions attached to these incentives require us to incur expenditures related to the construction of new manufacturing facilities, the purchase and installation of specialized tools and equipment, R&D expenditures, and/or maintain certain levels of fixed asset investment or employee headcount during the incentive terms.

The line items on the balance sheet affected by government incentives were as follows:

As of	August 31, 2023
Receivables	$ 105
Other noncurrent assets	179
Other current liabilities	11
Noncurrent unearned government incentives	727

As of August 31, 2023, we had aggregate commitments from various governmental entities of up to $2 billion to be received through 2033 (in addition to the receivables and other noncurrent assets in the table above), subject to achievement of certain performance conditions. We also receive a 25% investment tax credit on qualified investments in U.S. semiconductor manufacturing under the CHIPS Act. Subsequent to August 31, 2023, we finalized an incentive arrangement under which we will receive additional grants of up to $1.3 billion.

Government incentives related to capital expenditures have reduced property, plant and equipment by $1.57 billion as of August 31, 2023, of which $584 million pertained to 2023 expenditures.

In 2023, operating income (loss) benefited by $318 million (approximately 93% in COGS and 7% in R&D) from government incentives recognized as a reduction of expense, primarily in the form of reduced depreciation expense.

Revenue

Revenue is primarily recognized at a point in time when control of the promised goods is transferred to our customers in an amount that reflects the consideration we expect to be entitled to in exchange for those goods. Substantially all contracts with our customers are short-term in duration at fixed, negotiated prices with payment generally due shortly after delivery. From time to time, we have contracts with initial terms that include performance obligations that extend beyond one year. As of August 31, 2023, our future performance obligations beyond one year were not significant.

As of August 31, 2023 and September 1, 2022, other current liabilities included $453 million and $1.26 billion, respectively, for estimates of consideration payable to customers including estimates for pricing adjustments and returns.

In 2023, we received an aggregate of $228 million from settlements of insurance claims involving a power disruption in 2022 and an operational disruption in 2017, of which $186 million was for business interruption and recognized in revenue.

Revenue by Technology

For the year ended	2023	2022	2021
DRAM	$ 10,978	$ 22,386	$ 20,039
NAND	4,206	7,811	7,007
Other (primarily NOR)	356	561	659
	$ 15,540	$ 30,758	$ 27,705

See “Segment and Other Information” for disclosure of disaggregated revenue by market segment.

Restructure and Asset Impairments

For the year ended	2023	2022	2021
Employee severance	$ 163	$ —	$ 3
Asset impairments and other asset-related costs	14	63	478
Other	(6)	(15)	7
	$ 171	$ 48	$ 488

In 2023, we initiated the 2023 Restructure Plan in response to challenging industry conditions. Under the 2023 Restructure Plan, we expect our headcount reduction to approach 15% by the end of calendar 2023 through a combination of voluntary attrition and personnel reductions. In connection with the plan, we incurred restructure charges of $171 million in 2023, primarily related to employee severance costs. The plan was substantially completed in the third quarter of 2023. As of August 31, 2023, we had paid $167 million in 2023 in connection with the 2023 Restructure Plan and the remaining liability was $4 million.

Restructure and asset impairments for 2022 and 2021 are primarily related to the sale of our Lehi, Utah facility. See “Lehi, Utah Fab and 3D XPoint.”

Other Operating (Income) Expense, Net

For the year ended	2023	2022	2021
Goodwill impairment	$ 101	$ —	$ —
Litigation settlement	68	—	—
Patent license charges	—	—	128
(Gain) loss on disposition of property, plant, and equipment	(54)	(41)	(24)
Other	9	7	(9)
	$ 124	$ (34)	$ 95

Other Non-Operating Income (Expense), Net

For the year ended	2023	2022	2021
Gain (loss) on investments	$ (8)	$ 26	$ 82
Loss on debt repurchases and conversions	—	(83)	(1)
Other	15	19	—
	$ 7	$ (38)	$ 81

Income Taxes

Our income tax (provision) benefit consisted of the following:

For the year ended	2023	2022	2021
Income (loss) before income taxes and equity in net income (loss) of equity method investees			
U.S.	$ 235	$ 112	$ (211)
Foreign	(5,893)	9,459	6,429
	$ (5,658)	$ 9,571	$ 6,218
Income tax (provision) benefit			
Current			
U.S. federal	$ (5)	$ (65)	$ (42)
State	(1)	(1)	(1)
Foreign	(178)	(528)	(370)
	(184)	(594)	(413)
Deferred			
U.S. federal	(84)	(166)	(9)
State	—	(225)	28
Foreign	91	97	—
	7	(294)	19
Income tax (provision) benefit	$ (177)	$ (888)	$ (394)

The table below reconciles our tax (provision) benefit based on the U.S. federal statutory rate to our effective rate:

For the year ended	2023		2022		2021	
U.S. federal income tax (provision) benefit at statutory rate	$ 1,188	21.0 %	$ (2,010)	21.0 %	$ (1,306)	21.0 %
U.S. tax on foreign operations	6	0.1 %	(322)	3.4 %	(226)	3.6 %
Change in valuation allowance	(50)	(0.9)%	(241)	2.5 %	54	(0.9)%
Change in unrecognized tax benefits	(30)	(0.5)%	(67)	0.7 %	(238)	3.8 %
Foreign tax rate differential	(1,285)	(22.8)%	1,601	(16.7)%	951	(15.4)%
Research and development tax credits	43	0.8 %	66	(0.7)%	123	(2.0)%
State taxes, net of federal benefit	37	0.7 %	—	— %	59	(0.9)%
Debt premium deductions	—	— %	—	— %	130	(2.1)%
Other	(86)	(1.5)%	85	(0.9)%	59	(0.8)%
Income tax (provision) benefit	$ (177)	(3.1)%	$ (888)	9.3 %	$ (394)	6.3 %

We operate in a number of jurisdictions outside the United States, including Singapore, where we have tax incentive arrangements. These incentives expire, in whole or in part, at various dates through 2034 and are conditional, in part, upon meeting certain business operations and employment thresholds. As a result of a loss before taxes and geographic mix of income, the benefit from tax incentive arrangements was not material for 2023. These arrangements reduced our tax provision by $1.12 billion (benefiting our diluted earnings per share by $1.00) for 2022 and by $758 million ($0.66 per diluted share) for 2021.

As of August 31, 2023, certain non-U.S. subsidiaries had cumulative undistributed earnings of $4.28 billion that were deemed to be indefinitely reinvested. A provision has not been recognized to the extent that distributions from such subsidiaries are subject to additional foreign withholding or state income tax. Determination of the amount of unrecognized deferred tax liabilities related to investments in these foreign subsidiaries is not practicable.

Deferred income taxes reflect the net tax effects of temporary differences between the bases of assets and liabilities for financial reporting and income tax purposes as well as carryforwards. Deferred tax assets and liabilities consist of the following:

As of	August 31, 2023	September 1, 2022
Deferred tax assets		
Net operating loss and tax credit carryforwards	$ 1,112	$ 796
Accrued salaries, wages, and benefits	39	157
Operating lease liabilities	135	138
Inventories	52	77
Property, plant, and equipment	—	44
Other	75	142
Gross deferred tax assets	1,413	1,354
Less valuation allowance	(528)	(471)
Deferred tax assets, net of valuation allowance	885	883
Deferred tax liabilities		
Right-of-use assets	(115)	(126)
Property, plant, and equipment	(31)	—
Other	(100)	(68)
Deferred tax liabilities	(246)	(194)
Net deferred tax assets	$ 639	$ 689
Reported as		
Deferred tax assets	$ 756	$ 702
Deferred tax liabilities (included in other noncurrent liabilities)	(117)	(13)
Net deferred tax assets	$ 639	$ 689

We assess positive and negative evidence for each jurisdiction to determine whether it is more likely than not that existing deferred tax assets will be realized. As of August 31, 2023, and September 1, 2022, we had a valuation allowance of $528 million and $471 million, respectively, against our net deferred tax assets, primarily related to carryforwards in U.S. states and Malaysia. Changes in 2023 in the valuation allowance were due to adjustments based on management's assessment of the realizability of tax credits, allowances and net operating losses based on a level that is more likely than not to be realized.

As of August 31, 2023, our net operating loss carryforward amounts and expiration periods, as reported to tax authorities, were as follows:

Year of Expiration	Singapore	Malaysia	State	Japan	Other	Total
2024 - 2028	$ —	$ —	$ 47	$ 336	$ 25	$ 408
2029 - 2033	—	—	348	321	109	778
2034 - 2038	—	—	237	—	—	237
2039 - 2043	—	—	183	—	—	183
Indefinite	1,688	1,025	60	—	202	2,975
	$ 1,688	$ 1,025	$ 875	$ 657	$ 336	$ 4,581

As of August 31, 2023, our federal and state tax credit carryforward amounts and expiration periods, as reported to tax authorities, were as follows:

Year of Tax Credit Expiration	U.S. Federal	State	Total
2024 - 2028	$ —	$ 51	$ 51
2029 - 2033	—	120	120
2034 - 2038	—	137	137
2039 - 2043	306	5	311
Indefinite	—	131	131
	$ 306	$ 444	$ 750

Below is a reconciliation of the beginning and ending amount of our unrecognized tax benefits:

For the year ended	2023	2022	2021
Beginning unrecognized tax benefits	$ 731	$ 660	$ 411
Increases related to tax positions from prior years	2	14	2
Increases related to prior year tax positions taken in current year	27	—	—
Increases related to tax positions taken in current year	17	80	260
Decreases related to tax positions from prior years	(33)	(23)	(13)
Ending unrecognized tax benefits	$ 744	$ 731	$ 660

As of August 31, 2023, gross unrecognized tax benefits were $744 million, which would have an impact of approximately $581 million on our effective tax rate in the future, if recognized. Amounts accrued for interest and penalties related to uncertain tax positions were not significant for any period presented. The resolution of tax audits or expiration of statute of limitations could also reduce our unrecognized tax benefits. Although the timing of final resolution is uncertain, the estimated potential reduction in our unrecognized tax benefits in the next 12 months would not be significant.

We and our subsidiaries file income tax returns with the U.S. federal government, various U.S. states, and various foreign jurisdictions throughout the world. We regularly engage in discussions and negotiations with tax authorities regarding tax matters, including transfer pricing, and we continue to defend any and all such claims presented. Our U.S. federal and state tax returns remain open to examination for 2018 through 2023. We are currently under audit by the Internal Revenue Service for our 2018 and 2019 tax years. In addition, tax returns that remain open to examination in Singapore, Taiwan and Japan range from the years 2014 to 2023. We believe that adequate amounts of taxes and related interest and penalties have been provided, and any adjustments as a result of examinations are not expected to materially adversely affect our business, results of operations, or financial condition.

Earnings Per Share

For the year ended	2023	2022	2021
Net income (loss) – Basic and Diluted	$ (5,833)	$ 8,687	$ 5,861
Weighted-average common shares outstanding – Basic	1,093	1,112	1,120
Dilutive effect of equity plans and convertible notes	—	10	21
Weighted-average common shares outstanding – Diluted	1,093	1,122	1,141
Earnings (loss) per share			
Basic	$ (5.34)	$ 7.81	$ 5.23
Diluted	(5.34)	7.75	5.14

Antidilutive potential common shares excluded from the computation of diluted earnings per share, that could dilute basic earnings per share in the future, were as follows at the end of the periods shown:

For the year ended	2023	2022	2021
Equity plans	33	5	2

Segment and Other Information

Segment information reported herein is consistent with how it is reviewed and evaluated by our chief operating decision maker. We have the following four business units, which are our reportable segments:

***Compute and Networking Business Unit ("CNBU")*:** Includes memory products and solutions sold into client, cloud server, enterprise, graphics, and networking markets.
***Mobile Business Unit ("MBU")*:** Includes memory and storage products sold into smartphone and other mobile-device markets.
***Embedded Business Unit ("EBU")*:** Includes memory and storage products and solutions sold into automotive, industrial, and consumer markets.
***Storage Business Unit ("SBU")*:** Includes SSDs and component-level solutions sold into enterprise and cloud, client, and consumer storage markets.

Certain operating expenses directly associated with the activities of a specific segment are charged to that segment. Other indirect operating income and expenses are generally allocated to segments based on their respective percentage of cost of goods sold or forecasted wafer production. We do not identify or report internally our assets (other than goodwill) or capital expenditures by segment, nor do we allocate gains and losses from equity method investments, interest, other non-operating income or expense items, or taxes to segments.

For the year ended	2023	2022	2021
Revenue			
CNBU	$ 5,710	$ 13,693	$ 12,280
MBU	3,630	7,260	7,203
EBU	3,637	5,235	4,209
SBU	2,553	4,553	3,973
All Other	10	17	40
	$ 15,540	$ 30,758	$ 27,705
Operating income (loss)			
CNBU	$ (585)	$ 5,844	$ 4,295
MBU	(1,750)	2,160	2,173
EBU	382	1,752	1,006
SBU	(1,887)	513	173
All Other	8	12	20
	(3,832)	10,281	7,667
Unallocated			
Provision to write down inventories to net realizable value	(1,831)	—	—
Lower costs from sale of inventory written down in prior periods	844	—	—
Stock-based compensation	(564)	(501)	(395)
Inventory accounting policy change to FIFO	—	—	(133)
Change in inventory cost absorption	—	—	(160)
3D XPoint inventory write-down	—	—	(49)
Restructure and asset impairments	(171)	(48)	(488)
Goodwill impairment	(101)	—	—
Litigation settlement	(68)	—	—
Patent license charges	—	—	(128)
Other	(22)	(30)	(31)
	(1,913)	(579)	(1,384)
Operating income (loss)	$ (5,745)	$ 9,702	$ 6,283

Depreciation and amortization expense included in operating income (loss) was as follows:

For the year ended	2023	2022	2021
CNBU	$ 2,512	$ 2,766	$ 2,497
MBU	2,149	1,725	1,553
EBU	1,324	1,280	1,028
SBU	1,751	1,323	1,101
All Other	1	2	8
Unallocated	19	20	27
	$ 7,756	$ 7,116	$ 6,214

Certain Concentrations

Revenue by market segment as an approximate percent of total revenue is presented in the table below:

For the year ended	2023	2022	2021
Automotive, industrial, and consumer	25 %	15 %	15 %
Mobile	25 %	25 %	25 %
Client and graphics	15 %	20 %	20 %
Enterprise and cloud server	15 %	20 %	20 %
SSDs and other storage	15 %	15 %	15 %

No customer accounted for 10% or more of total revenue in 2023. Revenue from Kingston Technology Company, Inc. was 12% of total revenue in 2022 and revenue from WPG Holdings Limited was 11% and 13% of total revenue in 2022 and 2021, respectively. Sales to Kingston were primarily included in our CNBU and SBU segments and sales to WPG were primarily included in our MBU, CNBU, and EBU segments.

We generally have multiple sources of supply for our raw materials and production equipment; however, only a limited number of suppliers are capable of delivering certain raw materials and production equipment that meet our standards and, in some cases, materials or production equipment are provided by a single supplier.

Financial instruments that potentially subject us to concentrations of credit risk consist principally of cash, money market accounts, certificates of deposit, fixed-rate debt securities, trade receivables, share repurchase, and derivative contracts. We invest through high-credit-quality financial institutions and, by policy, generally limit the concentration of credit exposure by restricting investments with any single obligor and monitoring credit risk of bank counterparties on an ongoing basis. A concentration of credit risk may exist with respect to receivables of certain customers. We perform ongoing credit evaluations of customers worldwide and generally do not require collateral from our customers. Historically, we have not experienced material losses on receivables. A concentration of risk may also exist with respect to our foreign currency hedges as the number of counterparties to our hedges is limited and the notional amounts are relatively large. We seek to mitigate such risk by limiting our counterparties to major financial institutions and through entering into master netting arrangements.

Geographic Information

Revenue based on the geographic location of our customers' headquarters was as follows:

For the year ended	2023	2022	2021
United States	$ 7,805	$ 16,026	$ 12,155
Taiwan	2,697	6,185	6,606
Mainland China (excluding Hong Kong)	2,181	3,311	2,456
Japan	987	1,696	1,652
Other Asia Pacific	752	1,223	1,420
Europe	682	505	573
Hong Kong	340	1,665	2,582
Other	96	147	261
	$ 15,540	$ 30,758	$ 27,705

Long-lived assets by geographic area consisted of property, plant, and equipment and operating lease right-of-use assets and were as follows:

As of	August 31, 2023	September 1, 2022
Taiwan	$ 12,926	$ 13,143
Singapore	11,283	12,045
Japan	7,323	7,113
United States	5,196	5,155
Malaysia	1,124	994
China	395	440
Other	347	337
	$ 38,594	$ 39,227

Report of Independent Registered Public Accounting Firm

To the Board of Directors and Shareholders of Micron Technology, Inc.

Opinions on the Financial Statements and Internal Control over Financial Reporting

We have audited the accompanying consolidated balance sheets of Micron Technology, Inc. and its subsidiaries (the "Company") as of August 31, 2023 and September 1, 2022, and the related consolidated statements of operations, of comprehensive income (loss), of changes in equity and of cash flows for each of the three years in the period ended August 31, 2023, including the related notes and schedule of valuation and qualifying accounts for each of the three years in the period ended August 31, 2023 appearing under Item 15 (collectively referred to as the "consolidated financial statements"). We also have audited the Company's internal control over financial reporting as of August 31, 2023, based on criteria established in *Internal Control - Integrated Framework* (2013) issued by the Committee of Sponsoring Organizations of the Treadway Commission (COSO).

In our opinion, the consolidated financial statements referred to above present fairly, in all material respects, the financial position of the Company as of August 31, 2023 and September 1, 2022**,** and the results of its operations and its cash flows for each of the three years in the period ended August 31, 2023 in conformity with accounting principles generally accepted in the United States of America. Also in our opinion, the Company maintained, in all material respects, effective internal control over financial reporting as of August 31, 2023, based on criteria established in *Internal Control - Integrated Framework* (2013) issued by the COSO.

Change in Accounting Principle

As discussed in the Significant Accounting Policies and Inventories notes to the consolidated financial statements, the Company changed the manner in which it accounts for inventory costing from the average cost inventory accounting method to the first-in, first-out inventory accounting method in 2021.

Basis for Opinions

The Company's management is responsible for these consolidated financial statements, for maintaining effective internal control over financial reporting, and for its assessment of the effectiveness of internal control over financial reporting, included in Management's Report on Internal Control over Financial Reporting appearing under Item 9A. Our responsibility is to express opinions on the Company's consolidated financial statements and on the Company's internal control over financial reporting based on our audits. We are a public accounting firm registered with the Public Company Accounting Oversight Board (United States) (PCAOB) and are required to be independent with respect to the Company in accordance with the U.S. federal securities laws and the applicable rules and regulations of the Securities and Exchange Commission and the PCAOB.

We conducted our audits in accordance with the standards of the PCAOB. Those standards require that we plan and perform the audits to obtain reasonable assurance about whether the consolidated financial statements are free of material misstatement, whether due to error or fraud, and whether effective internal control over financial reporting was maintained in all material respects.

Our audits of the consolidated financial statements included performing procedures to assess the risks of material misstatement of the consolidated financial statements, whether due to error or fraud, and performing procedures that respond to those risks. Such procedures included examining, on a test basis, evidence regarding the amounts and disclosures in the consolidated financial statements. Our audits also included evaluating the accounting principles used and significant estimates made by management, as well as evaluating the overall presentation of the consolidated financial statements. Our audit of internal control over financial reporting included obtaining an understanding of internal control over financial reporting, assessing the risk that a material weakness exists, and testing and evaluating the design and operating effectiveness of internal control based on the assessed risk. Our audits also included performing such other procedures as we considered necessary in the circumstances. We believe that our audits provide a reasonable basis for our opinions.

Definition and Limitations of Internal Control over Financial Reporting

A company's internal control over financial reporting is a process designed to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with generally accepted accounting principles. A company's internal control over financial reporting includes those policies and procedures that (i) pertain to the maintenance of records that, in reasonable detail, accurately and fairly reflect the transactions and dispositions of the assets of the company; (ii) provide reasonable assurance that transactions are recorded as necessary to permit preparation of financial statements in accordance with generally accepted accounting principles, and that receipts and expenditures of the company are being made only in accordance with authorizations of management and directors of the company; and (iii) provide reasonable assurance regarding prevention or timely detection of unauthorized acquisition, use, or disposition of the company's assets that could have a material effect on the financial statements.

Because of its inherent limitations, internal control over financial reporting may not prevent or detect misstatements. Also, projections of any evaluation of effectiveness to future periods are subject to the risk that controls may become inadequate because of changes in conditions, or that the degree of compliance with the policies or procedures may deteriorate.

Critical Audit Matters

The critical audit matter communicated below is a matter arising from the current period audit of the consolidated financial statements that was communicated or required to be communicated to the audit committee and that (i) relates to accounts or disclosures that are material to the consolidated financial statements and (ii) involved our especially challenging, subjective, or complex judgments. The communication of critical audit matters does not alter in any way our opinion on the consolidated financial statements, taken as a whole, and we are not, by communicating the critical audit matter below, providing a separate opinion on the critical audit matter or on the accounts or disclosures to which it relates.

Net Realizable Value of Finished Goods and Work in Process Inventories

As described in the Inventories note to the consolidated financial statements, as of August 31, 2023, the Company had net finished goods and work in process inventories totaling $7.7 billion. As disclosed by management, determining the net realizable value of the Company's finished goods and work in process inventories involves significant judgments, including projecting future average selling prices, future sales volumes, and future cost per part. The memory and storage industry environment deteriorated sharply in the fourth quarter of 2022 and throughout 2023 due to weak demand in many end markets combined with global and macroeconomic challenges and lower demand resulting from customer actions to reduce elevated inventory levels. This led to significant reductions in average selling prices for both DRAM and NAND, resulting in declines in revenue across all of the Company's business segments and nearly all end markets. The Company recorded charges of $1.83 billion to cost of goods sold to write down the carrying value of work in process and finished goods inventories to their estimated net realizable value.

The principal considerations for our determination that performing procedures relating to the net realizable value of finished goods and work in process inventories is a critical audit matter are (i) the significant judgment by management in determining the net realizable value of finished goods and work in process inventories and (ii) a high degree of auditor judgment, subjectivity, and effort in performing procedures and evaluating management's significant assumptions related to future average selling prices and future cost per part.

Addressing the matter involved performing procedures and evaluating audit evidence in connection with forming our overall opinion on the consolidated financial statements. These procedures included testing the effectiveness of controls relating to management's determination of the net realizable value of finished goods and work in process inventories, including controls over significant assumptions and data utilized. These procedures also included, among others (i) testing management's process for determining the net realizable value of finished goods and work in process inventories; (ii) evaluating the appropriateness of management's methodology; (iii) testing the completeness and accuracy of underlying data used in determining the net realizable value; and (iv) evaluating the reasonableness of management's significant assumptions related to future average selling prices and future cost per part. Evaluating management's assumption related to future average selling prices for certain products involved evaluating whether the assumption used by management was reasonable considering (i) current and past results, including recent sales; (ii) the consistency with external market, industry data or current contract prices; (iii) a comparison of the prior year estimates to actual results in the current fiscal year; and (iv) whether the assumption was consistent with evidence obtained in other areas of the audit. Evaluating management's assumption related to future cost per part for certain products involved evaluating whether the assumption used by management was reasonable considering (i) current and past results; (ii) a comparison of the prior year estimates to actual results in the current fiscal year; and (iii) whether the assumption was consistent with evidence obtained in other areas of the audit.

/s/ PricewaterhouseCoopers LLP

San Jose, California
October 6, 2023

We have served as the Company's auditor since 1984.

ITEM 9. CHANGES IN AND DISAGREEMENTS WITH ACCOUNTANTS ON ACCOUNTING AND FINANCIAL DISCLOSURE

None.

ITEM 9A. CONTROLS AND PROCEDURES

An evaluation was carried out under the supervision and with the participation of our management, including our principal executive officer and principal financial officer, of the effectiveness of the design and operation of our disclosure controls and procedures (as defined in Rules 13a-15(e) and 15d-15(e) under the Securities Exchange Act of 1934, as amended (the "Exchange Act")) as of the end of the period covered by this report. Based upon that evaluation, the principal executive officer and principal financial officer concluded that those disclosure controls and procedures were effective to ensure that information required to be disclosed by us in the reports that we file or submit under the Exchange Act are recorded, processed, summarized, and reported within the time periods specified in the SEC's rules and forms and that such information is accumulated and communicated to our management, including the principal executive officer and principal financial officer, to allow timely decisions regarding disclosure.

During the fourth quarter of 2023, there were no changes in our internal control over financial reporting that have materially affected, or are reasonably likely to materially affect, our internal control over financial reporting.

Management's Report on Internal Control Over Financial Reporting

Our management is responsible for establishing and maintaining adequate internal control over financial reporting. Internal control over financial reporting is a process designed to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with accounting principles generally accepted in the United States of America. Our internal control over financial reporting includes those policies and procedures that (i) pertain to the maintenance of records that in reasonable detail accurately reflect the transactions and dispositions of our assets; (ii) provide reasonable assurance that transactions are recorded as necessary to permit preparation of financial statements in accordance with generally accepted accounting principles, and that our receipts and expenditures are being made only in accordance with authorizations of our management and directors; and (iii) provide reasonable assurance regarding prevention or timely detection of unauthorized acquisition, use, or disposition of our assets that could have a material effect on our financial statements.

Because of its inherent limitations, internal control over financial reporting may not prevent or detect misstatements. Also, projections of any evaluation of effectiveness to future periods are subject to the risk that controls may become inadequate because of changes in conditions or that the degree of compliance with the policies or procedures may deteriorate.

Management conducted an evaluation of the effectiveness of our internal control over financial reporting based on the framework in Internal Control – Integrated Framework (2013) issued by the Committee of Sponsoring Organizations of the Treadway Commission. Based on this evaluation, management concluded that our internal control over financial reporting was effective as of August 31, 2023. The effectiveness of our internal control over financial reporting as of August 31, 2023 has been audited by PricewaterhouseCoopers LLP, an independent registered public accounting firm, as stated in their report, which is included in Part II, Item 8, of this Form 10-K.

ITEM 9B. OTHER INFORMATION

Securities Trading Plans of Directors and Executive Officers

The following director and officer, as defined in Rule 16a-1(f) of the Exchange Act, adopted a “Rule 10b5-1 trading arrangement,” as defined in Item 408 of Regulation S-K, as follows:

On May 15, 2023, Sanjay Mehrotra, our President, Chief Executive Officer and Director, adopted a Rule 10b5-1 trading arrangement providing for the sale of an aggregate of up to 812,284 shares of our common stock, including up to 612,284 shares subject to outstanding stock options, which were granted in calendar 2017 and would otherwise expire in calendar 2025. The remaining shares subject to the trading arrangement are shares acquired by Mr. Mehrotra pursuant to our Restricted Stock Awards. The trading arrangement is intended to satisfy the affirmative defense in Rule 10b5-1(c). The first date that sales of any shares were permitted to be sold under the trading arrangement was August 14, 2023, and subsequent sales under the trading arrangement may occur on a regular basis for the duration of the trading arrangement until May 8, 2025, or earlier if all transactions under the trading arrangement are completed.

No other officers or directors, as defined in Rule 16a-1(f), adopted and/or terminated a “Rule 10b5-1 trading arrangement” or a “non-Rule 10b5-1 trading arrangement,” as defined in Item 408 of Regulation S-K, during the last fiscal quarter.

ITEM 9C. DISCLOSURE REGARDING FOREIGN JURISDICTIONS THAT PREVENT INSPECTIONS

Not applicable.

PART III

ITEM 10. DIRECTORS, EXECUTIVE OFFICERS, AND CORPORATE GOVERNANCE

ITEM 11. EXECUTIVE COMPENSATION

ITEM 12. SECURITY OWNERSHIP OF CERTAIN BENEFICIAL OWNERS AND MANAGEMENT AND RELATED STOCKHOLDER MATTERS

ITEM 13. CERTAIN RELATIONSHIPS AND RELATED TRANSACTIONS, AND DIRECTOR INDEPENDENCE

ITEM 14. PRINCIPAL ACCOUNTANT FEES AND SERVICES

Certain information concerning our executive officers is included under the caption, “Information About Our Executive Officers” in Part I, Item 1 of this report. Other information required by Items 10, 11, 12, 13, and 14 will be contained in our 2023 Proxy Statement which will be filed with the SEC within 120 days after August 31, 2023 and is incorporated herein by reference.

PART IV

ITEM 15. EXHIBITS AND FINANCIAL STATEMENT SCHEDULE

(a) The following documents are filed as part of this report:

1 Financial Statements: See our consolidated financial statements under Item 8.

2 Financial Statement Schedule:
See “Schedule II – Valuation and Qualifying Accounts” within Item 15 below.

Certain Financial Statement Schedules have been omitted since they are either not required, not applicable, or the information is otherwise included.

3 Exhibits. See “Index to Exhibits” within Item 15 below.

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SCHEDULE II

VALUATION AND QUALIFYING ACCOUNTS
(In millions)

	Balance at Beginning of Year	Charged (Credited) to Income Tax Provision	Currency Translation and Charges to Other Accounts	Balance at End of Year
Deferred Tax Asset Valuation Allowance				
Year ended August 31, 2023	$ 471	$ 58	$ (1)	$ 528
Year ended September 1, 2022	233	241	(3)	471
Year ended September 2, 2021	294	(54)	(7)	233

Index to Exhibits

Exhibit Number	Description of Exhibit	Filed Herewith	Form	Period Ending	Exhibit/ Appendix	Filing Date
3.1	Restated Certificate of Incorporation of the Registrant		8-K		99.2	1/26/15
3.2	Bylaws of the Registrant, Amended and Restated		8-K		3.1	2/16/21
4.1	Indenture, dated as of February 6, 2019, by and between Micron Technology, Inc. and U.S. Bank National Association, as Trustee		8-K		4.1	2/6/19
4.2	First Supplemental Indenture, dated as of February 6, 2019, by and between Micron Technology, Inc. and U.S. Bank National Association, as Trustee		8-K		4.2	2/6/19
4.3	Form of Note for Micron Technology, Inc.'s 4.975% Senior Notes due 2026 (included in Exhibit 4.2)		8-K		4.4	2/6/19
4.4	Form of Note for Micron Technology, Inc.'s 5.327% Senior Notes due 2029 (included in Exhibit 4.2)		8-K		4.5	2/6/19
4.5	Second Supplemental Indenture, dated as of July 12, 2019, by and between Micron Technology, Inc. and U.S. Bank National Association, as Trustee		8-K		4.2	7/12/19
4.6	Form of Note for Micron Technology, Inc.'s 4.185% Senior Notes due 2027 (included in Exhibit 4.5)		8-K		4.3	7/12/19
4.7	Form of Note for Micron Technology, Inc.'s 4.663% Senior Notes due 2030 (included in Exhibit 4.5)		8-K		4.4	7/12/19
4.8	Fourth Supplemental Indenture, dated as of November 1, 2021, by and between Micron Technology, Inc. and U.S. Bank National Association, as Trustee		8-K		4.2	11/1/21
4.9	Form of Note for Micron Technology, Inc.'s 2.703% Senior Notes due 2032 (included in Exhibit 4.8)		8-K		4.3	11/1/21
4.10	Form of Note for Micron Technology, Inc.'s 3.366% Senior Notes due 2041 (included in Exhibit 4.8)		8-K		4.4	11/1/21
4.11	Form of Note for Micron Technology, Inc.'s 3.477% Senior Notes due 2051 (included in Exhibit 4.8)		8-K		4.5	11/1/21
4.12	Description of Registrant's Securities		10-K	9/1/22	4.12	10/7/22
4.13	Fifth Supplemental Indenture, dated as of October 31, 2022, by and between Micron Technology, Inc. and U.S. Bank Trust Company, National Association, as Trustee		8-K		4.2	10/31/22
4.14	Form of Note for Micron Technology, Inc.'s 6.750% Senior Notes due 2029 (included in Exhibit 4.13)		8-K		4.3	10/31/22
4.15	Sixth Supplemental Indenture, dated as of February 9, 2023, by and between Micron Technology, Inc. and U.S. Bank Trust Company, National Association, as Trustee		8-K		4.3	2/9/23
4.16	Form of Note for Micron Technology, Inc.'s 5.875% Senior Notes due 2033 (included in Exhibit 4.15)		8-K		4.5	2/9/23
4.17	Seventh Supplemental Indenture, dated as of April 11, 2023, by and between Micron Technology, Inc. and U.S. Bank Trust Company, National Association, as Trustee		8-K		4.2	4/11/23
4.18	Form of Note for Micron Technology, Inc.'s 5.375% Senior Notes due 2028 (included in Exhibit 4.17)		8-K		4.3	4/11/23
4.19	Form of Note for Micron Technology, Inc.'s 5.875% Senior Notes due 2033 (included in Exhibit 4.17)		8-K		4.4	4/11/23
10.1*	Micron Technology, Inc. Executive Officer Performance Incentive Plan		DEF 14A		B	12/7/17
10.2*	Amended and Restated 2004 Equity Incentive Plan		10-Q	12/1/22	10.1	12/22/22
10.3*	2004 Equity Incentive Plan Forms of Agreement and Terms and Conditions		10-Q	12/1/22	10.2	12/22/22
10.4*	Amended and Restated 2007 Equity Incentive Plan		DEF 14A		A	12/1/20

Exhibit Number	Description of Exhibit	Filed Herewith	Form	Period Ending	Exhibit/ Appendix	Filing Date
10.5*	2007 Equity Incentive Plan Forms of Agreement and Terms and Conditions		10-Q	12/1/22	10.3	12/22/22
10.6*	Nonstatutory Stock Option Plan, as Amended		10-K	9/1/16	10.10	10/28/16
10.7*	Nonstatutory Stock Option Plan Form of Agreement and Terms and Conditions		10-K	9/1/16	10.11	10/28/16
10.8*	Form of Indemnification Agreement between the Registrant and its officers and directors		10-Q	2/27/14	10.3	4/7/14
10.9*	Form of Severance Agreement		8-K		99.2	11/1/07
10.10*	Deferred Compensation Plan, as amended	X				
10.11*	Amended and Restated Executive Agreement by and between Micron Technology, Inc. and Sanjay Mehrotra		10-K	9/1/22	10.11	10/7/22
10.12*	Severance Benefits for Sumit Sadana		10-Q	11/30/17	10.70	12/20/17
10.13*	Form of Amendment to Executive/Severance Agreement		8-K		99.1	11/13/17
10.14*	Severance Benefits for Manish Bhatia		10-Q	11/30/17	10.74	12/20/17
10.15*	Micron Technology, Inc. Employee Stock Purchase Plan, as amended and restated		10-Q	6/2/22	10.1	7/1/22
10.16*	Severance Benefits for Mark Murphy		10-Q	6/2/22	10.3	7/1/22
10.17	Credit Agreement, dated as of May 14, 2021, by and among Micron Technology, Inc., as borrower, HSBC Bank USA, National Association, as administrative agent, the other agents party thereto, and each financial institution party from time to time thereto		10-Q	6/3/21	10.22	7/1/21
10.18	Term Loan Credit Agreement, dated as of May 14, 2021, by and among Micron Technology, Inc., as borrower, Wells Fargo Bank, National Association, as administrative agent, the other agents party thereto, and each financial institution party from time to time thereto		10-Q	6/3/21	10.23	7/1/21
10.19	Term Loan Credit Agreement, dated as of November 3, 2022, by and among Micron Technology, Inc., as borrower, Wells Fargo Bank, National Association, as administrative agent, the other agents party thereto, and each financial institution party from time to time thereto		10-Q	12/1/22	10.4	12/22/22
10.20	Incremental Amendment No. 1, dated as of January 5, 2023, to the Term Loan Credit Agreement, dated as of November 3, 2022, by and among Micron Technology, Inc., as borrower, Wells Fargo Bank, National Association, as administrative agent, and the lenders party thereto		10-Q	3/2/23	10.1	3/29/23
10.21	Amendment No. 1 to Term Loan Credit Agreement, dated as of March 27, 2023, by and among Micron Technology, Inc., as borrower, Wells Fargo Bank, National Association, as administrative agent, and the lenders party thereto		10-Q	3/2/23	10.3	3/29/23
10.22	Amendment No. 2 to Term Loan Credit Agreement, dated as of March 27, 2023, by and among Micron Technology, Inc., as borrower, Wells Fargo Bank, National Association, as administrative agent, and the lenders party thereto		10-Q	3/2/23	10.2	3/29/23
10.23	Amendment No. 1 to Credit Agreement, dated as of March 27, 2023, by and among Micron Technology, Inc., as borrower, HSBC Bank USA, National Association, as administrative agent, and the lenders party thereto		10-Q	3/2/23	10.4	3/29/23
10.24*	Form of Consent for Named Executive Officers		10-Q	3/2/23	10.5	3/29/23
10.25	Amendment No. 2 to Credit Agreement, dated as of June 7, 2023, by HSBC Bank USA, National Association, as administrative agent		10-Q	6/1/23	10.1	6/29/23
10.26	Amendment No. 2 to Term Loan Credit Agreement, dated as of June 7, 2023, by Wells Fargo Bank, National Association, as administrative agent		10-Q	6/1/23	10.2	6/29/23
21.1	Subsidiaries of the Registrant	X				
23.1	Consent of Independent Registered Public Accounting Firm	X				
31.1	Rule 13a-14(a) Certification of Chief Executive Officer	X				

Exhibit Number	Description of Exhibit	Filed Herewith	Form	Period Ending	Exhibit/ Appendix	Filing Date
31.2	Rule 13a-14(a) Certification of Chief Financial Officer	X				
32.1	Certification of Chief Executive Officer Pursuant to 18 U.S.C. 1350	X				
32.2	Certification of Chief Financial Officer Pursuant to 18 U.S.C. 1350	X				
97.1	Compensation Recoupment (Clawback) Policy, as amended and restated	X				
101.INS	Inline XBRL Instance Document - the instance document does not appear in the Interactive Data File because its XBRL tags are embedded within the Inline XBRL document	X				
101.SCH	Inline XBRL Taxonomy Extension Schema Document	X				
101.CAL	Inline XBRL Taxonomy Extension Calculation Linkbase Document	X				
101.DEF	Inline XBRL Taxonomy Extension Definition Linkbase Document	X				
101.LAB	Inline XBRL Taxonomy Extension Label Linkbase Document	X				
101.PRE	Inline XBRL Taxonomy Extension Presentation Linkbase Document	X				
104	Cover Page Interactive Data File (formatted as Inline XBRL and contained in Exhibit 101)	X				

* Indicates management contract or compensatory plan or arrangement.

ITEM 16. FORM 10-K SUMMARY

None.

SIGNATURES

Pursuant to the requirements of Section 13 or 15(d) of the Securities Exchange Act of 1934, the Registrant has duly caused this report to be signed on its behalf by the undersigned, thereunto duly authorized.

Micron Technology, Inc.

Date October 6, 2023

By: */s/ Mark Murphy*
Mark Murphy
Executive Vice President and Chief Financial Officer
(Principal Financial Officer)

Pursuant to the requirements of the Securities Exchange Act of 1934, this report has been signed below by the following persons on behalf of the Registrant and in the capacities and on the dates indicated.

Signature	Title	Date
/s/ Sanjay Mehrotra **(Sanjay Mehrotra)**	President and Chief Executive Officer and Director (Principal Executive Officer)	October 6, 2023
/s/ Mark Murphy **(Mark Murphy)**	Executive Vice President and Chief Financial Officer (Principal Financial Officer)	October 6, 2023
/s/ Scott Allen **(Scott Allen)**	Corporate Vice President and Chief Accounting Officer (Principal Accounting Officer)	October 6, 2023
/s/ Richard M. Beyer **(Richard M. Beyer)**	Director	October 6, 2023
/s/ Lynn Dugle **(Lynn Dugle)**	Director	October 6, 2023
/s/ Steve Gomo **(Steve Gomo)**	Director	October 6, 2023
/s/ Linnie Haynesworth **(Linnie Haynesworth)**	Director	October 6, 2023
/s/ Mary Pat McCarthy **(Mary Pat McCarthy)**	Director	October 6, 2023
/s/ Robert E. Switz **(Robert E. Switz)**	Chair of the Board Director	October 6, 2023
/s/ MaryAnn Wright **(MaryAnn Wright)**	Director	October 6, 2023

Exhibit 10.10

MICRON TECHNOLOGY, INC.
DEFERRED COMPENSATION PLAN

Effective March 1, 2017

Amended and Restated Effective October 1, 2023

PREAMBLE

The Plan is intended to be a "plan which is unfunded and is maintained by an employer primarily for the purpose of providing deferred compensation for a select group of management or highly compensated employees" within the meaning of Sections 201(2), 301(a)(3) and 401(a)(1) of the Employee Retirement Income Security Act of 1974, as amended, or an "excess benefit plan" within the meaning of Section 3(36) of the Employee Retirement Income Security Act of 1974, as amended, or a combination of both. The Plan is further intended to conform with the requirements of Internal Revenue Code Section 409A and the final regulations issued thereunder and shall be interpreted, implemented and administered in a manner consistent therewith.

Article 1 - GENERAL

1.1 **Purpose**. The purpose of the Plan is to provide Eligible Employees an opportunity to defer to a future date the receipt of base and bonus compensation for services performed for the Employer.

1.2 **Effective Date.** The Effective Date of the Plan is March 1, 2017.

Article 2 - DEFINITIONS

Pronouns used in the Plan are in the masculine gender but include the feminine gender unless the context clearly indicates otherwise. Wherever used herein, the following terms have the meanings set forth below, unless a different meaning is clearly required by the context:

2.1 **"Account"** means an account established for the purpose of recording amounts credited on behalf of a Participant and any income, expenses, gains, losses or distributions included thereon. The Account shall be a bookkeeping entry only and shall be utilized solely as a device for the measurement and determination of the amounts to be paid to a Participant or to the Participant's Beneficiary pursuant to the Plan.

2.2 **"Administrator"** means the DCP Committee.

2.3 "**Base Compensation**" means the Participant's base rate of compensation (including regular compensation, holiday, vacation, personal and sick pay) payable for services performed for the Employer for the Plan Year, as adjusted to reflect increases and decreases to the base rate during the Plan Year.

2.4 **"Beneficiary"** means the persons, trusts, estates or other entities entitled under Section 8.2 to receive benefits under the Plan upon the death of a Participant.

2.5 **"Board" or "Board of Directors"** means the Board of Directors of the Plan Sponsor.

2.6 **"Bonus Compensation"** means the Participant's annual bonus or incentive compensation payable for services performed for the Employer for the Plan Year pursuant to, among others designated by the Employer, the Micron Technology, Inc. Executive Incentive Plan, the Micron Technology, Inc. Annual Incentive Plan, and/or the Micron Technology, Inc. Incentive Pay Plan.

2.7 **"Change in Control"** means the occurrence of an event involving the Plan Sponsor that is described in Section 9.6.

2.8 **"Code"** means the Internal Revenue Code of 1986, as amended.

2.9 "**Compensation**" means Base Compensation, Bonus Compensation, Fiscal Year Compensation and/or Performance-Based Compensation.

2.10 "**Covered Compensation**" means such Compensation deferred under the Plan that constitutes incentive compensation under the Micron Recoupment Policy.

2.11 "**DCP Committee**" means the Senior Vice President and Chief People Officer of Micron (or individual with similar successor responsibilities) or any other individual or committee appointed by such officer to administer the Plan.

2.12 **"Disability"** means a determination by the Administrator that the Participant is either (a) unable to engage in any substantial gainful activity by reason of any medically determinable physical or mental impairment which can be expected to result in death or can be expected to last for a continuous period of not less than 12 months, or (b) is, by reason of any medically determinable physical or mental impairment which can be expected to result in death or last for a continuous period of not less than twelve months, receiving income replacement benefits for a period of not less than three months under an accident and health plan covering employees of the Employer. A Participant will be considered to have incurred a Disability if he is determined to be totally disabled by the Social Security Administration or the Railroad Retirement Board.

2.13 **"Discretionary Credits"** has the meaning set forth in Section 5.1 hereof.

2.14 **"Distribution Date"** means the earliest to occur of: (1) a Specified Payment Date elected by the Participant or (2) the Participant's Separation from Service for any reason (including death or Disability). Notwithstanding the foregoing, in the case of a distribution to a Specified Employee on account of Separation from Service, the Distribution Date shall be the Specified Employee Delayed Payment Date.

2.15 "**Election Period**" means the period established by the Administrator during which Participant deferral and distribution elections must be made in accordance with the requirements of Code Section 409A. The Election Period for Base Compensation and for Bonus Compensation shall end no later than the last day of the Plan Year immediately preceding the Plan Year in which such Base Compensation or Bonus Compensation is earned. The Election Period for Fiscal Year Compensation that does not qualify as Performance-Based Compensation shall end no later than the last day of the immediately preceding Fiscal Year in which such Fiscal Year Compensation is earned (or such earlier date as the Administrator may prescribe). The Election Period for Performance-Based Compensation shall end no later than six (6) months before the end of the Fiscal Year or other period in which the Performance-Based Compensation is earned (or such earlier date as the Administrator may prescribe); provided, that the Eligible Employee is employed continuously from the later of the beginning of the performance period or the date the performance criteria are established through the date an election is made to defer such Performance-Based Compensation and the amount of such Performance-Based Compensation has not become readily ascertainable as of the date the election is made; and further provided, however, that the Election Period with respect to the first Plan Year in which an Eligible Employee is eligible to participate in the Plan may, to the extent permitted under Code Section 409A, end no later than thirty (30) days after the Eligible Employee first becomes eligible under the Plan and shall apply only to compensation earned after such election is made. A former Eligible Employee who again becomes an Eligible Employee shall be treated as newly eligible to make deferrals under the Plan within thirty (30) days upon return to eligible status if: (i) the former Eligible Employee has received distribution of the full amount of his or her Account balance attributable to deferral contributions and on or before the last such distribution was not eligible to make deferral contributions for periods after the last distribution payment; or (ii) the former Eligible Employee has not been eligible to make deferral contributions at any time during the twenty-four (24)-month period ending on the date he or she again becomes an Eligible Employee. In addition, if an Eligible Employee is or was eligible to participate in another plan that is aggregated with the elective deferral portion of the Plan under Code Section 409A, participation in such plan shall be treated as participation in the Plan for purposes of determining whether the Eligible Employee is treated as newly eligible under the Plan. Except in the case of the first Plan Year in which an Eligible Employee is eligible to participate in the Plan, including a former Eligible Employee who is treated as newly eligible to make deferrals, the effective date of elections to defer Base or Bonus Compensation shall be the first day of the calendar year following such election, the effective date of elections to defer Fiscal Year Compensation shall be the first day of the Fiscal Year following such election, and in the case of an election to defer Performance-Based Compensation, such election shall be effective with respect to Performance-Based Compensation payable after the end of the applicable performance period.

2.16 **"Eligible Employee"** means an employee of the Employer selected by the Employer for participation in the Plan.

2.17 **"Employer"** means the Plan Sponsor and any other entity which is authorized by the Plan Sponsor to participate in and, in fact, does adopt the Plan.

2.18 **"ERISA"** means the Employee Retirement Income Security Act of 1974, as amended.

2.19 **"Fiscal Year"** means the Employer's fiscal year, if other than the calendar year.

2.20 **"Fiscal Year Compensation"** means the Participant's actual bonus or incentive compensation earned for services performed for the Employer for the Fiscal Year, of which no amount is paid or payable during the Fiscal Year, pursuant to, among others designated by the Employer, the Micron Technology, Inc. Executive Incentive Plan, the Micron Technology, Inc. Annual Incentive Plan, and/or the Micron Technology, Inc. Incentive Pay Plan.

2.21 **"Micron Recoupment Policy"** means the Micron Technology, Inc. Compensation Recoupment (Clawback) Policy, as adopted by the Compensation Committee of the Board of Directors on September 25, 2023, as amended and restated from time-to-time, and any similar successor policy.

2.22 **"Participant"** means an Eligible Employee who commences participation in the Plan in accordance with Article 3.

2.23 **"Performance-Based Compensation"** means any bonus, award or other compensation paid or payable during the Fiscal Year, pursuant to, among others designated by the Employer, the Micron Technology, Inc. Executive Incentive Plan, the Micron Technology, Inc. Annual Incentive Plan, and/or the Micron Technology, Inc. Incentive Pay Plan, the amount of which, or the entitlement to which, is contingent on the satisfaction of pre-established organizational or individual performance criteria relating to a performance period of at least twelve (12) consecutive months. For such bonus or award to be performance-based with respect to a Participant's deferral election with respect to such bonus or award, the following requirements must be met: (i) the performance criteria must be established in writing no later than ninety (90) days after the beginning of the applicable "performance period"; (ii) the outcome of the performance criteria must be substantially uncertain when the criteria are established; (iii) no bonus or award, or portion of any bonus or award, that will be paid either regardless of performance, or based upon a level of performance that is substantially certain to be met at the time the criteria are established, shall be considered Performance-Based Compensation; (iv) Performance-Based Compensation shall not include payments based upon subjective performance criteria unless: (a) the subjective performance criteria are bona fide and relate to the Participant's performance, the performance of a group of employees that includes the Participant, or the performance of a business unit for which the Participant provides services (which may include the entire organization); and (b) the determination that any subjective performance criteria have been met is not made by the Participant or a family member of the Participant (as defined in Code Section 267(c)(4), applied as if the family of an individual includes the spouse of any member of the family), or a person under the effective control of the Participant or such a family member, and no amount of the compensation of the person making such determination is effectively controlled in whole or in part by the Participant or such a family member. A performance-based bonus that otherwise meets the above criteria may provide for payment regardless of satisfaction of the performance criteria upon the Participant's death, disability (defined as a medically determinable physical or mental impairment resulting in the Participant's inability to perform the duties of his or her position or any substantially similar position, where such impairment can be expected to result in death or can be expected to last for a continuous period of not less than six (6) months), or a change in control event (as defined in Treasury Regulations Section 1.409A-3(i)(5)(i)). Any amount that actually becomes payable upon such events without regard to the satisfaction of the performance criteria will not be considered Performance-Based Compensation.

2.24 **"Plan"** means the unfunded plan of deferred compensation set forth herein, as adopted by the Plan Sponsor and as amended from time to time.

2.25 **"Plan Sponsor"** means Micron Technology, Inc. or any successor by merger, consolidation or otherwise.

2.26 **"Plan Year"** means the period commencing January 1 and ending on December 31.

2.27 **"Related Employer"** means the Employer and (a) any corporation that is a member of a controlled group of corporations as defined in Code Section 414(b) that includes the Employer and (b) any trade or business that is under common control as defined in Code Section 414(c) that includes the Employer.

2.28 **"Separation from Service"** means the date that the Participant dies, retires or otherwise has a termination of employment with respect to all entities comprising the Related Employer. A Separation from Service does not occur if the Participant is on military leave, sick leave or other bona fide leave of absence if the period of leave does not exceed six months or such longer period during which the Participant's right to reemployment is provided by statute or contract. If the period of leave exceeds six months and the Participant's right to re-employment is not provided either by statute or contract, a Separation from Service will be deemed to have occurred on the first day following the six-month period. If the period of leave is due to any medically determinable physical or mental impairment that can be expected to result in death or can be expected to last for a continuous period of not less than six months, where the impairment causes the Participant to be unable to perform the duties of his or her position of employment or any substantially similar position of employment, a 29 -month period of absence may be substituted for the six -month period.

Whether a termination of employment has occurred is based on whether the facts and circumstances indicate that the Related Employer and the Participant reasonably anticipated that no further services would be performed after a certain date or that the level of bona fide services the Participant would perform after such date (whether as an employee or as an independent contractor) would permanently decrease to no more than 20 percent of the average level of bona fide services performed (whether as an employee or an independent contractor) over the immediately preceding 36 -month period (or the full period of services to the Related Employer if the employee has been providing services to the Related Employer for less than 36 months).

An independent contractor is considered to have experienced a Separation from Service with the Related Employer upon the expiration of the contract (or, in the case of more than one contract, all contracts) under which services are performed for the Related Employer if the expiration constitutes a good-faith and complete termination of the contractual relationship.

If a Participant provides services as both an employee and an independent contractor of the Related Employer, the Participant must separate from service both as an employee and as an independent contractor to be treated as having incurred a Separation from Service. If a Participant ceases providing services as an independent contractor and begins providing services as an employee, or ceases providing services as an employee and begins providing services as an independent contractor, the Participant will not be considered to have experienced a Separation from Service until the Participant has ceased providing services in both capacities.

If a Participant provides services both as an employee and as a member of the board of directors of a corporate Related Employer (or an analogous position with respect to a noncorporate Related Employer), the services provided as a director are not taken into account in determining whether the Participant has incurred a Separation from Service as an employee for purposes of a nonqualified deferred compensation plan in which the Participant participates as an employee that is not aggregated under Code Section 409A with any plan in which the Participant participates as a director.

If a Participant provides services both as an employee and as a member of the board of directors of a corporate related Employer (or an analogous position with respect to a noncorporate Related Employer), the services provided as an employee are not taken into account in determining whether the Participant has experienced a Separation from Service as a director for purposes of a nonqualified deferred compensation plan in which the Participant participates as a director that is not aggregated under Code Section 409A with any plan in which the Participant participates as an employee.

All determinations of whether a Separation from Service has occurred will be made in a manner consistent with Code Section 409A and the final regulations thereunder.

2.29 **"Specified Employee"** is an employee who on the date of his Separation from Service is a "specified employee" within the meaning given such term under Code Section 409A and the regulations thereunder applying the default criteria.

2.30 **"Specified Employee Delayed Payment Date"** means the first business day of the seventh month following the date of a Specified Employee's Separation from Service.

2.31 **"Specified Payment Date"** means a calendar year elected by the Participant to receive his or her deferrals that is after the Plan Year for which the deferrals are made.

2.32 **"Valuation Date"** means each business day of the Plan Year that the Nasdaq Global Stock Market is open.

2.33 **"Years of Service"** shall be determined in accordance with the Participant's Years of Service credited under the Micron Technology, Inc. Retirement at Micron (RAM) Plan.

Article 3 - PARTICIPATION

3.1 **Participation.** An Eligible Employee shall commence participation in the Plan upon the effectiveness of his first deferral election in accordance with Section 4.1.

3.2 **Termination of Participation.** The Administrator may terminate a Participant's participation in the Plan in a manner consistent with Code Section 409A. If the Employer terminates a Participant's participation before the Participant experiences a Separation from Service the Participant's vested Accounts shall be paid in accordance with the provisions of Article 9.

Article 4 - PARTICIPANT ELECTIONS

4.1 **Deferral Agreement**. An Eligible Employee may elect during the applicable Election Period, by executing in writing or electronically a deferral agreement on form(s) approved by the Administrator, to defer the receipt of a designated percentage of Base Compensation per payroll period that is earned and payable after the effective date of such election, a designated percentage of Bonus Compensation per payroll period that is earned and payable after the effective date of such election, a designated percentage of Fiscal Year Compensation that is earned and payable after the effective date of such election and a designated percentage of Performance-Based Compensation that is payable after the effective date of such election and have such amount credited to the Participant's Account pursuant to the terms of the Plan. The Participant shall make a separate deferral election for Base and Bonus Compensation deferrals for each Plan Year and a separate deferral election of Performance-Based Compensation and Fiscal Year Compensation for a Fiscal Year.

A new deferral election must be timely executed for each Plan Year or Fiscal Year, as applicable, during which the Eligible Employee desires to defer Compensation. An Eligible Employee who does not timely execute a deferral election shall be deemed to have elected zero deferrals of Compensation for such Plan Year or Fiscal Year, as applicable.

4.2 **Revocation/Modification of Deferral Elections**. Except as otherwise provided in Section 9.2, a Participant may not revoke or modify his deferral agreement after the Election Period. The Administrator in its discretion may cancel a deferral election if permitted under Code Section 409A (such as upon disability), provided that the Participant shall not be provided an election with respect to such cancellation.

4.3 **Amount of Deferrals**. An Eligible Employee is not required to make a deferral election for any Plan Year or Fiscal Year. However, if an Eligible Employee makes a deferral election, the following minimums and maximums apply. These minimums and/or maximums may be modified by the Administrator for a given Plan Year or Fiscal Year on the election forms for such Plan Year or Fiscal Year without the need of a formal plan amendment.

(a) **Minimum Base Compensation Deferral Election**. The minimum deferral election percentage an Eligible Employee may make for a Plan Year with respect to Base Compensation is 1% of Base Compensation.

(b) **Minimum Bonus, Fiscal Year and Performance-Based Compensation Deferral Election**. The minimum deferral election percentage an Eligible Employee may make for a Plan Year or Fiscal Year, as applicable, with respect to Bonus, Fiscal Year or Performance-Based Compensation is 1% of such Eligible Employee's bonus or incentive compensation for a Plan Year or Fiscal Year, as applicable.

(c) **Maximum Base Compensation Deferral Election**. The maximum deferral election percentage an Eligible Employee may make for a Plan Year with respect to Base Compensation is 75% of Base Compensation.

(d) **Maximum Bonus, Fiscal Year and Performance-Based Compensation Deferral Election**. The maximum deferral election percentage an Eligible Employee may make for a Plan Year or Fiscal Year, as applicable, with respect to Bonus, Fiscal Year or Performance-Based Compensation is 100% of such Eligible Employee's bonus or incentive compensation for a Plan Year or Fiscal Year, as applicable.

4.4 **Timing of Election to Defer.** Each Eligible Employee who desires to defer Compensation otherwise payable during a Plan Year or Fiscal Year must execute a deferral agreement within the Election Period.

4.5 **Election of Payment Schedule and Form of Payment.** All elections of a payment schedule and a form of payment will be made in accordance with rules and procedures established by the Administrator. At the time an Eligible Employee completes a deferral agreement during the Election Period, the Eligible Employee must elect a form of payment in which to receive such deferrals in a payment schedule permitted under Section 9.3 and may elect a Specified Payment Date that occurs during the Participant's employment. If an Eligible Employee fails to elect a form of payment permitted under Section 9.3, then he shall be deemed to have elected a lump sum form of payment.

4.6 **No Deferrals from Severance**. Deferral elections shall not apply to severance or other amounts payable after a Participant's Separation from Service.

Article 5 - EMPLOYER CONTRIBUTIONS

5.1 **Employer Contributions.** The Employer may, in its sole discretion, make discretionary Employer credits ("Discretionary Credits") on behalf of any Eligible Participant. In its sole discretion, the Employer shall determine the Eligible Participants to be credited with any Discretionary Credit, the amount of any such Discretionary Credit and the vesting schedule applicable thereto (including any accelerated vesting thereof and the events of such acceleration). In addition, the Employer may permit the Participant to elect the timing and form of distribution of such Discretionary Credits, provided that any such election shall be made no later than the latest time permitted by Code Section 409A.

Article 6 - ACCOUNTS AND CREDITS

6.1 **Establishment of Account.** For accounting and computational purposes only, the Administrator will establish and maintain an Account on behalf of each Participant which will reflect the credits made pursuant to Section 6.2, distributions or withdrawals, along with the earnings, expenses, gains and losses allocated thereto, attributable to the hypothetical investments made with the amounts in the Account as provided in Article 7. The Administrator will establish and maintain such other records and accounts, as it decides in its discretion to be reasonably required or appropriate to discharge its duties under the Plan.

6.2 **Credits to Account.** A Participant's Account will be credited with the amount of his elective deferrals under Section 4.1 at the time the amount subject to the deferral election would otherwise have been payable to the Participant and the amount of Employer contributions treated as allocated on his behalf under Article 5.

Article 7 - INVESTMENT OF CONTRIBUTIONS

7.1 Investment Options. The amount credited to each Account shall be treated as invested in the investment options selected in advance by the Administrator. The Administrator, in its sole discretion, shall be permitted to add or remove notional investment options from the Plan menu from time to time, provided that any such additions or removals of investment options shall not be effective with respect to any period prior to the effective date of such change.

7.2 Investment Allocations. A Participant's investment allocation constitutes a deemed, not actual, investment among the investment options comprising the investment menu. At no time shall a Participant have any real or beneficial ownership in any investment option included in the investment menu, nor shall the Employer or any trustee acting on its behalf have any obligation to purchase actual securities as a result of a Participant's investment allocation. A Participant's investment allocation shall be used solely for purposes of adjusting the value of a Participant's Account.

(a) A Participant shall specify an investment allocation for each of his Accounts in accordance with procedures established by the Administrator. Except as otherwise provided by the Administrator, the following provisions of this Section 7.2 shall apply to allocations under the Plan.

(i) Allocation among the investment options must be designated in increments of 1%. The Participant's investment allocation will become effective on the same business day or, in the case of investment allocations received after a time specified by the Administrator, the next business day.

(ii) A Participant may change an investment allocation on any business day, both with respect to future credits to the Plan and with respect to existing Accounts, in accordance with procedures adopted by the Administrator. Changes shall become effective on the same business day or, in the case of investment allocations received after a time specified by the Administrator, the next business day, and shall be applied prospectively.

7.3 Adjustment of Accounts. The amount credited to each Account shall be adjusted for hypothetical investment earnings, expenses, gains or losses in an amount equal to the earnings, expenses, gains or losses attributable to the investment options selected by the Participant from among the investment options provided in Section 7.1. A Participant (or the Participant's Beneficiary after the death of the Participant) may, in accordance with rules and procedures established by the Administrator, select the investments from among the options provided in Section 7.1 to be used for the purpose of calculating future hypothetical investment adjustments to the Account or to future credits to the Account under Section 6.2 effective as of the Valuation Date coincident with or next following notice to the Administrator. Each Account shall be adjusted as of each Valuation Date to reflect: (a) the hypothetical earnings, expenses, gains and losses described above; (b) amounts credited pursuant to Section 6.2; and (c) distributions or withdrawals. In addition, each Account may be adjusted for its allocable share of the hypothetical costs and expenses associated with the maintenance of the hypothetical investments provided in Section 7.1.

Article 8 - RIGHT TO BENEFITS

8.1 Vesting.

(a) A Participant, at all times, has a 100% nonforfeitable interest in the amounts credited to his Account attributable to his elective deferrals made in accordance with Section 4.1.

(b) A Participant's right to the amounts credited to his Account attributable to Discretionary Credits made in accordance with Article 5, if any, shall vest at to 100% of the applicable Discretionary Credit on the date that such Participant achieves two Years of Service (each, an "Employer Contribution Vesting Date"). Upon a Separation from Service prior to an Employer Contribution Vesting Date, the Participant shall forfeit the nonvested portion of his Account. Notwithstanding the foregoing, a Participant's rights to the amounts credited to his Account attributable to Discretionary Credits made in accordance with Article 5, if any, shall vest as to 100% of the applicable Discretionary Credit in the event of such Participant's death or Disability, or upon the occurrence of a Change in Control.

8.2 Death; Disability.

A Participant may designate a Beneficiary or Beneficiaries, or change any prior designation of Beneficiary or Beneficiaries in accordance with rules and procedures established by the Administrator.

A copy of the death notice or other sufficient documentation must be filed with and approved by the Administrator. If upon the death of the Participant there is, in the opinion of the Administrator, no designated Beneficiary for part or all of the Participant's vested Account, such amount will be paid to his estate (such estate shall be deemed to be the Beneficiary for purposes of the Plan) in accordance with the provisions of Article 9.

Article 9 - DISTRIBUTION OF BENEFITS

9.1 Amount of Benefits. The vested amount credited to a Participant's Account as determined under Articles 6, 7 and 8 shall determine and constitute the basis for the value of benefits payable to the Participant under the Plan.

9.2 **Method and Timing of Distributions**. Except as otherwise expressly provided herein, amounts credited to a Participant's Account shall be paid to the Participant in accordance with the Participant's distribution election under Article 4. Distributions shall commence to be paid to the Participant as soon as administratively feasible following the Distribution Date, but in no event later than the time prescribed by Treas. Reg. Section 1.409A-3(d). A Participant may make a one (1) time change to his or her distribution election for a Plan Year or Fiscal Year, as applicable, to elect a later Specified Payment Date in accordance with this Section 9.2 and may make a one (1) time change to his or her distribution election for a Plan Year or Fiscal Year, as applicable, to elect a different payment schedule in accordance with this Section 9.2; provided, however, that an election to defer payment or change the form of distribution shall not take effect until at least 12 months after the date on which the election is made and shall be effective only if (i) the election is made at least twelve (12) months before the Specified Payment Date or payment schedule would otherwise commence or occur, and (ii) the Participant elects a new Specified Payment Date or payment schedule that delays the Specified Payment Date or payment schedule at least five (5) years. For purposes of this Section 9.2, a series of installment payments is always treated as a single payment and not as a series of separate payments.

9.3 **Form of Distribution**. Vested amounts credited to a Participant's Account shall, at the Participant's election specified in his deferral agreement in accordance with Article 4, be payable to the Participant in a single sum cash payment or in substantially equal annual cash installments over not less than two (2) years and not more than ten (10) years. Annual installment payments shall be calculated by dividing the Account balance by the remaining annual installments to be made.

9.4 **Payment Election Overrides.** Notwithstanding the Participant's election as to the time and form of payment, upon the Participant's death or Disability, the Participant's entire Account (including any amounts with respect to which installment payments have previously commenced) shall be paid to the Participant or his Beneficiary in a single sum cash payment.

9.5 **Change in Control.** Notwithstanding the Participant's election as to the time and form of payment, in the event of a Change in Control, the Participant's entire Account (including any amounts with respect to which installment payments have previously commenced) shall be paid to the Participant in a single sum cash payment upon the Change in Control.

A Change in Control, for purposes of the Plan, will occur upon a change in the ownership of the Plan Sponsor, a change in the effective control of the Plan Sponsor or a change in the ownership of a substantial portion of the assets of the Plan Sponsor. The Plan Sponsor, for this purpose, includes any corporation identified in this Section 9.6.

If a Participant continues to make deferrals in accordance with Article 4 after he has received a distribution due to a Change in Control, the residual amount payable to the Participant shall be paid at the time and in the form specified in the elections he makes in accordance with Article 4 or upon his death or Disability as provided in Article 8.

Whether a Change in Control has occurred will be determined by the Administrator in accordance with the rules and definitions set forth in this Section 9.6. A distribution to the Participant will be treated as occurring upon a Change in Control if the Plan Sponsor terminates the Plan in accordance with Section 10.2 and distributes the Participant's benefits within twelve months of a Change in Control as provided in Section 10.3.

(a) **Relevant Corporations.** To constitute a Change in Control for purposes of the Plan, the event must relate to (i) the corporation for whom the Participant is performing services at the time of the Change in Control, (ii) the corporation that is liable for the payment of the Participant's benefits under the Plan (or all corporations liable if more than one corporation is liable) but only if either the deferred compensation is attributable to the performance of services by the Participant for such corporation (or corporations) or there is a bona fide business purpose for such corporation (or corporations) to be liable for such payment and, in either case, no significant purpose of making such corporation (or corporations) liable for such payment is the avoidance of federal income tax, or (iii) a corporation that is a majority shareholder of a corporation identified in (i) or (ii), or any corporation in a chain of corporations in which each corporation is a majority shareholder of another corporation in the chain, ending in a corporation identified in (i) or (ii). A majority shareholder is defined as a shareholder owning more than fifty percent (50%) of the total fair market value and voting power of such corporation.

(b) **Stock Ownership.** Code Section 318(a) applies for purposes of determining stock ownership. Stock underlying a vested option is considered owned by the individual who owns the vested option (and the stock underlying an unvested option is not considered owned by the individual who holds the unvested option). If, however, a vested option is exercisable for stock that is not substantially vested (as defined by Treasury Regulation Section 1.83-3(b) and (j)) the stock underlying the option is not treated as owned by the individual who holds the option.

(c) **Change in the Ownership of a Corporation.** A change in the ownership of a corporation occurs on the date that any one person or more than one person acting as a group, acquires ownership of stock of the corporation that, together with stock held by such person or group, constitutes more than fifty percent (50%) of the total fair market value or total voting power of the stock of such corporation. If any one person or more than one person acting as a group is considered to own more than fifty percent (50%) of the total fair market value or total voting power of the stock of a corporation, the acquisition of additional stock by the same person or persons is not considered to cause a change in the ownership of the corporation (or to cause a change in the effective control of the corporation as discussed below in Section 9.6(d)). An increase in the percentage of stock owned by any one person, or persons acting as a group, as a result of a transaction in which the corporation acquires its stock in exchange for property will be treated as an acquisition of stock. Section 9.6(c) applies only when there is a transfer of stock of a corporation (or issuance of stock of a corporation) and stock in such corporation remains outstanding after the transaction. For purposes of this Section 9.6(c), persons will not be considered to be acting as a group solely because they purchase or own stock of the same corporation at the same time or as a result of a public offering. Persons will, however, be considered to be acting as a group if they are owners of a corporation that enters into a merger, consolidation, purchase or acquisition of stock, or similar business transaction with the corporation. If a person, including an entity, owns stock in both corporations that enter into a merger, consolidation, purchase or acquisition of stock, or similar transaction, such shareholder is considered to be acting as a group with other shareholders in a corporation only with respect to ownership in that corporation prior to the transaction giving rise to the change and not with respect to the ownership interest in the other corporation.

(d) **Change in the effective control of a corporation.** A change in the effective control of a corporation occurs on the date that either (i) any one person, or more than one person acting as a group, acquires (or has acquired during the twelve month period ending on the date of the most recent acquisition by such person or persons) ownership of stock of the corporation possessing thirty percent (30%) or more of the total voting power of the stock of such corporation, or (ii) a majority of members of the corporation's board of directors is replaced during any twelve month period by directors whose appointment or election is not endorsed by a majority of the members of the corporation's board of directors prior to the date of the appointment or election, provided that for purposes of this paragraph (ii), the term corporation refers solely to the relevant corporation identified in Section 9.6(a) for which no other corporation is a majority shareholder for purposes of Section 9.6(a). In the absence of an event described in Section 9.6(d)(i) or (ii), a change in the effective control of a corporation will not have occurred. A change in effective control may also occur in any transaction in which either of the two corporations involved in the transaction has a change in the ownership of such corporation as described in Section 9.6(c) or a change in the ownership of a substantial portion of the assets of such corporation as described in Section 9.6(e). If any one person, or more than one person acting as a group, is considered to effectively control a corporation within the meaning of this Section 9.6(d), the acquisition of additional control of the corporation by the same person or persons is not considered to cause a change in the effective control of the corporation or to cause a change in the ownership of the corporation within the meaning of Section 9.6(c). For purposes of this Section 9.6(d), persons will or will not be considered to be acting as a group in accordance with rules similar to those set forth in Section 9.6(c) with the following exception. If a person, including an entity, owns stock in both corporations that enter into a merger, consolidation, purchase or acquisition of stock, or similar transaction, such shareholder is considered to be acting as a group with other shareholders in a corporation only with respect to the ownership in that corporation prior to the transaction giving rise to the change and not with respect to the ownership interest in the other corporation.

(e) **Change in the ownership of a substantial portion of a corporation's assets.** A change in the ownership of a substantial portion of a corporation's assets occurs on the date that any one person, or more than one person acting as a group (as determined in accordance with rules similar to those set forth in Section 9.6(d)), acquires (or has acquired during the twelve month period ending on the date of the most recent acquisition by such person or persons) assets from the corporation that have a total gross fair market value equal to or more than forty percent (40%) of the total gross fair market value of all of the assets of the corporation immediately prior to such acquisition or acquisitions. For this purpose, gross fair market value means the value of the assets of the corporation or the value of the assets being disposed of determined without regard to any liabilities associated with such assets. There is no Change in Control event under this Section 9.6(e) when there is a transfer to an entity that is controlled by the shareholders of the transferring corporation immediately after the transfer. A transfer of assets by a corporation is not treated as a change in ownership of such assets if the assets are transferred to (i) a shareholder of the corporation (immediately before the asset transfer) in exchange for or with respect to its stock, (ii) an entity, fifty percent (50%) or more of the total value or voting power of which is owned, directly or indirectly, by the corporation, (iii) a person, or more than one person acting as a group, that owns, directly or indirectly, fifty percent (50%) or more of the total value or voting power of all the outstanding stock of the corporation, or (iv) an entity, at least fifty (50%) of the total value or voting power of which is owned, directly or indirectly, by a person described in Section 9.6(e)(iii). For purposes of the foregoing, and except as otherwise provided, a person's status is determined immediately after the transfer of assets.

9.6 Permissible Delays in Payment. Distributions may be delayed beyond the date payment would otherwise occur in accordance with the provisions of Articles 8 and 9 in any of the following circumstances as long as the Employer treats all payments to similarly situated Participants on a reasonably consistent basis.

(a) The Employer may delay payment if it reasonably anticipates that its deduction with respect to such payment would be limited or eliminated by the application of Code Section 162(m). Payment must be made during the Participant's first taxable year in which the Employer reasonably anticipates, or should reasonably anticipate, that if the payment is made during such year the deduction of such payment will not be barred by the application of Code Section 162(m) or during the period beginning with the Participant's Separation from Service and ending on the later of the last day of the Employer's taxable year in which the Participant separates from service or the 15th day of the third month following the Participant's Separation from Service. If a scheduled payment to a Participant is delayed in accordance with this Section 9.7(a), all scheduled payments to the Participant that could be delayed in accordance with this Section 9.7(a) will also be delayed.

(b) The Employer may also delay payment if it reasonably anticipates that the making of the payment will violate federal securities laws or other applicable laws provided payment is made at the earliest date on which the Employer reasonably anticipates that the making of the payment will not cause such violation.

(c) The Employer reserves the right to amend the Plan to provide for a delay in payment upon such other events and conditions as the Secretary of the Treasury may prescribe in generally applicable guidance published in the Internal Revenue Bulletin.

9.7 Permitted Acceleration of Payment. The Employer may permit acceleration of the time or schedule of any payment or amount scheduled to be paid pursuant to a payment under the Plan provided such acceleration would be permitted by the provisions of Reg. Sec. 1.409A-3(j)(4), including the following events:

(a) **Domestic Relations Order.** A payment may be accelerated if such payment is made to an alternate payee pursuant to and following the receipt and qualification of a domestic relations order as defined in Code Section 414(p).

(b) **Compliance with Ethics Agreements and Legal Requirements.** A payment may be accelerated as may be necessary to comply with ethics agreements with the Federal government or as may be reasonably necessary to avoid the violation of Federal, state, local or foreign ethics law or conflicts of laws, in accordance with the requirements of Code Section 409A.

(c) **FICA Tax.** A payment may be accelerated to the extent required to pay the Federal Insurance Contributions Act tax imposed under Code Sections 3101, 3121(a) and 3121(v)(2) with respect to compensation deferred under the Plan (the "FICA Amount"). Additionally, a payment may be accelerated to pay the income tax on wages imposed under Code Section 3401 on the FICA Amount and to pay the additional income tax at source on wages attributable to the pyramiding Code Section 3401 wages and taxes. The total payment under this subsection (c) may not exceed the aggregate of the FICA Amount and the income tax withholding related to the FICA Amount.

(d) **Section 409A Additional Tax.** A payment may be accelerated if the Plan fails to meet the requirements of Code Section 409A; provided that such payment may not exceed the amount required to be included in income as a result of the failure to comply with the requirements of Code Section 409A.

(e) **Offset.** A payment may be accelerated in the Employer's discretion as satisfaction of a debt of the Participant to the Employer, where such debt is incurred in the ordinary course of the service relationship between the Participant and the Employer, the entire amount of the reduction in any of the Employer's taxable years does not exceed $5,000, and the reduction is made at the same time and in the same amount as the debt otherwise would have been due and collected from the Participant.

(f) **Other Events.** A payment may be accelerated in the Administrator's discretion in connection with such other events and conditions as permitted by Code Section 409A.

Article 10 - AMENDMENT AND TERMINATION

10.1 Amendment by Plan Sponsor. The Plan Sponsor reserves the right to amend the Plan (for itself and each Employer) through action of its Board of Directors. No amendment can directly or indirectly deprive any current or former Participant or Beneficiary of all or any portion of his Account which had accrued and vested prior to the amendment.

10.2 Plan Termination Following Change in Control or Corporate Dissolution. The Plan Sponsor reserves the right to terminate the Plan and distribute all amounts credited to all Participant Accounts within the 30 days preceding or the twelve months following a Change in Control as determined in accordance with the rules set forth in Section 9.6. For this purpose, the Plan will be treated as terminated only if all agreements, methods, programs and other arrangements sponsored by the Related Employer immediately after the Change in Control which are treated as a single plan under Reg. Sec. 1.409A-1(c)(2) are also terminated so that all participants under the Plan and all similar arrangements are required to receive all amounts deferred under the terminated arrangements within twelve months of the date the Plan Sponsor irrevocably takes all necessary action to terminate the arrangements. In addition, the Plan Sponsor reserves the right to terminate the Plan within twelve months of a corporate dissolution taxed under Code Section 331 or with the approval of a bankruptcy court pursuant to 11 U. S. C. Section 503(b)(1)(A) provided that amounts deferred under the Plan are included in the gross incomes of Participants in the latest of (a) the calendar year in which the termination and liquidation occurs, (b) the first calendar year in which the amount is no longer subject to a substantial risk of forfeiture, or (c) the first calendar year in which payment is administratively practicable.

10.3 Other Plan Terminations. The Plan Sponsor retains the discretion to terminate the Plan if (a) all arrangements sponsored by the Plan Sponsor that would be aggregated with any terminated arrangement under Code Section 409A and Reg. Sec. 1.409A-1(c)(2) are terminated, (b) no payments other than payments that would be payable under the terms of the arrangements if the termination had not occurred are made within twelve months of the termination of the arrangements, (c) all payments are made within twenty-four months of the date the Plan Sponsor takes all necessary action to irrevocably terminate and liquidate the arrangements, (d) the Plan Sponsor does not adopt a new arrangement that would be aggregated with any terminated arrangement under Code Section 409A and the regulations thereunder at any time within the three year period following the date of termination of the arrangement, and (e) the termination does not occur proximate to a downturn in the financial health of the Plan sponsor. The Plan Sponsor also reserves the right to amend the Plan to provide that termination of the Plan will occur under such conditions and events as may be prescribed by the Secretary of the Treasury in generally applicable guidance published in the Internal Revenue Bulletin.

Article 11 - THE TRUST

11.1 Establishment of Trust. The Plan Sponsor may but is not required to establish a trust to hold amounts which the Plan Sponsor may contribute from time to time to correspond to some or all amounts credited to Participants under Section 6.2. In the event that the Plan Sponsor wishes to establish a trust to provide a source of funds for the payment of Plan benefits, any such trust shall be constructed to constitute an unfunded arrangement that does not affect the status of the Plan as an unfunded plan for purposes of Title I of ERISA and the Code.

11.2 Rabbi Trust. Any trust established by the Plan Sponsor shall be between the Plan Sponsor and a trustee pursuant to a separate written agreement under which assets are held, administered and managed, subject to the claims of the Plan Sponsor's creditors in the event of the Plan Sponsor's insolvency. The trust is intended to be treated as a rabbi trust in accordance with existing guidance of the Internal Revenue Service, and the establishment of the trust shall not cause the Participant to realize current income on amounts contributed thereto. The Plan Sponsor must notify the trustee in the event of a bankruptcy or insolvency.

11.3 Investment of Trust Funds. Any amounts contributed to the trust by the Plan Sponsor shall be invested by the trustee in accordance with the provisions of the trust and the instructions of the Plan Sponsor. Trust investments need not reflect the hypothetical investments selected by Participants under Section 7.1 for the purpose of adjusting Accounts and the earnings or investment results of the trust need not affect the hypothetical investment adjustments to Participant Accounts under the Plan.

Article 12 - PLAN ADMINISTRATION

12.1 Powers and Responsibilities of the Administrator. The Administrator has the full power and the full responsibility to administer the Plan in all of its details, subject, however, to the applicable requirements of ERISA. The Administrator's powers and responsibilities include, but are not limited to, the following:

(a) To make and enforce such rules and procedures as it deems necessary or proper for the efficient administration of the Plan;

(b) To interpret the Plan, its interpretation thereof to be final, except as provided in Section 12.2, on all persons claiming benefits under the Plan;

(c) To decide all questions concerning the Plan and the eligibility of any person to participate in the Plan;

(d) To administer the claims and review procedures specified in Section 12.2;

(e) To compute the amount of benefits which will be payable to any Participant, former Participant or Beneficiary in accordance with the provisions of the Plan;

(f) To determine the person or persons to whom such benefits will be paid;

(g) To authorize the payment of benefits;

(h) To comply with the reporting and disclosure requirements of Part 1 of Subtitle B of Title I of ERISA;

(i) To appoint such agents, counsel, accountants, and consultants as may be required to assist in administering the Plan;

(j) By written instrument, to allocate and delegate its responsibilities, including the formation of an administrative committee to administer the Plan.

12.2 Claims and Review Procedures.

Claims Procedure. If any person believes he is being denied any rights or benefits under the Plan, such person may file a claim in writing with the Administrator. If any such claim is wholly or partially denied, the Administrator will notify such person of its decision in writing. Such notification will be given within 90 days (45 days in the case of a claim regarding Disability) after the claim is received by the Administrator. The Administrator may extend the period for providing the notification by 90 days (30 days in the case of a claim regarding Disability) if special circumstances require an extension of time for processing the claim and if written notice of such extension and circumstance is given to such person within the initial 90 -day period (45 day period in the case of a claim regarding Disability). If such notification is not given within such period, the claim will be considered denied as of the last day of such period and such person may request a review of his claim. Such notification will contain (i) specific reasons for the denial, (ii) specific reference to pertinent Plan provisions, (iii) a description of any additional material or information necessary for such person to perfect such claim and an explanation of why such material or information is necessary, and (iv) a description of the Plan's review procedures and the time limits applicable to such procedures, including a statement of the person's right to bring a civil action following an adverse decision on review. In addition, for a claim regarding Disability, such notification will be provided in a culturally and linguistically appropriate manner and will contain (v) a discussion of the decision, including an explanation of the basis for disagreeing with or not following: (a) the views provided by the claimant's health care or vocation professionals who treated and evaluated the claimant; (b) the views of medical or vocational experts whose advice was obtained by the plan, regardless of whether the advice was relied upon in making the benefit determination; and (c) any disability determination made by the Social Security Administration, (vi) if the adverse benefit determination is based on medical necessity, experimental treatment, or similar exclusion or limit, either an explanation of the scientific or clinical judgement for the determination, applying the terms of the plan to the claimant's medical circumstances, or a statement that an explanation will be provided free of charge upon request, (vii) the specific internal rules, guidelines, protocols, standards or other similar criteria (a "Guideline") that were relied upon in making the adverse determination or a statement that such Guideline does not exist, and (viii) a statement that the claimant is entitled to receive, upon request and free of charge, reasonable access to, and copies of, all documents, records, and other information relevant to the claim for benefits.

Review Procedure. Within 60 days (180 days in the case of a claim regarding Disability) after the date on which a person receives a written notification of denial of claim (or, if written notification is not provided, within 60 days (180 days in the case of a claim regarding Disability) of the date denial is considered to have occurred), such person (or his duly authorized representative) may (i) file a written request with the Administrator for a review of his denied claim and of pertinent documents and (ii) submit written issues and comments to the Administrator. The decision on review will be made within 60 days (45 days in the case of a claim regarding Disability). The Administrator may extend the period for making the decision on review by 60 days (45 days in the case of a claim regarding Disability) if special circumstances require an extension of time for processing the request such as an election by the Administrator to hold a hearing, and if written notice of such extension and circumstances is given to such person within the initial 60-day period (45 days in the case of a claim regarding Disability). If the decision on review is not made within such period, the claim will be considered denied. In the case of a claim regarding Disability, before a final adverse benefit determination is made, the Administrator will provide the claimant, free of charge, with any new or additional evidence or rationale considered, relied upon, or generated by the plan in connection with the claim as soon as possible and sufficiently in advance of the final notice to give the claimant a reasonable opportunity to respond prior to that date.

The Administrator will notify such person of its decision in writing. Such notification will be written in a manner calculated to be understood by such person and will contain specific reasons for the decision as well as specific references to pertinent Plan provisions. The notification will explain that the person is entitled to receive, upon request and free of charge, reasonable access to and copies of all pertinent documents and has the right to bring a civil action following an adverse decision on review. In addition, for a claim regarding Disability, the notification will be provided in a culturally and linguistically appropriate manner and will contain (i) a discussion of the decision, including an explanation of the basis for disagreeing with or not following the views provided by the claimant's health care or vocation professionals that treated and evaluated the claimant; the views of medical or vocational experts whose advise was obtained by the plan, regardless of whether the advice was relied upon in making the benefit determination; and any disability determination made by the Social Security Administration, (ii) if the adverse benefit determination is based on medical necessity, experimental treatment, or similar exclusion or limit, either an explanation of the scientific or clinical judgement for the determination, applying the terms of the plan to the claimant's medical circumstances, or a statement that explanation will be provided free of charge upon request, (iii) any Guideline that was relied upon in making the adverse determination or a statement that such Guideline does not exist.

Exhaustion of Claims Procedures and Right to Bring Legal Claim. No action at law or equity shall be brought more than one (1) year after the Administrator's affirmation of a denial of a claim, or, if earlier, more than four (4) years after the facts or events giving rising to the claimant's allegation(s) or claim(s) first occurred.

12.3 Plan Administrative Costs. All reasonable costs and expenses (including legal, accounting, and employee communication fees) incurred by the Administrator in administering the Plan shall be paid by the Plan to the extent not paid by the Employer.

Article 13 - MISCELLANEOUS

13.1 Unsecured General Creditor of the Employer. Participants and their Beneficiaries, heirs, successors and assigns shall have no legal or equitable rights, interests or claims in any property or assets of the Employer. For purposes of the payment of benefits under the Plan, any and all of the Employer's assets shall be, and shall remain, the general, unpledged, unrestricted assets of the Employer. Each Employer's obligation under the Plan shall be merely that of an unfunded and unsecured promise to pay money in the future.

13.2 Employer's Liability. Each Employer's liability for the payment of benefits under the Plan shall be defined only by the Plan and by the deferral elections entered into between a Participant and the Employer. An Employer shall have no obligation or liability to a Participant under the Plan except as provided by the Plan and a deferral election or agreements. An Employer shall have no liability to Participants employed by other Employers.

13.3 Limitation of Rights. Neither the establishment of the Plan, nor any amendment thereof, nor the creation of any fund or account, nor the payment of any benefits, will be construed as giving to the Participant or any other person any legal or equitable right against the Employer, the Plan or the Administrator, except as provided herein; and in no event will the terms of employment or service of the Participant be modified or in any way affected hereby.

13.4 Anti-Assignment. Except as may be necessary to fulfill a domestic relations order within the meaning of Code Section 414(p), none of the benefits or rights of a Participant or any Beneficiary of a Participant shall be subject to the claim of any creditor. In particular, to the fullest extent permitted by law, all such benefits and rights shall be free from attachment, garnishment, or any other legal or equitable process available to any creditor of the Participant and his or her Beneficiary. Neither the Participant nor his or her Beneficiary shall have the right to alienate, anticipate, commute, pledge, encumber, or assign any of the payments which he or she may expect to receive, contingently or otherwise, under the Plan, except the right to designate a Beneficiary to receive death benefits provided hereunder. Notwithstanding the preceding, the benefit payable from a Participant's Account may be reduced, at the discretion of the administrator, to satisfy any debt or liability to the Employer.

13.5 Facility of Payment. If the Administrator determines, on the basis of medical reports or other evidence satisfactory to the Administrator, that the recipient of any benefit payments under the Plan is incapable of handling his affairs by reason of minority, illness, infirmity or other incapacity, the Administrator may direct the Employer to disburse such payments to a person or institution designated by a court which has jurisdiction over such recipient or a person or institution otherwise having the legal authority under State law for the care and control of such recipient. The receipt by such person or institution of any such payments therefore, and any such payment to the extent thereof, shall discharge the liability of the Employer, the Plan and the Administrator for the payment of benefits hereunder to such recipient.

13.6 Notices. Any notice or other communication to the Employer or Administrator in connection with the Plan shall be deemed delivered in writing if addressed to the Plan Sponsor at the following address: 8000 South Federal Way, Boise, ID 83707, and if either actually delivered at said address or, in the case or a letter, 5 business days shall have elapsed after the same shall have been deposited in the United States mails, first-class postage prepaid and registered or certified.

13.7 Tax Withholding. If the Employer concludes that tax is owing with respect to any deferral or payment hereunder, the Employer shall withhold such amounts from any payments due the Participant or from amounts deferred, as permitted by law, or otherwise make appropriate arrangements with the Participant or his Beneficiary for satisfaction of such obligation. Tax, for purposes of this Section 13.7 means any federal, state, local or any other governmental income tax, employment or payroll tax, excise tax, or any other tax or assessment owing with respect to amounts deferred, any earnings thereon, and any payments made to Participants under the Plan.

13.8 Indemnification.

(a) Each Indemnitee (as defined in Section 13.8(e)) shall be indemnified and held harmless by the Employer for all actions taken by him and for all failures to take action (regardless of the date of any such action or failure to take action), to the fullest extent permitted by the law of the jurisdiction in which the Employer is incorporated, against all expense, liability, and loss (including, without limitation, attorneys' fees, judgments, fines, taxes, penalties, and amounts paid or to be paid in settlement) reasonably incurred or suffered by the Indemnitee in connection with any Proceeding (as defined in Subsection (e)). No indemnification pursuant to this Section shall be made, however, in any case where (1) the act or failure to act giving rise to the claim for indemnification is determined by a court to have constituted willful misconduct or recklessness or (2) there is a settlement to which the Employer does not consent.

(b) The right to indemnification provided in this Section shall include the right to have the expenses incurred by the Indemnitee in defending any Proceeding paid by the Employer in advance of the final disposition of the Proceeding, to the fullest extent permitted by the law of the jurisdiction in which the Employer is incorporated; provided that, if such law requires, the payment of such expenses incurred by the Indemnitee in advance of the final disposition of a Proceeding shall be made only on delivery to the Employer of an undertaking, by or on behalf of the Indemnitee, to repay all amounts so advanced without interest if it shall ultimately be determined that the Indemnitee is not entitled to be indemnified under this Section or otherwise.

(c) Indemnification pursuant to this Section shall continue as to an Indemnitee who has ceased to be such and shall inure to the benefit of his heirs, executors, and administrators. The Employer agrees that the undertakings made in this Section shall be binding on its successors or assigns and shall survive the termination, amendment or restatement of the Plan.

(d) The foregoing right to indemnification shall be in addition to such other rights as the Indemnitee may enjoy as a matter of law or by reason of insurance coverage of any kind and is in addition to and not in lieu of any rights to indemnification to which the Indemnitee may be entitled pursuant to the by-laws of the Employer.

(e) For the purposes of this Section, the following definitions shall apply:

(i) "Indemnitee" shall mean each person serving as an Administrator (or any other person who is an employee, director, or officer of the Employer) who was or is a party to, or is threatened to be made a party to, or is otherwise involved in, any Proceeding, by reason of the fact that he is or was performing administrative functions under the Plan.

(ii) "Proceeding" shall mean any threatened, pending, or completed action, suit, or proceeding (including, without limitation, an action, suit, or proceeding by or in the right of the Employer), whether civil, criminal, administrative, investigative, or through arbitration.

13.9 Successors. The provisions of the Plan shall bind and inure to the benefit of the Plan Sponsor, the Employer and their successors and assigns and the Participant and the Participant's designated Beneficiaries.

13.10 Disclaimer. It is the Plan Sponsor's intention that the Plan comply with the requirements of Code Section 409A. Neither the Plan Sponsor nor the Employer shall have any liability to any Participant should any provision of the Plan fail to satisfy the requirements of Code Section 409A.

13.11 Governing Law. The Plan will be construed, administered and enforced according to the laws of Delaware.

13.12 Clawback. Covered Compensation that is elected to be deferred under the Plan, including amounts currently deferred under the Plan (and earnings thereon) and any amounts previously deferred under the Plan and subsequently paid to Participants (and earnings thereon), shall at all times remain subject to the Micron Recoupment Policy as follows:

(a) If a Participant has timely and properly elected to defer Covered Compensation under the Plan that has become subject to recoupment or forfeiture under the Micron Recoupment Policy prior to the date such Covered Compensation would otherwise be credited as a deferral under the Plan, the Participant's deferral election with respect to such Covered Compensation will remain in full force and effect (without adjustment or proration) and will be applied to the amount of Covered Compensation that remains payable to such Participant after reduction of the amount of Covered Compensation payable in accordance with the Micron Recoupment Policy.

(b) In the event a Participant's Covered Compensation becomes subject to recoupment or forfeiture under the Micron Recoupment Policy, and all or a portion of such Covered Compensation was credited to the Participant's Account under the Plan, the Participant's Account may be reduced by forfeiting the amount of such Covered Compensation (and any earnings thereon) that remains credited to the Participant's Account under the Plan.

(c) In the event a Participant's Covered Compensation becomes subject to recoupment or forfeiture under the Micron Recoupment Policy, and all or a portion of such Covered Compensation was credited to the Participant's Account under the Plan, and all or a portion of such Covered Compensation so credited (and any earnings thereon) was subsequently distributed from the Plan to the Participant, the amount of such Covered Compensation (and any earnings thereon) so distributed from the Plan shall remain subject to the Micron Recoupment Policy. Such Covered Compensation (including earnings) so distributed shall be subject to recoupment in accordance with the Micron Recoupment Policy as though such amount was not previously credited under the Plan.

(d) In the event that a Participant's Account has been paid or has become payable to a Beneficiary or alternate payee in accordance with the operation of the Plan or in accordance with law, any amount subject to forfeiture or recoupment under subsections (b) and (c) above shall remain subject to forfeiture or recoupment in accordance with the terms of the Micron Recoupment Policy with respect to such Beneficiary or alternate payee to the maximum extent permitted by law.

(e) The provisions of this Section 13.12 are not intended to constitute an assignment of a Participant's interest under the Plan in violation of Section 13.4 of the Plan. Further, the reduction of a Participant's Account by forfeiture in accordance with this Section 13.12 is not intended to constitute an impermissible acceleration of benefits in violation of Code Section 409A or a payment to the Plan Sponsor in violation of any trust established by the Plan Sponsor under Article 11 of the Plan.

Effective as of October 1, 2023, except as otherwise expressly provided herein.

MICRON TECHNOLOGY, INC.

/s/ April Arnzen
By: April Arnzen
Its: Senior Vice President and Chief People Officer

EXHIBIT 21.1

MICRON TECHNOLOGY, INC.
SUBSIDIARIES OF THE REGISTRANT*

Name	State (or Jurisdiction) in which Organized
Micron Europe Limited	United Kingdom
Micron Japan, Ltd.	Japan
Micron Memory Japan, K.K.	Japan
Micron Memory Malaysia Sdn. Bhd.	Malaysia
Micron Memory Taiwan Co., Ltd.	Taiwan
Micron Semiconductor Asia, LLC	Delaware
Micron Semiconductor Asia Operations Pte. Ltd.	Singapore
Micron Semiconductor Asia Pte. Ltd.	Singapore
Micron Semiconductor Products, Inc.	Idaho
Micron Semiconductor (Xi'an) Co., Ltd.	China
Micron Technology B.V.	Netherlands
Micron Technology Taiwan, Inc.	Taiwan
S-Squared Insurance Company, Inc.	Hawaii

* The above list of subsidiaries of Micron Technology, Inc. omitted subsidiaries which, considered in the aggregate as a single subsidiary, would not constitute a significant subsidiary as of the end of the year covered by this report.

EXHIBIT 23.1

CONSENT OF INDEPENDENT REGISTERED PUBLIC ACCOUNTING FIRM

We hereby consent to the incorporation by reference in the Registration Statements on Form S-3 (File No. 333-249838) and Form S-8 (File Nos. 333-17073, 333-50353, 333-103341, 333-120620, 333-133667, 333-140091, 333-148357, 333-159711, 333-171717, 333-179592, 333-190010, 333-196293, 333-203467, 333-217314, 333-223874, 333-234359, 333-255794, 333-273808) of Micron Technology, Inc. of our report dated October 6, 2023 relating to the financial statements and financial statement schedule and the effectiveness of internal control over financial reporting, which appears in this Form 10-K.

/s/ PricewaterhouseCoopers LLP

San Jose, California
October 6, 2023

EXHIBIT 31.1

RULE 13a-14(a) CERTIFICATION OF CHIEF EXECUTIVE OFFICER

I, Sanjay Mehrotra, certify that:

1. I have reviewed this Annual Report on Form 10-K of Micron Technology, Inc.;

2. Based on my knowledge, this report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this report;

3. Based on my knowledge, the financial statements, and other financial information included in this report, fairly present in all material respects the financial condition, results of operations, and cash flows of the registrant as of, and for, the periods presented in this report;

4. The registrant's other certifying officer(s) and I are responsible for establishing and maintaining disclosure controls and procedures (as defined in Exchange Act Rules 13a-15(e) and 15d-15(e)) and internal control over financial reporting (as defined in Exchange Act Rules 13a-15(f) and 15d-15(f)) for the registrant and have:

   a. Designed such disclosure controls and procedures, or caused such disclosure controls and procedures to be designed under our supervision, to ensure that material information relating to the registrant, including its consolidated subsidiaries, is made known to us by others within those entities, particularly during the period in which this report is being prepared;

   b. Designed such internal control over financial reporting, or caused such internal control over financial reporting to be designed under our supervision, to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with generally accepted accounting principles;

   c. Evaluated the effectiveness of the registrant's disclosure controls and procedures and presented in this report our conclusions about the effectiveness of the disclosure controls and procedures, as of the end of the period covered by this report based on such evaluation; and

   d. Disclosed in this report any change in the registrant's internal control over financial reporting that occurred during the registrant's most recent fiscal quarter (the registrant's fourth fiscal quarter in the case of an annual report) that has materially affected, or is reasonably likely to materially affect, the registrant's internal control over financial reporting; and

5. The registrant's other certifying officer(s) and I have disclosed, based on our most recent evaluation of internal control over financial reporting, to the registrant's auditors and the audit committee of the registrant's board of directors (or persons performing the equivalent functions):

   a. All significant deficiencies and material weaknesses in the design or operation of internal control over financial reporting which are reasonably likely to adversely affect the registrant's ability to record, process, summarize, and report financial information; and

   b. Any fraud, whether or not material, that involves management or other employees who have a significant role in the registrant's internal control over financial reporting.

Date: October 6, 2023

/s/ Sanjay Mehrotra

Sanjay Mehrotra
President and Chief Executive Officer and Director

EXHIBIT 31.2

RULE 13a-14(a) CERTIFICATION OF CHIEF FINANCIAL OFFICER

I, Mark Murphy, certify that:

1. I have reviewed this Annual Report on Form 10-K of Micron Technology, Inc.;

2. Based on my knowledge, this report does not contain any untrue statement of a material fact or omit to state a material fact necessary to make the statements made, in light of the circumstances under which such statements were made, not misleading with respect to the period covered by this report;

3. Based on my knowledge, the financial statements, and other financial information included in this report, fairly present in all material respects the financial condition, results of operations, and cash flows of the registrant as of, and for, the periods presented in this report;

4. The registrant's other certifying officer(s) and I are responsible for establishing and maintaining disclosure controls and procedures (as defined in Exchange Act Rules 13a-15(e) and 15d-15(e)) and internal control over financial reporting (as defined in Exchange Act Rules 13a-15(f) and 15d-15(f)) for the registrant and have:

   a. Designed such disclosure controls and procedures, or caused such disclosure controls and procedures to be designed under our supervision, to ensure that material information relating to the registrant, including its consolidated subsidiaries, is made known to us by others within those entities, particularly during the period in which this report is being prepared;

   b. Designed such internal control over financial reporting, or caused such internal control over financial reporting to be designed under our supervision, to provide reasonable assurance regarding the reliability of financial reporting and the preparation of financial statements for external purposes in accordance with generally accepted accounting principles;

   c. Evaluated the effectiveness of the registrant's disclosure controls and procedures and presented in this report our conclusions about the effectiveness of the disclosure controls and procedures, as of the end of the period covered by this report based on such evaluation; and

   d. Disclosed in this report any change in the registrant's internal control over financial reporting that occurred during the registrant's most recent fiscal quarter (the registrant's fourth fiscal quarter in the case of an annual report) that has materially affected, or is reasonably likely to materially affect, the registrant's internal control over financial reporting; and

5. The registrant's other certifying officer(s) and I have disclosed, based on our most recent evaluation of internal control over financial reporting, to the registrant's auditors and the audit committee of the registrant's board of directors (or persons performing the equivalent functions):

   a. All significant deficiencies and material weaknesses in the design or operation of internal control over financial reporting which are reasonably likely to adversely affect the registrant's ability to record, process, summarize, and report financial information; and

   b. Any fraud, whether or not material, that involves management or other employees who have a significant role in the registrant's internal control over financial reporting.

Date: October 6, 2023

/s/ Mark Murphy

Mark Murphy
Executive Vice President and Chief Financial Officer

EXHIBIT 32.1

CERTIFICATION OF CHIEF EXECUTIVE OFFICER
PURSUANT TO 18 U.S.C. 1350

I, Sanjay Mehrotra, certify, pursuant to 18 U.S.C. 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002, that the Annual Report of Micron Technology, Inc. on Form 10-K for the period ended August 31, 2023, fully complies with the requirements of Section 13(a) or 15(d) of the Securities Exchange Act of 1934 and that information contained in the Annual Report on Form 10-K fairly presents, in all material respects, the financial condition and results of operations of Micron Technology, Inc.

Date: October 6, 2023

/s/ Sanjay Mehrotra

Sanjay Mehrotra
President and Chief Executive Officer and Director

EXHIBIT 32.2

CERTIFICATION OF CHIEF FINANCIAL OFFICER
PURSUANT TO 18 U.S.C. 1350

I, Mark Murphy, certify, pursuant to 18 U.S.C. 1350, as adopted pursuant to Section 906 of the Sarbanes-Oxley Act of 2002, that the Annual Report of Micron Technology, Inc. on Form 10-K for the period ended August 31, 2023, fully complies with the requirements of Section 13(a) or 15(d) of the Securities Exchange Act of 1934 and that information contained in the Annual Report on Form 10-K fairly presents, in all material respects, the financial condition and results of operations of Micron Technology, Inc.

Date: October 6, 2023

/s/ Mark Murphy

Mark Murphy
Executive Vice President and Chief Financial Officer

Exhibit 97.1

MICRON TECHNOLOGY, INC.

COMPENSATION RECOUPMENT (CLAWBACK) POLICY

As Amended and Restated effective September 25, 2023

Micron Technology, Inc. (the "**Company**") is committed to strong corporate governance. As part of this commitment, the Compensation Committee (the "**Compensation Committee**") of Company's Board of Directors (the "**Board**"), having previously adopted a Compensation Recoupment (Clawback) Policy effective as of October 20, 2016, hereby amends and restates the Policy, effective as of the date specified above. This Policy is intended to further the Company's pay-for-performance philosophy and to comply with applicable law by providing for the recovery of certain executive compensation in the event of an Accounting Restatement. The capitalized terms in this Policy are defined below.

The application of the Policy to Executive Officers is not discretionary and applies without regard to whether an Executive Officer was at fault, except to the limited extent provided below.

Persons Covered by the Policy

This Policy is binding and enforceable against all Executive Officers.

Administration of the Policy

The Compensation Committee has full authority to administer this Policy. The Compensation Committee is authorized to interpret and construe this Policy and to make all determinations necessary, appropriate, or advisable for the administration of this Policy. In addition, if determined in the discretion of the Board, this Policy may be administered by the independent members of the Board or another independent committee thereof, in which case all references herein to the Compensation Committee shall be deemed references to the independent members of the Board or the other independent committee of the Board, as applicable. All determinations of the Compensation Committee and any other administrator of the Policy will be final and binding on all interested persons and will be given the maximum deference permitted by law.

Compensation Covered by the Policy

This Policy applies to all Incentive-Based Compensation that is Received on or after October 2, 2023, by a person (a) after such individual became an Executive Officer, (B) who was as an Executive Officer at any time during the applicable performance period for that Incentive-Based Compensation and (c) during the Covered Period ("**Clawback Eligible Incentive-Based Compensation**").

Events Requiring Application of the Policy

If the Company is required to prepare an accounting restatement due to the material noncompliance of the Company with any financial reporting requirement under the securities laws, including any required accounting restatement to correct an error in previously issued financial statements that is material to the previously issued financial statements, or that would result in a material misstatement if the error were corrected in the current period or left uncorrected in the current period (an "**Accounting Restatement**"); AND

any Executive Officer has Received Clawback Eligible Incentive-Based Compensation that exceeds the amount of Incentive-Based Compensation that otherwise would have been Received had such Incentive-Based Compensation been determined based on the restated amounts, computed without regard to any taxes paid (such compensation, the "**Excess Compensation**" (which the Nasdaq listing standards describe as erroneously awarded incentive-based compensation);

then, the Company will recover reasonably promptly the amount of such Excess Compensation in compliance with this Policy unless an exception applies under this Policy.

Determining Excess Compensation for Certain Incentive-Based Compensation

To determine the amount of Excess Compensation for Incentive-Based Compensation based on stock price or total shareholder return, where it is not subject to mathematical recalculation directly from the information in an Accounting Restatement:

- The amount must be based on a reasonable estimate of the effect of the Accounting Restatement on the stock price or total shareholder return upon which the Incentive-Based Compensation was Received; and
- The Company must maintain documentation of the determination of that reasonable estimate and provide such documentation to the Exchange.

Exceptions to the Policy

The Company must recover the Excess Compensation in accordance with this Policy except to the limited extent that the conditions set forth below are met, and the Compensation Committee has made a determination that recovery of the Excess Compensation would be impracticable:

A. The direct expense paid to a third party to assist in enforcing this Policy would exceed the amount to be recovered. Before reaching this conclusion, the Company must make a reasonable attempt to recover such Excess Compensation, document such reasonable attempt(s) to recover, and provide that documentation to the Exchange; or

B. Recovery would violate home country law where that law was adopted prior to November 28, 2022. Before reaching this conclusion, the Company must obtain an opinion of home country counsel, acceptable to the Exchange, that recovery would result in such a violation, and must provide such opinion to the Exchange; or

C. Recovery would likely cause an otherwise tax-qualified retirement plan, under which benefits are broadly available to employees of the Company, to fail to meet the requirements of 26 U.S.C. 401(a)(13) or 26 U.S.C. 411(a) and regulations thereunder.

Defined Terms in this Policy

The capitalized terms in this Policy have the following meaning, unless clearly required otherwise by the context.

"**Accounting Restatement**" is defined in the "Events Requiring Application of the Policy" section of this Policy.

"**Accounting Restatement Determination Date**" means the earliest to occur of:

A. The date the Board, a committee of the Board, or one or more of the officers of the Company authorized to take such action if Board action is not required, concludes, or reasonably should have concluded, that the Company is required to prepare an Accounting Restatement; and

B. The date a court, regulator, or other legally authorized body directs the Company to prepare an Accounting Restatement.

"**Covered Period**" means the three completed fiscal years immediately preceding the Accounting Restatement Determination Date, as well as any transition period (that results from a change in the Company's fiscal year) within or immediately following those three completed fiscal years in accordance with Rule 10D-1 under the Exchange Act. The Company's obligation to recover Excess Compensation (as defined below) is not dependent on if or when the restated financial statements are filed.

"**Excess Compensation**" is defined in the "Events Requiring Application of the Policy" section of this Policy.

"**Executive Officer**" means each individual who either (a) at the time of determination is designated as an "officer" of the Company in accordance with Exchange Act Rule 16a-1(f), (b) at any time prior to the time of determination was designated as an "officer" of the Company in accordance with Exchange Act Rule 16a-1(f). Each Executive Officer must sign and return to the Company an acknowledgement (in substantially the form provided in this Policy or provided by a duly authorized representative of the Company) that the Executive Officer agrees to be bound by the terms and comply with the Policy. However, this Policy will be enforceable against each Executive Officer whether or not the Executive Officer complies with the preceding sentence.

"**Exchange**" is defined in the "Other Important Information in the Policy" section of this Policy.

"**Exchange Act**" means the Securities Exchange Act of 1934, as amended and any valid regulation or applicable guidance of general applicability thereunder.

"**Financial Reporting Measure**" means a measure that is determined and presented in accordance with the accounting principles used in preparing the Company's financial statements, and any measure that is derived wholly or in part from such measure. Stock price and total shareholder return are also Financial Reporting Measures. A Financial Reporting Measure need not be presented within the financial statements or included in a filing with the Securities and Exchange Commission.

"**Incentive-Based Compensation**" means any compensation that is granted, earned, or vested based wholly or in part upon the attainment of a Financial Reporting Measure.

The following items of compensation are not Incentive-Based Compensation under the Policy: salaries, bonuses paid solely at the discretion of the Compensation Committee or the Board that are not paid from a bonus pool that is determined by satisfying a Financial Reporting Measure, bonuses paid solely upon satisfying one or more subjective standards and/or completion of a specified employment period, non-equity incentive plan awards earned solely upon satisfying one or more strategic measures or operational measures, and equity awards for which the grant is not contingent upon achieving any Financial Reporting Measure performance goal and vesting is contingent solely upon completion of a specified employment period (e.g., time-based vesting equity awards) and/or attaining one or more non-Financial Reporting Measures.

"Policy" means this Compensation Recoupment (Clawback) Policy (a compensation "clawback" policy), as it may be amended from time to time.

"**Received**" means that the Financial Reporting Measure specified for earning an Incentive-Based Compensation award is attained in the relevant Company fiscal period, even if the payment or grant of the Incentive-Based Compensation occurs after the end of that fiscal period. As described above in Compensation Covered by the Policy, Incentive-Based Compensation that is Received before the Effective Date is not subject to this amended and restated Policy, although such Incentive-Based Compensation may be subject to recoupment as provided in the Company's Compensation Recoupment (Clawback) Policy adopted effective as of October 20, 2016 (that is, the Policy as in effect prior to this amendment and restatement).

Repayment of Excess Compensation

The Company will seek recovery of any Excess Compensation reasonably promptly and any affected Executive Officer is required to repay such Excess Compensation. Subject to applicable law, the Company may recover such Excess Compensation by requiring the Executive Officer to repay such amount to the Company by direct payment to the Company or such other means or combination of means as the Compensation Committee determines to be appropriate (which determinations need not be identical as to each Executive Officer), including but not limited to (a) seeking recovery of any gain realized on the vesting, exercise, settlement, sale, transfer, or other disposition of any equity-based awards; (b) offsetting the amount to be recovered from any compensation otherwise owed by the Company to the Executive Officer, whether earned before or after the date of the foregoing determination and whether earned pursuant to employment or under a severance, consulting or other post-employment agreement or arrangement; (c) cancelling outstanding vested or unvested equity awards; (d) requiring reimbursement of previously-paid cash Incentive-Based Compensation; and/or (e) taking any other remedial and recovery action permitted by law, as determined by the Compensation Committee, in each case, notwithstanding any Executive Officer's belief (whether legitimate or reasonably or not) that the Excess Compensation had been previously earned under applicable law and therefore not subject to recoupment. This Policy does not preclude the Company from taking any other action to enforce an Executive Officer's obligations to the Company or to discipline an Executive Officer, including (without limitation) termination of employment, institution of civil proceedings, reporting of misconduct to appropriate governmental authorities, reduction of future compensation opportunities or change in role.

This Policy is in addition to the requirements of Section 304 of the Sarbanes-Oxley Act of 2002 that are applicable to the Company's Chief Executive Officer and Chief Financial Officer and any other applicable regulatory requirements.

Notwithstanding the terms of any of the Company's organizational documents (including, but not limited to, the Company's Bylaws), any corporate policy or any contract (including, but not limited to, any indemnification agreement), the Company will not indemnify any Executive Officer or former Executive Officer against any loss of Excess Compensation. The Company will not pay for or reimburse insurance premiums for an insurance policy that covers potential recovery obligations. In the event the Company is required to recover Excess Compensation from a former Executive Officer pursuant to this Policy, the Company will be entitled to seek such recovery in order to comply with applicable law, regardless of the terms of any release of claims or separation agreement the former Executive Officer may have signed.

This Policy is intended to comply with Section 10D of the Exchange Act, Rule 10D-1 under the Exchange Act, and with the listing standards of the New York Stock Exchange (the "**Exchange**"), the trading platform on which the securities of the Company primarily are listed. This Policy will be interpreted in a manner that is consistent with the requirements of Section 10D of the Exchange Act, Rule 10D-1 under the Exchange Act and with the listing standards of the Exchange, including (but not limited to) any interpretive guidance provided by the Exchange.

Other Important Information

The Compensation Committee or Board may amend and/or terminate this Policy from time to time. Unless otherwise determined by the Compensation Committee, this Policy will terminate upon the Company ceasing to be a listed issuer within the meaning of Section 10D of the Exchange Act.

If any provision of this Policy or the application of any such provision to any Executive Officer shall be adjudicated to be invalid, illegal or unenforceable in any respect, such invalidity, illegality or unenforceability shall not affect any other provisions of this Policy, and the invalid, illegal or unenforceable provisions shall be deemed amended to the minimum extent necessary to render any such provision or application enforceable.

ACKNOWLEDGEMENT

- I acknowledge that I have received, read and understand the Micron Technology, Inc. (the "**Company**") Compensation Recoupment (Clawback) Policy, as amended and restated effective October 2, 2023 (the "**Policy**").

- I agree that the Policy applies to me, and is binding on all of my beneficiaries, heirs, executors, administrators or other legal representatives, and that the Company's right to recovery in order to comply with applicable law will apply, regardless of the terms of any release of claims or separation agreement I have signed or will sign in the future.

- I agree to be bound by and to comply with the Policy and understand that determinations of the Compensation Committee (as such term is used in the Policy) will be final and binding and will be given the maximum deference permitted by law.

- I agree that my current indemnification rights, whether in an individual agreement or the Company's organizational documents, exclude the right to be indemnified for amounts required to be recovered under the Policy.

- I agree that my failure to comply in all respects with the Policy is a basis for termination of my employment with the Company and any affiliate of the Company as well as any other appropriate discipline.

- I understand that neither the Policy, nor the application of the Policy to me, provides a basis for resignation for good reason, constructive termination or any similar concept under any applicable employment agreement or arrangement.

- I understand that if I have questions concerning the meaning or application of the Policy, it is my responsibility to seek guidance from Human Resources or my own personal advisers.

- I agree that neither this Acknowledgement nor the Policy is meant to constitute an employment contract.

Agreed and accepted:

Executive

_____
(*print name*)

_____
(*signature*)

_____
(date)

Exhibit 12

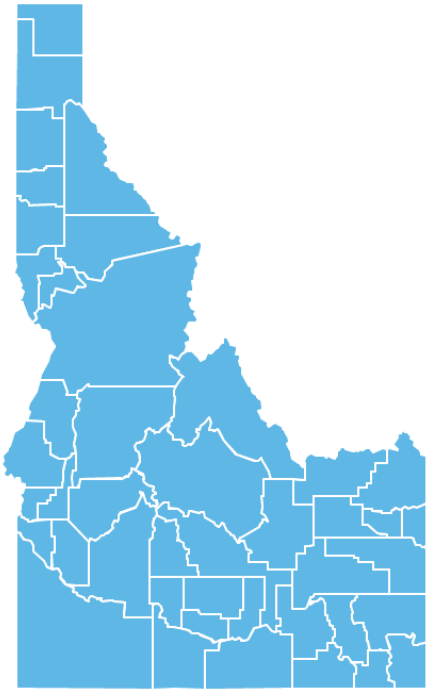


State of Idaho Labor Force And Economic Profile

Last Updated: November 2023

State of Idaho Economic Overview

Civilian Labor Force (Oct 2023)	971,208
Unemployment Rate (Oct 2023)	3.2%
Population (2022)	1,939,033
Median Household Income (2021)	$63,377
Per Capita Personal Income (2021)	$52,369
Poverty Rate (2021)	11.4%



1. Statewide Demographic Characteristics, 2021 5-Year ACS

	State of Idaho	State of Idaho (%)	United States (%)
Total Population	1,811,617	100.0%	329,725,481
Race/Ethnicity			
White, one race	1,567,799	86.5%	68.2%
Black or African American alone, not hispanic	12,242	0.7%	12.6%
Native American alone, not hispanic	22,799	1.3%	0.8%
Asian alone, not hispanic	24,616	1.4%	5.7%
Hispanic or Latino (of any race)	234,561	12.9%	18.4%
Gender			
Male	912,529	50.4%	49.5%
Female	899,088	49.6%	50.5%
Age			
Median age	36.8	-	38.4
Under 18 years	458,830	25.3%	22.5%
Over 18 years	1,352,787	74.7%	77.5%
21 years and over	1,185,197	65.4%	68.3%
Over 65 years	287,098	15.8%	16.0%
Educational Attainment (Population 25 years and over)			
Less than 9th grade	39,820	2.2%	3.3%
High school graduate (with equivalencies)	338,282	18.7%	18.2%
Some college, no degree	296,583	16.4%	13.4%
Associate's degree	126,524	7.0%	6.1%
Bachelor's degree	253,762	14.0%	14.7%
Graduate or professional degree	132,502	7.3%	9.5%
Median Household Income	$63,377	-	$69,021

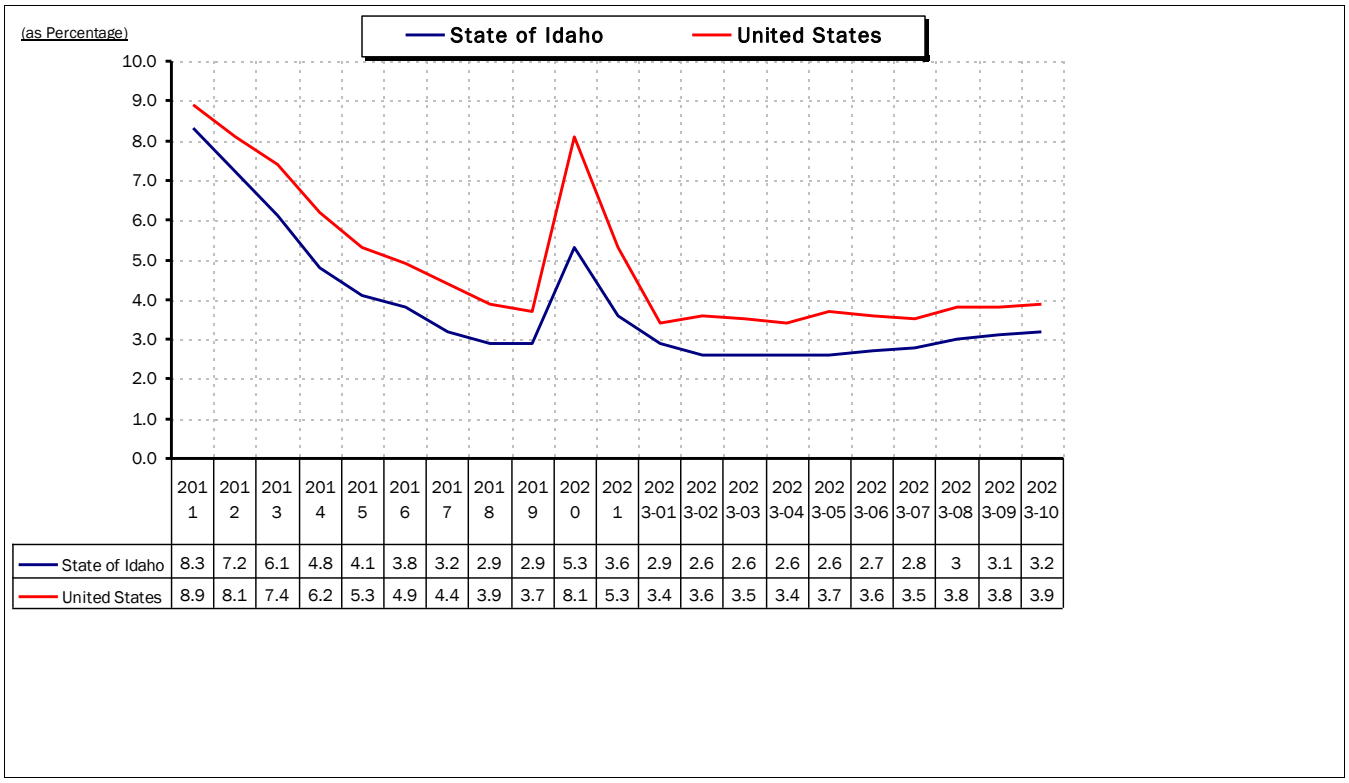
Source: US Census Bureau- American Community Survey 5-Year Estimates

2. Labor Force Growth, October 2022 to October 2023

	Labor Force	Employment	Unemployed	Unemployment Rate
October 2023	971,208	939,743	31,465	3.2%
October 2022	954,969	928,189	26,780	2.8%
YoY % Change	1.7%	1.2%	17.5%	0.4%

Source: Idaho Department of Labor- Local Area Unemployment Statistics (LAUS)

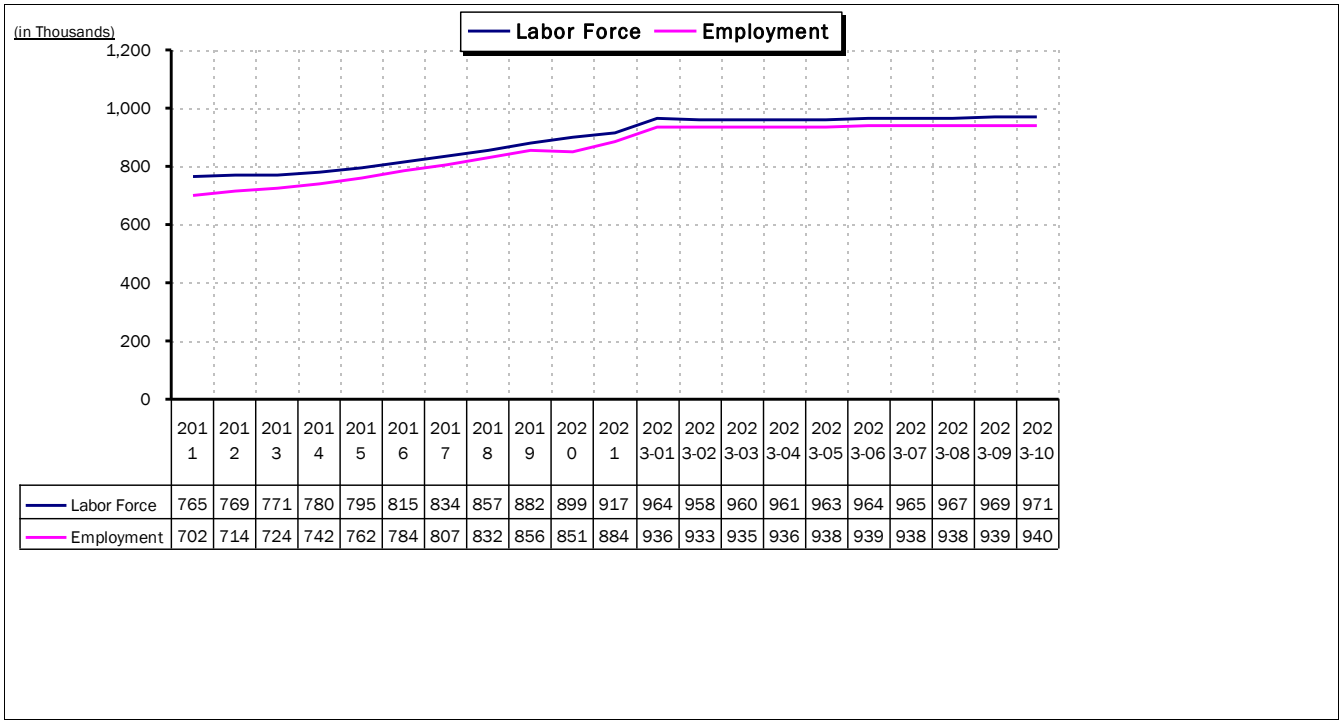
3. Seasonally-Adjusted Unemployment Rate, 2012 to October 2023



	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2023-01	2023-02	2023-03	2023-04	2023-05	2023-06	2023-07	2023-08	2023-09	2023-10
State of Idaho	8.3	7.2	6.1	4.8	4.1	3.8	3.2	2.9	2.9	5.3	3.6	2.9	2.6	2.6	2.6	2.6	2.7	2.8	3	3.1	3.2
United States	8.9	8.1	7.4	6.2	5.3	4.9	4.4	3.9	3.7	8.1	5.3	3.4	3.6	3.5	3.4	3.7	3.6	3.5	3.8	3.8	3.9

Source: Idaho Department of Labor- Local Area Unemployment Statistics (LAUS)

4. Seasonally-Adjusted Labor Force and Employment, 2012 to October 2023



	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2023-01	2023-02	2023-03	2023-04	2023-05	2023-06	2023-07	2023-08	2023-09	2023-10
Labor Force	765	769	771	780	795	815	834	857	882	899	917	964	958	960	961	963	964	965	967	969	971
Employment	702	714	724	742	762	784	807	832	856	851	884	936	933	935	936	938	939	938	938	939	940

Source: Idaho Department of Labor- Local Area Unemployment Statistics (LAUS)

5. Industry Covered Employment and Wages, 2012, 2021, and 2022

Industry Sector	2012		2021		2022	
	Average Employment	Average Wages	Average Employment	Average Wages	Average Employment	Average Wages
Total Covered Wages	605,430	$36,690	790,554	$50,718	807,317	$55,134
Natural Resources and Mining	24,636	$34,355	26,896	$45,743	26,261	$49,802
Construction	29,152	$40,785	58,870	$52,186	62,175	$58,288
Manufacturing	56,082	$50,908	70,192	$67,003	72,224	$71,093
Trade,Transportation, and Utilities	125,700	$34,021	159,720	$47,865	160,757	$52,292
Information	9,825	$44,295	8,771	$73,750	9,627	$80,498
Financial Activities	26,706	$46,221	37,222	$73,839	38,404	$76,313
Professional and Business Services	73,810	$44,104	102,395	$65,692	103,724	$73,668
Education and Health Services	138,879	$35,367	175,678	$47,000	180,004	$50,562
Leisure and Hospitality	62,089	$14,838	85,251	$21,304	88,488	$23,421
Other Services	15,446	$25,705	20,313	$37,326	20,788	$41,890
Public Administration	43,040	$43,877	45,233	$55,074	44,862	$58,985

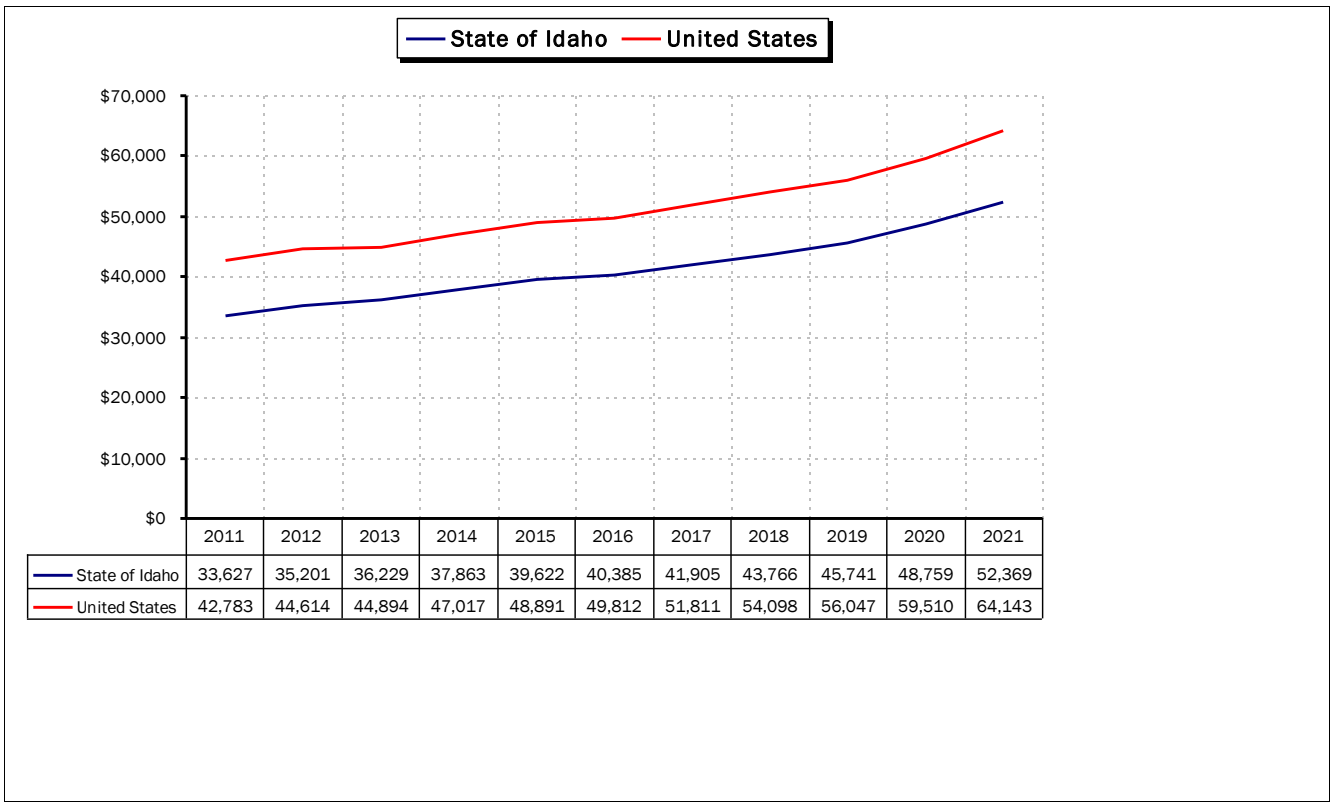
Source: Idaho Department of Labor- Quarterly Census of Employment Wages (QCEW)

6. Top Employers, 2022

Employer	Ownership	Employee Range
St. Luke's Health System	Private	10,000+
Wal-Mart	Private	5,000+
Micron Technology	Private	5,000+
Albertson's Inc.	Private	5,000+
Saint Alphonsus Health System	Private	5,000+
Boise State University	State Government	2,500 - 4,999
Battelle Energy Alliance	Private	5,000+
West Ada School District	Local Government	2,500 - 4,999
Boise School District	Local Government	2,500 - 4,999
Kootenai Health	Local Government	2,500 - 4,999

NOTE: Only employers that have given the Department permission to release employment range data are listed. Source: Idaho Department of Labor- Quarterly Census of Employment Wages (QCEW)

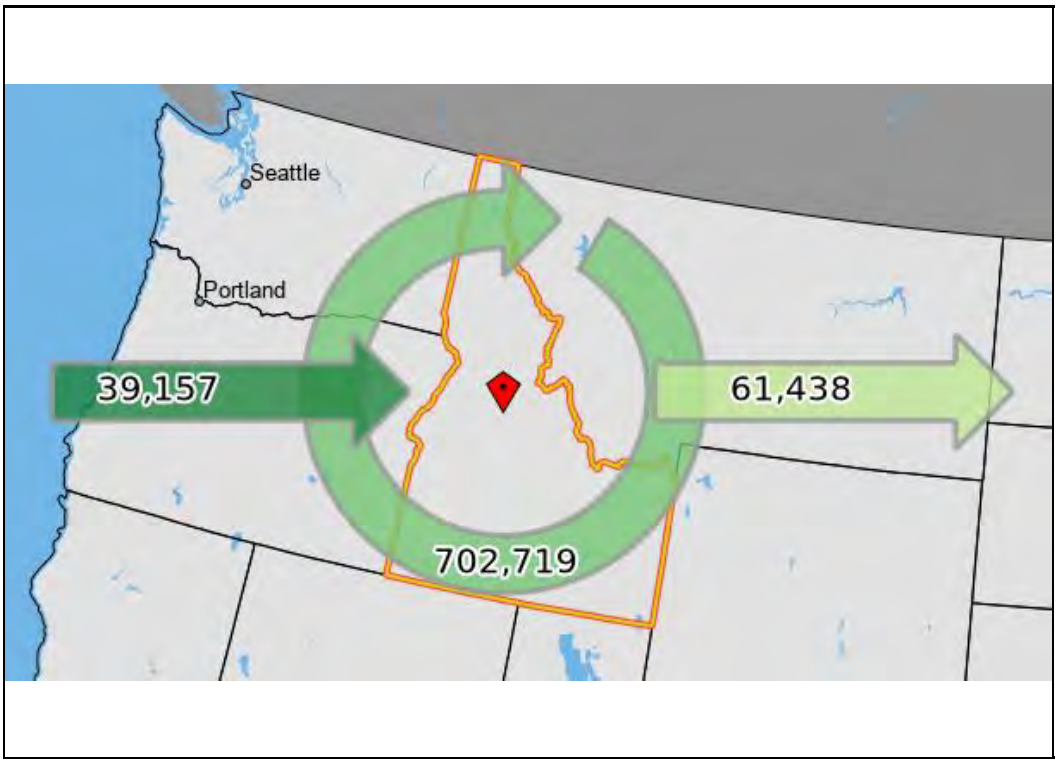
7. Real Per Capita Income, 2011 to 2021



	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021
State of Idaho	33,627	35,201	36,229	37,863	39,622	40,385	41,905	43,766	45,741	48,759	52,369
United States	42,783	44,614	44,894	47,017	48,891	49,812	51,811	54,098	56,047	59,510	64,143

8. Labor Force Commuting Patterns, 2020

It is estimated that 702,719 workers lived and worked in Idaho in 2020. Another 39,157 workers were employed in the State Idaho but lived outside, while 61,438 workers commuted to other States for work.



Source: US Census Bureau

9. Top 10 Cities Where People Who Work in the State of Idaho Live, 2020

City of Residence	Count of All Jobs	Percentage of Total Jobs
Boise City	106,867	14.4%
Meridian	50,267	6.8%
Nampa	42,021	5.7%
Idaho Falls	25,900	3.5%
Caldwell	23,202	3.1%
Pocatello	21,370	2.9%
Twin Falls	19,011	2.6%
Coeur d'Alene	17,928	2.4%
Lewiston	11,478	1.5%
Post Falls	11,152	1.5%

Note: "All Jobs" includes private and public sector jobs. It also includes a count of workers with multiple jobs. Source: US Census Bureau- Longitudinal Employer-Household Dynamics (LEHD)

10. Top 10 Cities Where People Who Live in the State of Idaho Work, 2020

City of Employment	Count of All Jobs	Percentage of Total Jobs
Boise City	172,757	22.6%
Meridian	49,721	6.5%
Idaho Falls	43,823	5.7%
Nampa	38,353	5.0%
Twin Falls	28,267	3.7%
Coeur d'Alene	27,887	3.6%
Pocatello	24,884	3.3%
Caldwell	17,048	2.2%
Rexburg	11,945	1.6%
Lewiston	11,254	1.5%

Note: "All Jobs" includes private and public sector jobs. It also includes a count of workers with multiple jobs. Source: US Census Bureau- Longitudinal Employer-Household Dynamics (LEHD)

For more Information, Contact:

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Exhibit 13

Micron Initiates Construction on Leading-Edge Memory Manufacturing Fab

October 5, 2023 at 5:31 PM EDT

On the 45th anniversary of company's founding, Micron lays the foundation for America's future

Micron to invest $75 million toward building America's semiconductor workforce of the future in Idaho

BOISE, Idaho, Oct. 05, 2023 (GLOBE NEWSWIRE) -- Micron Technology, Inc. (Nasdaq: MU), one of the world's largest semiconductor companies and the only U.S.-based manufacturer of memory, will today celebrate the start of construction on the nation's first new memory manufacturing fab in 20 years. Company executives will join Idaho Governor Brad Little, Boise Mayor Lauren McLean, other community partners and team members to mark the milestone with a ceremonial concrete pour at Micron's Boise headquarters on the 45 th anniversary of the company's founding.

Just over a year ago, Micron announced its plans to invest approximately $15 billion through the end of the decade to construct a new fab for leading-edge memory manufacturing, to be co-located with the company's R&D epicenter in its hometown of Boise. Through the lifespan of the project, Micron will directly infuse $15.3 billion into the Idaho economy and directly spend $13.0 billion with Idaho businesses. The project will create over 17,000 new Idaho jobs, including 2,000 Micron direct jobs, furthering the need for a diverse, highly skilled workforce.

Boise is home to Micron's corporate headquarters, its newly expanded Technology Innovation Center of Excellence and the only DRAM R&D fabrication facility in North America. Nearly two-thirds of Micron's patents are generated from Boise team members — at a rate of more than three patents per day. Co-locating the leading-edge memory manufacturing fab is expected to provide multiple strategic benefits for the company and the U.S. semiconductor industry at large as Micron continues to drive industry leadership.

"We are laying the foundation for Micron's future and charting a path for revitalized U.S. high-tech manufacturing — just a year since we first broke ground here in Boise," said Micron President and CEO Sanjay Mehrotra. "As I reflect on the opportunity ahead, I value all of the incredible Micron team members, who over the last 45 years, have contributed to driving record-breaking innovations and making the Boise community the remarkable place that it is today. Our investments here and in New York will secure domestic memory production in the U.S., meeting the advanced applications of the future's demands for the vast amounts of memory required for fast and efficient data storage and processing."

The Idaho Community Investment Framework, which reflects the shared priorities Micron and its partners have identified to lead inclusive growth across the state, was formalized in May 2023 alongside Governor Little and Mayor McLean. Today, Micron is proud to announce its plans to invest $75 million over the next 10 years toward the Idaho community and workforce development priorities formalized earlier this year. In support of the Community Investment Framework, the State of Idaho and the City of Boise will recognize state and local efforts to bolster the success of new manufacturing in the state.

"On the 45 th anniversary of this iconic Idaho company's founding, it's a pleasure to celebrate the start of construction on the largest private investment ever made in our state," said Governor Little. "Micron is building the foundation for its next decades here in Idaho — with its new fab and its $75 million commitment to the priorities formalized in the Community Investment Framework. Micron and the State of Idaho have a long-standing partnership, and I'm looking forward to our continued cooperation as we pursue a shared goal of further developing Idaho's motivated and capable workforce."

Micron is dedicated to effective and creative workforce development solutions that make careers in the semiconductor industry accessible to all. Decades of investment in Idaho's workforce have driven the innovation that sets Micron apart as a technology leader.

"Today's announcement of Micron's $75 million investment in support of the goals set out in the Community Investment Framework is just the latest example of Micron enhancing and elevating the incredible community we're proud to call home," said Mayor McLean. "In aiming to achieve 100% water reuse, recycling and restoration, as well as use 100% renewable electricity at the new facility, Micron's leadership in keeping Boise a place we can all thrive shines through. The City of Boise and Micron are long-standing partners, and we're excited for the next 45 years."

Cleanroom space in the new fab is expected to come online in phases starting in 2025, with DRAM production ramping over the second half of the decade in line with industry demand growth. Ultimately, the cleanroom space will reach 600,000 square feet — the size of approximately 10 U.S. football fields, and at its completion, the largest single cleanroom ever built in the country.

Micron's Idaho investment plans will be enabled by the anticipated grants and credits provided by the CHIPS and Science Act, which allows projects like Micron's to start construction in the U.S. and be cost-competitive with the rest of the world. Micron filed applications for its Idaho and New York projects with the U.S. Department of Commerce's CHIPS Program Office in August 2023.

About Micron Technology, Inc.
We are an industry leader in innovative memory and storage solutions, transforming how the world uses information to enrich life *for all*. With a relentless focus on our customers, technology leadership and manufacturing and operational excellence, Micron delivers a rich portfolio of high-performance DRAM, NAND and NOR memory and storage products through our Micron® and Crucial® brands. Every day, the innovations that our people create fuel the data economy, enabling advances in artificial intelligence and 5G applications that unleash opportunities — from the data center to the intelligent edge and across the client and mobile user experience. To learn more about Micron Technology, Inc. (Nasdaq: MU), visit micron.com.

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Exhibit 14

Micron Announces Historic Investment of up to $100 Billion to Build Megafab in Central New York

October 4, 2022

Sustainably built and operated, leading-edge memory fab to create nearly 50,000 New York jobs; New Green CHIPS Community Fund to invest $500 million in community and workforce development over time

BOISE, Idaho, Oct. 04, 2022 (GLOBE NEWSWIRE) -- Micron Technology, Inc. (NASDAQ: MU), one of the world's largest semiconductor companies and the only U.S.-based manufacturer of memory, today announced plans to build the largest semiconductor fabrication facility in the history of the United States. The new megafab will increase domestic supply of leading-edge memory and create nearly 50,000 New York jobs, including approximately 9,000 high paying Micron jobs.

Micron intends to invest up to $100 billion over the next 20-plus years to construct a new megafab in Clay, New York, with the first phase investment of $20 billion planned by the end of this decade. This represents the largest private investment in New York state history. Micron's investment in Onondaga County, New York, will complement the company's previously announced high-volume manufacturing fab in Boise, Idaho. Micron will design, build and operate the facility in accordance with its sustainability goals. The site could eventually include four 600,000 square foot cleanrooms, for a total of 2.4 million square feet of cleanroom space – the size of approximately 40 U.S. football fields.

Micron's New York megafab is part of its strategy to gradually increase American-made leading-edge DRAM production to 40% of the company's global output over the next decade. Site preparation work will start in 2023, construction will begin in 2024 and production output will ramp in the latter half of the decade, gradually increasing in line with industry demand trends. Locating Micron's industry-leading DRAM production in the U.S. brings tremendous benefits for its customers, enabling them to build their innovative products and solutions using a more resilient, secure and geographically diverse supply chain.

"I am grateful to President Biden and his Administration for making the CHIPS and Science Act a priority, to Senator Schumer and a bipartisan coalition in Congress for passing the legislation, and to Governor Hochul and County Executive McMahon for the local and state partnerships that made this investment possible. Micron will leverage the diverse, highly educated and skilled talent in New York as we look to build our workforce in the Empire State," said Micron President and CEO Sanjay Mehrotra. "This historic leading-edge memory megafab in Central New York will deliver benefits beyond the semiconductor industry by strengthening U.S. technology leadership as well as economic and national security, driving American innovation and competitiveness for decades to come."

The $5.5 billion in incentives from the state of New York over the life of the project alongside anticipated federal grants and tax credits from the CHIPS and Science Act are critical to support hiring and capital investment. In addition, the Town of Clay and Onondaga County are providing key infrastructure support for Micron's new leading-edge semiconductor facility.

Central New York is the Ideal Home for America's New Leading-Edge Semiconductor Megafab

Micron is excited to build this new megafab in New York, making the Empire State the location of the largest leading-edge memory site in the U.S. Micron selected the Onondaga County, New York site based on its multiple advantages including leading higher education institutions, access to talent traditionally underrepresented in technology jobs and a significant military population aligned with Micron's commitment to veteran hiring. It also offers availability of water and clean, reliable power to enable a project of this scale while achieving our long-term environmental goals. The area has much to offer for future Micron employees and families, including urban and outdoor lifestyles, an affordable cost of living and a strong local school system. New York provides partnership opportunities with local K-12 education programs, community colleges and institutions for top engineering and technical talent. The state has a long history of semiconductor development and manufacturing, providing promising opportunities to collaborate on R&D initiatives with organizations like the Albany NanoTech Complex and the U.S. Air Force Research Laboratory.

Senate Majority Leader Charles Schumer said, "After years of work, it's official—Micron is coming to Central New York! With the CHIPS and Science bill, I wrote and championed as the fuse, Micron's $100 billion investment in Upstate New York will fundamentally transform the region into a global hub for manufacturing and bring tens of thousands of good-paying high-tech and construction jobs to Central New York. This project is a dramatic turning point for a region that has faced decades of lost manufacturing jobs, and, in combination with New York's already robust microchip industry from the Hudson Valley, Albany, and the Mohawk Valley to Binghamton, Rochester, and Buffalo, it will put Upstate New York on the map in a way we haven't seen in generations. This is our Erie Canal moment. Just as the original Erie Canal did centuries ago, this 21st Century Erie Canal will flow through the heart of Central New York and redefine Upstate New York's place in the global economy for generations to come. Micron's investment will make New York's semiconductor corridor into a major engine powering our economy and will supply 'Made in New York' microchips to everything from electric vehicles, 5G, and defense technology to personal computers and smartphones. Today's announcement is the result of my long fight to bring manufacturing back to Upstate New York. The bottom line is that without the CHIPS and Science legislation, Micron would have decided to build its mega-fab overseas. This investment leaves no question that the future of microchip manufacturing will remain not just in this country, but in Syracuse specifically, and that our future will be built in Upstate New York, with Central New York as a global center of the chip industry."

Historic Investment in Community and Workforce Development

Micron and the state of New York are also announcing a historic $500 million investment in community and workforce development with a focus on disadvantaged populations over the duration of the project. Micron will invest $250 million over the next 20-plus years as part of the company's commitment to the Green CHIPS Community Investment Fund. An additional $250 million is expected to be invested, with $100 million from New York and $150 million from local, other state and national partners.

Aimed at expanding and preparing the workforce in the region and providing additional support for disadvantaged community populations, the fund will be used for workforce training, education programs, housing and other community investments. Micron will work with the state and other partners to

form a local Community Advisory Committee to provide inputs into additional future investments from the Fund.

Governor Hochul said, “Micron’s $100 billion investment in New York marks the start of something transformative in scale and possibility for our state’s economic future. I promised that we would jump start the economy by being the most business-friendly and worker-friendly state in the nation, and thanks to our State Green CHIPS legislation, the federal CHIPS and Science Act, and extraordinary partnerships with business, labor, and local and federal leaders, this project will do exactly that. Together, we are leveraging this investment – the largest private-sector investment in state history – to secure our economic future, solidify New York’s standing as a global manufacturing hub, and usher the state into another Industrial Revolution.”

Reflecting the company’s broad DEI commitments, Micron’s New York plans include initiatives to address economic disparities and accelerate economic opportunity for underserved communities in the semiconductor industry. Micron aims to hire a diverse workforce for both direct roles as well as broader construction ecosystem jobs.

Onondaga County Executive McMahon said, “Today’s announcement validates what we have known all along – White Pine Business Park is the premier site in the Country for attracting an investment in the semiconductor industry, and we are thrilled to welcome Micron to our community. This is our generation’s Erie Canal moment and my administration is committed to meeting this pivotal and exciting moment in time. We will make sure that every neighborhood in every corner of the County feels part of this historic and transformational project.” McMahon continued, “As important, this is a project that many people felt we weren’t worthy of, but at the end of the day the greatest memory technology company in the world chose Onondaga County. Micron is going to invest one-hundred billion dollars to not only solve global demand challenges, but to meet national security demands for this country. The decision by Micron to invest in Central New York and solve these problems not only supports our greater strategy for growing our community, but validates our undeniable progress. I look forward to a long and successful partnership.”

Sustainability Initiatives for New York Leading-Edge Megafab

Micron will design and operate its new megafab in line with the company’s sustainability framework and commitments. Micron aims to use 100% renewable electricity at the new facility. Additionally, Micron plans to use green infrastructure and sustainable building attributes for the construction of the New York fab to attain Leadership in Energy and Environmental Design (LEED) Gold status. Greenhouse gas emissions (GHG) for the new facility will be mitigated and controlled by using state-of-the-art technology. These efforts support Micron’s global target to achieve a 42% reduction in GHG emissions from operations by 2030 and net-zero emissions by 2050.

Micron was recently named one of the 2022 World’s Most Ethical Companies , awarded a Ecovadis Sustainability Platinum medal (top 1%) and named one of Newsweek America’s Most Responsible Companies .

For more information, reference the New York fact sheet at Micron.com/NY.

About Micron Technology, Inc.
We are an industry leader in innovative memory and storage solutions transforming how the world uses information to enrich life *for all*. With a relentless focus on our customers, technology leadership, and manufacturing and operational excellence, Micron delivers a rich portfolio of high-performance DRAM, NAND and NOR memory and storage products through our Micron® and Crucial® brands. Every day, the innovations that our people create fuel the data economy, enabling advances in artificial intelligence and 5G applications that unleash opportunities — from the data center to the intelligent edge and across the client and mobile user experience. To learn more about Micron Technology, Inc. (Nasdaq: MU), visit micron.com.

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Exhibit 15

March 26, 2015

Micron and Intel Unveil New 3D NAND Flash Memory

Technology Advancements Enable Three Times More Capacity[1] than Other NAND Technologies

NEWS HIGHLIGHTS

- 3D NAND technology uses floating gate cells and enables the highest-density flash device ever developed-three times higher capacity[1] than other NAND die in production.
- Enables gum stick-sized SSDs with more than 3.5 terabytes (TB) of storage and standard 2.5-inch SSDs with greater than 10TB
- Innovative process architecture techniques extend Moore's Law for flash storage, bringing significant improvements in density while lowering the cost of NAND flash.

Multimedia Elements:

- Media Kit - Micron / Intel

BOISE, Idaho and SANTA CLARA, Calif., March 26, 2015 - Micron Technology, Inc. (Nasdaq: MU), and Intel Corporation today revealed the availability of their 3D NAND technology, the world's highest-density flash memory. Flash is the storage technology used inside the lightest laptops, fastest data centers, and nearly every cellphone, tablet and mobile device.

This new 3D NAND technology, which was jointly developed by Intel and Micron, stacks layers of data storage cells vertically with extraordinary precision to create storage devices with three times higher capacity1 than competing NAND technologies. This enables more storage in a smaller space, bringing significant cost savings, low power usage and high performance to a range of mobile consumer devices as well as the most demanding enterprise deployments.

Planar NAND flash memory is nearing its practical scaling limits, posing significant challenges for the memory industry. 3D NAND technology is poised to make a dramatic impact by keeping flash storage solutions aligned with Moore's Law, the trajectory for continued performance gains and cost savings, driving more widespread use of flash storage.

"Micron and Intel's collaboration has created an industry-leading solid-state storage technology that offers high density, performance and efficiency and is unmatched by any flash today," said Brian Shirley, vice president of Memory Technology and Solutions at Micron Technology. "This 3D NAND technology has the potential to create fundamental market shifts. The depth of the impact that flash has had to date-from smartphones to flash-optimized supercomputing-is really just scratching the surface of what's possible."

"Intel's development efforts with Micron reflect our continued commitment to offer leading and innovative non-volatile memory technologies to the marketplace," said Rob Crooke, senior vice president and general manager, Non-Volatile Memory Solutions Group, Intel Corporation. "The significant improvements in density and cost enabled by our new 3D NAND technology innovation will accelerate solid-state storage in computing platforms."

Innovative Process Architecture
One of the most significant aspects of this technology is in the foundational memory cell itself. Intel and Micron chose to use a floating gate cell, a universally utilized design refined through years of high-volume planar flash manufacturing. This is the first use of a floating gate cell in 3D NAND, which was a key design choice to enable greater performance and increase quality and reliability.

The new 3D NAND technology stacks flash cells vertically in 32 layers to achieve 256Gb multilevel cell (MLC) and 384Gb triple-level cell (TLC) die that fit within a standard package. These capacities can enable gum stick-sized SSDs with more than 3.5TB of storage and standard 2.5-inch SSDs with greater than 10TB. Because capacity is achieved by stacking cells vertically, the individual cell dimensions can be considerably larger. This is expected to increase both performance and endurance and make even the TLC designs well-suited for data center storage.

The key product features of this 3D NAND design include:

- **Large Capacities** -Three times the capacity of existing 3D technology[1]-up to 48GB of NAND per die-enabling three-fourths of a terabyte to fit in a single fingertip-sized package.
- **Reduced Cost per GB** - First-generation 3D NAND is architected to achieve better cost efficiencies than planar NAND.
- **Fast** - High read/write bandwidth, I/O speeds and random read performance.
- **Green** - New sleep modes enable low-power use by cutting power to inactive NAND die (even when other die in the same package are active), dropping power consumption significantly in standby mode.
- **Smart** - Innovative new features improve latency and increase endurance over previous generations, and also make system integration easier.

The 256Gb MLC version of 3D NAND is sampling with select partners today, and the 384Gb TLC design will be sampling later this spring. The fab production line has already begun initial runs, and both devices will be in full production by the fourth quarter of this year. Both companies are also developing individual lines of SSD solutions based on 3D NAND technology and expect those products to be available within the next year.

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Micron Technology, Inc., is a global leader in advanced semiconductor systems. Micron's broad portfolio of high-performance memory technologies-including DRAM, NAND and NOR Flash-is the basis for solid state drives, modules, multichip packages and other system solutions. Backed by more than 35 years of technology leadership, Micron's memory solutions enable the world's most innovative computing, consumer, enterprise storage, networking, mobile, embedded and automotive applications. Micron's common stock is traded on the NASDAQ under the MU symbol. To learn more about Micron Technology, Inc., visit www.micron.com

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[1]Capacity difference based on comparison between Micron and Intel 384 Gb TLC 3D NAND die and other industry 3D NAND TLC

Exhibit 16

US008320181B2

(12) **United States Patent**
Violette

(10) **Patent No.: US 8,320,181 B2**
(45) **Date of Patent: Nov. 27, 2012**

(54) **3D MEMORY DEVICES DECODING AND ROUTING SYSTEMS AND METHODS**

(75) Inventor: **Michael P. Violette**, Boise, ID (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 160 days.

(21) Appl. No.: **12/547,337**

(22) Filed: **Aug. 25, 2009**

(65) **Prior Publication Data**

US 2011/0051512 A1 Mar. 3, 2011

(51) **Int. Cl.**
G11C 11/34 (2006.01)

(52) **U.S. Cl.** **365/185.17**; 365/185.11

(58) **Field of Classification Search** 365/189.17, 365/158.11, 185.01, 185.17, 185.11
See application file for complete search history.

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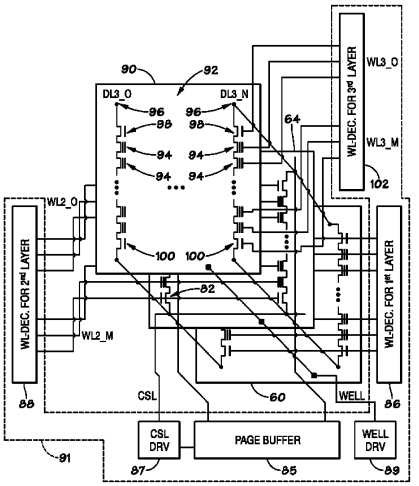
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Primary Examiner — VanThu Nguyen
Assistant Examiner — Khamdan Alrobaie
(74) *Attorney, Agent, or Firm* — Fletcher Yoder

(57) **ABSTRACT**

3D memory devices are disclosed, such as those that include multiple two-dimensional tiers of memory cells. Each tier may be fully or partially formed over a previous tier to form a memory device having two or more tiers. Each tier may include strings of memory cells where each of the strings are coupled between a source select gate and a drain select gate such that each tier is decoded using the source/drain select gates. Additionally, the device can include a wordline decoder for each tier that is only coupled to the wordlines for that tier.

26 Claims, 6 Drawing Sheets



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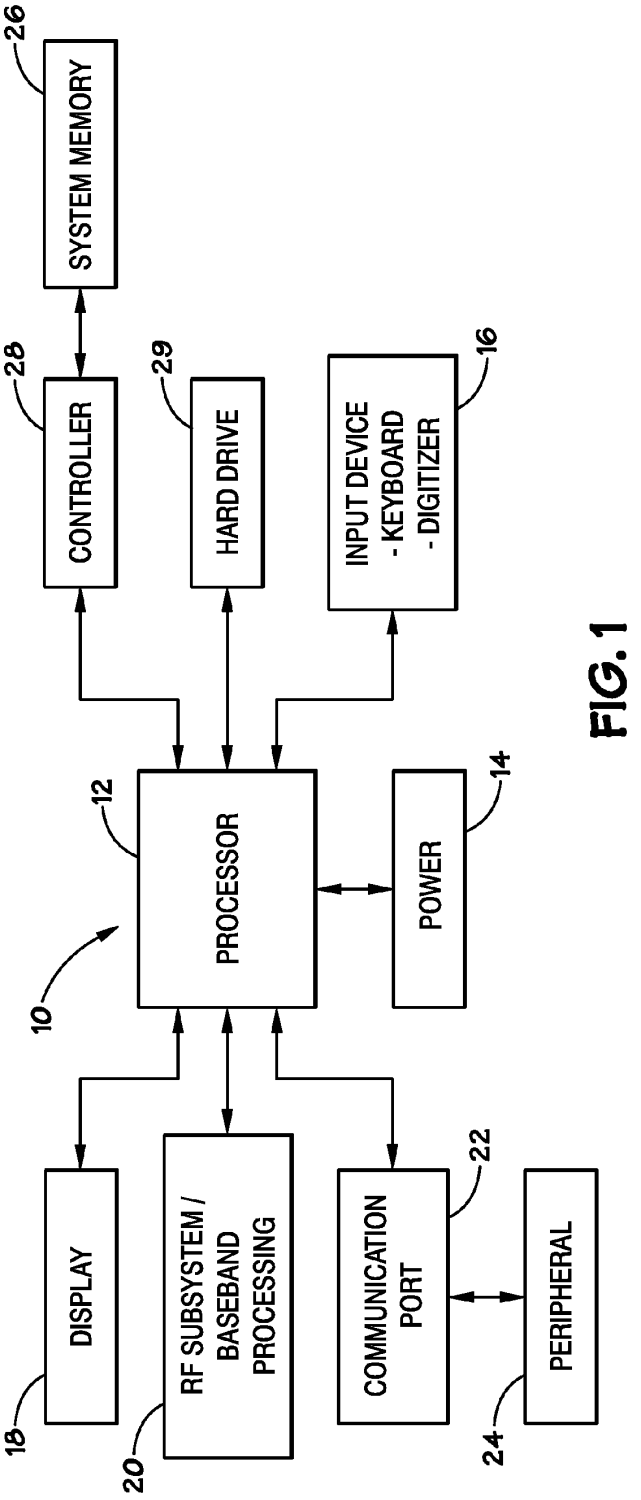

26
SYSTEM MEMORY
28
CONTROLLER
29
HARD DRIVE
16
INPUT DEVICE
- KEYBOARD
- DIGITIZER
12
PROCESSOR
14
POWER
10
18
DISPLAY
20
RF SUBSYSTEM /
BASEBAND
PROCESSING
22
COMMUNICATION
PORT
24
PERIPHERAL

FIG. 1

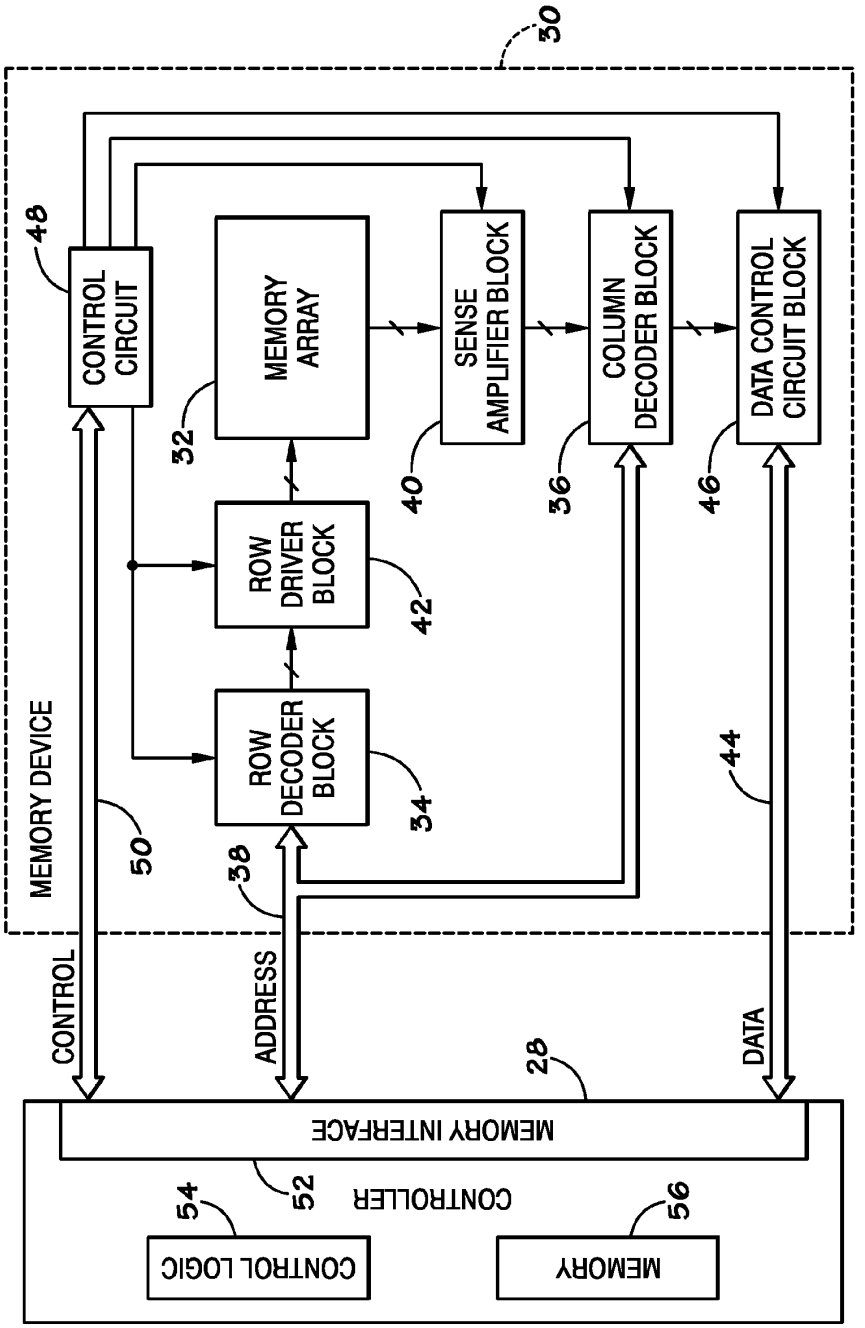

30
48
CONTROL CIRCUIT
MEMORY ARRAY
SENSE AMPLIFIER BLOCK
COLUMN DECODER BLOCK
DATA CONTROL CIRCUIT BLOCK
32
40
36
46
ROW DRIVER BLOCK
42
ROW DECODER BLOCK
34
MEMORY DEVICE
50
38
44
CONTROL
ADDRESS
DATA
28
MEMORY INTERFACE
52
CONTROLLER
54
56
CONTROL LOGIC
MEMORY

FIG. 2

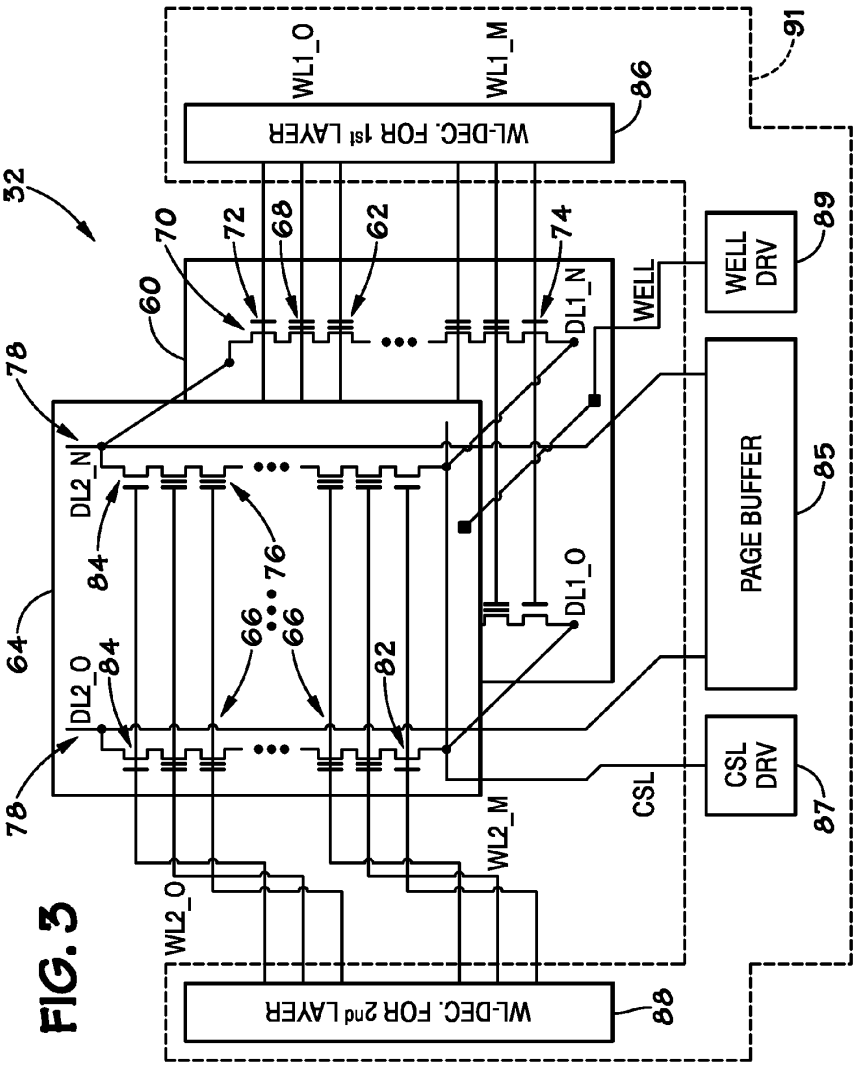
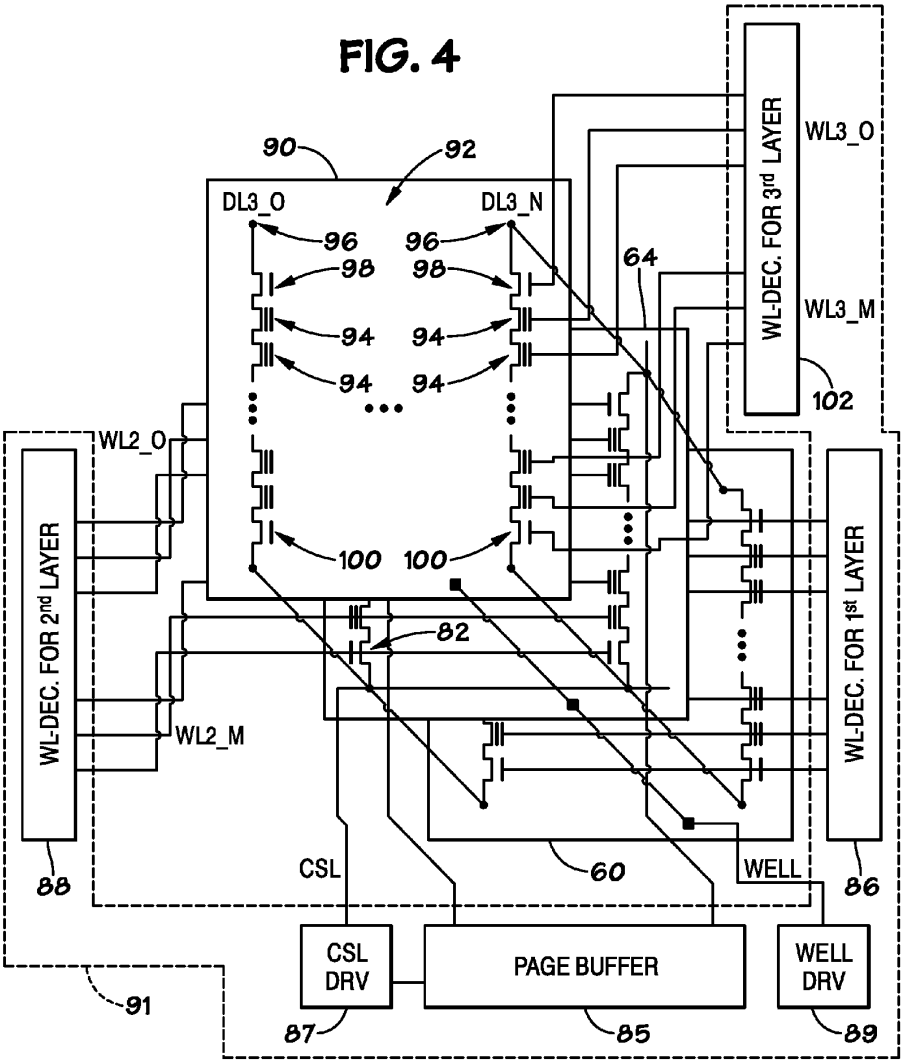

WL1_O
WL1_M
WL-DEC. FOR 1st LAYER
86
91
32
70
72
68
62
74
60
WELL
DL1_N
WELL DRV
89
78
DL2_N
84
76
66
66
82
DL1_O
PAGE BUFFER
85
64
DL2_O
84
78
CSL
CSL DRV
87
WL2_M
WL2_O
WL-DEC. FOR 2nd LAYER
88

FIG. 3

FIG. 4


90
92
DL3_O
DL3_N
96
96
98
98
94
94
94
94
64
WL3_O
WL-DEC. FOR 3rd LAYER
WL3_M
102
WL2_O
WL-DEC. FOR 2nd LAYER
100
100
82
WL2_M
WL-DEC. FOR 1st LAYER
88
CSL
60
WELL
86
CSL DRV
PAGE BUFFER
WELL DRV
91
87
85
89

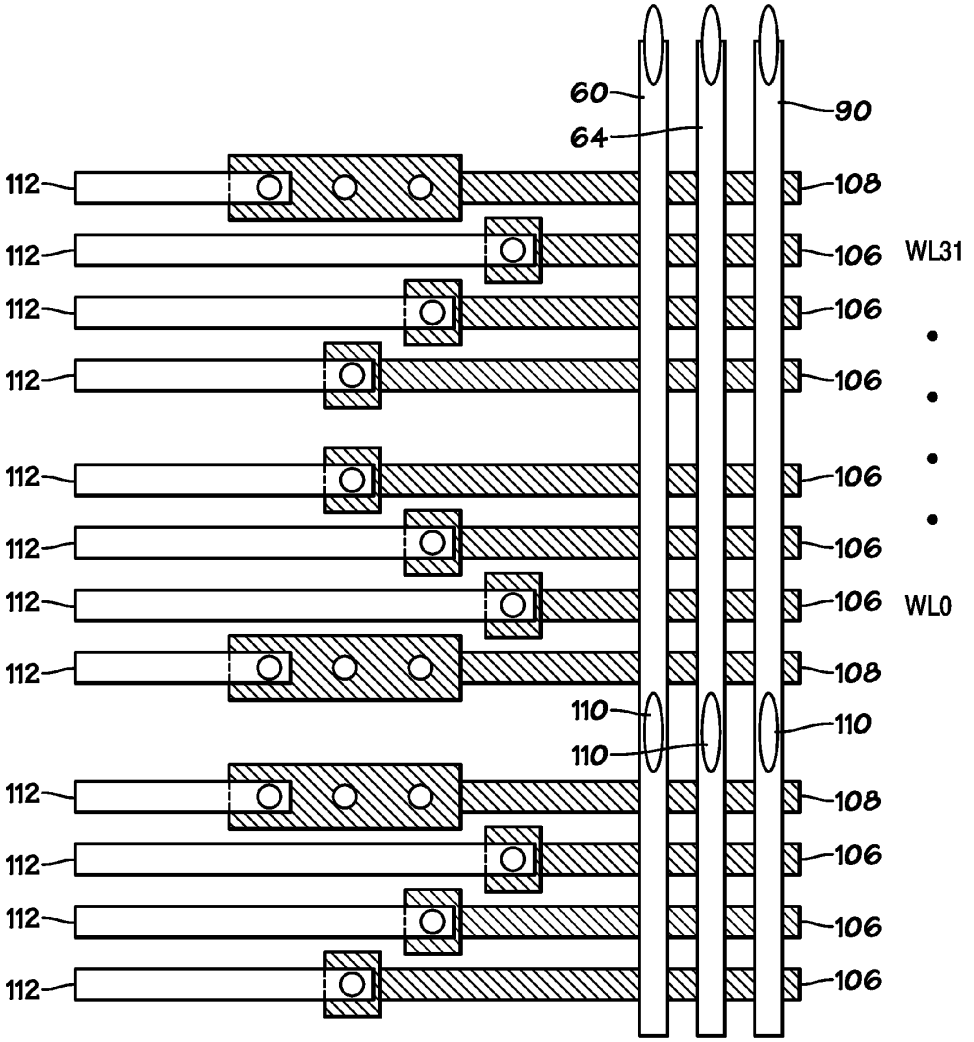


FIG. 5

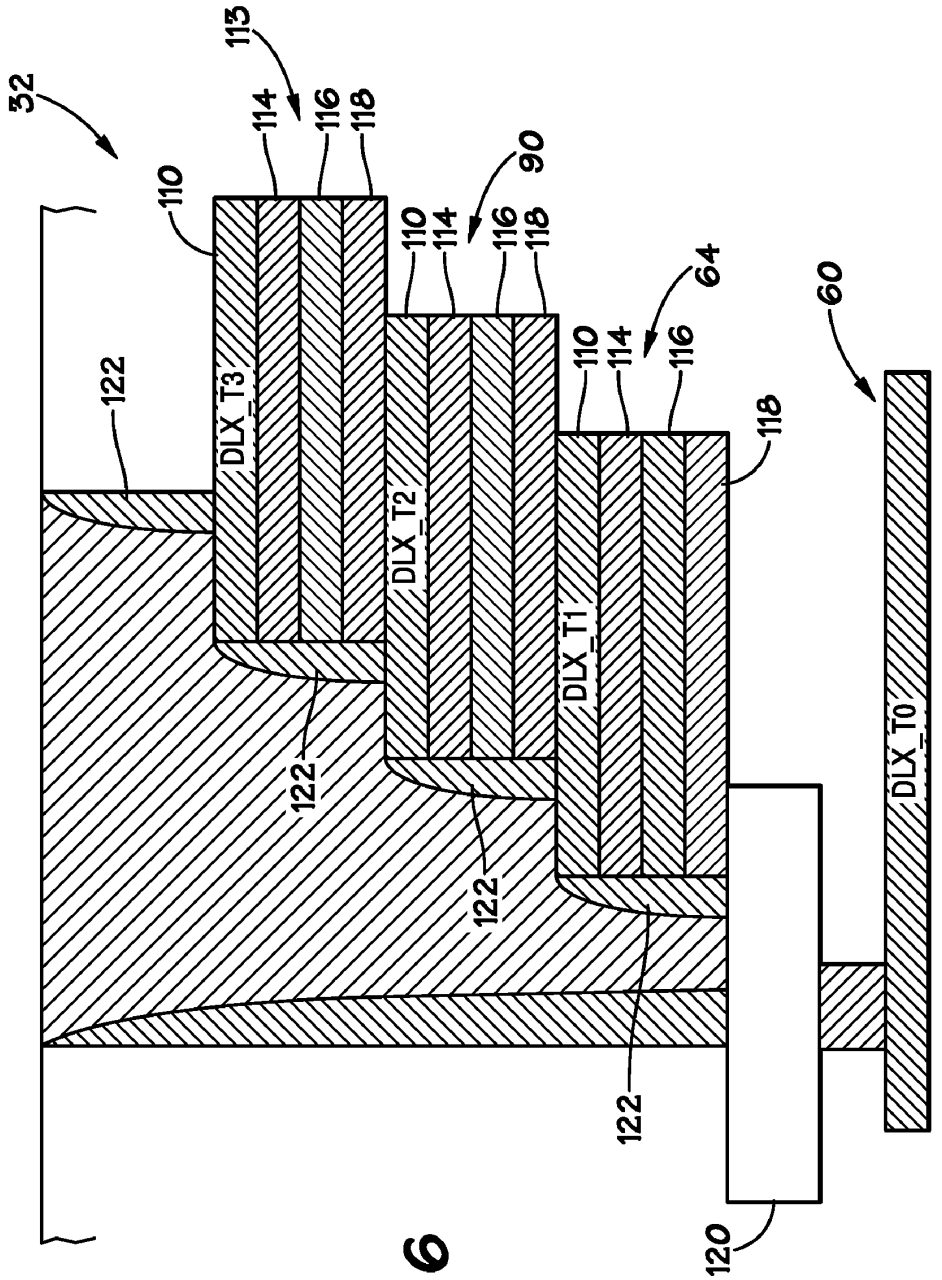

32
113
114
116
118
110
90
110
114
116
118
64
110
114
116
118
60
122
DLX_T3
DLX_T2
DLX_T1
DLX_T0
122
122
122
120

FIG. 6

3D MEMORY DEVICES DECODING AND ROUTING SYSTEMS AND METHODS

BACKGROUND

1. Field of Invention

Embodiments of the invention relate generally to memory devices and, specifically, to non-volatile memory array architectures.

2. Description of Related Art

Electronic systems, such as computers, personal organizers, cell phones, portable audio players, etc., typically include one or more memory devices to provide storage capability for the system. System memory is generally provided in the form of one or more integrated circuit chips and generally includes both random access memory (RAM) and read-only memory (ROM). System RAM is typically large and volatile and provides the system's main memory. Static RAM and Dynamic RAM are commonly employed types of random access memory. In contrast, system ROM is generally small and includes non-volatile memory for storing initialization routines and identification information. Non-volatile memory may also be used for caching or general data storage. Electrically-erasable read only memory (EEPROM) is one commonly employed type of read only memory, wherein an electrical charge may be used to program data in the memory.

One type of non-volatile memory that is of particular use is a flash memory. A flash memory is a type of EEPROM that can be erased and reprogrammed in blocks. Flash memory is often employed in personal computer systems in order to store the Basic Input Output System (BIOS) program such that it can be easily updated. Flash memory is also employed in portable electronic devices, such as wireless devices, because of the size, durability, and power requirements of flash memory implementations. Various types of flash memory may exist, depending on the arrangement of the individual memory cells and the requirements of the system or device incorporating the flash memory. For example, NAND flash memory is a common type of flash memory device.

In some architectures, flash memory stores information in an array of floating gate transistors, called "cells", each of which traditionally stores one bit of information that is represented as a "0" or a "1". In other architectures, each cell may store more or less digits of information, such as in multi-level cell (MLC) flash or when a state of a cell may be used to represent a non-integer value. The memory device often includes a grid-like arrangement of the cells. Each of the cells in the grid consumes a given amount of area and is spaced from one another by a generally uniform distance (e.g., pitch). Accordingly, the size and the pitch of the cells directly contribute to the overall size of the memory device. This becomes more evident as the number of cells and associated storage capacity of memory devices increase.

As technology continues to advance, it is often desirable that memory devices decreases in size. Smaller memory devices can be employed in smaller spaces and/or can increase storage capacity in a limited area or volume. One technique for reducing the memory device size may include stacking memory cells in a vertical arrangement (creating a "3D" architecture). As the cells and associated transistors are scaled and densities of such devices increase, manufacture and functionality of such devices may introduce challenges with respect to contacts and signaling for the cells of this 3D architecture.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** illustrates a block diagram of an embodiment of a processor-based device having a memory that includes memory devices in accordance with embodiments of the present invention;

FIG. **2** illustrates a block diagram of an embodiment of a flash memory device having a memory array in accordance with embodiments of the present invention;

FIG. **3** is a schematic diagram of a 3D array having two tiers in accordance with an embodiment of the present invention;

FIG. **4** is schematic diagram of a 3D array having three tiers in accordance with an embodiment of the present invention;

FIG. **5** is a cross-sectional diagram of the 3D array of FIG. **4** in accordance with an embodiment of the present invention;

FIG. **6** is a cross-sectional view of the digitlines of a 3D array in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

FIG. **1** is a block diagram depicting an embodiment of a processor-based system, generally designated by reference numeral **10**. The system **10** may be any of a variety of types such as a computer, pager, cellular phone, personal organizer, portable audio player, control circuit, camera, etc. In a typical processor-based device, a processor **12**, such as a microprocessor, controls the processing of system functions and requests in the system **10**. Further, the processor **12** may comprise a plurality of processors that share system control.

The system **10** typically includes a power supply **14**. For instance, if the system **10** is a portable system, the power supply **14** may advantageously include permanent batteries, replaceable batteries, and/or rechargeable batteries. The power supply **14** may also include an AC adapter, so the system **10** may be plugged into a wall outlet, for instance. The power supply **14** may also include a DC adapter such that the system **10** may be plugged into a vehicle cigarette lighter, for instance.

Various other devices may be coupled to the processor **12**, depending on the functions that the system **10** performs. For instance, an input device **16** may be coupled to the processor **12**. The input device **16** may include buttons, switches, a keyboard, a light pen, a stylus, a mouse, and/or a voice recognition system, for instance. A display **18** may also be coupled to the processor **12**. The display **18** may include an LCD, a CRT, LEDs, and/or an audio display, for example.

Furthermore, an RF sub-system/baseband processor **20** may also be coupled to the processor **12**. The RF sub-system/baseband processor **20** may include an antenna that is coupled to an RF receiver and to an RF transmitter (not shown). A communications port **22** may also be coupled to the processor **12**. The communications port **22** may be adapted to be coupled to one or more peripheral devices **24** such as a modem, a printer, a computer, or to a network, such as a local area network, remote area network, intranet, or the Internet, for instance.

Generally, the memory is coupled to the processor **12** to store and facilitate execution of various programs. For instance, the processor **12** may be coupled to system memory **26** through a controller **28**. The system memory **26** may include volatile memory, such as Dynamic Random Access Memory (DRAM) and/or Static Random Access Memory (SRAM). The system memory **26** may also include non-volatile memory, such as read-only memory (ROM), PC-RAM, silicon-oxide-nitride-oxide-silicon (SONOS)

memory, metal-oxide-nitride-oxide-silicon (MONOS) memory, polysilicon floating gate based memory, and/or other types of flash memory of various architectures (e.g., NAND memory, NOR memory, etc.) to be used in conjunction with the volatile memory.

As described further below, the system memory **26** may include one or more memory devices, such as flash memory devices, that may be fabricated and operated in accordance with embodiments of the present invention. Such devices may be referred to as or include solid state drives (SSD's), MultiMediaMediaCards (MMC's), SecureDigital (SD) cards, CompactFlash (CF) cards, or any other suitable device. Further, it should be appreciated that such devices may couple to the system **10** via any suitable interface, such as Universal Serial Bus (USB), Peripheral Component Interconnect (PCI), PCI Express (PCI-E), Small Computer System Interface (SCSI), IEEE 1394 (Firewire), or any other suitable interface. To facilitate operation of the system memory **26**, such as the flash memory devices, the system **10** may include a memory controller **28**, as described in further detail below. As will be appreciated, the memory controller **28** may be an independent device or it may be integral with the processor **12**. Additionally, the system **10** may include a hard drive **29**, such as a magnetic storage device.

FIG. **2** is a block diagram illustrating a flash memory device **30** that may be included as a portion of the system memory **26** of FIG. **1**. FIG. **2** also depicts the memory controller **28** coupled to the memory device **30**. The flash memory device **30** can include a 3D memory array **32** having multiple tiers of memory cells (as illustrated below in FIGS. **3** and **4**). The memory array **32** generally includes many rows and columns of conductive traces arranged in a grid pattern to form a number of memory cells. The lines used to select cells in the memory array **32** are generally referred to herein as "access lines", and are referred to in the industry as "wordlines." The lines used to sense (e.g., read) the cells are generally referred to herein as "digit lines," which are often referred to in the industry as "bit lines." The size of the memory array **32** (i.e., the number of memory cells) will vary depending on the size of the flash memory device **30**.

To access the memory array **32**, a row decoder block **34** and a column decoder block **36** are provided and are configured to receive and translate address information from the controller **28** via the address bus **38** to access a particular memory cell in the memory array **32**. In some embodiments, the address and data information may be multiplexed and provided on the same bus. As discussed in more detail below, each group of wordlines for a tier of the memory array **32** may be decoded by a separate row decoder. A sense block **40**, such as one having a plurality of sense amplifiers, is also provided between the column decoder **36** and the memory array **32** to sense (and in some cases amplify) individual values stored in the memory cells. Further, a row driver block **42** is provided between the row decoder block **34** and the memory array **32** to activate a selected word line in the memory array according to a given row address.

During read and program operations, such as a write operation, data may be transferred to and from the flash memory device **30** from the controller **28** via the data bus **44**. The coordination of the data and address information may be conducted through a data control circuit block **46**. Finally, the flash memory device **30** may include a control circuit **48** configured to receive control signals from the controller **28** via the control bus **50**. The control circuit **48** is coupled to each of the row decoder block **34**, the column decoder block **36**, the sense block **40**, the row driver block **42** and the data control circuit block **46**, and is generally configured to coordinate timing and control among the various circuits in the flash memory device **30**.

As mentioned above, the controller **28** provides control signals over the control bus **50**, address signals via the address bus **38**, and data via the data bus **44**, to the memory device **30**. As mentioned above, in some embodiments, the address signals and data may be multiplexed and provided on a single bus. The controller **28** may include a memory interface **52**, control logic **54**, memory **56** (such as registers) and striping and error control logic **58**. The memory interface **52** enables the controller **28** to communicate with the memory device **30**. The control logic **54** processes incoming requests and data, such as from the processor **12**, and provides signals to the memory device **30** to perform the requests.

FIG. **3** is a schematic diagram of one potential embodiment 3D array **32** in accordance with an embodiment of the present invention. As shown in FIGS. **3** and **4**, the 3D array **32** may include two, three, or more tiers. Each tier may include one or more layers used to form a horizontal array of memory cells. As described below, a single tier may include memory cells logically arranged in rows and columns in the horizontal plane of the array. In some embodiments, the memory cells may be single-level cells (SLC), multi-level cells (MLC), or any other suitable memory element.

The 3D array **32** may include a first tier **60** having a first two-dimensional plane of memory cells **62**. A second tier **64** may be fully or partially formed over the first tier **60** in a direction perpendicular to the plane of the first tier **60**. The second tier **64** includes a second two-dimensional plane of memory cells **66**.

The first tier **60** includes word lines WL**1**_**0**-WL**1**_M and intersecting local digit lines DL**1**_**0**-DL**1**_N. The first tier **60** includes a memory cell, such as a floating gate transistor **68**, located at each intersection of a word line (WL) and a string of memory cells coupled to a digit line (DL). The floating gate transistors **68** serve as non-volatile memory cells for storage of data in the memory array **32**. As will be appreciated, each floating gate transistor **68** includes a source, a drain, a floating gate, and a control gate. The control gate of each floating gate transistor **68** is coupled to (and in at least some cases form) a respective local word line (WL). The floating gate transistors **68** are connected in series, source to drain, to form NAND strings **70**, which are each formed between respective select gates. Specifically, each of the NAND strings **70** are formed between a local drain select gate **72** and a local source select gate **74**. The drain select gates **72** and the source select gates **74** may each comprise a field-effect transistor (FET), for instance. A "column" of the first tier **60** includes a NAND string **70** and the source select gate **74** and drain select gate **72** connected thereto. A "row" of the floating gate transistors **68** are those transistors commonly coupled to a given access line, such as a word line (WL). As used herein, the terms "row" and "column" are used to describe the logical arrangement of the embodiment depicted in FIG. **3** and are not limiting to any specific physical arrangement. For example, in other embodiments a "rows" and/or "column" may include a stagger or other non linear arrangement, or the "rows" may not necessarily be perpendicular to the "columns" or vice-versa.

The second tier **64** includes word lines WL**2**_**0**-WL**2**_M and intersecting local digit lines DL**2**_**0**-DL**2**_N. Similar to the first tier **60**, the second tier **64** includes a memory cell, such as a floating gate transistor **76**, located at each intersection of a wordline (WL) and a string of memory cells coupled to a digitline (DL). The control gate of each floating gate transistor **76** is coupled to (and in at least some cases form) a respective local word line (WL). The floating gate transistors

76 may be connected in series, source to drain, to form NAND strings 78 formed between respective select gates. Each of the NAND strings 78 are formed between a local drain select gate 84 and a local source select gate 82. The drain select gates 84 and the source select gates 82 may each comprise a field-effect transistor (FET), for instance. A "column" of the second tier 64 includes a NAND string 78 and the source select gate 82 and drain select gate 84 connected thereto. A "row" of the floating gate transistors 76 are those transistors commonly coupled to a given access line, such as a word line (WL).

As shown in FIG. 3, each group of parallel wordlines for a tier are decoded together. The wordlines WL1_0-WL1_M of the first tier 60 are coupled to a first wordline decoder 86. The first wordline decoder 86 only decodes wordlines coupled to floating gate transistors 68 of the first tier 60. As also shown in FIG. 3, the wordlines WL2_0 and WL2_M are coupled to a second wordline decoder 88. The second wordline decoder 88 is only coupled to the wordlines of the floating gate transistors 76 of the second tier 64. As also shown in FIG. 3, the digitlines DL0 through DLN are coupled to a page buffer 85. In some embodiments, as described below, the decoders 86 and 88 may be in a single tier or base of the device 32. In other embodiments, each wordline decoder 86 and 88 may be a part of, e.g., in the same horizontal structure as, the respective tier. For example, the wordline decoder 86 may a part of the first tier 60 and the wordline decoder 88 may be a part of the second tier 64.

The wells (e.g., a p-well) of both the first tier 60 and the second tier 64 may be coupled together and to a well driver 89. As shown in FIG. 3, the contact for the well driver 89 may extend at least partially through the second tier 64 and the first tier 60 to the well driver 89.

Each tier of the array 32 may be uniquely accessed using the source and drain select gates of a selected tier. For example, the source select gates 82 of the second tier 64 may be used to couple the NAND strings of the second tier to a common source line (CSL) and CSL driver 87. The drain select gates 84 of the second tier may be used to couple the NAND strings of the second tier 64 to respective digitlines DL2_0 through DL2_N. The source select gates 74 of the first tier may also be used to couple the NAND strings of the first tier 60 to the common source line and the CSL driver 87, as a contact(s) that extend at least partially through the second tier 64 and the first tier 60 and couples, for example, the sources of the source select gates 82 to the sources of the source select gates 74. Thus, a contact couples each source select gate of the second tier 64 to a corresponding source select gate of the first tier 60. Each tier 60 and 64 may be uniquely selected by activating the select gates of a desired tier, i.e., by activating the source select gates of a desired tier via respective source select line (SSL) and activating the drain select gates of the desired tier via a respective drain select line (DSL). Any or all of the row and column decode circuitry, e.g., the wordline decoders, the page buffer, drivers, etc., may be located on a base logic substrate 91. The tiers 60 and 64 are disposed on the base logic substrate, such that the first tier 60 is disposed on the base logic substrate 91 and the second tier 64 is disposed on the first tier 60 in the manner described above. Thus, the connections described above, e.g., between wordlines and the wordline decoders 88 and 86 and/ the digitlines and page buffer 85, may electrically connect each tier 60 and 64 to the base logic substrate 91.

FIG. 4 is a schematic of another potential embodiment of the 3D array 32 illustrating a third tier 90 in accordance with an embodiment of the present invention. The 3D array 32 may include the first tier 60 and the second tier 64 described above. The third tier 90 includes a third two-dimensional plane of memory cells 92. As noted above, the memory cells 92 may be SLC memory elements, MLC memory elements, or any other suitable memory element.

The third tier 90 may be partially or fully formed over the second tier 64. The third tier 90 includes word lines WL3_0-WL3_M and intersecting local digit lines DL3_0-DL3_N. The third tier 90 includes a memory cell, such as a floating gate transistor 94, located at each intersection of a word line (WL) and a string of memory cells coupled to a digit line (DL).

The floating gate transistors 94 can be connected in series, source to drain, to form NAND strings 96 formed between respective select gates. Each of the NAND strings 96 are formed between a local drain select gate 98 and a local source select gate 100, which may each comprise a field-effect transistor (FET), for instance. A "column" of the first tier 90 includes a NAND string 96 and the source select gate 100 and drain select gate 98 connected thereto. A "row" of the floating gate transistors 94 are those transistors commonly coupled to a given access line, such as a word line (WL).

The digitlines of the third tier 90 are coupled to the page buffer 85. The wordlines WL3_0-WL3_N of the first tier 90 are coupled to a third wordline decoder 102. The third wordline decoder 102 only decodes wordlines coupled to floating gate transistors 94 of the first tier 90. Similarly, as described above with regard to the first and second tiers 60 and 64, the well contact extends through to the third tier 90, coupling the well of the third tier 90, second tier 64, and first tier 60 to the well driver 89. The wordline decoder 102 may a part of, e.g., of the same horizontal structure as, the third tier 90.

As in the embodiment depicted in FIG. 3, each tier of the array 32 can be uniquely decoded using the source and drain select gates of that tier. The source select gates 100 of the third tier 90 can also be used to couple the NAND strings 96 of the third tier to a common source line and the CSL driver 87. As mentioned above, a source line contact may extend at least partially through the third tier 90, the second tier 64, and the first tier 60, coupling the sources of the source select gates of each tier to the common source line (CSL) and CSL driver 87. The drains of the drain select gates 98 of the third tier 90 are coupled to respective digitlines and the page buffer 85. For example, the drains of the drain select gates 98 can be coupled to the drains of drain select gates 84 and 72 by digit line contacts extending at least partially through the third tier 90, second tier 64, and first tier 60. Thus, the digitline contacts couple the digitlines of each tier to the page buffer 85. Thus, each tier 90, 62, and 60 may be uniquely selected by activating the select gates for a desired tier. As described above, the row and column decode logic may all reside in the base logic substrate 91. Thus, the connections between the wordlines of the third tier 90 and the third wordline decoder 102 may electrically couple the wordlines of the third tier to the third wordline decoder 102.

FIG. 5 is a cross-sectional diagram showing the 3D array 32 in accordance with an embodiment of the present invention. FIG. 5 depicts wordlines 106 extending at least partially through one or more of the tiers 60, 64, and 90, select gate lines 108, and digitlines 110. Each of the wordlines 106 and select gate lines 108 may be coupled to an appropriate driver via conductors 112.

FIG. 6 depicts a cross-sectional diagram of the digitlines of the tiers of the 3D NAND array 32 in accordance with an embodiment of the present invention. As depicted in FIG. 6, the 3D NAND array 32 includes the first tier 60, the second tier 64, and the third tier 90. Additionally, a fourth tier 113 is shown disposed on the third tier 90. As discussed above, the

array **32** may include digitline conductors **110** in each tier, e.g., DLX_T**0**, DLX_T**1**, DLX_T**2**, and DLX_T**3** (for the fourth tier **113**).

The digitline conductors **110** provide contact between the digitline for that tier and a base logic substrate that provides the decoding logic. Also shown in each tier of FIG. **6** are a field oxide layer **114**, a silicon layer **116**, and a bonding oxide layer **118**. Each tier may be bonded to the previous tier by Smart Cut or any suitable bonding technique. A final conductor **120** is also depicted to enable contact between the digitline conductors **110** and the underlying base logic substrate. An insulating spacer **122** may be provided to isolate each digitline conductor **110** of a tier from the silicon substrate layer. For example, as shown in FIG. **6**, one of the insulating spacers electrically insulates the digitline conductors DLX_T**1** from the silicon substrate layer of the second tier **64**.

While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

What is claimed is:

1. A memory array, comprising:

a first tier comprising a first plurality of memory cells, a first plurality of source select gates, and a first plurality of drain select gates, wherein a string of memory cells of the first tier comprises one or more of the plurality of memory cells disposed between one of the plurality of source select gates and one of the plurality of drain select gates;

a second tier formed at least partially over the first tier and comprising a second plurality of memory cells, a second plurality of source select gates, and a second plurality of drain select gates, wherein each of a string of memory cells of the second tier comprises one or more of the second plurality of memory cells disposed between one of the second plurality of source select gates and one of the second plurality of drain select gates;

a first contact extending at least partially through the first tier and the second tier, the first contact coupling the first plurality of source select gates to the second plurality of source select gates and to a common source line;

wherein the first tier comprises a first plurality of digitlines, wherein each of the first plurality of drain select gates is coupled to a respective one of the first plurality of digitlines, and wherein each of the first plurality of digitlines is coupled to a respective one of a second plurality of contacts adjacent to the first tier and the second tier and each of the first plurality of digitlines is laterally insulated from a respective one of the second plurality of contacts by an insulator disposed between a horizontal end of each of the first plurality of digitlines and the respective one of the second plurality of contacts; and

wherein the second tier comprises a second plurality of digitlines, wherein each of the second plurality of drain select gates is coupled to a respective one of the second plurality of digitlines, and wherein each of the second plurality of digitlines is coupled to a respective one of the second plurality of contacts and each of the second plurality of digitlines is laterally insulated from a respective one of the second plurality of contacts by an insulator disposed between a horizontal end of each of the second plurality of digitlines and the respective one of the second plurality of contacts.

2. The memory array of claim **1**, wherein the first plurality of digitlines and the second plurality of digitlines are coupled to a page buffer.

3. The memory array of claim **1**, wherein the first plurality of source select gates and the second plurality of source select gates are coupled to a common source line driver via the common source line.

4. The memory array of claim **1**, wherein the first tier and the second tier are coupled to a well contact that extends at least partially through the first tier and the second tier.

5. The memory array of claim **4**, wherein the well contact is coupled to a well driver.

6. The memory array of claim **1**, further comprising a third tier at least partially over the second tier and comprising a third plurality of memory cells, a third plurality of source select gates, and a third plurality of drain select gates, wherein a string of memory cells of the third tier comprises one or more of the third plurality of memory cells disposed between one of the third plurality of source select gates and one of the third plurality of drain select gates; wherein the first contact also couples the third plurality of source select gates to the common source line.

7. The memory array of claim **6**, wherein the first contact further extends at least partially through the first tier, the second tier, and the third tier.

8. The memory array of claim **6**, wherein the third tier comprises a third plurality of digitlines, wherein each of the third plurality of drain select gates is coupled to a respective one of the third plurality of digitlines, and wherein each of the third plurality of digitlines is coupled to a respective one of the second plurality of contacts adjacent to the first tier, the second tier, and the third tier and each of the third plurality of digitlines is laterally insulated from the second plurality of contacts.

9. A memory array, comprising:

a first tier comprising a first plurality of memory cells, a first plurality of source select gates, a first plurality of drain select gates, a first plurality of digitlines, a first plurality of digitline conductors each coupled to a respective one of the first plurality of digitlines, and a first plurality of insulating spacers disposed between a horizontal end of each of the first plurality of digitlines and a respective one of the first plurality of digitline conductors;

a second tier at least partially over the first tier and comprising a second plurality of memory cells, a second plurality of source select gates, a second plurality of drain select gates, a second plurality of digitlines, a second plurality of digitline conductors each coupled to a respective one of the second plurality of digitlines, and a second plurality of insulating spacers disposed between a horizontal end of each of the second plurality of digitlines and a respective one of the second plurality of digitline conductors;

a first decoder;

a first plurality of access lines coupled to the first plurality of memory cells of the first tier and to the first decoder;

a second decoder; and

a second plurality of access lines coupled to the second plurality of memory cells of the second tier and to the second decoder.

10. The memory array of claim **9**, wherein the first decoder only decodes the first plurality of access lines.

11. The memory array of claim **9**, wherein the second decoder only decodes the second plurality of access lines.

12. The memory array of claim 9, wherein the each of the first plurality of memory cells comprise a floating gate and a control gate.

13. The memory array of claim 9, wherein the each of the second plurality of memory cells comprise a floating gate and a control gate.

14. The memory array of claim 9, wherein the first plurality of source select gates and the first plurality of drain select gates comprise field effect transistors.

15. The memory array of claim 9, wherein the second plurality of source select gates and the second plurality of drain select gates comprise field effect transistors.

16. The memory array of claim 9, comprising a third tier at least partially over on the second tier and comprising a third plurality of memory cells, a third plurality of source select gates, and a third plurality of drain select gates.

17. The memory array of claim 16, comprising a third decoder and a third plurality of access lines coupled to the third tier and the third decoder.

18. The memory array of claim 17, wherein the third decoder only decodes the third plurality of wordlines.

19. The memory array of claim 9, comprising a contact coupled to each of the first plurality of source select gates and each of the second plurality of source select gates.

20. A system, comprising:

a memory controller;

a memory device coupled to the memory controller and comprising:

a memory array comprising:

a first tier comprising a first plurality of memory cells, wherein the first tier is accessed via a first plurality of source select gates of the first tier, a first plurality of drain select gates of the first tier, and a first plurality of digitlines each coupled to a respective one of the first plurality of drain select gates, wherein the first plurality of source select gates are coupled to a first contact extending at least partially through the first tier and a second tier, and the first plurality of digitlines are coupled to a respective one of a second plurality of contacts adjacent to the first tier and the second tier, wherein the first plurality of digitlines are laterally insulated from the second plurality of contacts by an insulator disposed between a horizontal end of each of the first plurality of digitlines and the respective one of the second plurality of contacts;

the second tier comprising a second plurality of memory cells, wherein the second tier is accessed via a second plurality of source select gates of the second tier, a second plurality of drain select gates of the second tier, and a second plurality of digitlines each coupled to a respective one of the second plurality of drain select gates, wherein the second plurality of source select gates are coupled to the first contact, and the second plurality of digitlines are coupled to a respective one of the second plurality of contacts, wherein the second plurality of digitlines are laterally insulated from the second plurality of contacts by an insulator disposed between a horizontal end of each of the second plurality of digitlines and the respective one of the second plurality of contacts.

21. The system of claim 20, comprising a processor coupled to the memory controller and the memory device.

22. A memory device, comprising:

a first tier comprising a first plurality of rows of memory cells, wherein each row of memory cells is coupled to one of a first plurality of wordlines;

a second tier at least partially over the first tier and comprising a second plurality of rows of memory cells, wherein each row of memory cells is coupled to one of a second plurality of wordlines;

a first decoder configured to decode the first plurality of wordlines; and

a second decoder configured to decode the second plurality of wordlines,

wherein the first tier comprises a first plurality of digitlines, wherein each of the first plurality of digitlines is coupled to a respective one of a plurality of contacts extending adjacent to the first tier and the second tier and the first plurality of digitlines are laterally insulated from the plurality of contacts by an insulator disposed between a horizontal end of each of the first plurality of digitlines and the respective one of the plurality of contacts; and

wherein the second tier comprises a second plurality of digitlines, wherein each of the second plurality of digitlines is coupled to a respective one of the plurality of contacts and the second plurality of digitlines are laterally insulated from the plurality of contacts by an insulator disposed between a horizontal end of each of the second plurality of digitlines and the respective one of the plurality of contacts.

23. The device of claim 22, wherein the first tier is accessed via a first plurality of source select gates and a first plurality of drain select gates.

24. The device of claim 23, wherein the second tier is accessed via a second plurality of source select gates and second plurality of drain select gates.

25. A method of operating a memory array, comprising:

accessing a first tier of memory cells via a first plurality of source select gates, a first plurality of drain select gates, and a first plurality of digitlines coupled to a respective one of a plurality of contacts, wherein the first plurality of digitlines are laterally insulated from the plurality of contacts by an insulator disposed between a horizontal end of each of the first plurality of digitlines and the respective one of the plurality of contacts; and

accessing a second tier of memory cells via a second plurality of source select gates, a second plurality of drain select gates, and a second plurality of digitlines coupled to a respective one of the plurality of contacts, wherein the second plurality of digitlines are laterally insulated from the plurality of contacts by an insulator disposed between a horizontal end of each of the second plurality of digitlines and the respective one of the plurality of contacts.

26. The method of claim 25, comprising decoding a first plurality of wordlines of the first tier via a first decoder and decoding a second plurality of wordlines of the second tier via a second decoder.

* * * * *

Exhibit 17

US008912589B2

(12) **United States Patent**
Wang

(10) **Patent No.: US 8,912,589 B2**
(45) **Date of Patent: Dec. 16, 2014**

(54) **METHODS AND APPARATUSES INCLUDING STRINGS OF MEMORY CELLS FORMED ALONG LEVELS OF SEMICONDUCTOR MATERIAL**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 179 days.

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(22) Filed: **Aug. 31, 2011**

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H01L 27/115 (2006.01)
H01L 29/788 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 29/7926*** (2013.01); ***H01L 27/11582*** (2013.01); ***H01L 27/11565*** (2013.01); ***H01L 29/7889*** (2013.01); ***H01L 27/1157*** (2013.01); ***H01L 27/11556*** (2013.01); ***H01L 27/11519*** (2013.01); ***H01L 27/11524*** (2013.01)
USPC **257/324**; 365/185.05; 438/584; 257/E29.129

(58) **Field of Classification Search**
USPC 257/324, E21.645–E21.695; 365/185.05
See application file for complete search history.

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Primary Examiner — Sonya D McCall Shepard
(74) *Attorney, Agent, or Firm* — Schwegman Lundberg & Woessner, P.A.

(57) **ABSTRACT**

Various embodiments include methods and apparatuses including strings of memory cells formed along levels of semiconductor material. One such apparatus includes a stack comprised of a number of levels of single crystal silicon and a number of levels of dielectric material. Each of the levels of silicon is separated from an adjacent level of silicon by a level of the dielectric material. Strings of memory cells are formed along the levels of silicon. Additional apparatuses and methods are disclosed.

24 Claims, 17 Drawing Sheets

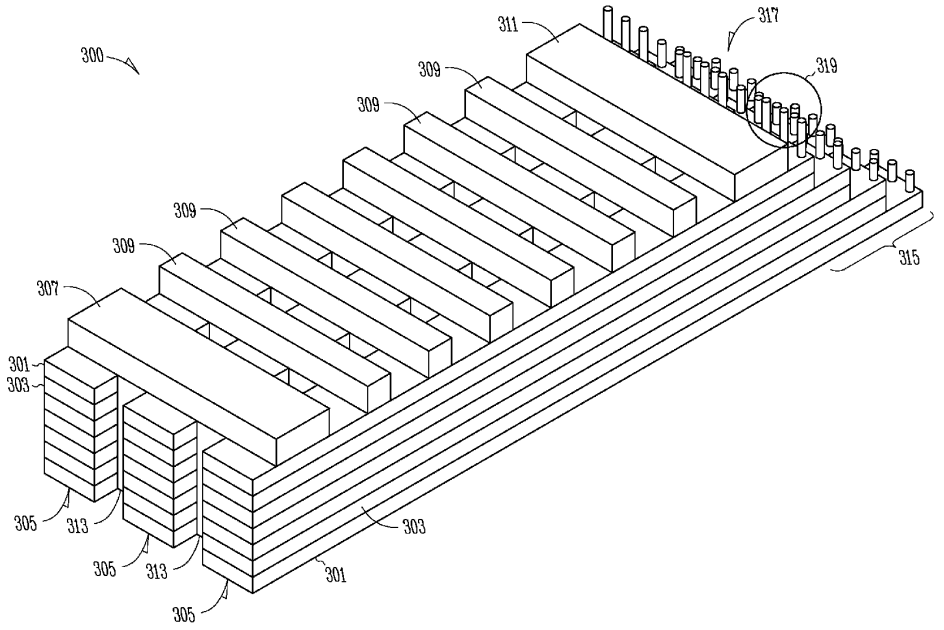


Fig. 1

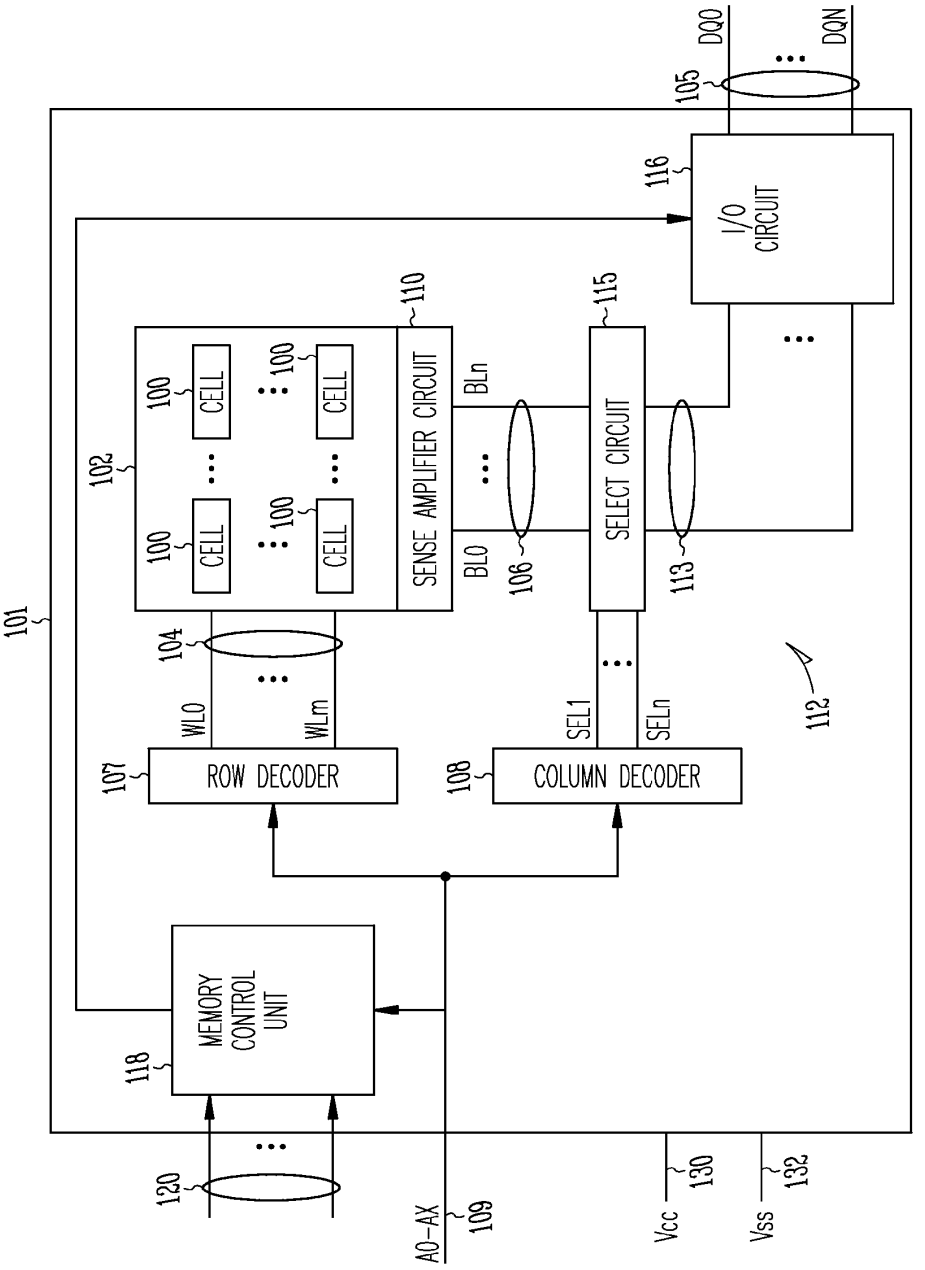
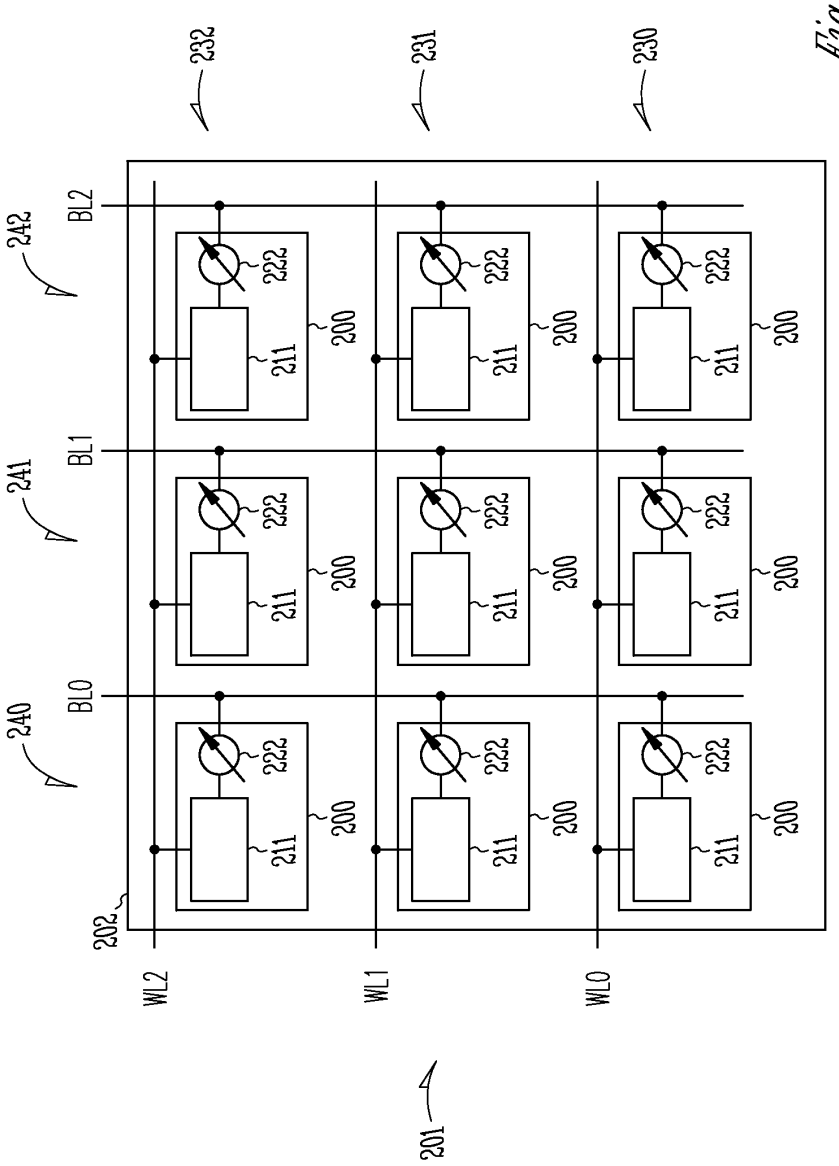

DQ0
DQN
105
116
I/O CIRCUIT
110
115
SENSE AMPLIFIER CIRCUIT
SELECT CIRCUIT
BLn
BL0
106
113
100
CELL
102
101
104
WL0
WLm
SEL1
SELn
112
107
ROW DECODER
108
COLUMN DECODER
MEMORY CONTROL UNIT
118
120
A0-AX
109
Vcc
130
Vss
132

Fig.2


232
231
230
242
241
240
BL2
BL1
BL0
222
211
200
202
WL2
WL1
WL0
201

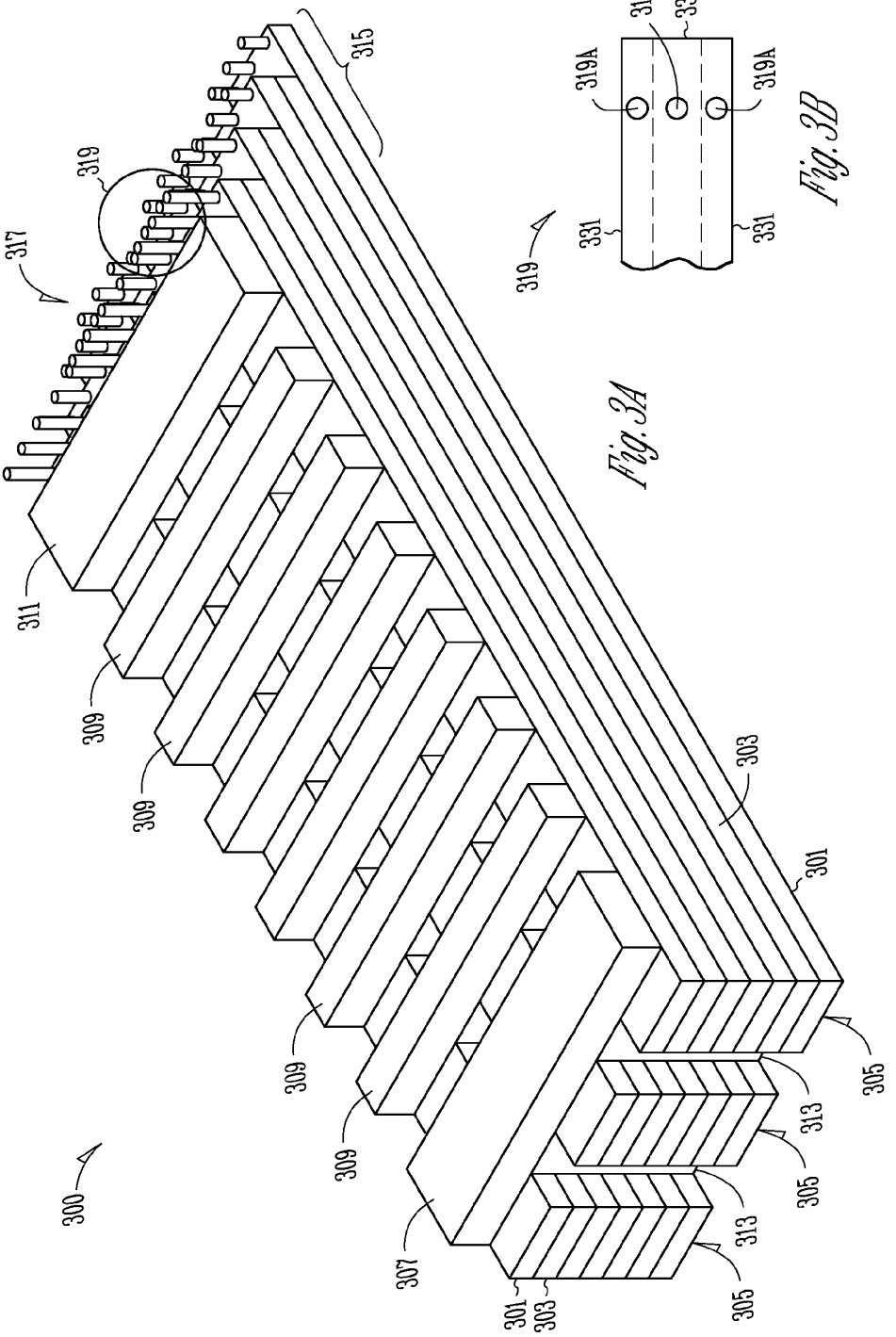

315
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303
300

Fig. 3A

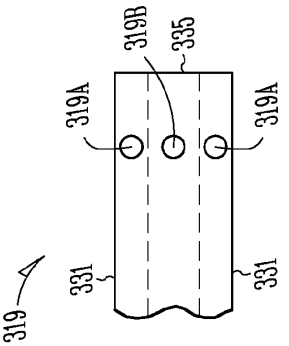

319B
335
319A
319A
331
331
319

Fig. 3B

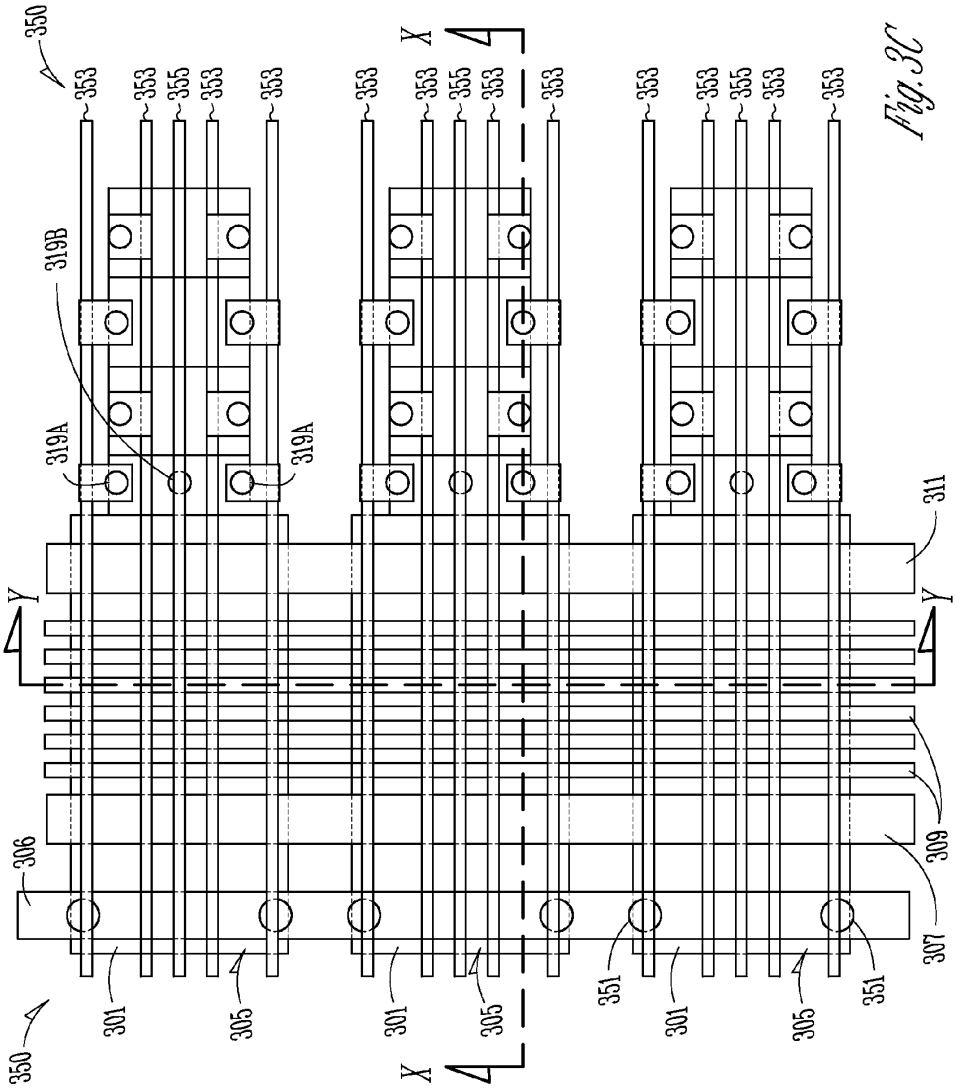
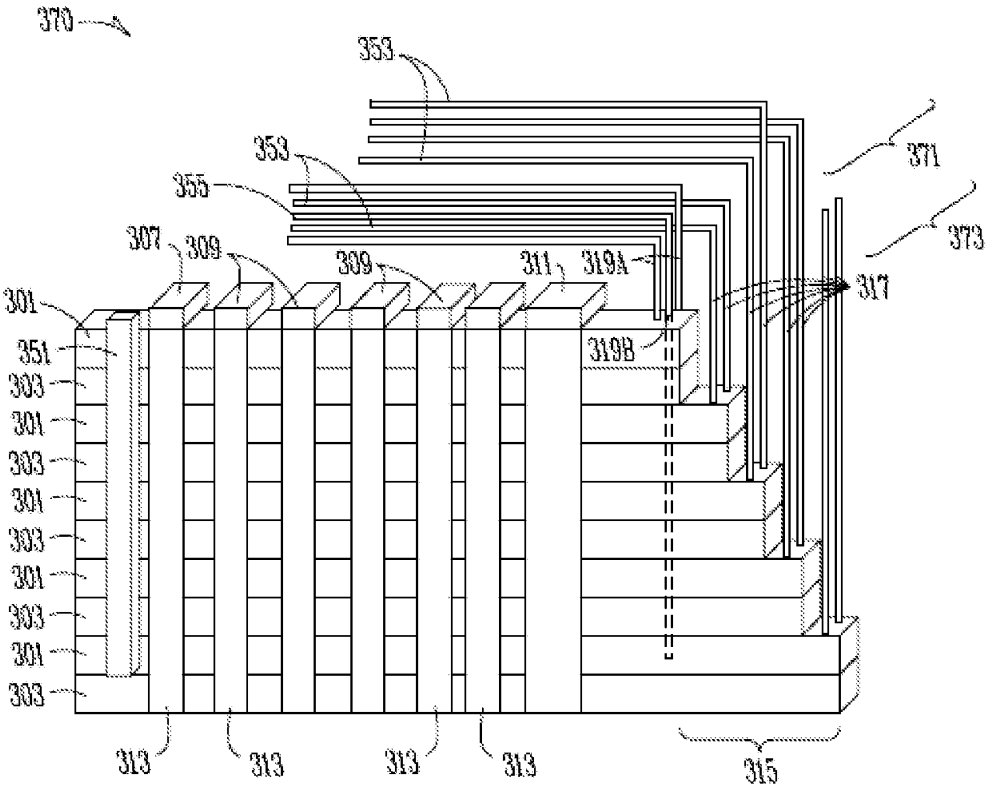
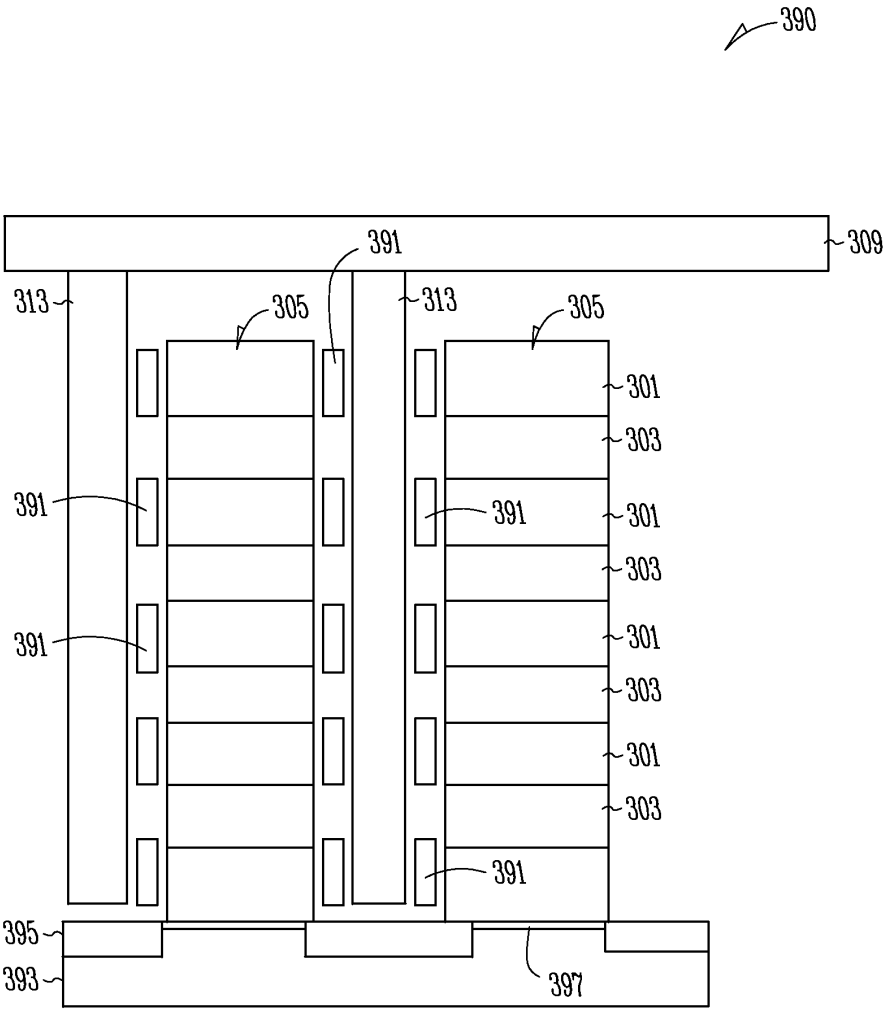


Fig. 3C



SECTION X–X

Fig. 3D



SECTION Y-Y

Fig. 3E

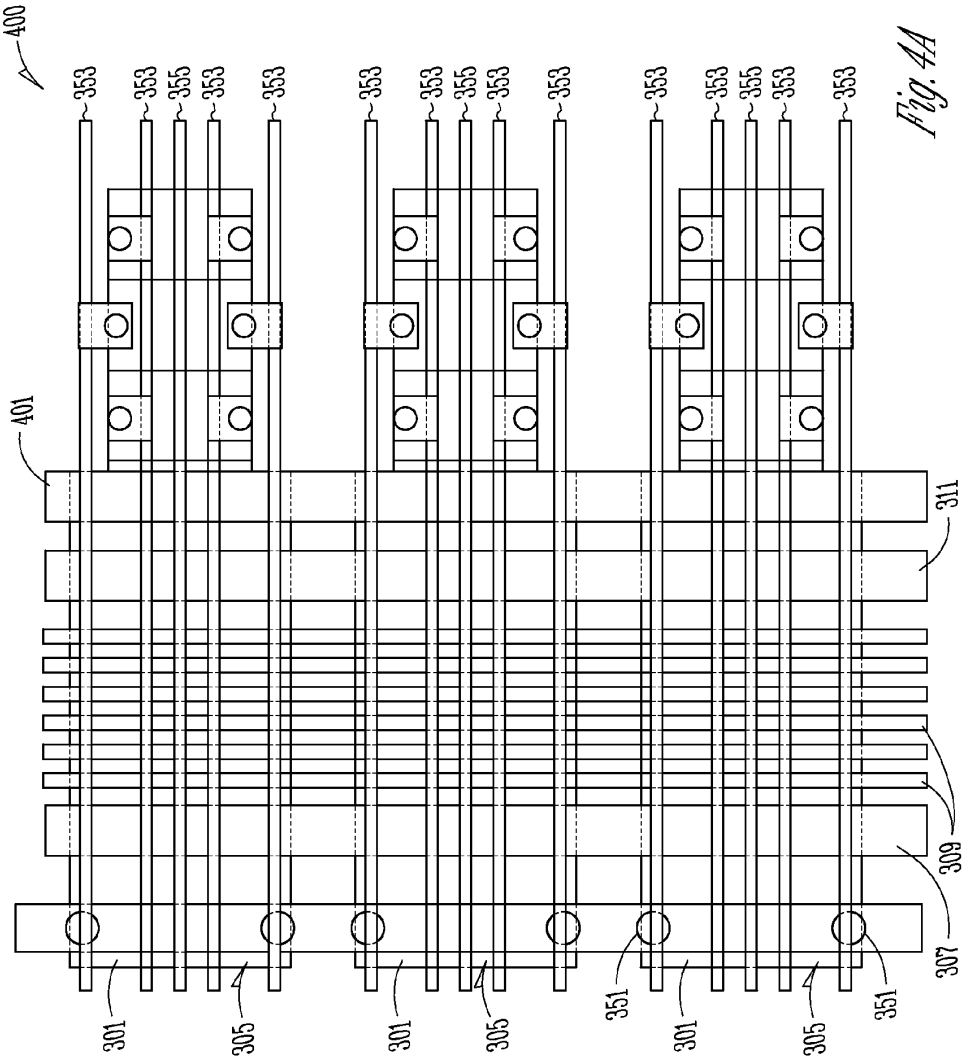


Fig. 4A

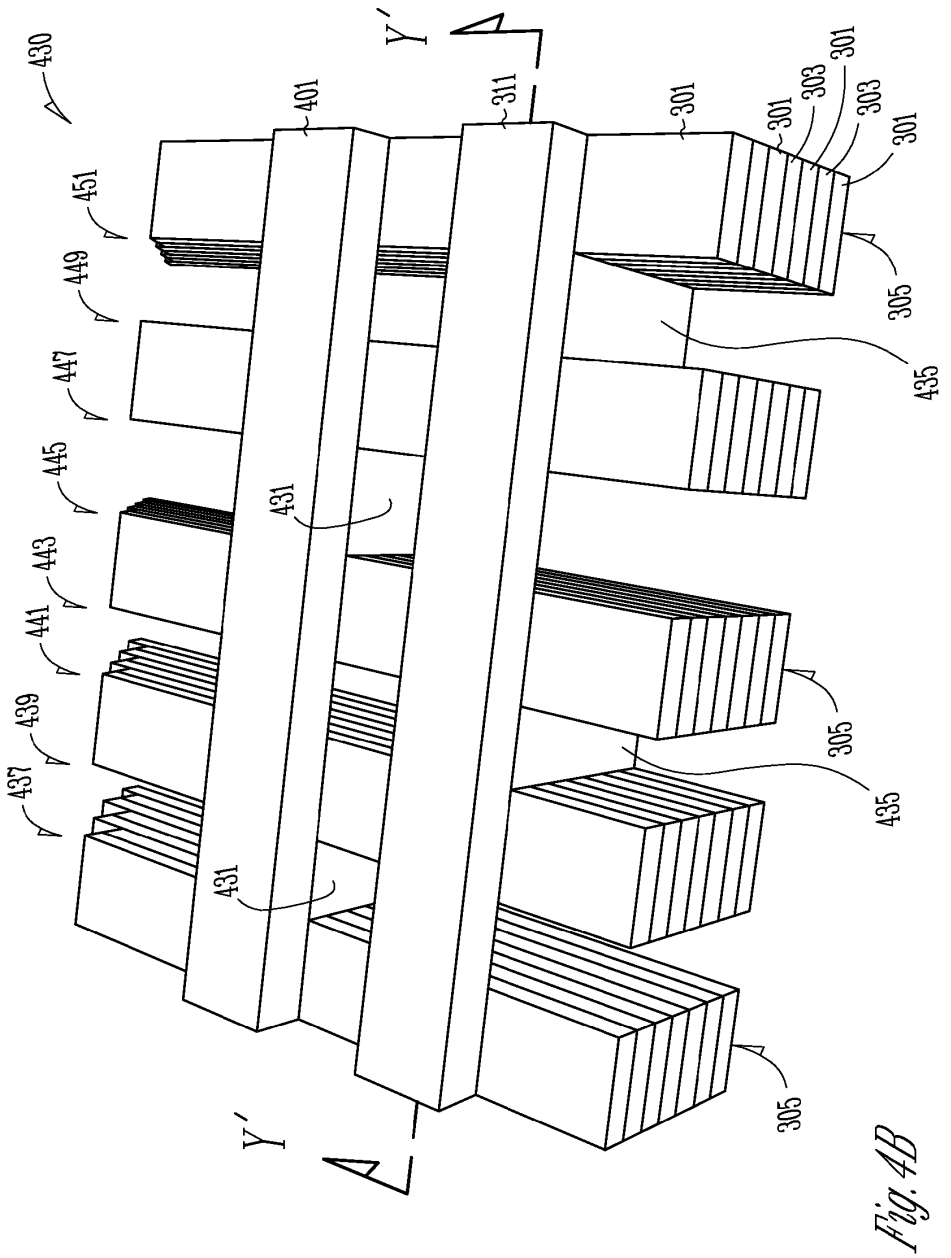
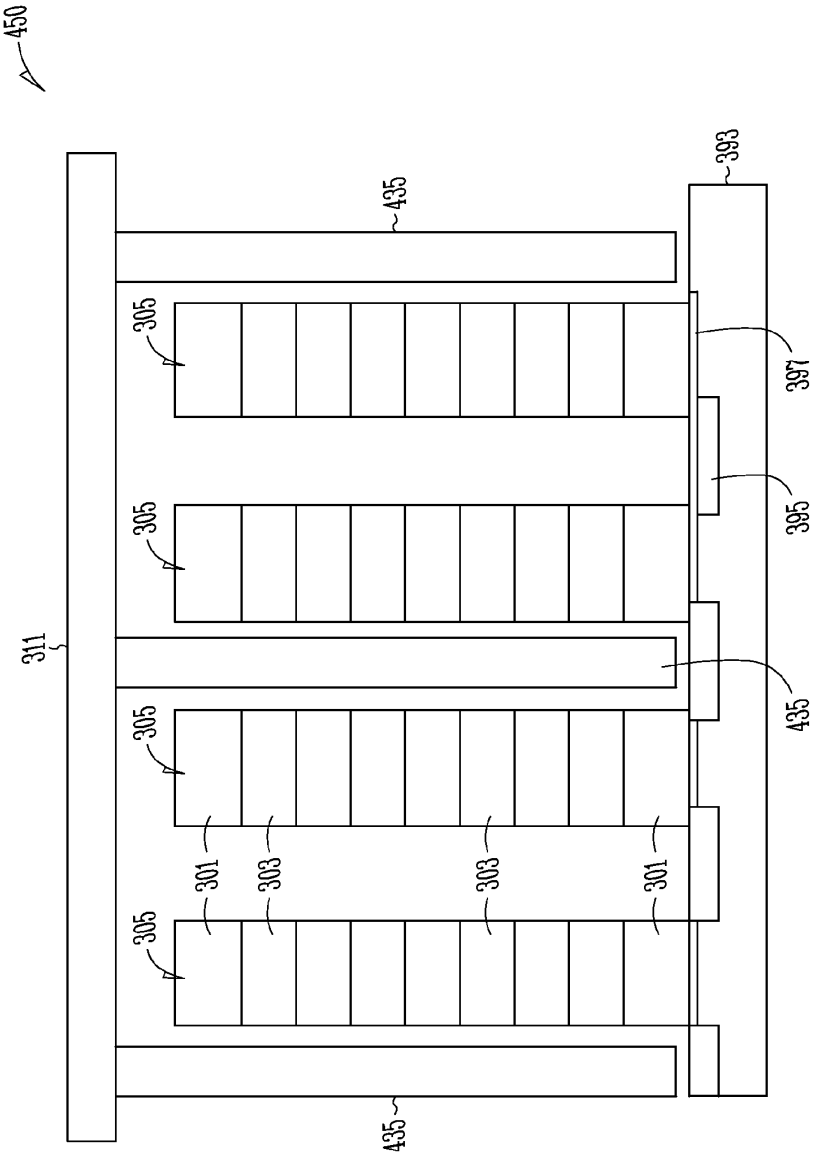

Y'
430
401
311
301
301
303
303
301
451
449
447
445
443
441
439
437
431
431
305
305
305
435
435
Y'

Fig. 4B



SECTION Y'-Y'

Fig. 4C

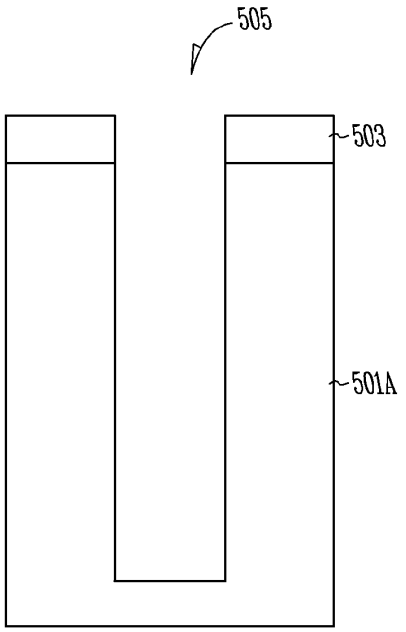


Fig. 5A

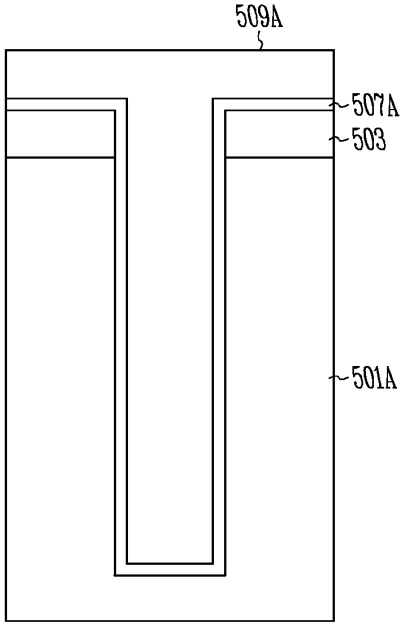


Fig. 5B

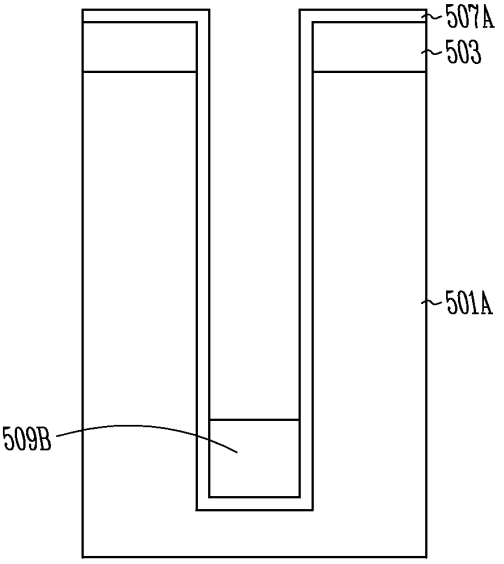


Fig. 5C

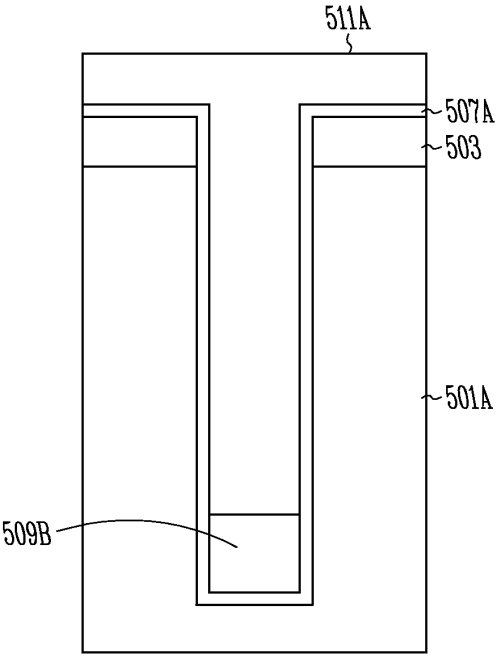


Fig. 5D

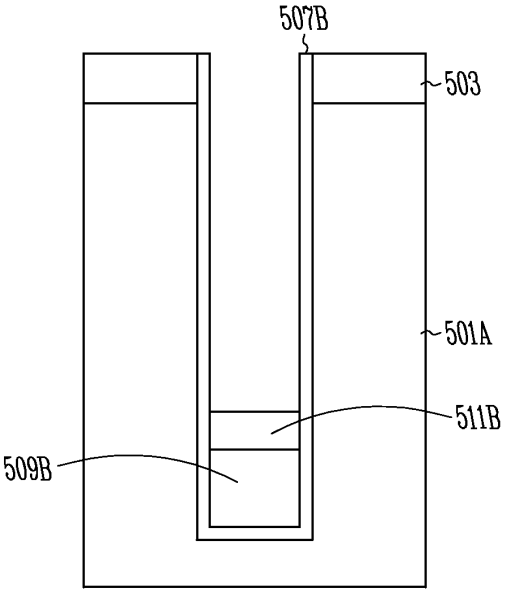

507B
503
501A
511B
509B

Fig. 5E

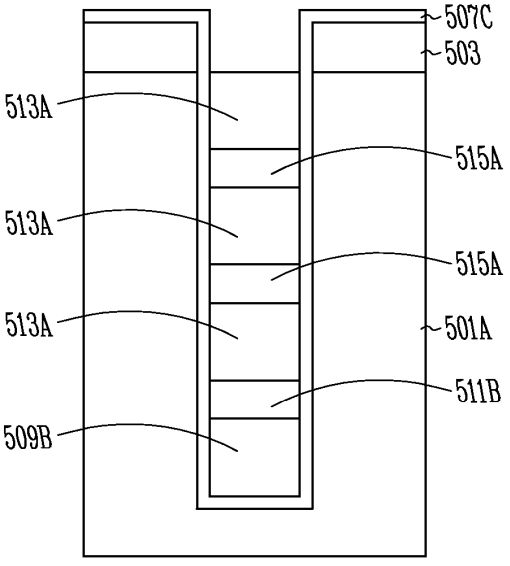

507C
503
513A
515A
513A
515A
513A
501A
511B
509B

Fig. 5F

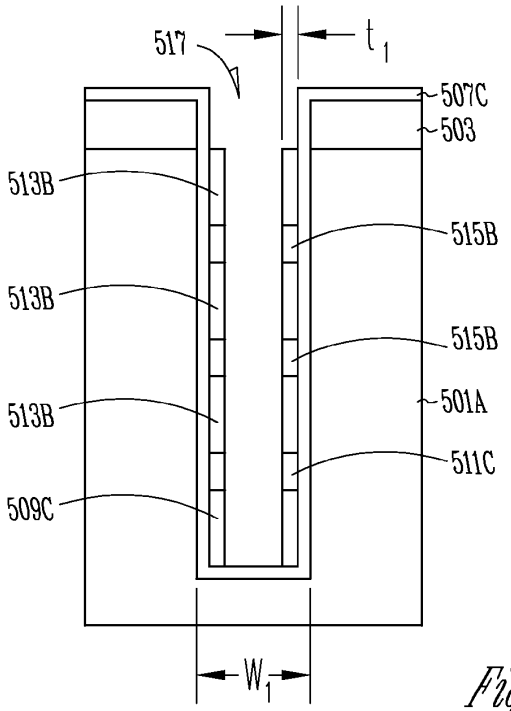

517
t_1
507C
503
513B
515B
513B
515B
513B
501A
511C
509C
W_1

Fig. 5G

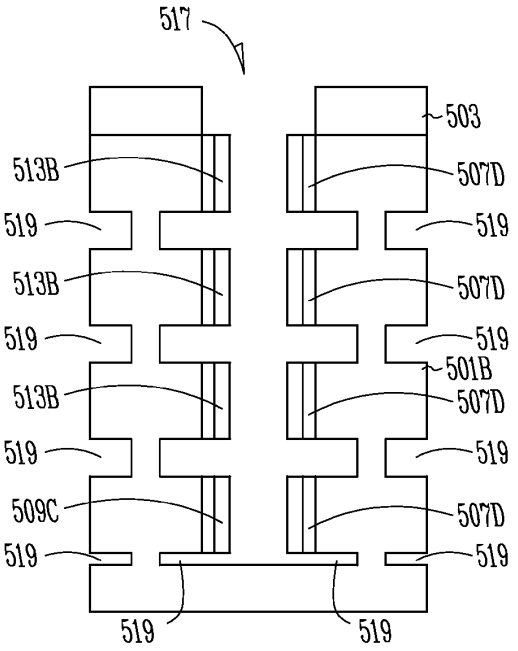

517
503
513B
507D
519
519
513B
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519
519
501B
513B
507D
519
519
509C
507D
519
519
519
519

Fig. 5H

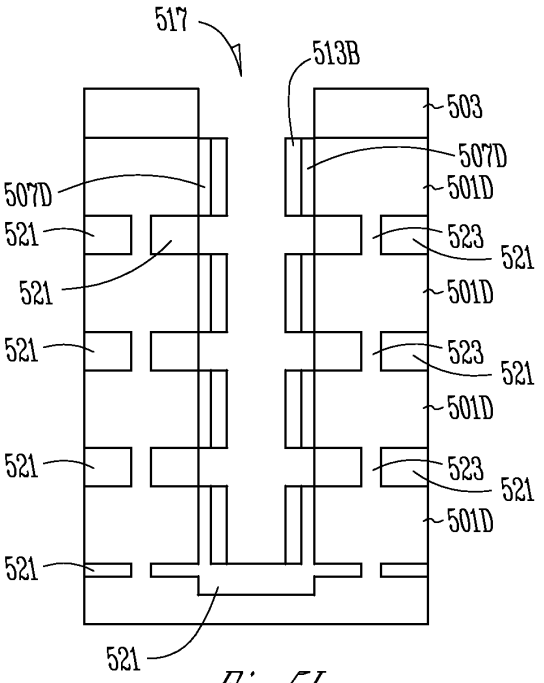

517
513B
503
507D
501D
507D
521
523
521
521
501D
521
523
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501D
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523
521
501D
521
521

Fig. 5I

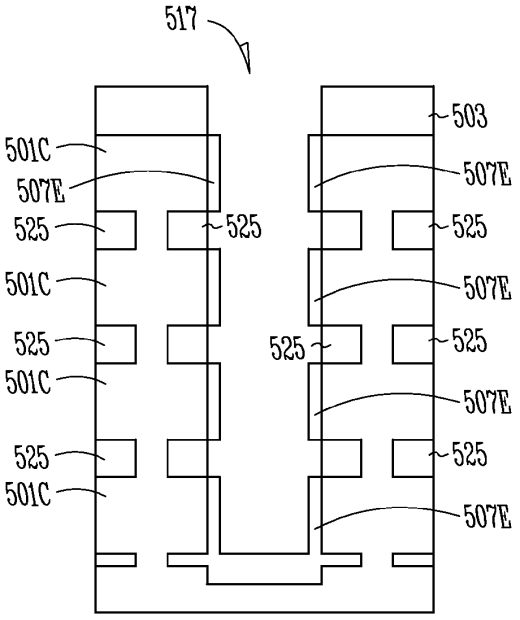


Fig. 5J-1

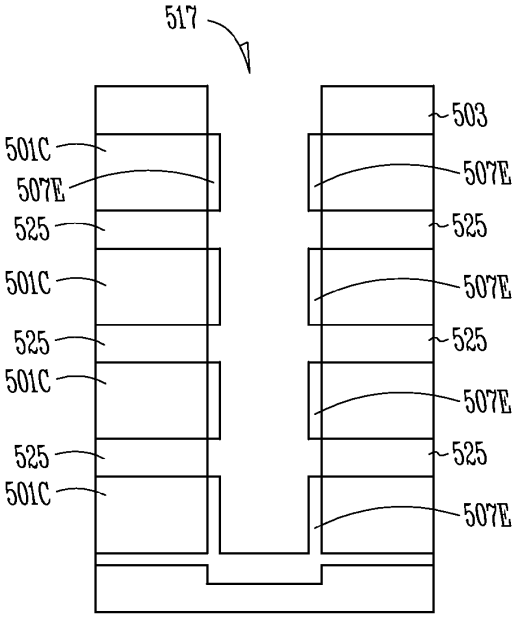


Fig. 5J-2

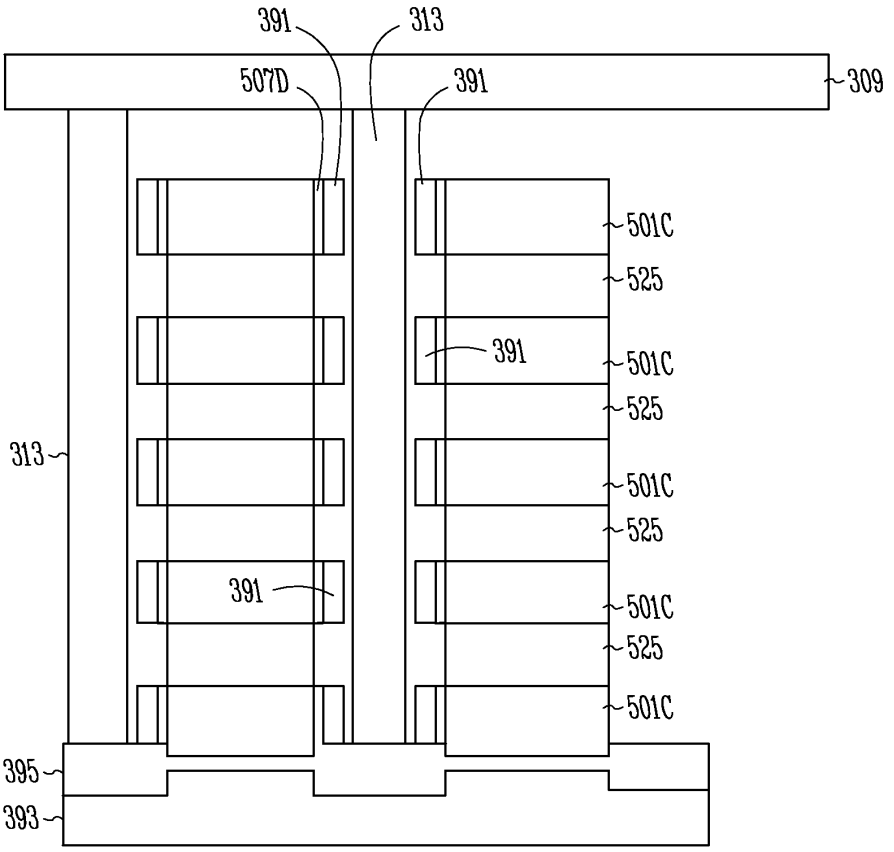

391
313
507D
391
309
501C
525
391
501C
525
313
501C
525
391
501C
525
501C
395
393

Fig. 5K

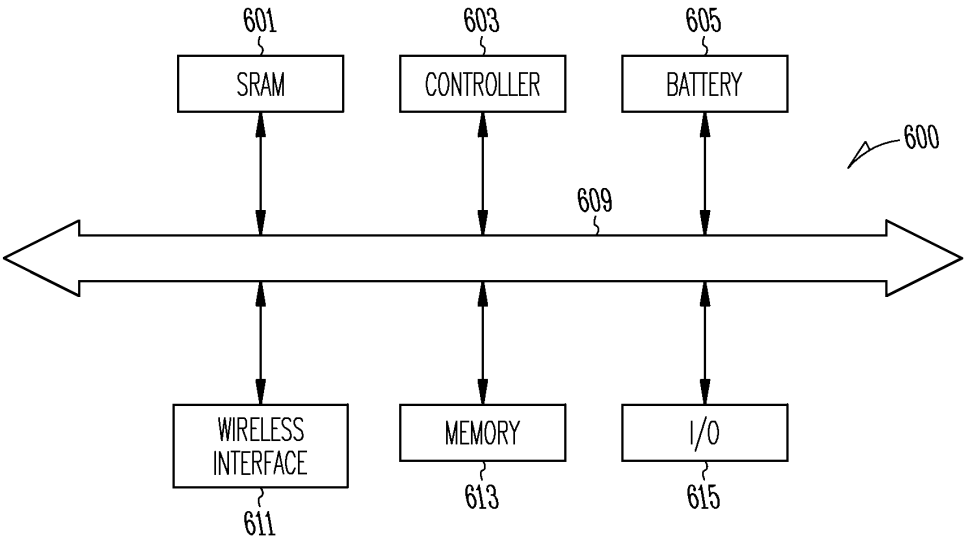

601
SRAM
603
CONTROLLER
605
BATTERY
600
609
WIRELESS INTERFACE
611
MEMORY
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I/O
615

Fig. 6

METHODS AND APPARATUSES INCLUDING STRINGS OF MEMORY CELLS FORMED ALONG LEVELS OF SEMICONDUCTOR MATERIAL

BACKGROUND

Computers and other electronic products, for example, digital televisions, digital cameras, and cellular phones, often use one or more memory devices to store information. Memory devices include memory cells. As the demand for increased storage capacity in memory devices increases, there is a need to increase the density of the memory cells to retain a correspondingly small device size.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a block diagram of a memory device having a memory array with memory cells, according to an embodiment;

FIG. **2** shows a partial block diagram of a memory device having a memory array including memory cells with access components and memory elements, according to an embodiment;

FIGS. **3**A through **3**E show a single select gate drain architecture according to an embodiment;

FIGS. **4**A through **4**C show a dual select gate drain architecture according to an embodiment;

FIGS. **5**A through **5**K show various portions of a fabrication process to form strings of memory cells, according to an embodiment; and

FIG. **6** shows a block diagram of a system embodiment, including a memory device.

DETAILED DESCRIPTION

The description that follows includes illustrative apparatuses (e.g., circuitry, devices, structures, and systems) and methods (e.g., fabrication processes, techniques, and technologies) that embody the inventive subject matter. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide an understanding of various embodiments of the inventive subject matter. It will be evident, however, to those skilled in the art that various embodiments of the inventive subject matter may be practiced without these specific details. Further, well-known instruction instances, protocols, structures, fabrication technologies, and techniques have not been shown in detail, so as not to obscure the various illustrated embodiments.

As used herein, the term "or" may be construed in an inclusive or exclusive sense. Additionally, although various exemplary embodiments discussed below focus on a three-dimensional (3D) NAND memory device, the embodiments are merely given for clarity in disclosure, and thus, are not limited to NAND memory devices or even to memory devices in general. As an introduction to the subject, a few embodiments will be described briefly and generally in the following paragraphs, and then a more detailed description, with reference to the figures, will ensue.

One disclosed method of fabrication, and resulting apparatus, has an architecture comprising a stacked three-dimensional structure. The structure may be used to form, for example, strings of memory cells. In various embodiments, single crystal silicon strings of memory cells are provided. In such an embodiment, rather than building vertical polysilicon strings on top of a substrate, the disclosed structure builds stacked horizontal silicon strings into the substrate. Separate

string channels can run along both sidewalls in a given level of single crystal silicon in the stacked structure. The sidewalls are described in more detail, by way of example, with reference to FIG. **4**B, below. The disclosed structure can utilize all functions developed for, for example, planar NAND logic. At the same time, the disclosed structure can increase the memory density by stacking more memory strings in a given area.

In various embodiments, an apparatus is provided that includes a stack comprising a number of levels of semiconductor material and a number of levels of dielectric material. Each of the levels of semiconductor material is separated from a respective adjacent one of the levels of semiconductor material by at least a respective one of the levels of dielectric material. A respective string of memory cells are formed along each of the levels of semiconductor material.

In some embodiments of the apparatus, each of the levels of semiconductor material comprises opposing ones of a first sidewall and a second sidewall. A respective one of the strings of memory cells is formed along a respective one of the levels of semiconductor material that includes a first string of memory cells formed along the first sidewall of the respective level of semiconductor material and a second string of memory cells formed along the second sidewall of the respective level of semiconductor material.

In various embodiments, a method is provided that includes forming a first opening in a semiconductor substrate and forming an alternating arrangement of first and second blocks within the first opening. The first block comprises a different material than the second block. A second opening is formed within the alternating arrangement to form an alternating arrangement of first and second sidewall blocks from the first and second blocks, respectively. At least a portion of the second sidewall blocks to expose portions of the substrate and lateral openings are formed in the substrate at the exposed portions.

In some embodiments of the method, prior to forming the alternating arrangement of first and second blocks within the first opening, a dielectric liner is formed on at least sidewalls of the first opening. Additionally, removing at least the second sidewall blocks to expose portions of the substrate further includes removing portions of the dielectric liner underlying the second sidewall blocks, forming a control gate in the second opening, and forming a number of charge storage structures disposed between the control gate and remaining portions of the substrate.

In various embodiments, an apparatus is provided that includes a base substrate having a number of openings formed therein and a stack formed between each of the number of openings. Each stack has a number of levels of semiconductor material and a number of levels of dielectric material. Each level of the number of levels of semiconductor material is separated from an adjacent level of semiconductor material by at least one of the number of levels of dielectric material. Also, each of the levels of semiconductor material has a first side and an opposing second side. At least one string of memory cells is formed along at least one of the first side and the second side of the levels of semiconductor material.

In some embodiments of the apparatus, a number of control gates are disposed within the number of openings in the base substrate. A charge storage structure is disposed between a portion of each of the number of control gates and at least one of the number of levels of semiconductor material.

In various embodiments, an apparatus is provided that includes a base substrate having a number of openings formed therein and a multiple level structure formed between each of the number of openings. Each multiple level structure has a

number of levels of silicon material and a number of levels of silicon dioxide material. Each level of the number of levels of silicon material is separated from an adjacent level of silicon material by at least one of the number of levels of silicon dioxide material. Each of the levels of silicon material has a first side and an opposing second side. At least one string of memory cells is formed on each of the first side and the second side of the levels of silicon material. A number of control gates are disposed within the number of openings in the base substrate. A charge storage structure is disposed between a portion of each of the number of control gates and at least one of the number of levels of silicon material.

Referring now to FIG. **1**, a block diagram of an apparatus in the form of a memory device **101** is shown. The memory device **101** is shown to include a memory array **102** having a number (e.g., one or more) of memory cells **100** according to an embodiment. The memory cells **100** can be arranged in rows and columns along with access lines **104** (e.g., wordlines to conduct signals WL**0** through WLm) and first data lines **106** (e.g., bit lines to conduct signals BL**0** through BLn). The memory device **101** can use the access lines **104** and the first data lines **106** to transfer information to and from the memory cells **100**. A row decoder **107** and a column decoder **108** decode address signals A**0** through AX on address lines **109** to determine which ones of the memory cells **100** are to be accessed.

A sense amplifier circuit **110** operates to determine a value of information read from the memory cells **100** and the information in the form of signals to the first data lines **106**. The sense amplifier circuit **110** can also use the signals on the first data lines **106** to determine values of information to be written to the memory cells **100**.

The memory device **101** is further shown to include circuitry **112** to transfer information between the memory array **102** and input/output (I/O) lines **105**. Signals DQ**0** through DQN on the I/O lines **105** can represent information read from or to be written into the memory cells **100**. The I/O lines **105** can include nodes within the memory device **101** (or alternatively, pins, solder balls, or other interconnect technologies such as controlled collapse chip connection (C4), or flip chip attach (FCA)) on a package where the memory device **101** can reside. Other devices external to the memory device **101** (e.g., a memory controller or a processor, not shown in FIG. **1**) can communicate with the memory device **101** through the I/O lines **105**, the address lines **109**, or control lines **120**.

The memory device **101** can perform memory operations, such as a read operation, to read information from selected ones of the memory cells **100** and a programming operation (also referred to as a write operation) to program (e.g., to write) information into selected ones of the memory cells **100**. The memory device **101** can also perform a memory erase operation to clear information from some or all of the memory cells **100**. A memory control unit **118** controls memory operations based on signals on the control lines **120**. Examples of the signals on the control lines **120** can include one or more clock signals and other signals to indicate which operation (e.g., a programming or read operation) the memory device **101** can or should perform. Other devices external to the memory device **101** (e.g., a processor or a memory controller) can control the values of the control signals on the control lines **120**. Specific combinations of values of the signals on the control lines **120** can produce a command (e.g., a programming or read command) that can cause the memory device **101** to perform a corresponding memory operation (e.g., a program, read, or erase operation).

Each of the memory cells **100** can be programmed to a different one of at least two data states to represent, for example, a value of a single bit or a value of multiple bits such as two, three, four, or a higher number of bits. For example, each of the memory cells **100** can be programmed to one of two data states to represent a binary value of "0" or "1" of a single bit. Such a cell is sometimes called a single level cell. In another example, each of the memory cells **100** can be programmed to one of more than two data states to represent a value of, for example, multiple bits, such as one of four possible values "00," "01," "10," and "11" of two bits, one of eight possible values "000," "001," "010," "011," "100," "101," "110," and "111" of three bits, or one of another set of values of multiple bits. A cell that can be programmed to more than two data states is sometimes referred to as a multi-level cell (or multi-state cell). Various operations on these types of cells are discussed in more detail, below.

The memory device **101** can receive a supply voltage, including supply voltage signals V_{cc} and V_{ss}, on a first supply line **130** and a second supply line **132**, respectively. Supply voltage signal V_{ss} can, for example, be at a ground potential (e.g., having a value of approximately zero volts). Supply voltage signal V_{ss} can also operate at other voltages. Supply voltage signal V_{cc} can include an external voltage supplied to the memory device **101** from an external power source such as a battery or an alternating-current to direct-current (AC-DC) converter circuitry (not shown in FIG. **1**).

The circuitry **112** of the memory device **101** is further shown to include a select circuit **115** and an input/output (I/O) circuit **116**. The select circuit **115** can respond to signals SEL**1** through SELn to select signals on the first data lines **106** and the second data lines **113** that can represent the information read from or to be programmed into the memory cells **100**. The column decoder **108** can selectively activate the SEL**1** through SELn signals based on the A**0** through AX address signals on the address lines **109**. The select circuit **115** can select the signals on the first data lines **106** and the second data lines **113** to provide communication between the memory array **102** and the I/O circuit **116** during read and programming operations.

The memory device **101** can include a non-volatile memory device and the memory cells **100** can include non-volatile memory cells such that the memory cells **100** can retain information stored therein when power (e.g., V_{cc}, V_{ss}, or both) is disconnected from the memory device **101**.

Each of the memory cells **100** can include a memory element having material, at least a portion of which can be programmed to a desired data state (e.g., by storing a corresponding amount of charge on a charge storage structure, such as a floating gate or charge trap, coupled with various threshold voltage, V_t, changes after program or erase operations). Different data states can thus represent different values of information programmed in each of the memory cells **100**.

The memory device **101** can perform a programming operation when it receives (e.g., from an external processor or a memory controller) a programming command and a value of information to be programmed into one or more selected ones of the memory cells **100**. Based on the value of the information, the memory device **101** can program the selected memory cells to appropriate data states to represent the values of the information to be stored therein.

One of ordinary skill in the art may recognize that the memory device **101** may include other components, at least some of which are discussed herein. However, several of these components are not necessarily shown in the figure, so as not to obscure the various embodiments described. The memory device **101** may include devices and memory cells,

and operate using memory operations (e.g., programming and erase operations) similar to or identical to those described below with reference to various other figures and embodiments discussed herein.

With reference now to FIG. **2**, a partial block diagram of an apparatus in the form of a memory device **201** is shown to include a memory array **202**, including memory cells **200** with access components **211** and memory elements **222**, according to an example embodiment. The memory array **202** may be similar or identical to the memory array **102** of FIG. **1**. As further shown in FIG. **2**, the memory cells **200** are shown to be arranged in a number of rows **230**, **231**, **232**, along with access lines, for example word lines, to conduct signals such as signals WL**0**, WL**1**, and WL**2**. The memory cells are also shown to be arranged in a number of columns **240**, **241**, **242** along with data lines, for example bit lines, to conduct signals such as signals BL**0**, BL**1**, and BL**2**. The access components **211** can turn on (e.g., by using appropriate values of signals WL**0**, WL**1**, and WL**2**) to allow access to the memory elements **222**, such as to operate the memory elements as pass elements, or to read information from or program (e.g., write) information into the memory elements **222**.

Depending on the memory type, programming information into the memory elements **222** can include causing the memory elements **222** to have specific resistance values or to store specific amounts of charge. Thus, reading information from a memory cell **200** can include, for example, determining a resistance value of the memory element **222** or determining whether the memory cell **200** is placed in a conductive state in response to a specific voltage being applied to its access component **211**. In either case, such a determining act may involve sensing a current (or absence of current) flowing through the memory cell **200** (e.g., by sensing a current of a bit line electrically coupled to the memory cell). Based on a measured value of the current, a corresponding value of the information stored in the memory can be determined. Determining values of the information based on the value of the current is discussed in more detail, below. The value of information stored in a memory cell **200** can be determined in still other ways, such as by sensing a voltage of a bit line electrically coupled to the memory cell.

FIGS. **3**A through **3**E show an apparatus in the form of a memory device having a single select gate drain architecture according to an embodiment. With specific reference to FIG. **3**A, a schematic three-dimensional representation of a portion of an apparatus **300** is shown to include three stacks **305**, each comprised of a number of levels of semiconductor material (e.g., silicon) **301** and a number of levels of dielectric material (e.g., silicon dioxide) **303**. In each stack **305**, each of the levels of the semiconductor material **301** is separated from a respective adjacent one of the levels of the semiconductor material **301** by at least a respective one of the levels of the dielectric material **303**. Each of the stacks **305** could be considered to be a multiple level structure. A person of ordinary skill in the art, upon reading the disclosure provided herein, will recognize that materials other than silicon and silicon dioxide may be used. For example, various types of semiconductor materials, such as various elemental and compound semiconductors may be used as an alternative for or in conjunction with the silicon. Additionally, various types of dielectric materials, such as tantalum pentoxide (Ta_2O_5), silicon nitride (Si_xN_y), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), or a variety of other dielectric materials can be used as an alternative to or in conjunction with the silicon dioxide.

The apparatus **300** is also shown to include a select gate source line **307**, a select gate drain line **311**, and a number of access lines **309**, for example word lines, to conduct signals. Although FIG. **3**A shows six of the access lines **309**, any number of lines may be used. As shown, each of the access lines **309**, the select gate source line **307**, and the select gate drain line **311** (albeit partially obscured) are electrically coupled to (e.g., in direct contact with) corresponding control gates **313**. The control gates **313** are located in trenches, where each of the illustrated trenches is formed between and separates adjacent ones of the stacks **305**. One example of such a trench is described in more detail with reference to FIG. **5**A, below. Thus, each of the illustrated ones of the control gates **313** is shared between respective neighboring ones of the stacks **305**, creating "common" control gates between adjacent ones of the stacks **305**. Further, as described in more detail below by way of example, strings of memory cells can be fabricated along the sidewalls of each of the stacks **305**.

As further shown in the apparatus **300**, each level of the semiconductor material **301** in a given stack **305** is electrically coupled at one end to a number of contacts **317**, described in more detail, below. To access each level of the semiconductor material **301** in the stack, an overlying level(s) **301**, **303** of the stack **305** is stepped back on at least one end from an underlying level of the semiconductor material **301**. Consequently, at least one end of the stack **305** is formed into a staircase structure **315**.

The smaller area shown encircled in FIG. **3**A illustrates a portion **319** of the contacts **317**. The portion **319** is discussed in detail with reference to FIG. **3**B.

FIG. **3**B shows a plan view of the portion **319** of FIG. **3**A. The portion **319** is shown to include two sidewall contacts **319**A and a body contact **319**B. The contacts **319**A, **319**B provide a point of electrical coupling on various portions of one end of a level of the semiconductor material **301**. Consequently, strings of memory cells can be fabricated on both sides of each of the stacks **305** (e.g., so there are two memory strings per each level of the semiconductor material **301** per stack **305**, one per level of the semiconductor material **301** on either side of the stack **305**). Consequently, with three of the stacks **305** as shown in FIG. **3**A, each with two sidewalls and each with four levels of the semiconductor material **301**, **24** separate strings of memory cells can be formed. Different numbers of strings may be formed in other embodiments.

With continuing reference to FIG. **3**B, in a specific embodiment, for example, in an NMOS device, an N+ region is diffused along the sidewall **331** along which various ones of the memory cells of a particular string can later be fabricated (discussed in more detail, below). In one example, the N+ region may be formed by implantation. Each of the two sidewall contacts **319**A contacts a respective N+ region of the illustrated level of the semiconductor material **301**. In an NMOS device, the body contact **319**B provides an electrical contact to a common body **335** of the illustrated level of the semiconductor material **301**—in this case, a P body. A person of ordinary skill in the art will readily recognize that a PMOS device can be constructed in a similar fashion with a N-type body and P-type sidewalls.

Referring now to FIG. **3**C, a plan view schematic **350** of the apparatus **300** of FIG. **3**A is shown. Each of the elements with the same numbers refers to the same elements as shown in FIG. **3**A.

The plan view schematic **350** is further shown to include a number of source contacts **351**, a number of data lines **353**, and a number of body contact lines **355** (although only one body contact is shown for clarity, additional body contacts may be formed to each of the levels of the semiconductor material **301**). Each of the source contacts **351** electrically couples a number of the strings to a source line **306**. Each of

the data lines **353** (e.g., bit lines) is electrically coupled to a respective one of the strings at each of a number of the levels of stack **305** by a respective one of the two sidewall contacts **319**A, as described in more detail, below. Each of the body contact lines **355** is electrically coupled to the body contacts **319**B of a respective one of the stacks **305** or, alternatively, to individual ones of the semiconductor materials **301** as discussed above.

As noted above with reference to FIGS. **3**A and **3**B, a respective string of memory cells is fabricated along each sidewall **331** at each level of each of the stacks **305**. Therefore, there are two strings per level of the semiconductor material **301** per stack **305**. Each of the two strings formed along a given level of the semiconductor material **301** of one of the stacks **305** shares a common body **335** (FIG. **3**B). As further illustrated in FIG. **3**C, two sectional indicators (Section X-X and section Y-Y) provide reference locations for the respective cross-sectional elevational views, discussed by way of example, with reference to FIGS. **3**D and **3**E, below.

FIG. **3**D shows a cross-sectional view **370** of Section X-X of the three-dimensional representation of an apparatus **300** of FIG. **3**A. The cross-sectional view **370** shows a number of the contacts **317** (including the two sidewall contacts **319**A and the body contact **319**B) electrically coupled to the data lines **353** of a first metal level **373** and a number of the contacts **317** electrically coupled to data lines **353** of a second metal level **371** (albeit not all the connections are shown so as not to obscure the drawing; the remaining connections are understandable by a person of ordinary skill in the art). The body contact **319**B may be punched through each level of the semiconductor material **301** in the stack **305** as indicated by the dashed line in FIG. **3**D. Alternatively, a separate body contact **319**B may be individually coupled to each of the semiconductor materials **301**. Also, the body contact lines **355** may be constructed similarly as the body contact **319**B. Individual conductive lines within the first metal level **373** and the second metal level **371** correspond to the data lines **353** discussed with reference to FIG. **3**C, above. A person of ordinary skill in the art will further understand that additional metal levels may be employed. Further, the cross-sectional view **370** indicates how each of the levels of the semiconductor material **301** can be electrically accessed by the contacts due to the staircase structure **315** discussed earlier with reference to FIG. **3**A. For clarity in understanding, in a specific embodiment of NMOS devices, a current (not shown) flows along each of the strings, during operation and activation of the string, from the select gate source line **307** to the select gate drain line **311**.

FIG. **3**E shows a cross-sectional view **390** of Section Y-Y of the three-dimensional representation of the apparatus **300** of FIG. **3**A. The cross-sectional view **390** indicates a number of charge storage structures **391** (e.g., floating gates or charge traps) disposed between each control gate **313** and each level of the semiconductor material **301** in the stacks **305**. Accordingly, a control gate **313** is separated from a level of the semiconductor material **301** by at least a charge storage structure **391**. As illustrated in the specific embodiment of FIG. **3**E, each of the charge storage structures **391** form a memory cell element for a total of 15 memory cell elements. As noted above, a different string of memory cells is running along each sidewall at each level of the semiconductor material **301** of each stack **305**. Consequently, each of the 15 memory cell elements shown in FIG. **3**E comprises one respective cell within a respective one of 15 different strings. A first dielectric material **395** electrically isolates each control gate **313** from an underlying portion of substrate **393**. A second dielectric material **397** electrically isolates each of the stacks **305** from an underlying portion of substrate **393**. As discussed below, by way of example with reference to FIGS. **5**A through **5**K, the first dielectric material **395** and the second dielectric material **397** may be the same material. In other embodiments, the first dielectric material **395** and the second dielectric material **397** may comprise different materials. Further, FIGS. **5**A through **5**K provide additional details on the overall structure of the cross-sectional view **390** of Section Y-Y.

In a specific embodiment, a lateral dimension (e.g., width) of the stacks **305** may be about 300 nm. A distance between adjacent ones of the stacks **305** may be about 100 nm. Therefore, a ratio of the width of the stacks **305** to the distance between the stacks is about 3 to 1. A dimension of each level of the semiconductor material **301** and each level of the dielectric material **303** may be from about 25 nm to about 40 nm in thickness. Thus, the ratio of width to thickness of the levels of the semiconductor material **301** and levels of the dielectric material **303** may each be from about less than 8 to 1 to about 12 to 1. However, depending upon a selection of final materials used in the various portions, the single select gate architecture and a contemporaneous state of the art, the dimensions shown may be considerably different than those numbers shown above.

Referring now to FIG. **4**A, a plan view schematic **400** shows an apparatus having a dual select gate drain architecture. The plan view schematic of FIG. **4**A is similar to the plan view schematic **350** of FIG. **3**C. However, FIG. **4**A is shown to include the second select gate drain line **401**. Therefore, the plan view schematic **400** may utilize two select gate drain transistors instead of a single select gate drain transistor as used by the device of FIGS. **3**A through **3**E. By adding an additional select gate drain transistor, the number of metal levels may be reduced to about one-half the number of levels used in the single select gate drain option, discussed above. Also, the number of contacts can be reduced by about one-half. Further, the length of each memory string may be reduced by about one-half. These reductions occur since the operation of a string is controlled by both the second select gate transistor and the data line.

For example, with the dual select gate drain architecture, an operation of one string is controlled by both one select gate drain transistors and one data line (e.g., the first data lines **106** (e.g., bit lines) of FIG. **1**). In contrast, for the single select gate drain approach of FIGS. **3**A through **3**E, a voltage is applied and passed through the single select gate drain during programming for an entire block of memory cells. A string of memory cells not receiving programming is inhibited by elevating a voltage on the appropriate data line to an inhibit voltage.

The dual select gate drain architecture functions similarly to the single select gate drain architecture. However, the dual select gate drain architecture can also inhibit a string of memory cells by turning off the appropriate select gate drain transistor that controls the string without necessarily applying an inhibit voltage to the data line corresponding to that string. This dual select gate drain approach is described in more detail, by way of example, with reference to FIGS. **4**B and **4**C, below. As discussed in further detail below, with the dual select gate drain architecture, the operation of one string is controlled by both a select gate and bitcon. For the single drain select gate approach, a select gate voltage is turn on during programming for an entire block, the string that is not to be programmed is inhibited by elevating a data line voltage. The dual drain select gate approach can use the single select gate inhibit scheme as well, however it also can inhibit one or more strings by turning off the select gate to shut off the string even the data line voltage is low. With this approach, two

strings on the same semiconductor level can share the same bitcon and same data line. Thus, the number of contact and the number of dataline can be cut to one-half the single drain select gate approach. Two strings on the same level can be electrical separated by the two drain select gates. For example, the second select gate drain line **401** can control left string, while the select gate drain line **311** can control the right string. This concept can be extended to multiple drain select gates. For example, for a given number, n, of drain select gates, the number of data line and contacts can be reduced by n times.

With reference to FIG. **4**B, a schematic three-dimensional representation of a portion of an apparatus having a dual select gate drain architecture **430** is shown to include five of the stacks **305** comprised of alternating levels of the semiconductor material **301** and the dielectric material **303**. Also as shown, the dual select gate drain architecture **430** is shown to include a first one of the select gate drain line **311** and a second select gate drain line **401**. In the example of FIG. **4**B, the first select gate drain line **311** is electrically coupled to a first set of control gates **435**. The second select gate drain line **401** is electrically coupled to a second set of control gates **431**. FIG. **4**B also indicates a Y'-Y' cross-section. The Y'-Y' cross-section is discussed below with reference to FIG. **4**C.

With continued reference to FIG. **4**B, the leftmost of the second set of control gates **431** is located between a right sidewall **437** and a left sidewall **439** of the first two (left-most) of adjacent ones of the stacks **305**, respectively. Thus, the second select gate drain line **401** is electrically coupled to the second set of the control gates **431**, with a respective one of the second set of control gates **431** in every other trench. The second set of control gates **431** and levels of the semiconductor material **301** in each of the four left-most ones of the stacks **305** form second select gate drain transistors, each of which controlling current flow through a respective string of memory cells formed along one respective sidewall **437**, **439**, **445**, **447** of each of the four left-most ones of the stacks **305**. Similarly, the first set of control gates **435** and levels of the semiconductor material **301** in each of the four right-most ones of the stacks **305** form first select gate drain transistors, each of which controlling current flow through a respective string of memory cells formed along one respective sidewall **441**, **443**, **449**, **451** of each of the four right-most ones of the stacks **305**. As shown in the example of FIG. **4**B, each of the stacks **305** has four levels of the semiconductor material **301**. Consequently, a total of 24 select gate transistors are formed between the total of five of the stacks **305** and first and second set of control gates **431**, **435** shown in FIG. **4**B. In various embodiments, other numbers of select gate transistors can be formed.

Each of the select gate drain transistors can control the current flowing through a respective sidewall of a respective one of the levels of the semiconductor material **301** and, as a result, the current flowing through a string of memory cells built along that sidewall of a respective one of the stacks **305**. A more detailed description and process of fabricating the memory cells is given, by way of example, with reference to FIGS. **5**A through **5**K, below.

FIG. **4**C shows a cross-sectional view **450** of Section Y'-Y' of the three-dimensional representation of the dual select gate drain architecture **430** of FIG. **4**B. Although the cross-sectional view **450** is similar to the cross-sectional view **390** of FIG. **3**E, the charge storage structures **391** disposed between the levels of the semiconductor material **301** in the stacks **305** and the control gates **431** (of FIG. **4**B) are not shown so as to more clearly illustrate the alternating nature of the control gates **435**. Based on at least FIG. **3**E, FIG. **4**C, and reading the disclosure provided herein, a person of ordinary skill in the art will readily understand how to fabricate and operate the various select gate transistors and strings of memory cells described. As noted above, a respective string of memory cells may be formed along a sidewall of each level of the semiconductor material **301** in each stack **305**.

FIGS. **5**A through **5**K show various portions of a fabrication process to form strings of memory cells, according to an embodiment. As discussed above, the techniques and fabrication processes described herein can be extended to a number of different apparatuses to be fabricated using a three-dimensional process. However, fabrication of strings of memory cells will be described below to retain clarity and consistency in the discussions that follow.

In FIG. **5**A, a substrate **501**A has been etched or otherwise partially opened to form an opening **505** therein. The substrate **501**A can include, for example, any of various types of substrates used in the semiconductor and allied industries (which are referred to herein as "semiconductor substrates"). Substrate types may therefore include silicon wafers, compound wafers, thin film head assemblies, polyethyleneterephthalate (PET) films deposited or otherwise formed with a semiconducting layer, or numerous other types of substrates known independently in the art. Also, the substrate may comprise a region of a semiconductor material formed over a non-semiconductor material, or vice-versa. For ease of understanding the fabrication activities that follow, the substrate **501**A may be considered to be a silicon wafer. Upon reading and understanding the disclosure provided herein, a person of ordinary skill in the art will understand how to modify the fabrication activities to account for other types of materials and electronic devices.

In one embodiment, the opening **505** is a trench. In other embodiments, the opening can be comprised of geometries other than a trench. However, for ease in understanding fabrication of the inventive subject matter discussed herein, the opening **505** can be considered to be a trench. In a specific example, the opening **505** is 1000 Å wide and may be formed to any depth as discussed, by way of example, below. In a specific embodiment, the opening **505** can be formed by an anisotropic dry etch process (e.g., reactive ion etch (RIE) or plasma etch). In other embodiments, the opening **505** may be formed by various types of chemical anisotropic etchants (e.g., such as potassium hydroxide (KOH) or tetramethyl ammonium hydroxide (TMAH)), mechanical techniques, other types of ion milling, or laser ablation techniques. In the case of a chemical etchant, various lattice planes in, for example, single crystal materials can assist in vertical sidewall formation. However, in other embodiments, vertical sidewall formation is not necessary and a sidewall slope to the opening **505** may be considered in certain applications. Related industries such as micro-electrical mechanical systems (MEMS) may independently supply techniques for still further means to form the opening **505**.

A hard mask **503** is formed over the substrate **501**A. The hard mask **503** may comprise, for example, a photoresist layer or other type of applied material that is resistant to various ones of the chemical process activities discussed, by way of example, below. Further, although the process actions may refer to particular dielectric materials, such as silicon dioxide, silicon nitride, or others, a person of ordinary skill in the art and familiar with this disclosure will recognize that other dielectric materials may be substituted and still be within a scope of the inventive subject matter. Thus, the material choices and selections presented are merely provided as an aid in understanding one example of a fabrication process.

In FIG. **5**B, a silicon dioxide liner **507**A may be formed over the substrate **501**A (including on the sidewalls and bottom of the opening **505**) and the hard mask **503**. A silicon nitride fill **509**A is then applied, deposited, or otherwise formed over the silicon dioxide liner **507**A. Although the example in FIG. **5**B shows the silicon nitride fill **509**A completely covering the silicon dioxide liner **507**A, it is sufficient to only partially fill a lower-most portion of a cavity (e.g., to cover the closed end of the cavity) formed within the silicon dioxide liner **507**A.

In FIG. **5**C, the silicon nitride fill **509**A is etched back or otherwise partially removed to form a first (silicon nitride) block **509**B. In a specific example, the first block **509**B may be from about 200 Å to about 300 Å (e.g., 20 nm to 30 nm) in thickness.

In FIG. **5**D, a silicon dioxide fill **511**A is then applied, deposited, or otherwise formed over the first block **509**B. As with the silicon nitride fill **509**A discussed above, the silicon dioxide fill **511**A may only partially fill the cavity remaining over the first block **509**B.

FIG. **5**E shows the silicon dioxide fill **511**A after being etched back or otherwise partially removed to form a second (silicon dioxide) block **511**B. In a specific example, the second block **511**B may be from about 100 Å to about 400 Å (e.g., 10 nm to 40 nm) in thickness. In other examples, the second block may be from about 100 Å to about 200 Å (e.g., 10 nm to 20 nm) in thickness. Portions of the silicon dioxide liner **507**A may also be removed during the partial removal of the silicon dioxide fill **511**A leaving a reduced silicon dioxide liner **507**B. The dimensions shown are merely provided as an aid in understanding and may vary considerably depending on, for example, different apparatuses or design rules.

With reference now to FIG. **5**F, the process discussed by way of example above with reference to FIGS. **5**B through **5**F may be repeated any number of times to form an alternating arrangement of the first blocks **513**A (e.g., including the first block **509**B) and the second blocks **515**A (including the block **511**B) within opening **505**. As further discussed above, each of the blocks may comprise different materials other than those shown. As readily understood by a person of ordinary skill in the art upon reading and understanding the disclosure provided herein, any number of materials may be selected for the blocks provided there is an etch or chemical consumption rate difference between adjoining blocks and the substrate **501**A. For example, alternating layers of aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) can be substituted for the silicon nitride and silicon dioxide blocks. Also, various other combinations may also be substituted or included.

Further, one or more of the various blocks may include more than one material type provided etch or chemical consumption differences, discussed above, are considered. Depending upon which of the blocks is last etched or otherwise partially removed, a dielectric liner **507**C may be present on the hard mask **503** as shown. The dielectric liner **507**C still separates the various blocks from the substrate **501**A in either case. For example, if the final material removed in the process is silicon nitride, the dielectric liner **507**C may be on the hard mask **503**. Alternatively, if the final material removed in the process is silicon dioxide, then the dielectric liner **507**C may not be present on the hard mask **503**.

Further, FIG. **5**F shows a first block **509**B, **513**A on both the bottom and top of the alternating arrangement. However, there is no requirement for this arrangement. For example, a second block **515**A, **511**B may be formed on the top and bottom of the alternating arrangement. Alternatively, a second block **511**B may be formed on the bottom and a first block **513**A on the top of the alternating arrangement, or vice versa. The final arrangement may be based on, for example, the particular apparatus being formed.

With reference now to FIG. **5**G, a second opening **517** is formed within the alternating arrangement (e.g., through the various blocks previously fabricated). The second opening may be formed by, for example, a dry etch process, such as a reactive ion etch (RIE) or various types of plasma etch. Alternatively or in conjunction, mechanical milling, ion milling, laser ablation, sputter etch, or vapor phase etchants may be used to form the second opening **517**. Forming the second opening forms an alternating arrangement of first sidewall (silicon nitride) blocks **513**B, **509**C and second sidewall (silicon dioxide) blocks **515**B, **511**C.

In a specific example, the second opening **517** may be formed such that a resulting width of the sidewall blocks is about 200 Å to about 300 Å. As discussed above with reference to FIG. **5**A, the opening **505** was described as a trench about 1000 Å wide, W_1. Thus, since the width, t_1, of the sidewall blocks on each side of the trench is about 300 Å and the opening **505** (FIG. **5**A) was about 1000 Å wide, a resultant width of the second opening can be about 400 Å wide. However, these numbers are merely provided as examples and may vary depending on a number of factors such as the apparatus being fabricated, a depth of the opening **505**, and an overall density of memory cells selected for a given design.

With concurrent reference to FIGS. **5**G and **5**H, the second sidewall blocks **515**B, **511**C and portions of the dielectric liner **507**C underlying the second sidewall blocks are etched or otherwise removed to expose portions of the substrate **501**A. After these silicon dioxide areas are removed, the first sidewall blocks **509**C, **513**B, and portions of the dielectric liner **507**D underlying the first sidewall blocks remain within the second opening **517**. A subsequent removal of at least a portion of the exposed portions of substrate **501**A occurs by, for example, use of an anisotropic removal activity.

In a specific example, the anisotropic removal activity may be performed with an etchant, such as TMAH, leaving an etched substrate **501**B. If the substrate **501**A is selected to be silicon or another single crystal material, an orientation may be selected to open a number of lateral openings **519** that are substantially perpendicular (i.e., about a 90° lateral etch) to the second opening **517**. For example, both a <100> and a <111> oriented silicon will etch with the lateral openings being substantially perpendicular to the second opening **517**. The etchant may be chosen to have a high etch selectivity between the silicon nitride and the substrate and high etch selectivity between crystal orientations. Both TMAH and KOH have a high etch selectivity rate difference between silicon nitride or silicon dioxide and silicon. KOH may also be used as a chemical etchant provided that potential potassium contamination is not a concern for a particular device being fabricated.

In other specific examples, other chemicals may be used for an anisotropic silicon etch. In addition to TMAH and KOH, ethylene-diamene-pyrocatechol (EDP) may also be an effective etchant. Although primarily anisotropic etchants have been discussed, isotropic etchants may also be employed. For example, a hydrofluoric/nitric/acetic (HNA) acid chemical etchant may be used.

Referring now to FIG. **5**I, an embodiment is shown for forming stacks of alternating levels of semiconductor material levels of dielectric material. Since the lateral openings **519** of FIG. **5**H were only partially etched through, a substrate pillar portion **523** was left between adjacent ones of the lateral openings **519**. In FIG. **5**I the lateral openings **519** of FIG. **5**H are now filled with, for example, a thermally grown silicon dioxide, creating a number of filled areas **521**. Alternatively,

rather than a thermally grown oxide, the filled areas **521** can be formed by a deposition process such as chemical vapor deposition (CVD), atomic level deposition (ALD), physical vapor deposition (PVD), or other techniques known independently in the art. The filled areas **521** formed in the lateral openings **519** between portions of the substrate **501**D. Depending upon the thickness of the substrate pillar portion **523**, the thermal oxidation process used to form the filled areas **525** in the example just described may completely consume the substrate pillar portion **523** as discussed, by way of example, with reference to FIG. **5**J-**2**, below. However, the device will still function with the substrate pillar portion **523** remaining.

In FIG. **5**J-**1**, the first sidewall blocks **509**C, **513**B have been removed. The first sidewall blocks **509**C, **513**B may be removed by various etchants or other means as discussed herein. Also, the remaining portions of the dielectric liner **507**D may optionally be removed and replaced by a higher quality dielectric **507**E, such as a tunnel oxide material. The tunnel oxide material may be, for example, a thermally grown silicon dioxide material. As can further be seen from FIG. **5**J-**1**, at least one material in the stack of alternating materials is substantially coplanar with a bottom portion of the number of trenches (see also FIGS. **3**E and **4**C).

FIG. **5**J-**2** is similar to the structure of FIG. **5**J-**1**. However, each of the substrate pillar portions **523** has been consumed by the thermal oxidation process as discussed above with reference to FIG. **5**I.

FIG. **5**K shows an elevational view of a completed portion of a stack of alternating levels of semiconductor material and dielectric material. The elevational view of FIG. **5**K may be similar to the cross-sectional view **390** of Section Y-Y of FIG. **3**E. The elevational view shows a number of the charge storage structures **391** that have been added and disposed between each level of the semiconductor material **301** and each control gate **313** in the stack **305**. Each of the charge storage structures **391** forms a memory cell element for a total of the 15 memory cell elements as viewable from FIG. **5**K. As noted above, a respective string of memory cells is disposed along a sidewall at each level of the semiconductor material **301** of the stack **305**. Consequently, each of the 15 memory cell elements shown in FIG. **5**K comprises one respective cell within a respective string. The control gates **313**, the charge storage structures **391**, and the access line **309** may be formed from, for example, polysilicon or some other conductor, using techniques such as those already known in the art.

The fabrication techniques and apparatuses resulting therefrom described, by way of example above, may use single crystal silicon as a string channel (e.g., see FIG. **3**B). However, the three-dimensional stacks (e.g., the stacks **305** of FIG. **3**A et seq.) can advantageously be used to increase cell density while maintaining a relatively small footprint. Further, the fabrication techniques and architectures resulting therefrom can be extended to NOR devices, microcontroller devices, other memory types, general purpose logic, or a host of other apparatuses. Various three-dimensional devices, repeating devices (e.g., SRAM), transistors, standard CMOS logic, and so on may all benefit from application of the three-dimensional processes disclosed herein.

With reference now to FIG. **6**, a block diagram of an illustrative embodiment of an apparatus in the form of a system **600** including one or more memory devices (e.g., the memory device **101** of FIG. **1**) is shown. The system **600** may be used in devices such as, for example, a personal digital assistant (PDA), a laptop or portable computer with or without wireless capability, a web tablet, a wireless telephone, a pager, an instant messaging device, a digital music player, a digital camera, or other devices that may be adapted to transmit or receive information either wirelessly or over a wired connection. The system **600** may be used in any of the following systems: a wireless local area network (WLAN) system, a wireless personal area network (WPAN) system, or a cellular network.

The system **600** of FIG. **6** is shown to include a controller **603**, an input/output (I/O) device **615** (e.g., a keypad or a display), the memory device **101** of FIG. **1**, a wireless interface **611**, and a static random access memory (SRAM) device **601** electrically coupled to each other via a bus **609**. A battery **605** may supply power to the system **600** in one embodiment. The memory device may include a NAND memory, a flash memory, a NOR memory, a combination of these, or the like.

The controller **603** may include, for example, one or more microprocessors, digital signal processors, micro-controllers, or the like. The memory device **101** may be used to store messages transmitted to or by the system **600**. The memory device **101** may optionally also be used to store instructions that are executed by the controller **603** during operation of the system **600** and may be used to store user data either generated, collected, or received by the system **600** (such as image data). The instructions may be stored as digital information and the user data, as disclosed herein, may be stored in one section of the memory as digital data and in another section as analog memory. As another example, a given section at one time may be labeled to store digital information and then later may be relabeled and reconfigured to store analog information.

The I/O device **615** may be used to generate a message. The system **600** may use the wireless interface **611** to transmit and receive messages to and from a wireless communication network with a radio frequency (RF) signal. Examples of the wireless interface **611** may include an antenna, or a wireless transceiver, such as a dipole antenna. However, the scope of the inventive subject matter is not limited in this respect. Also, the I/O device **615** may deliver a voltage reflecting what is stored as either a digital signal (if digital information was stored), or as an analog signal (if analog information was stored). While an example in a wireless application is provided above, embodiments of the inventive subject matter disclosed herein may also be used in non-wireless applications as well.

The various illustrations of apparatus (e.g., the memory device **101** and examples of the various fabrication stages illustrated with reference FIGS. **5** through **5**K) are intended to provide a general understanding of the structure of various embodiments and are not intended to provide a complete description of all the elements and features of the apparatus that might make use of the structures, features, and materials described herein.

The apparatus of the various embodiments may include or be included in, for example, electronic circuitry used in high-speed computers, communication and signal processing circuitry, single or multi-processor modules, single or multiple embedded processors, multi-core processors, data switches, and application-specific modules including multilayer, multi-chip modules, or the like. Such apparatuses may further be included as sub-components within a variety of electronic systems, such as televisions, cellular telephones, personal computers (e.g., laptop computers, desktop computers, hand-held computers, tablet computers, etc.), workstations, radios, video players, audio players, vehicles, medical devices (e.g., heart monitors, blood pressure monitors, etc.), set top boxes, and various other electronic systems.

One skilled in the art will appreciate that, for this and other methods disclosed herein, the methods may be implemented

in a differing order. Further, the outlined acts and operations are only provided as examples, and some of the acts and operations may be optional, combined into fewer acts and operations, or expanded into additional acts and operations without detracting from the essence of the disclosed embodiments.

The present disclosure is therefore not to be limited in terms of the particular embodiments described in this application, which are intended as illustrations of various aspects. For example, instead of floating gate flash memory devices, charge trap memory devices may be used. Many modifications and variations can be made, as will be apparent to a person of ordinary skill in the art upon reading and understanding the disclosure. Functionally equivalent methods and devices within the scope of the disclosure, in addition to those enumerated herein, will be apparent to a person of ordinary skill in the art from the foregoing descriptions. Portions and features of some embodiments may be included in, or substituted for, those of others. Many other embodiments will be apparent to those of ordinary skill in the art upon reading and understanding the description provided herein. Such modifications and variations are intended to fall within a scope of the appended claims. The present disclosure is to be limited only by the terms of the appended claims, along with the full scope of equivalents to which such claims are entitled. It is also to be understood that the terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting.

The Abstract of the Disclosure is provided to comply with 37 C.F.R. §1.72(b), requiring an abstract allowing the reader to quickly ascertain the nature of the technical disclosure. The abstract is submitted with the understanding that it will not be used to interpret or limit the claims. In addition, in the foregoing Detailed Description, it may be seen that various features are grouped together in a single embodiment for the purpose of streamlining the disclosure. This method of disclosure is not to be interpreted as limiting the claims. Thus, the following claims are hereby incorporated into the Detailed Description, with each claim standing on its own as a separate embodiment.

What is claimed is:

1. An apparatus comprising:

a stack comprising a number of levels of semiconductor material and a number of levels of dielectric material, each of the levels of semiconductor material being doped on at least one respective sidewall of the semiconductor material, a substantial remainder of each of the levels of semiconductor material being doped with a material having a predominant charge carrier that is opposite that of the dopant used on the at least one respective sidewall, each of the levels of semiconductor material being separated from a respective adjacent one of the levels of semiconductor material by at least a respective one of the levels of dielectric material, adjacent ones of the levels of semiconductor material being coupled together by a pillar of semiconductor material, at least one end of the stack being formed into a staircase structure with overlying levels of the stack on the at least one end being stepped back from underlying ones of the number of levels of semiconductor material thereby forming the staircase structure, the at least one respective sidewalls each being coupled to a separate respective sidewall contact line at an appropriate level of the staircase structure, the remainder of each of the levels of semiconductor material being coupled to a separate respective body contact line at an appropriate level of the staircase structure, a respective string of memory cells being formed along each of the levels of semiconductor material.

2. The apparatus of claim **1**, wherein the semiconductor material comprises single crystal silicon.

3. The apparatus of claim **1**, wherein each of the levels of semiconductor material comprises opposing ones of a first sidewall and a second sidewall, wherein a respective one of the strings of memory cells formed along a respective one of the levels of semiconductor material comprises:

a first string of memory cells formed along the first sidewall of the respective level of semiconductor material; and

a second string of memory cells formed along the second sidewall of the respective level of semiconductor material.

4. The apparatus of claim **1**, wherein each of the levels of semiconductor material is comprised of a same semiconductor material.

5. The apparatus of claim **1**, wherein each of the levels of dielectric material is comprised of a same dielectric material.

6. The apparatus of claim **1**, wherein each of the levels of semiconductor material are formed from a common substrate.

7. The apparatus of claim **1**, wherein each of the levels of semiconductor material being separated from a respective adjacent one of the levels of semiconductor material by at least a respective one of the levels of dielectric material comprises each of the levels of semiconductor material being completely separated from a respective adjacent one of the levels of semiconductor material by a respective one of the levels of dielectric material.

8. The apparatus of claim **1**, wherein the apparatus comprises a memory device.

9. The apparatus of claim **3**, wherein the first sidewall and the second sidewall of the respective one of the levels of semiconductor material comprise regions of a first diffusion type separated by a region of a second diffusion type.

10. The apparatus of claim **3**, wherein a common control gate is shared by a respective single memory cell of each of the strings formed along a respective one of the sidewalls of each of the levels of semiconductor material.

11. The apparatus of claim **10**, further comprising an adjacent stack, wherein the adjacent stack also comprises a number of levels of semiconductor material and a number of levels of dielectric material, wherein the common control gate is also shared by a respective single memory cell of each string of memory cells formed along a respective sidewall of each of the levels of semiconductor material in the adjacent stack.

12. The apparatus of claim **11**, wherein the stacks are separated by at least the common control gate.

13. The apparatus of claim **11**, wherein each of the memory cells sharing the common control gate comprises a respective charge storage structure, wherein the common control gate is separated from a respective one of the levels of semiconductor material of a respective one of the stacks by at least a respective one of the charge storage structures.

14. The apparatus of claim **11**, wherein the common control gate is electrically coupled to an access line formed over the stacks.

15. An apparatus comprising:

a base substrate having a number of openings formed therein; and

a stack formed between each of the number of openings, each stack having a number of levels of semiconductor material and a number of levels of dielectric material, each level of the number of levels of semiconductor material being separated from an adjacent level of semi-

conductor material by at least one of the number of levels of dielectric material, at least one end of the stack being formed into a staircase structure with overlying levels of the stack on the at least one end being stepped back from underlying ones of the number of levels of semiconductor material thereby forming the staircase structure, each of the levels of semiconductor material having a first side and an opposing second side; and

at least one string of memory cells being formed along at least one of the first side and the second side of the levels of semiconductor material.

16. The apparatus of claim **15**, further comprising:

a number of control gates disposed within the number of openings in the base substrate; and

a charge storage structure disposed between a portion of each of the number of control gates and at least one of the number of levels of semiconductor material.

17. The apparatus of claim **15**, wherein each of the number of levels of semiconductor material comprises silicon.

18. The apparatus of claim **15**, wherein each of the number of levels of dielectric material comprises silicon dioxide.

19. The apparatus of claim **15**, wherein the base substrate is a semiconductor material.

20. The apparatus of claim **15**, wherein the number of openings are adjacent trenches formed in the base substrate.

21. The apparatus of claim **16**, wherein each of the number of control gates is shared between a first stack and an adjacent second stack.

22. An apparatus comprising:

a base substrate having a number of openings formed therein; and

a multiple level structure formed between each of the number of openings, each multiple level structure having a number of levels of silicon material and a number of levels of silicon dioxide material, each level of the number of levels of silicon material being separated from an adjacent level of silicon material by at least one of the number of levels of silicon dioxide material, each of the levels of silicon material having a first side and an opposing second side;

at least one string of memory cells being formed on each of the first side and the second side of the levels of silicon material;

a number of control gates disposed within the number of openings in the base substrate;

a charge storage structure disposed between a portion of each of the number of control gates and at least one of the number of levels of silicon material; and

two select gate drain transistors coupled to alternating ones of the number of control gates.

23. An apparatus comprising:

a base substrate having a number of openings formed therein; and

a multiple level structure formed between each of the number of openings, each multiple level structure having a number of levels of silicon material and a number of levels of silicon dioxide material, each level of the number of levels of silicon material being separated from an adjacent level of silicon material by at least one of the number of levels of silicon dioxide material, at least one end of the multiple level structure being formed into a staircase structure with overlying levels of the multiple level structure on the at least one end being stepped back from underlying ones of the number of levels of semiconductor material thereby forming the staircase structure, each of the levels of silicon material having a first side and an opposing second side;

at least one string of memory cells being formed on each of the first side and the second side of the levels of silicon material;

a number of control gates disposed within the number of openings in the base substrate; and

a charge storage structure disposed between a portion of each of the number of control gates and at least one of the number of levels of silicon material.

24. An apparatus comprising:

a stack comprising a number of levels of semiconductor material and a number of levels of dielectric material, each of the levels of semiconductor material being separated from a respective adjacent one of the levels of semiconductor material by at least a respective one of the levels of dielectric material, at least one end of the stack being formed into a staircase structure with overlying levels of the stack on the at least one end being stepped back from underlying ones of the number of levels of semiconductor material thereby forming the staircase structure, a respective string of memory cells being formed along each of the levels of semiconductor material, each of the levels of semiconductor material comprising opposing ones of a first sidewall and a second sidewall, the first sidewall and the second sidewall each having a dopant material of a first type, a substantial remainder of each of the levels of semiconductor material having a dopant material of a second type that has a predominant charge carrier that is opposite that of the dopant material of the first type, a respective one of the strings of memory cells formed along a respective one of the levels of semiconductor material comprises:

a first string of memory cells formed along the first sidewall of the respective level of semiconductor material; and

a second string of memory cells formed along the second sidewall of the respective level of semiconductor material.

* * * * *

Exhibit 18

January 23, 2018

Micron Launches Industry's First Enterprise SATA Solid State Drives Built on Leading 64-layer 3D NAND Technology

Micron 5200 SATA Enterprise SSDs Empower Fast, Consistent Quality of Service for Business-Critical Virtualized Workloads and Cloud Architectures

News Highlights

- Class-leading enterprise SATA SSD: capacity, performance, consistency and reliability.
- Same trusted, proven architecture as the well-regarded Micron 5100 series for easy qualifications, better performance and better value.
- Micron 5200 SSDs are available to purchase now from distributors.

BOISE, Idaho, Jan. 23, 2018 (GLOBE NEWSWIRE) -- Micron Technology, Inc. (Nasdaq:MU) today launched the Micron® 5200 series of SATA solid state drives (SSDs), maintaining industry-leading performance, consistency, capacity, reliability, and overall infrastructure value. Built on Micron's new industry-leading 64-layer 3D NAND technology, the Micron 5200 series of SSDs offers a cost-optimized SATA platform for business-critical virtualized workloads that cripple on a hard drive, such as OLTP, BI/DSS, VDI, block/object and media streaming.

Leveraging the proven architecture, performance and capacity of the well-regarded 5100 SATA SSDs, the Micron 5200 series is engineered to deliver a fast, easy and cost-effective enterprise storage solution to replace existing hard drives and legacy SSDs. Micron 5200 SSDs immediately deliver better total cost of ownership and improve data center efficiency through server and storage platform consolidation, reducing IT costs and simplifying infrastructure and maintenance. Now it is easier than ever before for enterprises to add more flash into the data center and get more out of server deployments.

Better SSDs Come from Better NAND

As the first SATA enterprise SSD available with 64-layer 3D NAND technology, the Micron 5200 SSDs deliver improved densities, throughput, consistency, and power efficiency — all at a better value. The quality of an SSD depends on the NAND it's built on, and the Micron 5200 series of SSDs is engineered to deliver improved reliability with the industry's lowest annualized drive failure rate for SATA enterprise SSDs according to data sheet specifications, offering better value with Micron's known silicon-to-system quality advantage.

"Micron 5200 SSDs unleash market-leading performance, capacity and reliability, paired with a rich feature set and unprecedented flexibility, adding up to the ideal storage solution for business-critical workloads," said Micron Storage Business Unit Vice President and General Manager Derek Dicker. "We simplified the server qualification process by leveraging the same foundational architecture that's currently available on Micron SATA SSDs. Customers can trust the same proven controller and firmware design while taking advantage of advanced flash media for better performance, quality of service, and value."

"Today's business-critical, virtualized workloads simply cannot run at peak, consistent performance on yesterday's technology," said Dedicated Computing Senior Vice President Sales and Marketing Dave Guzzi. "Customers need advanced storage technology to achieve better performance and reliability — and a lower total cost of ownership. Fortunately, Micron offers all this along with the ease of a common platform that leverages the same proven controller and firmware design as previous SSD generations."

"It says a lot that Micron chose to release its next-generation SSD based on the architecture of its prior generation while only changing the NAND from 32-layer to 64-layer technology," said Jim Handy of Objective Analysis. "This shows that the company and its customers are pleased with the performance and reliability of the earlier 5100 series and are open to migrating to a new flash technology in a way that minimizes requalification costs."

Join the SOLID Storage Revolution

Built on Micron's industry-leading 64-layer 3D NAND technology for enterprise SATA SSDs, the Micron 5200 series of SSDs

accelerates applications that need faster, more consistent performance, while offering overall infrastructure value and quality of service (QoS) at an improved total cost of ownership. Optimized for latency-sensitive, read-intensive workloads, these new SATA SSDs minimize storage bottlenecks with faster, predictable performance, making the move from hard drives to SSDs easier than ever before. Key features include:

- **Quality of Service —** The Micron 5200 SSDs deliver extremely efficient QoS, offering up to 99.7 percent better QoS when compared to a mission-critical hard disk drive.[1]
- **Unmatched Capacity —** Micron 5200 SSDs offer the industry's broadest SATA portfolio with capacities up to 7.68TB, twice the capacity of other SSDs on the market.
- **Leading Performance —** Engineered for fast random IO performance that fuels virtualized applications, Micron 5200 SSDs deliver up to 95k IOPS random reads and best-in-class 33,000 random writes, delivering strong performance in both areas. The drive is also highly flexible, as data center managers can use the innovative Flex Capacity feature to adjust the drive's endurance, performance, and capacity to meet ever-changing workload demands.
- **Leader in MTTF Offering —** Micron 5200 SSD data sheet specifications offer a mean time to failure (MTTF) of 3 million device hours, compared to the industry average for SATA enterprise SSD specifications of 2 million hours MTTF.
- **Easy to Manage —** A fast, easy, affordable way to extend the life of existing server deployments, Micron 5200 SSDs are hot-swappable, easy to install, and only take minutes to configure, saving both time and money on setup and maintenance.

The Micron 5200 series of SSDs offers varying levels of performance and endurance to meet the diverse needs of low-latency, read-intensive workloads. Visit the Micron 5200 series SSD product flyer for additional information on the feature and function advantages. Micron 5200 SSDs are designed to replace 10K RPM hard drives and help IT managers deliver better performance and capacity — all while using less power. As an example, in an OLTP workload environment, a *single* Micron SSD allows you to get 3X more IOPS performance than an entire rack of 24 10K RPM hard drives.

- **5200 ECO SATA SSD —** Scale storage with fast, vast, built-to-last SSDs. Scale data center capabilities easily and efficiently. With capacities up to 7.68TB in a 2.5" form factor, the Micron 5200 ECO SSD meets and surpasses the capacity per unit of rack space and cost advantages that had been previously owned by HDDs. Specially designed for read-intensive workloads, the Micron 5200 ECO SSD provides cloud services and content sharing companies a reliable, easy-to-deploy SATA storage solution that works within existing infrastructure deployment models to deliver radically faster performance than an HDD − and a significantly better value.
- **5200 PRO SATA SSD —** An all-purpose drive to power read-intensive workload demands. Micron 5200 PRO SSDs are an all-purpose drive to power read-intensive workloads that require higher random write performance and endurance. The Micron 5200 PRO is quick to respond and deliver on the unforecasted demand of today's application workloads, including burst-driven transaction waves or sudden high volume web traffic. For IT administrators needing to ensure fast data throughput to keep their business running smoothly at all times, the Micron 5200 PRO SSD is a known storage workhorse and is engineered to deliver consistently fast, leading performance.

Micron 5200 SSDs are available now for OEM qualification and for purchase through distributors, such as ASI, Avnet, CDW, Ingram, Microland, WPG-Americas, Synnex and others. For more information, visit https://www.micron.com/products/solid-state-storage/product-lines/5200#.

Resources:

- Media Kit: Micron® 5200 SSDs - http://bit.ly/2E02N62
- Blog: www.micron.com/about/blogs
- Twitter: www.twitter.com/MicronStorage
- LinkedIn: www.linkedin.com/company/micron-storage
- YouTube: Micron® SATA SSDs vs. HDDs

About Micron Technology, Inc.

Micron Technology is a world leader in innovative memory solutions. Through our global brands — Micron, Crucial® and Ballistix® — our broad portfolio of high-performance memory technologies, including DRAM, NAND, NOR Flash and 3D XPoint™ memory, is transforming how the world uses information. Backed by nearly 40 years of technology leadership, Micron's memory solutions enable the world's most innovative computing, consumer, enterprise storage, data center, mobile, embedded, and automotive applications. Micron's common stock is traded on the Nasdaq under the MU symbol. To learn more about Micron Technology, Inc., visit micron.com.

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[1] Compared to a 15K RPM hard drive (600GB SAS 12Gb/s) vs Micron 5200 PRO 1920GB, Measurements performed on Intel Core i7-4790K @ 4.0GHz, Asus Maximum VII GENE motherboard, CentOS*6.5 64-bit, FIO* 2.2.6, Workload - 4KB Block Size, 100% Read, 100% Random, Queue Depth 32, 99.999% Quality of Service.

Exhibit 19

2023 Flash Memory Timeline

1952

MIT's Dudley Buck creates first semiconductor NVM from ferroelectric crystals.

1955

Bell Labs' Merz and Anderson create monolithic 256-bit FRAM ferroelectric NVM, the first monolithic memory chip.

1961

C.T. "Tom" Sah of Fairchild envisions floating gate NVM using charge storage on the gate electrode of a MOS tetrode transistor.

1965

Dov Frohman-Bentchkowsky writes Berkeley PhD thesis "Charge Transport and Trapping in MNOS Structures and its Memory Applications" and builds a 9-bit prototype.

1966

Edgar A. Sack, Ting L. Chu and others of Westinghouse use a Metal-Nitride-Oxide-Silicon (MNOS) structure as a charge-trapping element.

1967

Dawon Kahng and Simon Sze (2014 FMS Lifetime Achievement Awardee) invent the Non-Volatile Memory Floating Gate at Bell Labs; this is published as "A Floating Gate and Its Application to Memory Devices" (Bell System Technical Journal).

John R. Szedon (2020 FMS Lifetime Achievement Awardee) and Ting L. Chu of Westinghouse propose using a charge trap as a nonvolatile memory bit at the IEEE Solid State Device Research Conference.

1968

Stanford R. Ovshinsky announces the Ovonic Memory Switch, the basis for 3D XPoint memory as announced by Intel and Micron in 2015, and as later productized by Intel as Optane.

1970

Dov Frohman-Bentchkowsky invents the Erasable Programmable Read-Only Memory (EPROM) at Intel.

After work with Stanford R. Ovshinsky, Intel's Gordon Moore co-authors article for Electronics Magazine on the first demonstration of Phase Change Memory (PCM), the NVM technique used by 3D XPoint as announced by Intel and Micron in 2015, and as later productized by Intel as Optane.

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2023 Flash Memory Timeline

1971

Dov Frohman-Bentchkowsky presents "A fully-decoded 2048-bit electrically-programmable MOS ROM" paper describing the EPROM at the IEEE International Solid-State Circuits Conference (ISSCC) in Philadelphia, PA. His "Memory Behavior in a Floating-Gate Avalanche-Injection MOS (FAMOS) Structure" paper as published in Applied Physics Letters cites the 1967 Kahng/Sze Bell Labs Floating Gate publication.

1972

Toshiba's Iizuka, Masuoka and others introduce the first double-layered polysilicon memory cell with Floating Gate electrical erase as Stacked-Gate Avalanche-Injection Type MOS (SAMOS) Memory at the Conference on Solid State Devices and Materials in Tokyo. Fujio Masuoka goes on to receive the 2013 FMS Lifetime Achievement Award.

1974

General instrument ships EAROM, the first commercial EEPROM.

1975

Hitachi files for patent on NAND-type MROM.

Portable digital camera invented at Eastman Kodak Company with digital image storage on a cassette tape.

1976

Eli Harari (2012 and 2022 FMS Lifetime Achievement Awardee), then of Hughes Microelectronics, files for patent on first practical floating gate EEPROM using thin SiO2 and Fowler-Nordheim tunneling for program and erase.

1977

Eli Harari (2012 and 2022 FMS Lifetime Achievement Awardee), then of Hughes Microelectronics, publishes "Conduction and Trapping of Electrons in Highly Stressed Thin Films of Thermal SiO_2" (Applied Physics Letters).

P.C.Y. Chen of Fairchild introduces SONOS charge trap NVM cell in IEEE Transactions on Electron Devices paper.

Patent granted to TI's Gerald Rogers for mask ROM configured as a NAND array to reduce chip area and cost.

1978

Eli Harari (2012 and 2022 FMS Lifetime Achievement Awardee), then of Hughes Microelectronics, publishes "Dielectric Breakdown in Electrically Stressed Thin Films of Thermal SiO_2" (Journal of Applied Physics).

Hughes Microelectronics introduces first CMOS NOVRAM 256-bit chip (non-volatile SRAM) employing Fowler Nordheim floating gate EEPROM at IEEE ISSCC in San Francisco.

George Perlegos (2017 FMS Lifetime Achievement Awardee) designs the Intel 2816, which was introduced in 1980 and became the first commercially successful EEPROM.

1979

IEEE Solid State Circuits publishes paper titled "An Electrically Alterable Non-Volatile Memory Cell Using Floating Gate Structure" by Guterman, Rinawi, Chieu, Holvorson, and McElroy of Texas Instruments.

Hitachi presents paper describing 16K EEPROM using Silicon-Nitride-Oxide-Silicon (SNOS) charge trap technology at IEEE ISSCC in Philadelphia, PA.

2023 Flash Memory Timeline

1980 1981 1982 1983 1984 1985 1986 1987

Annual Flash Chip Revenue > **$ 1,600,000**

Hughes Microelectronics introduces the 3108, first CMOS EEPROM 8Kb chip employing Fowler Nordheim tunneling.

Intel introduces the 2816, a 16Kb HMOS EEPROM with a FLOTOX (floating gate tunnel oxide) structure employing Fowler-Nordheim tunneling, at IEEE ISSCC in San Francisco.

Fujitsu files for patent on improvements to Hitachi's 1975 MROM.

British scientist and inventor Kane Kramer designs first digital audio player (IXI) based on magnetic bubble memory chips.

SEEQ Technology presents paper at ISSCC in San Francisco introducing its 5213, the first EEPROM with an on-chip charge pump for in-system write and erase, an invention used in all flash memory devices.

Ramtron introduces first commercial FRAM NVM.

Intel introduces 2817A 16Kb EEPROM.

First paper describing flash EEPROM (later known as NOR flash) presented by Toshiba's Fujio Masuoka (2013 FMS Lifetime Achievement Awardee) at IEEE International Electron Devices Meeting (IEDM) in San Francisco.

Intel begins flash process development.

George Perlegos (2017 FMS Lifetime Achievement Awardee) founds ATMEL (which stands for "Advanced Technology for Memory and Logic").

Exel files for patent on first NOR Flash cell.

NEC's Kitamura files for first MLC (Multi-Level Cell) EPROM patent (in Japan).

Flash card concept introduced with ECC and on-card controller by Intel.

Intel forms unit focusing on solid state drives.

R. Stewart *et. al.* of RCA publish first paper on a NAND-configured UV-EPROM at IEEE VLSI Symposium.

Toshiba's Fujio Masuoka (2013 FMS Lifetime Achievement Awardee) presents paper on NAND flash memory at IEEE IEDM in Washington, DC; the 35th anniversary of this inventive paper was celebrated at the 2022 FMS.

Intel introduces NOR flash chips.

2023 Flash Memory Timeline

1988

$ 6,400,000

SunDisk founded by Eli Harari (2012 and 2022 FMS Lifetime Achievement Awardee) to develop new "System Flash" architecture combining embedded controller, firmware and flash to emulate disk storage, and files for first MLC (Multi-Level Cell) flash patent.

First flash memory sampled by Intel as 1Mb NOR chips. Intel's Design Team of Richard Pashley, Stefan Lai, Bruce McCormick and Niles Kynett go on to receive 2011 FMS Lifetime Achievement Awards.

Intel and Psion design flash-based mobile PC.

First flash-based digital camera, Fuji DS-1P, demonstrated.

150mm wafers used.

1989

$ 25,600,000

SunDisk files for patent on "System Flash" which describes on-chip cell management.

M-Systems founded and introduces Flash Disk concept (precursor to flash SSDs); M-Systems co-founders Dov Moran and Aryeh Mergi went on to receive 2018 FMS Lifetime Achievement Awards.

Intel ships 512Kb and 1Mb NOR flash.

Psion flash-based PC introduced.

Microsoft introduces Flash File System in joint effort with Intel.

DigiPro introduces 8MB NOR Flashdisk at Comdex.

Western Digital and SunDisk pioneer NOR-based SSD fully emulating an ATA HDD.

Personal Computer Memory Card International Association (PCMCIA) founded.

Silicon Storage Technology (SST) founded to produce NOR SuperFlash, compatible with a CMOS logic process.

1990

$ 100,000,000

Sony introduces EReader using flash memory.

Kodak flash-based camera prototypes shown.

PCMCIA sets standard on ATA PC Card form factor and pinout, using SunDisk "System Flash" specification for full HDD compatibility.

Intel 1MB and 4MB linear flash PCMCIA cards introduced.

Intel introduces 2Mb NOR chip.

SunDisk introduces first NOR flash SSD: 20MB 2.5", fully compatible with Conner peripherals 2.5" ATA HDD.

Toshiba verifies NAND flash chip operation, and begins 4Mb and 16Mb NAND flash chip development.

1991

$ 170,000,000

Kodak ships DCS-100, its first DCS at $13,000.

Zenith, Poqet and HP palm-sized notebook computers using flash memory cards shown at Spring Comdex.

1992

$ 295,000,000

Toshiba ships first mass-produced NAND flash chips (4Mb).

Information Storage Devices introduces flash-based voice recorder chip.

AMD introduces its first NOR product.

Fujitsu introduces its first NOR product.

M-Systems introduces TrueFSS, the first flash memory card FTL; this was later adopted by the PCMCIA as its FTL.

Intel launches second-generation FFS2.

Intel introduces 8Mb NOR flash chips and 4MB-20MB linear flash memory cards.

Intel introduces 1Mb "boot block" NOR flash with sectors for BIOS applications—first use of internal write state machine to manage flash write algorithm.

SunDisk introduces first serial 9Mb NOR Flash chip for SSD applications.

PCs begin using flash for BIOS storage.

The Joint Photographic Experts Group published the JPEG standard, enabling digital cameras to store compressed photos using media such as flash memory.

1993

$ 505,000,000

Toshiba ships 16Mb NAND flash chips, which enable portable storage with the first PCMCIA cards.

Datalight introduces "Card Trick" flash management software.

Apple introduces NOR flash-based Newton PDA.

Intel introduces 16Mb and 32Mb NOR flash.

Intel and Conner Peripherals introduce jointly-developed 5MB/10MB ATA flash disk drive.

AMD introduces 5-volt-only NOR using negative gate erase.

1994

$ 864,805,000

SunDisk introduces CompactFlash card.

Norris Communications introduces Flashback, the first portable digital voice recorder with flash memory.

0.5 micron process announced.

SunDisk introduces 18Mb Serial NOR flash chip for SSD applications.

M-Systems introduces NOR-based DiskOnChip.

1995

$ 1,860,089,000

Flash (NOR and NAND) revenues exceed $1B.

Casio introduces the QV-11 digital camera with flash rather than film or floppy.

Mitsubishi introduces DiNOR.

SunDisk changes name to SanDisk.

CompactFlash Association (CFA) founded.

2023 Flash Memory Timeline

1996

$ 2,610,603,000

$2.6B in flash memory revenues, 163,063% growth in 10 years.

Toshiba introduces SmartMedia Memory Card (also called Solid State Floppy Disk Card).

Samsung starts shipping NAND flash.

Kodak DC-25 is first DSC with CompactFlash card.

Datalight introduces "FlashFX" flash management software supporting NOR and NAND in a single driver.

SanDisk introduces world's first MLC (2 bits/cell) flash chip (80 Mb) in a CompactFlash (CF) card.

Palm introduces flash memory-based PDA.

0.35 micron process announced.

Lexar Media spins off from Cirrus Logic.

USB Association (USBA) founded.

1997

$ 2,701,678,000

500 million flash chips ship.

SaeHan Information Systems introduces flash-based MPMan MP3 player.

SanDisk and Siemens introduce MultiMedia Card (MMC and MMCplus).

Sony introduces the Memory Stick.

First cell phones ship with flash memory.

M-Systems introduces NAND-based DiskOnChip.

200mm wafers begin production.

SanDisk begins using 256 Mb MLC flash chips in its CompactFlash (CF) cards.

Intel introduces 2-bit/cell 64Mb MLC StrataFlash chip.

MultiMediaCard (MMC) unveiled by SanDisk and Siemens.

SanDisk begins transition from NOR to NAND flash.

Atmel introduces DataFlash based on SPI NOR and 8-pin interface, leading to widespread consumer product usage.

1998

$ 2,492,552,000

NOR revenues exceed $2B.

250nm process announced.

SaeHan Information Systems and licensee Eiger ship first mass-produced MP3 player (MPMan) with 32MB.

Diamond Rio introduces PMP300 MP3 player.

MultiMediaCard Association (MMCA) founded by 14 companies.

Apple iMac introduced without floppy but with USB, encouraging USB-based external storage.

USB Implementers Forum first publishes USB Mass Storage Class spec (finalized in 1999) to standardize USB-based storage.

1999

$ 4,560,493,000

NOR revenues exceed $4B.

Over one billion flash chips ship.

Toshiba and SanDisk create flash memory manufacturing joint venture.

Micron announces NOR products.

Hagiwara Sys-Com begins shipping FlashGate, a USB SmartMedia flash memory card drive.

Dov Moran (2018 FMS Lifetime Achievement Co-Awardee) is co-inventor on M-Systems patent filing for USB flash drive.

Lexar Media introduces CompactFlash-to-USB JumpSHOT.

Panasonic (Matsushita), SanDisk and Toshiba introduce SD memory card.

2000

$ 10,637,231,000

Flash (NOR and NAND) revenues exceed $10B.

M-Systems (working with IBM) and Trek Technology introduce USB flash drives.

Intel ships its one-billionth flash unit.

160nm process announced.

Panasonic (Matsushita), SanDisk and Toshiba establish SD Association to standardize and promote the Secure Digital memory card.

SLC NAND-based SD cards introduced in 8MB to 64MB capacities.

2001

$ 7,594,502,000

NAND revenues exceed $1B.

Toshiba and SanDisk announce 1Gb MLC NAND.

SanDisk introduces first NAND "System Flash" product.

Hitachi introduces AG-AND.

Samsung begins mass production of 512Mb flash memory device.

Saifun develops NROM with charge trap flash structure, the basis for Spansion's MirrorBit.

2002

$ 7,766,797,000

Olympus and FujiFilm introduce xD-Picture Card.

MMCmoblie card introduced by MMCA (MultiMediaCard Association).

Sony and SanDisk jointly introduce the Memory Stick PRO and half-size Memory Stick PRO Duo cards.

M-Systems introduces Mobile DiskOnChip, the first SSD in a chip; this was used in handsets by Nokia, Motorola and Ericsson.

AMD introduces MirrorBit using hot electron injection-based charge trap flash.

Cypress introduces Programmable System on Chip (PSoC) with first embedded SONOS using quantum mechanical tunneling-based charge trap flash.

130nm process announced.

2003

$ 11,739,282,000

NAND revenues exceed $5B.

SanDisk introduces miniSD card.

Sony and SanDisk jointly introduce Memory Stick PRO Micro.

Spansion spins out of AMD and Fujitsu.

Samsung introduces TaNOS structure, a technology later used in 3D NAND, at IEEE IEDM in Washington, DC.

2023 Flash Memory Timeline

2004

$ 15,610,575,000

NAND prices drop below DRAM prices.

U3 software system for USB flash drives introduced by SanDisk and M-Systems.

SanDisk and Motorola introduce TransFlash card, now the microSD card.

Datalight introduces multi-threaded "FlashFX Pro." management software to support multimedia NAND devices.

Spansion announces MirrorBit Quad 4-bit NOR.

90nm process announced.

Hynix and ST Micro form flash joint venture.

Hynix NAND product introduced.

Infineon NAND product introduced based on Saifun Charge Trap Flash.

Panasonic and Sanyo introduce first flash-based camcorders.

SanDisk introduces Flash Sansa MP3 players.

Freescale (later Everspin) ships first commercial MRAM NVM.

Pankaj Mehra and Sam Fineberg of Hewlett-Packard present Persistent Memory paper at IEEE Computer Society's 18th IPDPS.

2005

$ 18,568,940,000

NAND revenues exceed $10B.

Over three billion flash chips ship.

NAND GB shipments overtake those of DRAM.

Apple introduces first two flash-based iPods: iPod shuffle and iPod nano.

Microsoft introduces Hybrid Hard Disk Drive concept.

MMCmicro card introduced by MMCA.

70nm process announced.

Micron introduces NAND product.

2006

$ 20,076,313,000

Flash revenues exceed $20B.

First Flash Memory Summit held in San Jose.

Intel introduces Robson Cache Memory (now called Turbo Memory).

Microsoft introduces ReadyBoost.

SanDisk announces 3-bit MLC (aka TLC) NAND technology.

M-Systems announces 4-bit MLC technology.

SanDisk announces microSDHC card.

SanDisk acquires Matrix Semiconductor.

SanDisk acquires M-Systems.

Samsung and Seagate demonstrate first Hybrid Hard Disk Drives.

IMFT formed by Intel and Micron to manufacture NAND flash.

STEC acquires Gnutech.

Spansion introduces ORNAND flash.

56nm process announced.

300mm wafers begin production.

Micron acquires Lexar Media.

Open NAND Flash Interface (ONFi) V1.0 spec published.

Numonyx and Samsung introduce phase change NVM.

2007

$ 22,182,405,000

Flash revenues exceed $22B, almost 9 times 1997 revenues.

NAND revenues exceed $14.5B.

Non-Volatile Memory Host Controller Interface (NVMHCI) Working Group formed, with Intel's Amber Huffman as Chair.

Toshiba introduces eMMC NAND.

IMFT begins shipping 50nm NAND flash.

Toshiba introduces first SATA-based MLC SSD.

Apple introduces the iPhone.

Fusion-io announces 640GB ioDrive MLC NAND-based PCIe X4 board.

BiTMICRO launches 3.5" SSD with capacity of 1.6TB (for military applications).

Spansion acquires Saifun.

Several laptop MLC SSDs introduced with up to 128GB storage.

Dell introduces SSD option for laptop models.

Sub-$200 netbook computers introduced with flash memory storage.

Microsoft introduces flash-based Zune Player.

Seagate announces Hybrid Storage Alliance.

Seagate introduces first hybrid HHD, the Momentus PSD.

MMCA/JEDEC e.MMC spec published.

Toshiba presents 3D flash BiCS memory at IEEE VLSI Symposium.

2008

$ 18,435,970,000

NVMHCI 1.0 Spec released by Intel.

SanDisk introduces ABL to enable high speed MLC, TLC and X4 QLC NAND.

34nm process announced by Intel and Micron.

Toshiba introduces first 512GB MLC SATA-based SSD.

Intel and STMicro spin off Numonyx.

IBM demos first "Million IOPS" array.

EMC announces use of flash-based SSDs for enterprise SAN applications.

Apple introduces SSD-based MacBook Air with no HDD option.

Micron, Samsung and Sun Microsystems announce high-endurance flash memory.

Violin Memory introduces first fully flash-based storage appliance.

Samsung announces 150GB 2.5" MLC SSD with SATA II Interface.

Several companies announce MLC flash SSDs with up to 256GB for notebook apps.

Micron introduces first serial NAND flash.

Apple sells one million flash-based iPhones in 3 days.

MMCA merges into JEDEC.

SNIA Solid State Storage Initiative (SSSI) formed.

HGST releases first SSD with a SAS interface.

2009

$ 19,302,693,000

SanDisk and Toshiba present 4-bit/cell flash at IEEE ISSCC in San Francisco.

Intel and Micron introduce 34nm TLC NAND.

Samsung introduces first full HD camcorder with 64GB SSD.

Seagate enters SSD market.

SandForce introduces first compression-based SSD controller.

Virident and Schooner introduce first flash-based application appliances for the data center.

Pillar Data converts Axiom SANs to SSD.

WD acquires SiliconSystems and gets into SSD business.

NVELO introduces first PC flash caching software "Dataplex."

SanDisk introduces 100-year flash storage vault.

AgigA ships NAND-backed DIMM.

2010

$ 26,734,247,000

Toshiba introduces 128GB SD card based on 16-chip stack.

Intel, Micron introduce 25nm TLC and MLC NAND.

Numonyx acquired by Micron.

Microchip acquires SST.

Samsung Electronics begins producing 64Gb 3-bit NAND.

Samsung Electronics introduces high-speed 512GB SSD utilizing toggle-mode DDR NAND memory.

Seagate announces first self-managed hybrid HDD, Momentus XT, with 4GB NAND flash and 500GB HDD storage.

Universal Flash Storage Association (UFSA) founded.

JEDEC publishes two specs for Solid-State Drives: "SSD Requirements and Endurance Test Method" and "SSD Endurance Workloads."

2011

$ 28,123,615,000

LSI acquires SandForce.

SanDisk acquires Pliant.

IMFT introduces 20nm NAND flash.

Intel announces Smart Response Technology (SRT) SSD caching for PCs.

Seagate announces second generation Momentus XT hybrid HDD with 8GB NAND flash and 750GB HDD storage.

Apple acquires signal-processing controller IP firm Anobit.

Fusion-io acquires virtualization-aware flash caching software company IO Turbine.

NVMHCI renamed "NVM Express" (aka NVMe) and NVM Express Work Group established; NVMe Rev. 1.0 published.

JEDEC publishes first Universal Flash Storage (UFS) spec.

SNIA publishes two Solid State Storage Performance specs: Enterprise and Client.

JEDEC publishes Serial Flash Discoverable Parameters (SFDP) spec.

Facebook launches the Open Compute Project (OCP) to enable broad industry collaboration of open source software and scalable energy-efficient data center hardware.

Facebook launches the Open Compute Project (OCP) to enable broad industry collaboration of open source software and scalable energy-efficient data center hardware.

Intel's 1988 NOR Flash Memory Design Team of Richard Pashley, Stefan Lai, Bruce McCormick and Niles Kynett receive first FMS Lifetime Achievement Awards.

2023 Flash Memory Timeline

2012

$ 28,213,759,000

- SanDisk and Toshiba announce 19nm process in 128Gb chips at IEEE ISSCC in San Francisco.
- Ultrabooks ship with Smart Response Technology (SRT) SSD cache.
- Macronix and Winbond enter NAND business.
- Seagate introduces SSHD, a Hybrid Hard Drive (HHD) pairing flash with an HDD.
- Elpida introduces ReRAM.
- Micron and Intel introduce 20nm 128Gb NAND chip using hi-k planar cell.
- SK hynix formed upon SK Telecom's acquisition of controlling interest in Hynix Semiconductor.
- MOSAID samples 333GB/s HL-NAND.
- Adesto acquires ATMEL's Serial NOR business.
- DensBits Technologies introduces Memory Modem.
- Proximal Data introduces AutoCache.
- SanDisk acquires FlashSoft.
- EMC acquires XtremIO.
- OCZ acquires Sanrad.
- Samsung acquires NVELO.
- Intel acquires Nevex and introduces CacheWorks.
- LSI introduces Nytro flash with MegaRAID Cache-Cade caching software.
- Integrated Device Technology (IDT) introduces first NVMe SSD controller chip.
- Micron introduces 2.5" PCIe enterprise SSD.
- IBM acquires Texas Memory Systems.
- Cypress Semiconductor acquires Ramtron.
- Western Digital acquires HGST.
- JEDEC and ONFi introduce toggle mode.
- SNIA forms NVM Programming TWG.
- SanDisk founder Eli Harari receives FMS Lifetime Achievement Award.

2013

$ 29,797,262,000

- Samsung announces 24-layer 3D V-NAND at FMS and demos it in a 1TB SSD.
- 11 companies participate in first NVMe Plugfest.
- Diablo Technologies announces Memory Channel Storage tech.
- SMART Storage Systems incorporates Diablo Tech designs into ULLtraDIMM.
- SNIA NVDIMM SIG formed; many NVDIMM products introduced.
- Western Digital and SanDisk introduce SSHD using iSSD combined with a Hard Disk Drive.
- Toshiba introduces line of SSHDs.
- Everspin Technologies announces shipments of STT MRAM.
- Micron and others sample 16nm flash memory.
- SanDisk releases CFast 2.0 professional video memory card.
- M.2 PCIe interface formalized.
- Western Digital acquires sTec, Virident, Velobit.
- SanDisk acquires SMART Storage Systems.
- NVMdurance introduces software to extend flash endurance.
- Micron acquires Elpida.
- Intel introduces Intel Cache Acceleration Software.
- First UFS devices sampled by Toshiba at 8GB.
- Panasonic ships first commercial embedded ReRAM in an MCU.
- Adesto ships Mavriq CBRAM: first commercial stand-alone ReRAM.
- SNIA publishes NVM Programming Model V1.0.
- Fujio Masuoka, formerly of Toshiba, receives FMS Lifetime Achievement Award.

2014

$ 30,236,484,000

- Samsung, SanDisk and Toshiba announce 3D NAND production facilities.
- Samsung starts mass-producing the first 3D flash SSDs based on its second generation 32-layer Vertical NAND (V-NAND) using TLC.
- SanDisk introduces 4TB Enterprise SSD.
- Intel ships first NVMe SSD.
- SanDisk announces 128GB microSD card, a 1000x increase in capacity on device's 10th anniversary.
- IBM announces eXFlash DIMMs using SanDisk ULLtraDIMM's implementation of Diablo Memory-Channel Storage technology.
- Spansion introduces HyperFlash NOR with 333 MB/s HyperBus.
- Toshiba acquires OCZ.
- Everspin introduces and ramps production of ST-MRAM.
- Adesto ships one-millionth CBRAM.
- SK hynix acquires Violin Memory's PCIe SSD business.
- Seagate acquires LSI/Avago storage business.
- SanDisk acquires Fusion-io.
- HGST acquires Skyera.
- Samsung acquires Proximal Data.
- Simon Sze, formerly of Bell Labs, receives FMS Lifetime Achievement Award.

2015

$ 30,385,906,000

- Flash Memory Summit's 10th conference.
- SanDisk introduces InfiniFlash storage system.
- Cypress Semiconductor acquires Spansion.
- Toshiba, Samsung, and SanDisk announce 48-layer 3D NAND.
- Intel and Micron announce 256Gb 3D NAND.
- Samsung introduces first NVMe m.2 SSDs.
- SanDisk introduces 200GB microSDXC UHS-1 card.
- Cypress introduces 4MB serial FRAM.
- Intel and Micron announce 3D XPoint Memory.
- Intel announces 3D XPoint-based "Optane" DIMMs and SSDs.
- Micron introduces device with CMOS Under 3D NAND Array (CUA).
- SanDisk introduces 200GB microSD card.
- Mellanox and partners demonstrate pre-standard NVMe over Fabrics (NVMe-oF).
- Pure Storage has IPO.
- JEDEC publishes first DDR4 NVDIMM-N Persistent Memory Module spec.
- LightNVM and Open-Channel SSD support added to Linux kernel.
- Bob Norman, formerly of SanDisk and Micron, receives FMS Lifetime Achievement Award.

2016

$ 33,732,901,000

- All major vendors ship 3D NAND products.
- XMC breaks ground on first China-owned NAND flash fab.
- Micron introduces 768Gb 3D NAND.
- Western Digital acquires SanDisk.
- Everspin announces 256Mb MRAM chips.
- IBM adapts TLC to PCM.
- Samsung ships 48-layer 3D NAND.
- NVMe-oF (NVM Express over Fabrics) Rev. 1.0 published.
- NVMe-oF products demonstrated by at least 12 vendors.
- Toshiba introduces Through-Silicon Via (TSV) in 16-die stack NAND.
- Spin Transfer Technologies delivers fully functional ST-MRAM samples.
- Micron launches Xccela Consortium.
- Toshiba ships industry's first NVMe BGA "SSD on a chip."
- Western Digital demonstrates prototype of the first 1TB SDXC card.
- Adesto launches CBRAM-based Moneta family of ReRAM.
- SFF Committee becomes SNIA SFF Technology Affiliate.
- SNIA publishes Swordfish Scalable Storage Management API spec V1.0.0.
- Microsemi acquires PMC-Sierra.
- Kinam Kim, President of System LSI / Semiconductor Business at Samsung, receives FMS Lifetime Achievement Award.

2017

$ 49,176,520,000

- Flash Memory market exceeds size of entire 1990 semiconductor market.
- Microchip ships its 75-billionth SST SuperFlash-based device.
- SK hynix announces 72-layer 3D NAND.
- Toshiba migrates all new SSDs to 64-layer BiCS FLASH TLC.
- Intel ships Optane (3D XPoint) SSD.
- Intel's "Ruler standard" donated to Enterprise & Data Center SSD Form Factor (EDSFF) WG.
- HPE acquires Nimble Storage and Simplivity.
- Micron ships first string-stacked 3D NAND.
- Samsung and Toshiba/WD announce 96-layer 3D NAND.
- NGD Systems ships NVMe 24TB Computational Storage Device (CSD).
- Everspin samples 1Gb STT MRAM chip.
- Global Foundries introduces embedded eMRAM.
- WD develops TLC on 64-layer 3D NAND.
- JEDEC and SNIA win FMS Award for NVDIMM-N Standard.
- ScaleFlux first to deploy production-qualified Computational Storage.
- Eli Harari (2012 and 2022 FMS Lifetime Achievement Awardee) inducted into National Inventors Hall of Fame.
- George Perlegos, formerly of Intel, SEEQ and ATMEL, receives FMS Lifetime Achievement Award.

2018

$ 56,396,437,000

- Cypress introduces 16Mb FRAMs.
- Toshiba completes $18B memory business sale.
- Samsung launches high-speed Z-SSD.
- Micron ships Enterprise SSD using QLC and 1Tb 3D NAND die.
- Hyperstone introduces flash controllers with AI and Machine Learning.
- Intel samples Optane (3D XPoint) DC Persistent Memory DIMM.
- China's "Big Fund" Phase 2 targets over $30B for semiconductor investments.
- NVMe/TCP Transport Binding spec ratified by NVMe WG.
- SNIA forms Computational Storage Technical Work Group (TWG).
- Gyrfalcon Technology ships AI accelerator incorporating first use of TSMC's eMRAM.
- SNIA publishes Performance specs for Solid State Storage and for Real World Storage Workloads.
- Amber Huffman of Intel receives first FMS SuperWomen in Flash Leadership Award.
- Microchip acquires Microsemi.
- Dov Moran and Aryeh Mergi, M-Systems co-founders, receive FMS Lifetime Achievement Awards.

2019

$ 41,940,494,000

- All major vendors ship or sample 96-Layer NAND; SK hynix, Samsung and Micron sample 128-layer NAND.
- All leading foundries produce embedded MRAM (eMRAM).
- Lightbits Labs ships first commercial NVMe/TCP software-defined disaggregated storage.
- YMTC samples 32-layer "Xtacking" NAND.
- Intel ships Optane (3D XPoint) DIMMs.
- Micron ships first QLC enterprise SSDs.
- Intel ships SSDs with both Optane (3D XPoint) and QLC NAND.
- Open-Channel SSDs begin transition to NVMe Zoned Namespaces (ZNS).
- Computer Express Link (CXL) introduced, CXL Consortium incorporates, and V1.0 and V1.1 specs published.
- NGD Systems ships first scalable ASIC-based Computational Storage NVMe SSD.
- Eideticom ships first NVMe-based Computational Storage Processor.
- SNIA publishes Key Value Store API V1.0, and wins FMS Award.
- Toshiba Memory becomes KIOXIA.
- Phison and AMD ship first PCIe 4.0 x4 NVMe SSD and motherboard solution.
- Calline Sanchez of IBM receives FMS SuperWomen in Flash Leadership Award.
- Sanjay Mehrotra of Micron, and formerly of Intel, SEEQ, IDT, ATMEL, SanDisk and WD, receives FMS Lifetime Achievement Award.

2023 Flash Memory Timeline

2020 2021 2022 2023

$ 51,152,080,000 $ 58,817,659,000 $ 51,485,810,000 $ 33,781,640,000 (est)

Flash Memory Summit's 15th conference (held as a virtual online-only event).

WDC ships 112-layer BiCS 3D NAND as 512 Gbit TLC part.

KIOXIA ships first Automotive UFS at 512GB density.

Lightbits Labs ships first clustered, redundant, scale-out NVMe/TCP software solution.

Infineon acquires Cypress Semiconductor.

KIOXIA acquires LITE-ON Technology.

NVMe ZNS Command Set Spec V1.0 published.

NVMe Computational Storage Task Group formed.

Open Compute Project (OCP) publishes V1.0 specs: NVMe Cloud SSD and NVMe Datacenter SSD.

JEDEC publishes first DDR4 NVDIMM-P Persistent Memory Module spec.

JEDEC publishes DDR5 SDRAM standard and Universal Flash Storage (UFS) Card Extension 3.0 standard.

SNIA publishes specs for Native NVMe-oF and Cloud Data Mgmnt. Interface (CDMI).

KIOXIA ships first PCIe 4.0 x4 Enterprise NVMe SSD.

Dialog Semiconductor acquires Adesto Technologies.

DNA Data Storage Alliance launched.

Barbara Murphy of WekaIO receives FMS SuperWomen in Flash Leadership Award.

John R. Szedon, formerly of Westinghouse, receives FMS Lifetime Achievement Award.

NOR revenues exceed $3.6B, primarily for SPI NOR.

KIOXIA and WDC announce 162-layer 3D NAND.

SK hynix starts mass production of 176-layer "4D" NAND.

Samsung announces the first DRAM-based memory running on CXL, based on DDR5.

JEDEC publishes XFM (Crossover Flash Memory) Embedded and Removable Memory Device standard.

SK hynix completes first phase of Intel NAND and SSD business acquisition, to be branded as Solidigm.

NVIDIA launches GPUDirect Storage (GDS), providing a direct NVMe-to-GPU data path.

KIOXIA and Samsung announce PCIe 5.0 x4 Enterprise NVMe SSDs.

Renesas acquires Dialog Semiconductor.

NVMe 2.0 standard released as a set of 9 specs: base, 3 cmd. sets, 4 transports, and Management I/F.

Winbond dual-buffer NAND with SPI interface gets wide adoption for automotive code storage, including for Advanced Driver Assistance Systems (ADAS) and Over-the-Air (OTA) updates.

SNIA publishes Transport Layer Security (TLS) spec V2.0.

Samsung introduces SmartSSD computational storage drive (CSD).

35th anniversary of NAND Flash celebrated at FMS.

PCI-SIG releases PCIe 6.0 spec.

Universal Chiplet Interconnect Express (UCIe) V1.0 spec published to standardize die-to-die interconnects.

JEDEC publishes HBM3 update to High Bandwidth Memory (HBM) DRAM standard.

Micron ships 176-layer QLC 3D NAND.

Lightbits Labs ships first clustered NVMe/TCP software-defined public cloud storage solution.

Solidigm demonstrates prototype Penta-Level Cell (PLC) SSD.

CXL Consortium and JEDEC sign MOU to advance DRAM and Persistent Memory.

NVMe Boot Specification published.

JEDEC publishes UFS 4.0 standard and Automotive SSD standard.

DNA Data Storage Alliance joins SNIA as a Technology Affiliate.

SNIA publishes Computational Storage Architecture and Programming Model V1.0.

Yan Li of Western Digital receives FMS SuperWomen in Flash Leadership Award.

Yoshishige Kitamura (formerly of NEC), SanDisk founder Eli Harari (2012 FMS Lifetime Achievement Awardee), and Greg Atwood (formerly of Intel, Numonyx, and Micron) receive FMS Lifetime Achievement Awards.

SK hynix ships 238-layer TLC "4D" NAND using peripheral under cells (PUC) layout.

Micron ships 232-layer TLC 3D NAND with 6-plane architecture.

KIOXIA and Western Digital ship 218-layer TLC and QLC 3D NAND using 4-plane CMOS directly Bonded to Array (CBA) technology.

Solidigm ships first product: the P5430 enterprise SSD with 192-layer QLC NAND.

Lightelligence announces Photowave to enable CXL data storage connectivity over optics.

NVMe-oF Boot Open Source Reference Code available.

JEDEC publishes CMM specification for CXL-attached Memory Modules.

SCSI Trade Association (STA) becomes SNIA SCSI Trade Association Forum (STA Forum).

SNIA publishes Smart Data Accelerator Interface V1.0.

SNIA Swordfish V1.2.4a becomes an ISO Standard.

NEO Semiconductor launches 3D X-DRAM, the first 3D NAND-like DRAM.

Amy Fowler of Pure Storage receives FMS SuperWomen in Flash Leadership Award.

Amber Huffman of Google Cloud, and formerly of Intel, receives FMS Lifetime Achievement Award.

Exhibit 20

Micron Ships World's First 176-Layer NAND, Delivering A Breakthrough in Flash Memory Performance and Density

November 9, 2020

New 3D NAND boosts storage capability across mobile, automotive, client and data center applications

BOISE, Idaho, Nov. 09, 2020 (GLOBE NEWSWIRE) -- Micron Technology, Inc. (Nasdaq: MU), today announced that it has begun volume shipments of the world's first 176-layer 3D NAND flash memory, achieving unprecedented, industry-pioneering density and performance. Together, Micron's new 176-layer technology and advanced architecture represent a radical breakthrough, enabling immense gains in application performance across a range of storage use cases spanning data center, intelligent edge and mobile devices.

"Micron's 176-layer NAND sets a new bar for the industry, with a layer count that is almost 40% higher than our nearest competitor's," said Scott DeBoer, executive vice president of technology and products at Micron. "Combined with Micron's CMOS-under-array architecture, this technology sustains Micron's industry cost leadership."

Representing Micron's fifth generation of 3D NAND and second-generation replacement-gate architecture, Micron's 176-layer NAND is the most technologically advanced NAND node in the market. Compared with the company's previous generation of high-volume 3D NAND, Micron's 176-layer NAND improves both read latency and write latency by more than 35% — dramatically accelerating application performance[1]. Featuring approximately 30% smaller die size than best-in-class competitive offerings, Micron's 176-layer NAND's compact design is ideal for solutions using small form factors.

Groundbreaking technology arms diverse markets with the fullest power of flash

"Micron's 176-layer NAND enables breakthrough product innovation for our customers," said Sumit Sadana, executive vice president and chief business officer at Micron. "We are deploying this technology across our broad product portfolio to bring value everywhere NAND is used, targeting growth opportunities in 5G, AI, cloud and the intelligent edge."

With its versatile design and unrivaled density, Micron's 176-layer NAND serves as an essential building block in technologists' toolboxes across a broad array of sectors, including mobile storage, autonomous systems, in-vehicle infotainment, and client and data center solid-state drives (SSDs).

Micron's 176-layer NAND offers improved quality of service (QoS [2]), a critical design criterion for data center SSDs.[3] This can accelerate data-intensive environments and workloads such as data lakes, artificial intelligence (AI) engines and big data analytics. For 5G smartphones, the enhanced QoS can enable faster launching and switching across multiple apps, creating a more seamless and responsive mobile experience and enabling true multitasking and full use of 5G's low-latency network.

Micron's fifth generation of 3D NAND also features an industry-leading maximum data transfer rate at 1,600 megatransfers per second (MT/s) on the Open NAND Flash Interface (ONFI) bus, a 33% improvement.[4] The increased ONFI speed leads to faster system bootup and application performance. In automotive applications, this speed will power near instant-on response times for in-vehicle systems as soon as engines are turned on, enhancing the user experience.

Micron is working with industry developers to quickly integrate the new products into solutions. To simplify firmware development, Micron's 176-layer NAND offers a single-pass programming algorithm, enabling easier integration and speeding time to market.

Micron achieves unparalleled density and cost leadership with novel architecture

With the slowing of Moore's Law, Micron's innovation in 3D NAND is critical to ensuring that the industry can keep pace with growing data requirements. To achieve this milestone, Micron has uniquely combined its stacked replacement-gate architecture, novel charge-trap and CMOS-under-array (CuA)[5] techniques. Micron's team of 3D NAND experts achieved rapid advancements with the company's proprietary CuA technique, which constructs the multilayered stack over the chip's logic — packing more memory into a tighter space and substantially shrinking the 176-layer NAND's die size, yielding more gigabytes per wafer.

In tandem, Micron has improved scalability and performance for future NAND generations by transitioning its NAND cell technology from legacy floating gate to charge-trap. This charge-trap technology is combined with Micron's replacement-gate architecture, which uses highly conductive metal wordlines[6] instead of a silicon layer to achieve unparalleled 3D NAND performance. Micron's adoption of this technology will also enable the company to drive aggressive, industry-leading cost reductions.

Applying these advanced techniques, Micron has increased endurance, which is particularly beneficial in write-intensive use cases — from black boxes in aerospace to video surveillance recording. In mobile storage, 176-layer NAND's replacement-gate architecture results in 15% faster mixed workload performance[7] to power ultra-fast edge computing, enhanced AI inference, and graphic-rich, real-time multiplayer gaming.

Availability
Micron's 176-layer triple-level cell 3D NAND is in volume production in Micron's Singapore fab and now shipping to customers, including through its Crucial consumer SSD product lines. The company will introduce additional new products based on this technology during calendar 2021.

Resources

- Product page: 176-layer NAND
- Blog: Doing What Can't Be Done (Again) — Micron Ships 176-Layer NAND
- Whitepaper: Micron Transitions to Next-Gen 3D NAND Replacement-Gate Technology
- Video: Taking 176-Layer Flash Memory from Lab to Fab
- Video: Just How Remarkable Is Micron's 176-Layer 3D Flash Memory?

About Micron Technology, Inc.

We are an industry leader in innovative memory and storage solutions. Through our global brands — Micron® and Crucial® — our broad portfolio of high-performance memory and storage technologies, including DRAM, NAND, 3D XPoint™ memory and NOR, is transforming how the world uses information to enrich life *for all*. Backed by more than 40 years of technology leadership, our memory and storage solutions enable disruptive trends, including artificial intelligence, 5G, machine learning and autonomous vehicles, in key market segments like mobile, data center, client, consumer, industrial, graphics, automotive, and networking. Our common stock is traded on the Nasdaq under the MU symbol. To learn more about Micron Technology, Inc., visit micron.com.

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[1] Comparison is based on Micron's high-volume, floating-gate 96-layer NAND. When comparing with 128-layer replacement-gate NAND, read latency and write latency for Micron's 176-layer NAND both improve by over 25%.

[2] Quality of service (QoS) refers to the consistency and predictability of SSD response times.

[3] Improved QoS is driven by a reduction in block size and less variance in read latency, as compared to Micron's high-volume, floating-gate 96-layer NAND.

[4] Improvement is over Micron's prior two generations of 3D NAND (96-layer NAND and 128-layer NAND) which featured a maximum of 1,200 MT/s data transfer rates.

[5] CMOS stands for complementary metal oxide semiconductor.

[6] Wordlines are connecting wires to the gate of each NAND memory storage element in a NAND memory array. Wordlines are used to select, program and erase groups of memory cells in an array of NAND memory.

[7] This is compared to Micron's previous generation universal flash storage 3.1-based multichip package using floating-gate 96-layer NAND.

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Exhibit 21

Micron Ships World's First 232-Layer NAND, Extends Technology Leadership

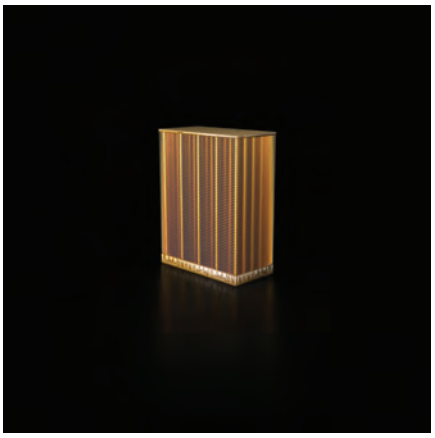
July 26, 2022

Latest innovations deliver TLC NAND with the highest performance and wafer density, all in the industry's smallest package

BOISE, Idaho, July 26, 2022 (GLOBE NEWSWIRE) -- Micron Technology, Inc. (Nasdaq: MU), today announced that it has begun volume production of the world's first 232-layer NAND, built with industry-leading innovations to drive unprecedented performance for storage solutions. It features the industry's highest areal density and delivers higher capacity and improved energy efficiency over previous generations of Micron NAND, to enable best-in-class support of the most data-intensive use cases from client to cloud.

"Micron's 232-layer NAND is a watershed moment for storage innovation as first proof of the capability to scale 3D NAND to more than 200 layers in production," said Scott DeBoer, executive vice president of technology and products at Micron. "This groundbreaking technology required extensive innovation, including advanced process capabilities to create high aspect ratio structures, novel materials advancements and leading-edge design enhancements that build on our market-leading 176-layer NAND technology."

Micron 232-layer NAND



The breakthrough capabilities of Micron's 232-layer NAND will enable customers to deliver more innovative solutions in data centers, thin and light laptops, mobile devices and across the intelligent edge

Leading-Edge Technology Delivers Unrivaled Performance

As the world generates more data, customers must expand their storage capacity and performance while reducing energy consumption and meeting more stringent environmental sustainability requirements. Micron's 232-layer NAND technology provides the high-performance storage necessary to support advanced solutions and real-time services required in data center and automotive applications, as well as responsive, immersive experiences on mobile devices, consumer electronics and PCs. This technology node enables the introduction of the industry's fastest NAND I/O speed – 2.4 gigabytes per second (GB/s) – to meet the low-latency and high-throughput needs of data-centric workloads such as artificial intelligence and machine learning, unstructured databases and real-time analytics, and cloud computing.[1] That speed represents a 50% faster data transfer than the fastest interface enabled on Micron's 176-layer node. [2] Micron 232-layer NAND also delivers up to 100% higher write bandwidth and more than 75% higher read bandwidth per die than the prior generation.[2] These per-die benefits translate to performance and energy efficiency gains in SSDs and embedded NAND solutions.

In addition, 232-layer NAND introduces the world's first six-plane TLC production NAND. [3] It has the most planes per die of any TLC flash[3] and features independent read capability in each plane. The combination of high I/O speed, read and write latency, and Micron's six-plane architecture provides best-in-class data transfers in many configurations. This structure ensures fewer collisions between write and read commands and drives system-level quality-of-service improvements.

Micron's 232-layer NAND is the first in production to enable NV-LPDDR4, a low-voltage interface that delivers per-bit transfer savings of more than 30% compared to prior I/O interfaces. As a result, 232-layer NAND solutions offer ideal support for mobile applications and deployments in the data center and at the intelligent edge that must balance improved performance with low power consumption. The interface is also backward compatible to support legacy controllers and systems.

The compact form factor of 232-layer NAND offers customers flexibility in their designs while enabling the highest TLC density per square millimeter ever produced (at 14.6 Gb/mm^2).[3] The areal density is between 35% and 100% greater than competing TLC products in the market today.[3] Shipping in a new 11.5mm x 13.5mm package, 232-layer NAND features a 28% smaller package size than previous Micron generations,[2] making it the smallest high-density NAND available.[3] More density in a smaller footprint minimizes board space for a diverse set of deployments.

Next-Generation NAND Enables Innovation Across Markets

"Micron has sustained technology leadership with successive first-to-market advancements in NAND layer count that enable benefits like longer battery life and more compact storage for mobile devices, better performance in cloud computing, and faster training of AI models," said Sumit Sadana, chief business officer at Micron. "Our 232-layer NAND is the new foundation and standard for end-to-end storage innovation underpinning digital transformation across industries."

The development of 232-layer NAND is the result of Micron's leadership in research, development and process technology advancements. The breakthrough capabilities of this NAND will enable customers to deliver more innovative solutions in data centers, thinner and lighter laptops, the latest mobile devices and across the intelligent edge.

Availability

Micron's 232-layer NAND is now in volume production in the company's Singapore fab. It is initially shipping to customers in component form and through its Crucial SSD consumer product line. Additional product and availability announcements will follow.

Micron's NAND Center of Excellence in Singapore is recognized by the World Economic Forum's Global Lighthouse Network for operational excellence in smart manufacturing. Advancements including AI tools, smart control systems and predictive capabilities allow Micron to accelerate

product development, improve quality and achieve faster manufacturing yield ramps to shorten the time to market.

Additional Resources

- Micron 232-layer NAND technology

About Micron Technology, Inc.
We are an industry leader in innovative memory and storage solutions transforming how the world uses information to enrich life *for all*. With a relentless focus on our customers, technology leadership, and manufacturing and operational excellence, Micron delivers a rich portfolio of high-performance DRAM, NAND and NOR memory and storage products through our Micron® and Crucial® brands. Every day, the innovations that our people create fuel the data economy, enabling advances in artificial intelligence and 5G applications that unleash opportunities — from the data center to the intelligent edge and across the client and mobile user experience. To learn more about Micron Technology, Inc. (Nasdaq: MU), visit micron.com.

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1 NAND I/O speed is 1.6GB/s at the time of market introduction
2 Based on comparison of Micron product data sheets
3 Based on comparison of NAND currently shipping in market

A photo accompanying this announcement is available at https://www.globenewswire.com/NewsRoom/AttachmentNg/00c4d618-332b-4ff9-b127-d78f67cd92e3

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Exhibit 22

Company awards | Crucial IN

crucial.in/company/awards

Crucial SSD

August 2018 – Wccftech.com

Crucial MX500 500GB SSD – Editor's Choice Award

"For a bit more money you get a better warranty and a very capable drive, it's one of if not the best SATA drives on the market." Read more

August 2018 – Wccftech.com

Crucial MX500 1TB SSD – Editor's Choice Award

"Crucial drives are a great option for strong performance from a brand that is well known and gives a great long-term warranty. 5 years is relatively long." Read more



August 2018 – Wccftech.com

Crucial MX500 1TB SSD – Killer Value Award

"A fantastic product for the money at time of writing blows away similarly priced drives at times and is almost always the fastest in the tests. High end performance for a cheap price." Read more



May 2018 - ModSynergy.com

Crucial MX500 1TB SSD - Editor's Choice Award

"The Crucial MX500 bucks the trend by setting several surprising performance records while offering competitive mainstream pricing." Read more



April 2018 - Anandtech.com

Crucial MX500 1TB SSD - Recommended Award

"The Crucial MX500 1TB SSD with Micron's 3D NAND flash memory is the fastest SATA SSD we've ever tested, reaching performance levels above the outgoing Crucial MX300 750GB SSD in virtually every category. The results are clear. And with a 5-year warranty and extremely competitive pricing, you'd be hard pressed to find a better top-tier SSD on the market today. The Crucial MX500 1TB SSD earns our top Editor's Choice Award rating!" Read more



March 2018 - Tom's Hardware

Crucial MX500 SSD - Tom's Hardware Editor's Choice Award

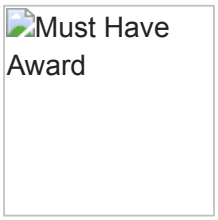
"The MX500 1TB is the best overall value in the SATA SSD market. Crucial priced the drive aggressively … and we can't think of a better value even if we factor in NVMe SSDs. The other capacities also appear impressive … " Read more



March 2018 - TechReport.com

Crucial MX500 1TB and 500GB SSD - TechReport Recommended Award

"The fact that the the MX500 1TB matches the 860 Pro 1TB's performance for a little over half its price highlights how strong of a contender the Crucial [MX500] is...Crucial has succeeded in releasing another 3D TLC drive worthy of the MX name at an easily digestible price, and that's more than enough to notch another TR Recommended award." Read more



February 2018- PureOverclock.com

Crucial MX500 500GB SSD- Must Have Award

"There are some hallmarks of excellence that make something worth buying: performance, quality, and price. I'm not going to wax poetic here, the MX500 has all of these things. It is stable, less expensive, and out performs its price range. An NVMe is going to out perform any SATA, but at an exceptional cost. As any solid state drive is an improvement over an HDD, the MX500 is the best possible performance for the most reasonable price. In fact, when we look at recommendations for buying a new storage solution for a PC, Crucial gives us something new to think about." Read more



February 2018- CDRlabs.com

Crucial MX500 1TB SSD- Editor's Choice Award

"Crucial has knocked another one out of the park with its new MX500 SSD. This next generation drive combines Silicon Motion's SM2258 with Micron's new 64-layer 3D TLC NAND to deliver good performance, enhanced features and a high level of endurance at a competitive price." Read more



January 2018- PCEnthusiast.com

Crucial MX500 500GB & 1TB SSD- Editor's Choice Award

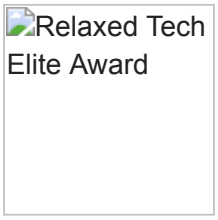
"Aside from the MX500's attractive price and performance, it also comes with a 5-year limited warranty, AES 256-bit hardware-based encryption, integrated power loss immunity, adaptive thermal protection, data defense against data corruption, dynamic write acceleration, and you also get a free Acronis True Image HD software. The data protection, data encryption plus the 5-year warranty is what really attracts me; aside from the price and performance of course. You simply can't go wrong with this SSD." Read more



January 2018- FunkyKit.com

Crucial MX500 1TB SSD- Recommend Award

"The Verdict - Opinion. The Crucial MX500 1TB SSD delivers consistent performance and is a welcome improvement to the MX series. Thanks to Micron 2nd Generation 64-layer 3D triple-level cell (TLC) NAND, we're also seeing larger, more desirable capacity options at a value price point. Not to mention the return of a 5 year warranty!" Read more



January 2018- RelaxedTech.com

Crucial MX500 500GB and 1TB SSD- Elite Relaxed Award

"Crucial has created a fantastic product with the MX500 SSDs. The MX500 series come loaded with features such as hardware encryption, dynamic write acceleration, and can also protect your data in case of a power outage. Price-wise, the MX500 SSDs are hard to beat and offer more performance per dollar compared against the Samsung 850 EVO SSDs. If you are using a traditional hard drive, definitely consider upgrading to an SSD like the MX500 because it will offer a massive upgrade in every aspect from read/write speeds to access times." Read more



January 2018- RealHardwareReviews.com

Crucial MX500 500GB and 1TB SSD- Innovation Award

"This model proves beyond a shadow of a doubt that Crucial is quickly learning how to refine their new 3D TLC NAND technology and fine-tune SMI controllers so as to take full advantage of its unique abilities. The end result is a new model that really doesn't need MLC NAND to be faster than its predecessors. Instead it is faster simply because it is a better design with more powerful components." Read more



January 2018- RealHardwareReviews.com

Crucial MX500 500GB and 1TB SSD- Real Deal Award

"Even though buyers should not expect NVMe performance levels the MX500 does indeed set the new gold standard upon which all SATA based SSD's need to be judged – and not just TLC drives. Put simply for the average consumer this drive acts more like a MLC NAND drive than a TLC based model – and yet costs well below what we would expect this performance to usually cost. In other words, consumers get great value and very good performance for their hard earned dollar. This combination is why we have zero problems with this drive." Read more



December 2017- PCper.com

Crucial MX500 1TB SSD- PC Perspective Gold PC Award

"The MX500 offers excellent performance for the price, and it will likely become one of our more recommended SSDs in the coming months." Read more



December 2017- TheSSDreview.com

Crucial MX500 1TB SSD- Top Value Award

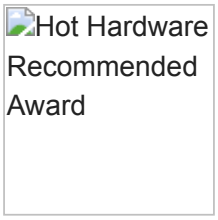
"Crucial's MX series has been known for delivering solid performance at a budget price while checking off all the features boxes one can think of. This time around, it is no exception. There has been a big improvement in performance thanks to its new 64-layer 3D TLC NAND and SMI 2258 controller. Warranty is longer, and endurance is much higher. It has everything you could want and more. There is no reason to hesitate to get your own. Stop reading and go buy one now!" Read more



November 2017- Proclockers.com

Crucial BX300 480GB SSD - Highly Recommended Award

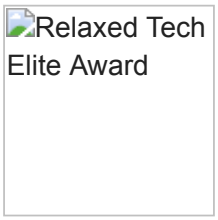
"After spending copious time with the Crucial BX300 480GB drive it's not really a budget drive at its heart but it's aimed at a budget minded market and that's a very good thing. With its Micron 3D MLC NAND flash and Silicon Motion SM2258XT controller, the guts in the Crucial BX300 drive it toward the theoretical upper limits of the SATA6 controllers' capabilities. If you need good solid storage at a fair price with the durability of 3D MLC Micron NAND and Crucial quality then the Crucial BX300 480GB drive should be a no-brainer decision!" Read more



November 2017 – Hothardware.com.com

Crucial BX300 SSD – Hot Hardware Recommended Award

"If you're still stuck chugging along with a hard drive and are considering an upgrade to an affordable SATA SSD, we recommend giving the Crucial BX300 series a look." Read more



October 2017 – RelaxedTech.com

Crucial BX300 240GB and 480GB SSD – Elite Relaxed Award

"Crucial has a winner on their hands with the BX300 SSDs. The 240GB and 480GB models we tested offer excellent performance and compare very well with the 850 EVO and 850 PRO. Price-wise, the BX300 SSDs are hard to beat and offer more performance per dollar compared against the Samsung SSDs. If you are using a traditional hard drive, definitely consider upgrading to an SSD like the BX300 because it will offer a massive upgrade in every aspect from read/write speeds to access times." Read more



August 2017 – RealHardwareReviews.com

Crucial BX300 SSD – Real Hardware Review - Innovation Award

"The all new BX300 series by Crucial is a very interesting series one that in many ways blurs the line between entry level ‘BX’ and mainstream ‘MX’ model designations. So much so you can almost consider it a ‘BX Plus’ model rather than just the successor to the BX200 series." Read more



August 2017 – RealHardwareReviews.com

Crucial BX300 SSD – Real Hardware Reviews - Real Deal Award

"When you mix great NAND with a good controller and then only charge the same prices as the last generation the end result in one incredible value. Crucial really out did themselves here." Read more



September 2016 – Bjorn3d.com

Crucial MX300 750GB Limited Edition – Bjorn3d Seal of Approval

"Using the MX300 as a primary OS drive supplementing, or even as a secondary drive used for storage is going to improve performance immensely when compared to a standard hard drive." Read more



August 2016 – pureoverclock.com

Crucial MX300 750GB Limited Edition – Pureoverclock Editor's Choice Award

"I really like how CRUCIAL has priced this drive and I think it’s an excellent choice for any prospective buyer." Read more



August 2016 – funkykit.com

Crucial MX300 525GB SSD – Funkykit Value Award

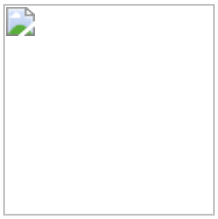
"If you are looking for an HDD or older SSD replacement then Crucial MX300 seems like a perfect option. It's fast, durable, based on high quality components and is also inexpensive." Read more



August 2016 – cdrlabs.com

Crucial MX300 1TB SSD – Best Buy Award

"Like Crucial's previous MX series SSDs, the MX300 is an great choice for anyone looking to improve the performance of their existing desktop or notebook computer." Read more



July 2016 – Big Bruin

Crucial MX300 750GB Limited Edition – Big Bruin Value/Highly Recommended awards

"The Crucial MX300 750GB solid state drive is a very impressive unit in terms of performance and the sweet spot it seems to have found in terms of price and capacity. The read and write speeds may not be the fastest possible, but 530MB/s and 510 MB/s, respectively, are definitely very respectable.The Crucial MX300 750GB solid state drive earns the Bigbruin.com "good Value" and "Highly Recommended" awards." Read more



June 2016 – Tech Report

Crucial MX300 750GB Limited Edition SSD – Tech Report Recommended

"Micron took a bold step by debuting its 3D NAND in a TLC drive poised to replace a well-loved MLC predecessor. Unlike the last time we tested the fruits of such a move, the switch to 3D NAND in the MX300 was well-executed, as we're happy to call the MX300 a worthy successor to the MX200." Read more



June 2016 – PC Perspective

Crucial MX300 750GB Limited Edition SSD – Editor's Choice Award

"For a budget SSD priced below $200, the 750GB Crucial MX300 delivers plenty of performance for the money. It represents a great showing of the first IMFT 3D NAND, coming in at a fraction of the cost/GB when compared with alternate 3D NAND solutions. The new and improved Dynamic Write Acceleration continues to sustain impressive performance even under more rigorous workloads, and the quad-core Marvell controller keeps overall performance at acceptable levels." Read more

Ballistix Memory



July 2018 – PureOverclock

Ballistix Tactical Tracer RGB – Editor’s Choice Award

"The overclocking performance of this kit was beyond anything I expected. I’m used to getting 200-300 MHz tops from a kit. Even though that’s because other kits I’ve used are at a stock voltage of 1.35v, my highest overclock was nearly 1000 MHz above stock! That insane!!!" Read more



June 2018 - PCEnthusiast.com

Ballistix Tactical Tracer RGB DDR4-2666 - Editor's Choice Award

"Build quality was top-notch, as expected from the company, and the aesthetics and design of the Tactical Tracer's heat spreader is great." Read more



May 2018 - HardwareAsylum.com

Ballistix Tactical Tracer RGB 2666 - Recommended Award

"These are a new series of high-performance memory designed for modern DDR4 systems... Not only do the modules look good but are currently available in two speeds starting at 2666Mhz and 3000Mhz with module densities of either 8GB or 16GB and timings of CL16." Read more



April 2018 - RelaxedTech.com

Ballistix Tactical Tracer RGB 2666 - Highly Recommended Score: 9/10

"Out of the box, the Tactical Tracer DDR4 memory has a diffused look but you can easily remove the light bar to get the maximum brightness. Also, I like the idea of giving users the ability to design their own light bar so if you have a 3D printer, go to the Ballistix's website to download the 3D printing files to customize your own light bar. Overall, I believe the Ballistix Tactical Tracer DDR4 2666Mhz 32GB (4x8GB) memory kit deserves our recommended award." Read more



April 2018 - RealHardwareReviews.com

Ballistix Tactical Tracer RGB - Excellence Award

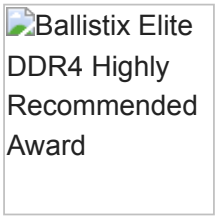
"Congratulations Ballistix for creating what is easily the best designed RGB LED enabled RAM series released to date. Hopefully other companies will take a page from your playbook and also start creating ‘proper’ LED DDR4 RAM series!" Read more



April 2018 - Pro Clockers

Ballistix Tactical Tracer RGB - Editor's Choice Award

"Ballistix has done it again with the Ballistix Tactical Tracer [RGB]. Combining solid performance with unparalleled looks is the key to victory so look for these in the scoreboards. The aesthetics are beautiful and the grey color scheme will blend in well with almost any system. The lighting is on point and the extra RGB zones over most kits on the market really gives more granular control and a smoother lighting scheme. We really love that Ballistix has provided 3D files for making your own top bars as well as making them user-removable without all that warranty-voiding modding business." Read more



March 2018 - Pro Clockers

Ballistix Elite DDR4 - Highly Recommended Award

"Out of the box, XMP settings are solid, giving it well but not class-leading performance. Overclocking it, on the other hand, has notable improvements. Just the small jump from 3466Mhz to 3600Mhz without touching any other settings places it in 1 st place across the board in our testing... Great job Ballistix!" Read more



January 2018-FunkyKit

Ballistix Sport LT DDR4- Editors Choice Award

"Even though Ballistix Sport LT doesn't look like top overclocking memory, it has really high overclocking potential and offers high performance even at default settings. There were no issues at all with compatibility or stability of whole platform in nearly three weeks of various tests. Since it's SODIMM memory then to make the best of it, is required high-end laptop or special motherboard which will support this type of memory." Read more



July 2016 – Benchmark Reviews

Ballistix Elite DDR4-2666

"At the current price I would not hesitate to buy the Crucial Ballistix Elite DDR4-2666MHz kit if I was in the market for some new memory. Crucials Ballistix Elite series has a variety of speeds from 2666MHz to 3200MHz if 2666MHz is just too slow for you." Read more



June 2016 – PC Enthusiast

Ballistix Sport LT DDR4 – PC Enthusiast Editor's Choice Award

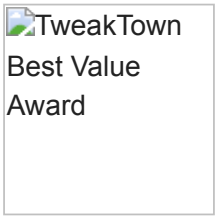
"Finally, the Crucial Ballistix Sport LT DDR4 series is a good solid performing memory kit, very stable and easy to use. It doesn't promise ultra-fast speeds, but its performance is definitely fast and very much acceptable on a day-to-day computing or gaming use. If you are planning to build or has a black and red themed PC (and doesn't want/need any LEDs on the mems sticks) the Ballistix Sport LT DDR4 should be on your short list." Read more



May 2015 – FunkyKit

Ballistix Sport LT DDR4 – Value Award

"Crucial Ballistix Sport LT 16GB DDR4-2400 CL16 memory kit is great option for all who wish to move to the latest Intel X99 platform without spending too much money. Ballistix Sport LT is inexpensive but it's high quality product and also provides high performance. If it's not enough then we can add high overclocking potential and great Crucial support which offers lifetime warranty." Read more



May 2015 – TweakTown

Ballistix Sport DDR4 – Best Value Award

"For most users out there, you are looking for a good mix of value and aesthetics as the main reasons to purchase any kit these days. Crucial seems to have hit the nail on the head when it comes to this…What Crucial has done here is delivered on everything that their specifications and marketing put forward. This is a kit for the masses for two very key reasons. The first we addressed, where the kit will look terrific in any system as it does in the image above of our system. The second part of the kit that is handy is that there were no issues along the way with this kit. Whether booting to 2133MHz by default, or opting for the XMP profile, this kit simply springs to life and boots right to desktop and is ready to take on

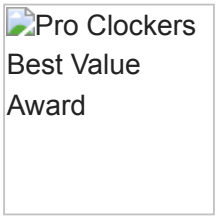
whatever it is you want to dish to it. Of course, having the ability to run a tad faster is a plus, but timings with this kit were definitely the key to extracting every bit of love we could get from the Ballistix Sport DDR4-2400 in testing." Read more



April 2015 – PureOverclock

Ballistix Sport LT DDR4 – Editor's Choice Award

"The Ballistix Sport LT kit should stand out for its overclocking head room, stock performance, unique heat spreader design and a color outside of the same hum drum blue and red. At the end of the day we are very impressed with the Sport LT kit, which is one of the best DDR4 products we have tested in looks and overall bench performance. We gladly give the Crucial Ballistix Sport LT 2400MHz 16GB kit our PureOverclock Editor's Choice Award." Read more



March 2015 – Pro Clockers

Ballistix Sport LT DDR4 – Best Value Award

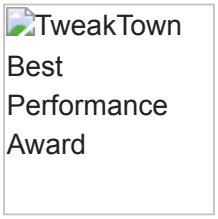
"The performance of the Crucial Ballistix Sport LT is about average at the stock clock and timings. Adding an additional .15v did allow for the timings to be tightened, even with the clocked raised to 2666MHz. This created a nice performance bump that rivaled some of the higher speed kits we have tested. Interestingly, overclocking the Crucial Ballistix Sport LT was almost identical to overclocking the Crucial Ballistix Elite we reviewed a short time ago." Read more



March 2015 – FunkyKit

Ballistix Elite DDR4 – Editor's Choice Award

"Crucial Ballistix Elite 16GB DDR4-2666 has all what perfect enthusiast and overclocking memory kit needs. It performs well, looks great and has high overclocking potential. Additionally Crucial is offering best available support and additional features. Since all that is available in really reasonable price then I can recommend Crucial Ballistix Elite memory without any hesitation and I believe that all who decide to buy this memory will be also satisfied." Read more



March 2015 – TweakTown

Ballistix Elite DDR4 – Best Performance Award

"So, let's consider what is good about this design. The black PCBs make nice looking heat spreaders without taking the design too far, the SPD profile is 2400MHz not 2133, the performance out of the box is definitely better than our baseline kit, and we were able to take these sticks to much higher speeds with lower timings. These are just some of the benefits found in the Ballistix Elite DDR4-2666MHZ 16GB kit. On top of that, you could even take these sticks that clock nicely, and remove the top of them to clear a large CPU air cooler, which is something we think all taller kits should offer… Overall, even with higher initial cost, the overall performance of this kit with XMP used is a nice jump from the 2133MHz kit, which is easy to see across all of our testing. Capacity is fine as well, but the looks and potential of the Ballistix Elite DDR4-2666Mhz 16GB kits are really going to bring the boys to the yard with this kit. A hundred dollars more than our last sample or not - we would much rather spend the cash to have this kit in our daily driver over plain green PCBs any day of the week." Read more

Learn

Our mission is to transform your system's performance — and your experience. The only way to do that is to help you learn.

LEARN

Support

Our experts are here to help. Give us a call, or install like a pro using our videos and guides.

SUPPORT

Exhibit 23

Micron and WekaIO Win Best of Show Award at the Flash Memory Summit 2019

August 29, 2019

Micron's 9000 Series SSDs and the Weka File System Honored for Most Innovative Flash Memory Enterprise Business Application

BOISE, Idaho and CAMPBELL, Calif., Aug. 29, 2019 (GLOBE NEWSWIRE) -- Micron Technology Inc. (Nasdaq: MU) and WekaIO today announced that they have won the 2019 Best of Show Award at this year's Flash Memory Summit for the Micron high-performance 9000 series NVMe SSD product line, along with the Weka File System (WekaFS™). The Micron 9000 series NVMe SSDs and WekaFS high-performance software were selected for the award category of Most Innovative Flash Memory Enterprise Business Application based on SPEC SFS 2014 benchmark test results.

"Flash memory solutions are addressing a wide range of data types including applications driven by video streaming, transactional databases, virtual desktops and other data-intensive environments demanding high scalability and accelerated speed," said Jay Kramer, chairman of the awards program and president of Network Storage Advisors Inc. "We are proud to recognize an array of Micron 9200 NVMe SSDs, combined with the Weka File System, achieving record-breaking performance with the trusted independent industry SPEC SFS 2014 benchmark."

Micron was chosen for its leadership and innovation in the flash memory and solid-state storage industries. The award category analyzes enterprise market segments, vertical market sectors and customer environments that demand high performance and scale such as artificial intelligence, machine learning, in-memory databases and other big data applications.

Micron 9000 series SSDs leverage 3D NAND and NVMe technology to maximize throughput and reduce latency for faster access to data for enterprises and cloud providers. WekaFS is the world's fastest parallel file system based on independent benchmark SPEC SFS 2014 test results. The results are based on tests conducted in February 2019 using WekaIO's software with Micron 9200 NVMe SSDs. In similar testing performed in June, Penguin Computing used the Micron 9000 series SSDs in conjunction with WekaFS to break eight world records on the STAC-M3 Benchmark. The benchmark is used to analyze high-speed analytics common in the financial services industry.

"Our flagship storage 9000 series NVMe SSDs are easy to deploy and help optimize existing infrastructure for our partners and customers," said Roger Peene, vice president of marketing, Storage Business Unit, Micron. "We are pleased that our technology alliance with WekaIO has resulted in setting records for industry-leading performance benchmarks."

"Our parallel file system, combined with the 9000 series NVMe SSDs, has proven to be a winning storage solution for data-intensive application workloads," said Barbara Murphy, vice president of marketing at WekaIO. "The records we've made this year have set the industry benchmark for breakthrough performance of storage solutions, and we have more benchmarks that we are targeting with WekaFS and the Micron 9300 series."

The Flash Memory Summit's annual best of show awards are a premier opportunity for the industry to recognize innovative products and solutions that are being used in the marketplace. A record number of award submissions were received this year, making the judging challenging and each of the categories extremely competitive.

About Micron Technology, Inc.
We are an industry leader in innovative memory and storage solutions. Through our global brands — Micron®, Crucial®, and Ballistix® — our broad portfolio of high-performance memory and storage technologies, including DRAM, NAND, NOR Flash and 3D XPoint™ memory, is transforming how the world uses information to enrich life. Backed by 40 years of technology leadership, our memory and storage solutions enable disruptive trends, including artificial intelligence, machine learning and autonomous vehicles, in key market segments like data center, networking, automotive, industrial, mobile, graphics and client. Our common stock is traded on the Nasdaq under the MU symbol. To learn more about Micron Technology Inc., visit micron.com.

About WekaIO
WekaIO helps companies manage, scale, and futureproof their data centers so they can solve big problems. WekaIO has built the world's fastest shared and parallel file system on new architecture optimized for NVMe flash that leapfrogs legacy storage infrastructures by delivering the best performance density at any scale, at a fraction of the cost. With the most flexible deployment models, the storage software is a modern file system designed for modern I/O-intensive and extreme technical computing workloads.

Follow WekaIO: Twitter, LinkedIn and Facebook

About Flash Memory Summit
The Flash Memory Summit, produced by Conference ConCepts, showcases the mainstream applications, key technologies and leading vendors that are driving the multibillion-dollar nonvolatile memory and SSD markets. Now in its 13th year, FMS is the world's largest event featuring the trends, innovations and influencers that are driving the adoption of flash memory in demanding enterprise storage applications, as well as in smartphones, tablets, and mobile and embedded systems. @FlashMem, #FlashMemorySummit2019 #FlashMemorySummitBestofShowAwardWinner.

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Exhibit 24

Tom’s Hardware Innovation Awards 2023: Game Changers

tomshardware.com/news/tomshardware-innovation-awards-2023

Matt Safford, Sarah Jacobsson Purewal, Brandon Hill, Paul Alcorn, Jarred Walton, Avram Piltch, Les Pounder, Andrew E. Freedman

April 26, 2023



(Image credit: Tom's Hardware)

It's our job and our joy here at Tom's Hardware to test the latest products and tech, while sharing our benchmark results and experiences with our readers. From graphics cards and CPUs to gaming laptops, Raspberry Pi expansion boards, and fast 3D printers, lots of enthusiast hardware passes through our labs throughout the year. And while many of those products deliver great performance and are worth your money, comparatively few actually break new ground.

To recognize the real game-changing devices and the companies that design and build them, we present the second-annual Tom’s Hardware Innovation Awards. The 25 products below all disrupt the market in some way and set a standard that others may follow.

In order to be eligible for consideration, products must have been either announced or shipped within the last year. While we tested many of the devices below – and linked to our reviews where available – some have not shipped yet and are included here based on their potential. Whether any untested products are worth your money is a question we’ll have to answer in future reviews, but what we can say for all of the products and tech below is that they break out of the box in ways that are likely to shape the tech industry’s future.

AMD Ryzen 7000X3D Series of CPUs (7800X3D, 7900X3D, 7950X3D)



(Image credit: Tom's Hardware)

Groundbreaking cache, record-breaking speeds

AMD's turbocharged Ryzen 7000X3D series leverages an innovative 3D-stacked slab of L3 cache to deliver unbeatable gaming performance. AMD's sole first-gen 3D V-Cache chip gave it a commanding win over Intel in our list of the best CPUs for gaming, but the tech resulted in significantly lower performance in some productivity workloads due to lower clock speeds, thus confining the chip to systems solely focused on gaming.

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AMD circumvented that challenge with the second-gen models by expanding the range of Zen 4 X3D chips to three processors: the eight-core Ryzen 7 7800X3D, the 12-core Ryzen 9 7900X3D, and the 16-core Ryzen 9 7950X3D. These three chips all beat every Intel

contender in gaming, but the higher core-count models bring the 3D V-Cache tech to those that want leading-edge gaming performance yet still need strong performance in productivity work.

These models use a single cache chiplet fused atop one of the two compute dies, thus preserving the higher boost clocks of the standard chiplet and adding extra cores to keep performance strong in heavy productivity work. This approach requires some software hand-holding to ensure workloads land in the right place, but AMD's new chipset drivers handle this transparently while also providing customization options.

The dual-chiplet models command a stiff premium, but the eight-core 7800X3D beats Intel's fastest gaming processor, the Core 19-13900K, at a much more affordable price point. This chip might not have quite the horsepower in productivity applications as its more core-heavy brethren, but it is the fastest gaming chip on the planet, bar none.

AMD's second-gen 3D V-Cache architecture takes the key advantage of chiplet-based design methodologies — using an older and less-expensive process node in tandem with expensive new process tech — into the third dimension: The second-gen 3D V-Cache technology leverages the less-expensive 7nm process node as a 3D-stacked cache die to boost the performance of its cutting-edge 5nm compute die, which AMD then places in a package with a 6nm I/O die. That's an innovative trifecta of process node technologies that, paired with cutting-edge packaging tech and transparent software, is simply impossible to beat — at least for now. Intel doesn't have a competing tech, so we expect AMD's Ryzen 7000X3D chips to remain at the top of our rankings for the remainder of the year.

Read: AMD Ryzen 7 7800X3D Review

– Paul Alcorn

Nvidia GeForce RTX 4090 Graphics Card



(Image credit: Tom's Hardware)

Incredibly powerful and packed with forward-looking tech

Nvidia's debut of the Ada Lovelace architecture threw down the gauntlet for what we can expect from a top-tier GPU. Yes, it's the fastest graphics card for gaming purposes, leading the next closest offering by 35% at 4K — that's the second-tier RTX 4080, if you're wondering. The RTX 4090 pummels AMD's closest rival, the RX 7900 XTX, by over 50%, and it's also over 60% faster than the previous generation halo part, the RTX 3090 Ti.

That doesn't even factor in DLSS upscaling, or the new DLSS 3 Frame Generation. It does include ray tracing benchmarks, another area Nvidia has upgraded substantially compared to the previous Ampere GPUs, with new technology like Shader Execution Reordering, Opacity Micro-Maps, and Displacement Micro-Meshes. The *Cyberpunk 2077* RT Overdrive mode with full path tracing makes use of SER and OMM, and with DLSS 3 enabled the RTX 4090 can still cruise along at a comfortable 103 fps, or 65 fps without Frame Generation. The 7900 XTX with FSR2 upscaling managed just 16 fps.

But it's not just about gaming. For AI workloads like Stable Diffusion, the RTX 4090 can spit out 49 images per minute, compared to less than 13 images per minute with the RX 7900 XTX. That's at 512x512; running the newer 768x768 target with Stable Diffusion 2.1, initial results were 20 images per minute, compared to just three on AMD's card. That's because there doesn't appear to be a fully tuned model for AMD just yet, which is part of the story. Nvidia's GPUs are the de facto standard for most publicly available AI projects, and getting them running on non-Nvidia hardware can be an exercise in frustration. If you're interested in toying around with AI, an Nvidia GPU will be both faster and easier to get running.

The RTX 4090 doesn't come cheap, but considering the features and performance on tap, it remains the best choice for an extreme GPU. It's a no compromise, fast at everything solution. It can also use a lot of power, 450W or more in some workloads — enough that the 16-pin adapters can melt if not plugged in properly. Even so, overall efficiency still shows a large improvement over the competition.

This is the graphics card to beat for the foreseeable future. AMD doesn't have a competing solution, and probably won't even try with this generation of GPUs. The only thing likely to top the RTX 4090 is the rumored Titan Ada Generation and/or RTX 4090 Ti — GPUs that will push even higher power use for likely minimal gains.

Read: Nvidia GeForce RTX 4090 Review

– Jarred Walton

Crucial T700 SSD



(Image credit: Tom's Hardware)

Super-speed storage, without the noise

There’s a new wave of PCIe 5.0 SSDs coming to market, all powered by Phison’s novel E26 SSD controller, but the Crucial T700 sets a high bar with the most advanced flash that delivers the fastest performance of the PCIe 5.0 crowd. In contrast to many competing PCIe 5.0 SSDs, it accomplishes this feat with a passive cooler that doesn’t have a built-in noisy fan like we see with many other models.

The PCIe 5.0 era actually began almost two years ago with the arrival of Intel's previous-gen CPUs, but SSDs that support the blazing-fast interface have been elusive due to numerous delays of the blazing-fast NAND flash memory needed to saturate the wider bus. New SSDs are now available at retail, so we can finally, truly say that the era of PCIe 5.0 SSDs has begun, promising to double throughput over prior-gen SSDs while significantly improving performance in random workloads.

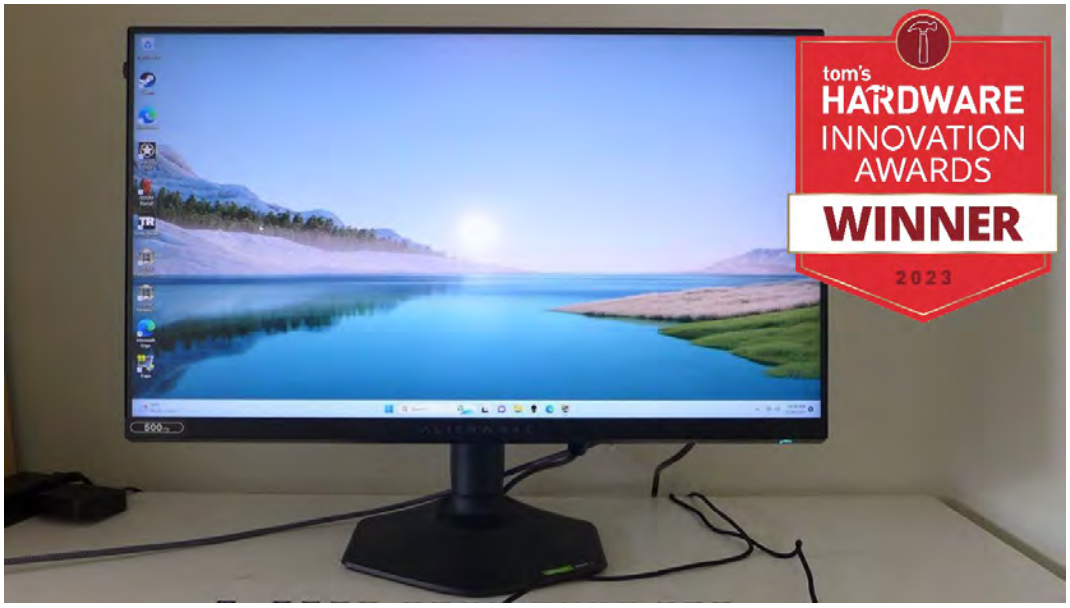
The Crucial T700 exemplifies the best of PCIe 5.0 SSDs. The drive delivers an incredible 12.4 / 11.8 GB/s of sequential read/write throughput and 1.5 million random read/write IOPS (who could've even imagined that ten years ago?). This leading performance comes courtesy of Phison's E26 SSD controller paired with Micron's best 232-Layer TLC flash that communicates at 2000 MT/s. Meanwhile, the competition is stuck with slower flash for now.

The Crucial T700 also supports DirectStorage, a boon for next-gen gaming that can deliver one-second loading times, along with the latest in encryption tech. The SSD can absorb 600 TB of write data per 1TB of capacity, so the 2TB model is rated for 1,200 TB of endurance over its five-year warranty period — that's more than enough for most users. The Crucial T700 has a strong warranty from a company that makes its own flash and delivers leading-edge performance, but pricing and availability information isn't available yet. However, we've already put the SSD through its paces in our Crucial T700 SSD Preview and came away impressed. .

Read: Crucial T700 SSD Preview: Fastest Consumer SSD Hits 12.4 GB/s

– Paul Alcorn

Alienware 500Hz Gaming Monitor (AW2524H)



(Image credit: Tom's Hardware)

500 Hz finally arrives for desktop monitors.

The Alienware AW2524H is the world's first 500Hz gaming monitor, far outpacing the growing number of 360Hz displays on the market. Dell's latest entry minimizes frame tears and motion blur, allowing today's flagship graphics cards like the Nvidia GeFore RTX 4090 push 400+ frames per second in eSports games.

The AW2524H also boasts a 2ms advantage in control lag over its 360Hz competition. If you're a competitive gamer, the AW2524H is an excellent tool for your arsenal. Throw in Alienware's usual excellent build quality and color performance, the AW2524H is among the best gaming monitors available on the market.

However, be warned that this excellent performance across-the-board comes at a relatively high price. As of this writing, the Alienware AW2524H costs $830, which puts it about $400 more expensive than its 360 Hz peers. But you have to pay to play at 500 Hz, and the AW2524H is worth every penny for the most discerning gamers out there.

Read: Alienware AW2524H 500 Hz Gaming Monitor Review

– Brandon Hill

Corsair Xenon Flex Bendable Gaming Monitor

Image 1 of 2



(Image credit: Tom's Hardware)

(Image credit: Tom's Hardware)

Flat or curved? You decide.

OLED panels are becoming more popular in the gaming monitor space, with many options appearing at affordable price points. However, Corsair's new 45-inch Xeneon Flex is priced in the premium sphere and with good reason – it has a bendable panel that allows you to

choose between a flat panel or an 800R (maximum) curve. You manually bend the screen using two handles that extend from the sides.

In addition to its trick, bending OLED panel, the Xeneon Flex also exhibits good contrast and high color accuracy. You also get a fast 240 Hz refresh rate and low input lag. Of course, Adaptive-Sync is standard, with support for AMD FreeSync Premium and Nvidia G-Sync. And the wide-screen format with a 3440 x 1440 resolution should be appealing to gamers and productivity workers alike.

No product is perfect, and the Xeneon Flex has a couple of dings due to its relatively low pixel density due to the 45-inch panel and slight misses with HDR color. But the biggest hurdle is the $1,999 price tag, which is likely well out of range for most mainstream gamers.

Read: Corsair Xeneon Flex 45WQHD240 Bendable OLED Review

– Brandon Hill

Acer SpatialLabs View Glasses-Free 3D Monitor



(Image credit: Tom's Hardware)

4K and glasses-free 3D

It can often be hard to stand out in the portable monitor crowd, but Acer knocked it out of the park with the SpatialLabs View. This 15.6-inch monitor offers up a 4K resolution along with accurate color and contrast from its IPS panel. However, its main party trick is the ability to deliver glasses-free 3D with supports apps and games.

The View makes full use of its 3840 x 2160 resolution to deliver stereoscopic 3D imagery at 1920 x 2160 per eye. The two images are quickly flashed, slightly offset from one another, which does a great job into fooling your eyes (and brain) into seeing a 3D image.

Not only is this 3D technique possible in supported games like God of War and Kena: Bridge of Spirits, but you can use the SpatialLabs Go to convert existing 2D video into 3D with the click of a button. However, remember that the final 3D output is only as good as your 2D source material – in other words, garbage in, garbage out. However, the high-quality videos that we tested were effectively translated into 3D output. Another plus is that the SpatialLabs Model Viewer allows you to import CAD files to view in 3D to help visualize models.

While the View's claim to fame is its 3D functionality, it can also function as a traditional, portable 4K monitor. While its 60 Hz refresh rate limits it from being used as a gaming-centric monitor, its 282 ppi pixel density, accurate color, and built-in battery make it a worthy tool for road warriors.

Read: Acer SpatialLabs View 15.6-inch Glasses-Free 3D Portable Monitor Review

– Brandon Hill

MSI RadiX BE22000 Turbo Wi-Fi Gaming Router



(Image credit: Tom's Hardware)

Wi-Fi 7 and rotating antennae

While's eight-antennae arrays are commonplace in today's high-end gaming routers to offer the best reception and performance for connected devices, MSI is going a different route with the RadiX BE22000 Turbo. This new Wi-Fi gaming router instead uses four motorized antennae that sprout from its base.

According to MSI, these antennae dynamically detect the location of clients connecting to the router and "change the antenna pattern for [the] best performance." Given that the RadiX BE22000 Turbo is still in the development phase and Wi-Fi 7 routers won't hit the market until late 2023 at the earliest, MSI didn't elaborate on what criteria it uses to point the antennae at clients. We also don't know how much of a performance increase we'll see with this arrangement over a gaming router with eight fixed antennae.

With that said, it just looks cool in action, which we're assuming will be part of the appeal of such a router. However, the RadiX BE22000 Turbo has more to offer than its motorized antenna pageantry. The router features automatic artificial intelligence-based QoS, 320MHz channel bandwidth to deliver a 4x speed uplift versus Wi-Fi 6 and enables multi-link operation to boost performance for a single client. As for wired connectivity, the RadiX BE22000 Turbo is equipped with two 10 GbE ports and four 2.5 GbE ports.

Pricing and availability haven't been announced at this time, but we expect to hear more from MSI in H2 2023.

Read: Wi-Fi 7 is Coming: Here's What You Need to Know

– Brandon Hill

Lenovo Yoga Book 9i



(Image credit: Tom's Hardware)

Two separate displays buck the foldable trend.

We've seen a few foldable laptops — both Lenovo and Asus have released them — but with the Yoga Book 9i, Lenovo is bucking the trend. Instead, this device will have two 13.3-inch screens when it releases in June. When closed, the Yoga Book will look like any other petite clamshell.

In a way, it emulates having multiple screens. A foldable screen may be *bigger*, but multiple screens 2880 x 1800 displays may keep you more organized. At least, several *Tom's Hardware* staffers with arguably too many screens seem to believe that.

Lenovo will stack the Yoga Book 9i with the latest specs, including a 13th Gen Intel Core i7 U-series chip, up to 16GB of LPDDR5X RAM and up to 1TB of PCIe SSD Gen 4 storage.

There are some questions we have, like whether or not the origami-style hand to hold up the Yoga Book will be cumbersome. But we're still thinking about its potential a few months after its announcement, and we're looking forward to trying it soon.

Read: Lenovo Yoga Book 9i Has Two 13-inch OLED Screens

– *Andrew E. Freedman*

Apple MacBook Air (M2)



(Image credit: Tom's Hardware)

Cool, collected, and almost perfected

Apple probably could've gone years without redesigning the MacBook Air. Its fanless design with M1 was a hit, but the new M2 redesign feels like it was made for the chip. What's arguably one of the highest regarded laptops has fully left Intel behind.

But beyond the new chip, the MacBook Air's new design brought in a slew of features, including bringing MagSafe back to the Air, a much-needed 1080p webcam and a keyboard with full sized function keys.

Pair all that with a top-class touchpad, a long-lasting battery, new colors and even new charger options, and it's an update to an icon that feels like a major upgrade. The one downside? It's far more expensive than the M1 version, which Apple kept on the market. .

Read: Apple MacBook Air (M2) Review

– Andrew E. Freedman

Framework Laptop 16



(Image credit: Framework)

If this works, it's a big deal for repairability.

When Framework introduced easily changeable port modules, that was cool. When it made easily replaceable mainboards that it has supported for three generations, that was sweet. When it announced a larger laptop that can also support upgradeable graphics and different keyboard configurations? Well, that made our jaws drop.

It's early days here. Framework hasn't announced pricing or specs for the Framework Laptop 16, nor how much the input modules or expansion pay upgrades are going to cost. But if Framework pulls this off, it will be a feat that shows up many major gaming companies, which have promised upgradeability but repeatedly faltered, especially in graphics. The expansion bay will also let the Framework Laptop 16 change sizes depending on whether it needs to accommodate bigger graphics cards. As a proof of concept, Framework also used the PCIe x8 interface to make a dual M.2 SSD card to add 16TB of storage.

The input modules will allow for people to choose whether they want a second screen, a number pad, or whatever other modules Framework and its partners choose to sell. Me? I wouldn't mind something with tasteful RGB.

Read: Framework Previews 16-inch Laptop With Upgradeable Graphics, Adds Ryzen Mainboards

– Andrew E. Freedman

Sony DualSense Edge



(Image credit: Tom's Hardware)

PS5 controller goes pro, but also modular.

Sony didn't invent the idea of a pro controller — Microsoft has been making them for years. But Sony's DualSense Edge is perhaps the most repairable of them. At least, when it comes to the joysticks.

The DualSense Edge's joysticks can be easily popped out of the controller if they start to experience drift. On the one hand, you could argue that it's a tacit admission that yes, the joysticks can fail, it also empowers Edge owners to make their own simple repairs (for $19.99 per module) without any tools. That's one way to keep on gaming without buying new controllers over and over again.

That's not all. The DualSense Edge is more comfortable to hold than the regular model, has a long, braided USB cable, and is better for accessibility with easy button remapping. The battery life isn't amazing, and $200 is a lot for a controller, but it mixes luxury with some neat tricks that PlayStation diehards will appreciate.

Read: Sony DualSense Edge Review

– Andrew E. Freedman

MSI Titan GT77 HX



(Image credit: Tom's Hardware)

Bleeding-edge mobile gaming

MSI's 17-inch Titan GT77 HX may lack the taller 18-inch displays of much of its 2023 competition, but its Mini-LED screen blew me away with its deep blacks and bright, vivid colors (looking arguably better than the OLED TV that I use as a monitor every day. And our testing backed up the enjoyment of my eyeballs, with the GT77 HX's screen delivering over 500 nits of brightness and 114.5% of the DCI-P3 color space. This may be the best laptop screen we've ever tested – at the very least it's the best among the handful of Mini-LED-equipped competitors we've tested this year.

And the Titan GT77 HX isn't *all* about the screen. It gets a lot of other important things right, like top-end performance (with our RTX 4090 review configuration) and a Cherry mechanical keyboard that's about as satisfying as keys get on a laptop. Combine cutting-edge gaming and productivity performance, one of the best keyboards, and one of (if not the) best screens, and MSI's GT77 HX stands tall among the gaming laptops of 2023, even if this Titan is technically a bit smaller than its big-screen competition.

Read: MSI Titan GT77 HX Review

– *Matt Safford*

Fractal Design North



(Image credit: Tom's Hardware)

Wood accents and mid-century design for your PC

After years of tempered glass and RGB everything, Fractal Design's North case wowed the PC builder world last year with its stunning mid-century design, complete with wood slats up front and brass or steel accents on the buttons and feet. Unless you absolutely hate the retro-aesthetic, the North just might be the prettiest PC case ever made. And at about $140, it's surprisingly affordable.

And unlike many design-forward cases, the North doesn't sacrifice performance for its stunning design. Behind the slim wood slats (oak on the white model and walnut for the black variant) the front panel is covered in fine mesh for excellent airflow. And the side panel is available in either tempered glass or perforated metal (for even more ventilation). And up to six 120 mm fans are supported. The mesh side panel model also ships with a fan hub and a bracket to mount two more fans (or a radiator against the side panel.

The North is a breath of fresh air in terms of design and performance. And clearly the competition is taking notice, because Corsair started selling wood panel kits for some of its existing cases early this year. And we'd be shocked if we didn't see some other wood-accent PC cases arrive before the end of the year.

Read: Fractal Design North Review

– Matt Safford

Team Group Siren DUO360 All-in-One ARGB



(Image credit: Team Group)

AIO cooling extends to your SSD.

The Best AIO coolers may be able to keep your CPU cool and quiet while looking good with some tasteful RGB, but Team Group's AIO DUO360 ARGB aims to do all that *and* keep your bleeding-edge SSD chilled as well. Now, it's debatable how much even a PCIe 5.0 SSD needs active cooling unless you're doing some kind of task that's hammering the drive for several minutes or hours at a time (and that's definitely not what a gaming load is like).

But many speedy SSDs come with heatsinks, and some come with active cooling. The Siren DUO360 gives you extra drive cooling that also matches the CPU cooler in the same loop.

Read: Team Group Launches Dual CPU and SSD Liquid Cooler

– *Matt Safford*

Buffalo SSD-PUT (2TB)



(Image credit: Tom's Hardware)

Yes, 2TB flash drives are real – and surprisingly affordable.

For years, the only pocket-friendly flash drives available in capacities up to two terabytes were either several hundred dollars, or scammy / fake no-name drives available via AliExpress or Amazon. But the 2TB Buffalo SSD-PUT is real and, at $115 when we wrote this, a surprisingly decent deal if you need lots of storage on the go. It's cheaper than most larger 2TB external SSDs, and significantly smaller. Just don't expect the same kind of performance you'd get from a pro-level SSD – although the SSD-PUT is pretty fast for a flash drive.

In our testing, the Buffalo drive wasn't the fastest flash drive we've tested, but its performance was very good overall. On our 10GB DiskBench transfer test, for instance, its read and write speeds were both above 440 MB/S, which was the third-fastest result among the dozens of recent drives we've tested.

Not everything is great about the Buffalo drive though. Its plastic shell is a bit bulky as flash drives go, and feels a little cheap. But it's hard to knock a drive that's this spacious, speedy and affordable while still being small enough to easily slide into your pocket.

Read: Best Flash Drives: Fast, Roomy USB Storage in Your Pocket

– *Matt Safford*

Corsair RMx Shift

Image 1 of 2

(Image credit: Tom's Hardware)

(Image credit: Tom's Hardware)

A shift to side-mounted cable connections

Much of the news this year in the power supply realm has revolved around ATX 3.0 and those pesky 16-pin 12VHPWR power connectors. But Corsair turned heads with its RMx Shift line, which turns the modular power cable connections from the rear to the side of the PSU, making for much easier access in some (but not all) PC cases.

Clearly, if your case is extremely narrow and / or has a shroud or panel that blocks access to the rear side of your PSU, then the RMX Shift isn't going to work well for your build. But for most cases moving the connectors to the side of the PSU will make it much easier to add or remove cables after the initial build, and may ease installation and cable routing during the initial setup process.

Corsair even includes both vertically and horizontally mounted connectors, so cables that are more likely to be routed vertically (like the main power connector and CPU/GPU connectors are easier to bend and route up the case, and other power cables can be routed horizontally. While this is a minor tweak, it can help cable routing to not have all your power cables exiting the PSU area in the same direction.

Again, side-mounted cables aren't going to work or be helpful with every case. But for those chassis with an open back and a fair bit of clearance behind the motherboard area, Corsair's RMx Shift might be the most useful design change in PSU design since the SFX form factor made smaller systems possible.

Read: Corsair RMx Shift PSUs Adopt Side-Mounted Modular Connectors

– Matt Safford

Prusa MK4



(Image credit: Tom's Hardware)

Awesome prints on any surface

Prusa's MK printers have long been among the most innovative and powerful in the industry, a perennial favorite of makers who can afford their premium prices. Available for $1,099, the new Prusa MK4 features amazing auto bed leveling that automatically sets the z height guarantees a perfect first layer, even if you attempt to print on top of a sheet of cardboard.

The MK4 has a new 32-bit board that allows it to use its custom firmware to print at high speeds. It features a direct drive and an all-metal hot end, yet remains extremely quiet during printing. An optional MMU (multi-material unit) makes it easy to print in different colors at the same time.

Read: Prusa MK4 Review

— *Avram Piltch*

Bambu Labs P1P



(Image credit: Tom's Hardware)

Blazing fast and easy to customize

Arguably, the biggest problem with 3D printing is how long it takes to complete your output. Bambu Lab's P1P has a turbo button that allows it to print at "ludicrous" speed, which is as fast as 300mm per second, about six times a normal 3D printer's speed. A model of a dragon that took 50 minutes to print on a Koba Neo, completed in just 18 minutes on the Bambu P1P. And, even at that speed, the quality is excellent.

Available for the relatively reasonable price of $699, the P1P offers a generous build volume of 256 x 256 x 256mm, a PEI build plate, auto leveling and direct drive that lets you print capably in flexible TPU filament. The auto leveling is so automated that you never need to even select a z offset, an annoying process that involves sticking a piece of paper under the nozzle on most printers. You can also print your own side panels, which we did in bright red and black PETG, showing our logo.

Bambu also sells its own, optional AMS (Automatic Material System) for $349. This add-on allows you to have one print that uses four different colors of filament at once, solving another huge problem of 3D printing, the fact that most prints are monochrome.

Read: Bambu Lab P1P Review

— *Avram Piltch*

Elegoo Neptune 3 Max



(Image credit: Tom's Hardware)

Max size and quality at a min price

Elegoo's line of Neptune FDM 3D printers continues to raise the bar when it comes to quality and features for the price, an innovation of value. For less than $500, the Neptune 3 Max offers a huge 420 x 420 x 500 mm build volume, enough to print huge cosplay items such as a sword or even a helmet.

But the Neptune 3 Max is more than just a giant printer. Its direct drive mechanism allows it to handle more exotic filaments such as TPM, a flexible material which can create rubbery models. Its automatic bed leveling and PEI build plate make getting a great first layer a breeze.

In our tests, the Neptune 3 Max delivered a gorgeous bust of Spider-Man in black PLA filament and a highly-detailed dragon in purple PETG, both using the maximum 500mm height. A translucent green trash can printed in TPU looked fantastic as did a Skyrim dagger printed in Silver PLA+.

Read: Elegoo Neptune 3 Max Review

—Avram Piltch

Asus ROG Azoth Gaming Keyboard



(Image credit: Tom's Hardware)

Keyboard enthusiasm goes mainstream.

The Asus ROG Azoth is one of the best gaming keyboards for several reasons — refined, well-built chassis, hot-swappable switches, excellent all-around typing and gaming experience. But the Azoth's gasket mount design and customizable OLED screen aren't unique — the reason this keyboard gets an innovation award is because of what it comes with.

The Azoth comes with an entire box of accessories, which include a 6.5-foot (2m) USB-C cable, a USB extender, a keycap puller, a switch puller, and a DIY lube kit. The lube kit includes lubricant (Krytox GPL205-GD0), a switch opener, a lube station, a brush, and a handful of extra switches. Asus also includes a QR code that links to a video tutorial on how to use the lube kit. The kit isn't made up of particularly pricey or hard-to-get items, but it's awesome to see all this packaged with a mainstream gaming keyboard — and a great one, at that.

Read: Asus ROG Azoth Review

—*Sarah Jacobsson Purewal*

Insta360 Link

Image 1 of 2

(Image credit: Tom's Hardware)

(Image credit: Tom's Hardware)

An action webcam with shockingly good auto-white balance

Action-cam maker Insta360's first webcam, the Insta360 Link, is pretty specc'd out — this 4K/30fps webcam comes with a built-in 3-axis gimbal and a variety of capture modes that make it perfect for streaming everything from business presentations to TikTok dance tutorials. But while the Link's AI-powered tracking and capture modes are impressive, what really stands out about the Link is its exceptionally accurate auto-white balance and auto-exposure.

Adjusting exposure, white balance, and brightness/contrast on the fly are tasks almost all webcams struggle with — and that's when you're in a balanced, evenly-lit setting (which most people are not). The Insta360 Link's ability to adjust exposure in well-lit, dark, and over-exposed settings — while also keeping the picture's white balance vibrant-yet-realistic, definitely stands out against the competition.

The Insta360 Link is packed with features, but it doesn't require much tweaking — it's an excellent plug-and-play device. (But if you want to tweak, the companion Link Controller app is practically professional when it comes to detailed control and thoroughness).

Read: Insta360 Link Review

– *Sarah Jacobsson Purewal*

Elgato Facecam Pro

Image 1 of 2

(Image credit: Tom's Hardware)

(Image credit: Tom's Hardware)

4K/60fps

There are a lot of 4K webcams on the market now, but almost all of them capture 4K video at 30 frames per second (fps). While this might seem fine considering most video conferencing apps limit streaming to 1080p/30fps at most, what about all those content creators who need to be able to capture video in ultra-high-res, ultra-smooth 4K/60fps?

Elgato's Facecam Pro features a premium autofocus lens, a wide 90-degree field of view, and can stream in 4K/60fps (as well as 4K/30fps, 1080p/60fps, 1080p/30fps, 720p/60fps, and 720p/30fps). It also comes bundled with Elgato's Camera Hub software, which offers impressively detailed control over the picture as well as streaming-focused features for setting up different "scenes." All it needs is an action-cam gimbal to go with that ultra-smooth 60fps video.

Read: Elgato Facecam Pro Review

– Sarah Jacobsson Purewal

Razer DeathAdder V3 Pro



(Image credit: Tom's Hardware)

This mouse feels better than my hand

Razer's flagship DeathAdder line of gaming mice has had the same general design — large, right-handed, flared at the front — since the original DeathAdder dropped in 2006. And it's a popular design: the DeathAdder is Razer's best-selling gaming mouse. So, naturally, Razer decided the best way to celebrate the DeathAdder's long-standing legacy would be to... give it a complete redesign.

The Razer DeathAdder V3 Pro features a fully redesigned body with reduced side flare, a more streamlined silhouette, and a split key cover instead of a unibody shell. It also sports some more subtle tweaks — the hump has been shifted slightly to the left, the thumb buttons

are slightly higher for better accessibility, etc. — all of which combine into what Razer calls “next-generation ergonomics,” and what I call witchcraft. Why does this stripped-down, lightweight gaming mouse feel *so damn good?*

The DeathAdder V3 Pro sports Razer’s latest Focus Pro 30K optical sensor, gets up to 90 hours of battery life, and comes with custom, pre-cut grip tape. It doesn’t have Bluetooth, RGB lighting, or more than five programmable buttons. It’s lightweight, but it’s not *that* lightweight — many ultra-lightweight FPS-oriented gaming mice weigh less than this mouse’s 2.26oz / 64g. And at $150, it’s pricey, considering all you don’t get. But I actually had to move it off of my desk because I couldn’t stop my hand from gravitating toward it in ridiculous situations (like when I was playing a game that required at least 15 additional mouse buttons). And that kind of speaks for itself.

Read: Razer DeathAdder V3 Pro Review

– *Sarah Jacobsson Purewal*

Pinecil V2



(Image credit: Tom's Hardware)

Low cost soldering iron, with high end features

$26 for a soldering iron is crazy cheap, but Pine64’s Pinecil v2 is much more than just a hot piece of metal. Inside this RISC-V powered soldering iron lies a temperature controlled soldering station, while still being just a little larger than a pen. It heats up fast, 20 seconds and you are ready to solder.

It can hit 450 degrees Celsius and a range of interchangeable tips means that we can tackle soldering jobs both big and small. Pinceil v2 can be powered by standard DC power or via USB C, which means with a USB powerbank we have a portable temperature controlled soldering station ready to fix our projects in the field.

We love its small size, easy-to-use interface and upgradable firmware. All of that makes this a great iron, but for $26, it is a steal. If you've never soldered before, get a Pinecil v2. If you are an experienced maker, Pinecil v2 is a great second soldering iron, either for your portable maker kit or for those quick jobs when a dedicated soldering station is not feasible.

Read: Pinecil V2 Review

– Les Pounder

Pimoroni Tufty RP2040



(Image credit: Tom's Hardware)

RP2040 Powered Full-Color Badge, Display or Games Console

Bringing a 2.4 inch IPS display to a badge is a bold move. Battery life for a backlit LCD screen is much lower than ePaper, but trading battery life for a full-color screen is worth it. Powered by the RP2040, Tufty 2040 is bold in features and design, just take a look at the silkscreen on the rear.

The screen is the big selling point, but this isn't a one-trick pony. Around the back is a battery connection, compatible with externally charged LiPo / Li-ion packs and a QW/ST connector. The QW/ST connector is compatible with Qwiic and Stemma QT components such as

sensors. Using these components with Tufty 2040's screen is made easy thanks to a great MicroPython module. In no time, we can have a custom sensor platform ready to serve data.

What if your ambitions lie in game creation? In that case you can also make your own games to play on Tufty 2040. Using Pimoroni's PicoGraphics module, Pixylatte recreated the Atari classic River Raid. There is nothing to stop you creating your own games, demos or name badge using Tufty 2040.

Read: Pimoroni Tufty 2040 Review

– Les Pounder

Tom's Hardware Innovation Awards 2023: Live Broadcast



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Matt Safford

After a rough start with the Mattel Aquarius as a child, Matt built his first PC in the late 1990s and ventured into mild PC modding in the early 2000s. He's spent the last 15 years covering emerging technology for Smithsonian, Popular Science, and Consumer Reports, while testing components and PCs for Computer Shopper, PCMag and Digital Trends.

With contributions from

- Sarah Jacobsson PurewalSenior Editor, Peripherals
- Brandon Hill
- Paul AlcornDeputy Managing Editor
- Jarred Walton
- Avram Piltch
- Les Pounder
- Andrew E. Freedman

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Exhibit 25

SEMICONDUCTORS

CEO of Chinese chipmaker Yangtze Memory steps down

Company is key asset in Beijing's push for self-reliance in semiconductors



Simon Yang, then CEO of Yangtze Memory Technologies, speaks at the China Flash Market Summit in Shenzhen in 2018. (Photo by Cheng Ting-Fang)

CHENG TING-FANG, Nikkei Asia chief tech correspondent
October 3, 2022 15:07 JST

TAIPEI -- The CEO of China's top memory chipmaker has stepped down, fueling uncertainty over a strategically important company that has sparked concerns among U.S. lawmakers over a potential deal with Apple.

Simon Yang was no longer chief executive of Yangtze Memory Technologies Co. (YMTC) as of the end of September, though he remains at the company, three people said.

They did not provide a reason for Yang stepping down, and said it was not clear what immediate impact the change might have on the company's strategic direction.

YMTC is China's most successful memory chip company and a key asset in the push to build a **self-reliant chip industry**. Yang served as CEO since it was incorporated in 2016, and industry executives and suppliers see him as one of the most important figures in fulfilling Beijing's chip ambitions.

Local Chinese media first reported the management change. YMTC declined to comment for this story.

Yang's change of role comes amid heightened American scrutiny of YMTC. U.S. senators have called for a review of the company, citing its "often opaque ties to the Chinese Communist Party." The lawmakers are also concerned that the adoption of the company's chips by American companies such as Apple "would introduce significant privacy and security vulnerabilities to the global digital supply chain."

Apple has been in close contact with YMTC since 2018 and is in the process of verifying the company's chip products for use in its devices, Nikkei Asia reported earlier.

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China, meanwhile, has launched a sweeping campaign against corruption in its chip industry. Multiple officials and senior executives are under investigation, including Din Wenwu, president of the China Integrated Circuit Industry Investment Fund. Nicknamed the Big Fund, the entity is the most important funding vehicle for China's chip industry. Many former executives of chip giant Tsinghua Unigroup, the former parent company of YMTC, have also been put under investigation.

YMTC still counts the Big Fund as a key stakeholder, with a holding of about 49%. The government of Hubei province, where the company is based, and its linked funds are now the biggest owner, with a stake of about 51%, after increasing its holding following a financial crisis at Tsinghua Unigroup.

Under Yang's leadership, YMTC has become the world's sixth-biggest maker of NAND flash memory by output, with about 5% of the global market last year, according to data from Counterpoint Research.

Its original plant in its headquarters of Wuhan is running at near full capacity, with a second plant set to **go into production** as soon as the end of this year, Nikkei Asia earlier reported. It mass-produces 128-layer NAND flash memory, which is about one or two generations behind global leaders like Samsung and SK Hynix.

An industry veteran, Yang has numerous links to international chip circles. He served as senior executive of the Singapore-based Chartered Semiconductor Manufacturing, now a part of GlobalFoundries, and was once chief operating officer of China's biggest contract chipmaker, Semiconductor Manufacturing International Corp. Yang also studied in the U.S. and worked for Intel for more than a decade earlier in his career.

As CEO, he worked to bring YMTC to the global stage. In 2018, he showed off the **company's technology** at the Flash Memory Summit in California. He stressed on multiple occasions that his company did not intend to be a "copycat" and its entrance **would not crash** the memory chip market.

YMTC Chairman Chen NanXiang will take over as CEO for now, people briefed on the matter said. Chen became chairman this year after Zhao Weiguo resigned from the post. Zhao was also the head of Tsinghua Unigroup but is now **under investigation** for alleged corruption.

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Exhibit 26

SEMICONDUCTORS

U.S. sanctions derail China chipmakers' expansion plans

Yangtze Memory and ChangXin forced to delay new factories and lay off staff



Yangtze Memory Technologies Corp. (YMTC) has faced delays over constructing a second plant in Hubei province, China. (Photo by Shunsuke Tabeta)

SHUNSUKE TABETA, Nikkei staff writer
February 15, 2023 02:03 JST

WUHAN/HEFEI, China -- Sweeping export bans imposed by the U.S. last fall have held up plans by major Chinese chipmakers to expand operations, dealing a setback to the government's ambitions to make the country a semiconductor powerhouse.

Uncertainty was the prevailing mood during a visit to the massive flagship production site of Yangtze Memory Technologies, about 40 kilometers east of central Wuhan. Both YMTC engineers and technicians at the site to deliver manufacturing equipment had no idea when its **second plant**, originally slated to start up in late 2022, would actually come online.

"Things like electrical equipment have been set up, but installation of chipmaking equipment hasn't started yet," one said.

YMTC was founded in 2016 by Tsinghua Unigroup in partnership with the National Integrated Circuit Industry Investment Fund, commonly known as the "Big Fund." It began mass-producing NAND flash memory chips in 2019.

After Unigroup went bankrupt, YMTC came under the management of the Big Fund and local authorities. It focused on honing its ability to compete in the global NAND market, reaching the point that Apple had reportedly been set to **use YMTC chips** in iPhones.

The company broke ground in 2020 on a second factory -- estimated to cost around 100 billion yuan ($15 billion at current rates) -- to triple production capacity.

But its ascent has stalled since Washington announced broad, stringent curbs on exports of technology and gear for making advanced semiconductors, as well as restrictions on U.S. nationals providing support to Chinese chipmakers.

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That September, not long before the sanctions were announced, Simon Yang -- who reportedly holds a U.S. passport -- **stepped down** as CEO of YMTC. The following month saw the departures of American engineers from U.S.-based chipmaking equipment companies who had supported YMTC's expansion plans.

The delays have forced YMTC to cut jobs.

"Our department started layoffs in January of around 10% of its staff," said an engineer who has worked at the company for about three years. "They've also frozen the hiring of graduate students."

The atmosphere at the company is grim, with its future looking uncertain, the engineer said.



ChangXin Memory Technologies (CXMT) is also encountering delays in building its research and development center in Anhui province, China. (Photo by Shunsuke Tabeta)

ChangXin Memory Technologies, which makes DRAM chips using advanced technology covered by the sanctions, has also had a wrench thrown into its plans.

CXMT finished a new office building for a planned second plant located near the company's headquarters in the city of Hefei. But the construction of the production facility itself is facing lengthy delays.

"We planned to begin operations in 2023, but it won't happen until 2024 or 2025 at the soonest," said a CXMT engineer.

The construction of CXMT's new research and development center appears to have made hardly any progress as well.

"The hiring of graduate students has been suspended temporarily," said the engineer, who added the company is cutting 5% to 7% of staff, depending on the department.

Neither YMTC nor CXMT responded to questions or requests for comment.

The government under President Xi Jinping announced the "Made in China 2025" initiative in 2015, which positioned semiconductors as a critical industry. The Big Fund was established as part of the initiative and has strongly supported the development of the chip industry. First-phase investments reached roughly 140 billion yuan.

Thanks to that fund, China's semiconductor industry attained rapid growth, with the three government-backed memory companies YMTC, CXMT and Fujian Jinhua Integrated Circuit Co. leading the way.

But as tensions flared between the U.S. and China, Washington tightened restrictions on exports to the Chinese chip sector, the technology of which lagged behind that of the U.S. industry.

Huawei Technologies, the telecommunications equipment manufacturing heavyweight, fell under the sanction crosshairs in 2019. China's largest chip foundry Semiconductor Manufacturing International Corp. soon found itself targeted as well.

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China's rate of self-sufficiency in semiconductors grew to 24% in 2021 from 10% in 2015, according to International Business Strategies. The U.S. research company put out a report in June last year that predicted the ratio will exceed 50% in 2030. But when the U.S. later toughened trade sanctions, IBS CEO Handel Jones warned the self-sufficiency share might stall at 30% by that date.

The semiconductor market has been lackluster as of late, with Chinese companies -- the main clients of YMTC and other chip suppliers -- easing up on orders. Considering those dynamics, the delayed expansion in production will not likely amount to a critical blow to the Chinese government's ambition of building a self-sustaining supply chain.

At the same time, the U.S. pressure campaign against the Chinese semiconductor industry is visibly taking its toll, putting the country on a steeper path on realizing its chip dreams.

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Exhibit 27

YMTC is a Leading Pioneer in 3D NAND

techinsights.com/blog/ymtc-leading-pioneer-3d-nand

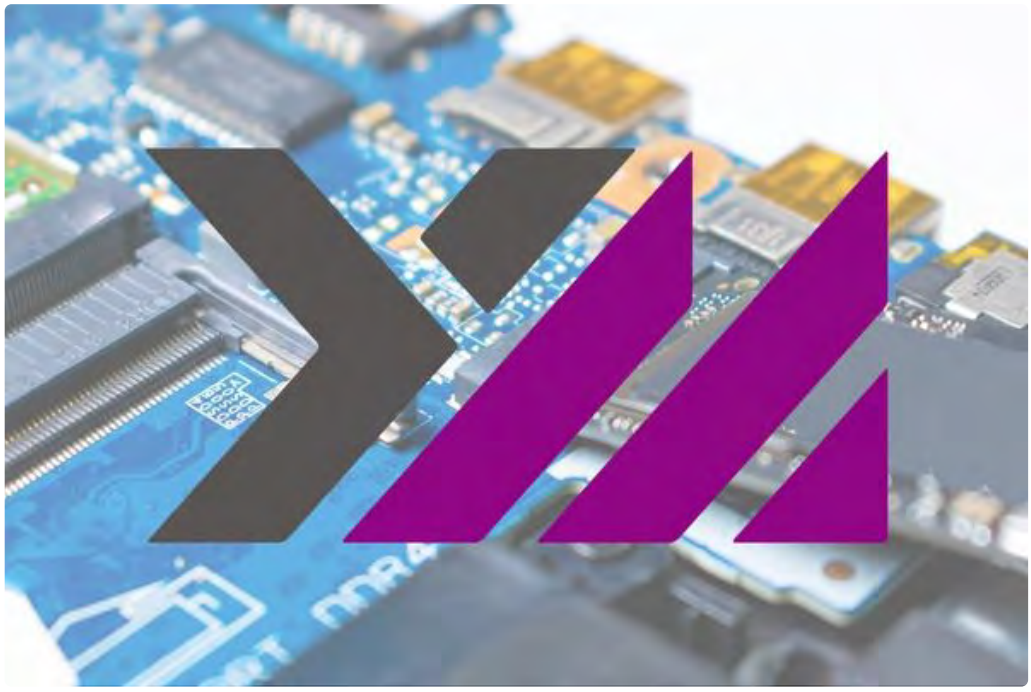
Memory Blog

YMTC 232L Xtacking3.0

Now, YMTC is a Leading Pioneer in 3D NAND

Jeongdong Choe

March 02, 2023



A note from the editor:

Dr. Jeongdong Choe penned the following article in December 2022. Technology moves quickly – here we are in March 2023, and it has just been announced that YMTC has received a huge cash infusion of $7 billion USD. We have also just received the Micron 232L NAND SSD, and will be reporting our findings shortly.

Jeongdong Choe
Senior Technical Fellow, TechInsights
Dec. 2022

Chinese NAND champion Yangtze Memory Technologies Corp's (YMTC's) recent remarkable growth and technological prowess took many of us by surprise. I am quite curious as to where and how they got their superpowers. In 2016, when YMTC announced that it would enter the 3D NAND business, six front runners including NAND veterans Samsung, SK Hynix, Micron, Toshiba, Western Digital (WD), and Intel, were already running the race; it seemed that if YMTC did jump into the 3D NAND world, it could only hope to rank 7th. In addition to market position, YMTC faced other challenges such as process, device, design, and circuit technologies in the early stages of starting a new NAND business, and a lack of experience in mass production as well.

At that time, it was predicted that even if YMTC could occupy part of the domestic market in China, 3D NAND would not be their future, and it would instead make products applicable only to low-level applications such as some of the domestic secure USB devices in China.

However, I would say this prediction was completely wrong. Since 2016, YMTC has successfully developed higher-density 3D NAND SSD products by combining their own process and design technologies based on Xtacking Hybrid bonding technology. Here, 'X' in Xtacking is from the first letter of the company, XMC. Now, by skipping the release of a 176-layer solution, YMTC has jumped directly into developing and mass-producing the 232-layer Xtacking3.0, which is the first 200+ layer solution we've found on the market. It's the most advanced product with the highest bit density and the highest number of layers ever in the 3D NAND field.

Given that Micron just started to ship 232L NAND SSD for PCs and laptops, Samsung has successfully developed 232L custom samples, and SK Hynix's 238L development is ongoing now, YMTC's new 232L Xtacking3.0 TLC technology is a disruptive one and it may lead the future of 3D NAND technology.

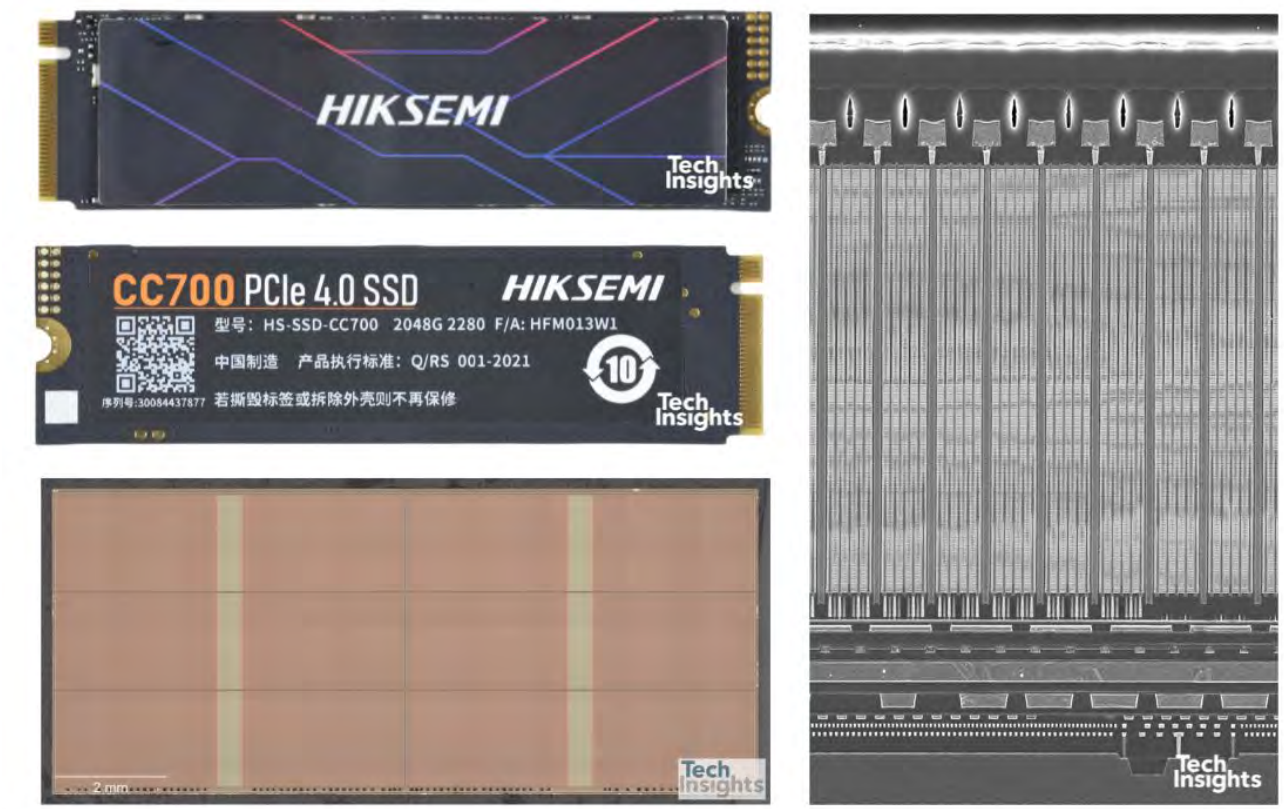


Figure 1. HIKSEMI CC700 PCIe 4.0 2TB SSD, YMTC Xtacking3.0 232L 1Tb TLC die, and 3D NAND array/Periphery X-section SEM images, TechInsights 2022

Compared to the 112-layer mass production and 162-layer prototype development stage of KIOXIA (previously Toshiba Memory), the founder of NAND that was developing and mass-producing on par with Samsung in the early days of 3D NAND, YMTC is already more than one generation ahead where they had previously been trailing 12 months behind their closest competitors. Moreover, YMTC made and commercialized products with more than 200 layers in just seven years, from and including 2016. Since the first 3D NAND prototypes from Samsung (TCAT V-NAND) and Toshiba (BiCS structure) introduced in 2007, the development and mass production of 2xx layer 3D NAND has taken more than 15 years. That being said, YMTC 232L Xtacking3.0 commercial SSD products are quite meaningful and represent remarkable technological growth. Where do the driving force and momentum of YMTC come from?

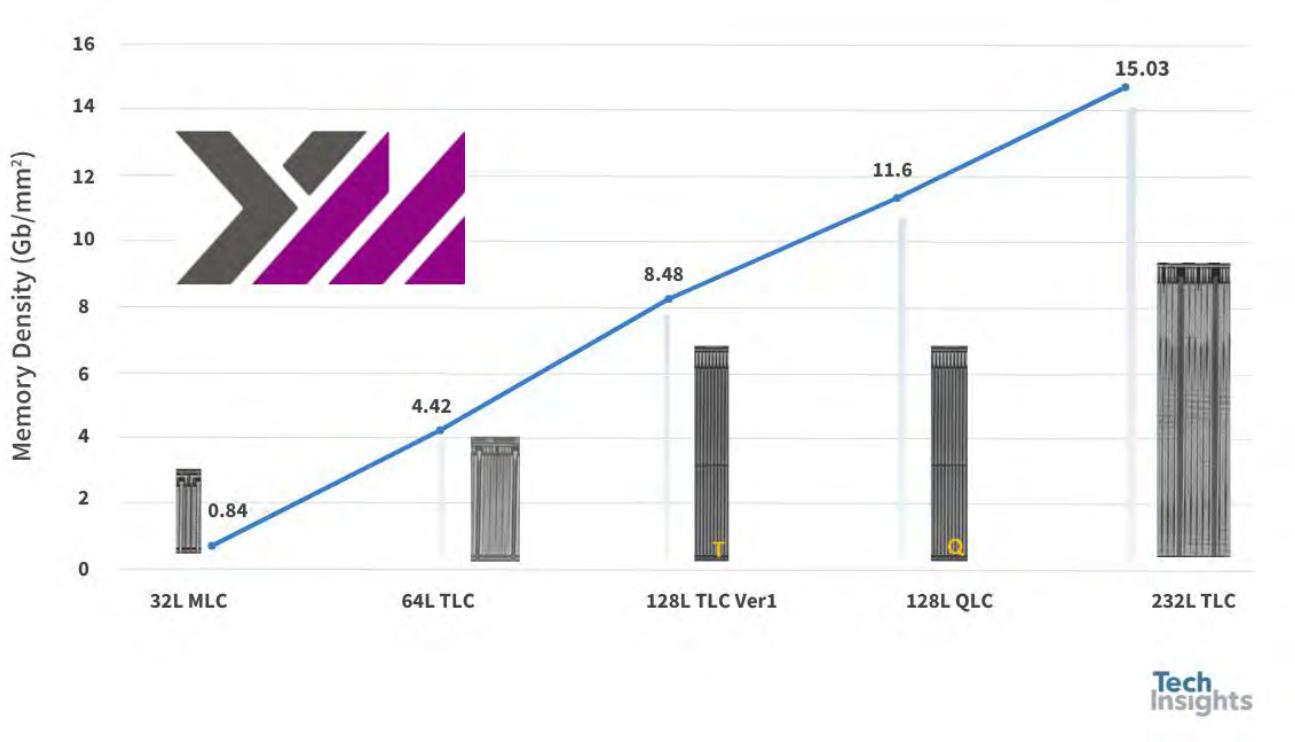


Figure 2. YMTC 3D NAND bit density trend, Gen1 through Gen4, TechInsights 2022

Let's take a quick look at YMTC's recently shipped 232L Xtacking3.0 SSD product here. The product with YMTC 232L chip is the HIKSEMI CC700 PCIe 4.0 2TB SSD, and the Xtacking3.0 chip consists of eight 1Tb dies stacked in a device package (Figure 1). The bit density increased by 76% from the previous 128L TLC second version Xtacking2.0 512Gb die (Figure 1), and the total number of vertical gates counted 253 (Figure 2).

Now, the bit density of NAND has exceeded 15.0 Gb/mm^2 even with TLC products instead of QLC ones. For reference, the Micron 176L QLC N48R die has 14.9 Gb/mm^2 density and 14.6 Gb/mm^2 for the 232L TLC chip. Considering that the total number of vertical gates is 253, the vertical cell efficiency exceeded 91.6%. These figures show quite a difference in technology compared to the current 176-layer mass-products from leading companies Samsung, Micron, and SK Hynix. It should be noted that Micron was the first to announce 232L 3D NAND products last August, and Samsung recently started to ship 236L sample products, but TechInsights has not yet been able to find these products in the open market. The YMTC 232L Xtacking3.0 SSD products we purchased and analyzed show that YMTC's 3D NAND technology and productivity have risen considerably.

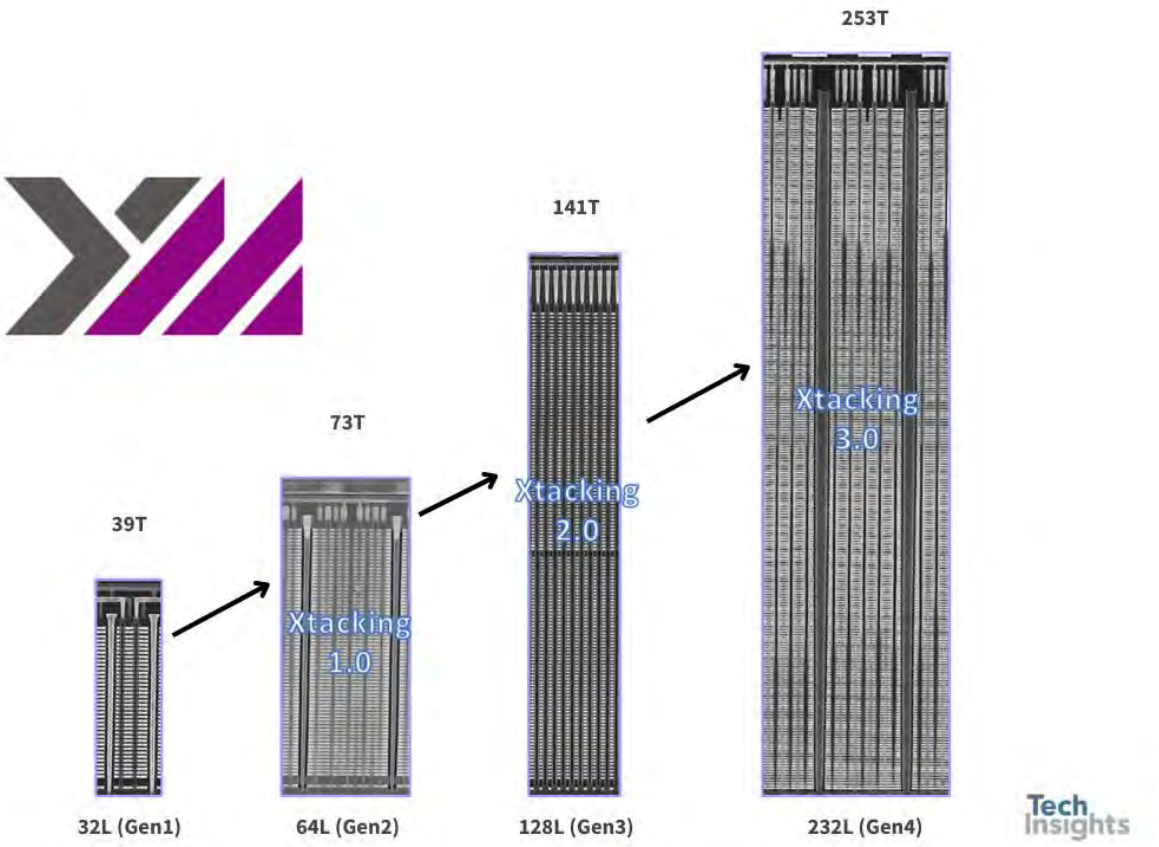


Figure 3. YMTC 3D NAND cell structure, Gen1 32L through Gen4 232L (x-sectioned SEM images in BL direction), TechInsights 2022

A comparison of YMTC's 3D NAND technology by generation can be seen in Table 1. The first baby product of YMTC's 3D NAND had a 32-layer structure and was not much different in structure and process from Samsung TCAT V-NAND which was mass-produced by Samsung at the time. However, YMTC did not focus long on the mass-production of 32-layer products, and instead skipped right over 48-layer products and jumped to developing 64-layer products. They introduced an Xtacking technology in which H-bonding with two wafers, a NAND wafer and a peripheral logic circuitry wafer, were used. NAND and logic wafers are separately processed and attached, followed by TAC and BEOL. The Xtacking technology was the world-first applied to memory devices, and YMTC successfully entered the high-density and high-performance 3D NAND market. Since then, they skipped 96-layer products and succeeded in mass-producing 128-layer Xtacking2.0 in which some of the innovations such as new material for the gates (NiSi) and a 2-deck process were applied to secure their reputation for technological prowess.

Items	YMTC 3D NAND Gen1 (32L MLC)	YMTC 3D NAND Gen2 (64L TLC)	YMTC 3D NAND Gen3 (128L TLC, 1B-Die)	YMTC 3D NAND Gen4 (232L TLC)

Items	YMTC 3D NAND Gen1 (32L MLC)	YMTC 3D NAND Gen2 (64L TLC)	YMTC 3D NAND Gen3 (128L TLC, 1B-Die)	YMTC 3D NAND Gen4 (232L TLC)
Parent Product (Example)	32 GB Secure USB	Gloway YCT512GS3-S7 Pro 512GB SSD	Asgard PC!e4.0 NVMe1.4 AN4 1TB SSD	HIKSEMI CC700 PCIe 4.0 2TB SSD
Package Markings	YMEC6A1MA3A2C1	YMN08TB1BHU1B	YMN09TC1B1HC6C	YMC6G008Tb78DA1C0
Memory/Device	256 Gb	1 Tb	2 Tb	8 Tb
Die Markings	98081A	BCT1B	CDT1B	EET1A
Architecture	T-CAT	Xtacking1.0	Xtacking2.0	Xtacking3.0
# Dice, Memory/Die	4, 64 Gb	4, 256 Gb	4, 512 Gb	8, 1 Tb
Die Size	76.30 mm^2	57.96 mm^2	60.42 mm^2	68.15 mm^2
Memory Density	0.84 Gb/mm^2	4.42 Gb/mm^2	8.48 Gb/mm^2	15.03 Gb/mm^2
# Planes	1	2	4	6 (Center-XDEC)
# Decks, # Gates	1, 39T	1, 73T	1, 141T (69 + 72)	2, 253T (128 + 125)
Vertical Cell Efficiency	82.1%	87.7%	90.8%	91.7%
# Metals	3	8	11	11 (BSSC)
Channel Hole Height	2.74 µm	4.14 µm	8.49 µm	12.0 µm
WL Pitch (Z-direction, min.)	70 nm	58 nm	58 nm	48 nm
BL Pitch	39 nm	39 nm	39 nm	39 nm
Unit Cell Area	0.018 $µm^2$	0.021 $µm^2$	0.021 $µm^2$	0.021 $µm^2$

Table 1. A comparison of YMTC 3D NAND devices; Gen1 (32L) through Gen4 (232L), TechInsights 2022

Driven by that momentum, now, ahead of other companies, YMTC has commercialized SSD products using 232L Xtacking3.0 technology. It would not be an exaggeration to say that YMTC is now one of the leading companies in 3D NAND technology. Looking at the NAND cell array of YMTC's Xtacking3.0 chip, the new BSSC (Backside Source Connect) technology is applied to simplify the source connection process, and the cost and throughput are significantly improved by removing the interlayer between decks (Figure 4). Further, the new Xtacking3.0 1Tb die uses a center-XDEC which improves NAND operation speed compared to the previous edge-XDEC.

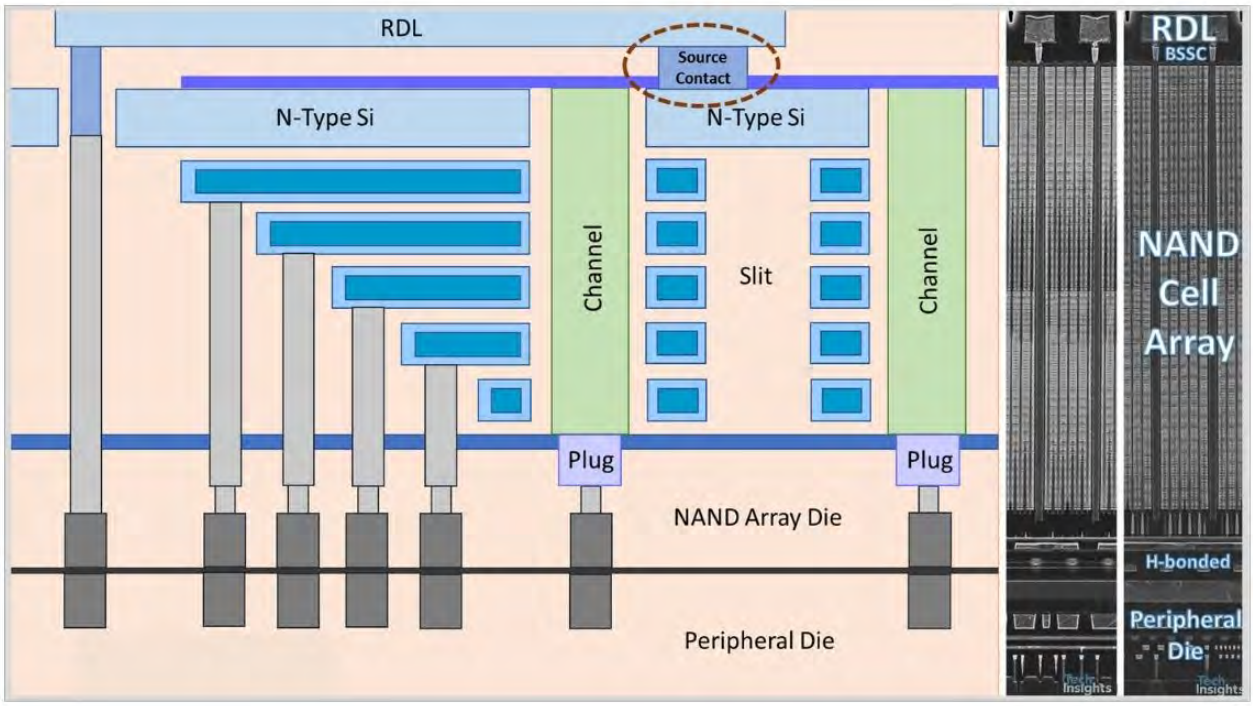


Figure 4. YMTC's newly adopted BSSC (Backside Source Connect) structure for Xtacking3.0, TechInsights 2022

YMTC's fairytale 3D NAND story has a few background factors to consider. The Chinese government's strong investment into and encouragement of YMTC took much of the cost risk out of R&D, highly skilled hard-working engineers in YMTC and experienced and skilled engineers contributed from external organizations, the timely investment into and securing of Fabs, and management of YMTC's supply chain (HIKSEMI) are major drivers behind YMTC to get them to this point, and for YMTC to continue their tales of success. In addition, Western sanctions levied against several Chinese technology companies in recent years have further fueled China's interests in becoming technologically independent. Unlike the Logic Foundry and DRAM business which have no choice but to use EUVL equipment from ASML and semiconductor equipment from US companies such as AMAT and LAM for future advanced generations such as FinFET, GAA, MBCFET, and nanowire, 3D NAND processes do not use EUVL equipment. It is expected that Chinese independent technological prowess and preemption of the next-generation 3D NAND products will continue for the time being.

YMTC's main cause for concern is that the commercial market for their 3D NAND products is mostly limited to mainland China. Most of YMTC's Xtacking products have been used for secure, SSD, and USB applications which are used only in China. Recently, YMTC 3D NAND chips have started to be used for some Chinese smartphone products. For example, TechInsights confirmed YMTC 3D NAND chips were used in Huawei Mate Xs 2 foldable phones.

Only 15 years ago, the question was whether or not 3D NAND could be commercialized. 5 years ago, people questioned whether 3D NAND products could exceed 200 layers due to technical limitations such as wafer warpage, cell current, and HAR. However, today we have seen SSD products with over 200 layers in the open market. Now, our question has changed to whether NAND products and technologies will exceed 1,000 layers. The technological challenges for the next 3D NAND generations will be overcome and resolved in the future, and it is expected that this will lead to the advancement of higher memory density, higher speed, and higher bandwidth memory technology along with hybrid-bonding, package solution, and CXL interface technology. From where I sit, it looks like YMTC will continue to be among the leaders as 3D NAND continues to evolve.

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Exhibit 28



SSD Database ▸ Lexar NM800 Specs

Lexar NM800 512 GB

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512 GB	IG5236	TLC	PCIe 4.0 x4	M.2 2280
CAPACITY	CONTROLLER	FLASH	INTERFACE	FORM FACTOR

Multiple hardware versions found.
Performance could vary due to unannounced flash/controller changes.









The Lexar NM800 is a solid-state drive in the M.2 2280 form factor, launched on September 15th, 2021. It is available in capacities ranging from 512 GB to 1 TB. This page reports specifications for the 512 GB variant. With the rest of the system, the Lexar NM800 interfaces using a PCI-Express 4.0 x4 connection. The SSD controller is the IG5236 (Rainier) from InnoGrit. Lexar has installed 64-layer TLC NAND flash on the NM800, the flash chips are made by YTMC. Please note that this SSD is sold in multiple variants with different NAND flash or controller, which could affect performance, the "Notes" section at the end of this page has more info. To improve write speeds, a pseudo-SLC cache is used, so bursts of incoming writes are absorbed more quickly. Thanks to support for the fast PCI-Express 4.0 interface, performance is excellent. The NM800 is rated for sequential read speeds of up to 7,000 MB/s and 3,000 MB/s write; random IO reaches 200K IOPS for read and 550K for writes.
At its launch, the SSD was priced at 88 USD. The warranty length is set to five years, which is an excellent warranty period. Lexar guarantees an endurance rating of 1500 TBW, a high value.

Solid-State-Drive	
Capacity:	512 GB
Variants:	512 GB · 1 TB
Overprovisioning:	35.2 GB / 7.4 %
Production:	Active

Physical	
Form Factor:	M.2 2280 (Single-Sided)
Interface:	PCIe 4.0 x4
Protocol:	NVMe 1.4
Power Draw:	Unknown

Controller	
Manufacturer:	InnoGrit
Name:	IG5236 (Rainier)
Architecture:	ARM 32-bit Cortex-R5
Core Count:	Quad-Core

Released:	Sep 15th, 2021
Price at Launch:	88 USD
Part Number:	LNM800X512G-RNNNG
Market:	Consumer

DRAM Cache

Type:	Unknown
Capacity:	512 MB (1x 512 MB)

Features

TRIM:	Yes
SMART:	Yes
Power Loss Protection:	No
Encryption:	No
RGB Lighting:	No
PS5 Compatible:	Yes

NAND Flash

Manufacturer:	YTMC
Name:	Xtacking 1.0
Rebranded:	(Rebranded by Lexar)
Type:	TLC
Technology:	64-layer
Speed:	800 MT/s
Capacity:	2 chips @ Unknown
ONFI:	4.0
Topology:	Charge Trap
Process:	40 nm
Die Size:	58 mm² (4.4 Gbit/mm²)
Planes per Die:	2
Decks per Die:	1
Word Lines:	73 per NAND String 87.7% Vertical Efficiency
Read Time (tR):	74 µs
Program Time (tProg):	760 µs
Block Erase Time (tBERS):	9.0 ms
Die Read Speed:	432 MB/s
Die Write Speed:	42 MB/s
Endurance: (up to)	1500 P/E Cycles
Page Size:	16 KB
Block Size:	1152 Pages
Plane Size:	1006 Blocks

Frequency:	667 MHz
Foundry:	TSMC FinFET
Process:	12 nm
Flash Channels:	8 @ 1,200 MT/s
Chip Enables:	4
Controller Features:	DRAM

Performance

Sequential Read:	7,000 MB/s
Sequential Write:	3,000 MB/s
Random Read:	200,000 IOPS
Random Write:	550,000 IOPS
Endurance:	1500 TBW
Warranty:	5 Years
MTBF:	1.5 Million Hours
Drive Writes Per Day (DWPD):	1.6
SLC Write Cache:	Yes

Notes

Drive:
Could also be YMTC's 2nd Generation Xtacking 2.0 (128-Layers)

NAND Die:
Array Eficiency of over 90%
The 64-Word Layers NAND Die from YMTC actuall has 73-Gate Layers, being 64 for storage, 5 DWL (Dummy Word Layers) alongside 4 select Gates (1 SG and 3 Drain SGs)

PS: Bit-line pitch is 40nm
NAND Die Endurance: From 1500 to 3000 P.E.C.
NAND Flash Bus: Up to 800 MT/s
Page Read in SLC Mode: 34µs

```
Page Write in SLC Mode: 34µs
Block Erase in SLC Mode: 3.3ms
```

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USD

Lexar Professional 512GB NM800 M.2 2280 PCIe Gen4x4 NVMe Internal SSD, Solid State Drive, Up To 7000MB/s Read, for Gamers and Creative Professionals (LNM800X512G-RNNNG)

$196.99

- Make sure this fits by entering your model number.
- Superior speed PCIe Gen4x4 interface: 7000MB/s read and 3000MB/s write – NVMe 1.4, with M.2 2280 form factor
- Get 12.7x the speed of a SATA-based SSD

- Designed for hardcore gamers and creative professionals
- Shock and vibration resistant with no moving parts
- Designed with heat dissipation label that keeps your computer cool

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Description **Additional information**

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Designed for hardcore gamers and creative professionals, the Lexar Professional NM800 M.2 2280 NVMe SSD provides maximum SSD performance with speeds up to 7000MB/sread and 3000MB/s write. It's supported by the PCIe Gen4x4 NVMe 1.4 technology standard and backwards compatible with PCIe 3.0.

SKU: B09GR3G7XJ Category: Data Storage Tags: Data Storage, Internal Data Storage, Internal Solid State Drives

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Excellent	86%
Very good	12%
Average	1%
Poor	1%
Terrible	0%

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DATE:
February 12, 2024

TOTAL:
$418.98

PAYMENT METHOD:
Secure Credit Card

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Order details

Product	Total
Lexar Professional 512GB NM800 M.2 2280 PCIe Gen4x4 NVMe Internal SSD, Solid State Drive, Up To 7000MB/s Read, for Gamers and Creative Professionals (LNM800X512G-RNNNG) × 2	$393.98
Subtotal:	$393.98
Shipping:	$25.00 **via USPS / DHL (2 - 6 days) - No PO Boxes**
Payment method:	**Secure Credit Card**
Total:	$418.98

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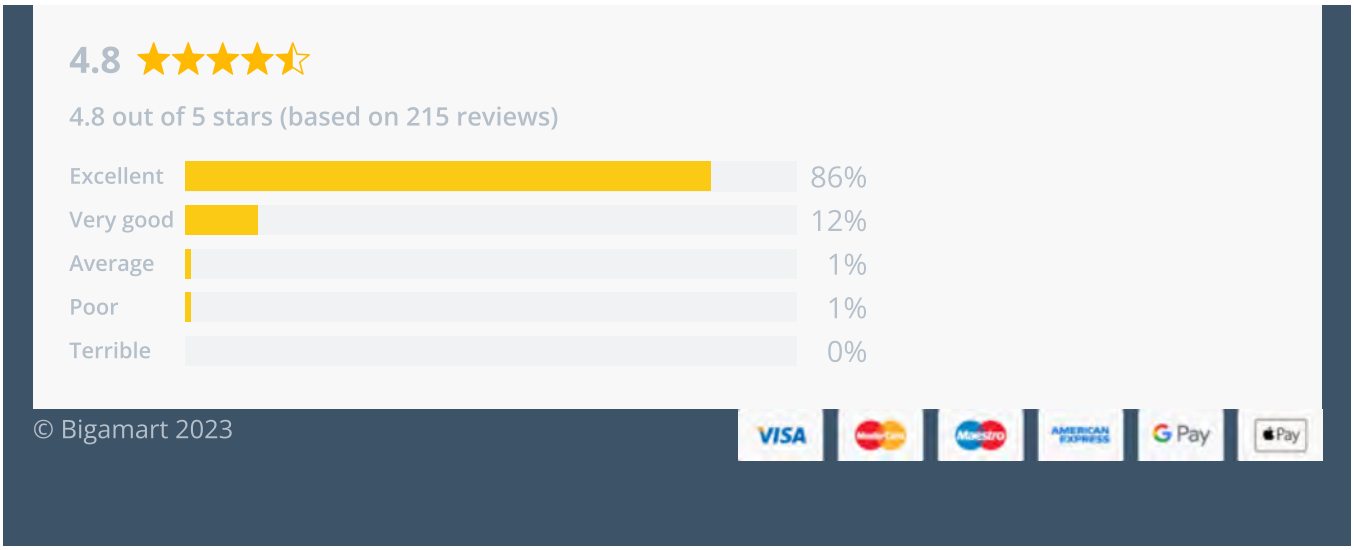
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Very good 12%
Average 1%
Poor 1%
Terrible 0%
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Subject: Your BigaMart order has been received!

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bigamart

Thank you for your order



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Thanks for your order. It's on-hold until we confirm that payment has been received.

[Order #10552271] (February 12, 2024)

Product	Quantity	Price
Lexar Professional 512GB NM800 M.2 2280 PCIe Gen4x4 NVMe Internal SSD, Solid State Drive, Up To 7000MB/s Read, for Gamers and Creative Professionals (LNM800X512G-RNNNG)	2	$393.98
Subtotal:		$393.98
Shipping:		$25.00 via USPS / DHL (2 - 6 days) - No PO Boxes
Payment method:		Secure Credit Card
Total:		$418.98

Billing address

Matthew Bonini
338 Rolling Hills Ave.
San Mateo, CA 94403
United States (US)
415-531-0507
mbonini@orrick.com

Shipping address

Matthew Bonini
Orrick Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025
United States (US)

We look forward to fulfilling your order soon.

Thank you again,
BigaMart

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Bonini, Matthew

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Subject: Your invoice is attached.

[EXTERNAL]

bigamart

Your order is Complete!



We have finished processing your order.

Tracking Information

Shipped

Shipped on: **February 15, 2024**

DHL Express 1017809435 Track Your Order

Items in this shipment



Lexar Professional 512GB NM800 M.2 2280 PCIe Gen4x4 NVMe Internal SSD, Solid State Drive, Up To 7000MB/s Read, for Gamers and Creative Professionals (LNM800X512G-RNNNG) x 2

Shipping address

Matthew Bonini
Orrick Herrington & Sutcliffe LLP
1000 Marsh Road
Menlo Park, CA 94025
United States (US)

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BigaMart

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Bonini, Matthew

From: contact@bigamart.com on behalf of BigaMart <contact@bigamart.com>
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To: Bonini, Matthew
Subject: Your Order Has Shipped

[EXTERNAL]

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Matthew Bonini
Orrick Herrington & Sutcliffe LLP
1000 Marsh Road Menlo Park, CA 94025 US

Order ID:	10552271
Order Date:	02/12/2024

Name	Price	SKU	Quantity
Lexar Professional 512GB NM800 M.2 2280 PCIe Gen4x4 NVMe Internal SSD, Solid State Drive, Up To 7000MB/s Read, for Gamers and Creative Professionals (LNM800X512G-RNNNG)	196.99	B09GR3G7XJ	2

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Exhibit 29

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Lexar NM710 1 TB

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1 TB	MAP1602A	TLC	PCIe 4.0 x4	M.2 2280
CAPACITY	CONTROLLER	FLASH	INTERFACE	FORM FACTOR















The Lexar NM710 is a solid-state drive in the M.2 2280 form factor, launched in 2023. It is available in capacities ranging from 500 GB to 2 TB. This page reports specifications for the 1 TB variant. With the rest of the system, the Lexar NM710 interfaces using a PCI-Express 4.0 x4 connection. The SSD controller is the MAP1602A Falcon Lite from MaxioTech, a DRAM cache is not available. Lexar has installed 128-layer TLC NAND flash on the NM710, the flash chips are made by YMTC. To improve write speeds, a pseudo-SLC cache is used, so bursts of incoming writes are soaked up more quickly. The cache is sized at 156 GB, once it is full, writes complete at 1500 MB/s. Copying data out of the SLC cache (folding) completes at 500 MB/s. Thanks to support for the fast PCI-Express 4.0 interface, performance is excellent. The NM710 is rated for sequential read speeds of up to 5,000 MB/s and 4,500 MB/s write.
At its launch, the SSD was priced at 54 USD. The warranty length is set to five years, which is an excellent warranty period. Lexar guarantees an endurance rating of 600 TBW, a typical value for consumer SSDs.

Solid-State-Drive	
Capacity:	1 TB (1000 GB)
Variants:	500 GB · 1 TB · 2 TB
Overprovisioning:	92.7 GB / 10.0 %
Production:	Active
Released:	2023
Price at Launch:	54 USD

Physical	
Form Factor:	M.2 2280
Interface:	PCIe 4.0 x4
Protocol:	NVMe 1.4
Power Draw:	0.79 W (Idle) 3.2 W (Avg) 4.2 W (Max)

NAND Flash

Controller	
Manufacturer:	MaxioTech
Name:	MAP1602A Falcon Lite
Architecture:	ARM 32-bit Cortex-R5
Core Count:	Quad-Core
Foundry:	TSMC
Process:	12 nm

Part Number:	LNM710X001T-RNNNG
Market:	Consumer

DRAM Cache

Type:	None
Host-Memory-Buffer (HMB):	32 MB

Features

TRIM:	Yes
SMART:	Yes
Power Loss Protection:	No
Encryption:	Unknown
RGB Lighting:	No
PS5 Compatible:	Yes

Reviews

- Techpowerup

Same Drive

This section lists other SSDs in our database using the exact same hardware components

- Silicon Power UD90

Manufacturer:	YMTC
Name:	Xtacking 2.0 (CDT1B)
Rebranded:	RH14TAA1442256G (Rebranded by Longsys)
Type:	TLC
Technology:	128-layer
Speed:	1600 MT/s
Capacity:	4 chips @ 2 Tbit
ONFI:	4.1
Topology:	Charge Trap
Die Size:	60 mm² (8.5 Gbit/mm²)
Dies per Chip:	4 dies @ 512 Gbit
Planes per Die:	4
Decks per Die:	2
Word Lines:	141 per NAND String 90.8% Vertical Efficiency
Read Time (tR):	50 µs
Program Time (tProg):	910 µs
Block Erase Time (tBERS):	20 ms
Die Read Speed:	1280 MB/s
Die Write Speed:	70 MB/s
Endurance: (up to)	3000 P/E Cycles
Page Size:	16 KB
Block Size:	2304 Pages
Plane Size:	1980 Blocks

Flash Channels:	4 @ 2,400 MT/s
Chip Enables:	4
Controller Features:	HMB (enabled)

Performance

Sequential Read:	5,000 MB/s
Sequential Write:	4,500 MB/s
Random Read:	Unknown
Random Write:	Unknown
Endurance:	600 TBW
Warranty:	5 Years
MTBF:	1.5 Million Hours
Drive Writes Per Day (DWPD):	0.3
SLC Write Cache:	approx. 156 GB (dynamic only)
Speed when Cache Exhausted:	approx. 1500 MB/s
Cache Folding Speed:	500 MB/s

Notes

Controller:

This controller features multiples variants:
F1C - Uses NVMe 1.4
F2C - Uses NVMe 1.4
F3C - Uses NVMe 2.0
F3C U - For 4TB SSDs and uses NVMe 2.0

NAND Die:

Read Time (tR): Maximum is 50 µs, typical is lower
Program Time (tPROG): Maximum is 910 µs, typical is lower
Block Erase Time (tBERS): Maximum is 20 ms, typical is lower
Array Eficiency of over 92%
YMTC 128L Xtacking 2.0 cell architecture consists of two decks connected through deck-interface buffer layer which is the same process with KIOXIA 112L BiCS 3D NAND structure. Cell size, CSL pitch, and 9-hole VC layouts keep the same design and dimension (horizontal/vertical WL and BL pitches) with previous

```
64L Xtacking 1.0 cell. Total number of gates is 141 (141T) including selectors and dummy WLs for the TLC
operation.
This layout has a 1x 4 Plane layout, each one lineup side by side
```

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TECHPOWERUP





Lexar NM710 1 TB Review

Discuss in our Forums 13

by W1zzard, on Oct 19th, 2023, in SSD. Manufacturer: Lexar

Pictures & Components »

Introduction

Lexar has made a name for itself in the portable storage market—they are very well known for their SD cards and USB drives, so it's natural for them to expand into other areas of flash storage, like consumer SSDs. Lexar was founded as a subsidiary of Micron, but was sold to Longsys in 2017 and has been operating quite independently since.



Today, we're reviewing the Lexar NM710 1 TB, the latest PCI-Express 4.0 M.2 NVMe SSD introduced by the company as their new entry-level option. Just like the NM790 that we reviewed a few weeks ago, the NM710 is based on the Maxiotech MAP1602 controller paired with YTMC 3D TLC NAND flash. Unlike the NM790, which uses the newer 232-layer NAND, the NM710 is built with the slightly older and more affordable 128-layer X2-9060 TLC flash. A DRAM cache chip is not included, just like on other MAP1602 designs, to help achieve the highly competitive price point of $89 for 2 TB (yes, 2 TB, not 1 TB).

The Lexar NM710 is available in capacities of 512 GB ($33), 1 TB ($47) and 2 TB ($89) . Endurance for these models is set to 300 TBW, 600 TBW and 1200 TBW, respectively. Lexar includes a five-year warranty with the NM710.

Specifications: Lexar NM710 1 TB SSD	
Brand:	Lexar
Model:	LNM710X001T
Capacity:	1000 GB (931 GB usable)

Specifications: Lexar NM710 1 TB SSD	
	24 GB additional overprovisioning
Controller:	Maxiotech MAP1602A
Flash:	YMTC 128-Layer 3D TLC
DRAM:	N/A, but 32 MB Host-Memory-Buffer (HMB)
Endurance:	600 TBW
Form Factor:	M.2 2280
Interface:	PCIe Gen 4 x4, NVMe 1.4
Device ID:	Lexar SSD NM710 1TB
Firmware:	9742
Warranty:	5 years
Price at Time of Review:	$47 / $47 per TB

Page: 1- Introduction & Specifications View as single page

Next Page »
Pictures & Components

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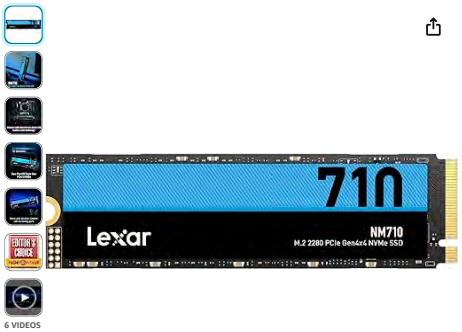
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6 VIDEOS

Roll over image to zoom in

Lexar 1TB NM710 SSD PCIe Gen4 NVMe M.2 2280 Internal Solid State Drive, Up to 5000/4500 MB/s Read/Write (LNM710X001T-RNNNU)

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4.8 ★★★★★ 820 ratings | Search this page

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Style: **NM710**

NM710 | NM620 | NM790 | NM800 PRO | NM800 PRO w/ Heatsink | NM790 w/ Heatsink | PLAY

Pattern: **2280**

2280 | 2230

Capacity: **1TB**

500GB | 512GB | **1TB** | 2TB | 4TB

Digital Storage Capacity	1024 GB
Hard Disk Interface	NVMe
Connectivity Technology	PCIe
Brand	Lexar
Special Feature	Shock Resistant

See more

About this item

- High-speed PCIe Gen4x4 interface
- Features HMB (Host Memory Buffer) 3.0 and SLC Cache technology
- Shock and vibration resistant with no moving parts
- More than 40% faster speed than PCIe 3.0 SSDs
- [1TB] Sequential read speed up to 5000MB/s, sequential write speed up to 4500MB/s
- [1TB] 600TBW
- Five-year limited warranty

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Price	$64.99	-13% $104.99 List: $119.99	$69.99	$199.99
Delivery	Get it as soon as **Tuesday, Feb 20**	—	—	Get it **Feb 26 - 27**
Customer Ratings	4.8 ★★★★★ 820	4.8 ★★★★★ 820	4.7 ★★★★½ 100,841	5.0 ★★★★★ 6
Easy To Install	4.8 ★★★★★	4.8 ★★★★★	4.7 ★★★★★	5.0 ★★★★★
Value For Money	4.7 ★★★★★	4.7 ★★★★★	4.6 ★★★★★	5.0 ★★★★★
Storage Capacity	4.8 ★★★★★	4.8 ★★★★★	4.7 ★★★★★	—
For Gaming	4.7 ★★★★★	4.7 ★★★★★	4.5 ★★★★★	—
Sold By	Amazon.com	NUTech	Amazon.com	PENNPC
Storage Capacity	1024 GB	2000 GB	1 TB	256 GB
Hardware Interface	solid state drive	solid state drive	sata 6 0 gb	pci express x4, solid state drive
Compatible Devices	Desktop	Desktop	Desktop, Laptop	Desktop
Form Factor	—	—	2.5-inch	—
Write Speed	4500 megabits per second	4500 megabits per second	510	—
Read Speed	5000 megabytes per second	5000 megabytes per second	560 megabytes per second	—

Product information

Technical Details

Collapse all

Summary

Hard Drive	2 TB Solid State Drive

Other Technical Details

Brand	Lexar
Series	NM710
Item model number	LNM710X001T-RNNNU
Item Weight	0.24 ounces
Package Dimensions	6.46 x 4.09 x 0.59 inches
Color	Black
Flash Memory Size	1 TB
Hard Drive Interface	NVMe
Manufacturer	Lexar International
ASIN	B0C5S3MKQX
Country of Origin	Taiwan
Date First Available	May 19, 2023

Additional Information

Customer Reviews	4.8 ★★★★★ 820 ratings 4.8 out of 5 stars
Best Sellers Rank	#257 in Internal Solid State Drives

Warranty & Support

Amazon.com Return Policy: You may return any new computer purchased from Amazon.com that is "dead on arrival," arrives in damaged condition, or is still in unopened boxes, for a full refund within 30 days of purchase. Amazon.com reserves the right to test "dead on arrival" returns and impose a customer fee equal to 15 percent of the product sales price if the customer misrepresents the condition of the product. Any returned computer that is damaged through customer misuse, is missing parts, or is in unsellable condition due to customer tampering will result in the customer being charged a higher restocking fee based on the condition of the product. Amazon.com will not accept returns of any desktop or notebook computer more than 30 days after you receive the shipment. New, used, and refurbished products purchased from Marketplace vendors are subject to the returns policy of the individual vendor.

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What's in the box

- SSD

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From the manufacturer



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(1) Up to 5000MB/s read transfer, write transfer speeds lower. Speeds based on internal testing. Actual performance may vary. (2) Comparison based on internal testing. Actual performance may vary. (3) Shock-resistant (1500G, duration 0.5ms, Half Sine Wave) and vibration-resistant (10~2000Hz, 1.5mm, 20G, 1 Oct/min, 30min/axis(X,Y,Z)). Based on internal testing. Actual performance may vary.

Actual usable memory capacity may vary. 1GB equals 1 billion bytes.

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Product guides and documents

Specification Sheet (PDF)

Product Description

The Lexar NM710 M.2 2280 PCIe Gen4x4 NVMe SSD is designed to boost your computing experience with faster Gen4x4 performance. With quick transfer speeds of up to 5000 MB/s read and 4500 MB/s write, this compact SSD with storage up to 2TB allows for faster, more efficient load times.

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Customer reviews

★★★★★ 4.8 out of 5

820 global ratings

5 star	87%
4 star	9%
3 star	1%
2 star	1%
1 star	2%

How customer reviews and ratings work

Customers say

Customers like the quality, performance, ease of installation, value, and speed of the computer drive. For example,they mention that it's a reliable SSD, runs fine using the heatsink that comes with the mobo, and is easy to install. That said, some appreciate the high transfer rates and the fast boot times.

AI-generated from the text of customer reviews

Speed | Performance | Quality | Value | Ease of installation | Thermal properties

Reviews with images

See all photos ›



Case 3:23-cv-05792-RFL Document 95-29 Filed 03/16/24 Page 11 of 15

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Top reviews

Top reviews from the United States

Jack L.

Nice SSD

Reviewed in the United States on February 11, 2024

Style: NM790 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

I'm using this 1TB SSD as my boot drive, and it is fast and works flawlessly. It offers great capacity and speed at a reasonable price point. It was easy to install in my new build.

Helpful | Report

Mauricio

Great Budget SSD with Effective Heatsin

Reviewed in the United States on December 20, 2023

Style: NM790 w/ Heatsink | Pattern: 2280 | Capacity: 1TB | Verified Purchase

I purchased the Lexar NM790 SSD with Heatsink 1TB PCIe Gen4 NVMe M.2 2280 for my budget PC build, and I'm quite satisfied with its performance.

The inclusion of the heatsink is a nice touch, as it helps keep the drive cool during heavy usage, ensuring consistent performance. The product's build quality appears to be decent, which is essential for long-term durability.

The SSD has worked flawlessly for my needs, and I've experienced noticeable improvements in load times and overall system responsiveness. It offers good value for the price, making it an excellent choice for those on a budget.

I'm pleased with my purchase and would definitely consider buying another Lexar NM790 SSD in the future.

6 people found this helpful

Helpful | Report

Critterbob

Great for a Second Drive

Reviewed in the United States on December 22, 2023

Style: NM790 w/ Heatsink | Pattern: 2280 | Capacity: 4TB | Verified Purchase

I'm using this for a data drive in a newly purchased computer. Access to the drive is very fast. The drive come unformatted, so, if using Windows, you must access the drive and format it through the Device Manager. It's an easy process (look it up on the web, if you don't know how) and everything works great. Very dependable. Since I've had this less than a month, I cannot say anything about its longevity, but I have used Lexar memory cards with no failures. I purchased this with the heat sink for added protection, although the other drive in the computer does not have one. Extra protection is always a better choice. I am pleased with the drive and am sure I will get many years of flawless performance.

One person found this helpful

Helpful | Report

B. Russo

Great amount of storage for an excellent price.

Reviewed in the United States on December 10, 2023

Style: NM790 | Pattern: 2280 | Capacity: 4TB | Verified Purchase

I've been looking at getting a larger NVMe SSD for a year or so now but prices have largely remained steady up until Fall off this year when they really started to get more affordable.

This is replacing an older Gen 3 MP510 960GB. I was getting rather tired of having to pick and choose what I wanted installed on the drive.

I picked the Lexar after reading numerous reviews and seeing nothing but positives.

It's TLC based drive unlike most of the others around this price point for 4TB models. QLC drives have their own issues, the most concerning being longevity, as their NAND is much more easily worn out and typically do have any DRAM so in heavy or intense workloads they can drop to speeds like that of normal mechanical hard drive.

It's got a rather high endurance rating, over twice the 1400 TBW of the drive out replaced. This was

Read more

10 people found this helpful

Helpful | Report

Brandon Buhr

high quality, fast, good price

Reviewed in the United States on February 3, 2024

Style: NM790 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

works great, no complaints

Helpful | Report

SebastianMF

Nice but.....

Reviewed in the United States on February 7, 2024

Style: NM710 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

Very good purchase, very good price, capacity and speed. The only thing I noticed is that it is somewhat hot at full load, so keep that in mind when purchasing it, if you don't have a motherboard with aluminum heatsinks for NVMe it is better not to buy it since at full load it goes up to 66 degrees. I would not recommend it for a laptop or console. But yes for a desktop computer with good ventilation.

YMTC EXHIBIT 1021
Page 565 of 629

One person found this helpful

Helpful | Report

Kim Taylor

Awesome upgrade!

Reviewed in the United States on December 26, 2023

Style: NM790 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

I purchased a portable ORICO M.2 NVMe USB SSD enclosure to clone the almost full 128GB NVMe SSD that came in my Lenovo IdeaPad-3 14IIL05 laptop. I installed this new Lexar 2TB NVMe SSD in the portable USB enclosure, and used EaseUS Disk Copy Pro to clone the 128GB SSD to this Lexar 2TB NVMe SSD via the laptop USB port. The whole cloning process took about ten minutes. I then safely ejected the ORICO M.2 NVMe SSD USB enclosure containing the Lexar 2TB NVMe SSD. After removing the bottom of the Lenovo IdeaPad-3 14IIL05 laptop, I disconnected the small battery plug from the motherboard and removed the 128GB NVMe SSD from its slot and replaced it with the new Lexar 2TB NVMe SSD that I had removed from the ORICO M.2 NVMe SSD USB enclosure after the cloning process. I applied the longer thermal sticky pad that came with the new Lexar 2TB NVMe SSD, reconnected the battery plug on the motherboard, and reinstalled the bottom panel of the laptop. I plugged in the laptop power adapter and booted up the laptop. Everything is working perfectly. My Lenovo laptop now boots up much faster than before, and I now have a ton of extra drive space for music and videos. I'm 100% happy with this purchase!

2 people found this helpful

Helpful | Report

Sqoopi

Works well so far

Reviewed in the United States on January 7, 2024

Style: NM790 | Pattern: 2280 | Capacity: 4TB | Verified Purchase

Runs fine using heatsink comes with mobo, easy to install. Not into name brand or speed test much, as long as I can see stuffs moving fast, and The price is right. Lexar has been there forever, I have confidence this SSD will last.

Helpful | Report

See more reviews ›

Top reviews from other countries

Translate all reviews to English

Simon Green

Works great in BosGame B100 Mini PC

Reviewed in Canada on February 12, 2024

Style: NM710 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

Upgraded an m.2 SSD in a Mini PC (BosGame B100) for extra capacity and faster performance to use as an Umbrel node - great budget option when you don't need the ultimate performance.

Report

Erick Torres

Fantastic

Reviewed in Canada on February 9, 2024

Style: NM790 | Pattern: 2280 | Capacity: 512GB | Verified Purchase

Very good SSD, it fits very well and comes with their screw, it is amazing terms of performance, I updated from HDD and now my computer is as fast as a new one.

Report

Michael H.

Very good ssd. Works well in HP Pavillion

Reviewed in Canada on February 5, 2024

Style: NM790 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

Initially purchased WD Green 1TB SSD as an upgrade for my HP Pavillion cs3003ca boot drive. Laptop would not recognize the WD SSD. Returned for refund and ordered this instead. Mirrored the existing SSD to the Lexamark SSD using clonezilla. Installed in laptop and although recognized the SSD, was giving a windows boot error. Followed blue screen options to re-install windows 11. Re-installation ran perfectly and computer functions really well with the new Lexmark SSD as the boot drive. Bit of a process, but happy with the end result.

Report

Christian O.

Fantastic Performance for the Price

Reviewed in Canada on January 25, 2024

Style: NM710 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

I was short on storage and my board had an unused M2 port available.

I always trusted Lexar and, once again, I was not disappointed. Performance is stellar for the price range,

reaching above 1,2 GB/sec in some cases.
Although it is fairly recent, I doubt reliability is going to be a concern.

Report

Jesus Najera

★★★★★ **CALIDAD-PRECIO**

Reviewed in Mexico on January 23, 2024

Style: NM790 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

Antes mi laptop tardaba hasta un minuto y medio en encender completamente y ahora con el ssd solo tarda maximo 2 a 3 segundos una enorme diferencia, y no me quiero imaginar como debe ser si le saco toda la velocidad posible ya que mi laptop solo puede alcanzar velocidades de 3 gb y el ssd alcanza hasta 7.4 gb de escritura, pero en general muy buen producto.

Report

Translate review to English

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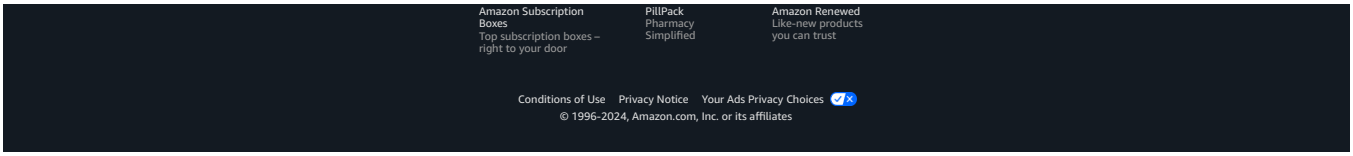
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Order Placed: February 8, 2024
Amazon.com order number: 113-5608959-5091462
Order Total: $142.16

Shipped on February 8, 2024

Items Ordered	Price
2 of: *Lexar NM710 SSD 1TB PCIe Gen4 NVMe M.2 2280 Internal Solid State Drive, Up to 5000MB/s (LNM710X001T-RNNNU)* Sold by: Amazon.com Services, Inc Supplied by: Other Condition: New	$64.99

Shipping Address:
Matthew G. Bonini
ORRICK HERRINGTON & SUTCLIFFE LLP
1000 MARSH RD
MENLO PARK, CA 94025-1015
United States

Shipping Speed:
FREE Prime Delivery

Payment information

Payment Method:
Visa ending in 3597

Billing address
Matthew Bonini
338 ROLLING HILLS AVE
SAN MATEO, CA 94403-4321
United States

Credit Card transactions

Item(s) Subtotal:	$129.98
Shipping & Handling:	$0.00
Total before tax:	$129.98
Estimated tax to be collected:	$12.18
Grand Total:	**$142.16**
Visa ending in 3597: February 8, 2024:	$142.16

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Exhibit 30

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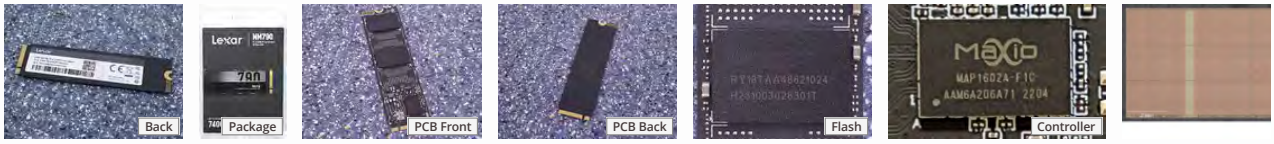


Lexar NM790 2 TB

Report an Error

2 TB	MAP1602A	TLC	PCIe 4.0 x4	M.2 2280
CAPACITY	CONTROLLER	FLASH	INTERFACE	FORM FACTOR





The Lexar NM790 is a solid-state drive in the M.2 2280 form factor, launched in 2023. It is available in capacities ranging from 512 GB to 4 TB. This page reports specifications for the 2 TB variant. With the rest of the system, the Lexar NM790 interfaces using a PCI-Express 4.0 x4 connection. The SSD controller is the MAP1602A Falcon Lite from MaxioTech, a DRAM cache is not available. Lexar has installed 232-layer TLC NAND flash on the NM790, the flash chips are made by YMTC. To improve write speeds, a pseudo-SLC cache is used, so bursts of incoming writes are handled more quickly. The cache is sized at 280 GB, once it is full, writes complete at 2500 MB/s. Copying data out of the SLC cache (folding) completes at 800 MB/s. Thanks to support for the fast PCI-Express 4.0 interface, performance is excellent. The NM790 is rated for sequential read speeds of up to 7,400 MB/s and 6,500 MB/s write; random IO reaches 1000K IOPS for read and 900K for writes.
At its launch, the SSD was priced at 110 USD. The warranty length is set to five years, which is an excellent warranty period. Lexar guarantees an endurance rating of 1500 TBW, a typical value for consumer SSDs.

Solid-State-Drive

Capacity:	2 TB (2048 GB)
Variants:	512 GB · 1 TB · 2 TB · 4 TB
Overprovisioning:	140.7 GB / 7.4 %
Production:	Active
Released:	2023
Price at Launch:	110 USD
Part Number:	LNM790X002T-RNNNC
Market:	Consumer

DRAM Cache

Type:	None
Host-Memory-Buffer (HMB):	32 MB

Features

Physical

Form Factor:	M.2 2280 (Single-Sided)
Interface:	PCIe 4.0 x4
Protocol:	NVMe 2.0
Power Draw:	0.80 W (Idle) 2.7 W (Avg) 3.7 W (Max)

NAND Flash

Manufacturer:	YMTC
Name:	Xtacking 3.0 (EET1A)
Rebranded:	RY18TAA48821024 H231003028301T
Type:	TLC
Technology:	232-layer
Speed:	2400 MT/s
Capacity:	2 chips @ 8 Tbit

Controller

Manufacturer:	MaxioTech
Name:	MAP1602A Falcon Lite
Architecture:	ARM 32-bit Cortex-R5
Core Count:	Quad-Core
Foundry:	TSMC
Process:	12 nm
Flash Channels:	4 @ 2,400 MT/s
Chip Enables:	4
Controller Features:	HMB (enabled)

Performance

Sequential Read:	7,400 MB/s
Sequential Write:	6,500 MB/s

TRIM:	Yes
SMART:	Yes
Power Loss Protection:	No
Encryption:	Unknown
RGB Lighting:	No
PS5 Compatible:	Yes

Reviews

- Techpowerup

Topology:	Charge Trap
Die Size:	68 mm² (15.1 Gbit/mm²)
Dies per Chip:	8 dies @ 1 Tbit
Planes per Die:	6
Decks per Die:	2
Word Lines:	253 per NAND String 91.7% Vertical Efficiency
Page Size:	16 KB

Same Drive

This section lists other SSDs in our database using the exact same hardware components

- Addlink A93
- Apacer AS2280Q4U
- Asgard AN4+
- Hikvision Hiksemi FUTURE
- Hikvision HikSemi CC700
- Hikvision HikSemi C4000

Random Read:	1,000,000 IOPS
Random Write:	900,000 IOPS
Endurance:	1500 TBW
Warranty:	5 Years
MTBF:	1.5 Million Hours
Drive Writes Per Day (DWPD):	0.4
SLC Write Cache:	approx. 280 GB (dynamic only)
Speed when Cache Exhausted:	approx. 2500 MB/s
Cache Folding Speed:	800 MB/s

Notes

Controller:
This controller features multiples variants:
F1C - Uses NVMe 1.4
F2C - Uses NVMe 1.4
F3C - Uses NVMe 2.0
F3C U - For 4TB SSDs and uses NVMe 2.0

NAND Die:
Wordline pitch - 48nm
Bitline pitch - 39nm

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Lexar NM790 2 TB Review

by W1zzard, on Nov 2nd, 2023, in SSD. Manufacturer: Lexar

Discuss in our Forums 33

Pictures & Components »

Introduction

Lexar has made a name for itself in the portable storage market—they are very well known for their SD cards and USB drives, so it's natural for them to expand into other areas of flash storage, such as consumer SSDs. Lexar was founded as a subsidiary of Micron, but was sold to Longsys in 2017 and has been operating quite independently since.



Just a few weeks ago we reviewed the Lexar NM790 4 TB. While 4 TB is a ton of capacity, a lot of readers have been wondering how the 2 TB model performs. That's why we have the 2 TB model for review today. Just like the 4 TB model, the NM790 2 TB uses the Maxiotech MAP1602 controller that we've seen on drives like the Acer Predator GM7, Colorful CN700 and Netac NV7000-T. There's also no change in the flash chips, the NAND flash is 232-layer TLC, made by YMTC. There's just two instead of four chips. Just like on other MAP1602 designs, a DRAM cache chip is not included.

The Lexar NM790 is available in capacities of 512 GB ($45), 1 TB ($63), 2 TB ($110) and 4 TB ($190). Endurance for these models is set to 500 TBW, 1000 TBW, 1500 TBW and 3000 TBW, respectively. Lexar includes a five-year warranty with the NM790.

Specifications: Lexar NM790 2 TB SSD	
Brand:	Lexar
Model:	LNM790X002T
Capacity:	2048 GB (1907 GB usable)

YMTC EXHIBIT 1021
Page 573 of 629

Specifications: Lexar NM790 2 TB SSD	
	No additional overprovisioning
Controller:	Maxiotech MAP1602A
Flash:	YMTC 232-Layer 3D TLC
DRAM:	N/A, but 32 MB Host-Memory-Buffer (HMB)
Endurance:	1500 TBW
Form Factor:	M.2 2280
Interface:	PCIe Gen 4 x4, NVMe 2.0
Device ID:	Lexar SSD NM790 2TB
Firmware:	9597
Warranty:	5 years
Price at Time of Review:	$110 / $54 per TB

Page: 1- Introduction & Specifications View as single page

Next Page »
Pictures & Components

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6 VIDEOS

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Lexar 2TB NM790 SSD PCIe Gen4 NVMe M.2 2280 Internal Solid State Drive, Up to 7400/6500 MB/s Read/Write, Compatible with PS5, for Gamers and Creators, Black (LNM790X002T-RNNNU)

Visit the Lexar Store

4.8 ★★★★★ 820 ratings | Search this page

Amazon's Choice in Internal Solid State Drives by Lexar

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Style: **NM790**

NM710 | NM620 | **NM790** | NM800 PRO | NM800 PRO w/ Heatsink | NM790 w/ Heatsink | PLAY

Pattern: **2280**

2280 | 2230

Capacity: **2TB**

500GB | 512GB | 1TB | **2TB** | 4TB

Digital Storage Capacity	2000 GB
Hard Disk Interface	NVMe
Connectivity Technology	M.2
Brand	Lexar
Special Feature	Single-sided design
Hard Disk Form Factor	2280 Inches

See more

About this item

- [2TB] Exceptional performance up to 7400MB/s read, 6500MB/s write; 1500TBW
- 2x faster than PCIe Gen 3 SSDs
- Up to 40% less power consumption than DRAM cache-enabled PCIe Gen 4 SSDs
- Host Memory Buffer (HMB) 3.0 activates the DRAM cache function of your device for a smoother transfer speed and seamless performance
- Designed for hardcore gamers, professionals, and creators
- Compatible with PlayStation 5
- Single-sided NVMe SSD is perfect for laptops
- Five-year limited warranty

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	Add to Cart	Add to Cart	Add to Cart	Add to Cart
Price	$129.99	$151.99	$249.99	$83.99
Delivery	Get it as soon as **Tuesday, Feb 20**	Get it as soon as **Tuesday, Feb 20**	Get it as soon as **Tuesday, Feb 20**	Get it as soon as **Tuesday, Feb 20**
Customer Ratings	4.8 ★★★★★ 820	4.8 ★★★★★ 6,755	4.8 ★★★★★ 820	4.7 ★★★★½ 8
Easy To Install	4.8 ★★★★½	4.8 ★★★★½	4.8 ★★★★½	—
Storage Capacity	4.8 ★★★★½	4.7 ★★★★½	4.8 ★★★★½	—
For Gaming	4.7 ★★★★½	4.5 ★★★★½	4.7 ★★★★½	—
Value For Money	4.7 ★★★★½	4.5 ★★★★½	4.7 ★★★★½	—
Longevity	4.8 ★★★★½	—	4.8 ★★★★½	—
Sold By	Amazon.com	Amazon.com	Amazon.com	DATOTEK
Storage Capacity	2000 GB	2 TB	4000 GB	1 TB
Hardware Interface	solid state drive	solid state drive	solid state drive	solid state drive
Compatible Devices	Desktop, PS5, Laptop	Gaming Console	Desktop, PS5, Laptop	Desktop, Laptop, Gaming Console
Form Factor	M 2	compact form	M 2	M.2
Write Speed	6500 megabits per second	6800 megabits per second	6500 megabits per second	3200 megabits per second
Read Speed	—	7100 megabytes per second	—	5000 megabytes per second

YMTC EXHIBIT 1021
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Product information

Technical Details

Collapse all

Summary

Hard Drive	Solid State Drive

Other Technical Details

Brand	Lexar
Series	NM790
Item model number	LNM790X002T-RNNNU
Item Weight	0.208 ounces
Package Dimensions	6.5 x 4.13 x 0.67 inches
Color	Black
Flash Memory Size	2 TB
Hard Drive Interface	NVMe
Manufacturer	Lexar International
ASIN	B0C91X5DZL
Country of Origin	Taiwan
Date First Available	July 14, 2023

Additional Information

Customer Reviews	4.8 ★★★★★ 820 ratings 4.8 out of 5 stars
Best Sellers Rank	#122 in Internal Solid State Drives

Warranty & Support

Amazon.com Return Policy: You may return any new computer purchased from Amazon.com that is "dead on arrival," arrives in damaged condition, or is still in unopened boxes, for a full refund within 30 days of purchase. Amazon.com reserves the right to test "dead on arrival" returns and impose a customer fee equal to 15 percent of the product sales price if the customer misrepresents the condition of the product. Any returned computer that is damaged through customer misuse, is missing parts, or is in unsellable condition due to customer tampering will result in the customer being charged a higher restocking fee based on the condition of the product. Amazon.com will not accept returns of any desktop or notebook computer more than 30 days after you receive the shipment. New, used, and refurbished products purchased from Marketplace vendors are subject to the returns policy of the individual vendor.

Manufacturer's warranty can be requested from customer service. Click here to make a request to customer service.

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What's in the box

- SSD

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From the manufacturer



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(1) Up to 7400MB/s read transfer, up to 6500MB/s write. Speeds based on internal testing. Actual performance may vary. (2) Comparison based on internal testing. Actual performance may vary.

Actual usable memory capacity may vary. 1GB equals 1 billion bytes.

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Product guides and documents

Specification Sheet (PDF)

Product Description

Whether you're looking to rampage in your favorite game or create massive, high-res files, the Lexar NM790 M.2 2280 PCIe Gen 4x4 NVMe SSD helps you get it done. It delivers incredible speeds of 7400MB/s read, 6500MB/s write thanks to its PCIe Gen4 tech, which includes HMB 3.0 and Dynamic SLC Cache. It's compatible with desktop computers, laptops, and PlayStation5, so whatever your pursuits, it's game.

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Customer reviews

4.8 out of 5

820 global ratings

5 star	87%
4 star	9%
3 star	1%
2 star	1%
1 star	2%

How customer reviews and ratings work

Customers say

Customers like the quality, performance, ease of installation, value, and speed of the computer drive. For example,they mention that it's a reliable SSD, runs fine using the heatsink that comes with the mobo, and is easy to install. That said, some appreciate the high transfer rates and the fast boot times.

AI-generated from the text of customer reviews

Speed | Performance | Quality | Value | Ease of installation | Thermal properties

Reviews with images

See all photos ›



Case 3:23-cv-05792-RFL Document 95-30 Filed 03/16/24 Page 10 of 14

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Top reviews

Top reviews from the United States

Jack L.

Nice SSD

Reviewed in the United States on February 11, 2024

Style: NM790 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

I'm using this 1TB SSD as my boot drive, and it is fast and works flawlessly. It offers great capacity and speed at a reasonable price point. It was easy to install in my new build.

Helpful | Report

Mauricio

Great Budget SSD with Effective Heatsin

Reviewed in the United States on December 20, 2023

Style: NM790 w/ Heatsink | Pattern: 2280 | Capacity: 1TB | Verified Purchase

I purchased the Lexar NM790 SSD with Heatsink 1TB PCIe Gen4 NVMe M.2 2280 for my budget PC build, and I'm quite satisfied with its performance.

The inclusion of the heatsink is a nice touch, as it helps keep the drive cool during heavy usage, ensuring consistent performance. The product's build quality appears to be decent, which is essential for long-term durability.

The SSD has worked flawlessly for my needs, and I've experienced noticeable improvements in load times and overall system responsiveness. It offers good value for the price, making it an excellent choice for those on a budget.

I'm pleased with my purchase and would definitely consider buying another Lexar NM790 SSD in the future.

6 people found this helpful

Helpful | Report

Critterbob

Great for a Second Drive

Reviewed in the United States on December 22, 2023

Style: NM790 w/ Heatsink | Pattern: 2280 | Capacity: 4TB | Verified Purchase

I'm using this for a data drive in a newly purchased computer. Access to the drive is very fast. The drive come unformatted, so, if using Windows, you must access the drive and format it through the Device Manager. It's an easy process (look it up on the web, if you don't know how) and everything works great. Very dependable. Since I've had this less than a month, I cannot say anything about its longevity, but I have used Lexar memory cards with no failures. I purchased this with the heat sink for added protection, although the other drive in the computer does not have one. Extra protection is always a better choice. I am pleased with the drive and am sure I will get many years of flawless performance.

One person found this helpful

Helpful | Report

B. Russo

Great amount of storage for an excellent price.

Reviewed in the United States on December 10, 2023

Style: NM790 | Pattern: 2280 | Capacity: 4TB | Verified Purchase

I've been looking at getting a larger NVMe SSD for a year or so now but prices have largely remained steady up until Fall off this year when they really started to get more affordable.

This is replacing an older Gen 3 MP510 960GB. I was getting rather tired of having to pick and choose what I wanted installed on the drive.

I picked the Lexar after reading numerous reviews and seeing nothing but positives.

It's TLC based drive unlike most of the others around this price point for 4TB models. QLC drives have their own issues, the most concerning being longevity, as their NAND is much more easily worn out and typically do have any DRAM so in heavy or intense workloads they can drop to speeds like that of normal mechanical hard drive.

It's got a rather high endurance rating, over twice the 1400 TBW of the drive out replaced. This was

Read more

10 people found this helpful

Helpful | Report

Brandon Buhr

high quality, fast, good price

Reviewed in the United States on February 3, 2024

Style: NM790 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

works great, no complaints

Helpful | Report

SebastianMF

Nice but.....

Reviewed in the United States on February 7, 2024

Style: NM710 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

Very good purchase, very good price, capacity and speed. The only thing I noticed is that it is somewhat hot at full load, so keep that in mind when purchasing it, if you don't have a motherboard with aluminum heatsinks for NVMe it is better not to buy it since at full load it goes up to 66 degrees. I would not recommend it for a laptop or console. But yes for a desktop computer with good ventilation.

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Page 579 of 629

One person found this helpful

Helpful | Report

Kim Taylor

Awesome upgrade!

Reviewed in the United States on December 26, 2023

Style: NM790 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

I purchased a portable ORICO M.2 NVMe USB SSD enclosure to clone the almost full 128GB NVMe SSD that came in my Lenovo IdeaPad-3 14IIL05 laptop. I installed this new Lexar 2TB NVMe SSD in the portable USB enclosure, and used EaseUS Disk Copy Pro to clone the 128GB SSD to this Lexar 2TB NVMe SSD via the laptop USB port. The whole cloning process took about ten minutes. I then safely ejected the ORICO M.2 NVMe SSD USB enclosure containing the Lexar 2TB NVMe SSD. After removing the bottom of the Lenovo IdeaPad-3 14IIL05 laptop, I disconnected the small battery plug from the motherboard and removed the 128GB NVMe SSD from its slot and replaced it with the new Lexar 2TB NVMe SSD that I had removed from the ORICO M.2 NVMe SSD USB enclosure after the cloning process. I applied the longer thermal sticky pad that came with the new Lexar 2TB NVMe SSD, reconnected the battery plug on the motherboard, and reinstalled the bottom panel of the laptop. I plugged in the laptop power adapter and booted up the laptop. Everything is working perfectly. My Lenovo laptop now boots up much faster than before, and I now have a ton of extra drive space for music and videos. I'm 100% happy with this purchase!

2 people found this helpful

Helpful | Report

Sqoopi

Works well so far

Reviewed in the United States on January 7, 2024

Style: NM790 | Pattern: 2280 | Capacity: 4TB | Verified Purchase

Runs fine using heatsink comes with mobo, easy to install. Not into name brand or speed test much, as long as I can see stuffs moving fast, and The price is right. Lexar has been there forever, I have confidence this SSD will last.

Helpful | Report

See more reviews ›

Top reviews from other countries

Translate all reviews to English

Simon Green

Works great in BosGame B100 Mini PC

Reviewed in Canada on February 12, 2024

Style: NM710 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

Upgraded an m.2 SSD in a Mini PC (BosGame B100) for extra capacity and faster performance to use as an Umbrel node - great budget option when you don't need the ultimate performance.

Report

Erick Torres

Fantastic

Reviewed in Canada on February 9, 2024

Style: NM790 | Pattern: 2280 | Capacity: 512GB | Verified Purchase

Very good SSD, it fits very well and comes with their screw, it is amazing terms of performance, I updated from HDD and now my computer is as fast as a new one.

Report

Michael H.

Very good ssd. Works well in HP Pavillion

Reviewed in Canada on February 5, 2024

Style: NM790 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

Initially purchased WD Green 1TB SSD as an upgrade for my HP Pavillion cs3003ca boot drive. Laptop would not recognize the WD SSD. Returned for refund and ordered this instead. Mirrored the existing SSD to the Lexamark SSD using clonezilla. Installed in laptop and although recognized the SSD, was giving a windows boot error. Followed blue screen options to re-install windows 11. Re-installation ran perfectly and computer functions really well with the new Lexmark SSD as the boot drive. Bit of a process, but happy with the end result.

Report

Christian O.

Fantastic Performance for the Price

Reviewed in Canada on January 25, 2024

Style: NM710 | Pattern: 2280 | Capacity: 2TB | Verified Purchase

I was short on storage and my board had an unused M2 port available.

YMTC EXHIBIT 1021
Page 580 of 629

I always trusted Lexar and, once again, I was not disappointed. Performance is stellar for the price range, reaching above 1,2 GB/sec in some cases.
Although it is fairly recent, I doubt reliability is going to be a concern.

Report

Jesus Najera

★★★★★ **CALIDAD-PRECIO**

Reviewed in Mexico on January 23, 2024

Style: NM790 | Pattern: 2280 | Capacity: 1TB | Verified Purchase

Antes mi laptop tardaba hasta un minuto y medio en encender completamente y ahora con el ssd solo tarda maximo 2 a 3 segundos una enorme diferencia, y no me quiero imaginar como debe ser si le saco toda la velocidad posible ya que mi laptop solo puede alcanzar velocidades de 3 gb y el ssd alcanza hasta 7.4 gb de escritura, pero en general muy buen producto.

Report

Translate review to English

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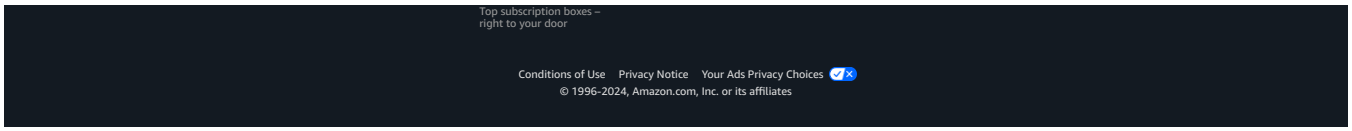
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Sell apps on Amazon
Supply to Amazon
Protect & Build Your Brand
Become an Affiliate
Become a Delivery Driver
Start a Package Delivery Business
Advertise Your Products
Self-Publish with Us
Host an Amazon Hub
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Amazon Visa
Amazon Store Card
Amazon Secured Card
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Kindle Direct Publishing Indie Digital & Print Publishing Made Easy
Amazon Photos Unlimited Photo Storage Free With Prime
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Final Details for Order #113-3740982-7333021

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Order Placed: February 6, 2024
Amazon.com order number: 113-3740982-7333021
Order Total: $282.80

Shipped on February 6, 2024

Items Ordered	Price
2 of: *Lexar NM790 SSD 2TB PCIe Gen4 NVMe M.2 2280 Internal Solid State Drive, Up to 7400MB/s, Compatible with PS5, for Gamers and Creators (LNM790X002T-RNNNU)* Sold by: Amazon.com Services, Inc Supplied by: Other Condition: New	$129.28

Shipping Address:
Matthew G. Bonini
ORRICK HERRINGTON & SUTCLIFFE LLP
1000 MARSH RD
MENLO PARK, CA 94025-1015
United States

Shipping Speed:
FREE Prime Delivery

Payment information

Payment Method:
Visa ending in 3597

Billing address
Matthew Bonini
338 ROLLING HILLS AVE
SAN MATEO, CA 94403-4321
United States

Credit Card transactions

Item(s) Subtotal:	$258.56
Shipping & Handling:	$0.00
Total before tax:	$258.56
Estimated tax to be collected:	$24.24
Grand Total:	**$282.80**
Visa ending in 3597: February 6, 2024:	$282.80

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Exhibit 31

Contact

www.linkedin.com/in/david-duffin-2a54678 (LinkedIn)

Top Skills

Product Engineering
Test Engineering
Failure Analysis

David Duffin

US General Manager and Head International Customer Sales at Yangtze Memory Technologies
Santa Clara, California, United States

Summary

Experienced Engineering leader.
• Have been in the Semiconductor / Flash Memory / Storage industry continuously since 1987, mostly in Product & Test Engineering with time spent in additional roles such as Country General Management, Customer Support, Development, Manufacturing, PMO, Customer Field Support and Physical Failure Analysis.
• Have worked with a wide range of customers in Military, Automotive, Mobile, Industrial, Enterprise, Channel and Retail markets.
• Responsible for $5B+ in shipments per year.
• Have built and managed multiple worldwide cross functional teams, of up to 350 engineers.
• Am used to regularly and directly interacting with customers, partners, and all functions within the company from the top executive to individual contributor levels
• I understand engineering is a relentless focus on time to market, cost reduction and quality improvement and the ability to balance these items to meet the market needs and to maximize profitability.
• I strongly believe in an environment of strong processes with a culture of empowerment and responsibility and believe that identifying and growing future leaders across all levels of the organization is a key attribute.

Experience

Yangtze Memory Technologies
US General Manager and Head International Customer Sales
March 2019 - Present (5 years)
San Jose, California, United States

Yangtze Memory Technologies Co.
Vice President Product & Test Engineering

May 2016 - March 2019 (2 years 11 months)
San Jose

Leading all Product, Test and Assembly Engineering for YMTC

SanDisk
VP Product & Test Engineering
April 2011 - March 2016 (5 years)

Responsible for a multidisciplinary team comprised of Memory PE, Final Product PE, Memory TE, System TE, Memory Health, ASIC and Test Equipment Engineering that owned all wafers from Die Sort (memory and controller) through to all final products including wafers, packaged memory, USB, SD/uSD, mobile and embedded MCPs, Client and Enterprise SSDs. Team was also responsible for the verification and screen development of all new die nodes, die, revisions, excursions and process changes.
Led culture change from Retail focused company to one that became a quality leader at some of the most demanding OEM customers with much improved processes and consistent delivery of schedules and world class yield and test time indices.
Grew management depth and built strongly executing teams in multiple locations in the US, Israel, Japan, China, India and Malaysia.

Spansion
11 years 5 months

Director, Program Management Office
March 2010 - April 2011 (1 year 2 months)

Responsible for the Infrastructure and Compliance of all Spansion products to Spansion's Product Life Cycle Management Systems and methodologies from design Tape Out to production End Of Life

Director, Product Engineering
December 1999 - February 2010 (10 years 3 months)

Responsible for all Product and Test Engineering Worldwide for the Wireless Solutions Division.

AMD
10 years

Product Engineer
1995 - 2005 (10 years)

Product and Device Analysis Engineer at Frimley Facility
September 1995 - November 1999 (4 years 3 months)

Electrically and Physically Analyze all AMD Flash / Eprom Customer returns in Europe.

Hughes MicroElectronics
Test Engineer at Glenrothes Facility
July 1990 - September 1995 (5 years 3 months)

Test and Product Engineering developing new ASICs and supporting Production

Education

Edinburgh Napier University
System Engineering · (1991 - 1992)

Abertay University
· (1985 - 1990)

Dundee Institute of Technology
· (1985 - 1990)

Kirkland High School
· (1979 - 1985)

Exhibit 32

BA20220583384

B0956-1752 07/28/2022 9:08 AM Received by California Secretary of State

STATE OF CALIFORNIA
Office of the Secretary of State
STATEMENT OF INFORMATION
CORPORATION
California Secretary of State
1500 11th Street
Sacramento, California 95814
(916) 653-3516

For Office Use Only

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File No.: BA20220583384

Date Filed: 7/28/2022

Entity Details

Corporation Name	YANGTZE MEMORY TECHNOLOGIES, INC.
Entity No.	3953819
Formed In	CALIFORNIA

Street Address of Principal Office of Corporation

Principal Address	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054

Mailing Address of Corporation

Mailing Address	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054
Attention	

Street Address of California Office of Corporation

Street Address of California Office	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054

Officers

Officer Name	Officer Address	Position(s)
– ~~DAVID DUFFIN~~	~~145 RIO ROBLES SAN JOSE, CA 95134~~	~~Chief Executive Officer, Secretary~~
– ~~Ying Li~~	~~145 Rio Robles San Jose, CA 95134~~	~~Chief Financial Officer~~
+ DAVID DUFFIN	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054	Chief Executive Officer, Secretary
+ YING LI	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054	Chief Financial Officer

Additional Officers

Officer Name	Officer Address	Position	Stated Position
None Entered			

Directors

Director Name	Director Address
– ~~Tuenlap Chan~~	~~145 Rio Robles San Jose, CA 95134~~
– ~~Daesik Song~~	~~145 Rio Robles San Jose, CA 95134~~
+ TUENLAP CHAN	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054
+ DAESIK SONG	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054

The number of vacancies on Board of Directors is: 1

Agent for Service of Process

B0956-1753 07/28/2022 9:08 AM Received by California Secretary of State

Agent Name	DAVID DUFFIN
Agent Address	2953 BUNKER HILL LANE STE. 206 SANTA CLARA, CA 95054

Type of Business

Type of Business	TECHNOLOGY

Email Notifications

Opt-in Email Notifications	No, I do NOT want to receive entity notifications via email. I prefer notifications by USPS mail.

Labor Judgment

No Officer or Director of this Corporation has an outstanding final judgment issued by the Division of Labor Standards Enforcement or a court of law, for which no appeal therefrom is pending, for the violation of any wage order or provision of the Labor Code.

Electronic Signature

☒ By signing, I affirm that the information herein is true and correct and that I am authorized by California law to sign.

Allie Schwenn	*07/28/2022*
Signature	Date

Exhibit 33

Contact

www.linkedin.com/in/daesik-song-a5a05221 (LinkedIn)

Top Skills

ASIC
Analog
Mixed Signal

Daesik Song

NAND Design Engneer
Sunnyvale, California, United States

Experience

YMTC
Director
February 2017 - Present (7 years 1 month)
San Jose, California

Micron Technology
Principal Design Eng.
December 2008 - February 2017 (8 years 3 months)

NAND Flash Memory design

ST Microelectronics
Senior Design Engineer
October 2003 - September 2007 (4 years)

Nand Design

Hynix
Design Engineer
1996 - 2002 (6 years)

SDR/DDR DRAM design

Education

Korea University
MS, Electrical Engineering · (1988 - 1996)

Exhibit 34

IAM

Yangtze Memory Technologies' IP strategy for independence

13 February 2024

Wuhan-based Yangtze Memory Technologies Co (YMTC) first entered the global IP transaction market when it **licensed** an IP portfolio covering DBI hybrid bonding technology from US-based Xperi in 2021. The move came only five years after the Chinese chipmaker's inception, marking an important step forward in China's push for greater semiconductor self-sufficiency.

Since then, the company has faced a fair few challenges, including a US government tech crackdown that prevented it from becoming the supplier of 128-layer 3D NAND flash memory for Apple's iPhones in 2022. Last month, the US Pentagon also **added** YMTC to its list of entities that it claims assist China's military, which already includes the likes of Huawei, Semiconductor Manufacturing International Corp and Advanced Micro-Fabrication Equipment Inc.

YMTC, however, seems determined to catch up with its competitors. In November, it **sued** US-based Micron over eight of its patents related to 3D NAND flash memory chip technology. Litigation is not YMTC's first choice to be able to compete fairly and share its innovations across the globe – but in some situations, litigation may be necessary, the company's IP Head Daniel Chan told IAM in an exclusive interview.

Chan sat down with IAM to discuss how the young company has shifted its priorities around IP, the different ways in which his unit communicates the value of their IP to the C-suite and the increasing significance of an effective trade secret strategy.

Transforming an IP unit into a strategic business partner

Chan has headed up YMTC's 40-person IP team out of China since May 2020. Together, the team manages over 3,500 active granted patents worldwide, which are spread across China, the US, Europe and several jurisdictions in Southeast Asia. "Our patent portfolio is designed to protect our innovations in markets that matter to YMTC and its partners," he says.

The IP head also notes that his team is split based on practice areas, rather than technological areas, allowing them to grow as subject matter experts whom the company's internal clients may rely upon for addressing specific IP issues. For example, the team that is responsible for patent prosecution will perform tasks such as the drafting, filing, issuance, and post-issuance practices, and will cover multiple technological areas – such as the fabrication process and circuit design around the semiconductors.

The unit sits within the business's legal organisation and reports directly to the CEO. It has always had two key objectives: safeguard the wider company's operations from IP-related risks and manage its IP assets to protect its R&D investment.

But, since his appointment, Chan has strived to build a world-class IP portfolio, and "transcended [his unit's] role to a strategic organisational partner for advancing YMTC's business objectives", he reveals.

Chan clearly understands the value of his team and the IP that he and his team manages. However, he notes that there are many ways in which this value can be communicated to the wider company, including the C-suite: "When we think about value, we often associate it with money or currency. In that sense, the value of an IP portfolio may be expressed as either revenue generated by that portfolio (eg, licensing revenue) or cost savings made possible because of that portfolio (eg, avoidance of litigation)." This concept is something most C-suite leaders can grasp, but it is up to the IP departments to quantify it in a way that is "believable and agreeable" to C-suite leadership, Chan says.

"This quantification exercise is more of an art than a science," he adds. One of the most direct approaches is through patent assertion activities, he explains, as licensing revenue and/or cross-licensing arrangements resulting from such activities may reflect at least some of the value of your portfolio.

However, patent assertion comes with varying degrees of risk – making it not such a viable option when working with C-suite leaders who are demonstrably risk-averse. In those situations, Chan says IP units may express the value of a portfolio based on various forms of projection instead.

One approach that he believes to be less controversial among in-house practitioners is framing the value of a portfolio in terms of its deterrence effect against potential litigation threats. He comments: "The credibility of this projection can be established upon benchmark data and a landscape analysis showing the relevancy of the portfolio to the market that is essential to a company's ability to generate revenue or operate its business. In the end, the delivery of this projection could be the key, and that is where the art form kicks in."

Monetisation

In November YMTC **asserted** eight of its patents against US-based Micron Technology Co before the US District Court for the Northern District of California, alleging that its rival was using its patented innovations to force YMTC out of the 3D NAND flash memory market. While Chan declined to comment directly on the pending litigation, he noted that patent enforcement could play a role in a company's IP strategy if certain conditions are met.

"The importance of this role may shift over time depending on the overall market environment and the relative position of the company," he clarified. Litigation is not YMTC's first choice to achieve its goals of competing openly and fairly "but in some situations, [it] may be necessary", he says.

Patents are not the only intangible asset that Chan understands and values. Know-how plays a "critical role" in YMTC's IP strategy. "Primarily because the nature of some innovations renders it extremely difficult, if not impossible, to receive meaningful protection under the patent system," he says.

He comments: "Some technologies are better kept secret where their intrinsic value under secrecy outweighs the value of a limited right-to-exclude. This calculus is particularly relevant to firms owning IP that is difficult to develop and even harder to discover or show that someone has used that IP. In jurisdictions where discovery is either limited or unavailable, it would be virtually impossible to prove infringement of a patent that purports to protect this type of IP."

The company has therefore developed a "rather comprehensive" strategy when it comes to trade secret protection – including the enforcement of those assets "when it is necessary".

The IP head notes that while it would like to develop a world-class IP portfolio – as a young company, YMTC understands that doing so will take time and perseverance.

Moving forward, Chan is keen on undertaking a "balanced approach" to growing YMTC's patent portfolio while ensuring the quality of its filings. "Our focus today and for the future is to be involved in building an ecosystem and continuing to make an important contribution to global economic prosperity," he says.

He adds: "The world around us continues to change, spurred on by technological advancements that pour in like waves, one after the other [...] We are proud of what we've accomplished in our first seven years, but we recognise that much work still needs to be done."

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Exhibit 35

Contact

www.linkedin.com/in/danchanipwizard (LinkedIn)
www.fr.com/Daniel-T-Chan/ (Company)

Top Skills

Patent Strategy
analog
Patent Invalidity

Languages

Chinese

Daniel Chan

Deputy General Counsel, Head of IP Department at Yangtze Memory Technologies
Richardson, Texas, United States

Summary

Daniel Chan is the Head of IP at Yangtze Memory Technologies (YMTC), where he leads a growing team of IP professionals to navigate through complex issues for advancing YMTC's competitive position in the global memory supply chain.

Daniel has extensive experience in IP portfolio and risk management, IP litigation, licensing and technology transactions, FTO clearance, and IP procurement. Daniel specializes his practice in the semiconductor and computer science sectors with a passion for tailoring balanced legal strategies to achieve various business goals and objectives.

Daniel earned a B.S. in Electrical Engineering from the University of Texas at Austin with the Highest Honor, and a J.D. from the University of California, Los Angeles. Prior to his legal career, Daniel was an analog circuit designer for Sandisk, where he helped develop the 70nm and 55nm NAND flash products.

Experience

Yangtze Memory Technologies
4 years

Deputy General Counsel, Head of Intellectual Property Department
February 2022 - Present (2 years 1 month)
Santa Clara County, California, United States

Assistance General Counsel, Head of IP Dispute & IP Licensing
March 2020 - February 2022 (2 years)
San Jose, California, United States

Texas Instruments
5 years 2 months

Senior Counsel, Chairman of Analog Power Products (APP) Patent Committee
September 2017 - February 2020 (2 years 6 months)
Dallas/Fort Worth Area

Patent Counsel
January 2015 - August 2017 (2 years 8 months)
Dallas/Fort Worth Area

Fish & Richardson P.C.
Intellectual Property Attorney
August 2011 - December 2014 (3 years 5 months)

Snell & Wilmer
Intellectual Property Attorney
April 2010 - August 2011 (1 year 5 months)
Costa Mesa

Baker & McKenzie
Summer Associate
June 2007 - August 2008 (1 year 3 months)

Christie, Parker & Hale LLP
Summer Associate
May 2008 - July 2008 (3 months)

SanDisk Company
Analog Design Engineer
June 2004 - September 2006 (2 years 4 months)

3M Corporation
Summer Internship
June 2002 - August 2003 (1 year 3 months)

Education

UCLA School of Law
J.D, Patent Law, Copyright Law, Law and Economics · (2006 - 2009)

The University of Texas at Austin
BS, Electrical and Computer Engineering · (2001 - 2004)

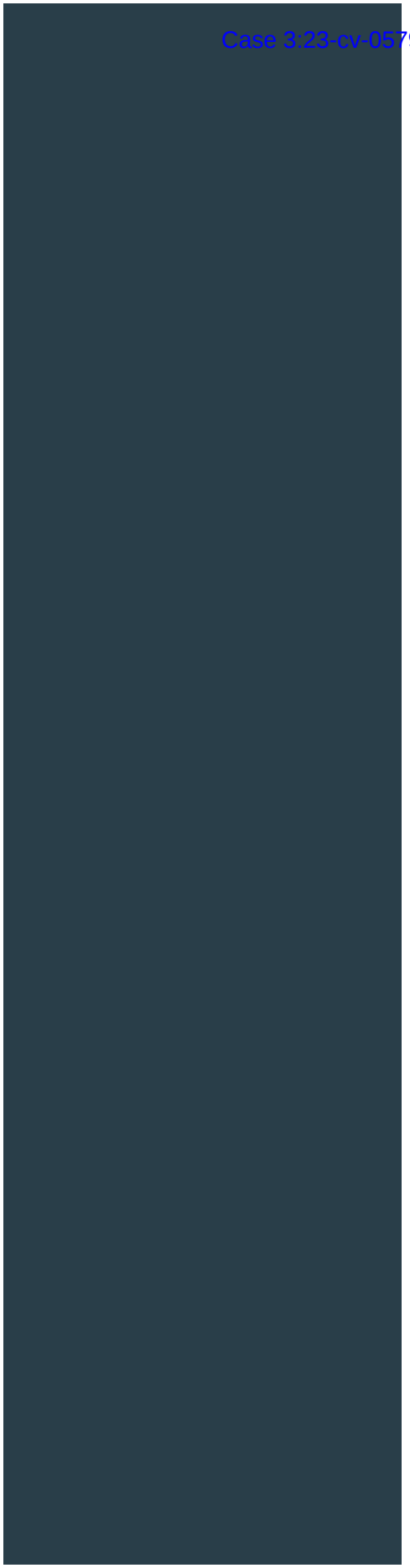


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MARK	mark
LITERAL ELEMENT	YMTC
STANDARD CHARACTERS	YES
USPTO-GENERATED IMAGE	YES
MARK STATEMENT	The mark consists of standard characters, without claim to any particular font style, size or color.
OWNER SECTION (current)	
NAME	Yangtze Memory Technologies Co., Ltd.
INTERNAL ADDRESS	Rm. 7018, No. 18 Huaguang Ave., Guandong
MAILING ADDRESS	Sci. and Tech. Ind. Park,East Lake Dvpt.
CITY	Zone, Wuhan, Hubei,
ZIP/POSTAL CODE	430074
STATE/COUNTRY/REGION/JURISDICTION/U.S. TERRITORY	China
OWNER SECTION (proposed)	
NAME	Yangtze Memory Technologies Co., Ltd.
INTERNAL ADDRESS	Rm. 7018, No. 18 Huaguang Ave., Guandong
MAILING ADDRESS	Sci. and Tech. Ind. Park,East Lake Dvpt.
CITY	Zone, Wuhan, Hubei,
ZIP/POSTAL CODE	430074
STATE/COUNTRY/REGION/JURISDICTION/U.S. TERRITORY	China
EMAIL	XXXX
ATTORNEY INFORMATION (current)	
NAME	Yue (Robert) Xu
ATTORNEY BAR MEMBERSHIP NUMBER	NOT SPECIFIED
YEAR OF ADMISSION	NOT SPECIFIED
U.S. STATE/ COMMONWEALTH/ TERRITORY	NOT SPECIFIED

FIRM NAME	APEX ATTORNEYS AT LAW, LLP
STREET	160 ALAMO PLAZA #942
CITY	ALAMO
STATE	California
POSTAL CODE	94507
COUNTRY/REGION/JURISDICTION/U.S. TERRITORY	United States
PHONE	408-647-5296
FAX	408-458-2551
EMAIL	trademark@apex-attorneys.com
DOCKET/REFERENCE NUMBER	190171YMTC-U
ATTORNEY INFORMATION (proposed)	
NAME	Yue (Robert) Xu
ATTORNEY BAR MEMBERSHIP NUMBER	XXX
YEAR OF ADMISSION	XXXX
U.S. STATE/ COMMONWEALTH/ TERRITORY	XX
FIRM NAME	APEX ATTORNEYS AT LAW, LLP
STREET	160 ALAMO PLAZA #942
CITY	ALAMO
STATE	California
POSTAL CODE	94507
COUNTRY/REGION/JURISDICTION/U.S. TERRITORY	United States
PHONE	408-647-5296
FAX	408-458-2551
EMAIL	trademark@apex-attorneys.com
DOCKET/REFERENCE NUMBER	190171YMTC-U
CORRESPONDENCE INFORMATION (current)	
NAME	YUE (ROBERT) XU
PRIMARY EMAIL ADDRESS FOR CORRESPONDENCE	trademark@apex-attorneys.com
SECONDARY EMAIL ADDRESS(ES) (COURTESY COPIES)	apex.attorneys@aol.com; trademark.aaal@gmail.com
DOCKET/REFERENCE NUMBER	190171YMTC-U
CORRESPONDENCE INFORMATION (proposed)	
NAME	Yue (Robert) Xu
PRIMARY EMAIL ADDRESS FOR CORRESPONDENCE	trademark@apex-attorneys.com
SECONDARY EMAIL ADDRESS(ES) (COURTESY COPIES)	apex.attorneys@aol.com; trademark.aaal@gmail.com
DOCKET/REFERENCE NUMBER	190171YMTC-U

GOODS AND/OR SERVICES SECTION	
INTERNATIONAL CLASS	009
CURRENT IDENTIFICATION	Semi-conductors; Wafers for integrated circuits; Electronic chips for the manufacture of integrated circuits; Integrated circuits; Semiconductor devices; Semiconductor chips; Computer chips; Silicon chips; Computer memory devices; Cell phones; Central processing units for processing information, data, sound or images; Cards with integrated circuits; Blank USB flash drives; Printed circuit boards; Computer hardware; Transistors; Central processing units (CPU) being computer hardware
GOODS OR SERVICES	KEEP ALL LISTED
FIRST USE ANYWHERE DATE	09/09/2016
FIRST USE IN COMMERCE DATE	09/09/2016
SPECIMEN FILE NAME(S)	\\TICRS\EXPORT18\IMAGEOUT 18\884\967\88496703\xml1 \ SOU0002.JPG
	\\TICRS\EXPORT18\IMAGEOUT 18\884\967\88496703\xml1 \ SOU0003.JPG
SPECIMEN DESCRIPTION	Pictures showing use of the mark on chips and integrated circuits.
REQUEST TO DIVIDE	NO
PAYMENT SECTION	
NUMBER OF CLASSES IN USE	1
SUBTOTAL AMOUNT [ALLEGATION OF USE FEE]	100
TOTAL AMOUNT	100
SIGNATURE SECTION	
DECLARATION SIGNATURE	/YUE XU r/
SIGNATORY'S NAME	Yue (Robert) Xu
SIGNATORY'S POSITION	Attorney of record, California bar member
DATE SIGNED	05/21/2020
SIGNATORY'S PHONE NUMBER	408-647-5296
FILING INFORMATION	
SUBMIT DATE	Fri May 22 14:51:12 ET 2020
TEAS STAMP	USPTO/SOU-XX.XXX.XX.XX-20 200522145112899704-884967 03-710ed1ce7ba8fd1a3669bb 6118888b55cd61688e7e485c4 1f13badb3ed1d6a7-CC-51114 452-20200520185404851192

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(15 U.S.C. Section 1051(d))

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MARK: YMTC(Standard Characters, see https://tmng-al.uspto.gov/resting2/api/img/88496703/large)
SERIAL NUMBER: 88496703

OWNER AND/OR ENTITY INFORMATION
The owner proposes to amend the following:
Current: Yangtze Memory Technologies Co., Ltd., having an address of
Rm. 7018, No. 18 Huaguang Ave., Guandong
Sci. and Tech. Ind. Park,East Lake Dvpt.
Zone, Wuhan, Hubei,, 430074
China
Proposed: Yangtze Memory Technologies Co., Ltd., having an address of
Rm. 7018, No. 18 Huaguang Ave., Guandong
Sci. and Tech. Ind. Park,East Lake Dvpt.
Zone, Wuhan, Hubei,, 430074
China
Phone:
Email: XXXX

The owner is submitting the following allegation of use information:

For International Class 009:
Current identification: Semi-conductors; Wafers for integrated circuits; Electronic chips for the manufacture of integrated circuits; Integrated circuits; Semiconductor devices; Semiconductor chips; Computer chips; Silicon chips; Computer memory devices; Cell phones; Central processing units for processing information, data, sound or images; Cards with integrated circuits; Blank USB flash drives; Printed circuit boards; Computer hardware; Transistors; Central processing units (CPU) being computer hardware

The mark is in use in commerce on or in connection with all of the goods/services, or to indicate membership in the collective organization listed in the application or Notice of Allowance or as subsequently modified for this specific class.

The mark was first used by the applicant, or the applicant's related company, licensee, or predecessor in interest at least as early as 09/09/2016, and first used in commerce at least as early as 09/09/2016, and is now in use in such commerce. The applicant is submitting one specimen for the class showing the mark as used in commerce on or in connection with any item in the class, consisting of a(n) Pictures showing use of the mark on chips and integrated circuits..
Specimen File1
Specimen File2

The applicant is not filing a Request to Divide with this Allegation of Use form.

The owner's/holder's current attorney information: Yue (Robert) Xu. Yue (Robert) Xu of APEX ATTORNEYS AT LAW, LLP, is located at

160 ALAMO PLAZA #942
ALAMO, California 94507
United States
The docket/reference number is 190171YMTC-U.

The phone number is 408-647-5296.

The fax number is 408-458-2551.

The email address is trademark@apex-attorneys.com

The owner's/holder's proposed attorney information: Yue (Robert) Xu. Yue (Robert) Xu of APEX ATTORNEYS AT LAW, LLP, is a member of the XX bar, admitted to the bar in XXXX, bar membership no. XXX, is located at

160 ALAMO PLAZA #942
ALAMO, California 94507
United States

The docket/reference number is 190171YMTC-U.

The phone number is 408-647-5296.

The fax number is 408-458-2551.

The email address is trademark@apex-attorneys.com

Yue (Robert) Xu submitted the following statement: The attorney of record is an active member in good standing of the bar of the highest court of a U.S. state, the District of Columbia, or any U.S. Commonwealth or territory.

Correspondence Information (current):
YUE (ROBERT) XU
PRIMARY EMAIL FOR CORRESPONDENCE: trademark@apex-attorneys.com
SECONDARY EMAIL ADDRESS(ES) (COURTESY COPIES): apex.attorneys@aol.com; trademark.aaal@gmail.com

The docket/reference number is 190171YMTC-U.

Correspondence Information (proposed):
Yue (Robert) Xu
PRIMARY EMAIL FOR CORRESPONDENCE: trademark@apex-attorneys.com
SECONDARY EMAIL ADDRESS(ES) (COURTESY COPIES): apex.attorneys@aol.com; trademark.aaal@gmail.com

The docket/reference number is 190171YMTC-U.

Requirement for Email and Electronic Filing: I understand that a valid email address must be maintained by the applicant owner/holder and the applicant owner's/holder's attorney, if appointed, and that all official trademark correspondence must be submitted via the Trademark Electronic Application System (TEAS).

A fee payment in the amount of $100 will be submitted with the form, representing payment for the allegation of use for 1 class.

Declaration

- ☑ The signatory believes that the applicant is the owner of the mark sought to be registered.
  For a trademark or service mark application, the mark is in use in commerce on or in connection with all the goods/services in the application or notice of allowance, or as subsequently modified.
  For a collective trademark, collective service mark, collective membership mark application, the applicant is exercising legitimate control over the use of the mark in commerce by members on or in connection with all the goods/services/collective membership organization in the application or notice of allowance, or as subsequently modified.
  For a certification mark application, the applicant is exercising legitimate control over the use of the mark in commerce by authorized users on or in connection with the all goods/services in the application or notice of allowance, or as subsequently modified, and the applicant is not engaged in the production or marketing of the goods/services to which the mark is applied, except to advertise or promote recognition of the certification program or of the goods/services that meet the certification standards of the applicant.
- ☑ The specimen(s) shows the mark as used on or in connection with the goods/services/collective membership organization in commerce.
- ☑ To the best of the signatory's knowledge and belief, no other persons, except, if applicable, authorized users, members, and/or concurrent users, have the right to use the mark in commerce, either in the identical form or in such near resemblance as to be likely, when used on or in connection with the goods/services/collective membership organization of such other persons, to cause confusion or mistake, or to deceive.
- ☑ To the best of the signatory's knowledge, information, and belief, formed after an inquiry reasonable under the circumstances, the allegations and other factual contentions made above have evidentiary support.
- ☑ The signatory being warned that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §

1001, and that such willful false statements and the like may jeopardize the validity of the application or submission or any registration resulting therefrom, declares that all statements made of his/her own knowledge are true and all statements made on information and belief are believed to be true.

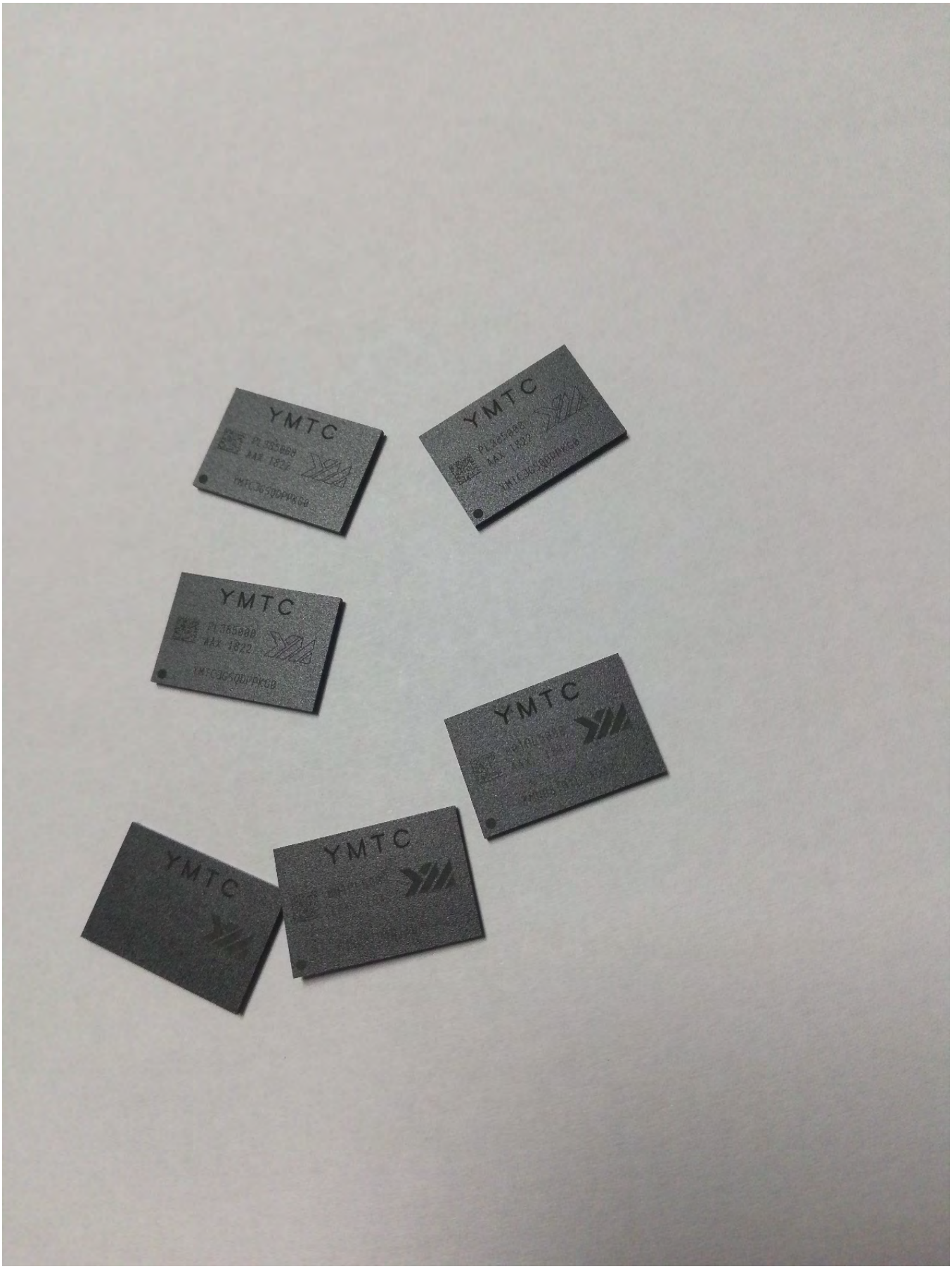
Signature: /YUE XU r/ Date Signed: 05/21/2020
Signatory's Name: Yue (Robert) Xu
Signatory's Position: Attorney of record, California bar member
Signatory's Phone: 408-647-5296

Mailing Address:
APEX ATTORNEYS AT LAW, LLP

160 ALAMO PLAZA #942
ALAMO, California 94507

RAM Sale Number: 88496703
RAM Accounting Date: 05/22/2020

Serial Number: 88496703
Internet Transmission Date: Fri May 22 14:51:12 ET 2020
TEAS Stamp: USPTO/SOU-XX.XXX.XX.XX-20200522145112899
704-88496703-710ed1ce7ba8fd1a3669bb61188
88b55cd61688e7e485c41f13badb3ed1d6a7-CC-
51114452-20200520185404851192


YMTC
YMTC
YMTC
YMTC
YMTC
YMTC


Product Name
Capacity
M.2 NVMe PCIe Gen3.0x4
P/N: XXXXXXXXXXXXXXX
RATED: DC +3.3V = 2.8A
CAN ICES-3XXX/XXXXXXXX
FW:XXXXXXXX
WARRANTY VOID IF REMOVED
CUST P/N:XXXXXXXXXX
Model:XXXXXXXXXX
SN:MBZYYWWDXXXX
EUI64: 5CD2EXXXXXXXXXX
MSIP-REM-XXX-XXXXXXXXXXXXX
PSID: 88888888888888888888888888888888
DUID: 88888888888888888888888888888888
YMTC
Xtacking TM
Yangtze Memory
Made In China

FEE RECORD SHEET

Serial Number: 88496703



RAM Sale Number: 88496703

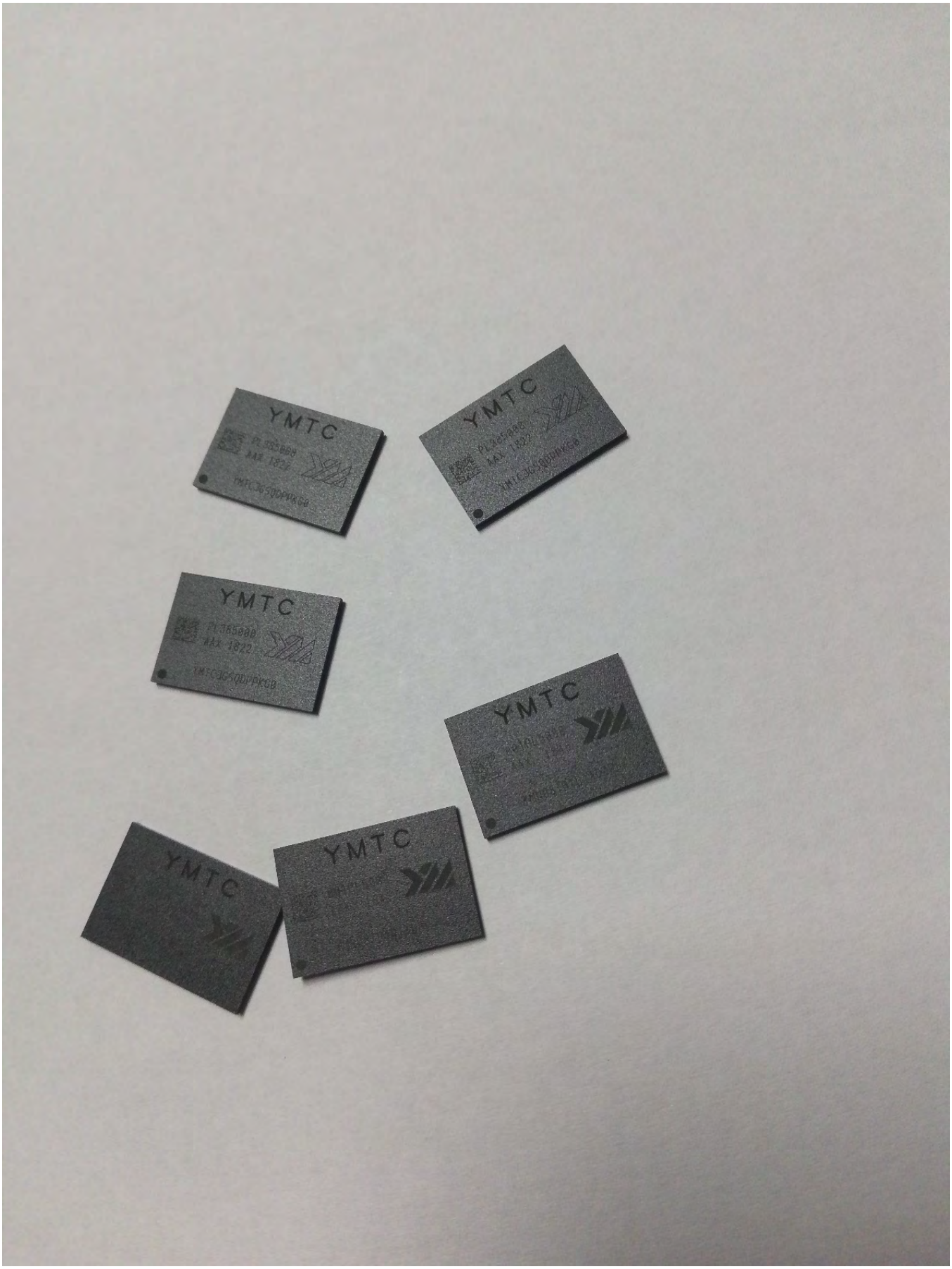
Total Fees: $100

RAM Accounting Date: 20200522

Transaction	Fee Code	Transaction Date	Fee per Class	Number of Classes	Total Fee
Statement of Use (SOU)	7003	20200522	$100	1	$100

Transaction Date: 20200522




YMTC
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YMTC
YMTC


Product Name
Capacity
M.2 NVMe PCIe Gen3.0x4
P/N: XXXXXXXXXXXXXXX
RATED: DC +3.3V = 2.8A
CAN ICES-3XXX/XXXXXXXX
FW:XXXXXXXX
WARRANTY VOID IF REMOVED
CUST P/N:XXXXXXXXXX
Model:XXXXXXXXXX
SN:MBZYYWWDXXXX
EUI64: 5CD2EXXXXXXXXXX
MSIP-REM-XXX-XXXXXXXXXXXXX
PSID: 8888888888888888888888888888888
DUID: 8888888888888888888888888888888
YMTC
Xtacking TM
Yangtze Memory
Made In China

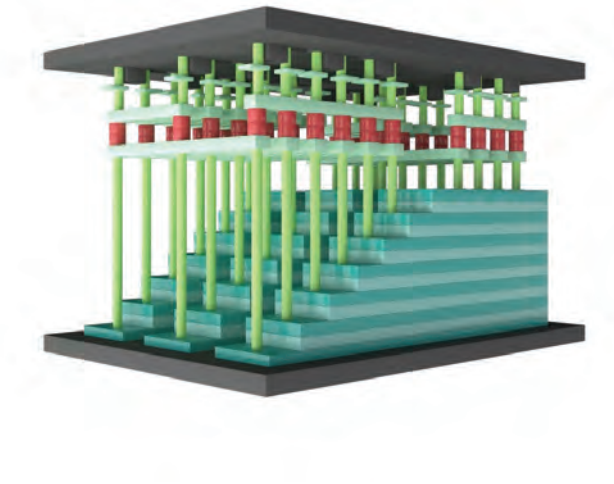
Exhibit 37

About Xtacking®-YMTC

ymtc.com/en/technicalintroduction.html

Xtacking® architecture developed by YMTC is an innovative 3D NAND technology with excellent performance

The ground-breaking technology was designed to provide enterprises and consumers with comprehensive 3D NAND related solutions.

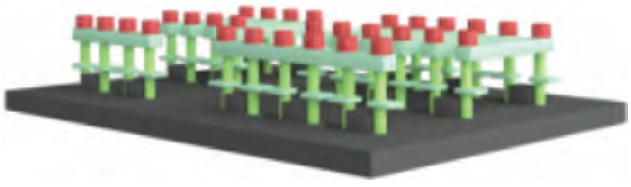


PLAY

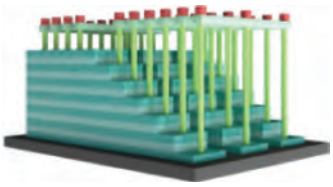
About Xtacking®

A unique way of technical development driven by innovative practice

Independent processing on separated wafers

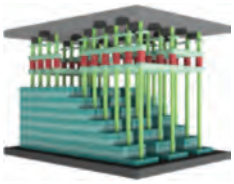


CMOS wafer



Memory cell wafer

Wafer bonding processing with millions of metal VIAs(Vertical Interconnect Accesses)



Into one wafer
Before the launch of Xtacking® architecture, 3D NAND architectures in the market were divided into traditional side-by-side structure and CnA (CMOS next to Array) architecture. After 8 years of development and 3 years of R&D verification in the 3D IC field, YMTC finally bonded two wafers to 3D NAND flash memory, with innovative layouts and precise verification. Memory cells and peripheral circuits are bonded by billions of metal VIAs on a die the size of a fingernail, and the reliability of the bonding interface is tested as effectively as what is processed on a single wafer. This new technology is bound to empower 3D NAND with technical superiority and unleash its potential. 3D NAND flash memory products based on Xtacking® will provide more cost-effective and innovative options as they scale up.

8 years

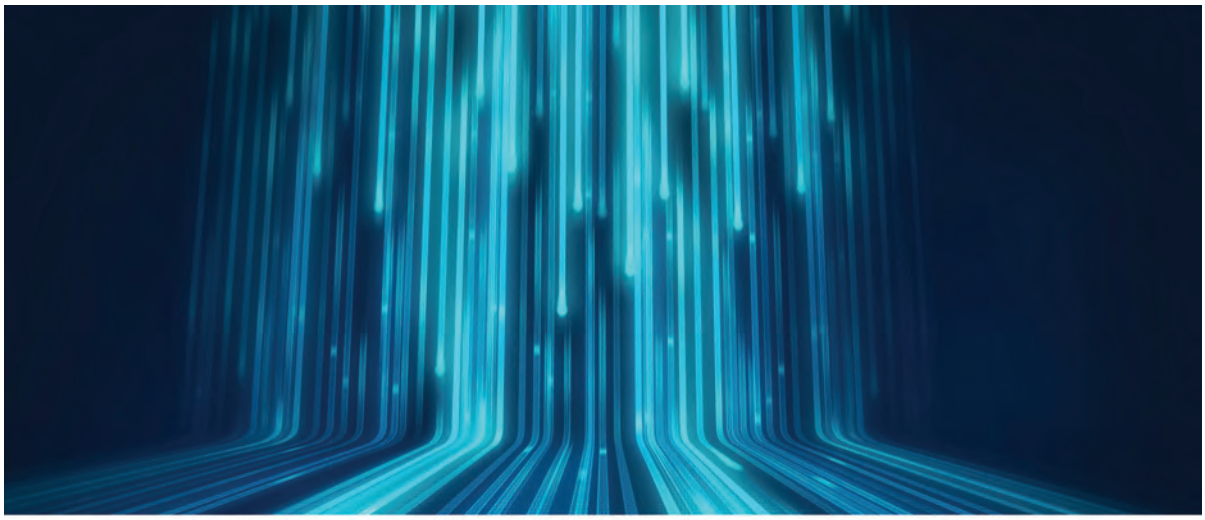
Development

3years

Verification

Innovative Architecture
Technology-powered Flash Memory Innovation

YMTC EXHIBIT 1021
Page 614 of 629



Celerity

Xtacking® enables DRAM-like high I/O speed

With Xtacking® , the periphery circuits as well as memory cell array are processed on two separate wafers using the logic technology node that enables the desired I/O speed and functions. Once the processing of the array wafer is completed, the two wafers are connected electrically through billions of metal VIAs (Vertical Interconnect Accesses) that are formed simultaneously across the whole wafer in one process step.



Scalability

Xtacking® enables smaller die size and higher bit density

In the conventional 3D NAND architecture, the periphery circuits take up ~20-30% of the die area, lowering NAND bit density. As 3D NAND technology continues to progress to 128 layers and above, the periphery circuits will likely take up more than 50% of the total die area. With Xtacking®, the periphery circuits are now above the array chip, enabling much higher NAND bit density than conventional 3D NAND.



Flexibility

Xtacking® : Modular approach to accelerate Time-to-Market

Xtacking® utilizes fully independent processing of the array and periphery, which offers a modularized, parallel approach to product development and manufacturing, reducing product development time by at least three months and shortening manufacturing cycle time by 20%, significantly accelerating 3D NAND time-to-market. This modular approach also opens possibilities for customized NAND flash solutions by the incorporation of innovative functionalities in the periphery.
Award-winning Xtacking®

YMTC Xtacking® technology
has won many awards in industry events around the world



In August 2018, YMTC officially launched its ground-breaking Xtacking® architecture at the Flash Memory Summit, and won the “Best of Show” award. This award is designed for the startup with the most innovation and entrepreneurship.



On January 2, 2020, YMTC won the“Technology Breakthrough of the Year” award at the 2020 China IC Top Award, jointly organized by China Semiconductor Investment Alliance (CSIA), and jiwei.com, the exclusive media outlet for the semiconductor industry in China. This award is undoubtedly a recognition for YMTC’s innovation and achievements given by the authoritative investment agency and the media outlet of semiconductor integrated circuits in China.

Constant Improvement——Xtacking® 2.0

YMTC 128-layer series applies Xtacking® 2.0 technology to unleash the potential of 3D NAND flash memory

Xtacking® 2.0 will provide more added value for customers with Xtacking® architecture. This includes Higher NAND throughput, better performance at the system level, and a new business model for customized NAND solutions.

Through close cooperation with clients, business partners, and industry organizations, the third-generation NAND solutions powered by Xtacking® 2.0 will be widely used for data centers, enterprise-level servers, PCs, mobile devices, and other fields, which will open a new chapter of customized high-performance NAND solutions.

With ongoing investment in R&D, YMTC is committed to making each generation of products more competitive and better able to satisfy our customers.

The era of 5G, AI, and super data centers require enormous demands of the flash memory market. The mass production of 3D NAND flash memory products based on Xtacking® technology will spur the further development of the global memory market and define the future of 3D flash memory technology.

Exhibit 38

3D NAND Flash Memory-YMTC

ymtc.com/en/buslist.html

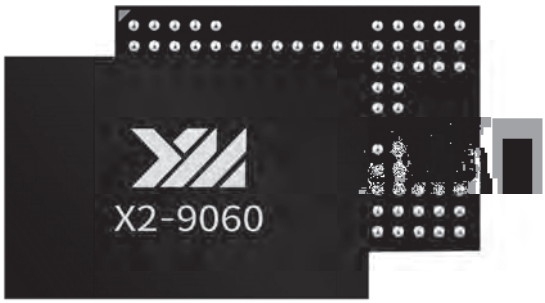
Home / Products /For Enterprises / 3D NAND Flash Memory



X1-9050

Gen 2 TLC 3D NAND Flash Memory

Learn More



X2-9060

Gen 3 TLC 3D NAND Flash Memory

Learn More



X2-6070

Gen 3 QLC 3D NAND Flash Memory

Learn More

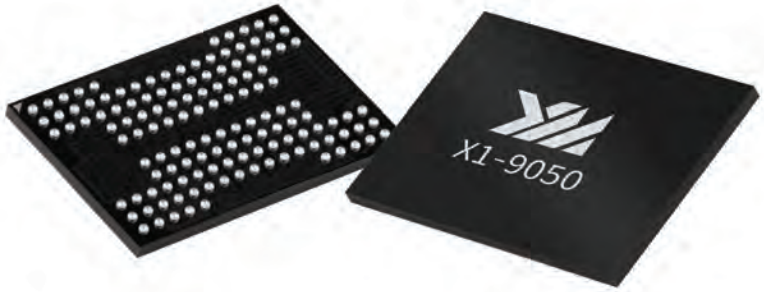
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Filing Number: 鄂ICP 17013673

64层TLC 3D NAND闪存-YMTC-YMTC

ymtc.com/en/products/4.html





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/ 02



YMTC EXHIBIT 1021
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Gen 2 TLC 3D NAND Flash Memory

X1-9050

X1-9050 is the 2nd-generation of YMTC 3D NAND flash memory products. It was put into small-scale mass production in August 2019. It is YMTC's first product designed and processed with the Xtacking® architecture to be put into mass production. Chip capacity is 256GB, and maximum I/O speed can reach 800MT/s.

X1-9050 is supported by mainstream controllers in the industry and can be widely used in the development of consumer, enterprise, and mobile storage products.
Storage Capacity

256Gb

Contact Us Now
Product Details

X1-9050 is the 2nd-generation of YMTC 3D NAND flash memory products. It was put into small-scale mass production in August 2019. It is YMTC's first product designed and processed with the Xtacking®architecture to be put into mass production. The capacity is 256GB, and the maximum I/O speed can reach 800MT/s.

X1-9050 is supported by mainstream controllers in the industry and can be widely used in the development of consumer, enterprise, and mobile storage products.

*Note: Part number, data, performance, specifications, and other information are for reference only. Please refer to the actual product in all cases.

More Materials

Technical Specifications

Part No.	X1-9050
Product Architecture	Xtacking®
Memory Type	TLC
Storage Capacity	256Gb
NAND Flash Memory Interface	ONFI 4.0
Maximum IO speed (MT/s)	800
Bus Width	X8
VCC(V)	2.5/3.3
VCCQ(V)	1.8/1.2
Operating Temperatures (°C)	-20~85

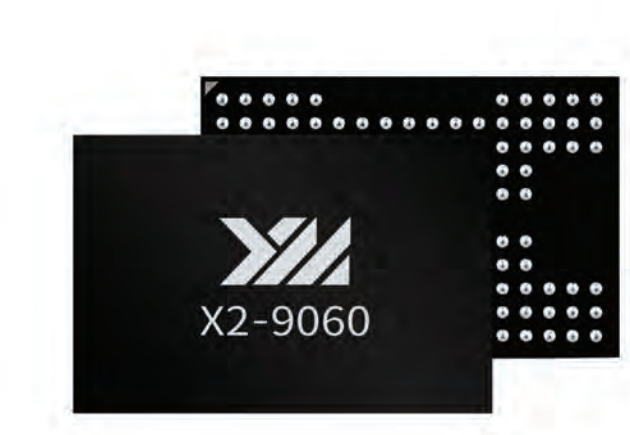
YMTC reserves the right to adjust the above test specifications, and test environment, and update the relevant test results according to the changes in industry development.

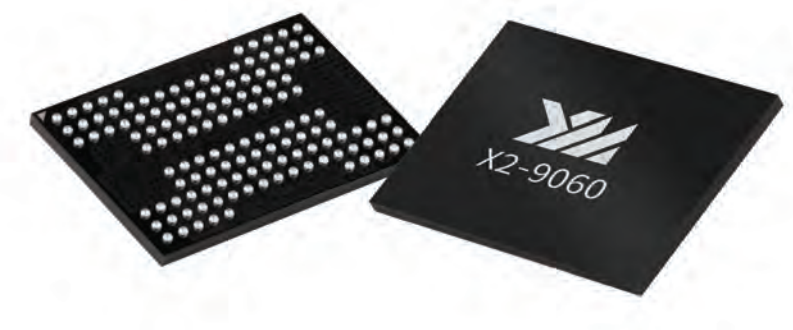
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Filing Number: 鄂ICP 17013673

128层TLC 3D NAND闪存-YMTC-YMTC

ymtc.com/en/products/9.html





01

/ 02



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Gen 3 TLC 3D NAND Flash Memory

X2-9060

X2-9060 is YMTC's 3rd-generation 3D NAND flash memory product developed in the fourth quarter of 2019. It combines high density with fast I/O speed and high-capacity chips.

The YMTC 3rd-generation applies Xtacking® 2.0 technology and unleashes the potential of 3D NAND flash memory. X2-9060 was first applied to consumer SSDs and then extended to enterprise servers, data centers, and other fields to meet the diversified needs for data storage in the era of 5G and AI.
Storage Capacity

512Gb

Contact Us Now
Product Details

X2-9060 is YMTC's 3rd-generation 3D NAND flash memory product developed in the fourth quarter of 2019. It combines high density with fast I/O speed and high-capacity chips.

The YMTC 3rd-generation applies Xtacking®2.0 technology and unleashes the potential of 3D NAND flash memory. X2-9060 was first applied to consumer SSDs and then extended to enterprise servers, data centers, and other fields to meet the diversified needs for data storage in the era of 5G and AI.

*Note: Part number, data, performance, specifications, and other information are for reference only. Please refer to the actual product in all cases.

More Materials

Technical Specifications

Part No.	X2-9060
Product Architecture	Xtacking®
Memory Type	TLC
Storage Capacity	512Gb
NAND Flash Memory Interface	ONFI 4.2
Maximum IO Speed	1.6GT/s

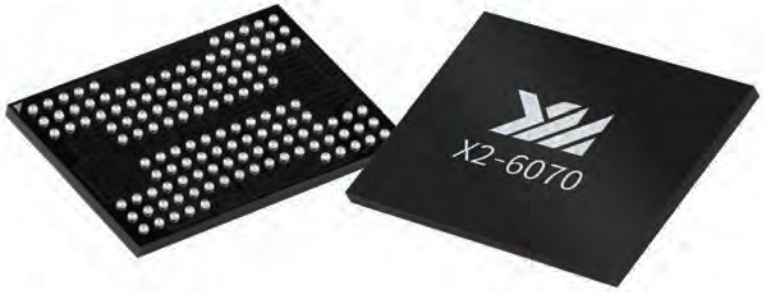
YMTC reserves the right to adjust the above test specifications, and test environment, and update the relevant test results according to the changes in industry development.

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Filing Number: 鄂ICP 17013673

128层QLC 3D NAND闪存-YMTC-YMTC

ymtc.com/en/products/6.html





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/ 02





Gen 3 QLC 3D NAND Flash Memory

X2-6070

X2-6070 is YMTC's 3rd-generation 3D NAND flash memory product developed in April 2020. It combines high density with fast I/O speed and high-capacity chips.

The YMTC 3rd-generation applies Xtacking® 2.0 technology and unleashes the potential of 3D NAND flash memory. X2-6070 was first applied to consumer SSDs and then extended to enterprise servers, data centers, and other fields to meet the diversified needs for data storage in the era of 5G and AI.
Storage Capacity

1.33Tb

Contact Us Now
Product Details

X2-6070 is YMTC's 3rd-generation 3D NAND flash memory product developed in April 2020. It combines high density with fast I/O speed and high-capacity chips.

The YMTC 3rd-generation applies Xtacking®2.0 technology and unleashes the potential of 3D NAND flash memory. X2-6070 was first applied to consumer SSDs and then extended to enterprise servers, data centers, and other fields to meet the diversified needs for data storage in the era of 5G and AI.

*Note: Part number, data, performance, specifications, and other information are for reference only. Please refer to the actual product in all cases.

More Materials

Technical Specifications

Part No.	X2-6070
Product Architecture	Xtacking®
Memory Type	QLC
Storage Capacity	1.33Tb
NAND Flash Memory Interface	ONFI 4.2
Maximum IO Speed (MT/s)	1.6GT/s

YMTC reserves the right to adjust the above test specifications, and test environment, and update the relevant test results according to the changes in industry development.

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Filing Number: 鄂ICP 17013673