



January 9, 2025

Certification

Welocalize Translations

TRANSLATOR'S DECLARATION:

I, Youngjo Yoo, hereby declare:

That I possess advanced knowledge of the Korean and English languages. The attached Korean into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of:
Korean Patent Application No. 10-2014-0176089

A handwritten signature in black ink, appearing to read "Youngjo Yoo".

Youngjo Yoo

BAYE_2412_P0001



This is to certify that the following application annexed hereto is a true copy from the records of the Korean Intellectual Property Office

Application Number: 10-2014-0176089

Filing Date: DEC. 09, 2014

Applicant(s) : SAMSUNG ELECTRONICS CO., LTD

February 9, 2016

Commissioner of the Patent Office

[Bibliographic Data]**[Document Name]** Patent application form**[Application Type]** Patent Application**[Applicant]****[Name]** Samsung Electronics Co., Ltd.**[Applicant Code]** 1-1998-104271-3**[Agent]****[Name]** Sangsoo Park**[Agent Code]** 9-1998-000642-5**[Registration of General Power of Attorney Number]** 2000-054081-9**[Korean Title of Invention]** 반도체 소자**[English Title of Invention]** Semiconductor device**[Inventor]****[Name]** LIM, JOON SUNG**[English spelling of name]** LIM, JOON SUNG**[Resident Registration Number]** 780528-1XXXXXX**[ZIP Code]** 448-150**[Address]** 9, 12beon-gil, Sinbong 3-ro, Suji-gu, Yongin-si, Gyeonggi-do, 411-dong, 1701-ho (Sinbong-dong, Dongil Highville 4th Apartment)**[Nationality]** KR**[Inventor]****[Name]** YUN, JANG GN**[English Spelling of Name]** YUN, JANG GN**[Resident Registration Number]** 800121-1XXXXXX**[ZIP Code]** 445-988**[Address]** 35, Byeongjeom 2-ro, Hwaseong-si, Gyeonggi-do, 101-dong, 603-ho (Byeongjeom-dong, Jugong 1st complex apartment)**[Nationality]** KR**[Inventor]**

[Name] YUN, JAE SUN
[English Spelling of Name] YUN, JAE SUN
[Resident Registration Number] 710704-1XXXXXX
[ZIP Code] 431-793
[Address] 28, Pyeongchon-daero 180beongil, Dongan-gu, Anyang-si,
Gyeonggi-do, 306-dong, 601-ho (Pyeongchon-dong, Hyangchon
Lotte Apartment)
[Nationality] KR
[Plaintiff's Demand] I hereby submit to the Commissioner of the Patent Office as above.

Agent Park Sang-soo (signature or seal)

[Fee]

[Application Fee]	0 pages	46,000 won
[Additional Application Fee]	129 pages	0 won
[Claim of Priority Fee]	0 cases	0 won
[Request for Examination Fee]	0 claims	0 won
[Total]	46,000 won	

[Specification]

TITEL OF THE INVENTION

Semiconductor device

TECHNICAL FIELD

<1> The technical idea of the present invention relates to a semiconductor device, a method for manufacturing a semiconductor device, and an electronic system adopting the same.

BACKGROUND

<2> In semiconductor devices such as flash memory, a degree of integration is one of the important factors that can determine the price of semiconductor products. In general, for two-dimensional semiconductor devices containing two-dimensionally arranged memory cells, systems of a super-high price for the refinement of patterns are required in order to increase the degree of integration. Therefore, there is a limit to increasing the degree of integration of semiconductor devices containing two-dimensionally arranged memory cells. To overcome the limitations of increasing the degree of integration of these two-dimensional semiconductor devices, three-dimensional semiconductor devices including three-dimensionally arranged memory cells have been proposed.

SUMMARY OF THE INVENTION

Problems to be Solved

<3> A problem to be solved by the technical idea of the present invention is to provide a semiconductor device capable of increasing the degree of integration.

<4> A problem to be solved by the technical idea of the present invention is to

provide a semiconductor device including a peripheral circuit area and a cell array area disposed on the peripheral circuit area.

<5> A problem to be solved by the technical idea of the present invention is to provide a semiconductor device including a contact structure that electrically connects the peripheral circuit region and the cell array area arranged perpendicular to the semiconductor substrate.

<6> A problem to be solved by the technical idea of the present invention is to provide a method for forming the semiconductor device.

<7> A problem to be solved by the technical idea of the present invention is to provide an electronic device and electronic system having the semiconductor device.

<8> The problems to be solved by the present invention are not limited to the problems mentioned above, and other problems not mentioned will be clearly understood by those skilled in the art from the description below.

Means for Solving the Problems

<9> A semiconductor device according to one aspect of the technical idea of the present invention is provided. The semiconductor device includes a semiconductor pattern, which is disposed on a semiconductor substrate and has an opening. The semiconductor pattern includes a first impurity region having a first conductivity type and a second impurity region having a second conductivity type different from the first conductivity type. A peripheral transistor is disposed between the semiconductor substrate and the semiconductor pattern. A first peripheral interconnection structure is disposed between the semiconductor substrate and the semiconductor pattern.

The first peripheral interconnection structure is electrically connected to the peripheral transistor. Cell gate conductive patterns are disposed on the semiconductor pattern. Cell vertical structures are disposed to pass through the cell gate conductive patterns and to be connected to the semiconductor pattern. Cell bit line contact plugs are disposed on the cell vertical structures. A bit line is disposed on the cell bit line contact plugs. A peripheral bit line contact structure is disposed between the bit line and the first peripheral interconnection structure. The peripheral bit line contact structure crosses the opening of the semiconductor pattern.

<10> A semiconductor device according to one aspect of the technical idea of the present invention is provided. The semiconductor device includes a semiconductor pattern, which is disposed on a semiconductor substrate and has an opening. A first peripheral interconnection structure having a first peripheral contact pad is disposed between the semiconductor substrate and the semiconductor pattern. A second peripheral interconnection structure is disposed to be disposed between the semiconductor substrate and the semiconductor pattern, to extend in an outside direction of the semiconductor pattern, and to have a second peripheral contact pad. A cell array area is disposed on the semiconductor pattern. A first step area is disposed on a side of the cell array area on the semiconductor pattern. A cell gate conductive pattern is disposed on the semiconductor pattern. The cell gate conductive pattern is disposed in the cell array area and extends to the first step area. A cell vertical structure is disposed to pass through the cell gate conductive pattern in the cell array area and to be connected to the semiconductor pattern. A bit line is disposed on the cell vertical structure. A peripheral bit line contact structure

is disposed between the bit line and the first peripheral contact pad. The peripheral bit line contact structure crosses the opening of the semiconductor pattern. A cell gate contact structure is disposed on the cell gate conductive pattern of the step area on the semiconductor pattern. A peripheral word line contact structure is disposed on the second peripheral contact pad. The peripheral word line contact structure is disposed on an outside of the semiconductor pattern. A word line interconnection structure is disposed to electrically connect the cell gate contact structure to the peripheral word line contact structure.

<11> A semiconductor device according to one aspect of the technical idea of the present invention is provided. The semiconductor device includes a semiconductor pattern disposed on a semiconductor substrate. A peripheral transistor is disposed between the semiconductor substrate and the semiconductor pattern. A peripheral interconnection structure is disposed between the semiconductor substrate and the semiconductor pattern. The peripheral interconnection structure is electrically connected to the peripheral transistor and has a peripheral contact pad. A gate conductive structure is disposed on the semiconductor pattern. The gate conductive structure includes a plurality of cell gate conductive patterns stacked in a direction perpendicular to the semiconductor pattern. A cell vertical structure is disposed to pass through the gate conductive structure. A cell conductive line is disposed on the cell vertical structure. The cell conductive line has a length smaller than a width of the semiconductor pattern. A peripheral contact structure is disposed between the cell conductive line and the peripheral contact pad.

<12> A semiconductor device according to one aspect of the technical idea of the

present invention is provided. The semiconductor device includes a peripheral transistor disposed on a semiconductor substrate. A peripheral interconnection structure is disposed on the semiconductor substrate to be electrically connected to the peripheral transistor. The peripheral interconnection structure has a peripheral contact pad. A lower interlayer insulating layer is disposed on the semiconductor substrate to cover the peripheral transistor and the peripheral interconnection structure. A buffer insulating layer is disposed on the lower interlayer insulating layer. A semiconductor pattern is disposed on the buffer insulating layer. The semiconductor pattern overlaps the peripheral transistor and the peripheral interconnection structure. A first gate conductive structure, a second gate conductive structure, and a third gate conductive structure are disposed on the semiconductor pattern to be sequentially arranged in a horizontal direction. Each of the first to third gate conductive structures includes a plurality of cell gate conductive patterns stacked in a direction perpendicular to the semiconductor pattern. Cell vertical structures are disposed to pass through the first to third gate conductive structures. Cell bit line contact plugs are disposed on the cell vertical structures. A bit line is disposed on the cell bit line contact plugs. A peripheral bit line contact structure is disposed between the bit line and the peripheral contact pad to pass through the semiconductor pattern.

<13> Specific details of other embodiments are included in the detailed descriptions and drawings.

EFFECT OF THE INVENTION

<14> According to embodiments of the technical idea of the present invention, a

three-dimensional semiconductor device capable of improving a degree of integration can be provided.

<15> According to embodiments of the technical idea of the present invention, the peripheral circuit area and the memory cell array area are arranged vertically, and a structure for electrically connecting a bit line of the memory cell array area and the peripheral circuit area is disposed to vertically penetrate the memory cell array area or to be disposed at a position close to the memory cell array area, thereby improving the degree of integration.

[BRIEF DESCRIPTION OF THE DRAWINGS]

<16> FIG. 1 is a conceptual view showing a semiconductor device according to embodiments of the technical idea of the present invention.

FIGS. 2A and 2B are plan views showing the semiconductor devices according to embodiments of the technical idea of the present invention.

FIGS. 3A and 3B are cross-sectional views showing the semiconductor devices according to embodiments of the technical idea of the present invention, and FIG. 3C is an enlarged partial view of part "A" of FIG. 3A.

FIGS. 4A and 4B are cross-sectional views showing semiconductor devices according to embodiments of the technical idea of the present invention.

FIGS. 5A and 5B are plan views showing the semiconductor devices according to embodiments of the technical idea of the present invention.

Each of FIGS. 6 to 10 is a plan view showing a semiconductor device according to one embodiment of the technical idea of the present invention.

FIGS. 11A and 11B are cross-sectional views showing semiconductor devices

according to embodiments of the technical idea of the present invention.

Figure 12 is a conceptual view showing a semiconductor device according to embodiments of the technical idea of the present invention.

FIGS. 13A and 13B are plan views showing semiconductor devices according to one embodiment of the technical idea of the present invention.

FIG. 14 is a cross-sectional view showing a semiconductor device according to one embodiment of the technical idea of the present invention.

FIG. 15 is a cross-sectional view showing a semiconductor device according to embodiments of the technical idea of the present invention.

FIG. 16 is a cross-sectional view showing a semiconductor device according to embodiments of the technical idea of the present invention.

FIG. 17 is a cross-sectional view showing a semiconductor device according to embodiments of the technical idea of the present invention.

FIG. 18 is a cross-sectional view showing a semiconductor device according to embodiments of the technical idea of the present invention.

FIG. 19 is a flowchart showing a method for forming a semiconductor device according to embodiments of the technical idea of the present invention.

FIGS. 20A to 26B are cross-sectional views showing a method for forming a semiconductor device according to embodiments of the technical idea of the present invention.

FIG. 27 is a cross-sectional view showing a semiconductor device according to one embodiment of the technical idea of the present invention.

FIG. 28 is a cross-sectional view showing a semiconductor device according to

one embodiment of the technical idea of the present invention.

FIG. 29 is a flowchart showing a method for forming a semiconductor device according to one embodiment of the technical idea of the present invention.

Each of FIGS. 30A to 32B is a cross-sectional view showing a method for forming a semiconductor device according to one embodiment of the technical idea of the present invention.

Each of FIGS. 33 to 35 is a cross-sectional view showing a method for forming a semiconductor device according to one embodiment of the technical idea of the present invention.

Each of FIGS. 36 to 37 is a cross-sectional view showing a method for forming a semiconductor device according to one embodiment of the technical idea of the present invention.

FIG. 38 is a schematic drawing of a semiconductor module according to embodiments of the technical idea of the present invention.

FIG. 39 is a conceptual block diagram showing an electronic system according to an embodiment of the technical idea of the present invention.

FIG. 40 is a schematic block diagram showing an electronic system (500) according to an embodiment of the technical idea of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

<17> The advantages and features of the present invention and the method for achieving them will become clear with reference to the embodiments described in detail below together with the attached drawings. However, the present invention is not limited to the embodiments set forth herein, but may be embodied in various

different forms, and these embodiments are provided so that this disclosure is thorough and complete and fully conveys the inventive concept to those skilled in the art. The present invention is defined only by the scope of the claims. In the drawings, the sizes and relative sizes of layers and regions may be exaggerated for clarity. The same reference symbols denote the same components throughout the specification.

<18> Embodiments are described herein with reference to cross-sectional views, plan views, and/or block diagrams that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. Therefore, regions illustrated in the drawings are schematic in nature, and their shapes are not intended to limit the inventive concept but only to illustrate characteristic forms of regions of devices.

<19> The thicknesses of layers and regions in the drawings may be exaggerated for the sake of clarity. Further, it will be understood that when a layer is referred to as being “on” another layer or a substrate, the layer may be formed directly on the other layer or the substrate, or there may be an intervening layer therebetween. The same reference numerals indicate the same components throughout the specification.

<20> Terms such as top, bottom, upper, lower, above, below, and the like are used herein to describe the relative positions of elements or features. For example, when an upper part of a drawing is referred to as a top and a lower part of a drawing as a

bottom for the sake of convenience, in practice, the top may also be called a bottom and the bottom a top without departing from the teachings of the inventive concept.

<21> Furthermore, throughout this disclosure, directional terms such as “upper,” “intermediate,” “lower,” and the like may be used herein to describe the relationship of one element or feature with another, and the inventive concept should not be limited by these terms. Accordingly, these terms such as “upper,” “intermediate,” “lower,” and the like may be replaced by other terms such as “first,” “second,” “third,” and the like to describe the elements and features.

<22> It will be understood that, although the terms “first,” “second,” etc. may be used herein to describe various elements, these elements should not be limited by these terms. The above terms are used solely to distinguish one element from another. For example, “a first element” could be termed “a second element” without departing from the teachings of the present inventive concept.

<23> The terms used herein are only used to describe specific embodiments and are not intended to limit the technical spirit of the present invention.

<24> Singular expressions include plural expressions unless the context clearly indicates otherwise. It will be further understood that the terms “include” or “have,” when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

<25> Unless otherwise defined, all terms used herein, including technical or scientific terms, have the same meaning as commonly understood by one of ordinary skill in

the art to which the present invention pertains. Terms defined in commonly used dictionaries should be interpreted as having a meaning consistent with their meaning in the context of the relevant technology, and will not be interpreted in an idealized or overly formal sense unless expressly defined in this application.

<26> Figure 1 is a schematic conceptual diagram for explaining a semiconductor device according to one embodiment of the technical idea of the present invention. FIGS. 2A and 2B are plan views showing the semiconductor devices according to embodiments of the technical idea of the present invention. In FIGS. 2A and 2B, FIG. 2B is a plan view in which interconnection structures are added to the drawing of FIG. 2A to avoid complexity of the drawing. FIG. 3A is a cross-sectional view showing areas taken along lines I-I' and II-II' of Fig. 2A, respectively, and Fig. 3B is a cross-sectional view showing areas taken along lines III-III' and IV-IV' of Fig. 2B, respectively. Figure 3C is an enlarged view of part "A" of Figure 3A.

<27> First, a semiconductor device according to one embodiment of the technical idea of the present invention will be described with reference to FIGS. 1, 2A, 2B, 3A, 3B, and 3C.

<28> Referring to FIG. 1, FIG. 2a, FIG. 2b, FIG. 3a, FIG. 3b and FIG. 3c, a peripheral circuit area can be disposed on a semiconductor substrate (2). The semiconductor substrate (2) can be formed of a semiconductor material such as silicon. The peripheral circuit region may include a first peripheral circuit region (PC1), a second peripheral circuit region (PC2), and a third peripheral circuit region (PC3). The first peripheral circuit area (PC1) may include a page buffer circuit. The first peripheral circuit region (PC1) may include a peripheral transistor (PTR) that may configure a

circuit and a first peripheral interconnection structure (PW1) which is electrically connected to the peripheral transistor (PTR). The first peripheral interconnection structure (PW) may include a first peripheral contact pad part (PP1).

<29> The peripheral transistor (PTR) may include a peripheral gate (PG) and peripheral impurity regions (PS, PD). The peripheral gate (PG) may be disposed in an active region defined by an isolation area (3). The peripheral impurity regions (PS and PD) may be disposed in the active region of both sides of the peripheral gate (PG) and may serve as a source/drain.

<30> A lower interlayer insulating layer (LILD) may be disposed to cover the first to third peripheral circuit areas (PC1, PC2, PC3) of the semiconductor substrate (2). The lower interlayer insulating layer (LILD) can be formed of an insulating material including silicon oxide. The first peripheral interconnection structure (PW) and the first peripheral contact pad part (PP1) of the first peripheral interconnection structure (PW) can be covered by the lower interlayer insulating layer (LILD).

<31> A buffer insulating layer (10) can be disposed on the peripheral lower interlayer insulating layer (LILD). The buffer insulating layer (10) may have an etch selectivity different from a part of the lower interlayer insulating layer (LILD) that is in contact with the buffer insulating layer (10). For example, the buffer insulating layer (10) may be formed of silicon nitride, and the part of the lower interlayer insulating layer (LILD) in contact with the buffer insulating layer (10) may be formed of silicon oxide.

<32> A semiconductor pattern (14) having an opening (16) can be disposed on the buffer insulating layer (10). The semiconductor pattern (14) may overlap with the first peripheral circuit area (PC1), the second peripheral circuit area (PC2), and/or

the third peripheral circuit area (PC3). The semiconductor pattern (14) may include a first impurity region (LC) of a first conductivity type, a second impurity region (42) having a conductivity type different from the first conductivity type, a body contact impurity region (50) of the first conductivity type and having a higher impurity concentration than the first impurity region (LC), and a third impurity region (HC) of the first conductivity type and having a higher impurity concentration than the first impurity region (LC) and disposed under the first impurity region (LC). The first impurity region (LC) may be referred to as a low concentration impurity region, the second impurity region (42) may be referred to as a cell source impurity region, and the third impurity region (HC) may be referred to as a high concentration impurity region.

<33> In one embodiment, the first impurity region (LC), the third impurity region (HC), and the cell body contact impurity region (50) may be of P-type conductivity, and the second impurity region (42) may be of N-type conductivity.

<34> The peripheral transistor (PTR) and the first peripheral interconnection structure (PW1) can be interposed between the semiconductor substrate (2) and the semiconductor pattern (14).

<35> A second peripheral interconnection structure (PW2 of FIG. 1) and a third peripheral interconnection structure (PW3 of FIG. 3B) may be disposed to be interposed between the semiconductor substrate (2) and the semiconductor pattern (14) and to extend in the outside direction of the semiconductor pattern (14).

<36> The second peripheral interconnection structure (PW2 in FIG. 1) may have a second peripheral contact pad (PP2) in a part that does not overlap with the

semiconductor pattern (14). The third peripheral interconnection structure (PW3 in FIG. 3B) may have a third peripheral contact pad (PP3) in a part that does not overlap with the semiconductor pattern (14). The first peripheral contact pad (PP1) of the first peripheral interconnection structure (PW1) may be located between the semiconductor substrate (2) and the semiconductor pattern (14).

<37> An gap fill insulating layer (18) may be disposed within the opening (16) of the semiconductor pattern (14). An intermediate interlayer insulating layer (19) may be disposed on the side surface of the semiconductor pattern (14). The gap fill insulating layer (18) and the intermediate interlayer insulating layer (19) can be formed of silicon oxide.

<38> A cell array area (CA) and step areas (ST1, ST2, ST3, ST4) can be disposed on the semiconductor pattern (14). The step areas (ST1, ST2, ST3, ST4) may include first and third step areas (ST1, ST3) facing each other in which the cell array area (CA) is interposed therebetween, and second and fourth step areas (ST2, ST4) facing each other in which the cell array area (CA) is interposed therebetween.

<39> Cell gate conductive structures (GS1, GS2, GS3) can be disposed on the semiconductor substrate (14). The cell gate conductive structures (GS1, GS2, GS3) can be disposed within the cell array area (CA). The cell gate conductive structures (GS1, GS2, GS3) can extend from the cell array area (CA) into the first and third step areas (ST1, ST3).

<40> The cell gate conductive structures (GS1, GS2, GS3) may include a first gate conductive structure (GS1), a second gate conductive structure (GS2), and a third gate conductive structure (GS3). The separation distance between the first and

second gate conductive structures (GS1, GS2) may be greater than the separation distance between the second and third gate conductive structures (GS2, GS3).

<41> Each of the first, second and third gate conductive structures (GS1, GS2, GS3) may be sequentially stacked on the semiconductor pattern (14) and include cell gate conductive patterns (38a) spaced apart from each other. The cell gate conductive patterns (38a) can be disposed so as to have a step structure in the first step area (ST1) and the second step area (ST2) of the semiconductor pattern (14). The step structure may be gradually lowered as further away from the cell array area (CA).

<42> Cell interlayer insulating patterns (21) may be interposed between the cell gate conductive patterns (38a) and between a lowermost pattern of the cell gate conductive patterns (38a) and the semiconductor pattern (14). The cell interlayer insulating patterns (21) and the cell gate conductive patterns (38a) can be alternately and repeatedly stacked.

<43> An insulating structure (23) may be disposed on the semiconductor pattern (14) between the first and second gate conductive structures (GS1, GS2).

<44> The insulating structure (23) may include a first insulating pattern (20a) and a second insulating pattern (22b) that are alternately and repeatedly stacked. Accordingly, the insulating structure (23) may include a plurality of first insulating patterns (20a) and a plurality of second insulating patterns (22a).

<45> The first insulating pattern (20a) may have a width greater than that of the second insulating pattern (22a) and may have an etch selectivity with respect to the second insulating pattern (22a). For example, the first insulating pattern (20a) may be formed of silicon oxide, and the second insulating pattern (22a) may be formed

of silicon nitride.

<46> Dummy gate conductive patterns (38b) may be disposed in the horizontal direction of the second insulating pattern (22a) on the semiconductor pattern (14) between the first and second gate conductive structures (GS1, GS2). The second insulating patterns (22a) can be disposed on the same plane as the cell gate conductive patterns (38a).

<47> The insulating structure (23) can overlap with the opening (16). The insulating structure (23) can overlap with the gap fill insulating layer (18) within the opening (16).

<48> A third insulating pattern (20b) and a fourth insulating pattern (22b) may be alternately and repeatedly stacked on the second and fourth step areas (ST2, ST4) on the semiconductor pattern (14) and formed to have a step structure. The step structure may be gradually lowered in a direction further away from the cell array area (CA). The third insulating patterns (20b), the first insulating patterns (20a) and the cell interlayer insulating patterns (21) may be formed of the same material and disposed on the same plane. The fourth insulating patterns (22b) and the second insulating patterns (22a) can be formed of the same material and disposed on the same plane. The second insulating patterns (22a) and the fourth insulating patterns (22b) can be disposed on the same plane as the cell gate conductive patterns (38a).

<49> A first upper interlayer insulating layer (24) may be disposed on a substrate having the cell gate conductive structures (GS1, GS2, GS3), the insulating structure (23), and the second and fourth insulating patterns (22a, 22b).

<50> Cell vertical structures (CV) can be disposed within the cell array area (CA) on the semiconductor pattern (14). The cell vertical structures (CV) can be disposed on

the first impurity region (LC) of the semiconductor pattern (14). The cell vertical structures (CV) may pass through the first upper interlayer insulating layer (24), the cell gate conductive patterns (38a) and the cell interlayer insulating patterns (21) and may be connected to the first impurity region (LC) of the semiconductor pattern (14).

<51> Each of the cell vertical structures (CV) may include a first dielectric (27), a cell semiconductor layer (28), a core insulating pattern (29), and a cell pad pattern (30). The cell pad pattern (30) can be disposed on the core insulating pattern (29). The cell pad pattern (30) can be formed of doped silicon. The cell pad pattern (30) may have N-type conductivity.

<52> The cell semiconductor layer (28) can be disposed so as to surround the side and bottom of the core insulating pattern (29). The cell semiconductor layer (28) may be formed of a material that can be used as a channel of a transistor, for example, silicon. The first dielectric (27) can be disposed on the outer side of the cell semiconductor layer (28). The cell semiconductor layer (28) can be interposed between the first dielectric (27) and the core insulating pattern (29).

<53> A second dielectric (37) may be interposed between the cell vertical structures (CV) and the cell gate conductive patterns (38a).

<54> Either of the first and second dielectrics (27, 37) may include a data storage layer capable of storing data. For example, the first dielectric layer (27) may include a tunnel dielectric layer and a data storage layer formed sequentially from the cell semiconductor layer (28). The second dielectric (37) may include a blocking dielectric. The first and second dielectrics (27, 37) may have the same structure as

a dielectric between a control gate of a NAND flash memory device and a body of a cell transistor of the NAND flash memory device. However, the technical idea of the present invention is not limited to a structure of the NAND flash memory device and can be used in various memory devices.

<55> A second upper interlayer insulating layer (32) can be disposed on the first upper interlayer insulating layer (24).

<56> A plurality of cell source patterns (46) may be disposed on the semiconductor pattern (14) to cross the cell array area (CA) and extend into the first and third step areas (ST1, ST3). The cell source patterns (46) can be disposed on the second impurity regions, i.e., the cell source impurity regions (46). The cell source patterns (46) may include a conductive material. The cell source patterns (46) may overlap with and be electrically connected to the second impurity regions (46). The cell source patterns (46) may have a line shape extending in the first direction (X). The cell source patterns (46) are arranged sequentially in a second direction (Y) perpendicular to the first direction (X) and may be parallel to each other.

<57> The cell source patterns (46) may pass through the first and second upper interlayer insulating layers (24, 32) and vertically cross the cell gate conductive patterns (38a) and be connected to the second impurity regions (42) of the semiconductor pattern (14).

<58> The cell source patterns (46) may include first to third source patterns (46a, 46b, 46c) arranged sequentially and spaced apart from each other at different intervals. For example, a distance between the adjacent first and second source patterns (46a, 46b) may be greater than a distance between the adjacent second

and third source patterns (46b, 46c).

<59> Among the source patterns (46), the cell gate conductive patterns (38a) may be disposed between source patterns arranged at relatively narrow intervals, for example, the second and third source patterns (46b, 46c). Among the source patterns (46), the cell gate conductive patterns (38a) may not be disposed between source patterns arranged at relatively wide intervals, for example, the first and second source patterns (46b, 46c), and the insulating structure (23) and the dummy gate conductive patterns (38b) may be disposed therebetween.

<60> A third upper interlayer insulating layer (48) may be disposed on the second upper interlayer insulating layer (32) and the cell source patterns (46). A fourth upper interlayer insulating layer (60) may be disposed on the third upper interlayer insulating layer (48).

<61> A bit line contact structure (72) electrically connected to the peripheral transistor (PTR) under the semiconductor pattern (14) may be disposed. The bit line contact structure (72) may be electrically connected to the first peripheral contact pad (PP1) of the first peripheral circuit area (PC1) below the cell array area (CA) while vertically pass through the cell array area (CA).

<62> The bit line peripheral contact structure (72) may include a bit line lower contact plug (52) and a bit line upper contact plug (62) on the bit line lower contact plug (52). The bit line lower contact plug (52) pass through a part of the peripheral lower interlayer insulating layer (LILD) covering the first to third upper interlayer insulating layers (24, 32, 48), the insulating structure (23), the gap fill insulating layer (18) and the first peripheral contact pad (PP1), and can be electrically connected to the first

peripheral contact pad (PP1) of the first peripheral interconnection structure (PW1) that is electrically connected to the peripheral transistor (PTR). The upper contact plug (62) around the bit line can penetrate the fourth upper interlayer insulating layer (60) and be electrically connected to the lower contact plug (52) around the bit line.

<63> In one embodiment, as in FIG. 3C, the bit line lower contact plug (52 in FIG. 3C) may include a plug metal layer (52B) and a barrier metal layer (52a) on a side surface of the plug metal layer (52b). For example, the plug metal layer (52b) may include a metal material, and the barrier metal layer (52a) may include a metal nitride.

<64> In one embodiment, as in FIG. 3C, an oxide spacer (SP) may be disposed between the bit line lower contact plug (52 in FIG. 3C) and the contact hole (H). The oxide spacer (SP) can be formed of silicon oxide.

<65> Cell bit line plugs (68) electrically connected to the cell vertical structures (CV) can be disposed. The cell bit line plugs (68) can pass through the first to fourth interlayer insulating layers (24, 32, 48, 60).

<66> Cell gate contact structures (74) electrically connected to the cell gate conductive patterns (38a) can be disposed. The cell gate contact structures (74) can be disposed within the first step area (ST1).

<67> Each of the cell gate contact structures (74) may include a cell gate lower contact plug (54) and a cell gate upper contact plug (64) on the cell gate lower contact plug (54).

<68> The cell gate lower contact plug (54) can be electrically connected to the cell gate conductive patterns (38a) while pass through the first, second and third upper interlayer insulating layers (24, 32, 48). The cell gate upper contact plug (64) can be

electrically connected to the cell gate lower contact plug (54) while pass through the fourth upper interlayer insulating layer (60).

<69> A cell body contact structure (73) electrically connected to the cell body contact impurity region (50) can be disposed. The cell body contact structure (73) may include a cell body lower contact plug (53) and a cell body upper contact plug (63) on the cell body lower contact plug (53).

<70> The cell body lower contact plug (53) may pass through the first to third upper interlayer insulating layers (24, 32, 48) and the third and fourth insulating patterns (20b, 22b) within the step areas positioned in the second direction (Y) perpendicular to the cell source patterns (46) and be connected to the semiconductor pattern (14). The cell body lower contact plug (53) and the peripheral bit line lower contact plug (52) may have lower surfaces which are located on different planes and upper surfaces located on the same plane. The cell body upper contact plug (63) can be electrically connected to the cell body lower contact plug (53) while passing through the fourth upper interlayer insulating layer (60).

<71> A peripheral body contact structure (75) may be disposed between the semiconductor substrate (2) and the semiconductor pattern (14) and electrically connected to a third peripheral contact pad (PP3) of a third peripheral interconnection structure (PW3) extending in the outside direction of the semiconductor pattern (14). The cell body contact structure (73) may be disposed on the semiconductor pattern (14) and overlap with it, and the peripheral body contact structure (74) may not overlap with the semiconductor pattern (14). The peripheral body contact structure (75) can be disposed on the outside of the

semiconductor pattern (14).

<72> The peripheral body contact structure (75) may include a peripheral body lower contact plug (55) and a peripheral body upper contact plug (65) on the peripheral body lower contact plug (55). The peripheral body lower contact plug (55) can be electrically connected to the third peripheral contact pad (PP3) while passing through the first to third upper interlayer insulating layers (24, 32, 48), the buffer insulating layer (10) and a part of the lower interlayer insulating layer (LILD). The peripheral body upper contact plug (65) can pass through the fourth upper interlayer insulating layer (60).

<73> A interconnection structure can be disposed on the fourth interlayer insulating layer (60). The interconnection structure may include cell conductive lines (80), word line interconnection structures (81), and body interconnection structures (82). The cell conductive lines (80) may be cell bit lines.

<74> The cell conductive lines (80) are disposed on the cell bit line contact plugs (68) and the peripheral bit line contact structures (72) and can be electrically connected to the cell bit line contact plugs (68) and the peripheral bit line contact structures (72). The cell conductive lines (80) may be cell bit lines.

<75> The cell conductive lines, i.e., bit lines (80), may have a length smaller than the width of the semiconductor pattern (14). The cell challenge lines (80) may have a line shape which extends in the second direction (Y). The width of the semiconductor pattern (14) may be the width in the second direction (Y). The cell conductive lines (80) can overlap with the semiconductor pattern (14). The cell conductive lines (80) can be disposed between the side surfaces of the semiconductor pattern (14) while

overlapping the semiconductor pattern (14) in a plan view.

<76> The word line interconnection structures (81) may include a lower word line interconnection (81a), an upper word line interconnection (81b), and a word line interconnection contact plug (81c) between the lower and upper word line interconnections (81a, 81b), as in FIG. 2B. The lower word line interconnection (81a in FIG. 2B) may have a line shape in a direction (Y) perpendicular to the gate structures (GS1, GS2, GS3), and the upper word line interconnection (81b in FIG. 2B) may have a line shape perpendicular to the lower word line interconnection (81a). The upper word line interconnection (81b in FIG. 2b) can extend from the first step area (ST1) toward the outside of the semiconductor pattern (14).

<77> On the outside of the semiconductor pattern (14), a word line peripheral contact structure (77) may be disposed between the word line interconnection structure (81) and the second peripheral contact pad (PP2) of the second peripheral circuit interconnection structure of the second peripheral circuit area (PC).

<78> The body interconnection structures (82) can be electrically connected to the cell body contact structure (73) and the peripheral body contact structure (75).

<79> In one embodiment, the bit line lower contact plug (52) may have an upper surface positioned in the same plane as the upper surface of the body lower contact plug (53).

<80> In one embodiment, the bit line lower contact plug (52) may have an upper surface positioned at a higher level than the cell vertical structures (CV) and the source patterns (46). However, the technical idea of the present invention is not limited thereto.

<81> In one embodiment, as shown in FIGS. 4A and 4B, a bit line lower contact plug (52') and a body lower contact plug (53') having upper surfaces that are positioned at a lower level than the upper surfaces of the source patterns (46) and are positioned in the same plane as the upper surfaces of the cell vertical structures (CV) may be disposed.

<82> In one embodiment, as shown in FIGS. 5A and 5B a bit line lower contact plug (52'') and a body lower contact plug (53'') having upper surfaces positioned at a lower level than the upper surfaces of the cell vertical structures (CV) and the source patterns (46) may be disposed.

<83> The opening (16) of the semiconductor pattern (14) can be formed in a rectangular shape inside the semiconductor pattern (14). However, the technical idea of the present invention is not limited thereto.

<84> In one embodiment, referring to FIG. 6, the semiconductor pattern (14 of FIG. 6) may have an opening (16') shaped to cross the cell array area (CA) and cross one of the step areas (ST3) of the first and third step areas (ST1, ST3).

<85> In one embodiment, referring to FIG. 7, the semiconductor pattern (14 of FIG. 7) may have an opening (16'') shaped to cross the cell array area (CA) and cross both the first and third step areas (ST1, ST3). Therefore, the semiconductor pattern (14 in FIG. 7) may be configured of two patterns spaced apart from each other.

<86> In one embodiment, referring to FIG. 8, the semiconductor pattern (14 of FIG. 8) may have a plurality of openings (16a, 16b) crossing the cell array area (CA).

<87> The cell body lower plug (53) can be formed in a line shape. However, the technical idea of the present invention is not limited thereto. For example, cell body

lower plugs formed in a shape of a plurality of dots (53" in Fig. 9) can be disposed.

<88> A semiconductor device according to one embodiment of the technical idea of the present invention will be described with reference to FIGS. 1, 10, 11A and 11B.

<89> Referring to FIGS. 1, 10, 11a and 11b, the peripheral circuit regions (PC1, PC2, PC3) may be disposed on the semiconductor substrate (2) as described in FIGS. 2A, 2B 3A and 3B, the semiconductor pattern (14) having the opening (16) may be disposed on the peripheral circuit regions (PC1, PC2, PC3), and the cell array area (CA) and the first to fourth step areas (ST1 to ST4) may be disposed on the semiconductor pattern (14).

<90> As described in FIGS. 2A, 2B 3A and 3B, the cell vertical structures (CV), the cell gate conductive patterns (38a) and the source patterns (46) may be disposed on the semiconductor pattern (14), and the cell interlayer insulating patterns (21) may be disposed between the cell gate conductive patterns (38a).

<91> The first to fourth upper interlayer insulating layers (24, 32, 48, 60) as described in FIGS. 2A, 2B 3A, and 3B can be disposed.

<92> Among the source patterns (46), an insulating structure (123) may be disposed between the first and second source patterns (46a, 46b) that are relatively widely spaced apart. The insulating structure (123) can be disposed on the opening (16) of the semiconductor pattern (14). The insulating structure (123) can be formed of silicon oxide.

<93> First insulating patterns (120a) may be disposed on the side surface of the insulating structure (123). The first insulating patterns (120a) may be formed of the same material as the cell interlayer insulating patterns (21), for example, silicon

oxide, while being positioned on the same plane as the cell interlayer insulating patterns (21).

<94> Dummy gate conductive patterns (38b) may be disposed between the first insulating patterns (120a) while being disposed on the side surface of the insulating structure (123). The second dielectric (37) may be disposed between the dummy gate conductive patterns (38b) and the insulating structure (123), and between the dummy gate conductive patterns (38b) and the first insulating patterns (120a). The insulating structure (123) can be disposed in the shape of a structure passing through between the first insulating patterns (120a) and the dummy gate conductive patterns (38b).

<95> As described in FIGS. 2A, 2B, 3A and 3B, a bit line contact structure (72) electrically connected to the peripheral transistor (PTR) under the semiconductor pattern (14), cell bit line plugs (68) electrically connected to the cell vertical structures (CV), cell gate contact structures (74) electrically connected to the cell gate conductive patterns (38a), a cell body contact structure (73) electrically connected to the cell body contact impurity region (50), and a peripheral body contact structure (75) electrically connected to a third peripheral contact pad (PP3) extending from the third peripheral interconnection structure (PW3) under the semiconductor pattern (14) to the outside of the semiconductor pattern (14) can be disposed.

<96> As described in FIGS. 2A, 2B, 3A and 3B, the bit line peripheral contact structure (72) may include a bit line lower contact plug (52) and a bit line upper contact plug (62) on the bit line lower contact plug (52). The bit line lower contact

plug (52) pass through a part of the peripheral lower interlayer insulating layer (LILD) covering the first to third upper interlayer insulating layers (24, 32, 48), the insulating structure (123), the gap fill insulating layer (18) and the first peripheral contact pad (PP1), and can be electrically connected to the first peripheral contact pad (PP1) of the first peripheral interconnection structure (PW1) that is electrically connected to the peripheral transistor (PTR).

<97> As described in FIGS. 2A, 2B, 3A and 3B, the cell conductive lines, i.e., cell bit lines (80), the word line interconnection structures (81) and the body interconnection structures (82) can be disposed.

<98> A semiconductor device according to one embodiment of the technical idea of the present invention will be described with reference to FIGS. 12, 13A, 13B 14A and 14B.

<99> Figure 12 is a schematic conceptual diagram for explaining a semiconductor device according to one embodiment of the technical idea of the present invention. FIGS. 13A and 13B are plan views showing semiconductor devices according to one embodiment of the technical idea of the present invention. In FIGS. 13A and 13B, FIG. 13B is a plan view with interconnection structures added to the drawing of FIG. 13a to avoid complexity of the drawing. The part indicated as III-III' in Fig. 13A may correspond to the part indicated by line III-III' in Fig. 2A. And, the cross-sectional shape of the part indicated as III-III' in Fig. 13A may be substantially the same as the cross-sectional shape of the part indicated as line III-III' in Fig. 3B. Therefore, in order to avoid drawing duplication, the cross-sectional shape of the part indicated by III-III' in Fig. 13A corresponds to the cross-sectional shape of the part indicated

by line III-III' in Fig. 3B, and therefore, in the following drawings and descriptions, the cross-sectional shape of the part indicated by line III-III' in Fig. 3B will be referred to.

<100> Fig. 14 is a cross-sectional view showing areas taken along lines V-V' and VI-VI' of Fig. 13A, respectively.

<101> Referring to FIGS. 12, 13A, 13B and 14, along with the part indicated by line III-III' of FIG. 3B, a peripheral circuit area can be disposed on a semiconductor substrate (2). The peripheral circuit region may include a first peripheral circuit region (PC1), a second peripheral circuit region (PC2), and a third peripheral circuit region (PC3). The first peripheral circuit area (PC1) may include a page buffer circuit. The first peripheral circuit region (PC1) may include a peripheral transistor (PTR) that may constitute a peripheral circuit as described in FIGS. 1, 2A, 2B 3A and 3B, and a first peripheral interconnection structure (PW1) electrically connected to the peripheral transistor (PTR). The first peripheral interconnection structure (PW) may include a first peripheral contact pad part (PP1).

<102> A lower interlayer insulating layer (LILD) may be disposed to cover the first to third peripheral circuit areas (PC1, PC2, PC3) of the semiconductor substrate (2). The lower interlayer insulating layer (LILD) can be formed of an insulating material including silicon oxide. The first peripheral interconnection structure (PW) and the first peripheral contact pad part (PP1) of the first peripheral interconnection structure (PW) can be covered by the lower interlayer insulating layer (LILD).

<103> A buffer insulating layer (10) can be disposed on the peripheral lower interlayer insulating layer (LILD). The buffer insulating layer (10) may have a different etch

selectivity than a part of the lower interlayer insulating layer (LILD) that is in contact with the buffer insulating layer (10).

<104> A semiconductor pattern (214) having an opening (216) can be disposed on the buffer insulating layer (10). The semiconductor pattern (214) can be formed of polysilicon.

<105> The semiconductor pattern (214) may include a first impurity region (LC) of a first conductivity type, a second impurity region (42) having a conductivity type different from the first conductivity type, a body contact impurity region (50) of the first conductivity type and having a higher impurity concentration than the first impurity region (LC), and a third impurity region (HC) of the first conductivity type and having a higher impurity concentration than the first impurity region (LC) and disposed under the first impurity region (LC). The first impurity region (LC) may be referred to as a low-concentration impurity region, the second impurity region (42) may be referred to as a cell source impurity region, and the third impurity region (HC) may be referred to as a high-concentration impurity region. In one embodiment, the first impurity region (LC), the third impurity region (HC), and the cell body contact impurity region (50) may be of P-type conductivity, and the second impurity region (42) may be of N-type conductivity.

<106> An gap fill insulating layer (218) may be disposed within the opening (216) of the semiconductor pattern (214). An intermediate interlayer insulating layer (219) may be disposed on the side of the semiconductor pattern (214). The gap fill insulating layer (218) and the intermediate interlayer insulating layer (219) can be formed of silicon oxide.

<107> A cell array area (CA) and step areas (ST1, ST2, ST3, ST4) can be disposed on the semiconductor pattern (214). The step areas (ST1, ST2, ST3, ST4) may include first and third step areas (ST1, ST3) facing each other in which the cell array area (CA) is interposed therebetween, and second and fourth step areas (ST2, ST4) facing each other in which the cell array area (CA) is interposed therebetween. The first and third step areas (ST1, ST3) can be disposed between the second and fourth step areas (ST2, ST4).

<108> The opening (216) and the gap fill insulating layer (218) of the semiconductor pattern (214) may not overlap with the cell array area (CA). The opening (216) and the gap fill insulating layer (218) of the semiconductor pattern (214) may be positioned in one of the second and fourth step areas (ST2, ST4), for example, under the fourth step area (ST4).

<109> Cell gate conductive structures (GS) can be disposed on the semiconductor pattern (214). The cell gate conductive structures (GS) are disposed within the cell array area (CA) and can extend to the first and third step areas (ST1, ST3). The cell gate conductive structures (GS) can be spaced apart from each other at regular intervals. Each of the cell gate conductive structures (GS) may include cell gate conductive patterns (38a) vertically stacked on the semiconductor pattern (214). The cell gate conductive patterns (38a) can be formed in a step structure within the first and third step areas (ST1, ST3). The cell interlayer insulating patterns (21) can be disposed between the cell gate conductive patterns (38a).

<110> An insulating structure (223) may be disposed in one of the second and fourth step areas (ST2, ST4) on the semiconductor pattern (214), for example, in the fourth

step area.

<111> The insulating structure (223) may include a first insulating pattern (220a) and a second insulating pattern (220b) that are alternately and repeatedly stacked and stacked in a step structure. The step structure may be gradually lowered as further away from the cell array area (CA).

<112> The first insulating patterns (220a) may be formed of the same material as the cell interlayer insulating patterns (21) while being disposed on the same plane. The second insulating patterns (220b) can be disposed on the same plane as the cell gate conductive patterns (38a). The insulating structure (223) can be disposed on the opening (216) of the semiconductor pattern (214).

<113> A first upper interlayer insulating layer (24) may be disposed on a substrate having the cell gate conductive structures (GS), the cell interlayer insulating patterns (21), and the insulating structure (223).

<114> Cell vertical structures (CV) can be disposed within the cell array area (CA) on the semiconductor pattern (214). The cell vertical structures (CV) can be disposed on the first impurity region (LC) of the semiconductor pattern (214). The cell vertical structures (CV) may pass through the first upper interlayer insulating layer (24), the cell gate conductive patterns (38a) and the cell interlayer insulating patterns (21) and may be connected to the first impurity region (LC) of the semiconductor pattern (214).

<115> Each of the cell vertical structures (CV) may include the first dielectric (27), the cell semiconductor layer (28), the core insulating pattern (29), and the cell pad pattern (30) as described in FIG. 2A, FIG. 3A, and FIG. 3B.

- <116> As described in FIGS. 2A, 3A and 3B, a second dielectric (37) may be disposed between the cell vertical structures (CV) and the cell gate conductive patterns (38a), and either of the first and second dielectrics (27, 37) may include a data storage layer capable of storing data.
- <117> A second upper interlayer insulating layer (32) can be disposed on the first upper interlayer insulating layer (24). A plurality of cell source patterns (46) may be disposed on the semiconductor pattern (214) to cross the cell array area (CA) and extend into the first and third step areas (ST1, ST3). The source patterns (46) are disposed on the second impurity regions (46) and can be electrically connected to the second impurity regions (46). The cell source patterns (46) may be parallel to each other. The cell source patterns (46) may penetrate the first and second upper interlayer insulating layers (24, 32) and pass vertically through the cell gate conductive patterns (38a) to be connected to the second impurity regions (42) of the semiconductor pattern (214).
- <118> A third upper interlayer insulating layer (48) may be disposed on the second upper interlayer insulating layer (32) and the cell source patterns (46). A fourth upper interlayer insulating layer (60) may be disposed on the third upper interlayer insulating layer (48).
- <119> A bit line contact structure (272) may be disposed that penetrates the fourth step area (ST4) and the semiconductor substrate (214) below the fourth step area (ST4) and is electrically connected to the peripheral transistor (PTR) below the semiconductor pattern (214).
- <120> The bit line peripheral contact structure (272) may include a bit line lower

contact plug (252) and a bit line upper contact plug (262) on the bit line lower contact plug (252).

<121> The bit line lower contact plug (252) pass through a part of the peripheral lower interlayer insulating layer (LILD) covering the first to third upper interlayer insulating layers (24, 32, 48), the insulating structure (223), the gap fill insulating layer (218) and the first peripheral contact pad (PP1), and can be electrically connected to the first peripheral contact pad (PP1) of the first peripheral interconnection structure (PW1) that is electrically connected to the peripheral transistor (PTR).

The upper contact plug (262) around the bit line can pass through the fourth upper interlayer insulating layer (60) and be electrically connected to the lower contact plug (252) around the bit line.

<122> The cell bit line plugs (68), the cell gate contact structures (74), the cell body contact structure (73) and the peripheral body contact structure (75) as described in FIGS. 2A, 3A and 3B can be disposed.

<123> Cell conductive lines, for example, bit lines (280), may be disposed on the fourth interlayer insulating layer (60). The bit lines (280) can overlap with and be electrically connected to the cell bit line contact plugs (68) and the peripheral bit line contact structures (272). The bit lines (280) can extend from the cell array area (CA) to the fourth step area (ST4).

<124> On the fourth interlayer insulating layer (60), the word line interconnection structures (81) and the body interconnection structures (82) as described in FIG. 2A, FIG. 3A, and FIG. 3B can be disposed.

<125> In one embodiment, the bit line lower contact plug (252) may have an upper

surface positioned in the same plane as the upper surface of the body lower contact plug (53).

<126> In one embodiment, the bit line lower contact plug (252) may have an upper surface positioned at a higher level than the cell vertical structures (CV) and the source patterns (46). However, the technical idea of the present invention is not limited thereto.

<127> In one embodiment, as shown in FIG. 15, a bit line lower contact plug (252') and a body lower contact plug (253') having upper surfaces that are positioned at a lower level than the upper surfaces of the source patterns (46) and are positioned in the same plane as the upper surfaces of the cell vertical structures (CV) may be disposed.

<128> In one embodiment, as shown in FIG. 16 a bit line lower contact plug (252'') and a body lower contact plug (253'') having upper surfaces positioned at a lower level than the upper surfaces of the cell vertical structures (CV) and the source patterns (46) may be disposed.

<129> A semiconductor device according to one embodiment of the technical idea of the present invention will be described with reference to FIGS. 17 and 18.

<130> Referring to FIGS. 17 and 18, first to third peripheral circuit regions (PC1, PC2, PC3) may be disposed on the semiconductor substrate (214) as described in FIGS. 13A, 13B, and 14. The first peripheral circuit region (PC1) may include a peripheral transistor (PTR) that may constitute a peripheral circuit as described in FIGS. 1, 2A, 2B, 3A, and 3B, and a first peripheral interconnection structure (PW1) electrically connected to the peripheral transistor (PTR). The first peripheral interconnection

structure (PW) may include a first peripheral contact pad part (PP1).

<131> A lower interlayer insulating layer (LILD) may be disposed to cover the first to third peripheral circuit areas (PC1, PC2, PC3) of the semiconductor substrate (2).

<132> As described in FIG. 13A FIG. 13B and FIG. 14, a buffer insulating pattern (10) may be disposed on the lower interlayer insulating layer (LILD), a semiconductor pattern (214) having an opening (216) may be disposed on the buffer insulating pattern (10), a gap fill insulating layer (218) filling the opening (216) and a middle interlayer insulating layer (219) disposed on a side surface of the semiconductor pattern (214) may be disposed.

<133> The cell gate conductive patterns (38a), the first dielectric (37), the cell vertical structures (CV), the cell source patterns (46), the cell interlayer insulating patterns (21), and the first to fourth interlayer insulating layers (24, 32, 48, 60) as described in FIG. 13A, FIG. 13B, and FIG. 14 may be disposed on the semiconductor pattern (214).

<134> A first insulating structure (323) may be disposed on the gap-fill insulating layer (218) of the opening (216) of the semiconductor pattern (214).

<135> A second insulating structure (324) may be disposed spaced apart from the opening (216) of the semiconductor pattern (214) and spaced apart from the cell gate conductive patterns (38a). The first and second insulating structures (323, 324) can be formed of silicon oxide.

<136> In one embodiment, the second insulating structure (324) may be disposed on the semiconductor pattern (214) between the first insulating structure (323) and the cell gate conductive patterns (38a).

- <137> In one embodiment, a first insulating pattern (320a) and a second insulating pattern (320b) may be alternately and repeatedly stacked between the first and second insulating structures (323, 324). The first insulating pattern (320) may be formed of silicon oxide, and the second insulating pattern (320b) may be formed of silicon nitride.
- <138> In one embodiment, the first and second insulating structures (323, 324) may be disposed in a shape that passes through the first upper interlayer insulating layer (24) and the first and second insulating patterns (320a, 320b).
- <139> As described in FIG. 13A, FIG. 13B and FIG. 14, a bit line contact structure (372) may be disposed that passes through the fourth step area (ST4) and the semiconductor substrate (214) below the fourth step area (ST4) and is electrically connected to the peripheral transistor (PTR) below the semiconductor pattern (214).
- <140> The bit line peripheral contact structure (372) may include a bit line lower contact plug (352) and a bit line upper contact plug (362) on the bit line lower contact plug (352).
- <141> The bit line lower contact plug (352) passes through a part of the peripheral lower interlayer insulating layer (LILD) covering the first to third upper interlayer insulating layers (32, 48), the insulating structure (323), the gap fill insulating layer (218) within the opening (216) and the first peripheral contact pad (PP1), and can be electrically connected to the first peripheral contact pad (PP1) that is electrically connected to the peripheral transistor (PTR).
- <142> The upper contact plug (362) around the bit line can pass through the fourth upper interlayer insulating layer (60) and be electrically connected to the lower

contact plug (252) around the bit line.

<143> In one embodiment, the cell lower body contact plug (53) of the cell body contact structure (73) as described in FIGS. 2A, 3A and 3B may be connected to the semiconductor pattern (214) while penetrating the second insulating structure (324).

<144> The cell bit line plugs (68), the cell gate contact structures (74) and the peripheral body contact structure (75) as described in FIGS. 2A, 3A and 3B can be disposed.

<145> Cell conductive lines, for example, bit lines (280), may be disposed on the fourth interlayer insulating layer (60). The bit lines (280) can overlap with and be electrically connected to the cell bit line contact plugs (68) and the peripheral bit line contact structures (372). The bit lines (380) can extend from the cell array area (CA) to the fourth step area (ST4).

<146> On the fourth interlayer insulating layer (60), the word line interconnection structures (81) and the body interconnection structures (82) as described in FIG. 2A, FIG. 3A, and FIG. 3B can be disposed.

<147> A method for forming a semiconductor device according to one embodiment of the present invention will be described with reference to FIG. 19.

<148> Referring to FIG. 19, a peripheral circuit can be formed on a semiconductor substrate. (S10) A semiconductor pattern can be formed on the peripheral circuit. (S20) A molding structure can be formed on the semiconductor pattern. (S30) Vertical structures passing through the molding structure can be formed on the semiconductor pattern. (S40) Trenches can be formed. (S50) Empty spaces can be formed inside the molding structure. (S60) Gate conductive patterns can be formed

within the empty spaces. (S70) Contact structures can be formed. (S80) interconnection structures can be formed. (S90)

<149> An example of a method for forming a semiconductor device according to one embodiment of the present invention described with reference to FIG. 19 will be described with reference to FIGS. 1, 2A, 2B, 3A, and 3B, and FIGS. 20A to 26B.

<150> Referring to FIG. 19, FIG. 20A and FIG. 20B together with FIG. 1 and FIG. 2A, a semiconductor substrate (2) can be prepared. The semiconductor substrate (2) can be formed of a semiconductor material such as silicon. A peripheral circuit area can be formed on the semiconductor substrate (2). (S10) The peripheral circuit region may include a first peripheral circuit region (PC1), a second peripheral circuit region (PC2), and a third peripheral circuit region (PC3).

<151> The first peripheral circuit region (PC1) may include a peripheral transistor (PTR) that may configure a circuit and a first peripheral interconnection structure (PW1) which is electrically connected to the peripheral transistor (PTR). The first peripheral interconnection structure (PW1) may be disposed within the first peripheral circuit area (PC1) and include a first peripheral contact pad (PP1). The formation of the peripheral transistor (PTR) may include forming an isolation region (3) that defines an active region, forming a peripheral gate (PG) on the active region, and forming peripheral impurity regions (PS, PD) that can function as a source and a drain on both sides of the peripheral gate (PG).

<152> The second peripheral circuit region (PC2 in FIG. 1) may include a second peripheral interconnection structure (PW2 in FIG. 1) having a second peripheral contact pad (PP2). The third peripheral circuit region (PC3) may include a third

peripheral interconnection structure (PW3) having a third peripheral contact pad (PP3).

<153> A lower interlayer insulating layer (LILD) covering the peripheral circuits of the first to third peripheral circuit regions (PC1, PC2, PC3) of the semiconductor substrate (2) can be formed.

<154> The first peripheral interconnection structure (PW) may be composed of a plurality of components including a peripheral plug part, a peripheral interconnection part, and the first peripheral contact pad part (PP1). The peripheral plug part of the first peripheral interconnection structure (PW) can be formed so as to pass through a part of the lower interlayer insulating layer (LILD) after forming a part of the lower interlayer insulating layer (LILD). The peripheral interconnection part of the first peripheral interconnection structure (PW) can be formed to be electrically connected to the peripheral plug part. The first peripheral interconnection structure (PW) and the first peripheral contact pad part (PP1) of the first peripheral interconnection structure (PW) can be covered by the lower interlayer insulating layer (LILD).

<155> A buffer insulating layer (10) can be formed on the lower interlayer insulating layer (LILD). The buffer insulating layer (10) may have a different etch selectivity than a part of the lower interlayer insulating layer (LILD) that is in contact with the buffer insulating layer (10). For example, a part of the lower interlayer insulating layer (LILD) covering the pad part (PP1) of the peripheral interconnection structure (PW) may be formed of silicon oxide, and the buffer insulating layer (10) may be formed of silicon nitride.

<156> A semiconductor pattern (14) can be formed on the buffer insulating layer (10).

The semiconductor pattern (14) may have an opening (16). The formation of the semiconductor pattern (14) having the opening (16) may include forming a semiconductor layer on the buffer insulating layer (10) and patterning the semiconductor layer. The semiconductor pattern (14) can be formed of silicon. The semiconductor pattern (14) can be formed of polysilicon.

<157> The semiconductor pattern (14) may overlap the first peripheral circuit area (PC1), the second peripheral circuit area (PC2), and/or the third peripheral circuit area (PC3). The semiconductor pattern (14) can be formed on the first to third peripheral circuit areas (PC1, PC2, PC3). (S20)

<158> The semiconductor pattern (14) may include a high-concentration impurity region (HC) and a low-concentration impurity region (LC) formed on the high-concentration impurity region (HC) and having a lower impurity concentration than the high-concentration impurity region (HC). The high-concentration impurity region (HC) and the low-concentration impurity region (LC) can be of P-type conductivity.

<159> Referring to FIG. 1, FIG. 2A, FIG. 19, FIG. 21A and FIG. 21B, after forming an insulating material layer on a substrate having the semiconductor pattern (14), the insulating material layer is flattened until the semiconductor pattern (14) is exposed, thereby forming a gap fill insulating layer (18) that fills the inside of the opening (16) of the semiconductor pattern (14), and an intermediate interlayer insulating layer (19) can be formed on the side surface of the semiconductor pattern (14). The gap fill insulating layer (18) and the intermediate interlayer insulating layer (19) can be formed of silicon oxide.

<160> A molding structure (MS) can be formed on the semiconductor pattern (14).

(S30) The formation of the molding structure (MS) may include alternately and repeatedly forming a first molding layer and a second molding layer on a substrate having the semiconductor pattern (14), the gap fill insulating layer (18), and the intermediate interlayer insulating layer (19), and patterning the first and second molding layers (20, 22) to form an end part in a step structure. The end part of the molding structure (MS) can be formed into a step structure.

<161> The first molding layer (20) may be formed of a material having an etch selectivity with respect to the second molding layer (22). For example, the first molding layer (20) may be formed of silicon oxide, and the second molding layer (22) may be formed of silicon nitride.

<162> Referring to FIG. 1, FIG. 2A, FIG. 19, FIG. 22A and FIG. 22B, a first upper interlayer insulating layer (24) can be formed on a substrate having the molding structure (MS). The first upper interlayer insulating layer (24) can be formed of silicon oxide. The first upper interlayer insulating layer (24) can be formed to have a substantially flat upper surface while covering the molding structure (MS).

<163> Cell vertical structures (CV) passing through the molding structure (MS) can be formed. (S40) The cell vertical structures (CV) can be formed on the semiconductor pattern (14). The cell vertical structures (CV) can pass through the first upper interlayer insulating layer (24) and the molding structure (MS) and be connected to the semiconductor pattern (14).

<164> Each of the cell vertical structures (CV) may include a first dielectric (27), a cell semiconductor layer (28), a core insulating pattern (29), and a cell pad pattern (30). For example, the formation of the cell vertical structures (CV) may include forming

holes passing through the first upper interlayer insulating layer (24) and the molding structure (MS), forming a first cell dielectric (27) on sidewalls of the holes, conformally forming a cell semiconductor layer on a substrate having the first cell dielectric (27) formed thereon, forming core insulating patterns (28) partially filling the holes on the cell semiconductor layer, forming a pad layer on the substrate having the core insulating patterns (28), and planarizing the pad layer and the cell semiconductor layer until the first upper interlayer insulating layer (24) is exposed to form the cell pad pattern (30) and the cell semiconductor layer (28) defined within the holes.

<165> The cell semiconductor layer (28) can be connected to the semiconductor pattern (14). The cell semiconductor layer (28) and the cell pad pattern (30) can be formed of silicon. For example, the cell semiconductor layer (28) and the cell pad pattern (30) may be formed of polysilicon.

<166> The formation of the first cell dielectric (27) may include forming an information storage material layer (e.g., a silicon nitride layer capable of trapping a charge) and a tunnel oxide layer (e.g., silicon oxide). The cell pad pattern (30) can be formed into an N-type conductive pattern using an ion implantation process.

<167> Referring to FIG. 1, FIG. 2A, FIG. 19, FIG. 23A and FIG. 23B, a second upper interlayer insulating layer (32) can be formed on a substrate having the cell vertical structures (CV). The second upper interlayer insulating layer (32) can be formed of silicon oxide.

<168> Trenches (34) can be formed. (S50) The trenches (34) can pass through the first and second upper interlayer insulating layers (24, 32) and the molding structure

(MS) to expose the semiconductor pattern (14).

- <169> In one embodiment, the trenches (34) may cross the molding structure (MS).
- <170> The trenches (34) may be line shapes extending in the first direction (X). The trenches (34) can be arranged parallel to a second direction (Y) perpendicular to the first direction (X).
- <171> The trenches (34) are arranged sequentially in the second direction (Y) and may include a first trench (34a), a second trench (34b), and a third trench (34c) that are parallel to each other. The spacing between the adjacent first and second trenches (34a, 34b) may be greater than the spacing between the adjacent second and third trenches (34b, 34c). The cell vertical structures (CV) may be disposed between relatively narrowly spaced trenches (34), for example, the first and second trenches (34b, 34c).
- <172> The opening (16) of the semiconductor pattern (14) may be disposed within the semiconductor pattern (14) between relatively widely spaced trenches (34), for example, the first and second trenches (34a, 34b).
- <173> Empty spaces (36) can be formed inside the molding structure (MS). (S60) The formation of the empty spaces (36) may include etching the second molding layers (22) exposed by the trenches (34). The etched parts of the second molding layers (22) can be formed as the empty spaces (36).
- <174> Among the second molding layers (22), the second molding layers positioned between the first and second trenches (34a, 34b) that are relatively widely spaced apart may remain by partially etching. In this way, the second molding layers (22) remaining between the first and second trenches (34a, 34b) can be defined as

second insulating patterns (22a).

<175> In addition, among the second molding layers (22), the second molding layers (22) located in the step areas positioned in the second direction (Y) perpendicular to the trenches (34) may remain by partially etching. The second molding layers (22) remaining in the step areas in this way can be defined as fourth insulating patterns (22b).

<176> Among the trenches (34), the first molding layers (20) located between relatively narrowly spaced trenches, for example, the second and third trenches (34b, 34c), can be defined as cell interlayer insulating patterns (21). The first molding layer (20) positioned between the first and second trenches (34a, 34b) can be defined as first insulating patterns (20a). The first molding layers (20) positioned in the step areas positioned in the second direction (Y) perpendicular to the trenches (34) can be defined as third insulating patterns (20b).

<177> The first insulating patterns (20a) and the second insulating patterns (20b) positioned between the first and second trenches (34a, 34b) that are relatively widely spaced apart from each other can be defined as an insulating structure (23). Accordingly, the insulating structure (23) may include the first insulating pattern (20a) and the second insulating pattern (20b) alternately and repeatedly stacked. The second insulating patterns (20b) may have a smaller width than the first insulating patterns (20a).

<178> Referring to FIG. 1, FIG. 2A, FIG. 19, FIG. 24A and FIG. 24B, a second cell dielectric (36) can be conformally formed on a substrate having the empty spaces (36). Gate conductive patterns can be formed within the empty spaces (36). The

formation of the gate conductive patterns may include forming a conductive material layer on a substrate having the second cell dielectric (36) and removing the conductive material layer formed on top of the second upper interlayer insulating layer (32) and within the trenches (34) by an etching process.

<179> Among the gate conductive patterns, the gate conductive patterns that can be formed in the empty spaces (36) between trenches (34) having a relatively small separation distance among the trenches (34), for example, the second and third trenches (34b, 34c), and that surround the side surfaces of the cell vertical structures (CV) can be defined as cell gate conductive patterns, and the gate conductive patterns that can be formed in the empty spaces (36) between trenches (34) having a relatively large separation distance, for example, the first and second trenches (34a, 34b) and in the empty spaces located within the step area located in the direction perpendicular to the trenches (34) can be defined as dummy gate conductive patterns (38b). The cell gate conductive patterns (38a) can be formed in a step structure at the end parts positioned in the first direction (X) parallel to the trenches (34).

<180> Referring to FIG. 1, FIG. 2A, FIG. 25A and FIG. 25B, an insulating spacer (40) can be formed on the side walls of the trenches (34). The insulating spacer (40) can be formed of an insulating material such as silicon oxide or silicon nitride.

<181> By performing an ion implantation process, a cell source impurity region (42) can be formed within the semiconductor pattern (14) exposed by the trenches (34). It can be formed within the low-concentration impurity region (LC) of the semiconductor pattern (14). The cell source impurity region (42) may have a different

conductivity type from the low concentration impurity region (LC). For example, the low concentration impurity region (LC) may be of P type conductivity, and the cell source impurity region (42) may be of N type conductivity.

<182> Cell source patterns (46) can be formed within the trenches (34). The cell source patterns (46) can be formed of a conductive material (e.g., a material such as Ti, TiN, W, etc.).

<183> The cell source patterns (46) may include first to third cell source patterns (46a, 46b, 46c) corresponding to the first to third trenches (34a, 34b, 34c) described in FIGS. 23A and 23B.

<184> A third upper interlayer insulating layer (48) can be formed on a substrate having the cell source patterns (46). The third upper interlayer insulating layer (48) may be formed of silicon oxide.

<185> Referring to FIG. 1, FIG. 2A, FIG. 26A, and FIG. 26B, a peripheral bit line lower contact plug (52), a cell body lower contact plug (53), cell gate lower contact plugs (54), and a peripheral body lower contact plug (55) can be formed.

<186> The peripheral bit line lower contact plug (52) may be disposed between the first and second source patterns (46a, 46b). The peripheral bit line lower contact plug (52) can penetrate insulating material layers positioned on the first peripheral contact pad (PP1) and be connected to the first peripheral contact pad (PP1). For example, the peripheral bit line lower contact plug (52) may pass through the first to third upper interlayer insulating layers (24, 32, 48), the first and second insulating patterns (20a, 22a), the gap fill insulating layer (18), and the fourth lower interlayer insulating layer (LILD4) covering the peripheral pads (PP1, PP2) among the lower

interlayer insulating layers (LILD) and be electrically connected to the first peripheral contact pad (PP1).

<187> The cell body lower contact plug (53) may pass through the first to third upper interlayer insulating layers (24, 32, 48) and the third and fourth insulating patterns (20b, 22b) within the step areas positioned in the second direction (Y) perpendicular to the cell source patterns (46) and be connected to the semiconductor pattern (14).

<188> In one embodiment, the cell body lower contact plug (53) may be formed in a line shape.

<189> In one embodiment, the cell body lower contact plug (53) may be formed of a plurality of circular shapes spaced apart from each other.

<190> The cell gate lower contact plugs (54) can pass through the first to third upper interlayer insulating layers (24, 32, 48) and be connected to the cell gate conductive patterns (38a) of the step area located between the cell source patterns (46).

<191> The peripheral body lower contact plug (55) may sequentially pass through a part of the lower interlayer insulating layer (LILD) positioned on the third peripheral contact pad (PP3), the buffer insulating layer (10), the interlayer insulating layer (19), and the first to third upper interlayer insulating layers (24, 32, 48) and be electrically connected to the third peripheral contact pad (PP3).

<192> The formation of the peripheral bit line lower contact plug (52), the cell body lower contact plug (53), the cell gate lower contact plugs (54), and the second peripheral lower contact plug (55) may include performing a photolithography and etching process to form contact holes, and forming a conductive material layer that fills the contact holes.

- <193> In one embodiment, an ion implantation process may be performed before forming the contact holes and filling them with the conductive material layer to implant impurities into the contact parts exposed by the contact holes. Accordingly, a cell body contact impurity region (50) can be formed within the semiconductor pattern (14) below the cell body lower contact plug (53). The cell body contact impurity region (50) may be of P-type conductivity. The cell body contact impurity region (50) can be formed with a higher impurity concentration than the low-concentration impurity region (LC).
- <194> In one embodiment, after forming the cell body contact impurity region (50), a metal silicide can be formed between the cell body contact impurity region (50) and the cell body lower contact plug (53).
- <195> Referring again to FIG. 1, FIG. 2A, FIG. 2B, FIG. 19, FIG. 3A and FIG. 3B, a fourth upper interlayer insulating layer (60) can be formed on a substrate having the peripheral bit line lower contact plug (52), the cell body lower contact plug (53), the cell gate lower contact plugs (54) and the peripheral body lower contact plug (55).
- <196> A peripheral bit line upper contact plug (62), a cell body upper contact plug (63), cell gate upper contact plugs (64), the peripheral body upper contact plug (65), and cell bit line contact plugs (68) can be formed.
- <197> The upper contact plug (62) around the bit line can pass through the fourth upper interlayer insulating layer (60) and be electrically connected to the lower contact plug (52) around the bit line. The peripheral bit line upper contact plug (62) and the peripheral bit line lower contact plug (52) can form a peripheral bit line contact structure (72).

- <198> The cell body upper contact plug (63) can be electrically connected to the cell body lower contact plug (53) while passing through the fourth upper interlayer insulating layer (60). The cell body upper contact plug (63) and the cell body lower contact plug (53) can form a cell body contact structure (73).
- <199> The cell gate upper contact plugs (64) can pass through the fourth upper interlayer insulating layer (60) and be electrically connected to the cell gate lower contact plugs (54).
- <200> The cell gate upper contact plugs (64) and the cell gate lower contact plugs (54) can form a cell gate contact structure (74).
- <201> The upper peripheral body contact plug (65) can pass through the fourth upper interlayer insulating layer (60) and be electrically connected to the lower peripheral body contact plug (55). The peripheral body upper contact plug (65) and the peripheral body lower contact plug (55) can form a peripheral body contact structure (75).
- <202> In one embodiment, a peripheral word line contact structure (77 in FIG. 1) can be formed. The peripheral word line contact structure (77) can be formed simultaneously with and with the same structure as the peripheral body contact structure (75). Accordingly, the peripheral word line contact structure (77) may be composed of a peripheral lower word line contact plug and a peripheral upper word line contact plug corresponding to the peripheral lower body contact plug (55) and the peripheral upper body contact plug (65) of the peripheral body contact structure (75).
- <203> The cell bit line contact plugs (68) may be formed on the cell pad patterns (30)

while pass through the second to fourth upper interlayer insulating layers (32, 48, 60).

<204> Next, a interconnection process can be performed to form interconnection structures on the fourth interlayer insulating layer (60). (S90) The interconnection structures may include bit lines (80), word line interconnection structures (81), and body interconnection structures (82).

<205> The bit lines (80) can overlap and be electrically connected to the bit line contact plugs (68) and the peripheral bit line contact structures (72).

<206> The word line interconnection structures (81) can be electrically connected to the cell gate contact structure (74) and the peripheral word line contact structure (77).

<207> The body interconnection structures (82) can be electrically connected to the cell body contact structure (73) and the peripheral body contact structure (75).

<208> Therefore, a semiconductor device such as that described in FIG. 1, FIG. 2A, FIG. 2B, 3A, and FIG. 3B can be formed. An example of a method for forming a semiconductor device as described in FIGS. 4A and 4B using a method for forming a semiconductor device according to one embodiment of the technical idea of the present invention will be described with reference to FIG. 27.

<209> Referring to FIG. 27, as described in FIG. 19, a peripheral circuit area can be formed on a semiconductor substrate, (S10) a semiconductor pattern can be formed on the peripheral circuit area, (S20) a molding structure can be formed on the semiconductor pattern, and (S30) a vertical structure penetrating the molding structure can be formed on the semiconductor pattern. (S40)

- <210> First contact plugs passing through the molding structure can be formed. (S140)
The first contact plugs may be the peripheral bit line lower contact plugs (52') and the cell body lower contact plug (53') in FIGS. 4A and 4B.
- <211> As described in FIG. 19, a trench can be formed (S50), empty spaces can be formed inside the molding structure (S60), and gate conductive patterns can be formed within the empty spaces. (S70)
- <212> Second contact plugs can be formed. (S180) The second contact plugs may be the cell gate lower contact plugs (54) and the peripheral body lower contact plugs (55) of FIG. 4B. Next, the cell bit line contact plugs (68), the peripheral bit line upper contact plug (62') and the peripheral upper body contact plug (65) can be formed. Next, interconnection structures can be formed as described in Fig. 19. (S90)
- <213> Next, an example of a method for forming a semiconductor device such as that described in FIGS. 5A and 5B will be described with reference to FIG. 28.
- <214> Referring to FIG. 28, as described in FIG. 19, a peripheral circuit area can be formed on a semiconductor substrate (S10) a semiconductor pattern can be formed on the peripheral circuit area (S20), and a molding structure can be formed on the semiconductor pattern. (S30) First contact plugs passing through the molding structure can be formed. (S240) The first contact plugs may be the peripheral bit line lower contact plugs (52'') and the cell body lower contact plug (53'') in FIGS. 5A and 5B.
- <215> As described in FIG. 19, vertical structures penetrating the molding structure can be formed (S40), trenches can be formed (S50), empty spaces can be formed inside the molding structure (S60), and gate conductive patterns can be formed

within the empty spaces. (S70) Next, second contact plugs can be formed. (S280) The second contact plugs may be the cell gate lower contact plugs (54) and the peripheral body lower contact plugs (55) of FIG. 5B. Next, the cell bit line contact plugs (68), the peripheral bit line upper contact plug (62"), the cell gate upper contact plug (64) and the peripheral upper body contact plug (65) can be formed. Next, interconnection structures can be formed as described in Fig. 19. (S90) Next, interconnection structures can be formed as described in Fig. 19. (S90)

<216> Next, a method for forming a semiconductor device according to one embodiment of the technical idea of the present invention will be described with reference to FIG. 29.

<214> Referring to FIG. 29, as described in FIG. 19, a peripheral circuit area can be formed on a semiconductor substrate (S10), a semiconductor pattern can be formed on the peripheral circuit area (S20), and a molding structure can be formed on the semiconductor pattern. (S30) Next, an insulating structure passing throughj the molding structure can be formed. (S340) Contact structures can be formed. (S350) interconnection structures can be formed. (S360)

<218> A method for forming a semiconductor device according to one embodiment of the technical idea of the present invention will be described with reference to FIG. 29, and FIGS. 30A to 32B, together with FIGS. 1 and 10.

<219> Referring to FIGS. 1, 10, 29, 30A and 30B, as described in FIGS. 20A and 20B, the peripheral circuit regions (PC1, PC2, PC3) can be formed on the semiconductor substrate (2), (S10) a lower interlayer insulating layer (LILD) covering a transistor (PTR) and a peripheral interconnection structure (PW) that can configure the circuits

of the peripheral circuit regions (PC1, PC2, PC3) can be formed on the semiconductor substrate (2), and the semiconductor pattern (14) having the buffer insulating layer (10) and the opening (16) can be formed on the lower interlayer insulating layer (LILD). The semiconductor pattern (14) can be formed on the first to third peripheral circuit areas (PC1, PC2, PC3). (S20)

<220> As described in FIGS. 21A and 21B, the gap-fill insulating layer (18) filling the opening (16) of the semiconductor pattern (14) and the intermediate interlayer insulating layer (19) covering the side surface of the semiconductor pattern (14) can be formed, and the molding structure (MS) can be formed on the semiconductor pattern (14) and the gap-fill insulating layer (18). The molding structure (MS) may include the first molding layer (20) and the second molding layer (22) alternately and repeatedly stacked.

<221> As described in FIG. 22A and FIG. 22B, a first upper interlayer insulating layer (24) can be formed on a substrate having the molding structure (MS), and a plurality of the cell vertical structures (CV) that pass through the first upper interlayer insulating layer (24) on the molding structure (MS) and the molding structure (MS) and are connected to the semiconductor pattern (14) can be formed.

<222> In one embodiment, an insulating structure (123) may be formed between the cell vertical structures (CV) and on the opening (16) of the semiconductor pattern (14), and passing through the first upper interlayer insulating layer (24) on the molding structure (MS) and the molding structure (MS).

<223> The insulating structure (123) can be formed of silicon oxide. The planar size of the insulating structure (123) may be larger than the planar size of the opening (16)

of the semiconductor pattern (14).

<224> In one embodiment, after forming the cell vertical structures (CV), the insulating structure (123) can be formed. However, the technical idea of the present invention is not limited thereto. For example, after forming the insulating structure (123), the cell vertical structures (CV) may be formed.

<225> Referring to FIGS. 31A and 31B together with FIGS. 1 and 10, as described in FIGS. 23A and 23B, the second upper interlayer insulating layer (32) can be formed on a substrate having the cell vertical structures (CV) and the insulating structure (123), the trenches (34) passing through the first and second upper interlayer insulating layers (24, 32) and the molding structure (MS) can be formed, and the second molding layers (22) exposed by the trenches (34) can be partially etched to form the empty spaces (36).

<226> Since the insulating structure (123) can be formed of a material having an etch selectivity with respect to the second molding layers (22), the insulating structure (123) can have etching resistance in a process of etching the insulating layers (22).

<227> As described in FIGS. 23A and 23B, the trenches (34) may include the first trench (34a), the second trench (34b), and the third trench (34c) arranged in sequence, and the first molding layers (20) may remain between the first and second trenches (34a, 34b) having a relatively large separation distance to form first insulating patterns (120a), and the insulating structure (123) may be positioned. Accordingly, the first insulating patterns (120a) may be disposed on the side of the insulating structure (123).

<228> Referring to FIGS. 32A and 32B together with FIGS. 1 and 10, the second

dielectric (37) can be formed on a substrate having the empty spaces (36), as described in FIGS. 24A and 24B, and the cell gate conductive patterns (38a) and the dummy gate conductive patterns (38b, 38c) can be formed.

<229> As described in FIG. 25A and FIG. 25B, it may include forming the insulating spacer (40) on the sidewalls of the trenches (34), forming the cell source impurity region (42) within the semiconductor pattern (14) below the trenches (34), forming the source patterns (46) filling the trenches (34), and forming the third upper interlayer insulating layer (48).

<230> As described in FIGS. 26A and 26B, the peripheral bit line lower contact plug (52), the cell body lower contact plug (53), the cell gate lower contact plugs (54), and the peripheral body lower contact plug (55) can be formed.

<231> The peripheral bit line lower contact plug (52) can pass through the second and third upper interlayer insulating layers (32, 38), the insulating structure (123), the gap fill insulating layer (18) in the opening (16) of the semiconductor pattern (14), the buffer insulating layer (10), and the lower interlayer insulating layer (LILD) above the first peripheral pad (PP1).

<232> As described in FIGS. 26A and 26B, after forming contact holes for forming the peripheral bit line lower contact plug (52), the cell body lower contact plug (53), the cell gate lower contact plugs (54), and the peripheral body lower contact plug (55), the cell body contact impurity region (50) can be formed within the semiconductor pattern (14).

<233> Referring back to FIGS. 11A and 11B together with FIGS. 1 and 10, as described with FIGS. 1, 2A, 2B and 19, and again with FIGS. 3A and 3B, the fourth

upper interlayer insulating layer (60) may be formed, the peripheral bit line upper contact plug (62), the cell body upper contact plug (63), the cell gate upper contact plugs (64), the peripheral body upper contact plug (65) and the cell bit line contact plugs (68) may be formed, and the interconnection structures (80, 81, 82) may be formed.

<234> Next, an example of a method for forming a semiconductor element described with reference to FIGS. 12, 13A, 13B, and 14 will be described with reference to FIGS. 33 to 35.

<219> Referring to FIGS. 1, 10, 29, 30A and 30B, as described in FIGS. 20A and 20B, the peripheral circuit regions (PC1, PC2, PC3) can be formed on the semiconductor substrate (2), (S10) a lower interlayer insulating layer (LILD) covering a transistor (PTR) and a peripheral interconnection structure (PW) that can configure the circuits of the peripheral circuit regions (PC1, PC2, PC3) can be formed on the semiconductor substrate (2), and the semiconductor pattern (14) having the buffer insulating layer (10) and the opening (16) can be formed on the lower interlayer insulating layer (LILD). the semiconductor pattern (14) can be formed on the peripheral circuit regions (PC1, PC2, PC3). (S20)

<236> A semiconductor pattern (214) having an opening (216) can be formed on the buffer insulating layer (10).

<237> A gap-fill insulating layer (218) filling the opening (216) of the semiconductor pattern (214) and an intermediate interlayer insulating layer (219) covering the side surface of the semiconductor pattern (214) can be formed.

<238> As in FIG. 21A and FIG. 21B, the molding structure (MS) can be formed on the

semiconductor pattern (214) and the gap fill insulating layer (218). The molding structure (MS) may include the first molding layer (20) and the second molding layer (22) alternately and repeatedly stacked.

<239> As described in FIG. 22A and FIG. 22B, a first upper interlayer insulating layer (24) can be formed on a substrate having the molding structure (MS), and a plurality of the cell vertical structures (CV) that penetrate the first upper interlayer insulating layer (24) on the molding structure (MS) and the molding structure (MS) and are connected to the semiconductor pattern (14) can be formed.

<240> Referring to FIG. 12, FIG. 13A, and FIG. 34, a second upper interlayer insulating layer (32) can be formed on a substrate having the cell vertical structures (CV).

<241> The trenches (234) passing through the first and second upper interlayer insulating layers (24, 32) and the molding structure (MS) can be formed. The trenches (234) can be arranged at regular intervals.

<242> The second molding layers (22) exposed by the trenches (234) are partially etched to form the empty spaces, and within the empty spaces, the second dielectric (37) and the cell gate conductive patterns (38a) can be formed by performing substantially the same process as described in FIGS. 23A and 23B.

<243> In one embodiment, the molding structure (MS) may remain in the second and fourth step areas (ST2, ST4) and be formed as an insulating structure (223). The insulating structure (223) may include a first insulating pattern (220a) and a second insulating pattern (220b) that are alternately and repeatedly stacked and stacked in a step structure.

- <244> The first molding layer (20) remaining between the cell gate conductive patterns (38a) can be defined as cell interlayer insulating patterns (21).
- <245> An insulating spacer (40) can be formed on the side walls of the trenches (234).
- <246> By performing an ion implantation process, a cell source impurity region (242) can be formed within the semiconductor pattern (214) below the trenches (234). The cell source impurity region (242) can be formed with a different conductivity type from the low concentration impurity region (LC) of the semiconductor pattern (242). Source patterns (246) can be formed on the trenches (234).
- <247> Referring to FIG. 12, FIG. 13A, and FIG. 35, a second upper interlayer insulating layer (42) can be formed on a substrate having the source patterns (246). Lower contact plugs (252, 253, 255) passing through the second upper interlayer insulating layer can be formed.
- <248> In one embodiment, before forming the lower contact plugs (252, 253, 255), contact holes for forming the lower contact plugs (252, 253, 255) may be formed, and an ion implantation process may be performed to implant impurities into the contact part exposed by the contact holes. Accordingly, a cell body contact impurity region (50) can be formed within the semiconductor pattern (14) below the cell body lower contact plug (253).
- <249> Referring again to FIG. 12, FIG. 13A, FIG. 13B and FIG. 14, a fourth upper interlayer insulating layer (60) can be formed on the substrate having the lower contact plugs (252, 253, 255). Cell bit line plugs (68) penetrating through the second to fourth upper interlayer insulating layers (24, 32, 48, 60) and connected to the cell vertical structures (CV), a peripheral upper bit line plug (262) penetrating through

the fourth upper interlayer insulating layer (60) and connected to the peripheral lower bit line plug (252), a cell body upper contact plug (63) connected to the cell body lower contact plug (53), and a peripheral body upper contact plug (65) connected to the peripheral body lower contact plug (55) can be formed.

<250> Next, interconnection structures can be formed on the fourth peripheral interlayer insulating layer (60). The interconnection structures may include bit lines (280), word line interconnection structures (81), and body interconnection structures (82). The bit lines (280) can be connected to the cell bit line plugs (68) and the peripheral upper bit line plugs (262).

<251> Next, an example of a method for forming a semiconductor element described with reference to FIGS. 12, 17, and 18 will be described with reference to FIGS. 36 and 37.

<252> Referring to FIG. 12, FIG. 17 and FIG. 36, as described in FIG. 33, the peripheral circuit regions (PC1, PC2, PC3), the buffer insulating layer (10), the semiconductor pattern (214) having the opening (216), the molding structure (MS), the first upper interlayer insulating layer (24) and the vertical structures (CV) can be formed on the semiconductor substrate (2).

<253> In one embodiment, before forming the vertical structures (CV), a first insulating structure (323) and a second insulating structure (324) penetrating the first upper interlayer insulating layer (24) and the molding structure (MS) can be formed. However, the technical idea of the present invention is not limited thereto. In one embodiment, before forming the vertical structures (CV), a first insulating structure (323) and a second insulating structure (324) penetrating the first upper interlayer

insulating layer (24) and the molding structure (MS) can be formed.

<254> The first and second insulating structures (323, 324) can be formed of silicon oxide. The first insulating structure (323) can overlap with the opening (216) of the semiconductor pattern (214). The second insulating structure (324) may not overlap with the opening (216) of the semiconductor pattern (214).

<255> Referring to FIG. 12, FIG. 17 and FIG. 37, a second upper interlayer insulating layer (32) can be formed on the first upper interlayer insulating layer (24). By performing substantially the same process as described in FIGS. 25A and 25B, the cell source patterns (46), the cell source impurity regions (42) under the cell source patterns (46), and the insulating spacers (40) on the side surfaces of the cell source patterns (46) can be formed.

<256> Referring again to FIG. 12, FIG. 17 and FIG. 18, a third upper interlayer insulating layer (48) covering the cell source patterns (46) can be formed on the second upper interlayer insulating layer (32).

<257> A peripheral bit line lower contact plug (352) may be formed that is connected to the first peripheral pad (PP1) of the first peripheral circuit area (PC1) while passing through the second and third upper interlayer insulating layers (32, 48), the first insulating structure (323), and the gap fill insulating layer (218) within the opening (216) of the semiconductor pattern (214).

<258> In one embodiment, while forming the peripheral bit line lower contact plug (352), a cell body lower contact plug (355) that passes through the second and third upper interlayer insulating layers (32, 48) and the second insulating structure (324) and is connected to the semiconductor pattern (214) can be formed.

<259> In one embodiment, the formation of the lower contact plugs (352, 355) may include forming a bit line peripheral lower contact hole exposing the first peripheral pad (PP1) and a cell body lower contact hole exposing the semiconductor pattern (214), performing an ion implantation process to form a cell body contact impurity region (50) within the semiconductor pattern (214), and filling the contact holes with a metal material. Next, the fourth upper interlayer insulating layer (60) can be formed, upper contact plugs (68, 372) can be formed, and interconnection structures can be formed.

<260> FIG. 38 is a schematic drawing showing a semiconductor module (400) according to embodiments of the technical idea of the present invention.

<261> Referring to FIG. 38, a semiconductor module (400) may include a memory element (430) formed on a module substrate (410). The semiconductor module (400) may include a semiconductor element (420) mounted on the module substrate (410).

<262> The memory device (430) may include the semiconductor device according to embodiments of the technical idea of the present invention. Input/output terminals (440) may be disposed on at least one side of the module substrate (410).

<263> Figure 39 is a block diagram conceptually illustrating an electronic system (500) according to an embodiment of the technical idea of the present invention.

<264> Referring to FIG. 39, an electronic system (500) including a semiconductor device according to an embodiment of the technical idea of the present invention can be provided.

<265> The electronic system (500) may include a body (510). The body (510) may

include a microprocessor unit (560), a power supply (530), a function unit (540), and/or a display controller unit (550). The body (510) may be a system board or motherboard having a printed circuit board (PCB), etc.

<266> The microprocessor unit (560), the power supply (530), the function unit (540), and the display controller unit (550) can be mounted or installed on the body (510). A display unit (560) may be disposed on the upper surface of the body (510) or on the outside of the body (510). For example, the display unit (560) may be disposed on the surface of the body (510) and display an image processed by the display controller unit (550). The power supply (530) can receive a constant voltage from an external power source, etc., branch it into various voltage levels, and supply it to a microprocessor unit (560), a function unit (540), a display controller unit (550), etc. The microprocessor unit (560) can receive voltage from the power supply (530) and control the function unit (540) and the display unit (560).

<267> The function unit (540) can perform functions of various electronic systems (500). For example, if the electronic system (500) is a mobile electronic product such as a mobile phone, the function unit (540) may include various components that can perform wireless communication functions such as image output to the display unit (560) or voice output to a speaker through dialing or communication with an external apparatus (570), and if it includes a camera, it may function as an image processor.

<268> In one embodiment, when the electronic system (500) is connected to a memory card or the like for capacity expansion, the function unit (540) may be a memory card controller. The function unit (540) can exchange signals with an external device (570) through a wired or wireless communication unit (580).

<269> In addition, when the electronic system (500) requires a Universal Serial Bus (USB) or the like for functional expansion, the functional unit (540) may act as an interface controller.

<270> FIG. 40 is a schematic block diagram showing an electronic system (600) according to an embodiment of the technical idea of the present invention.

<271> Referring to FIG. 40, the electronic system (600) may include a semiconductor device according to an embodiment of the technical idea of the present invention. The electronic system (600) may include a memory system (612), a microprocessor (614), a RAM (616), and a user interface (618) that performs data communication using a bus (620). A microprocessor (614) can program and control the electronic system (600). RAM (616) can be used as operating memory of the microprocessor (614). The microprocessor (614), RAM (616) and/or other components may be assembled within a single package. The memory system (612) may include semiconductor devices according to embodiments of the present invention.

<272> The user interface (618) can be used to input data into the electronic system (600) or output data from the electronic system (600). The memory system (612) can store codes for operating the microprocessor (614), data processed by the microprocessor (614), or external input data. The memory system (612) may include a controller and memory.

<273> Although the embodiments of the present invention have been described above with reference to the attached drawings, those skilled in the art will understand that the present invention can be implemented in other specific forms without changing the technical idea or essential features thereof. Therefore, it should be understood

that the embodiments described above are exemplary in all respects and not restrictive.

[Explanation of symbols]

<274> 2: Board PC1, PC2, PC3: Peripheral circuit

PW1, PW2, PW3: Peripheral interconnection structure

PP1, PP2, PP3: Peripheral contact pads

LILD: Lower interlayer insulating layer 10: Buffer insulating layer

14, 214 : Semiconductor pattern 16, 216 : Aperture

18, 218: Gap fill insulating layer 19, 219: Interlayer insulating layer

HC: High concentration impurity region (3rd impurity region)

LC: Low concentration impurity region (1st impurity region)

MS: Molding structure

20a: 1st insulating pattern 20b: 3rd insulating pattern

21: Cell interlayer insulating patterns 22a: Second insulating pattern

22b: 4th insulating pattern

23, 223, 323, 324 : Insulating structures

24: First upper interlayer insulation layer CV: Cell vertical structure

27: First cell dielectric 28: Cell semiconductor layer

29: Core insulation pattern 30: Cell pad pattern

32: Second upper interlayer insulation layer 34: Trench

37: Second dielectric 38a: Cell gate conductive pattern

38b: Dummy Gate Challenge Pattern

GS1, GS2, GS3: Cell Gate Conductive Structure

40: Insulating spacer

42: Cell source impurity region

46: Source pattern

48: Third upper interlayer insulating

layer

50: Cell body contact impurity region H: Hole

SP: Insulating spacer

52, 252: Peripheral bit line lower contact plug

53: Cell body lower contact plug

54: Cell gate lower contact plug

55: Peripheral body lower contact plug

60: 4th upper interlayer insulation layer

62: Peripheral bit line upper contact plug

63: Cell body upper contact plug

64: Cell gate upper contact plug

65: Peripheral body upper contact plug

68: Cell bit line contact plug 71: Body contact structure

72: Bit line peripheral contact structure 73: Cell body contact structure

74: Cell gate contact structure 75: Peripheral body contact structure

77: Peripheral word line peripheral contact structure

80: bit line (=cell conductive line)

81: Word line interconnection structure 82: Body interconnection structure

What is claimed is:

1.

A semiconductor device comprising: a semiconductor pattern disposed on a semiconductor substrate and having an opening, wherein the semiconductor pattern comprises a first impurity region having a first conductivity type and a second impurity region having a second conductivity type different from the first conductivity type;

a peripheral transistor disposed between the semiconductor substrate and the semiconductor pattern;

a first peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern and electrically connected to the peripheral transistor;

cell gate conductive patterns disposed on the semiconductor pattern;

cell vertical structures disposed to pass through the cell gate conductive patterns and to be connected to the semiconductor pattern;

cell bit line contact plugs disposed on the cell vertical structures;

a bit line disposed on the cell bit line contact plugs; and

a peripheral bit line contact structure disposed between the bit line and the first peripheral interconnection structure and passing through the opening of the semiconductor pattern.

2

The semiconductor device of claim 1, further comprising:

a body contact impurity region having the same conductivity type as the first impurity region and a higher impurity concentration than the first impurity region.

3

The semiconductor device of claim 2, further comprising:

a cell body contact structure disposed on the body contact impurity region.

4

The semiconductor device of claim 3, comprising:

a second peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern and extending outside the semiconductor pattern; and

a peripheral body contact structure disposed outside the semiconductor pattern and on the peripheral interconnection structure; and

a cell body interconnection structure disposed on the peripheral body contact structure and the cell body contact structure and electrically connected to the peripheral body contact structure and the cell body contact structure.

5

The semiconductor device of claim 1, further comprising:

a third impurity region disposed within the semiconductor pattern and having the same conductivity type as the first impurity region but a higher impurity concentration than the first impurity region, and disposed below the first impurity region.

6

The semiconductor device of claim 1, further comprising:

a cell source pattern disposed on the second impurity region of the semiconductor pattern.

7

A semiconductor device comprising: a semiconductor pattern disposed on a semiconductor substrate and having an opening;

a first peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern and having a first peripheral contact pad;

a second peripheral interconnection structure disposed between the semiconductor substrate and the semiconductor pattern and extended in an outside direction of the semiconductor pattern, and having a second peripheral contact pad;

a cell array area disposed on the semiconductor pattern;

a step area disposed on the semiconductor pattern and disposed on one side of the cell array area;

a cell gate conductive pattern disposed on the semiconductor pattern, wherein the cell gate conductive pattern is disposed within the cell array area and extended to the step area;

a cell vertical structure disposed to pass through the cell gate conductive pattern in the cell array area and connected to the semiconductor pattern;

a bit line on the cell vertical structure;

a peripheral bit line contact structure disposed between the bit line and the first peripheral contact pad and passing through the opening of the semiconductor pattern;

a cell gate contact structure disposed on the cell gate conductive pattern of the step area on the semiconductor pattern;

a peripheral word line contact structure disposed on the second peripheral contact pad and disposed on the outer side of the semiconductor pattern; and

a word line interconnection structure electrically connecting the cell gate contact

structure and the peripheral word line contact structure.

8

The semiconductor device of claim 7,
wherein the opening is a semiconductor device deposited below the cell array area.

9

The semiconductor device of claim 7,
wherein the opening is a semiconductor device deposited below the step area.

10

The semiconductor device of claim 7,
wherein the opening is a semiconductor device deposited below the cell array area
and extended to the step area.

11

The semiconductor device comprising: a semiconductor pattern on a semiconductor
substrate;

a peripheral transistor disposed between the semiconductor substrate and the
semiconductor pattern;

a peripheral interconnection structure disposed between the semiconductor substrate
and the semiconductor pattern and electrically connected to the peripheral transistor, and
having a peripheral contact pad;

a gate conductive structure disposed on the semiconductor pattern, wherein the gate
conductive structure includes a plurality of cell gate conductive patterns stacked in a
direction perpendicular to the semiconductor pattern;

a cell vertical structure passing through the gate conductive structure;

a cell conductive line on the cell vertical structure, wherein the cell conductive line have a length smaller than the width of the semiconductor pattern; and

a peripheral contact structure disposed between the cell conductive line and the peripheral contact pad.

12

The semiconductor device of claim 11,

wherein the cell conductive line has an elongated line shape in the first direction, and the width of the semiconductor pattern is a width in the first direction.

13

The semiconductor device of claim 11, further comprising:

a buffer insulating layer disposed between the lower interlayer insulating layer and the semiconductor pattern.

14

The semiconductor device of claim 13, further comprising:

a gap-fill insulating layer filling the opening of the semiconductor pattern, wherein the gap-fill insulating layer is formed of a material having a different etch selectivity from the buffer insulating layer and the peripheral contact structure is a semiconductor device passing through the gap fill insulating layer.

15

The semiconductor device of claim 11, further comprising:

an insulating structure disposed on the semiconductor pattern,

wherein the peripheral contact structure is a semiconductor element passing through the insulating structure.

16

The semiconductor device of claim 15, comprising:

a first insulating pattern and a second insulating pattern alternately and repeatedly stacked,

wherein the first insulating pattern includes a material having an etch selectivity different from that of the second insulating pattern.

17

The semiconductor device of claim 16,

wherein the first insulating patterns have a width greater than that of the second insulating patterns.

18

The semiconductor device of claim 16,

whichin the first insulating patterns are disposed on the same plane as the cell gate conductive patterns.

19

The semiconductor device of claim 16, further comprising:

a third insulating pattern and a fourth insulating pattern which are disposed on the semiconductor pattern and alternately and repeatedly stacked,

wherein the third insulating patterns are disposed on the same plane as the first insulating patterns and formed of the same material as the first insulating patterns,

and the fourth insulating patterns are disposed on the same plane as the second insulating patterns and formed of the same material as the second insulating patterns.

20

The semiconductor device of claim 19, further comprising:

a body contact structure passing through the third and fourth insulating patterns and connected to the semiconductor pattern.

ABSTRACT

ABSTRACT

The semiconductor device includes a semiconductor pattern, which is disposed on a semiconductor substrate and has an opening. The semiconductor pattern includes a first impurity region having a first conductivity type and a second impurity region having a second conductivity type different from the first conductivity type. A peripheral transistor is disposed between the semiconductor substrate and the semiconductor pattern. A first peripheral interconnection structure is disposed between the semiconductor substrate and the semiconductor pattern. The first peripheral interconnection structure is electrically connected to the peripheral transistor. Cell gate conductive patterns are disposed on the semiconductor pattern. Cell vertical structures are disposed to pass through the cell gate conductive patterns and connected to the semiconductor patterns. Cell bit line contact plugs are disposed on the cell vertical structures. A bit line is disposed on the cell bit line contact plugs. A peripheral bit line contact structure is disposed between the bit line and the first peripheral interconnection structure. The peripheral bit line contact structure passes through the opening of the semiconductor pattern.

REPRESENTATIVES

FIG. 3A

DRAWINGS

FIG. 2A

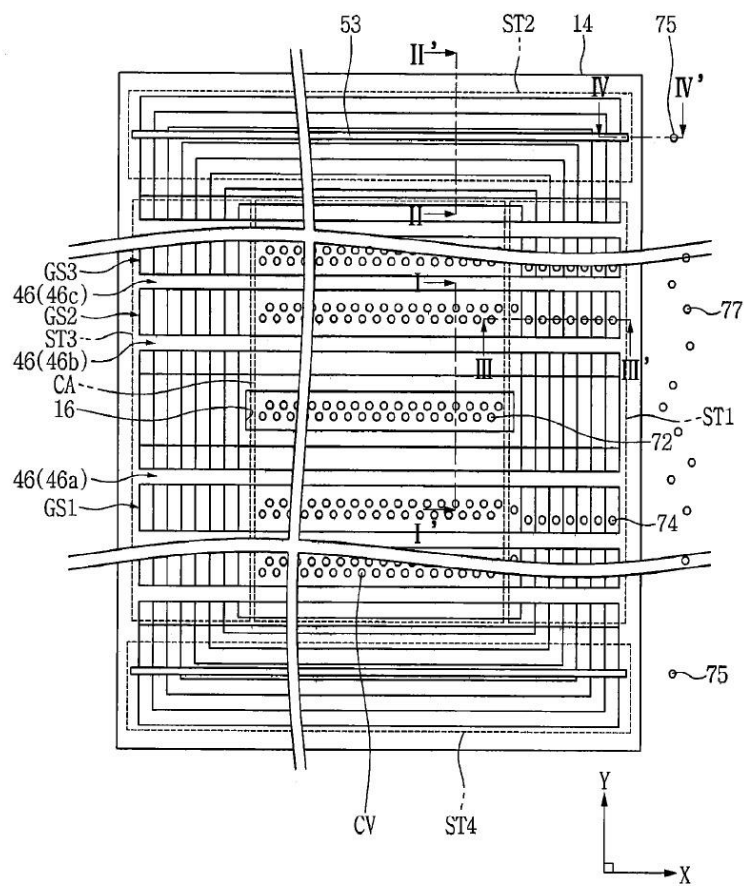


FIG. 2B

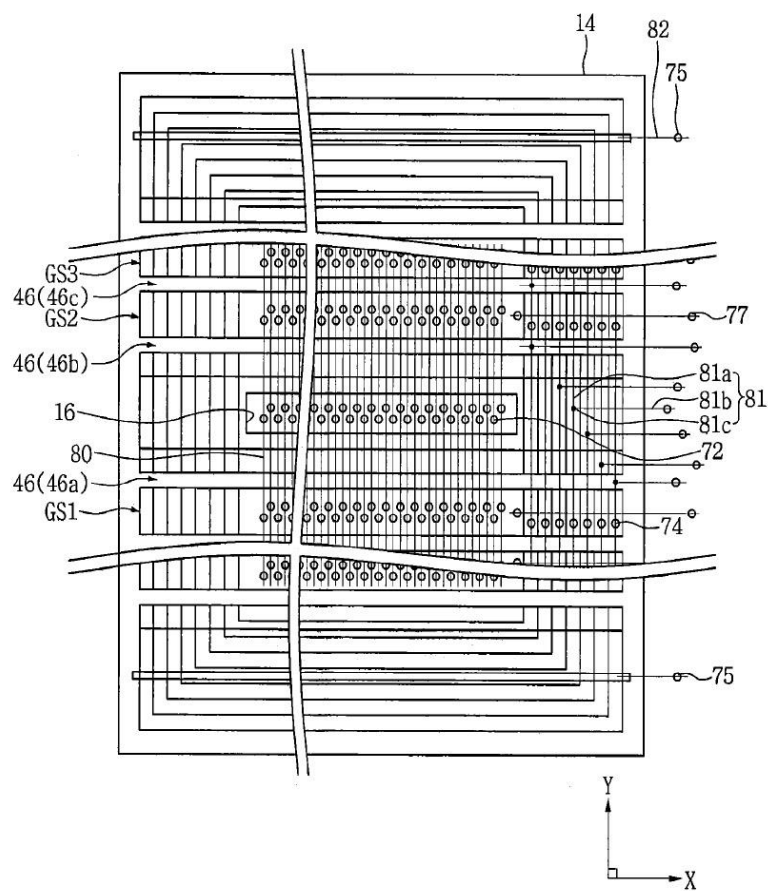


FIG. 3A

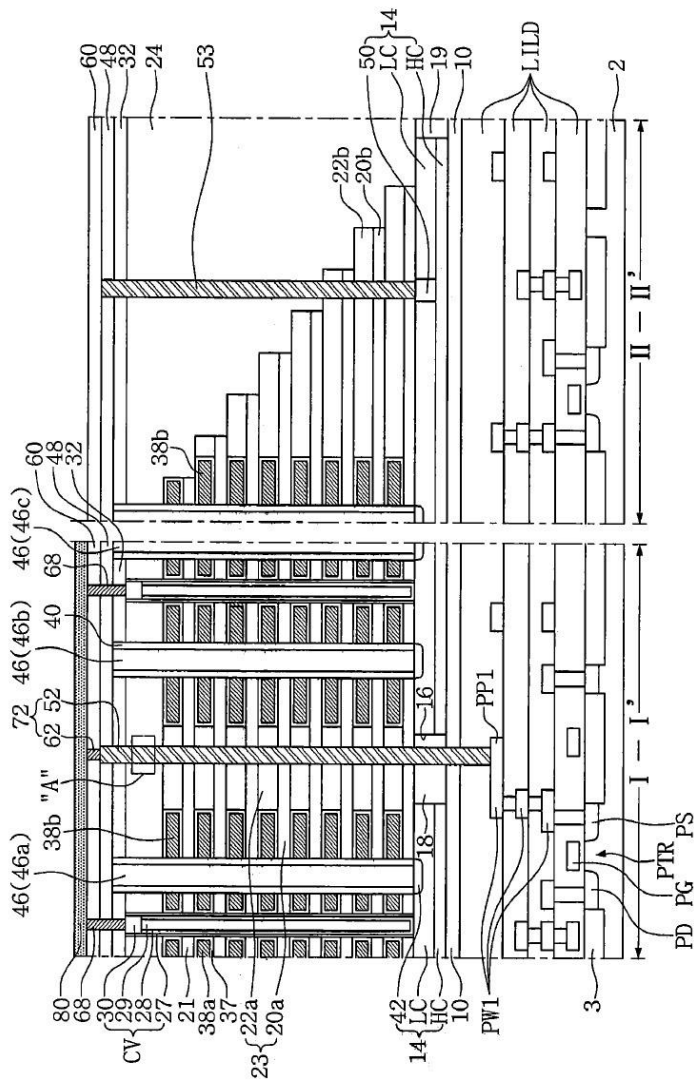


FIG. 3B

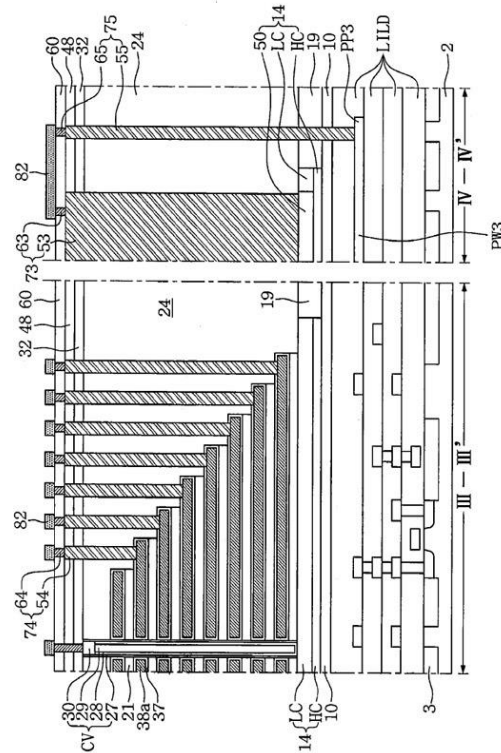


FIG. 3C

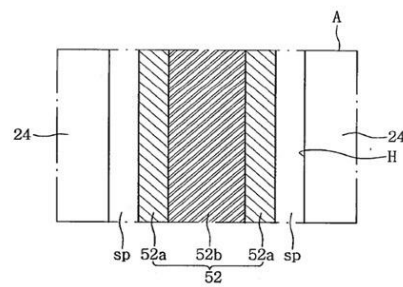


FIG. 4A

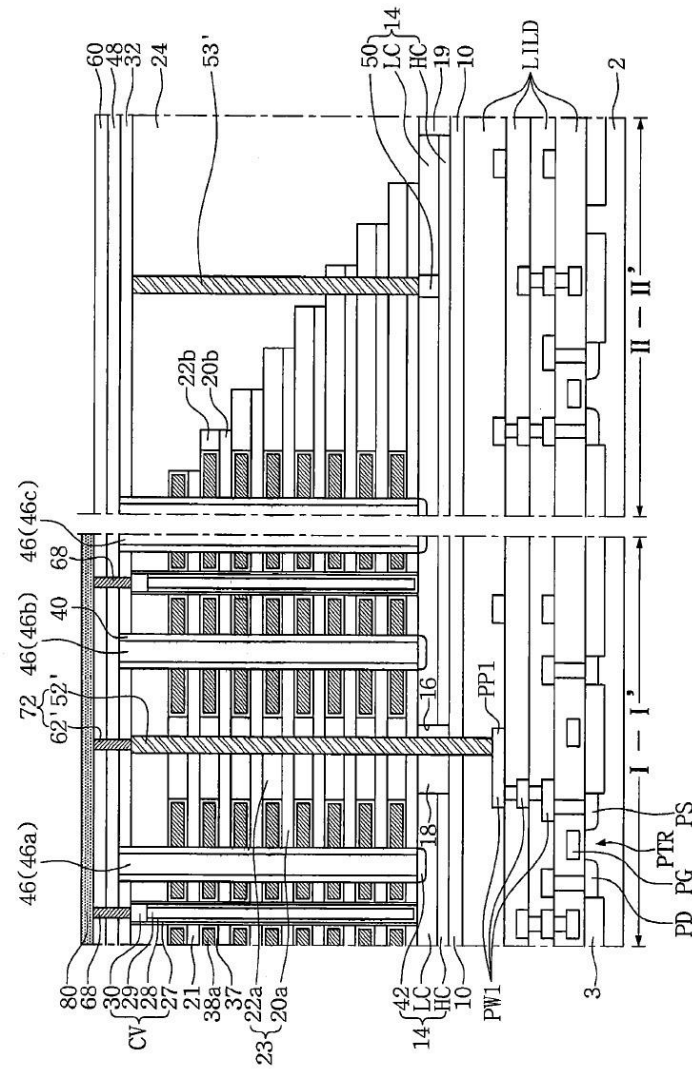


FIG. 4B

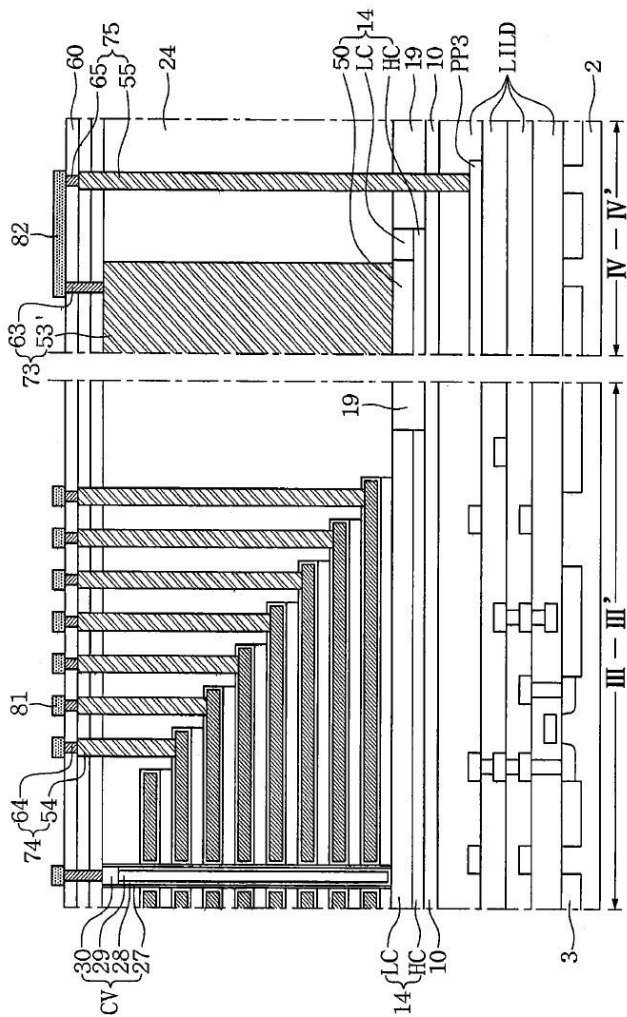


FIG. 5A

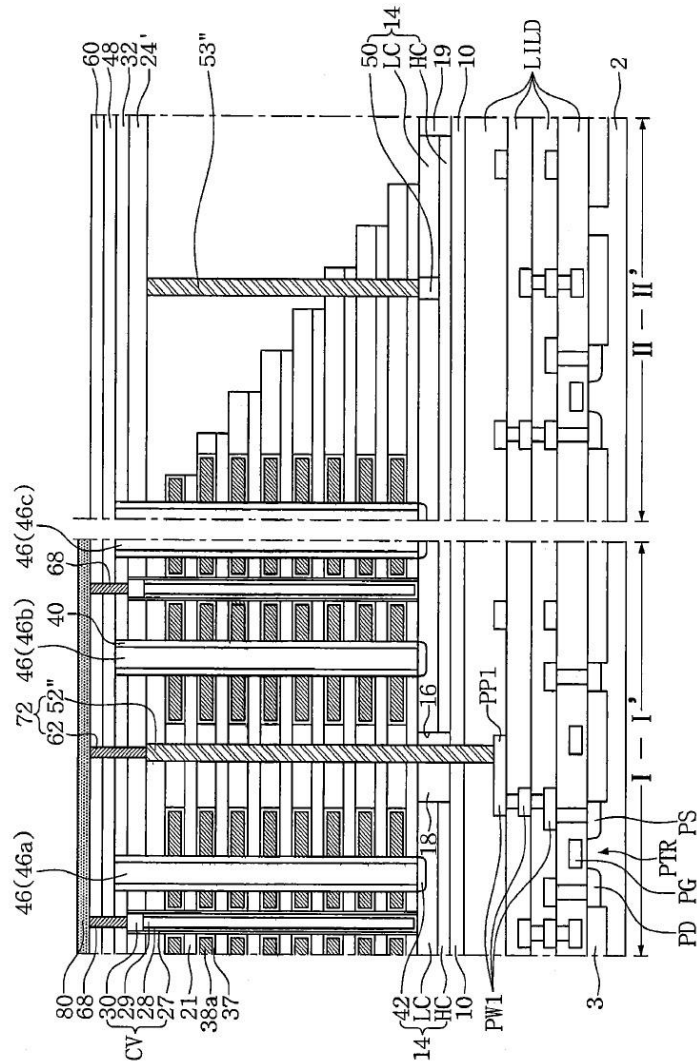


FIG. 5B

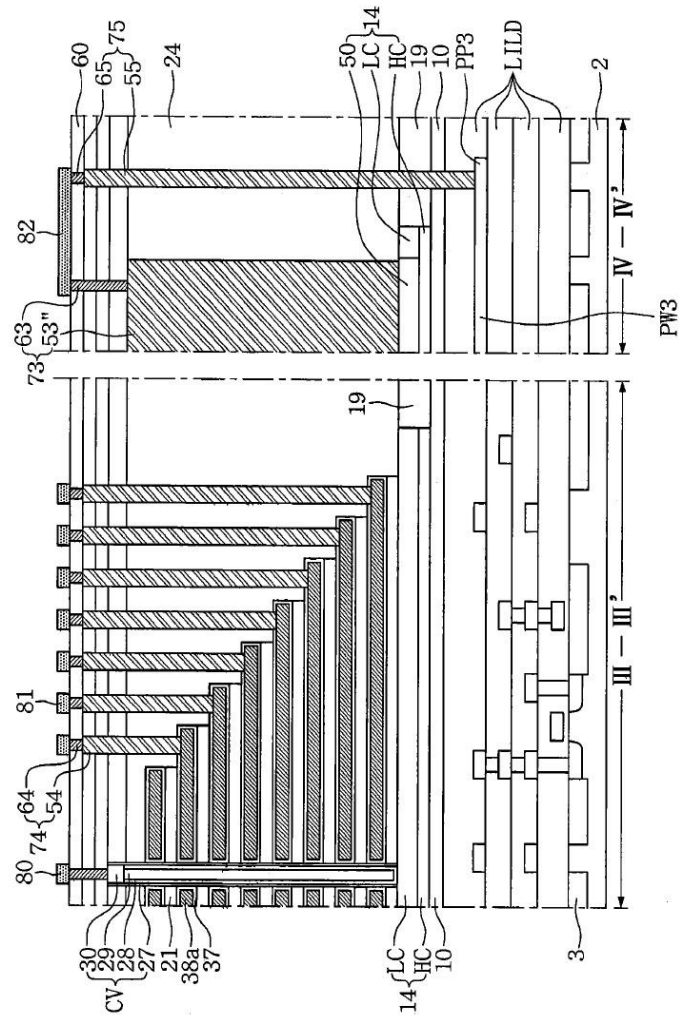


FIG. 6

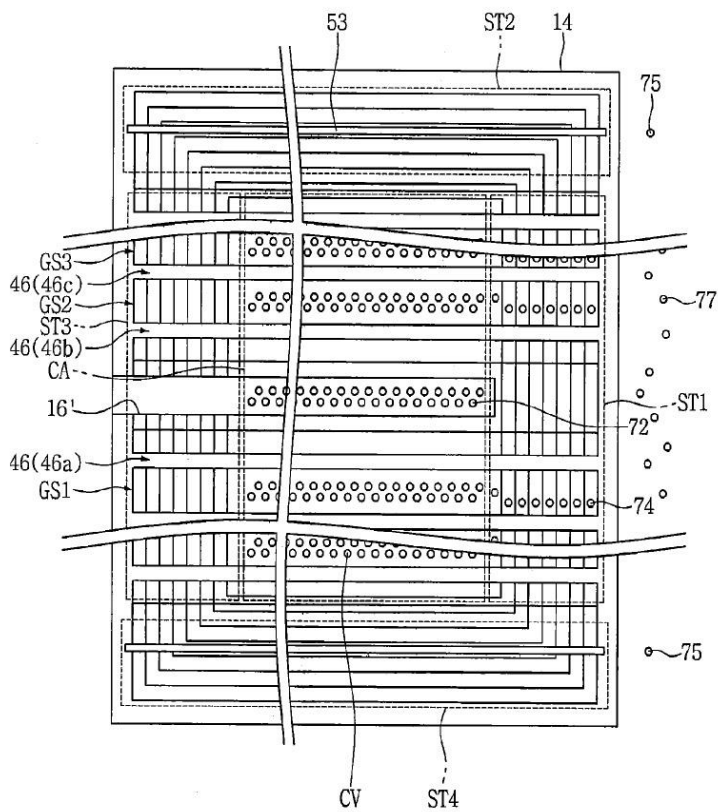


FIG. 7

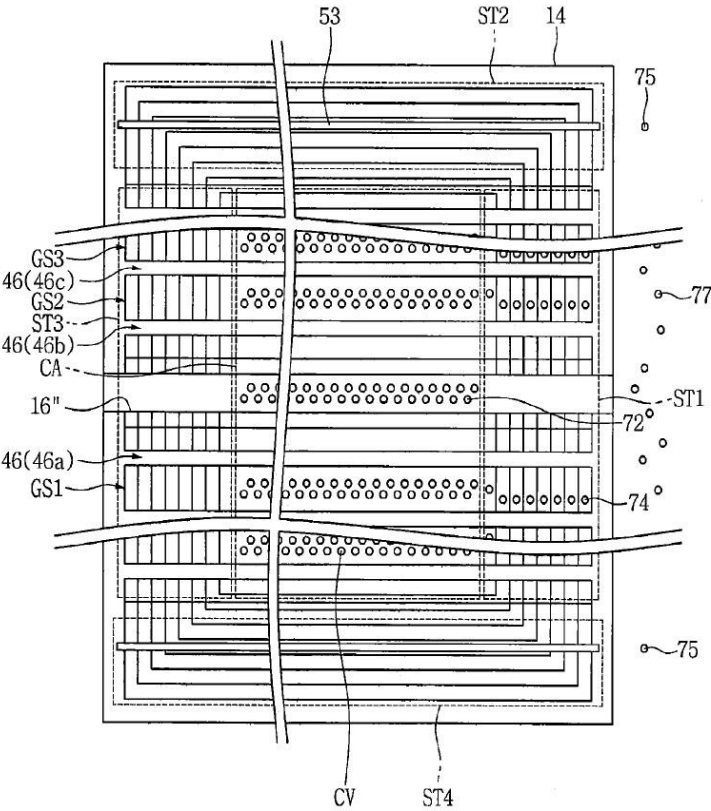


FIG. 8

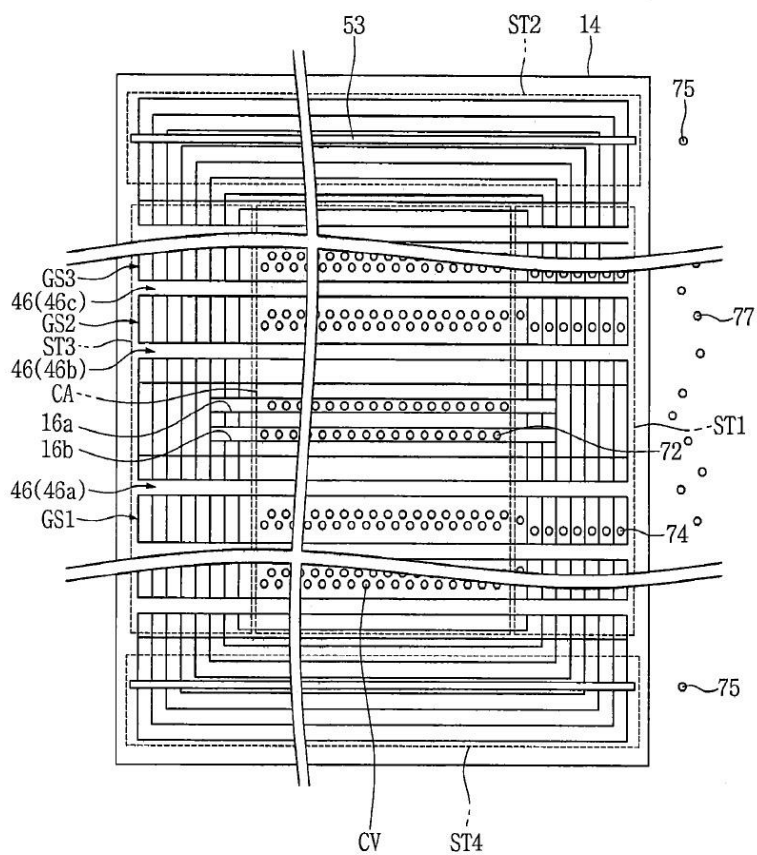


FIG. 9

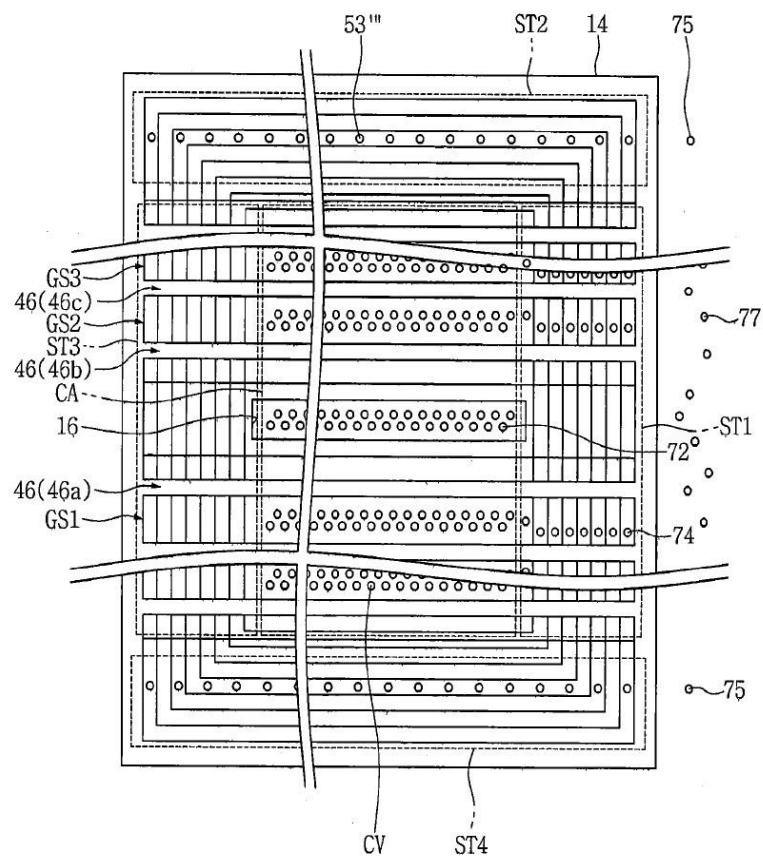


FIG. 10

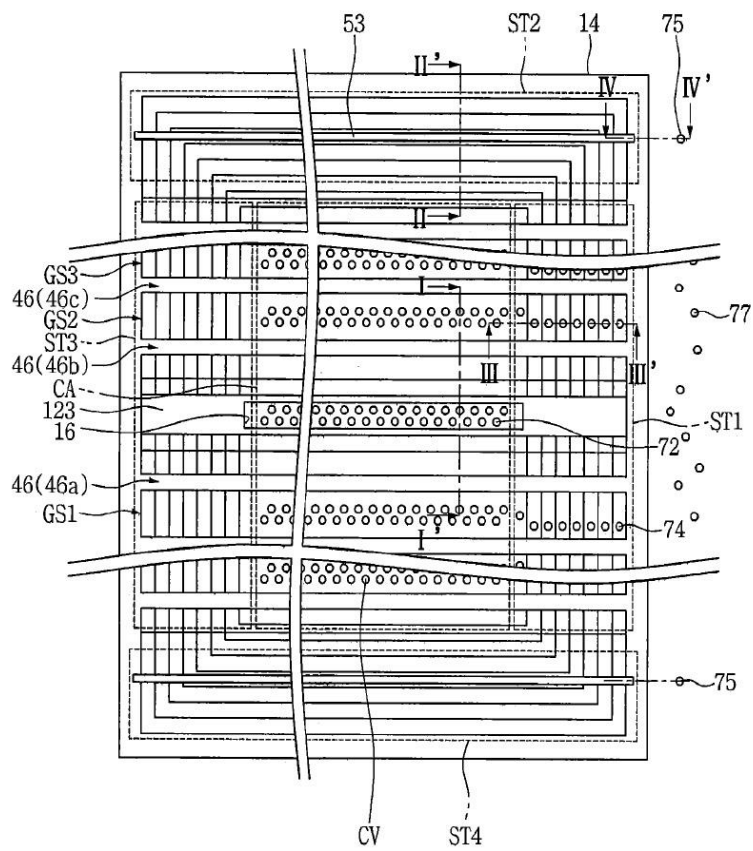


FIG. 11A

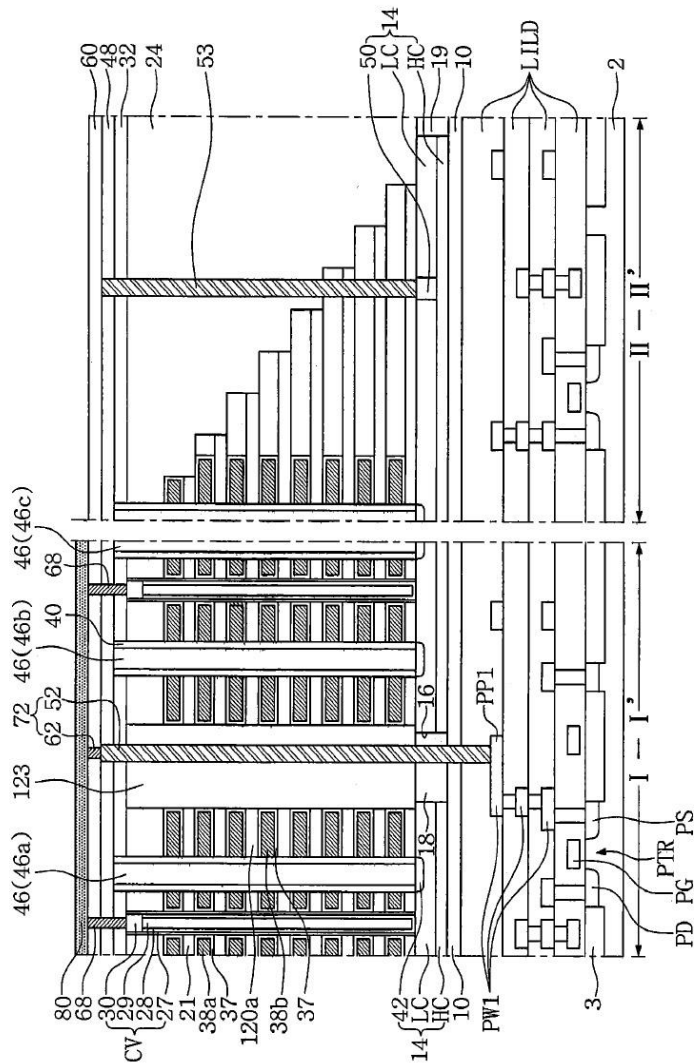


FIG. 11B

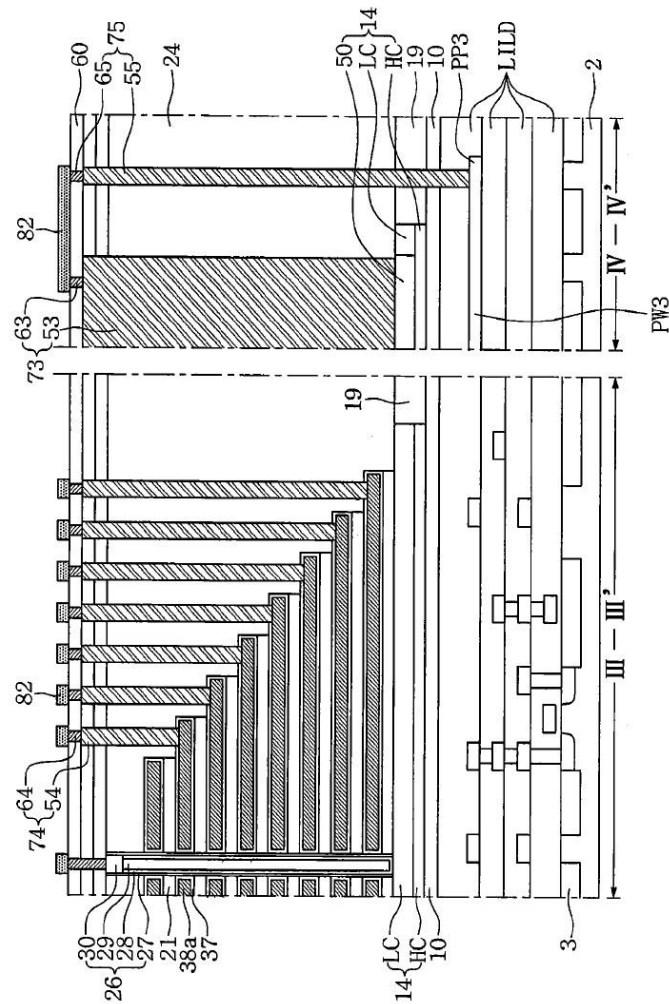


FIG. 12

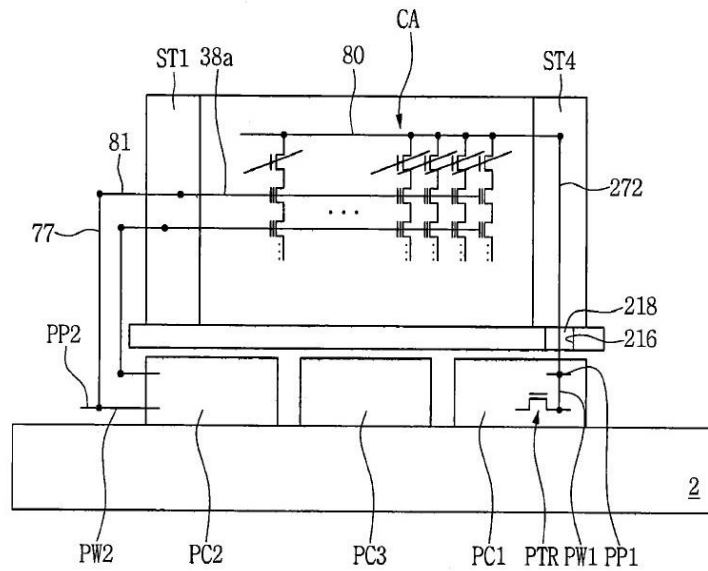


FIG. 13A

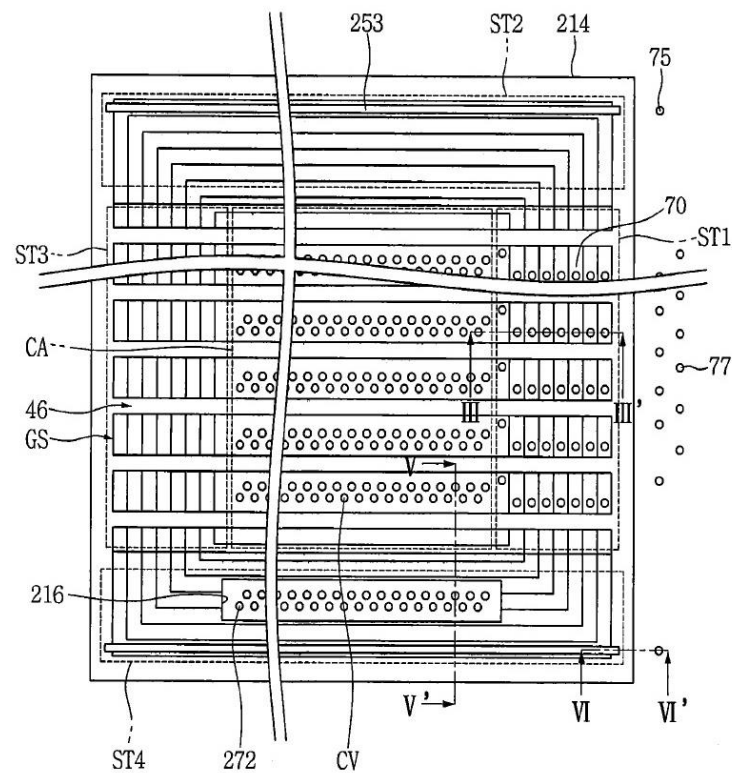


FIG. 13B

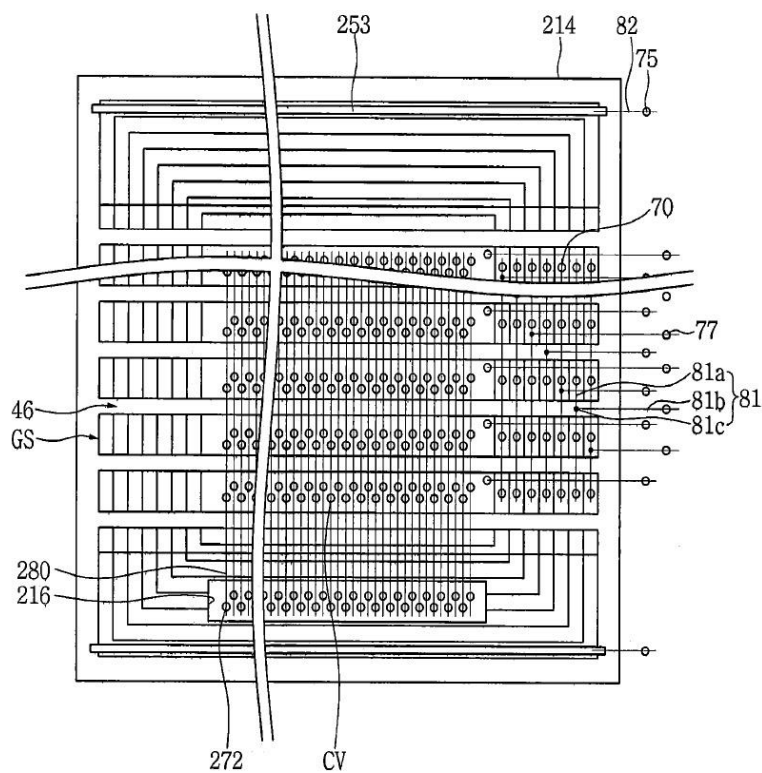


FIG. 14

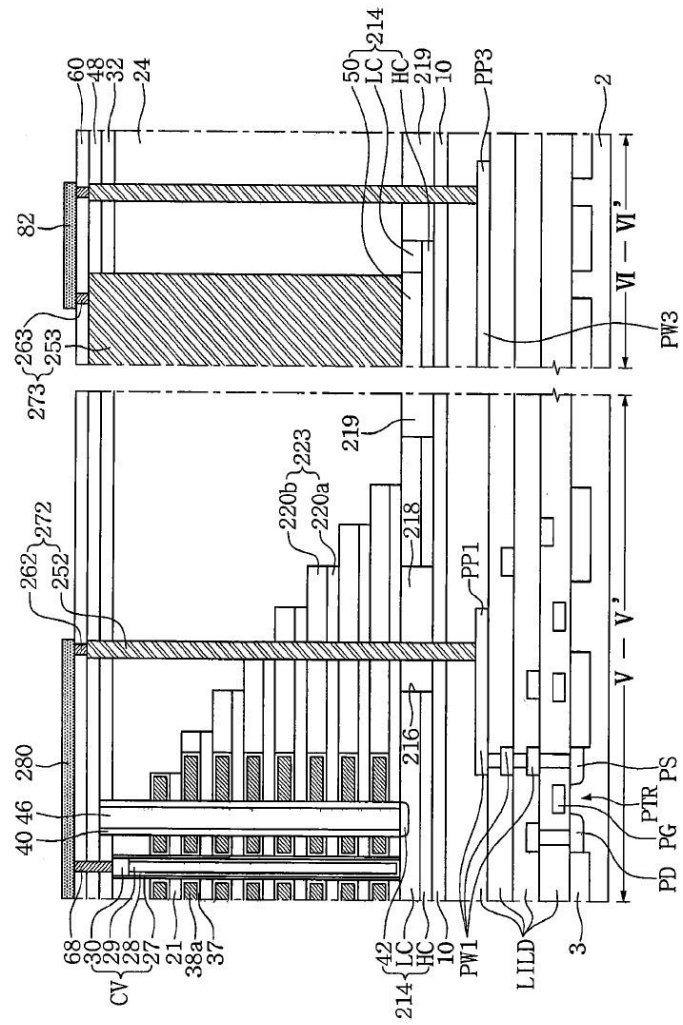


FIG. 15

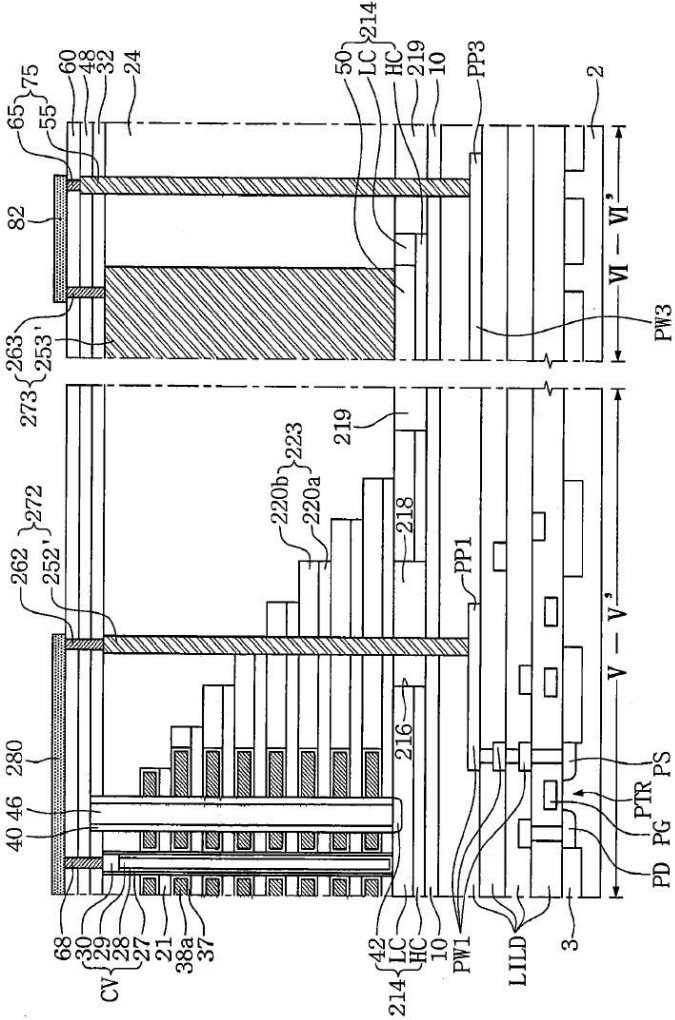


FIG. 16

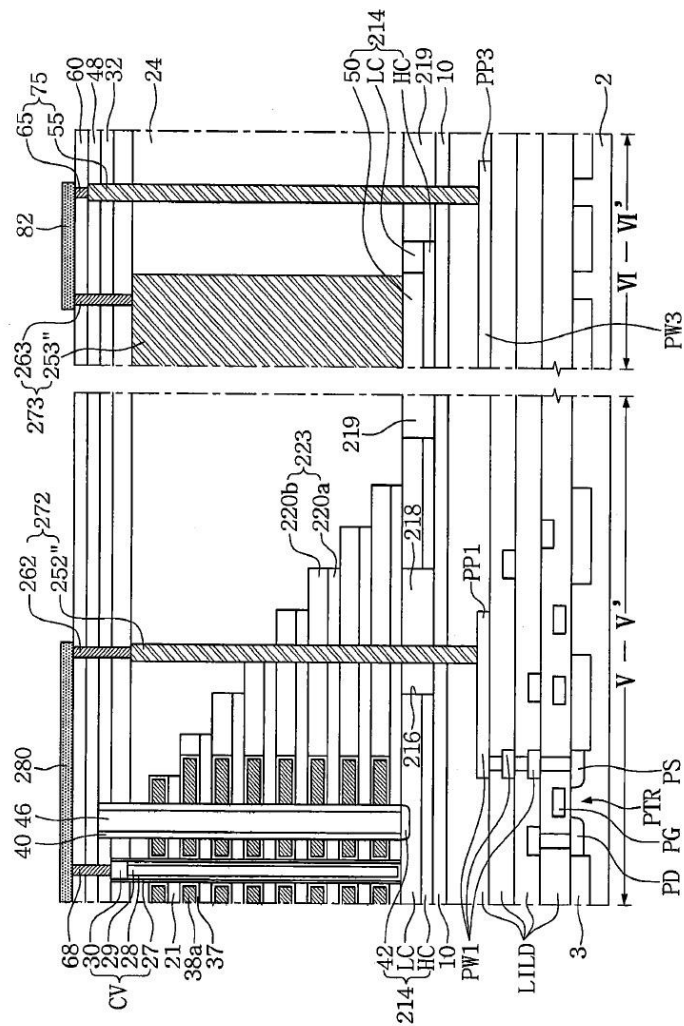


FIG. 17

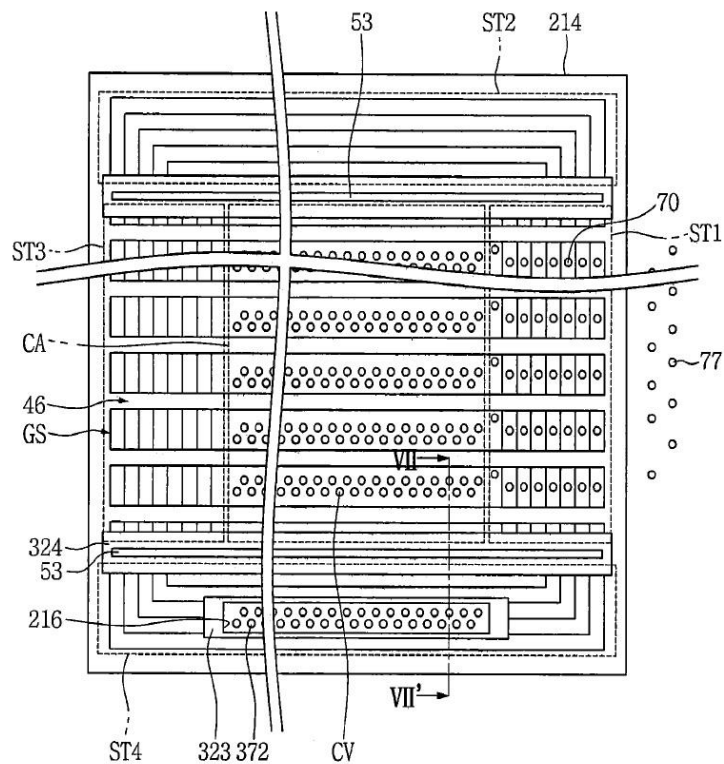


FIG. 18

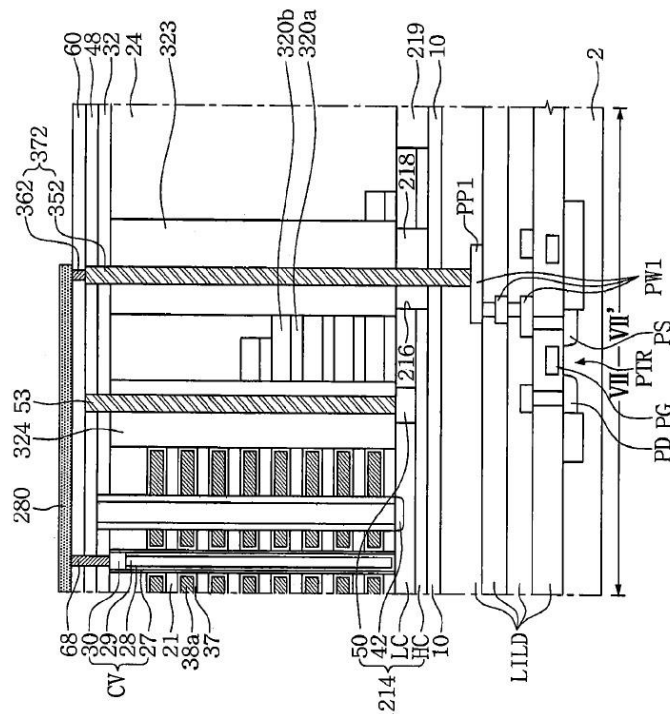


FIG. 19

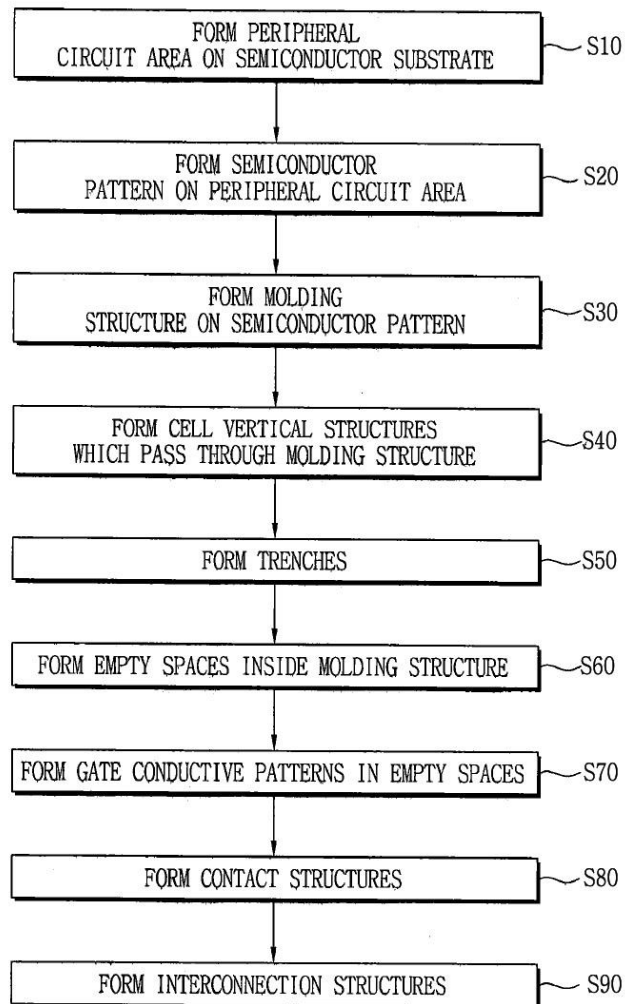


FIG. 20A

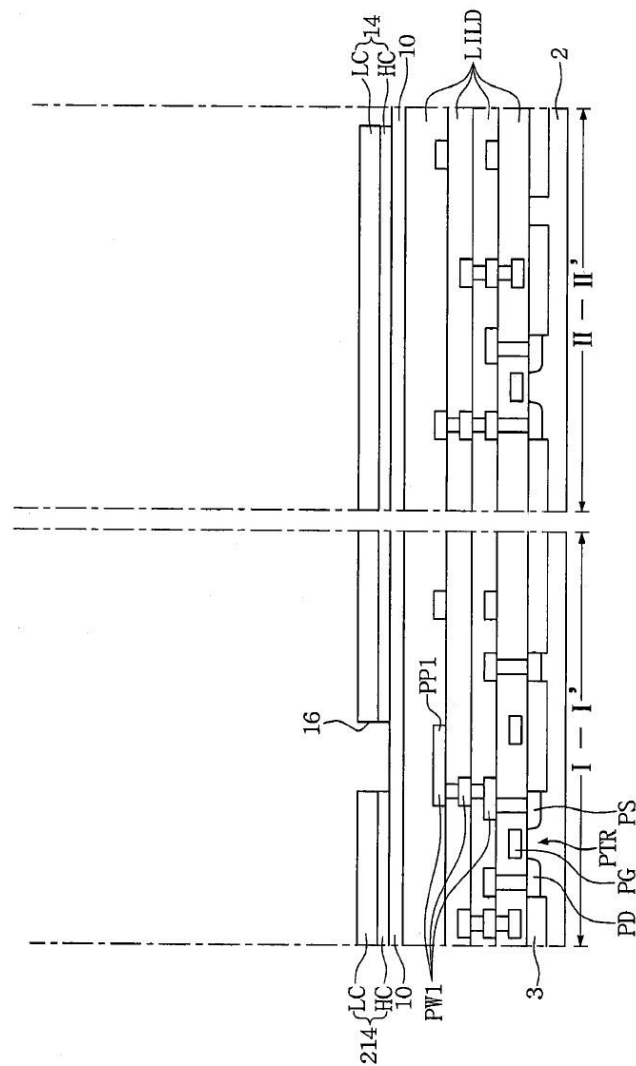


FIG. 20B

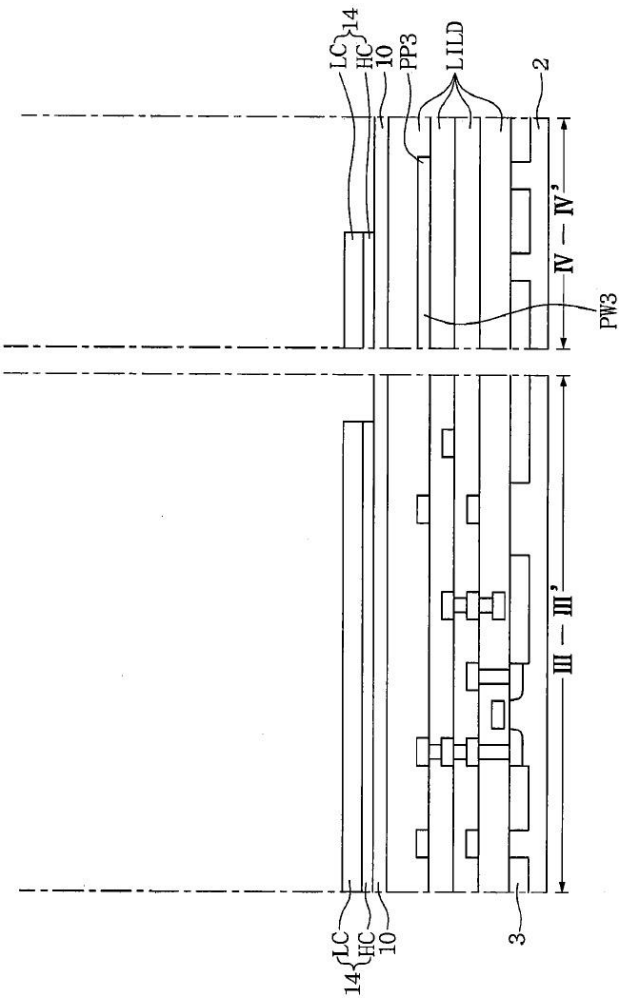


FIG. 21A

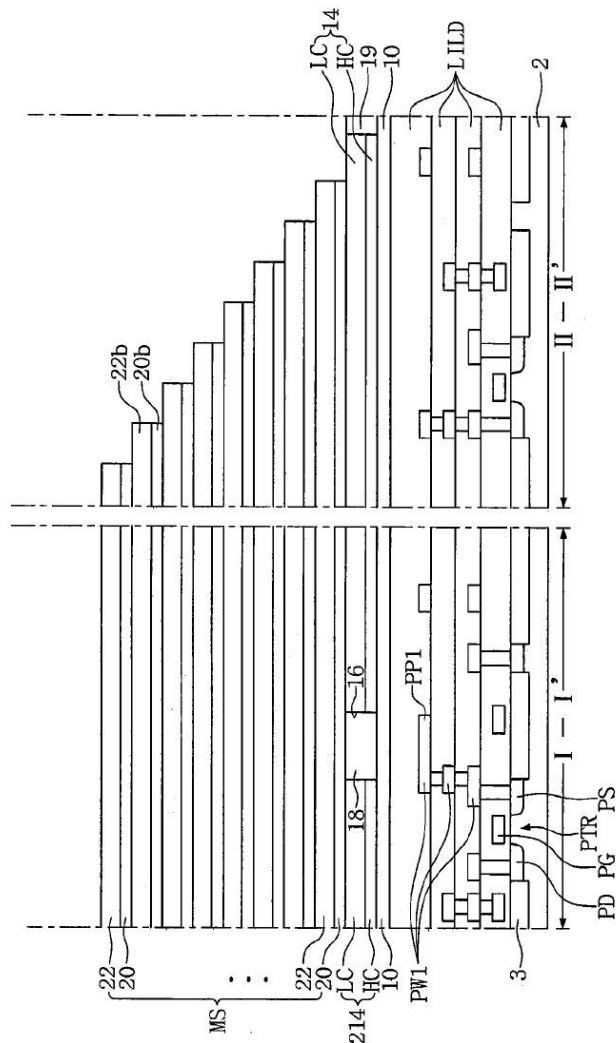


FIG. 21B

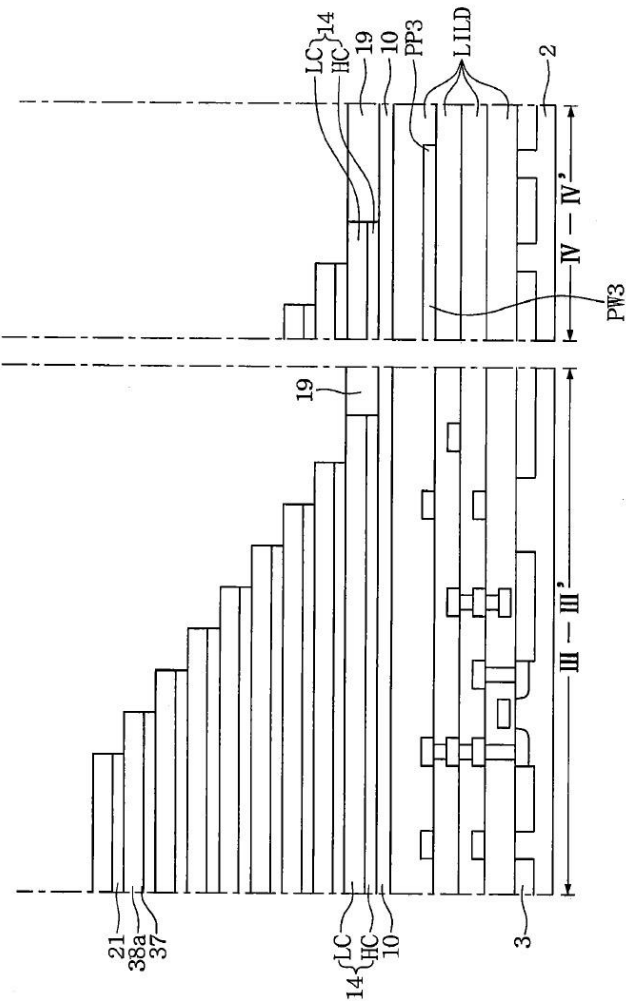


FIG. 22A

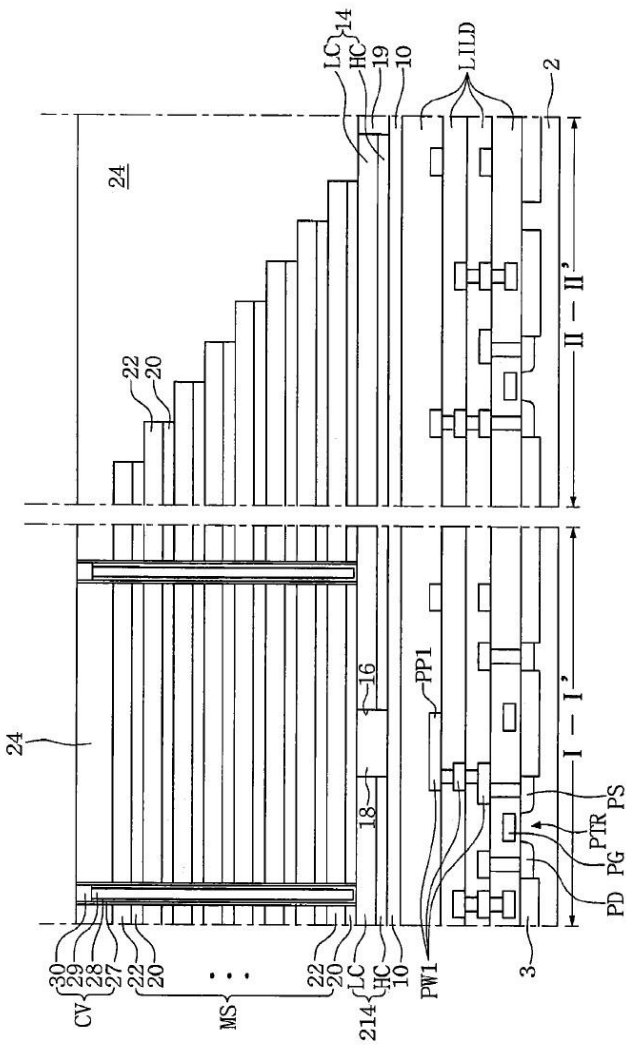


FIG. 22B

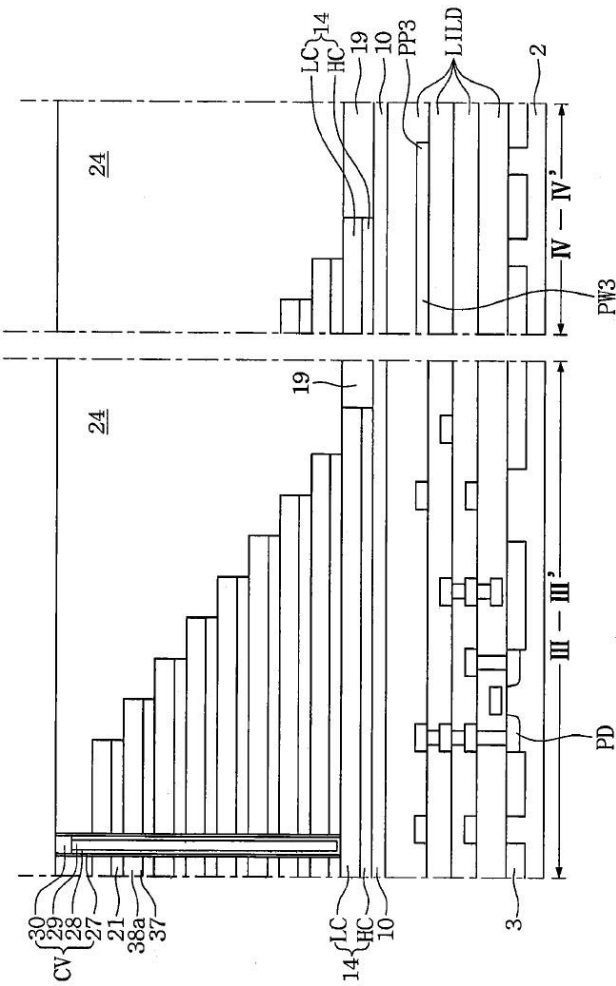


FIG. 23B

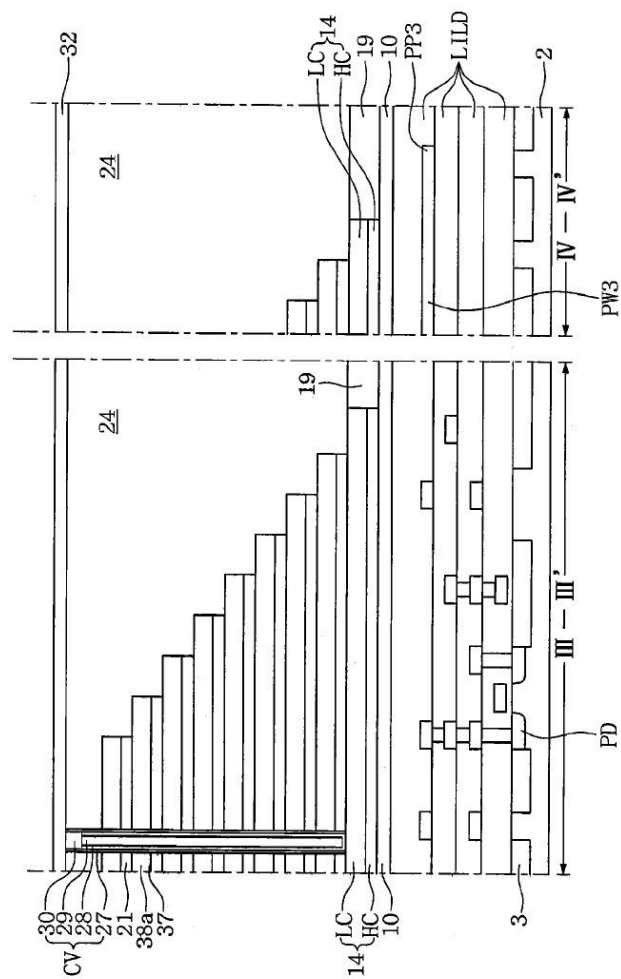


FIG. 24A

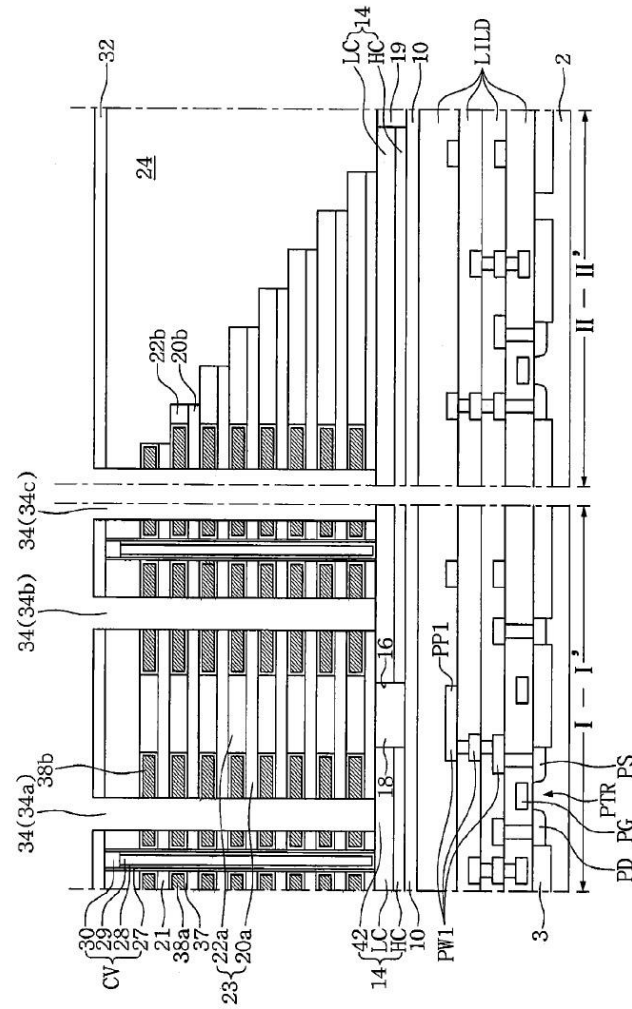


FIG. 24B

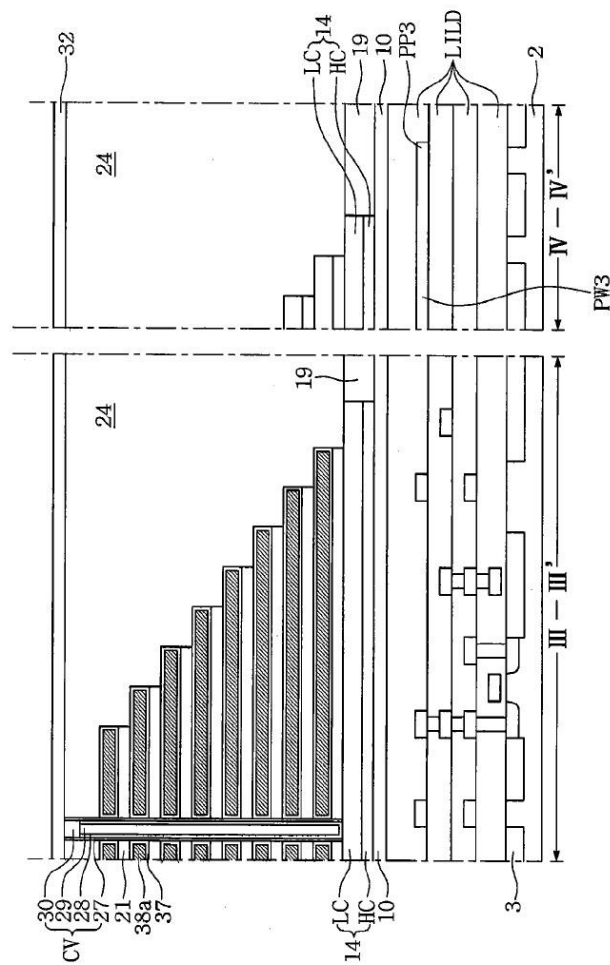


FIG. 25A

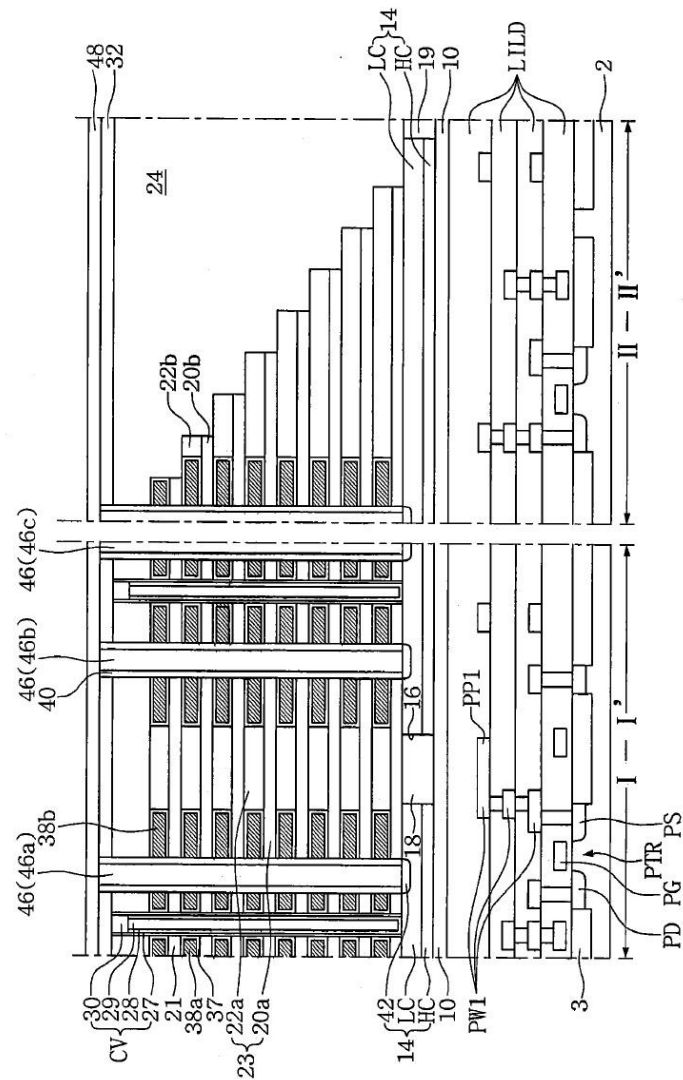


FIG. 25B

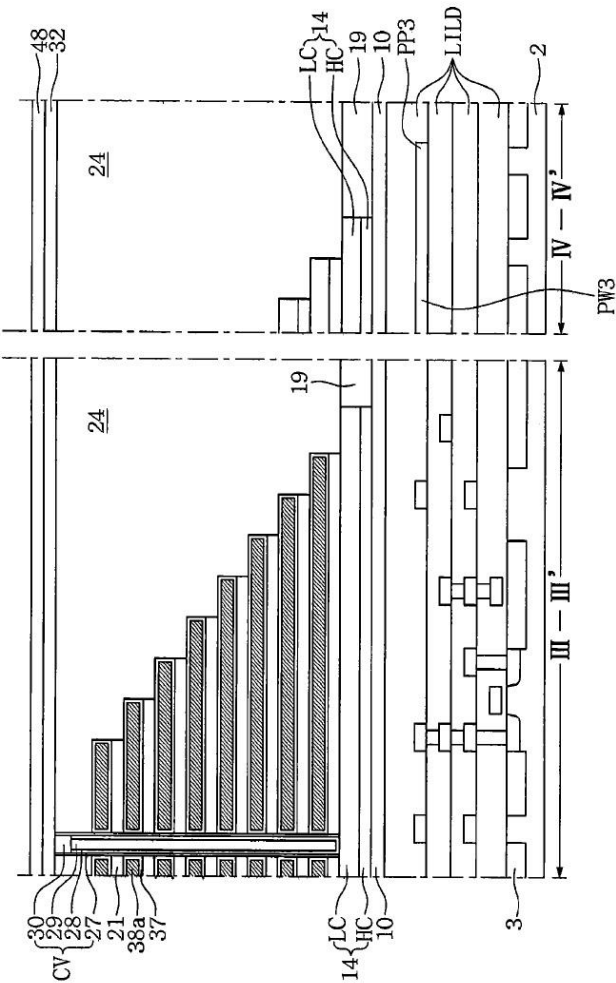


FIG. 26A

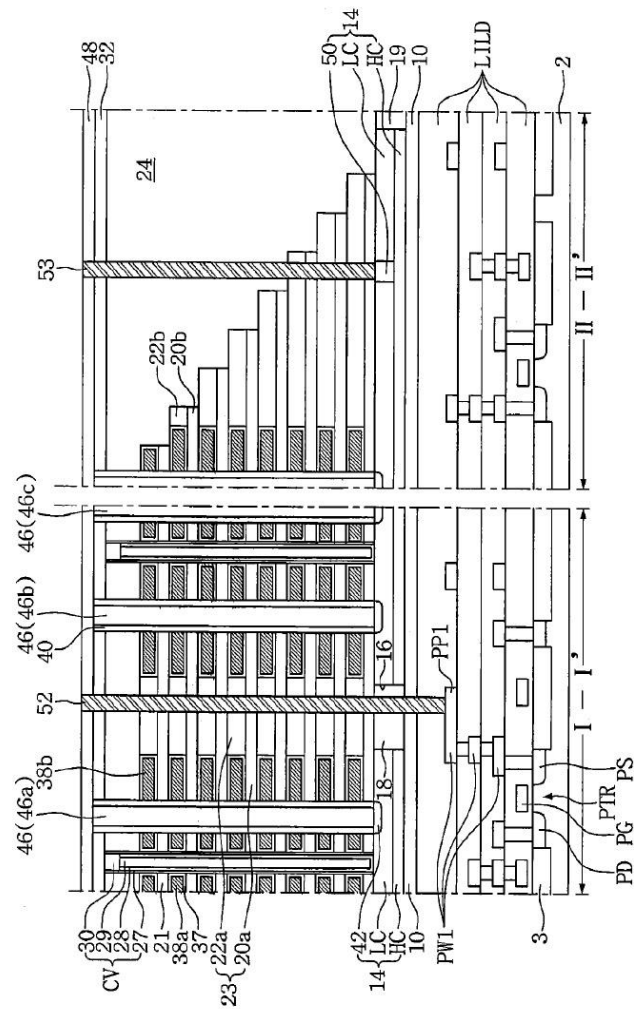


FIG. 26B

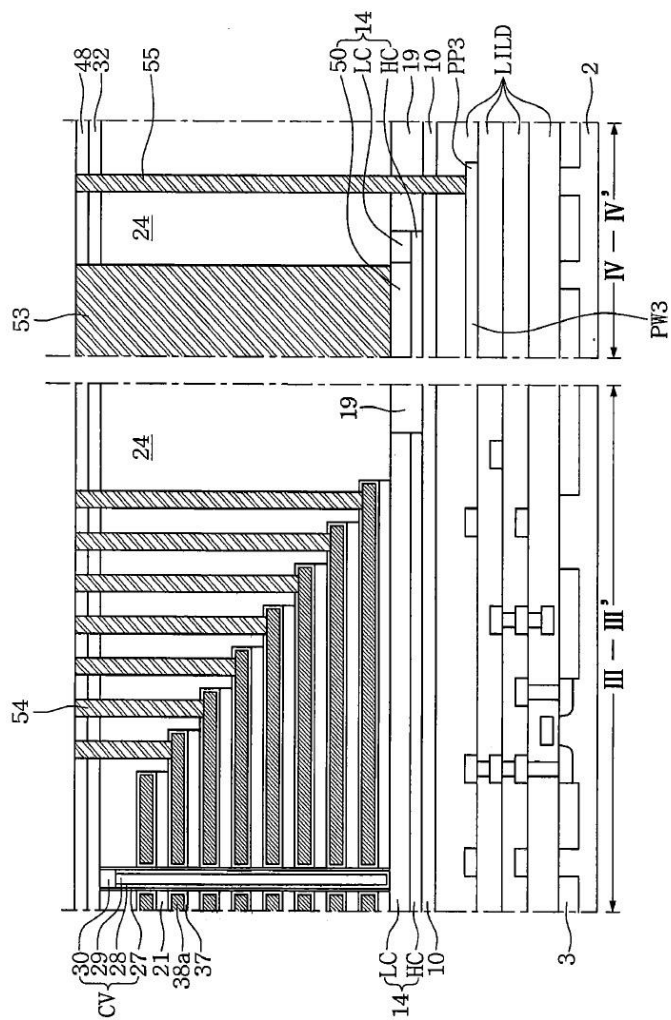
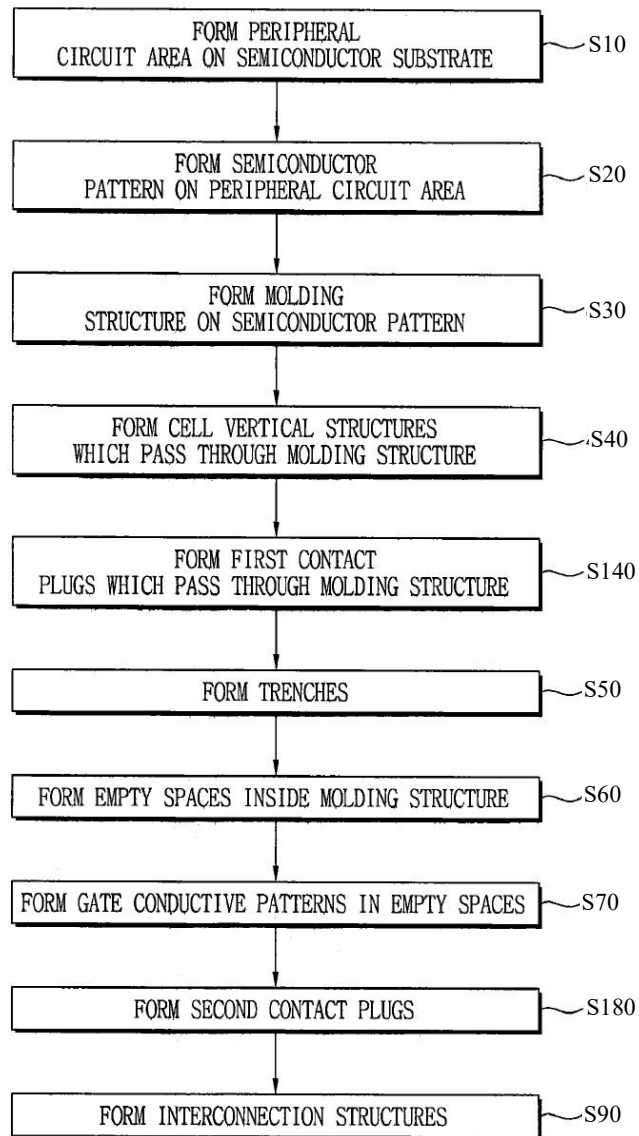


FIG. 27



1

FIG. 28

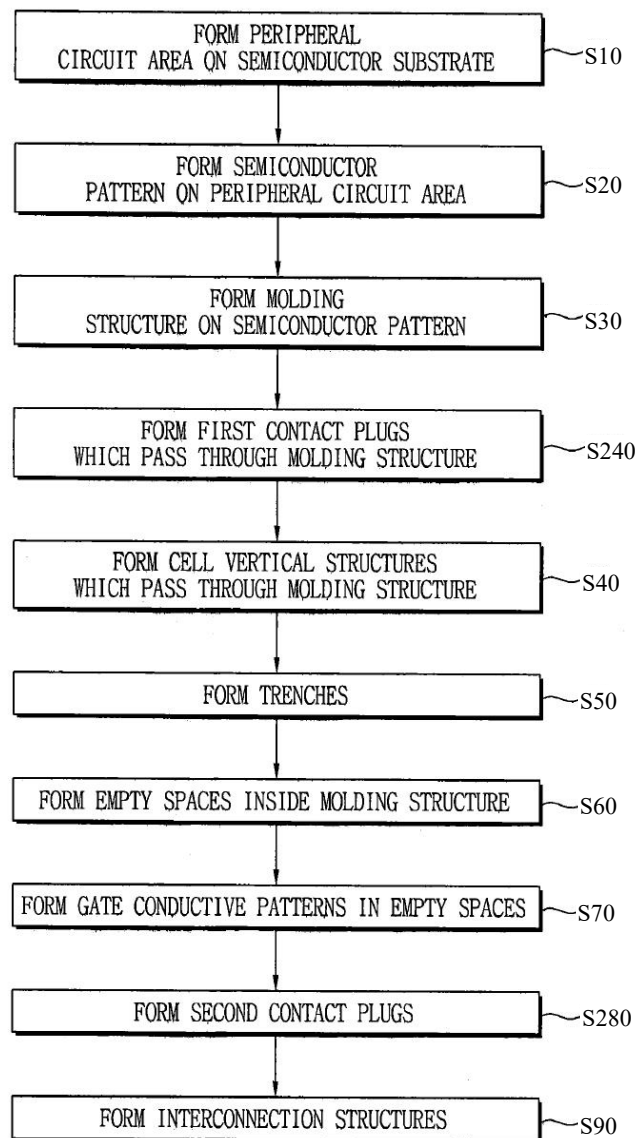


FIG. 29

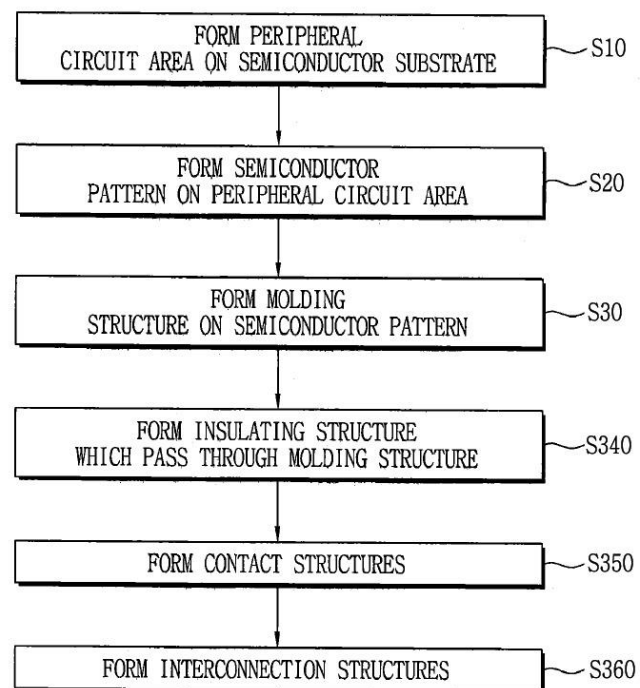


FIG. 30A

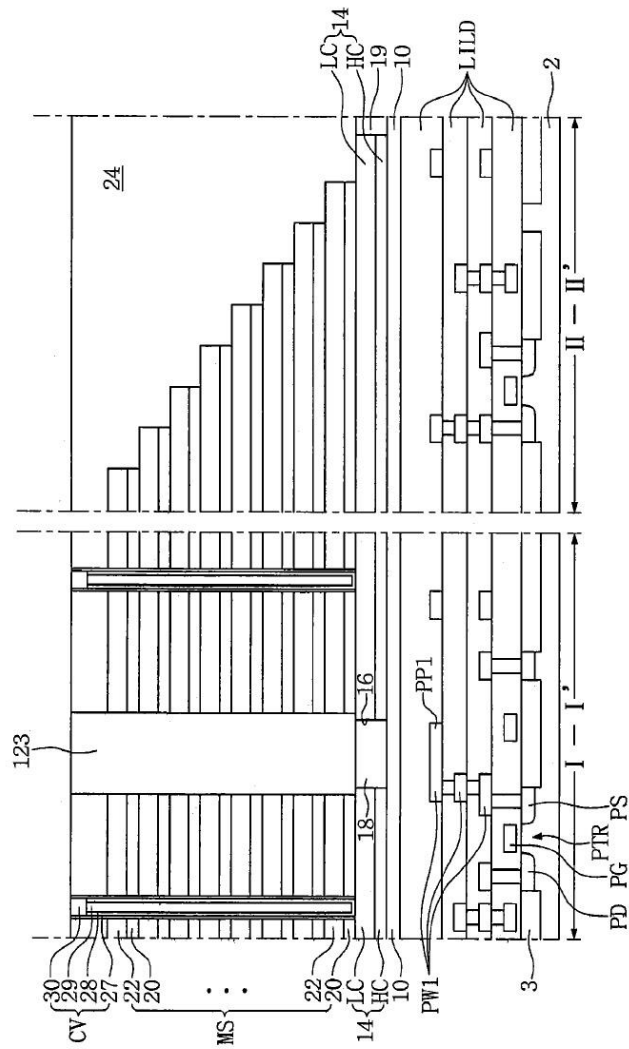


FIG. 30B

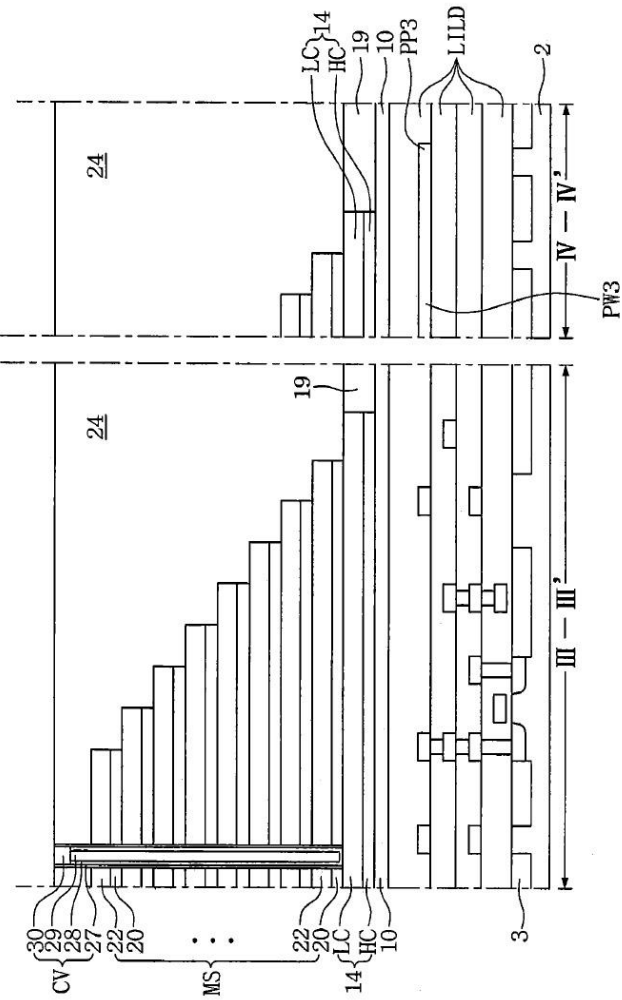


FIG. 31A

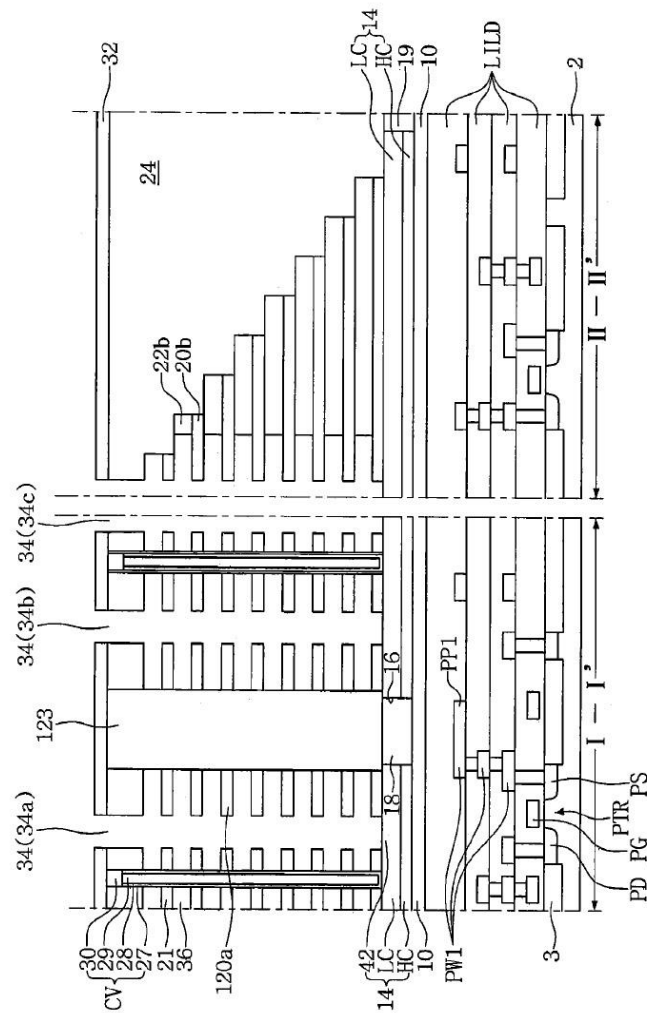


FIG. 31B

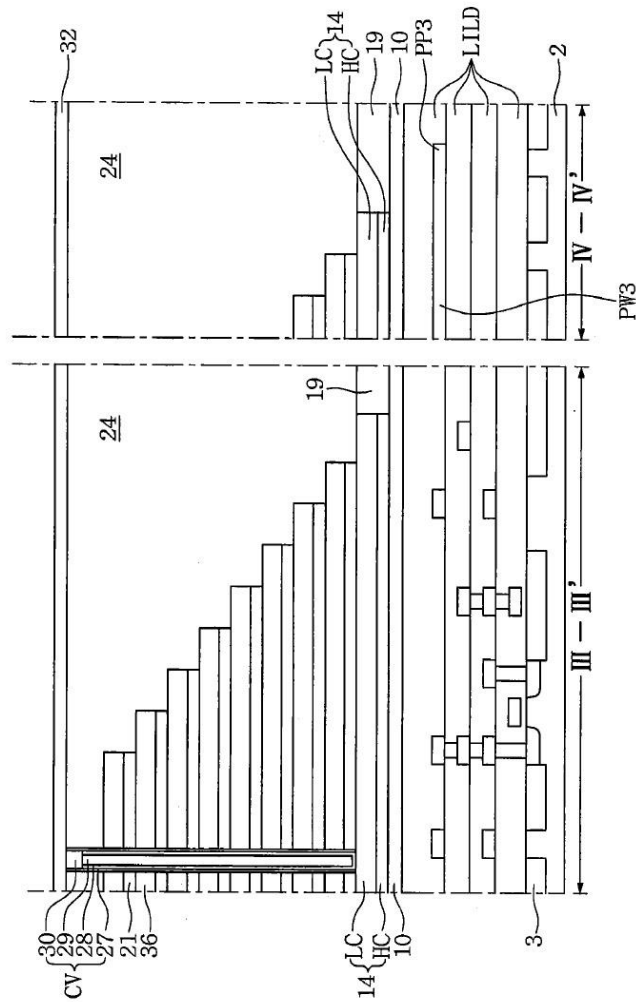


FIG. 32A

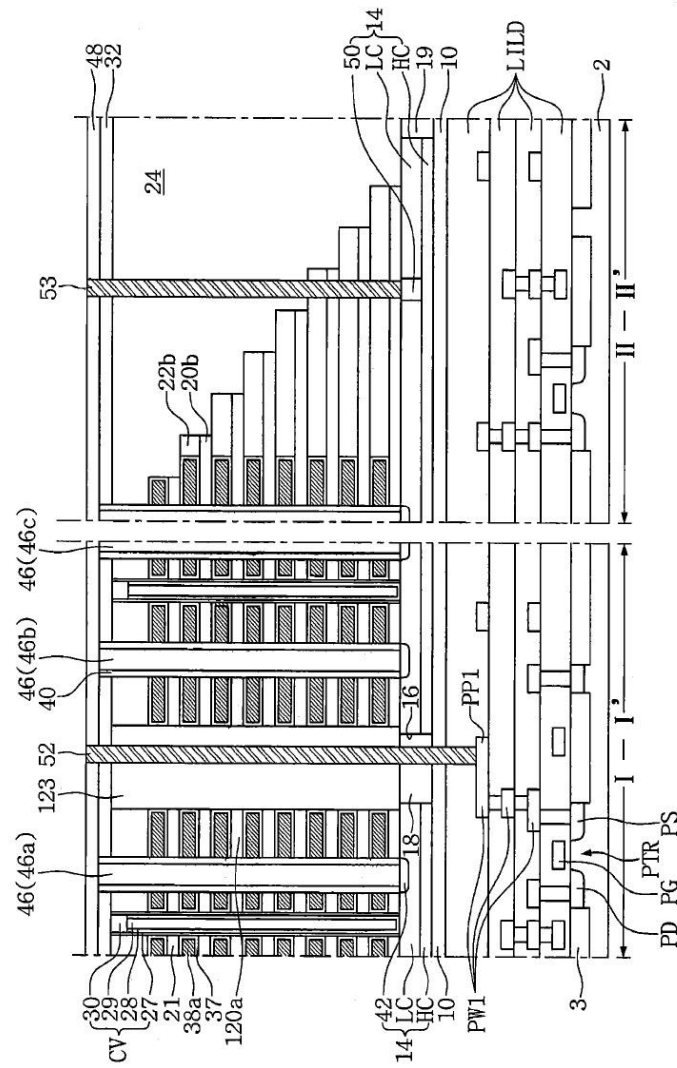


FIG. 32B

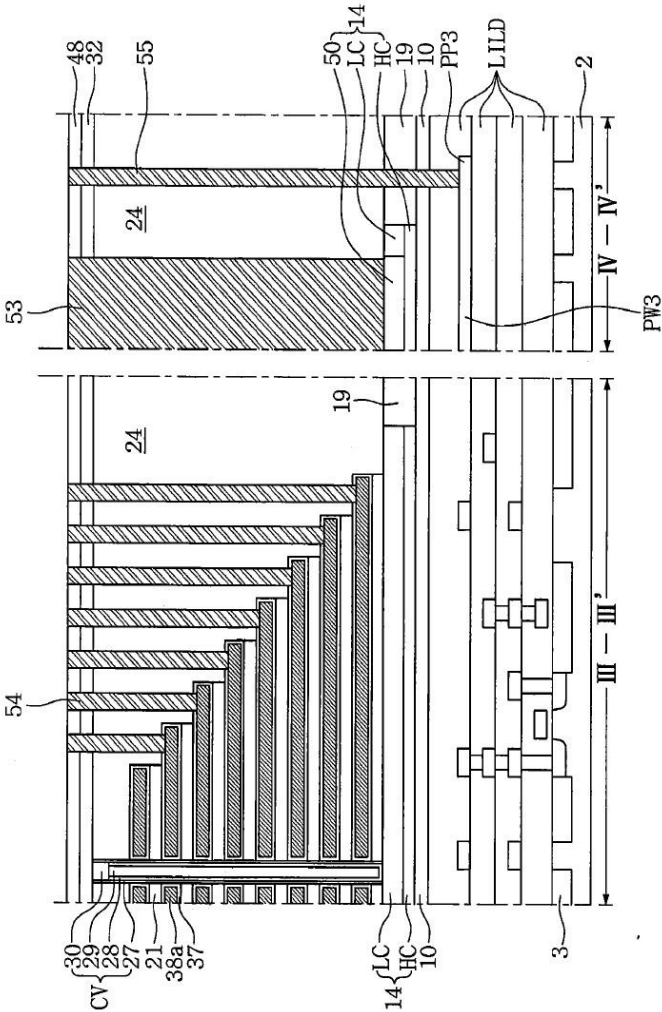


FIG. 33

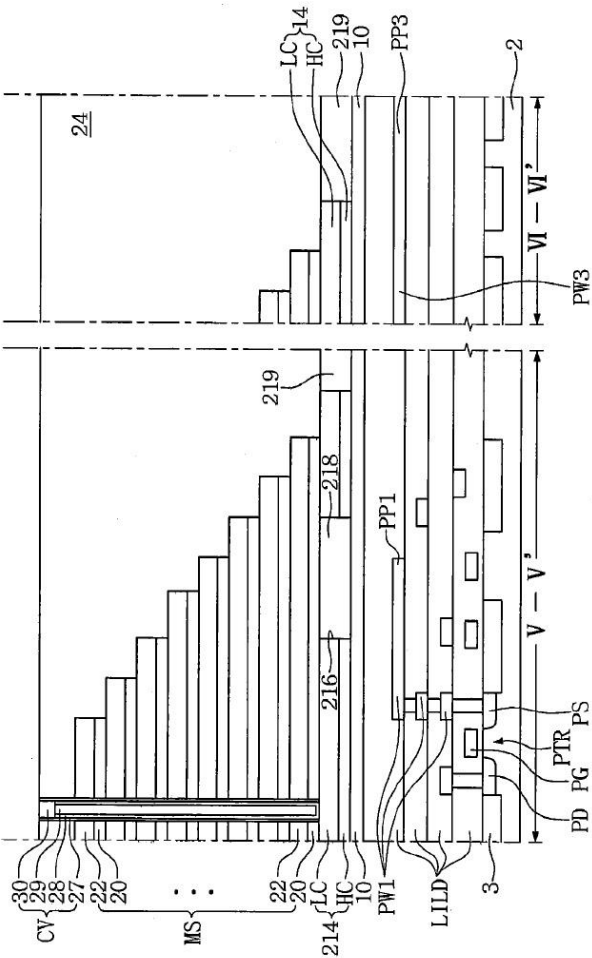


FIG. 34

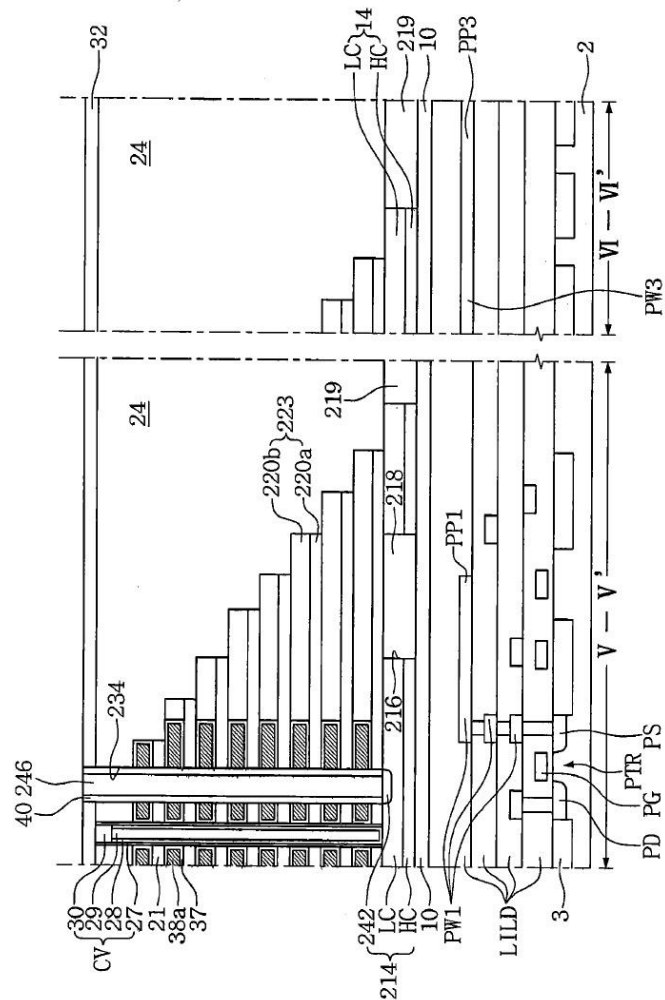


FIG. 35

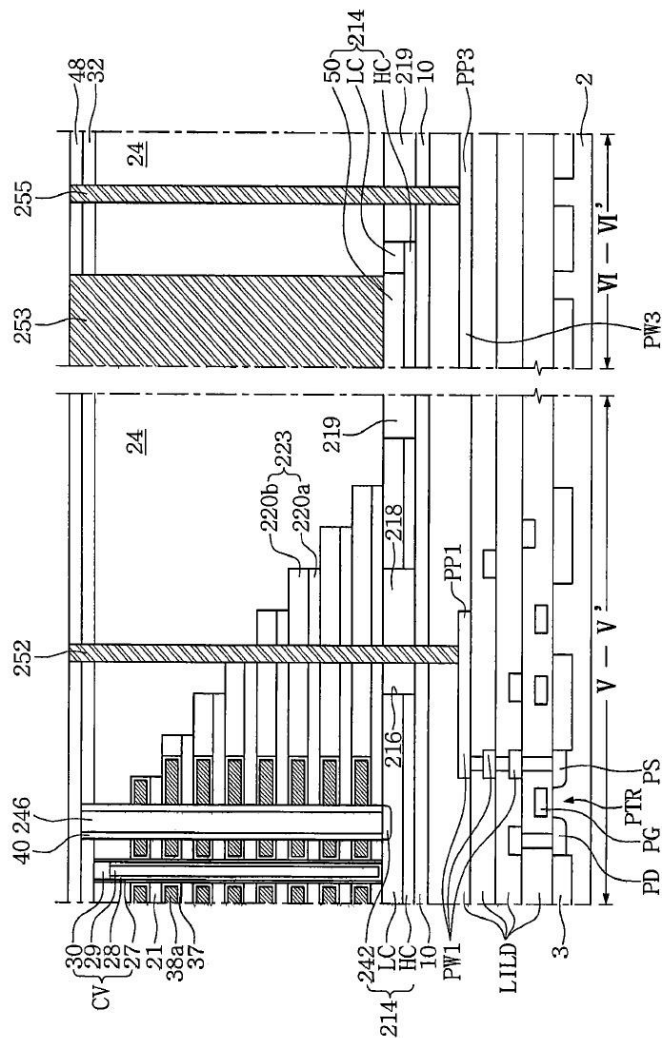


FIG. 36

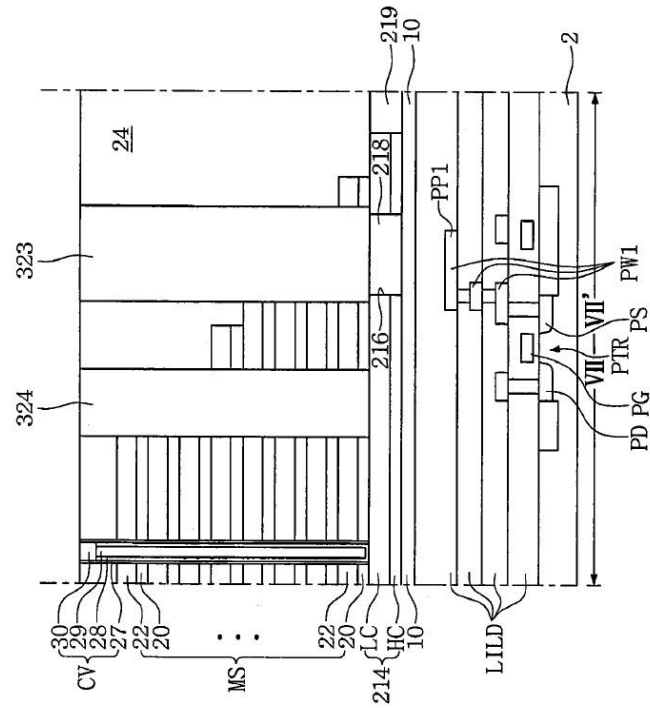


FIG. 37

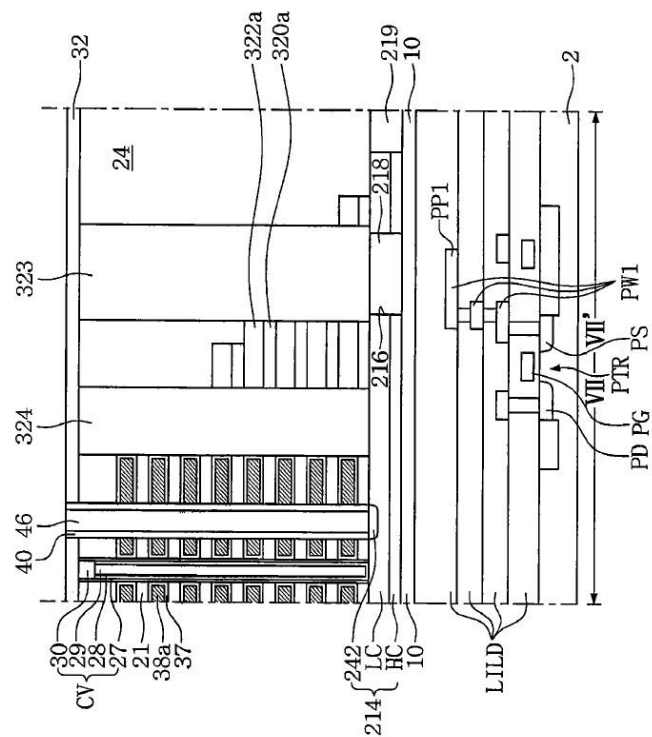


FIG. 38

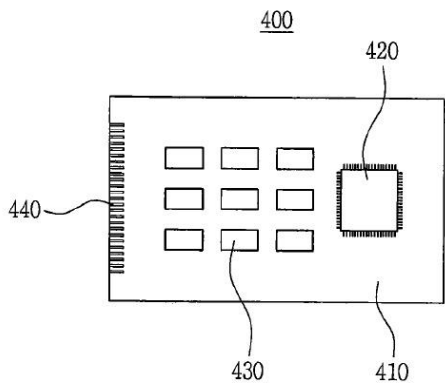


FIG. 39

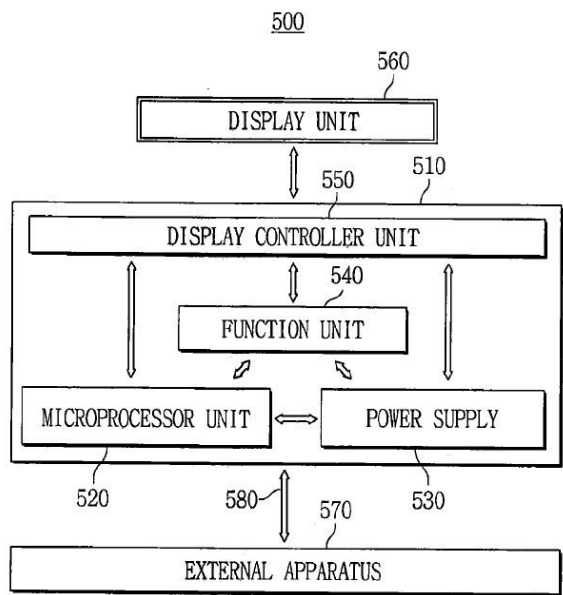


FIG. 40

