

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner

v.

MICRON TECHNOLOGY, INC.

Patent Owner

IPR2025-00501

U.S. PATENT 10,373,974

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 10,373,974

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	MANDATORY NOTICES UNDER 37 C.F.R. § 42.8.....	2
	A. Real Party-in-Interest	2
	B. Related Matters.....	2
	C. Lead and Back-up Counsel and Service Information	3
III.	CERTIFICATION OF GROUNDS FOR STANDING	3
IV.	RELIEF REQUESTED	4
	A. Claims for Which Review Is Requested	4
	B. Statutory Grounds of Challenge.....	4
V.	THE '974 PATENT.....	5
	A. Overview	5
	B. Prosecution History of '974 Patent	8
	C. The Level of Ordinary Skill in the Art.....	9
VI.	CLAIM CONSTRUCTIONS	9
VII.	GROUND 1 AND 2: LEE ANTICIPATES OR OTHERWISE RENDERS OBVIOUS CLAIMS 1, 4, 5, 7, 9, AND 11-19	10
	A. Overview of Lee.....	10
	B. Independent Claim 1	14
	1. Lee discloses a “ <i>microelectronic device comprising</i> ” [1.P].....	14
	2. Lee discloses “ <i>at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising</i> ” [1.a].....	14

3.	Lee discloses “ <i>an array of memory cells in a memory cell region</i> ” [1.a.1].	16
4.	Lee discloses “ <i>stair step structures in at least one stair step region</i> ” [1.a.2].	16
5.	Lee discloses “ <i>conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region</i> ” [1.a.3].	19
6.	Lee discloses “ <i>access lines extending through the at least one memory block.</i> ” [1.a.4].	21
7.	Lee discloses or suggests “ <i>a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region</i> ” [1.a.5].	23
C.	Dependent Claim 4	27
1.	Lee discloses “ <i>at least some of the stair step structures comprise: individual tiers aligned at different vertical levels from one another within a respective stair step structure</i> ” [4.a].	27
2.	Lee discloses or suggests “ <i>contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines</i> ” [4.b].	29
D.	Dependent Claim 5	31
E.	Independent Claim 7	32
1.	Lee discloses a “ <i>method of forming a microelectronic device</i> ” [7.P].	32
2.	Lee discloses or suggests “ <i>forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially</i>	

	<i>between the memory cell region and the stair step region” [7.a].</i>	32
3.	Lee discloses or suggests “ <i>forming an array of memory cells in the memory cell region</i> ” [7.b].	33
4.	Lee discloses “ <i>forming stair step structures in the stair step region</i> ” [7.c].	33
5.	Lee discloses or suggests “ <i>forming conductive vias in the via region</i> ” [7.d].	33
6.	Lee discloses or suggests “ <i>forming access lines extending through the memory block</i> ” [7.e].	34
7.	Lee discloses or suggests “ <i>forming slots extending between adjacent portions of individual access lines within the stair step region</i> ” [7.f].	34
8.	Lee discloses or suggests “ <i>forming a dielectric material within the slots</i> ” [7.g].	35
F.	Dependent Claim 9	35
G.	Dependent Claim 11	36
H.	Dependent Claim 12	38
I.	Dependent Claim 13	43
1.	Lee discloses or suggests “ <i>forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials</i> ” [13.a].	43
2.	Lee discloses or at least suggests “ <i>forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials</i> ” [13.b].	44
J.	Independent Claim 14	45

1.	Lee discloses a “ <i>method of forming a microelectronic device</i> ” [14.P].....	45
2.	Lee discloses or at least suggests “ <i>forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials</i> ” [14.a].	46
3.	Lee discloses or suggests “ <i>forming access lines coupled to memory cells of the array of memory cells</i> ” [14.b].	47
4.	Lee discloses or suggests “ <i>forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack</i> ” [14.c].	48
5.	Lee discloses or suggests “ <i>forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines</i> ” [14.d].	49
6.	Lee discloses or suggests “ <i>removing at least a portion of the stair step structures using at least one chop mask</i> ” [14.e].	50
K.	Dependent Claims 15, 16, and 18	50
L.	Dependent Claim 17	54
M.	Dependent Claim 19	55
VIII.	GROUND 3: LEE IN VIEW OF FREEMAN RENDERS OBVIOUS CLAIMS 12 AND 14-19	56
A.	Overview of Freeman.....	56
B.	Reasons to Combine Lee and Freeman.....	60
C.	Independent Claim 14 and Dependent Claims 12, 15, 16, 18, and 19	66

D.	Dependent Claim 17	66
1.	Lee in view of Freeman renders obvious “ <i>forming the stair step mask over the stack while exposing a width of a first step</i> ” [17.a].	66
2.	Lee in view of Freeman renders obvious “ <i>removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask</i> ” [17.b].	67
3.	Lee in view of Freeman renders obvious “ <i>recessing an edge of the stair step mask to expose a width of a second step</i> ” [17.c].	67
4.	Lee in view of Freeman renders obvious “ <i>removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask</i> ” [17.d].	68
IX.	GROUND 4: LEE IN VIEW OF LIM RENDERS OBVIOUS CLAIM 13	68
A.	Overview of Lim	68
B.	Reasons to Combine Lee and Lim	74
1.	The teaching, suggestion, and motivation in Lee and Lim would have led a POSITA to apply Lim’s partial gate replacement process to form Lee’s contact plugs in the remaining alternating dielectric stack.	74
2.	A POSITA would have a reasonable expectation of success in applying Lim’s known partial gate replacement technique to Lee’s fabrication process to form Lee’s contact plugs in an alternating dielectric stack.....	76
C.	Dependent Claim 13	78
X.	DISCRETIONARY DENIAL DOES NOT APPLY.....	79

A.	35 U.S.C. § 325(d).....	79
B.	35 U.S.C. § 314(a).....	81
XI.	CONCLUSION.....	82

LIST OF EXHIBITS

Exhibit	Description
EX1001	U.S. Patent No. 10,373,974 to Freeman <i>et al.</i>
EX1002	Prosecution History of U.S. Patent No. 10,373,974
EX1003	Declaration of Dr. Mariusz Orlowski
EX1004	U.S. Patent Application Publication No. 2016/0322376 in the Name of Lee
EX1005	U.S. Patent Application Publication No. 2012/0306089 in the Name of Freeman <i>et al.</i>
EX1006	U.S. Patent Application Publication No. 2016/0163732 in the Name of Lim <i>et al.</i>
EX1007	Korean Patent Application No. 10-2014-0176089
EX1008	Certified English Translation of Korean Patent Application No. 10-2014-0176089
EX1009	U.S. Patent Application Publication No. 2015/0129878 in the Name of Shin <i>et al.</i>
EX1010	U.S. Patent Application Publication No. 2010/0133598 in the Name of Chae <i>et al.</i>
EX1011	U.S. Patent Application Publication No. 2015/0137216 in the Name of Lee <i>et al.</i>
EX1012	“Adjacent” – Merriam-Webster Online Dictionary 2015, Retrieved September 12, 2015, from https://web.archive.org/web/20150912031420/https://www.merriam-webster.com/dictionary/adjacent
EX1013	U.S. Patent Application Publication No. 2015/0279852 in the Name of Mizutani <i>et al.</i>
EX1014	J. Jang <i>et al.</i> , “Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193
EX1015	Y. Noh <i>et al.</i> , “A New Metal Control Gate Last process (MCGL process) for High Performance DC-SF (Dual Control Gate with Surrounding Floating Gate) 3D NAND Flash Memory,” 2012 Symposium on VLSI Technology (VLSIT), Honolulu, HI, USA, 2012, pp. 19-20
EX1016	U.S. Patent Application Publication No. 2014/0138840 in the Name of

Exhibit	Description
	Ha <i>et al.</i>
EX1017	U.S. Patent Application Publication No. 2009/0310415 in the Name of Jin <i>et al.</i>
EX1018	U.S. Patent Application Publication No. 2016/0218059 in the Name of Nakada <i>et al.</i>
EX1019	U.S. Patent Application Publication No. 2016/0365351 in the Name of Nishikawa <i>et al.</i>
EX1020	R. Muller <i>et al.</i> , “Device Electronics for Integrated Circuits,” 3rd Edition, John Wiley & Sons, 2003, pp. 97-99
EX1021	Defendant’s Answer To First Amended Complaint And Counterclaims, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 35 (N.D. Cal. February 16, 2024)
EX1022	Order Granting Motion To Dismiss Counterclaims, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 78 (N.D. Cal. July 16, 2024)
EX1023	Defendant’s First Amended Counterclaims, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 93 (N.D. Cal. August 1, 2024)
EX1024	Defendant’s Unopposed Motion To Modify The Case Schedule To Permit Defendant To Reassert Counterclaims, <i>Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC.</i> , No. 3:23-cv-05792-RFL, D.I. 213 (N.D. Cal. January 29, 2025)

All citations to 35 U.S.C. §§ 102 and 103 in this paper refer to the AIA statutes.

All emphases in quotations are added unless otherwise noted.

Direct quotations of claim language are italicized.

This paper includes color illustrations and should be viewed in color.

I. INTRODUCTION

Yangtze Memory Technologies Company, Ltd. (“Petitioner”) petitions for *inter partes* review (“IPR”) of claims 1, 4, 5, 7, 9, and 11-19 (“challenged claims”) of U.S. Patent No. 10,373,974 (“’974 patent,” EX1001) assigned to Micron Technology, Inc. (“PO”).

The challenged claims pertain to well-known three-dimensional (3D) memory device structure and manufacturing. The purported novelty of the ’974 patent—a technique for forming through-array vias (TAVs) through existing dielectric materials—is not recited in independent claims or any challenged claims and is, in any case, disclosed by the prior art. Instead, the challenged claims merely recite well-known features in the design and manufacture of 3D memory devices, such as the conventional usage of TAVs to interconnect under-array circuits and forming stair-step structures with stair-step masks and chop masks. All of these claimed subject matters were well-documented and already widely recognized in the industry at the time of ’974 patent, which was also evidenced by PO’s self-admitted prior art cited throughout ’974 patent. In some instances, the challenged claims simply paraphrase the descriptions of prior art included in the patent itself.

Petitioner further demonstrates in Grounds 1 and 2 that, under any reasonable claim interpretation, all challenged claims are anticipated, or otherwise rendered obvious, by U.S. Patent Application Publication No. 2016/0322376 in the name of

Lee (“Lee,” EX1004). Additionally, two other prior art references—U.S. Patent Application Publication No. 2012/0306089 in the name of Freeman *et al.* (“Freeman,” EX1005) and U.S. Patent Application Publication No. 2016/0163732 in the name of Lim *et al.* (“Lim,” EX1006)—are combined with Lee in Grounds 3 and 4, supplementing Lee with more express and detailed teachings for some claim limitations for the sake of thoroughness.

Petitioner’s expert, Dr. Mariusz Orlowski, who has over 40 years of experience in the semiconductors industry, confirms that the challenged claims are unpatentable over these references.

Petitioner thus respectfully requests the Board cancel the challenged claims.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

A. Real Party-in-Interest

The real parties-in-interest are Yangtze Memory Technologies Company, Ltd. and Yangtze Memory Technologies, Inc.

B. Related Matters

The ’974 patent is not currently asserted in any pending civil action. In *Yangtze Memory Technologies Co. Ltd. v. Micron Technology, Inc. et al.*, No. 3:23-cv-05792-RFL (N.D. Cal.) (“NDCA case”), however, PO has filed an unopposed

motion for leave to amend its counterclaims to assert '974 patent in the NDCA case.¹

That motion remains pending.

C. Lead and Back-up Counsel and Service Information

Petitioner identifies the following lead and back-up counsels:

Lead Counsel	Back-up Counsel
Zhiwei (Wayne) Zou (Reg. No. 66,041) wayne.zou@bayes.law Bayes PLLC 8260 Greensboro Drive, Suite 625 McLean, VA 22102 Tel: 703-995-9887 Fax: 703-821-8128	Andrew Landers Ramos (Reg. No. 76,865) andrew.ramos@bayes.law Bayes PLLC 8260 Greensboro Drive, Suite 625 McLean, VA 22102 Tel: 703-995-9887 Fax: 703-821-8128 Jiayu (Mandy) Song (Reg. No. 69,583) mandy.song@bayes.law Bayes PLLC 8260 Greensboro Drive, Suite 625 McLean, VA 22102 Tel: 703-995-9887 Fax: 703-821-8128

Petitioner consents to electronic service at YMTC-Micron-IPR@bayes.law, as well as the above email addresses.

III. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that '974 patent is available

¹ The '974 patent was initially included in PO's February 16, 2024 Answer and Counterclaim, but the Court dismissed it under FRCP 12(b)(6), with leave to amend. EX1021-EX1022. Rather than amending the pleadings, PO chose to drop '974 patent on August 1, 2024. EX1023. Months later, PO now seeks to reassert '974 patent. EX1024.

for IPR, and Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified in this Petition.

IV. RELIEF REQUESTED

Under 35 U.S.C. § 311, Petitioner requests IPR of claims 1, 4, 5, 7, 9, and 11-19 of '974 patent.

A. Claims for Which Review Is Requested

Petitioner requests IPR and cancellation of challenged claims 1, 4, 5, 7, 9, and 11-19 of '974 patent under 35 U.S.C. § 311 based on the following grounds. This Petition is supported by the Declaration of Dr. Mariusz Orlowski ("Orlowski Decl.," EX1003).

B. Statutory Grounds of Challenge

Petitioner relies on the following prior art and statutory grounds of challenge to the challenged claims:

Name	Ex.	Publication No.	Filed²	Published	Prior art under at least
Lee	1004	US2016/0322376	10/2/2015	11/3/2016	§ 102(a)(2)
Freeman	1005	US2012/0306089	6/2/2011	12/6/2012	§ 102(a)(1)
Lim	1006	US2016/0163732	12/9/2014	6/9/2016	§ 102(a)(2)

² In this IPR, Petitioner relies on the filing date of Korean Application No. 10-2014-0176089 (EX1007), to which Lim has a right to claim priority as its effective filing date, to be eligible as prior art under 35 U.S.C. § 102(a)(2) with respect to the subject matter relied on herein. A certified English translation of Korean Application No. 10-2014-0176089 is submitted herewith (EX1008). For Lee, its U.S. filing date is early enough to be eligible as prior art under 35 U.S.C. § 102(a)(2). Petitioner preserves the right to use Lee's foreign priority date as its effective filing date if needed.

Ground	Claims	Basis	References
1 & 2	1, 4, 5, 7, 9, and 11-19	§§ 102/103	Lee
3	12 and 14-19	§ 103	Lee in view of Freeman
4	13	§ 103	Lee in view of Lim

Freeman qualifies as prior art under 35 U.S.C. § 102(a)(1) as it was published before the earliest possible effective filing date of '974 patent, November 16, 2015. Each of Lee and Lim names another inventor and was effectively filed before November 16, 2015, and therefore qualifies as prior art under 35 U.S.C. § 102(a)(2).

V. THE '974 PATENT

A. Overview

The '974 patent is directed to semiconductor devices, in particular, having vertical memory blocks with slots and conductive TAVs. EX1001, 1:17-22. The '974 patent purportedly “develop[s] improved structures and methods of forming vertical memory arrays with through-array vias for semiconductor devices (*e.g.*, vertical memory devices, such as NAND Flash memory devices) that reduce the number and complexity of additional processing acts practiced in conventional methods and structures.” EX1001, 2:8-14. The '974 patent contends “the methods described herein enable the formation of through-array vias 120 without the need for removing conductive material 116 and other portions of the vertical memory block 100 in a separate material removal act to form the conductive vias 120.” EX1001, 12:57-61.

Annotated FIG. 1 of '974 patent below represents the claimed invention related to a memory block 100 having a memory array region 102 (in blue dashed box) in the middle, two stair step regions 104 (in red dashed boxes) at both ends, and two via regions 106 (in black dashed boxes) between memory array region 102 and stair step regions 104, respectively. EX1001, 4:19-26; EX1003, ¶76.

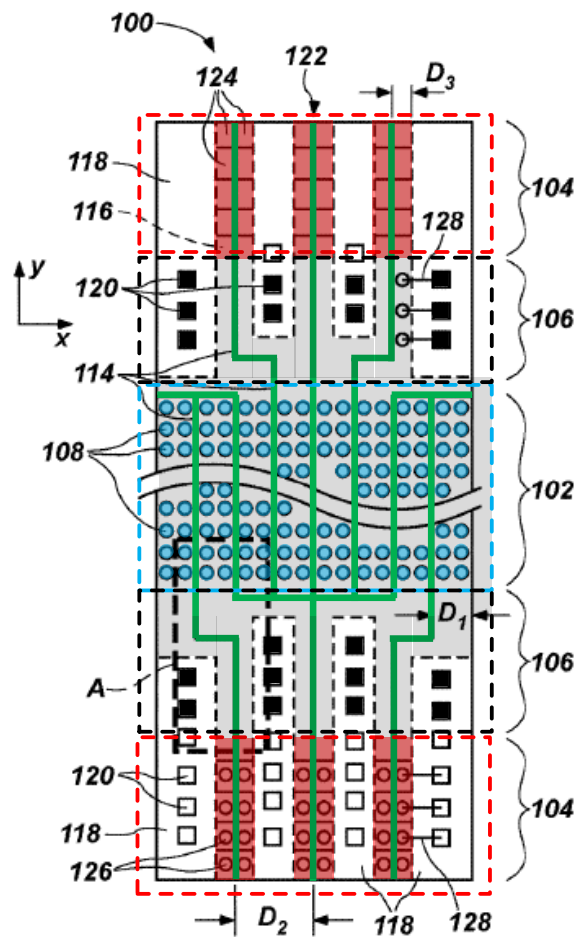


FIG. 1
EX1003 — FIG. L

As shown in annotated FIG. 1, slots 114 (in green), filled with a dielectric material (e.g., silicon oxide), “may extend through the memory array region 102

proximate to and between adjacent memory cell pillars 108” and “may vertically extend through a stack of alternating conductive word lines 116 and first dielectric materials 132.” EX1001, 4:37-40; 6:13-15, FIG. 3. Further, conductive word lines 116 (in gray) “may extend along the slots 114 and be coupled to the memory cell pillars 108” to form memory cells with memory cell pillars 108. EX1001, 4:57-65.

As shown in annotated FIG. 1 above, adjacent conductive word lines 116 in the x-direction are split by slots 114, and conductive word lines 116 and slots 114 both extend further from memory array region 102 into via regions 106 and stair step regions 104. EX1001, 5:57-61; EX1003, ¶78.

In memory array region 102, an array of memory cell pillars 108 (in blue) “may each extend vertically through the vertical memory block 100.” EX1001, 4:30-32. In each via region 106, conductive vias 120 (in black), “also referred to as ‘through-array vias’ or ‘TAVs,’” “may extend through the vertical memory block 100 within the dielectric stacks 118.” EX1001, 5:14-21. “For example, at least one of the conductive vias 120 may operatively couple the sub-array circuitry 136 to the vertical memory block 100.” EX1001, 6:52-54, FIG. 3. In each stair step region 104, one or more stair step structures 122 (in red) are formed “for electrically contacting and accessing different overlapping conductive word lines 116” and “may include contact regions 124 (*e.g.*, ‘stairs’) ... arranged like a staircase.” EX1001, 5:27-33.

In another embodiment described in connection with FIGs. 7 and 8, ’974

patent further discloses an additional slot 514A that further splits a conductive layer 516 in the stair step region. EX1001, 9:5-15; FIGs. 7-8.

The '974 patent notably includes various instances of Applicant-Admitted Prior Art ("AAPA"). In one instance, in its Background section, '974 patent explicitly acknowledges that the process of forming "alternating layers of the first dielectric material and the conductive word line plates" was "**conventional**" at that time (referred to herein as "AAPA-1"). EX1001, 1:43-59. This process was widely recognized by a POSITA as "gate replacement." EX1014, FIG. 3; EX1015, FIG. 2; EX1003, ¶83.

In another instance, '974 patent provides detailed descriptions of forming stair step structures using the "stair step mask" and "chop masks," characterizing those processes as "**known by those of ordinary skill in the art**" (referred to herein as "AAPA-2"). EX1001, 9:30-10:11, 12:36-39. AAPA-2 encompasses the "trim-etch" process for creating consecutive steps with the "stair step mask," as well as the "chopping" process with the "chop masks," both of which are well-known techniques to a POSITA. EX1016, FIGs. 8A-8L, [0069]-[0077]; EX1017, FIGs. 6A-8B, [0036]-[0041]; EX1003, ¶¶84-88.

B. Prosecution History of '974 Patent

In the first Office Action, the Examiner rejected issued claims 1-20 of '974 patent on the ground of nonstatutory double patenting over U.S. Patent Nos.

9,728,548 and 10,062,708 (collectively “parent patents”). EX1002, 66-68. The Examiner also indicated allowable subject matter in independent claims 1, 7, and 14, noting that the prior art on the record failed to teach, with emphasis in italics, the claim limitations related to “*stair step structures*,” “*conductive vias*,” and “*a dielectric material within slots*.” EX1002, 68-69. In response, PO filed a terminal disclaimer against the parent patents without presenting arguments on the merits. EX1002, 56.

The Examiner subsequently issued a Notice of Allowance. EX1002, 39.

C. The Level of Ordinary Skill in the Art

A person of ordinary skill in the art (POSITA) at the time of the claimed invention would have had a Bachelor’s degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. EX1003, ¶21. A higher level of education might make up for less experience, and vice versa. EX1003, ¶21.

VI. CLAIM CONSTRUCTIONS

Claim terms subject to IPR are construed using *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005). 37 C.F.R. § 42.100(b). Only terms necessary to resolve the controversy need construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). For all claim limitations, because the prior art relied on herein discloses embodiments indisputably within the

claims' scope, the Board need not construe the claims' outer bounds, and all claim terms should be construed according to their plain and ordinary meaning.

**VII. GROUNDS 1 AND 2: LEE ANTICIPATES OR OTHERWISE
RENDERS OBVIOUS CLAIMS 1, 4, 5, 7, 9, AND 11-19**

A. Overview of Lee

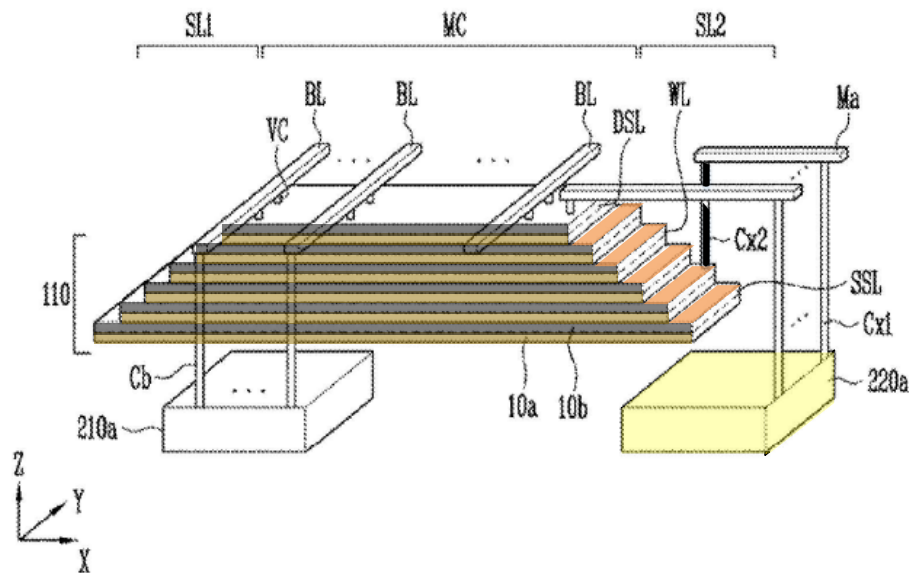
Lee relates to 3D semiconductor devices. EX1004, [0003]. Lee aims to simplify the manufacturing process and reduce the costs and sizes of the semiconductor devices. EX1004, [0009], [0011].

Specifically, FIGs. 1 and 2 show a semiconductor device 1000 including a memory cell array 100 having memory blocks 110 and a peripheral circuit 200. EX1004, [0028]. Peripheral circuit 200 is configured to perform operations of memory cell array 100, with certain circuits including row decoders 220a and 220b, disposed under memory cell array 100 to “decrease a size of the semiconductor device 1000.” EX1004, [0029]-[0031].

As illustrated in annotated FIG. 4 below, which illustrates region 100a of FIG. 2, memory cell array 100 includes three regions in the X-direction: a memory region MC in the middle where vertical channel layers VC (parts of memory cell strings, FIG. 3) are formed, and two slimming regions SL1 and SL2 on opposite ends. EX1004, [0034], [0036], [0045]; EX1003, ¶¶96-97. In the Z-direction, memory cell array 100 includes a stack of alternating insulating layers 10a (in brown) and

conductive layers 10b (in gray). EX1004, [0046]; EX1003, ¶98. Conductive layers 10b form source select lines SSL, word lines WL, and drain select lines DSL, which “are located in the memory region MC and extend in the X-direction hav[ing] step forms in the first slimming region SL1 and the second slimming region SL2.” EX1004, [0045]-[0046]. In a step structure of second slimming region SL2, contact plugs Cx2 (in black) are formed on the exposed ends (in orange) of gate lines SSL, WL, and DSL, which are respectively connected to row decoder 220a for transmitting operation voltages. EX1004, [0047]; EX1003, ¶99.

FIG. 4

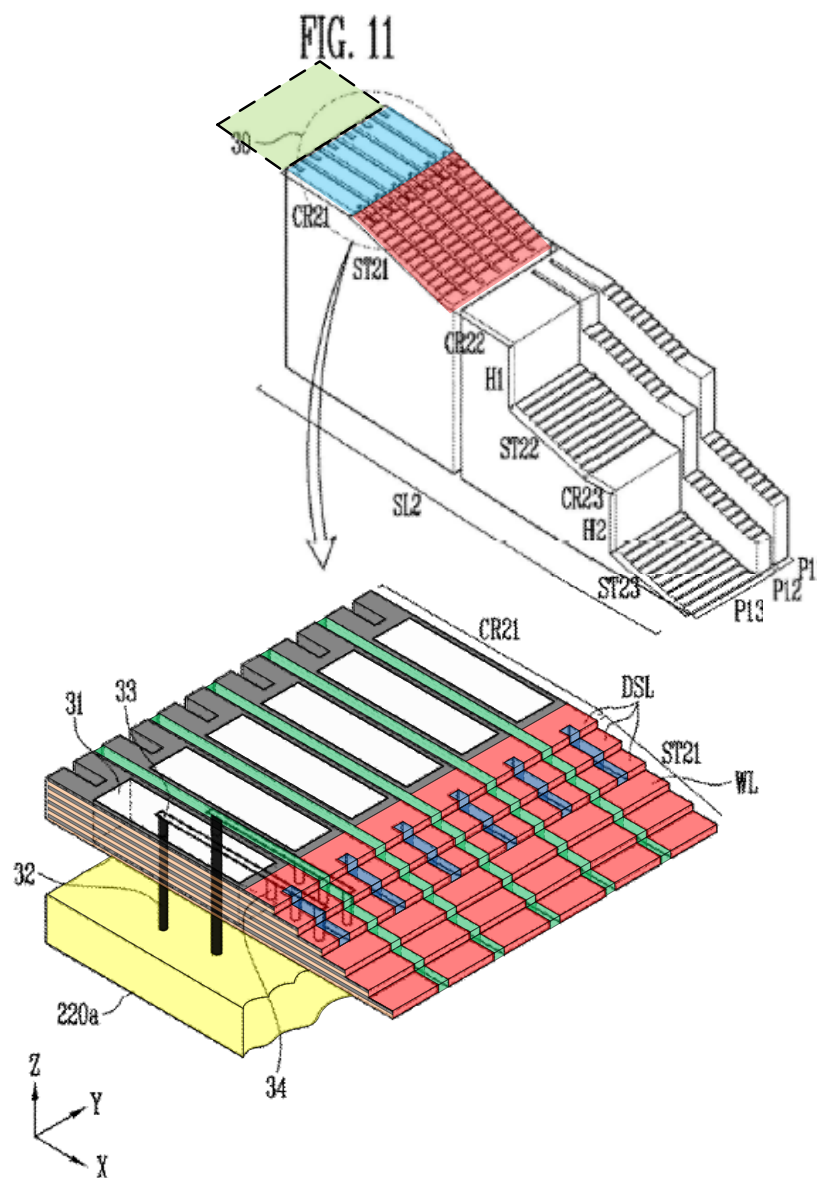


EX1003 — FIG. P

To reduce device size, Lee implements electrical connections between memory blocks 110 and sub-array row decoder 220a using various forms of TAVs

in various contact regions arranged in the X-direction of slimming regions SL1 and SL2, as detailed in FIGs. 11-14.

The detailed structures of the second slimming region SL2, including its contact regions and step regions, are further illustrated in FIG. 6 and annotated FIG. 11 below.



EX1003 — FIG. Q

Lee, like '974 patent, arranges a contact region CR21 (in light blue), in which contact plugs 32 (in black) for connecting sub-array row decoder 220a (in yellow) are formed, between step region ST21 (in red) and memory region MC (in light green, FIG. 6) in the X-direction. EX1004, [0077]; EX1003, ¶101. The top portion of FIG. 11 above also depicts two additional step regions ST22 and ST23, where more exposed ends of word lines WL are formed in pad regions P11, P12, and P13 along the Y-direction to increase the degree of integration. EX1004, [0063]; EX1003, ¶102.

As illustrated in the bottom portion of FIG. 11 above, parallel slots (in dark green) extend in the X-direction through contact region CR21 and step region ST21 and extend in the Z-direction through alternating insulating layers 10a (in brown) and conductive layers 10b (in gray). EX1003, ¶¶103-105. Moreover, additional parallel slots (in dark blue) extend along the X-direction in part of step region ST21, further dividing conductive layers 10b into drain select line (DSL) portions at the DSL levels. EX1003, ¶105.

Lee further discloses that the gate lines (*e.g.*, word lines WL) formed on the same conductive layer 10b and divided by the slots (in dark green) are still connected. EX1004, [0082]. For example, Lee discloses that as “unit[s] of the cell string,” word lines WL of the same conductive layer 10b are connected by connecting structures, including but not limited to contact plugs 41 and wires 42. EX1004, [0082], [0087];

EX1003, ¶106. The DSL portions divided by the additional slot (in dark blue) are electrically connected to row decoder 220a through contact plugs 32 and 34. EX1004, [0079]. As shown in FIG. 11 above, the two DSL portions divided by the same additional slot at the same vertical level are still connected to each other by the still-connected area in contact region CR21. EX1003, ¶106.

Lee provides detailed descriptions of the “slimming process of etching gate lines extended from the memory region MC to the first slimming region SL1 and the second slimming region SL2, respectively, in a step form or a pad form” in connection with FIGs. 7-10, as explained below in detail in Section VII.H. EX1004, [0065]-[0066].

B. Independent Claim 1

1. Lee discloses a “*microelectronic device comprising*” [1.P].

Lee discloses “a semiconductor device 1000,” which is a “*microelectronic device.*” EX1004, [0028].

2. Lee discloses “*at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising*” [1.a].

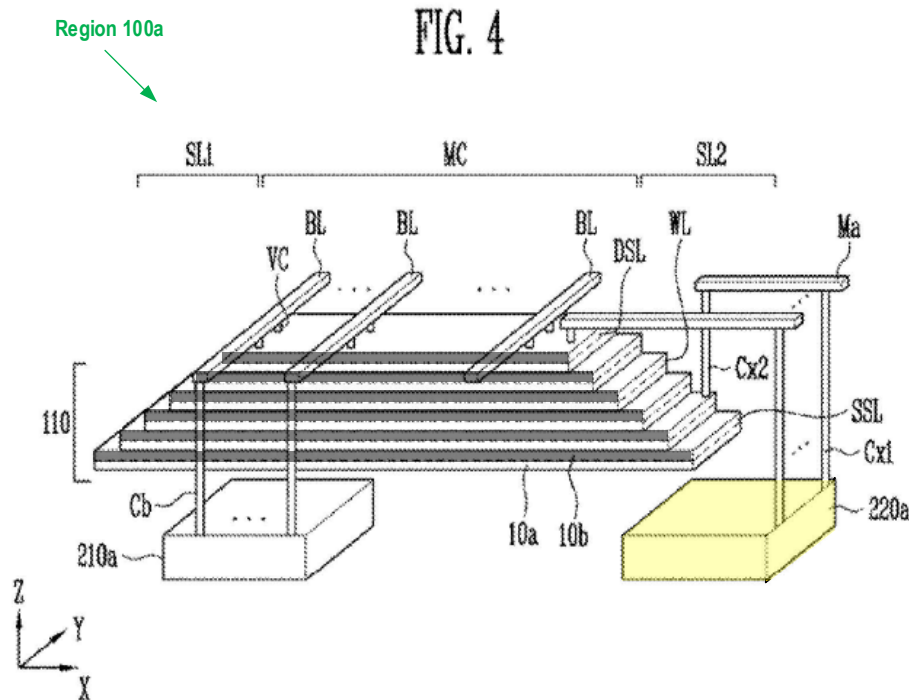
Lee discloses memory blocks 110 in a memory cell array 100 (“*at least one memory block*”) operatively coupled to row decoder 220a. EX1004, [0028]-[0031], [0033]-[0036], [0047].

Specifically, Lee discloses that “semiconductor 1000 may include memory

cell array 100 in which data is stored and a peripheral circuit 200 configured to perform program, read operation, or erase operations on the memory cell array 100.” EX1004, [0028]. Lee also discloses that “memory cell array 100 may include a plurality of memory blocks 110” and that “peripheral circuit 200 may include ... row decoders 220a.” EX1004, [0030]-[0031].

Lee explains that “peripheral circuit 200 may include a plurality of circuits, which may decrease a size of the semiconductor device 1000, some of the circuits included in the peripheral circuit 200 may be disposed **under** the memory cell array 100.” EX1004, [0029], FIGs. 1, 4, 11. As described by '974 patent, a sub-array circuitry (*e.g.*, circuit 136) is a circuit positioned under vertical memory block 100. EX1001, 6:49-54, FIG. 3. Thus, a POSITA would have understood that row decoder 220a is a “*sub-array circuitry*” for it is positioned under memory cell array 100. EX1003, ¶150.

Lee further discloses that “row decoder 220a may be connected to some of the memory blocks 110.” EX1004, [0033]. As shown in annotated FIG. 4 below, region 100a of memory cell array 100 is connected to row decoder 220a (in yellow) through contacts. EX1004, [0034]-[0036], [0046]-[0047]; EX1003, ¶¶152-153. Thus, Lee discloses [1.a].



EX1003 — FIG. AJ

3. Lee discloses *“an array of memory cells in a memory cell region”* [1.a.1].

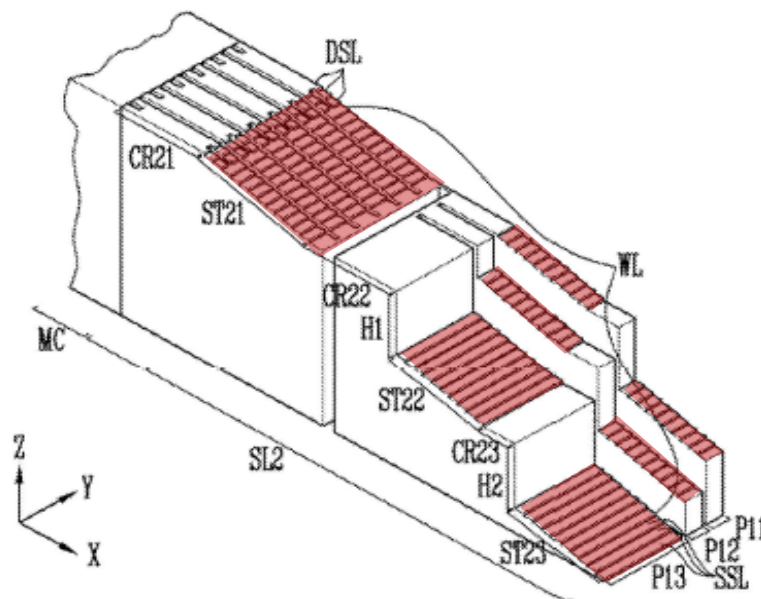
Lee discloses that “memory cell array 100 may include a plurality of memory blocks 110” and “[t]he region in which the memory blocks 110[] are formed is defined as a memory region MC.” EX1004, [0031], [0034], [0005]-[0006], FIG. 3; EX1003, ¶¶155-157. Thus, Lee discloses [1.a.1].

4. Lee discloses *“stair step structures in at least one stair step region”* [1.a.2].

Lee discloses that memory cell array 100 includes multiple “step regions, wherein gate lines are included in the step regions and arranged in a step form in the first direction.” EX1004, [0009].

For example, as shown in annotated FIG. 6 below, second slimming region SL2 at the end of memory cell array 100 includes step regions ST21, ST22, and ST23 (in red) where source select lines SSL, word lines WL, and drain select lines DSL extended from memory region MC are “formed in a step structure.” EX1004, [0054]-[0056]; EX1003, ¶160. Specifically, Lee discloses “**steps** may be generated between neighboring contact regions,” *i.e.*, in each step region. EX1004, [0055]. Since Lee discloses multiple step regions (*e.g.*, ST21, ST22, ST23), each including at least one structure formed by steps (referred to herein as “stepped structure,” which is the same as the claimed “*stair step structure*”), Lee discloses multiple “*stair step structures in at least one stair step region.*” EX1003, ¶¶160-161.

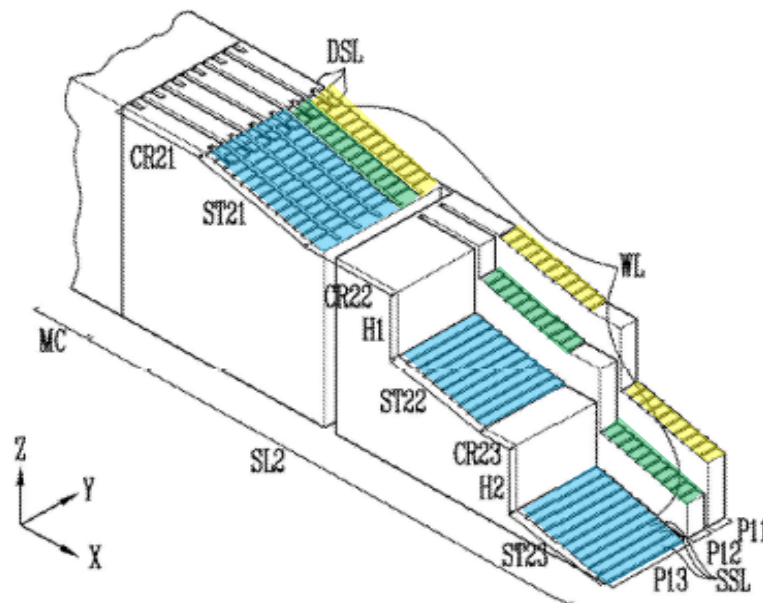
FIG. 6



EX1003 — FIG. AF

To the extent [1.a.2] further requires multiple stair step structures in one stair step region and/or along the bit line direction (which Petitioner does not concede), Lee also discloses pad regions P11, P12, and P13 “sequentially defined in the Y-direction” and “overlap[ping] the 21st step region ST21, the 22nd contact region CR22, the 22nd step region ST22, the 23rd contact region CR23, and the 23rd step region ST23.” EX1004, [0056]. Each pad region P11, P12, or P13 includes one or more stepped structures as “the step is formed in the word lines WL for each pad region within the step region.” EX1004, [0063].

FIG. 6



EX1003 — FIG. AG

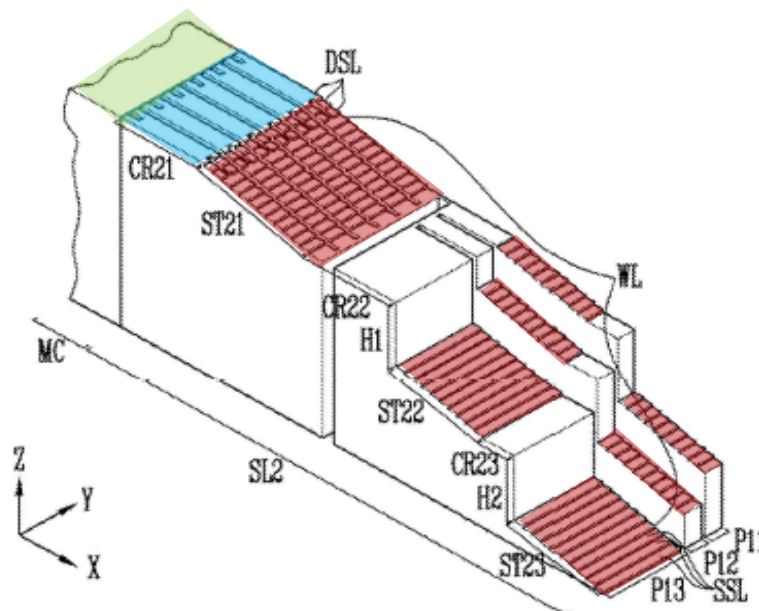
A POSITA thus would have understood, as depicted in annotated FIG. 6 above,

that each step region ST21, ST22, or ST23 includes multiple pad regions (e.g., P11, P12, and P13 in yellow, green, and blue, respectively, “*stair step structures*”) along the bit line direction, each having steps therein. EX1003, ¶163.

5. Lee discloses “*conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region*” [1.a.3].

Lee discloses memory cell array 100 further includes first contact plugs 32 in contact region CR21 (“*at least one via region*”), which is at least partially located between the memory region MC (“*memory cell region*”) and the step regions ST21, ST22, and ST23 (“*at least one stair step region*”). EX1004, [0056], [0077]-[0079].

FIG. 6

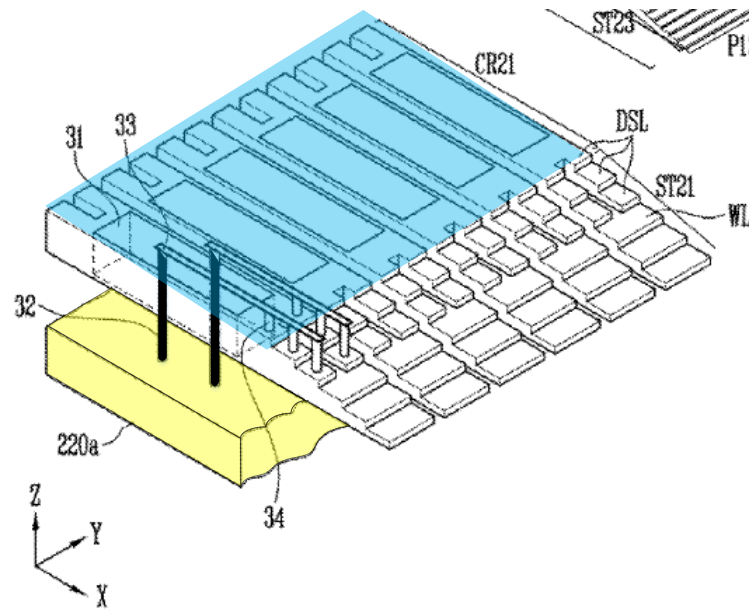


EX1003 — FIG. AH

As illustrated in annotated FIG. 6 above, contact region CR21 (in light blue)

is located between memory region MC (in light green) and step regions ST21, ST22, and ST23 (in red) in the X-direction. EX1004, [0056]; EX1003, ¶165. Additionally, contact region CR22 is also located between memory region MC and step region ST22, and contact region CR23 is further located between memory region MC and step region ST23. EX1003, ¶165.

As further illustrated in a portion of annotated FIG. 11 below, which is “an enlarged view of a portion 30 of the 21st contact region CR21 and the 21st step region ST21,” first contact plugs 32 (in black) “positioned vertically that is, in a [Z]-direction passing through the first blocking layers 31 are formed” in contact region CR21 (in blue). EX1004, [0077]; EX1003, ¶166. Lee explains that contact plugs 32 are “connected to the first row decoder 220a [(in yellow, “*sub-array circuitry*”)] located at the lower portion of the memory block” and “formed of conductive layers”. EX1004, [0078]-[0079]. Similarly, ’974 patent also discloses conductive vias 120 “extend through the vertical memory block 100” to be “electrically coupled to sub-array circuitry 136” and have “a conductive via material.” EX1001, 5:17-21, 6:49-52, 12:22-27. Thus, a POSITA would have understood that first contact plugs 32 are “*conductive vias*,” as they are formed of conductive materials and extend vertically through first blocking layer 31 to connect underneath row decoder 220a. EX1003, ¶167.



EX1003 — FIG. A1

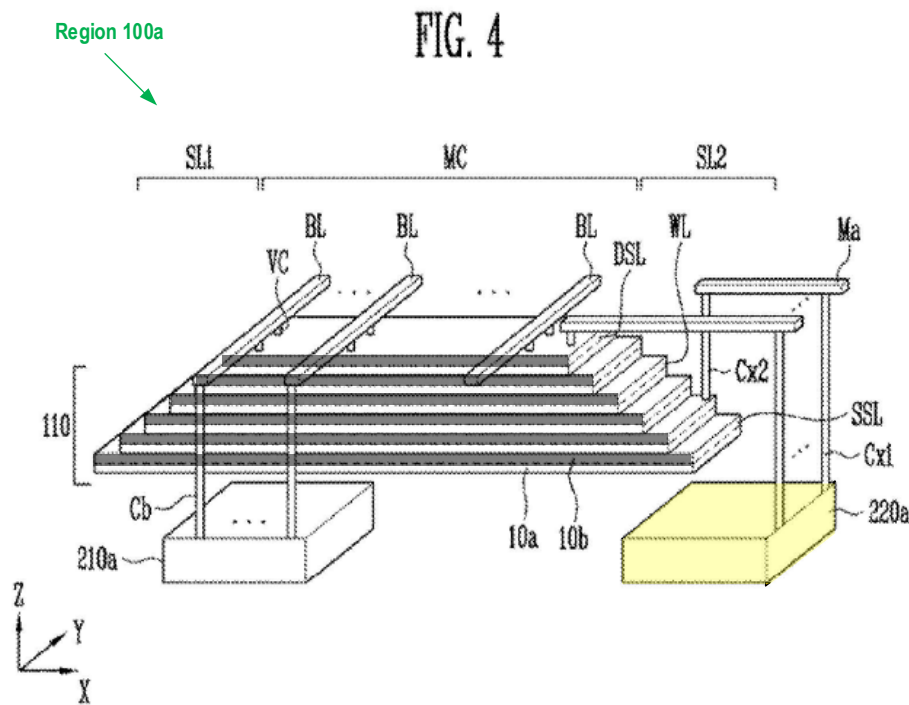
Thus, Lee discloses [1.a.3].

6. Lee discloses “access lines extending through the at least one memory block.” [1.a.4].

Lee discloses that memory cell array 100 further includes conductive layers 10b, which form source select lines, word lines, and drain select lines (collectively referred to as “gate lines” by Lee, EX1004, claim 2) and extend laterally through memory cell array 100. EX1004, [0045]-[0047].

Specifically, Lee discloses that “[t]he source select lines SSL, the word lines WL, and the drain select lines DSL may be formed of conductive layers 10b.” EX1004, [0046]. Lee also discloses that row decoder 220a “transmits operation voltages through ... the lines SSL, WL, and DSL extended in the first and second

slimming regions SL1 and SL2.” EX1004, [0008], [0047]. A POSITA thus would have understood that conductive layers 10b are “*access lines*” as they access the select transistors and memory cells in the memory region MC by way of “transmit[ting] operation voltages” thereto. EX1003, ¶171. Lee further discloses the gate lines formed of conductive layers 10b are “located in the memory region MC and extend in the X-direction have step forms in the first slimming region SL1 and the second slimming region SL2.” EX1004, [0045].



EX1003 — FIG. AJ

As shown in annotated FIG. 4 above, a POSITA would have understood that conductive layers 10b (in black) at different vertical levels are “*access lines*,” respectively, and extend across memory region MC into slimming regions SL1 and

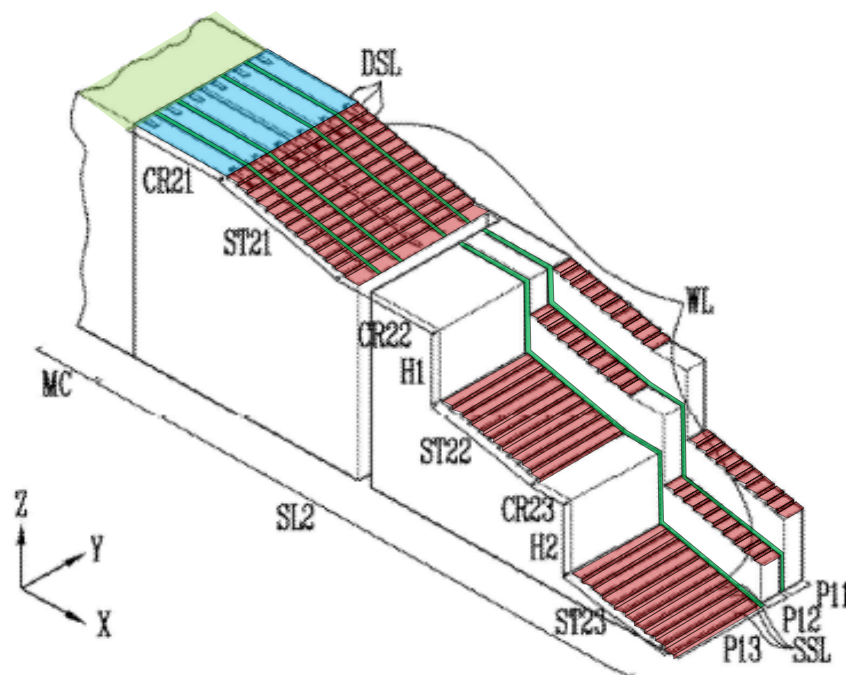
SL2 in the X-direction (“*through the at least one memory block*”). EX1003, ¶172.

Thus, Lee discloses [1.a.4].

7. Lee discloses or suggests “*a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region*” [1.a.5].

As illustrated in annotated FIG. 6 below, multiple parallel slots (in dark green) are present and extend in the X-direction in at least one of step regions ST21, ST22, and ST23 (“*the at least one stair step region*”). EX1003, ¶176.

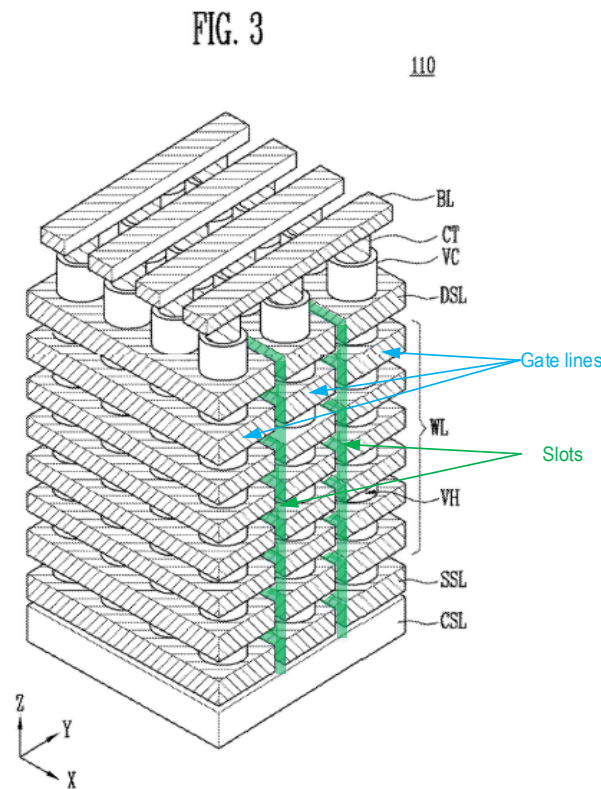
FIG. 6



EX1003 — FIG. AL

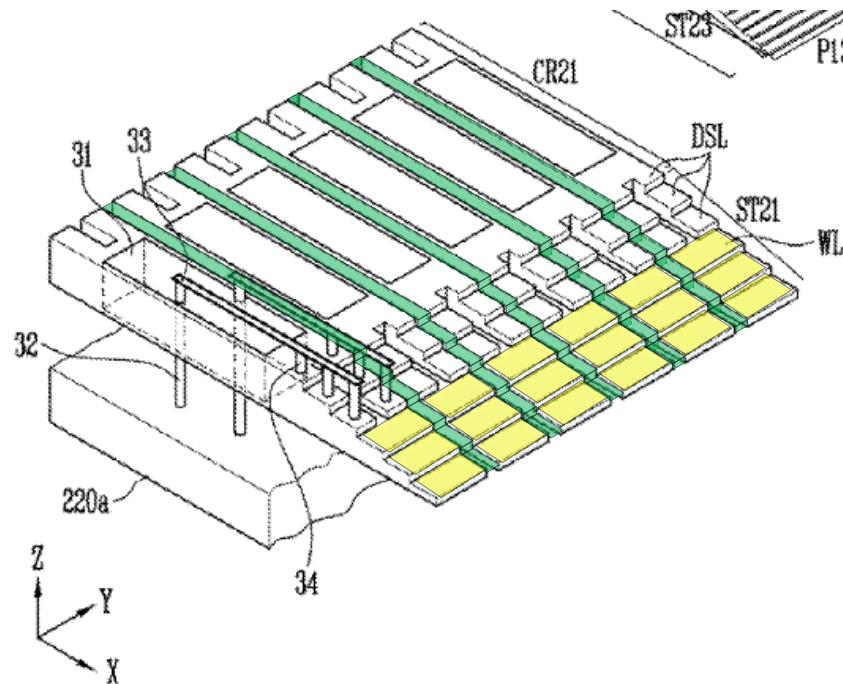
Annotated FIG. 3 below, which is “a perspective view illustrating a memory

block” generally applicable to FIG. 6, also shows that the slots (in dark green) extend in both the Z-direction and X-direction, dividing each conductive layer 10b into adjacent gate lines of the respective conductive layer 10b, which are “spaced apart from each other in the Y-direction” (“*adjacent access line portions of individual access lines*”). EX1004, [0036], [0039]-[0041]; EX1003, ¶¶174-175.



For instance, for word lines WL, Lee discloses that “the word lines WL formed **on the same layer** may so be electrically connected to each other,” “the third contact plugs 41 ... are formed on the word lines WL **divided** in the unit of the cell string, respectively” (FIG. 12), and that “the 11th pad region P11 has the same width

as a width of the word lines WL **divided** in the unit of the cell string” (FIG. 13). EX1004, [0082], [0087]. A POSITA would have understood, or at least found it obvious, that at each word line level, a respective conductive layer 10b is divided by the slots into word lines in the Y-direction. EX1003, ¶¶178-179. Illustrated below as a non-limiting example, the enlarged portion of annotated FIG. 11 shows five slots (in dark green) dividing three conductive layers 10b each into six word lines (in yellow). EX1003, ¶180.



EX1003 — FIG. AM

Thus, Lee discloses, or at least suggests, “*slots extending between adjacent access line portions of individual access lines within the at least one step region.*”

As to the claimed “*dielectric material within slots,*” Lee explains, with respect to FIG. 3 in which the slots are not shown as being filled, that “[a]lthough not

illustrated, insulating layers may be formed between ... the source select lines SSL, the word lines WL, the drain select lines DSL, and the bit lines VL.” EX1004, [0043]. Similarly, Lee explains, “[a] detailed structure, such as a spaced structure of the respective lines SSL, WL, and DSL, is omitted” from the schematic drawing of FIG. 4. EX1004, [0046]. Thus, Lee discloses, or at least suggests, the “*dielectric material*” within its slots. EX1003, ¶182.

Nevertheless, a POSITA would have understood, or at least found it obvious, that the spaced structure includes a dielectric material in the slots because the slots have to be sealed in semiconductor device 1000 to: (i) ensure process isolation and avoid damage and contamination to underlying structures through the opened slots during later fabrication process, (ii) provide mechanical stability to the structures above the slots and enhance the structural integrity of the device, and (iii) aid in planarization, ensuring a smooth upper surface necessary for subsequent photolithography steps. EX1013, [0064]; EX1003, ¶¶183-185, 188. Moreover, the sealing materials have to include at least a dielectric material to prevent short circuits, electrical interference, and crosstalk between gate lines at different vertical levels. EX1006, [0228], [0276]; EX1008, ¶¶180, 229; EX1009, [0071], FIG. 1C; EX1010, [0139], FIG. 16B; EX1011, [0093], FIG. 5; EX1018, [0095], [0105]; EX1019, [0143]; EX1020, 99; EX1003, ¶¶186-187.

Thus, Lee discloses, or at least suggests, an insulating layer (“*dielectric*

material”) present in the slots as spaced structures of the adjacent gate lines (“*between adjacent access line portion*”).

Accordingly, Lee discloses or suggests [1.a.5].

From the foregoing, Lee anticipates or otherwise renders obvious claim 1.

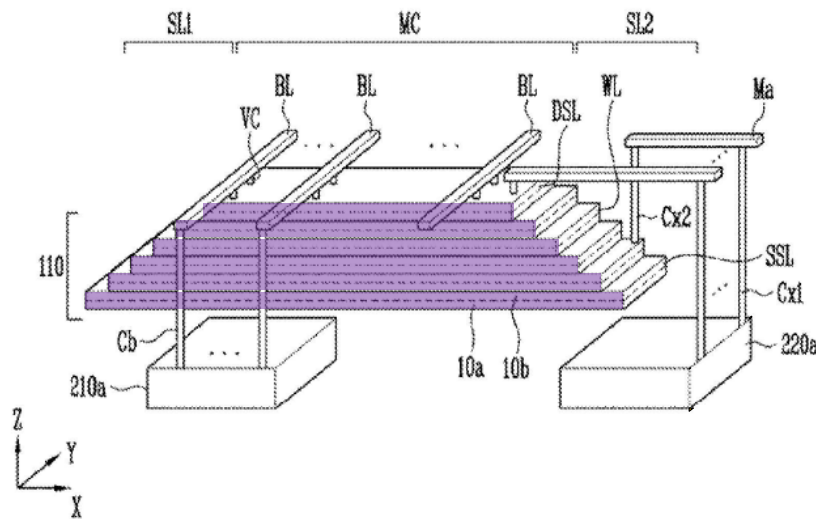
C. Dependent Claim 4

1. Lee discloses “*at least some of the stair step structures comprise: individual tiers aligned at different vertical levels from one another within a respective stair step structure*” [4.a].

Regarding element [4.a], Lee further discloses multiple pairs of conductive layers 10b and insulating layers 10a (referred to herein as “layer pairs”) stacked in the Z-direction to form a stepped structure (“*a respective stair step structure*”). EX1004, [0046].

For example, as shown in annotated FIG. 4 below, different layer pairs (in purple) are positioned at distinct vertical levels. EX1003, ¶¶193-194. A POSITA would have understood that each layer pair is “*individual tiers*,” consistent with the description of “tiers” in the ’947 patent, for example, the “five tiers” in FIG. 3. EX1001, 1:35-37, 43-45, 6:19-27; EX1003, ¶¶192-193. Thus, the layer pairs (“*individual tiers*”) in each stepped structure of step regions ST21, ST22, and ST23 are “*aligned at different vertical levels from one another*” under either mapping to “*stair step structure*” discussed in Section VII.B.4. EX1004, FIG. 6; EX1003, ¶194.

FIG. 4

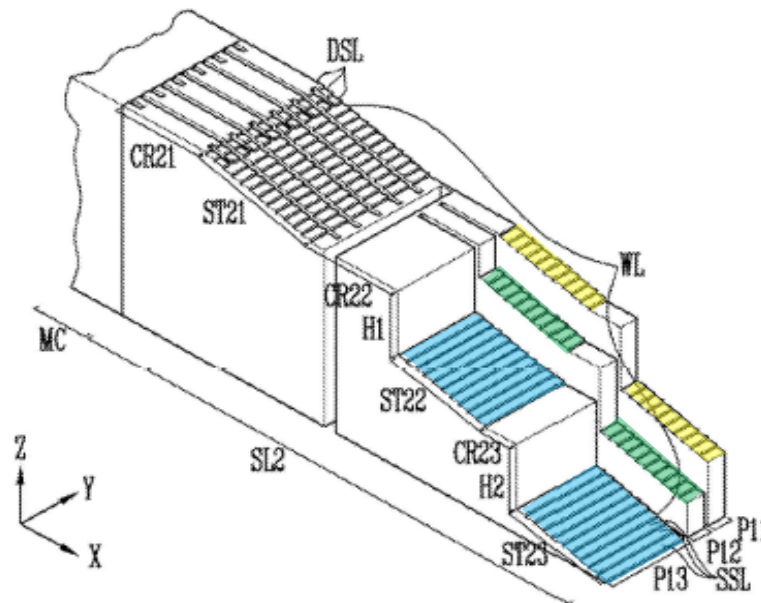


EX1003 — FIG. AQ

Lee still discloses element [4.a] with an alternative interpretation that it may read on different stair step structures in the bit line direction are aligned at different vertical levels (which Petitioner does not concede). This is because, as shown in annotated FIG. 6 below, Lee discloses that pad regions P11, P12, and P13 (in yellow, green, and blue, “*at least some of the stair step structures*”) have different heights in each of step regions ST22 and ST23, and that “the uppermost word lines WL included in the 22nd step region ST22 and the 12th[/13th] pad region P12[/P13] is located at a lower level than a word line located at the lowermost word line WL included in the 22nd step region ST22 and the 11th[/12th] pad region P11[/P12].” EX1004, [0057]-[0058], [0061]; EX1003, ¶¶195-197. Thus, at least in each of step regions ST22 and ST23, layer pairs (“*tiers*”) in the different stepped structures

(“*stair step structures*”) in pad regions P11, P12, and P13 in the Y-direction are aligned at different vertical levels from one another as well. EX1003, ¶198. Thus, Lee discloses [4.a].

FIG. 6



EX1003 — FIG. AR

2. Lee discloses or suggests “*contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines*” [4.b].

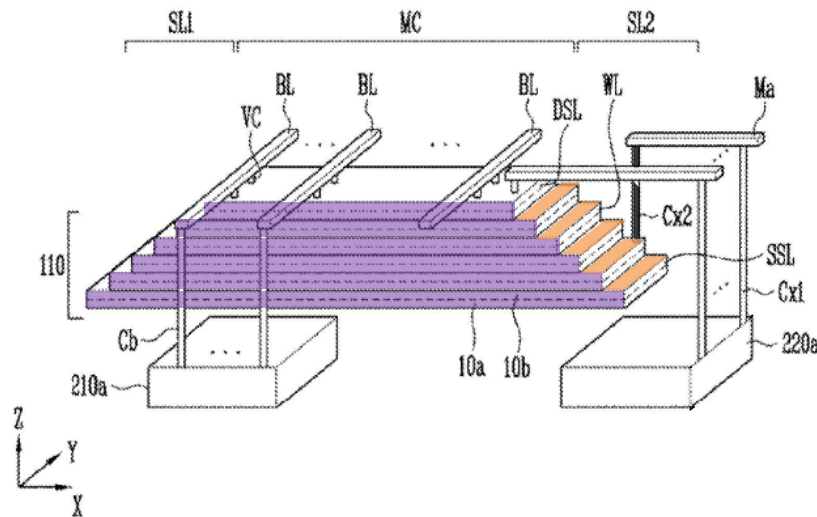
Lee discloses that each layer pair (“*individual tiers*”) has exposed ends (“*contact regions*”) on which contact plugs (e.g., contact plugs Cx2) are formed in the stepped structures. EX1004, [0047], [0063].

As shown in annotated FIG. 4 below, each layer pair (in purple) has a

respective exposed end (in orange) on which contact plug Cx2 (in black) is formed.

EX1004, [0047]; EX1003, ¶200.

FIG. 4



EX1003 — FIG. AS

Specifically, Lee discloses that “contact plugs 41 are formed on the word lines WL” and “contact plugs 52 may be formed on the word lines WL, respectively.” EX1004, [0082], [0087]. As shown in the enlarged views of FIGs. 12 and 13, each contact plug 41 or 52 is formed on the only exposed end (“*single contact region*”) of a respective word line WL (“*a respective access line portion of the individual access line*”) of a respective layer pair (“*each tier*”). EX1003, ¶201. Therefore, Lee discloses, or at least suggests, “*each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.*”

D. Dependent Claim 5

Claim 5 additionally requires that “*the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region,*” which is disclosed by Lee.

Besides step regions ST21, ST22, and ST23 in second slimming region SL2 (Section VII.B.4), Lee further discloses that “first and second slimming regions SL1 and SL2 are defined at both ends of the memory blocks,” and that step regions ST11, ST12, and ST13 in first slimming region SL1 are “at the other end of the memory region MC.” EX1004, [0034], [0051], FIGs. 4-5. Thus, Lee discloses “*two stair step regions at opposing ends of the at least one memory block.*”

As explained in Section VII.B.5, Lee discloses contact region CR21 between memory region MC and step regions ST21, ST22, and ST23 in the X-direction. Similarly, as shown in FIG. 5, another contact region CR11 is located between memory region MC and step regions ST11, ST12, and ST13 in the X-direction. EX1004, [0051], FIG. 5. Thus, each of step regions ST21, ST22, and ST23 and step regions ST11, ST12, and ST13 (“*each of the two stair step regions*”) are located remotely from memory region MC (“*memory cell region*”) by contact region CR21 or CR11.

E. Independent Claim 7

- 1. Lee discloses a “*method of forming a microelectronic device*” [7.P].**

Lee discloses a method for manufacturing a semiconductor device 1000 having slimming regions SL1 and SL2. EX1004, [0028], [0064]-[0065].

- 2. Lee discloses or suggests “*forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region*” [7.a].**

As explained above in Sections VII.B.2-VII.B.5, Lee discloses “*a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region.*” Lee specifically discloses “FIGS. 7 and 10 are perspective views for illustrating a method of forming the first slimming region and the second slimming region,” which include the step regions (“*stair step region*”) and contact regions (*e.g.*, CR21) (“*via region*”). EX1004, [0065], FIGs. 7-10. A POSITA thus would have understood, or at least found it obvious, that Lee also forms memory region MC (“*memory cell region*”) of the same memory cell array 100 when forming the step regions and contact regions. EX1004, [0005]; EX1003, ¶212.

3. Lee discloses or suggests “*forming an array of memory cells in the memory cell region*” [7.b].

Lee discloses that “memory cell array 100 may include a plurality of memory blocks 110” and “[t]he region in which the memory blocks 110[] are **formed** is defined as a memory region MC.” EX1004, [0031], [0034], [0005], FIGs. 3-4. Thus, a POSITA would have readily appreciated that Lee discloses, or at least suggests, “*forming an array of memory cells in the memory cell region.*” EX1003, ¶215; Section VII.B.3.

4. Lee discloses “*forming stair step structures in the stair step region*” [7.c].

As explained in Section VII.B.4, Lee discloses “*stair step structures in the stair step region.*” Lee specifically discloses, “FIGS. 7 and 10 are perspective views for illustrating a method of forming the first slimming region and the second slimming region,” which include the step regions (“*stair step region*”). EX1004, [0065], FIGs. 7-10. For example, Lee discloses, “a slimming process of etching gate lines extended from the memory region MC to the first slimming region SL1 and the second slimming region SL2, respectively, in a step form or a pad form, is performed.” EX1004, [0066].

5. Lee discloses or suggests “*forming conductive vias in the via region*” [7.d].

As explained above in Section VII.B.5, Lee discloses “*conductive vias in at least one via region.*” Lee specifically discloses that “[f]irst contact plugs 32

positioned vertically that is, in a [Z]-direction passing through the first blocking layers 31 are **formed**,” “first blocking layers 31 may be **formed** of an insulating material such as an oxidization layer,” and “contact plugs 32 ... are **formed** of conductive layers.” EX1004, [0077], [0079]. Thus, a POSITA would have readily appreciated that Lee discloses, or at least suggests, “*forming conductive vias in the via region.*” EX1003, ¶221.

6. Lee discloses or suggests “*forming access lines extending through the memory block*” [7.e].

As explained above in Section VII.B.6, Lee discloses or suggests “*access lines extending through the at least one memory block.*” Lee specifically discloses that “source select lines SSL, the word lines WL, and the drain select lines DSL may be **formed** of conductive layers 10b,” and “in the first slimming region SL1 and the second slimming region SL2, the drain select lines DSL and some word lines WL are **formed** in the 11th step region ST11 and the 21st step region ST21.” EX1004, [0046], [0066]; [0067]-[0068]. Thus, a POSITA would have readily appreciated that Lee discloses, or at least suggests, “*forming access lines extending through the memory block.*” EX1003, ¶225.

7. Lee discloses or suggests “*forming slots extending between adjacent portions of individual access lines within the stair step region*” [7.f].

As explained above in Section VII.B.7, Lee discloses or suggests “*slots*

extending between adjacent access line portions of individual access lines within the at least one stair step region.” Thus, a POSITA would have readily appreciated that Lee discloses, or at least suggests, *“forming slots extending between adjacent portions of individual access lines within the stair step region.”* EX1003, ¶228.

8. Lee discloses or suggests “forming a dielectric material within the slots” [7.g].

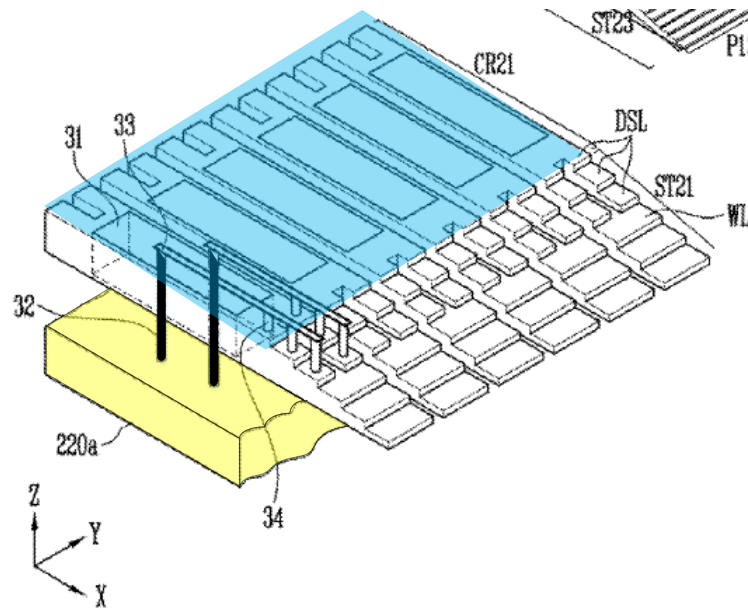
As explained above in Section VII.B.7, Lee discloses or suggests *“a dielectric material within slots.”* A POSITA would have readily appreciated that Lee discloses, or at least suggests, *“forming a dielectric material within the slots.”* EX1003, ¶231.

From the foregoing, Lee anticipates or otherwise renders obvious claim 7.

F. Dependent Claim 9

Claim 9 additionally requires that *“forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry,”* which is disclosed or suggested by Lee.

Lee discloses, “[f]irst contact plugs 32 positioned vertically that is, in a [Z]-direction passing through the first blocking layers 31 are **formed**,” and “first contact plugs 32 are connected to the first row decoder 220a located at the lower portion of the memory block.” EX1004, [0077]-[0078]. As further shown in the annotated enlarged view of FIG. 11 below, the two contact plugs 32 (in black) are formed substantially vertically aligned over row decoder 220a (in yellow). EX1003, ¶233.



EX1003 — FIG. A1

Thus, a POSITA would have understood, or at least found it obvious, that Lee discloses forming contact plugs 32 (“*at least some of the conductive vias*”) to be vertically aligned over row decoder 220a (“*portions of the sub-array circuitry*”). EX1003, ¶234.

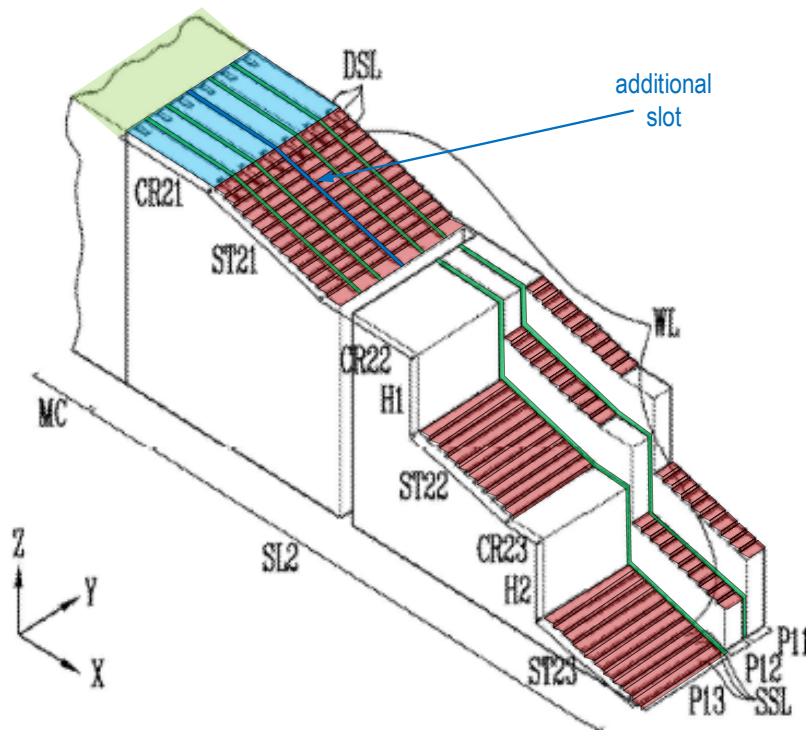
G. Dependent Claim 11

Claim 11 additionally requires that “*forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots,*” which is disclosed or suggested by Lee.

At the outset, the plain and ordinary meaning of the claim language does not require forming the additional slot before or after any other slot, which is consistent

with '974 patent. EX1001, 11:31-38, FIGs. 9A-9B; EX1003, ¶236.

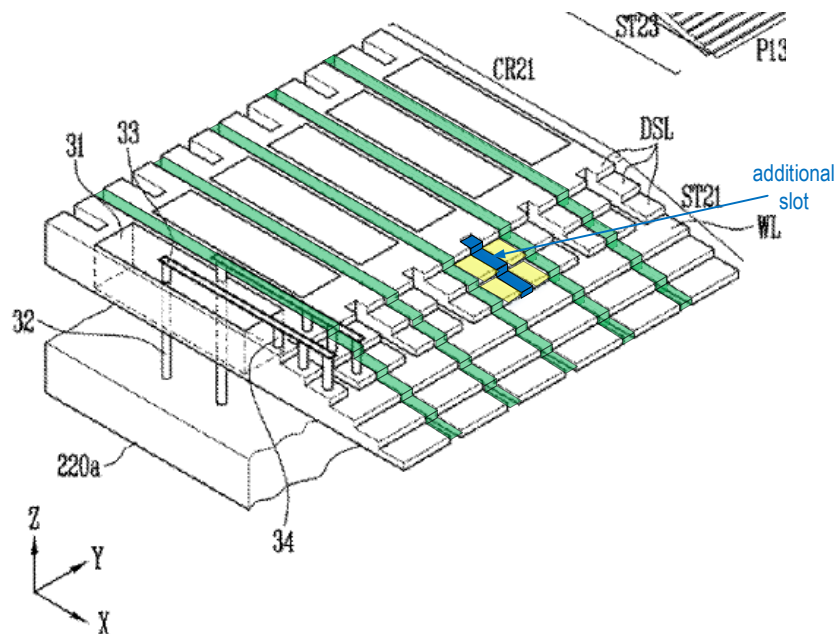
FIG. 6



EX1003 — FIG. AW

As discussed in Sections VII.B.7 and VII.E.7, Lee discloses or suggests “forming slots extending between adjacent portions of individual access lines.” For instance, as shown in annotated FIG. 6 above, a POSITA would have understood, or at least found it obvious, that Lee forms an additional slot (in dark blue) extending in the X-direction between the adjacent gate lines (“adjacent portions of the individual access lines”) in parallel with other slots (in dark green, “without intersecting any other slot of the slots”). EX1003, ¶237.

As another example depicted in the annotated enlarged portion of FIG. 11 below, a POSITA would have understood, or at least found it obvious, that Lee also forms an additional slot (in dark blue) extending in the Z-direction through only conductive layers 10b forming drain select lines DSL and extending in the X-direction only in part of step region ST21 between the adjacent DSL portions (in yellow, “*adjacent portions of the individual access lines*”) in parallel with the existing slots (in dark green, “*without intersecting any other slot of the slots*”). EX1003, ¶238.



EX1003 — FIG. AX

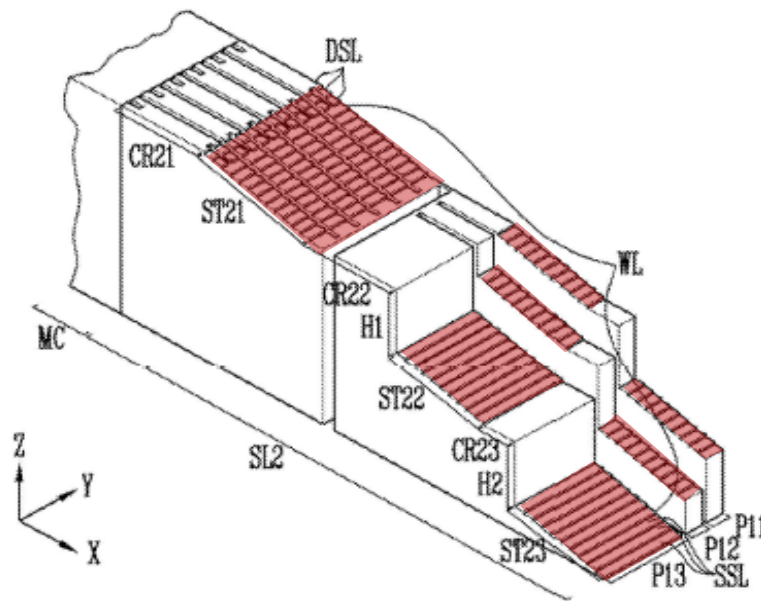
H. Dependent Claim 12

Claim 12 depends on claim 7 and additionally requires that “*forming the stair step structures comprises removing at least a portion of the stair step structures*

using a single stair step mask and two chop masks,” which is disclosed or suggested by Lee.

As discussed in Section VII.B.4 and further shown in annotated FIG. 6 below, Lee discloses second slimming region SL2 having multiple stepped structures (“*stair step structures*”), including the three adjacent stepped structures in the Y-direction in each of step regions ST22 and ST23 overlapping pad regions P11, P12, and P13, which have different heights in the Z-direction. EX1003, ¶240.

FIG. 6

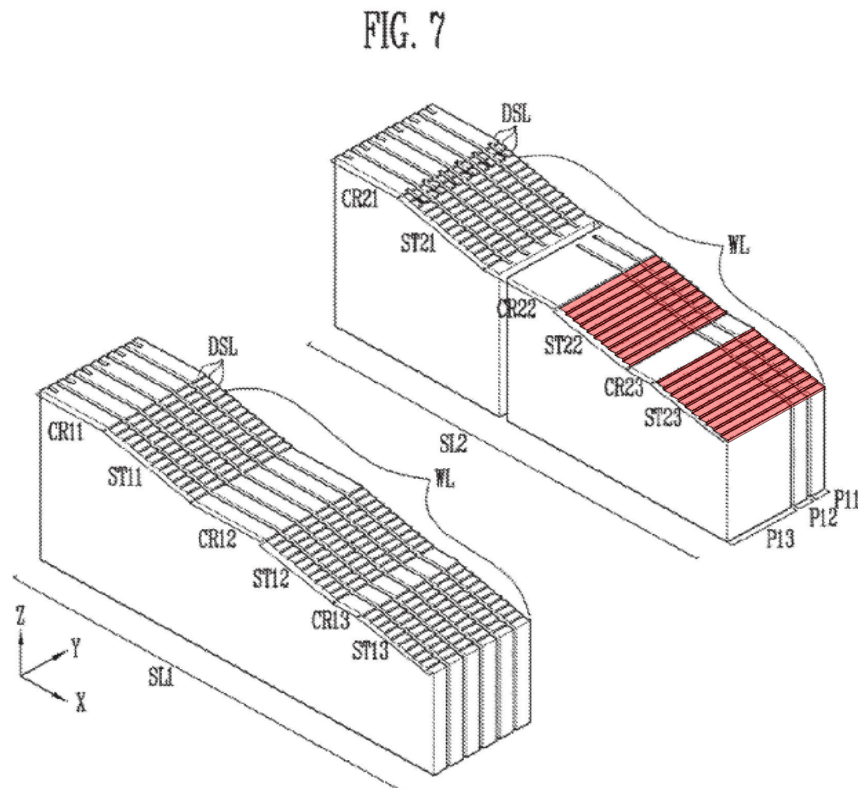


EX1003 — FIG. AF

Lee further discloses “a method of manufacturing the first and second slimming regions SL1 and SL2 shown in FIGS. 5 and 6” in FIGS. 7-10. EX1004, [0020], [0064]. Regarding the method, Lee discloses “a slimming process of etching

gate lines ... in a step form or a pad form,” and that “[b]y the aforementioned etching process, all of the drain select lines DSL, the word lines WL, and the source select lines SSL may be exposed.” EX1004, [0066], [0074], [0067]-[0073]. Thus, Lee discloses, “*removing at least a portion of the stair step structures.*” EX1003, ¶241.

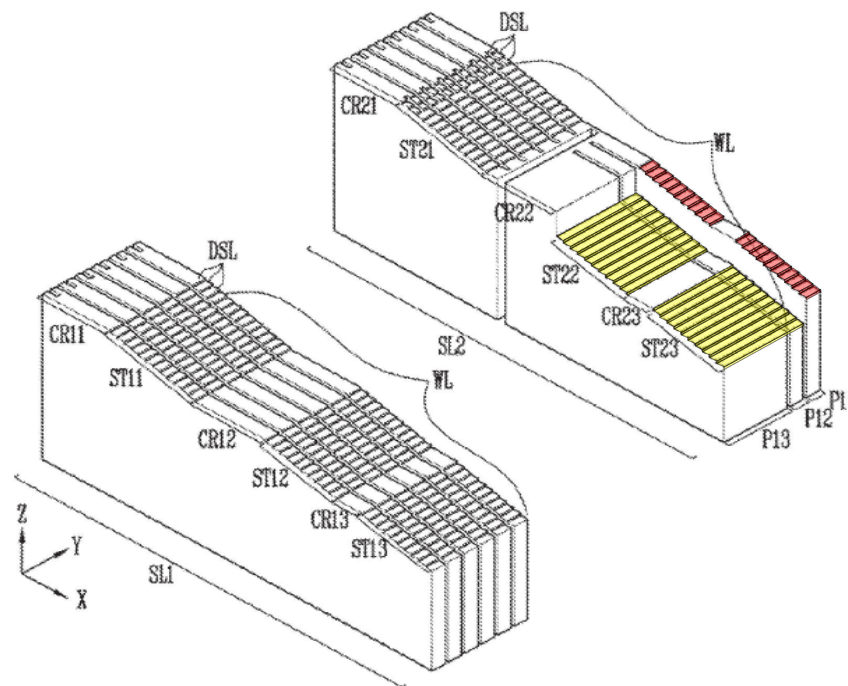
Specifically, Lee discloses a progression with respect to FIGs. 7-9, indicating, or at least suggesting, “*using a single stair step mask and two chop masks*” in its “slimming process of etching gate lines” to form its stepped structures in slimming region SL2. EX1003, ¶242.



First, referring to FIG. 7, gate lines are formed “in a step form” in step regions

ST22 and ST23 by etching the gate lines therein. EX1004, [0067]-[0068]. From annotated FIG. 7 above, a POSITA would have understood, or at least found it obvious, that the etching process to form the gate lines in step regions ST22 and ST23 in the current **step form** (in red) uses a single stair step mask. EX1003, ¶243.

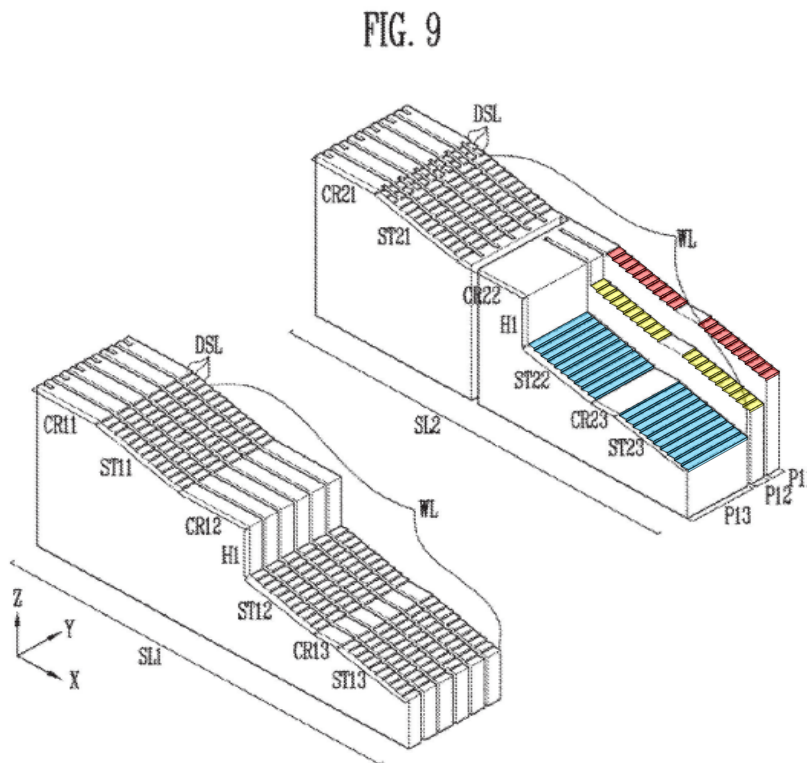
FIG. 8



EX1003 — FIG. BA

Second, referring to FIG. 8, “heights of the lines are decreased by etching the word lines included in the regions in which the 22nd step region ST22, ... and the 23rd step region ST23 of the second slimming region SL2 overlap the 12th pad region P12 and the 13th pad region P13.” EX1004, [0069]. In annotated FIG. 8 above, the gate lines in the area overlapping pad regions P12 and P13 (in yellow) are

“chopped off” to become lower than the other area overlapping pad region P11 (in red). EX1003, ¶245. Thus, a POSITA would have understood, or at least found it obvious, that the etching process applied to the gate lines in step regions ST22 and ST23 in the current **pad form** uses a first chop mask that covers pad region P11, such that the etching applies to pad regions P12 and P13 but not pad region P11. EX1003, ¶245.



EX1003 — FIG. BB

Third, referring to FIG. 9, “a height of the region is decreased by etching the word lines WL Included in the regions, in which the 22nd step region ST22, ... and the 23rd step region ST23 of the second slimming region SL2 overlap the 13th pad

region P13.” EX1004, [0072]. In annotated FIG. 9 above, the gate lines in the area overlapping pad region P13 (in blue) are “chopped off” again to become lower than the other area overlapping pad region P12 (in yellow). EX1003, ¶246. Thus, a POSITA would have understood, or at least found it obvious, that the etching process applied to the gate lines in step regions ST22 and ST23 in the current **pad form** uses a second chop mask that covers pad regions P11 and P12, such that the etching applies to pad region P13 but not pad regions P11 and P12. EX1003, ¶246.

Notably, AAPA-2, as evidence of common knowledge of a POSITA, strongly supports that a POSITA would have understood Lee discloses, or at least suggests, the usage of a stair step mask and chop masks in forming its stepped structures. EX1003, ¶247.

I. Dependent Claim 13

Claim 13 depends on claim 7 and additionally recites [13.a] and [13.b] below.

1. Lee discloses or suggests “*forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials*” [13.a].

Notably, [13.a] requires nothing more than what has been characterized as “**conventional**” in AAPA-1. EX1001, 1:43-59.

Lee discloses or at least suggests forming vertical channel layers VC (“*vertical memory cell pillars*”), which “include circular channel layers and memory

layers surrounding the channel layers” and “extend in a Z-direction,” consistent with ’974 patent. EX1004, [0037]-[0038]; EX1001, 4:32-37; EX1003, ¶252. Lee also discloses vertical channel layers VC are formed within a stack of alternating insulating layers 10a (“*dielectric materials*”) and conductive layers 10b. EX1004, [0039]-[0041], [0045]-[0046], FIGs. 3-4; EX1003, ¶253.

To the extent Lee does not explicitly disclose forming vertical channel layers VC within a stack of alternating dielectric materials, Lee at least suggests this. Lee’s stack of alternating insulating layers 10a and conductive layers 10b (collectively “a stack of alternating dielectric/conductive materials”) is formed using the well-known gate replacement process. EX1003, ¶254. This process involves first forming vertical channel layers VC within a stack of alternating dielectric materials—including insulating layers 10a and sacrificial layers having a different dielectric material—followed by replacing the sacrificial layers with conductive layers 10b, eventually resulting in the stack of alternating dielectric/conductive materials, as evidenced by AAPA-1. EX1001, 1:49-59; EX1003, ¶254. Thus, Lee discloses or at least suggests [13.a].

2. Lee discloses or at least suggests “*forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials*” [13.b].

The plain and ordinary meaning of [13.b] does not specify the timing of “*forming the conductive vias in the via region*” or “*isolating the conductive vias*”

much less with respect to the timing of forming “*the stack of alternating dielectric materials.*” This is consistent with ’974 patent, where it says, “[a]lthough the formation of the conductive vias 120 has been explained and illustrated as occurring subsequent to the formation of the conductive word lines 116 and the filling of the slots 114 with a dielectric material, **the present disclosure is not so limited,**” and as an example, “the conductive vias 120 may be formed **prior to, during, or after** the formation of the conductive word lines 116 and the filling of the slots 114 with a dielectric material.” EX1001, 12:46-53.

Thus, under the plain and ordinary meaning of [13.b], Lee discloses or at least suggests [13.b] because contact plugs 32 (“*conductive via*”) are formed in contact region CR21 (“*at least one via region*”) extending into the stack of alternating dielectric/conductive materials, which has alternating dielectric materials before the gate replacement process. Sections VII.B.5, VII.I.1; EX1003, ¶258. A POSITA would have understood that before gate replacement, contact plugs 32 are isolated from the stack of alternating dielectric materials by first blocking layers 31. EX1004, [0077]; EX1003, ¶258.

J. Independent Claim 14

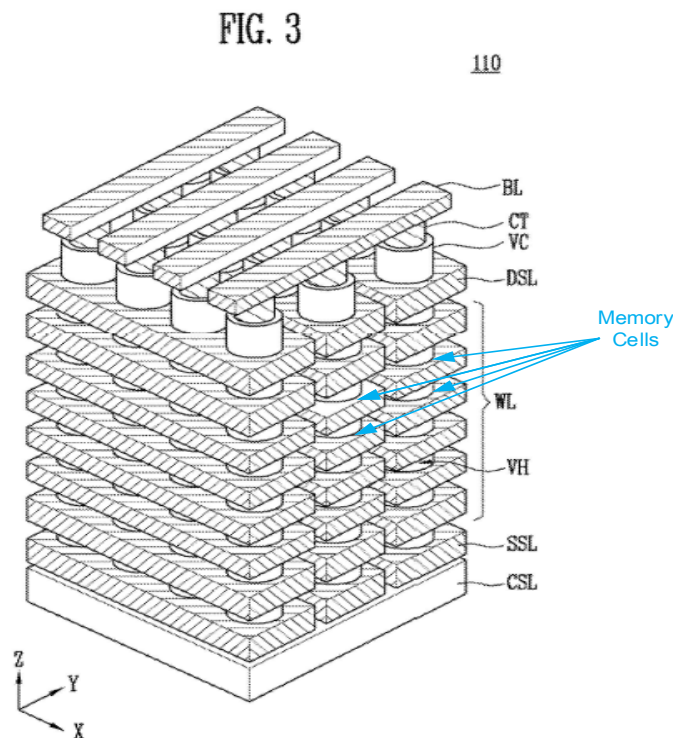
1. Lee discloses a “*method of forming a microelectronic device*” [14.P].

As explained above in Section VII.E.1, Lee discloses [14.P], which is the

same as [7.P].

2. Lee discloses or at least suggests “*forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials*” [14.a].

As explained above in Section VII.E.3, Lee discloses or at least suggests “*forming an array of memory cells.*” As further illustrated in annotated FIG. 3 below, an array of memory cells, each at a respective junction between word lines WL and vertical channel layers VC, are formed in memory region MC. EX1003, ¶261.



Lee also discloses, or at least suggests, that the memory cells are formed within a stack of alternating insulating layers 10a (“*dielectric materials*”) and conductive layers 10b (“*conductive materials*”). EX1004, [0039]-[0041], [0046].

From annotated FIG. 4 below, a POSITA would have understood, or at least found it obvious, that memory cells in memory region MC (e.g., shown in FIG. 3 above) are formed in a stack including alternating insulating layers 10a (in brown) and conductive layers 10b (in gray). EX1003, ¶262. Thus, Lee discloses or at least suggests [14.a].

FIG. 4

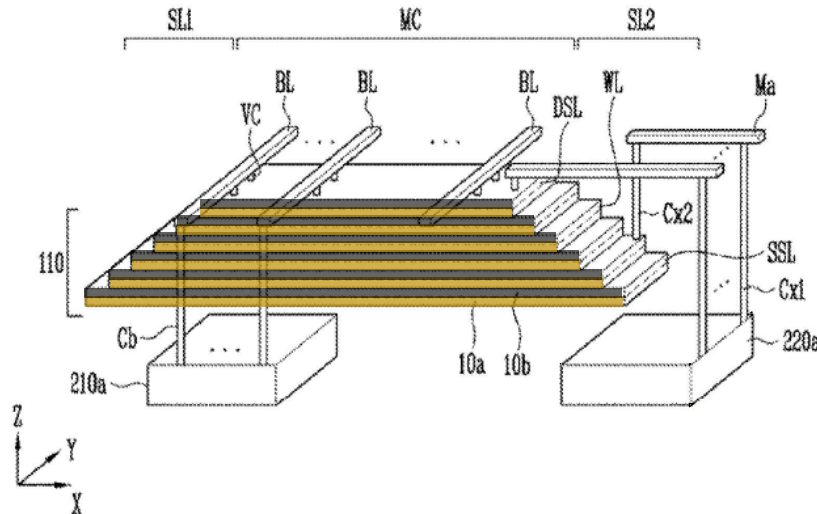


FIG. 5

EX1003 — FIG. BC

3. Lee discloses or suggests *“forming access lines coupled to memory cells of the array of memory cells”* [14.b].

As explained above in Section VII.E.6, Lee discloses or suggests *“forming access lines extending through the memory block.”* As shown in annotated FIG. 3 above, since each memory cell is formed at a respective junction between word lines

WL and vertical channel layers VC, conductive layers 10b forming the word lines WL (“*access lines*”) are formed “*coupled to memory cells of the array of memory cell*” to “transmit[] operation voltages” to the memory cells through word lines WL. EX1004, [0047], [0008]; EX1003, ¶264. Thus, Lee discloses [14.b].

4. Lee discloses or suggests “*forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack*” [14.c].

As explained above in Sections VII.E.5 and VII.F, Lee discloses or suggests “*forming conductive vias in the via region*” and “*forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.*”

Since Lee also discloses that contact region CR21 (“*via region*”) is next to memory region MC in which the array of memory cells is formed, a POSITA would have understood that contact plugs 32 (“*conductive vias*”) in contact region CR21 are formed “*adjacent the array of memory cells*” in memory region MC. EX1004, FIG. 6; EX1012, 1a; EX1003, ¶267.

Since Lee further discloses that “first contact plugs 32 are connected to the first row decoder 220a located at the lower portion of the memory block,” a POSITA would have understood that first contact plugs 32 are formed “*adjacent sub-array circuitry underlying the stack.*” EX1004, [0078], FIG. 11; EX1012, 1b; EX1003,

¶268. Accordingly, Lee discloses or suggests [14.c].

5. Lee discloses or suggests “*forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines*” [14.d].

As explained above in Sections VII.C.2, VII.E.4, and VII.H, Lee discloses or suggests “*forming stair step structures in the stair step region,*” “*removing at least a portion of the stair step structures using a single stair step mask and two chop masks,*” and “*contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.*”

Lee specifically discloses that “**steps** may be generated between two neighboring contact regions,” *i.e.*, the stepped structures (“*stair step structures*”) in step regions ST21, ST22, and ST23 in slimming region SL2. EX1004, [0055]. Lee also discloses the gate lines of different conductive layers 10b are formed “in a step form,” and contact plugs are formed on “the lines SSL, WL, and DSL **exposed in a step structure** in the second slimming region SL2.” EX1004, [0045], [0047]. Accordingly, Lee discloses that the stepped structures (“*stair step structures*”) include steps having exposed ends of conductive layers 10b (“*contact regions comprising ends of the access lines*”).

Accordingly, Lee discloses or suggests [14.d].

6. Lee discloses or suggests “*removing at least a portion of the stair step structures using at least one chop mask*” [14.e].

As explained in Section VII.H, since Lee discloses or suggests “*removing at least a portion of the stair step structures using a single stair step mask and two chop masks,*” Lee also discloses or suggests [14.e].

From the foregoing, Lee anticipates or suggests claim 14.

K. Dependent Claims 15, 16, and 18

Claims 15, 16, and 18 each depends on claim 14 and further requires that “*removing the at least a portion of the stair step structures using the at least one chop mask comprises*”: (i) *forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures*” [15]; (ii) “*using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask*” [16]; and (iii) “*covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask*” [18.a], and “*vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed*” [18.b].

Claims 15, 16, and 18 require nothing more than the well-known “chopping” process for “provid[ing] contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover,” which is part

of AAPA-2. EX1001, 9:50-10:11. Specifically, element [15] would have been known by a POSITA in AAPA-2 as “provid[ing] contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover” (EX1001, 9:65-67); element [16] would have been known by a POSITA in AAPA-2 as “[a] single chop mask may be used to double the number of contact regions (“stairs”) of a stair step structure formed using a single stair step mask” (EX1001, 10:4-7); element [18.a] would have been known by a POSITA in AAPA-2 as “[a] chop mask may be used cover one or more particular stair step structures or portions thereof ... , while leaving one or more other stair step structures or portions thereof exposed through the chop mask” (EX1001, 9:50-54); element [18.b] would have been known by a POSITA in AAPA-2 as “[t]he entire exposed one or more other stair step structures or portions thereof is vertically recessed, such that one or more exposed tiers is removed” (EX1001, 9:54-57). EX1003, ¶¶275, 279, 290.

For claim 15, in view of the common knowledge evidenced by AAPA-2 and as further explained in Section VII.H, a POSITA would have understood, or at least found it obvious, that during each etching process using a chop mask to form gate lines in a pad form, more gate lines become exposed in the newly “chopped” pad regions. EX1004, [0069], [0072], [0074], FIGs. 7-9; EX1003, ¶¶275-277. This process creates additional exposed ends (“*additional contact regions*”) in step

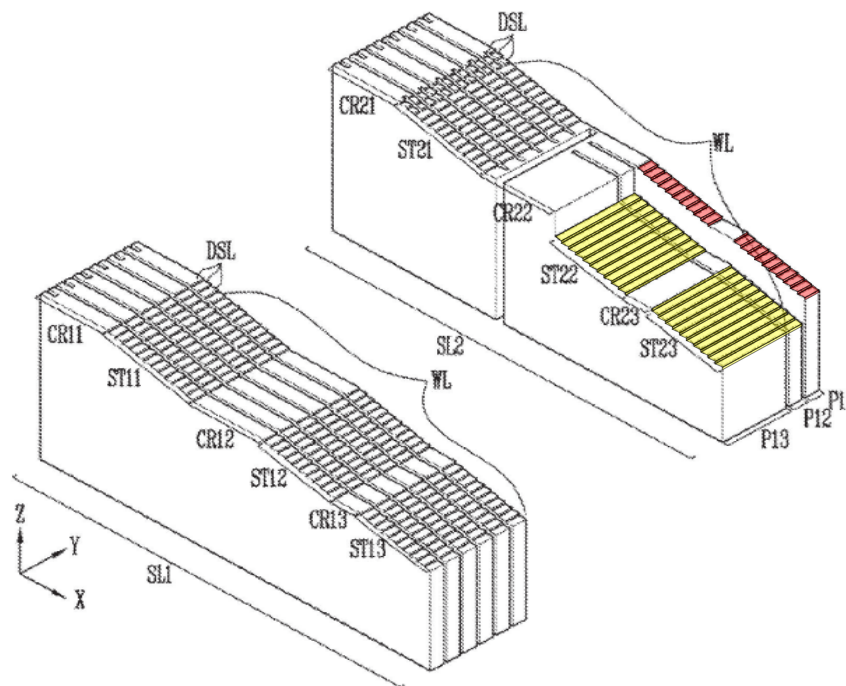
regions ST22 and T23 (“*at least one stair step region*”). EX1003, ¶275. Each etching process using a chop mask also results in the reduction of the area (“*at least one stair step region*”) of the newly “chopped” stepped structures (“*stair step structures*”). EX1003, ¶275.

For claim 16, in view of the common knowledge evidenced by AAPA-2 and as further explained in Section VII.H, a POSITA would have understood, or at least found it obvious, that after the first etching process using the single step mask to form the gate lines in a step form (“*after using the stair step mask*”), a second etching process using a first chop mask is performed (“*using the at least one chop mask*”) to form the gate lines in a pad form. EX1004, FIGs. 7-8; EX1003, ¶¶279-280. As a result of the second etching process, the number of exposed ends (“*contact regions*”) of the gate lines in step region ST22 or ST23 is doubled, comparing Lee’s FIG. 8 with FIG. 7. EX1003, ¶281.

For claim 18, in view of the common knowledge evidenced by AAPA-2, and as further explained in Section VII.H, a POSITA would have understood, or at least found it obvious, that as shown in annotated FIG. 8 below, in the second etching process using the first chop mask, the first areas of step regions ST22 and ST23 overlapping pad region P11 (in red, “*a first portion of the stair step structures*”) are covered by the first chop mask, while the second areas of step regions ST22 and ST23 overlapping pad regions P12 and 13 (in yellow, “*a second portion of the stair*

step structures”) are exposed. EX1003, ¶291. As a result, only the second areas are etched (“chopped”). EX1003, ¶291. The same explanation applies to the second chop mask, referring to FIG. 9 as well. Thus, Lee discloses or suggests [18.a].

FIG. 8



EX1003 — FIG. BA

Lee specifically discloses “[r]eferring to FIG. 8, heights of the lines are decreased by etching the word lines included in the regions in which the 22nd step region ST22, ... and the 23rd step region ST23 of the second slimming region SL2 overlap the 12th pad region P12 and the 13th pad region P13.” EX1004, [0069]. As discussed above in Section VII.C, a pair of conductive layer 10b (including gate lines) and insulating layer 10a is a “*tier*.” Thus, Lee discloses [18.b].

Accordingly, Lee anticipates or otherwise renders obvious claims 15, 16, and 18.

L. Dependent Claim 17

Claim 17 further recites, “*forming the at least one stair step region comprises:*” “*forming the stair step mask over the stack while exposing a width of a first step*” [17.a], “*removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask*” [17.b], “*recessing an edge of the stair step mask to expose a width of a second step*” [17.c], and “*removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask*” [17.d].

Claim 17 requires nothing more than the well-known “trim-etch” process using a stair step mask to form stair step structures, which is also part of AAPA-2. EX1001, 9:30-49; EX1003, ¶284. Specifically, a POSITA would have known the following: (i) [17.a] is in AAPA-2 as “[a] stair step mask may be formed over the vertical memory block while leaving one step-width (*e.g.*, a width of one contact region 524 measured in the longitudinal direction *y*) exposed”; (ii) [17.b] is in AAPA-2 as “[o]ne or more tiers of conductive material (*e.g.*, of the conductive word lines 516) exposed through the stair step mask may be removed”; (iii) [17.c] is in AAPA-2 as “[a]n edge of the stair step mask may be removed to recess the edge of the stair step mask and to expose another step-width, in addition to the original

exposed step-width”; and (iv) [17.d] is in AAPA-2 as “[a]nother cycle of material removal may be performed to remove another one or more tiers of conductive material exposed through the recessed stair step mask.” EX1003, ¶284.

As explained in Section VII.H, the process shown in FIG. 7 of Lee discloses or suggests “*forming at least one stair step region comprising stair step structures using a stair step mask.*” Thus, given the common knowledge in the art of using the trim-etch process and stair step mask to form stair step structures, as evidenced by AAPA-2 and Freeman, a POSITA would have understood that Lee discloses or suggests [17.a]-[17.d]. EX1003, ¶287.

M. Dependent Claim 19

Claim 19 further requires “*forming the conductive vias comprises forming at least some of the conductive vias between the array of memory cells and the at least one stair step region.*”

As described above in Sections VII.B.5 and VII.J.4, Lee discloses “*forming conductive vias adjacent the array of memory cells*” and “*conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region.*” Thus, Lee anticipates or otherwise renders obvious claim 19.

VIII. GROUND 3: LEE IN VIEW OF FREEMAN RENDERS OBVIOUS CLAIMS 12 AND 14-19

As discussed in Section VII, Lee anticipates or otherwise renders obvious claims 12 and 14-19. To the extent further disclosures are required, Lee in view of Freeman renders these claims obvious.

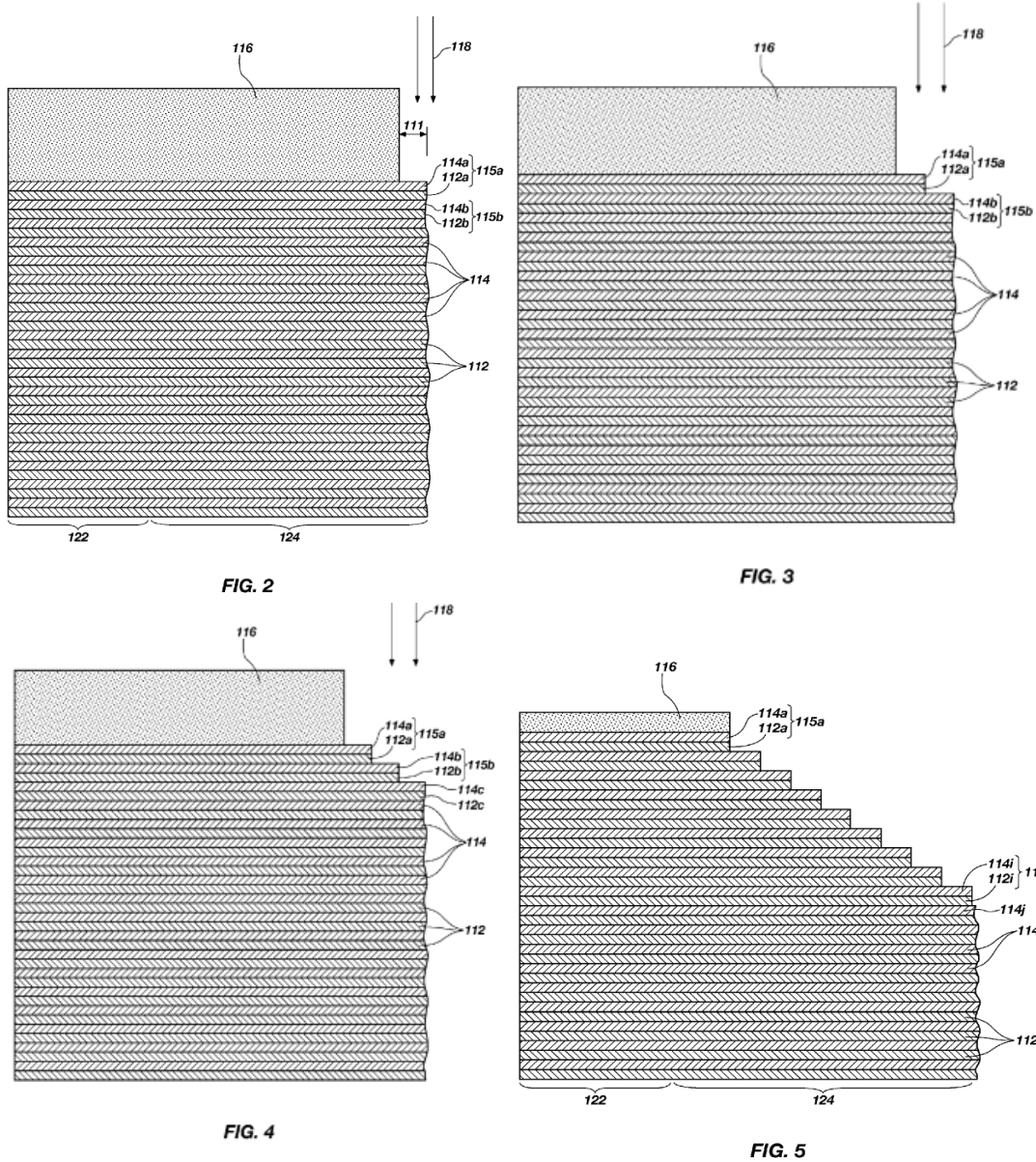
A. Overview of Freeman

Freeman also relates to 3D semiconductor devices, specifically, methods for forming stair-step structures and devices including stair-step structures. EX1005, [0001]. Freeman provides a detailed description of “[s]everal embodiments of stair-step structures and methods for forming stair-step structures,” by which “a margin of error in forming the plurality of stair-steps may be kept to a more reasonable and attainable level,” “a stair-step structure of the present disclosure may cover less area than some conventional stair-step structures,” and “a space between adjacent stair-step structures may be reduced in size.” EX1005, [0061].

Freeman’s stair-step structure forming method, in particular, the usage of a stair step mask and chop masks, matches well with AAPA-2 and supplements additional details. EX1003, ¶¶109-123, 285-286.

In Freeman’s first embodiment, a first mask 116, “referred to as a stair-step mask 116,” is used to form an intermediate stair-step structure 150 in a stair-step region 124. EX1005, [0028], [0035], FIG. 6. A second mask, “referred to as a chop

mask 126,” is then used to form a stair-step structure 100 having two regions 170 and 180 with separate contact regions. EX1005, [0036], [0038], FIG. 9.



EX1003 — FIG. R

First, in FIG. 2 above, stair-step mask 116 is patterned over a stack of conductive material 112 and insulating material 114b by removing a portion thereof at an outer edge of stair-step region 124, with the width 111 of a step. EX1005,

[0028]. Second, in FIG. 3 above, a portion of a first set 115a of insulating material 114a and conductive material 112a exposed through stair-step mask 116 is removed. EX1005, [0030]-[0031]. Third, still in FIG. 3, stair-step mask 116 is patterned again by removing another portion thereof (recessed) to expose another portion of insulating material 114a in first set 115a, with the width of a step. EX1005, [0032]. Fourth, in FIG. 4, the exposed portions of both first and second sets 115a and 115b are removed by one cycle of anisotropic etch 118. EX1005, [0033]. The processes described above in FIGs. 2-4 are repeated multiple times, as shown in FIG. 5, to form intermediate stair-step structure 150 in FIG. 6. EX1005, [0034]-[0035].

Freeman further discloses, as shown in FIG. 7 below, chop mask 126 is patterned over insulation layers 114, covering first region 170 of stair-step region 124, while leaving a second region 180 exposed. EX1005, [0036]. As shown in FIG. 8 below, the exposed second region 180 is then etched to remove materials from a number of sets 115 to expose sets 115 in the bottom portion of the stack, while leaving first region 170 covered by chop mask 126 intact. EX1005, [0037]. Once chop mask 126 is removed, stair-step structure 100, having separate contact regions in regions 170 and 180, is formed. EX1005, [0038], FIG. 9. Thus, the contact regions formed in FIG. 9 are doubled compared to the contact regions formed in FIG. 6 by using stair-step mask 116. EX1005, [0035], [0038]. By exposing second half of sets 115 to form additional contact regions in second region 180 in, an X-Y-plane

area of the newly “chopped” stair-step structure in second region 180 in FIG. 9 is reduced compared with an X-Y-plane area of intermediate stair-step structure 150 shown in FIG. 6. EX1005, [0042].

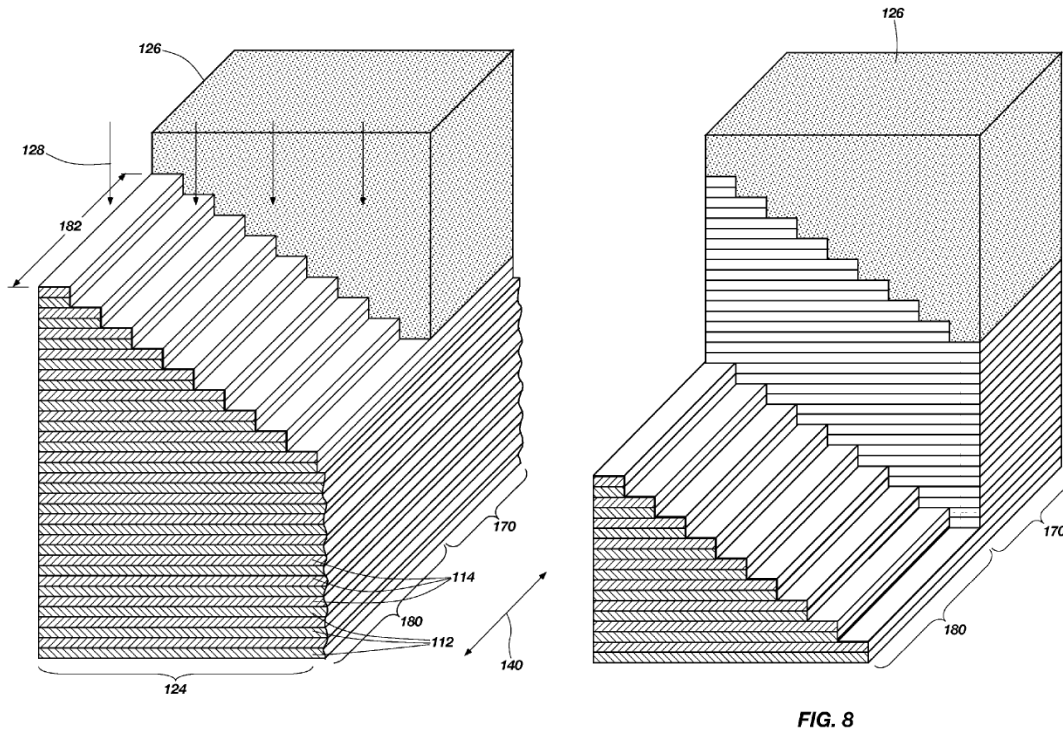


FIG. 7

FIG. 8

EX1003 — FIG. S

In the second embodiment, Freeman further discloses using a third mask 246 (a second chop mask in addition to second mask/first chop mask 236) to further form a stair-step structure 200 having four regions 241, 243, 261, and 263 with separate contact regions. EX1005, [0043]-[0046], FIG. 14. As shown in FIG. 13 below, second chop mask 246 is formed and patterned over exposed insulating material 214 to expose a second portion 243 of first region 240 and a second portion 263 of second region 260 and cover the rest portions. EX1005, [0045]. The exposed materials of

sets 215 in exposed portions 243 and 263 are then etched away to form stair-step structure 200 having separate contact regions in four regions 241, 243, 261, and 263.

EX1005, [0046], FIG. 14.

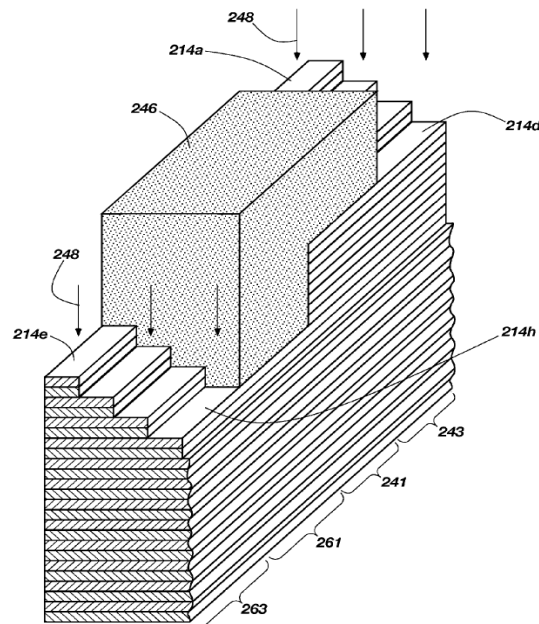


FIG. 13

EX1003 — FIG. U

B. Reasons to Combine Lee and Freeman

As discussed in Sections VII.J.5, VII.J.6, and VII.K-VII.L, Lee discloses, or at least suggests, the various claim limitations related to using “*a stair step mask*” ([14.d] and claim 17) and “*at least one chop mask*” ([14.e], claims 15, 16, and 18) in “*forming at least one stair step region*” (collectively “mask limitations”).

Additionally, the claimed invention requiring the mask limitations would have been obvious to a POSITA in view of Lee and Freeman, based on the “interrelated teachings of multiple patents” from Lee and Freeman. *Plantronics, Inc. v. Aliph, Inc.*,

724 F.3d 1343, 1354 (Fed. Cir. 2013). A POSITA, examining Lee's methods for forming stepped structures in FIGs. 7-10 alongside Freeman's explicit teachings in FIGs. 2-14, which describe using a stair-step mask and a chop mask to form similar stair-step structures, would have understood, or at least found it obvious, that Lee also employs the stair-step mask and chop masks in its stepped structure forming method. EX1003, ¶299.

For instance, as shown in FIG. BE of Orlowski Decl. below, comparing FIG. 7 of Lee (top) and FIGs. 5-6 of Freeman (bottom), a POSITA would have understood that Lee's present stepped structures (in red) in step regions ST22 and ST23 of FIG. 7 are substantially the same as Freeman's intermediate stair-step structure 100 (in red) of FIG. 6. EX1003, ¶300. Thus, a POSITA would have found it obvious to combine Freeman's interrelated teachings of the process (as shown in FIG. 5), which would result in the same stepped structure of Lee, supplementing any missing details of Lee, including the usage of stair-step mask 116, because forming intermediate stair-step structure 100 requires stair-step mask 116. Sections VII.H, VIII.A; EX1003, ¶300.

FIG. 7

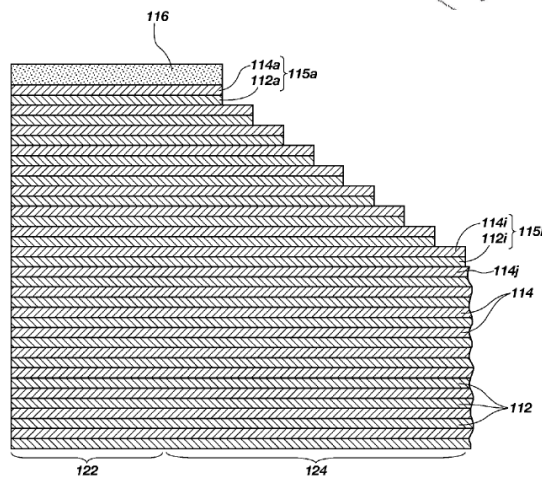
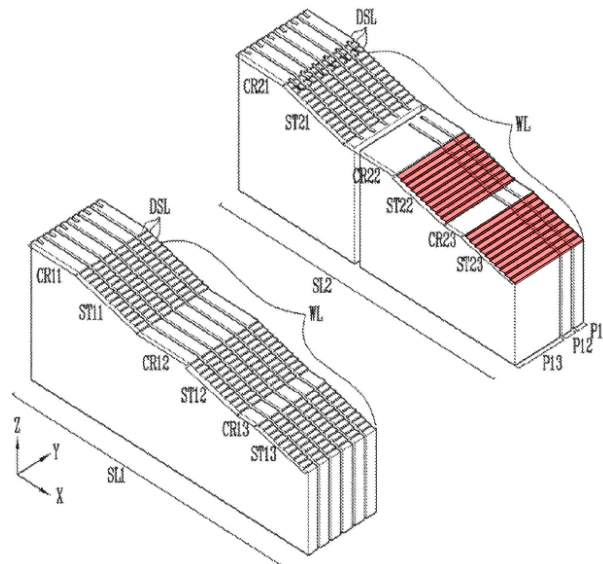


FIG. 5

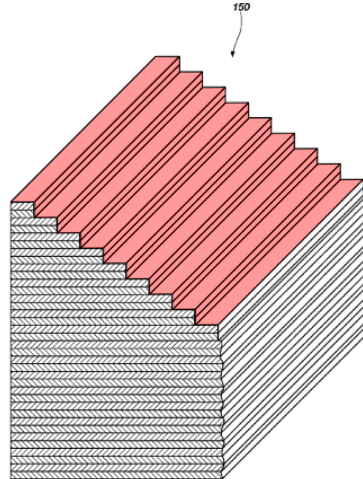


FIG. 6

EX1003 — FIG. BE
(Comparison of FIG. 7 of Lee with FIGs. 15-16 of Freeman)

Next, as shown in FIG. BF of Orłowski Decl. below, comparing FIG. 8 of Lee (top) and FIGs. 11-12 of Freeman (bottom), a POSITA would have understood that Lee's present stepped structures (in red and yellow) in step regions ST22 and ST23 of FIG. 8 are substantially the same as Freeman's current stair-step structures (in red and yellow) of FIG. 12. EX1003, ¶301. Thus, a POSITA would have found it

obvious to combine Freeman’s interrelated teachings of the process (as shown in FIG. 11), which would result in the same stepped structures of Lee, supplementing any missing details of Lee, particularly the usage of first chop mask 236, because forming the current stair-step structure requires using first chop mask 236. Sections VII.H, VIII.A; EX1003, ¶301.

FIG. 8

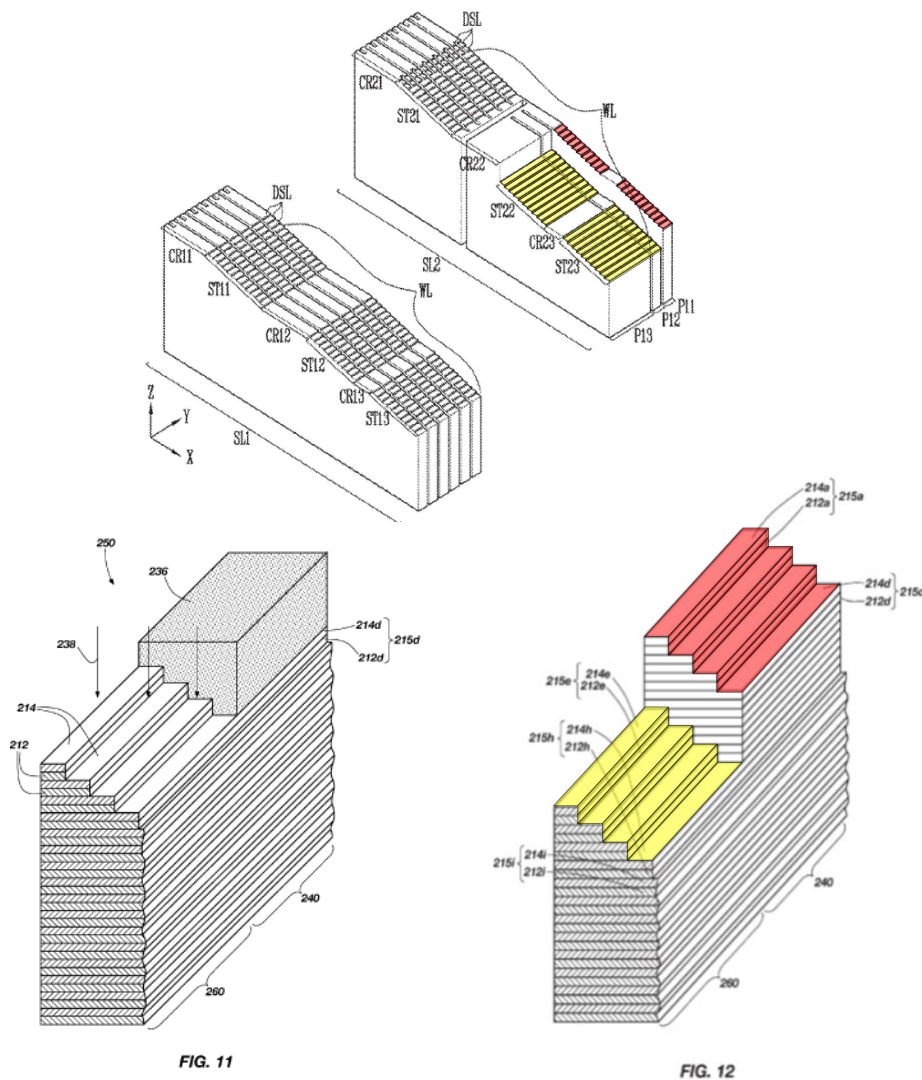


FIG. 11

FIG. 12

EX1003 — FIG. BF

(Comparison of FIG. 8 of Lee with FIGs. 11-12 of Freeman)

Subsequently, as shown in FIG. BG of Orlowski Decl. below, comparing FIG. 9 of Lee (top) and FIGs. 13 and 14 of Freeman (bottom), a POSITA would have understood that Lee's stepped structures (in red, yellow, and blue) in step regions ST22 and ST23 of FIG. 9 are substantially the same as Freeman's stair-step structure 200 (in red, yellow, and blue) of FIG. 14. EX1003, ¶302. Thus, a POSITA would have found it obvious to combine Freeman's interrelated teachings of the process (as shown in FIG. 13), which would result in the same stepped structures of Lee, supplementing any missing details of Lee, particularly the usage of second chop mask 246, because forming stair-step structure 200 requires second chop mask 246. Sections VII.H, VIII.A; EX1003, ¶302.

FIG. 9

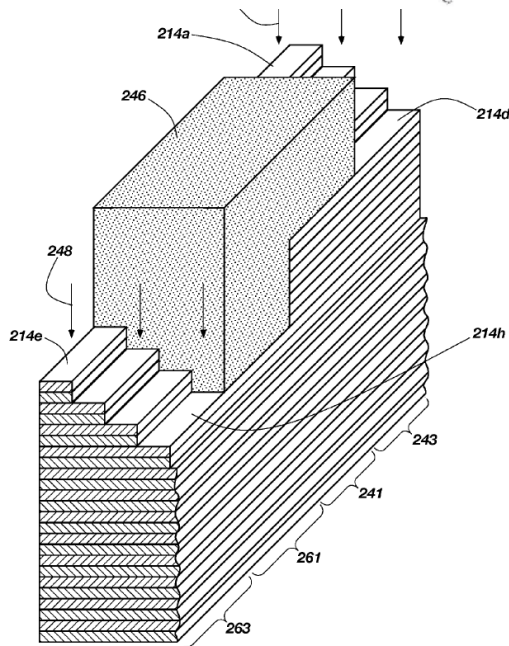
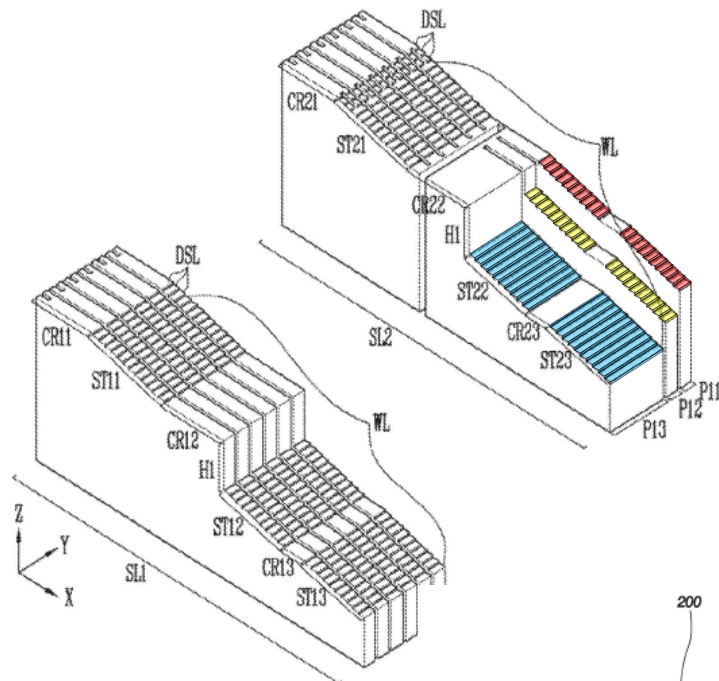


FIG. 13

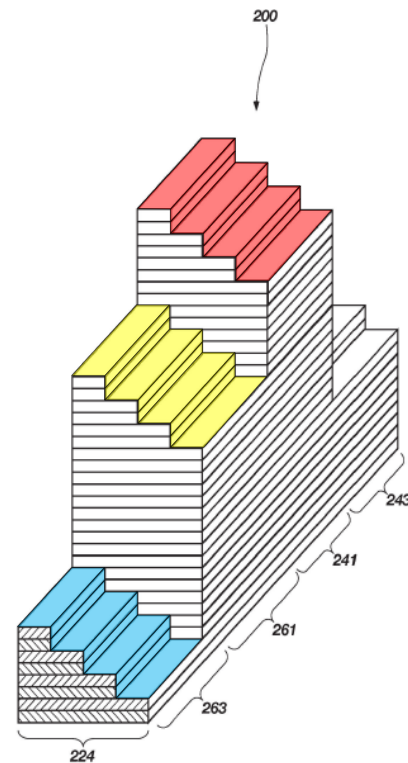


FIG. 14

EX1003 — FIG. BG
(Comparison of FIG. 9 of Lee with FIGs. 13-14 of Freeman)

For at least these reasons, a POSITA would have found it obvious to combine Lee and Freeman, supplementing Lee's stepped structure forming method with Freeman's express teachings of using a stair-step mask and chop masks to form stair step structures, resulting in the claimed invention's mask limitations. EX1003, ¶303.

C. Independent Claim 14 and Dependent Claims 12, 15, 16, 18, and 19

To the extent that additional disclosures are required to render obvious claims 12, 14-16, 18, and 19 besides Lee's disclosures and suggestions explained in Sections VII.H, VII.J, VII.K, and VII.M, Freeman provides explicit teachings of the mask limitations. Section VIII.A. A POSITA would have found it obvious to combine Lee and Freeman to arrive at the claimed invention as recited in claims 12, 14-16, 18, and 19. Section VIII.B.

D. Dependent Claim 17

As discussed in Section VII.L, Lee discloses or suggests [17.a]-[17.d]. To the extent that additional disclosures are required, a POSITA would have found it obvious to combine Lee and Freeman to supplement Freeman's additional processing details of using the stair step mask regarding [17.a]-[17.d], as discussed below, to Lee's process of FIG. 7. Sections VII.H, VIII.B.

1. **Lee in view of Freeman renders obvious “*forming the stair step mask over the stack while exposing a width of a first step*” [17.a].**

Besides the prior art shown in FIG. 1A, Freeman also discloses forming stair-

step mask 116 “over the topmost set 115a of conductive material 112a and insulating material 114a” to “expose a portion of a major surface of the topmost insulating material 114a in the stair-step region 124 that has a width 111 of approximately a desired width of the step to be formed.” EX1005, [0004], [0028], FIG. 2; Section VIII.A. Thus, Lee in view of Freeman renders obvious [17.a].

2. Lee in view of Freeman renders obvious “*removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask*” [17.b].

Besides the prior art shown in FIG. 1B, Freeman further discloses removing a portion of first set 115a of conductive material 112a and insulating material 114a (“*at least one tier of the dielectric materials and the conductive materials*”) exposed through stair step mask 116. EX1005, [0004], [0030], FIG. 3; Section VIII.A. Thus, Lee in view of Freeman renders obvious [17.b].

3. Lee in view of Freeman renders obvious “*recessing an edge of the stair step mask to expose a width of a second step*” [17.c].

Besides the prior art shown in FIG. 1B, Freeman further discloses removing an end portion of staircase mask 116 (“*recessing an edge of the stair step mask*”) “to the extent that the portion of the first insulating material 114a that is exposed exhibits a width that is approximately a desired width of a step.” EX1005, [0004], [0032], FIG. 3; Section VIII.A. Thus, Lee in view of Freeman renders obvious [17.c].

4. **Lee in view of Freeman renders obvious “*removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask*” [17.d].**

Besides the prior art shown in FIG. 1C, Freeman further discloses removing a portion of second set 115b of conductive material 112b and insulating material 114b (“*another tier of the dielectric materials and the conductive materials*”) exposed through stair step mask 116. EX1005, [0005], [0033], FIG. 4; Section VIII.A. Thus, Lee in view of Freeman renders obvious [17.d].

Accordingly, Lee in view of Freeman renders obvious claim 17.

IX. GROUND 4: LEE IN VIEW OF LIM RENDERS OBVIOUS CLAIM 13

As discussed above in Section VII, Lee anticipates or otherwise renders obvious claim 13. To the extent element [13.b] of claim 13 requires “*forming the conductive vias in the via region*” and “*isolating the conductive vias,*” when “*the stack of alternating dielectric materials*” still exists, Lee in view of Lim suggests [13.b] and thus, renders claim 13 obvious.

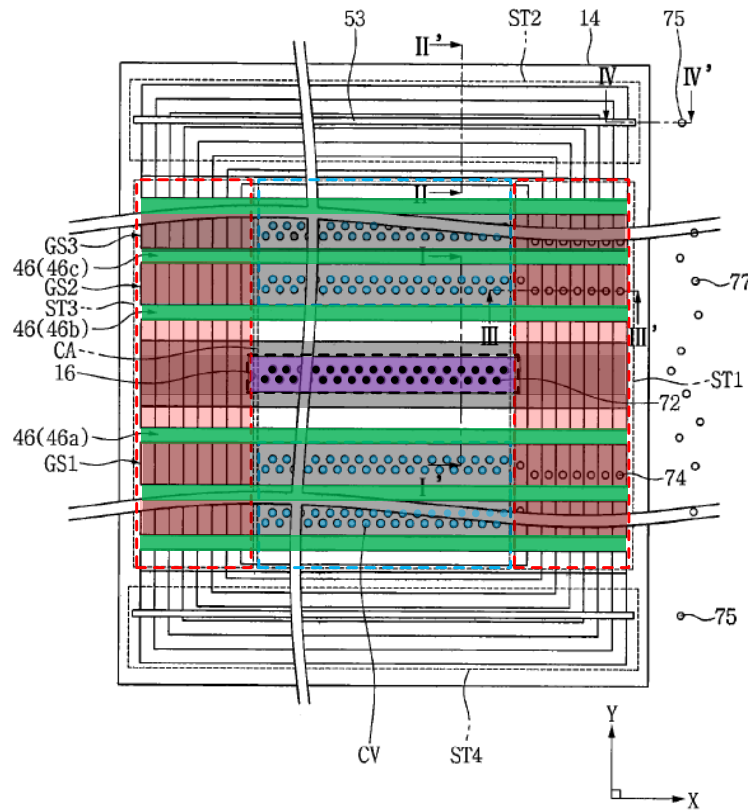
A. Overview of Lim

Lim relates to semiconductor devices and manufacturing methods thereof. EX1006, [0003]; EX1008, ¶1. Lim recognizes the need for increasing semiconductor devices’ degree of integration in reducing their costs. EX1006, [0005]; EX1008, ¶2. Lim provides various designs and fabrication processes related

to TAVs to improve the degree of integration. EX1006, [0320]-[0321]; EX1008, ¶¶14-15.

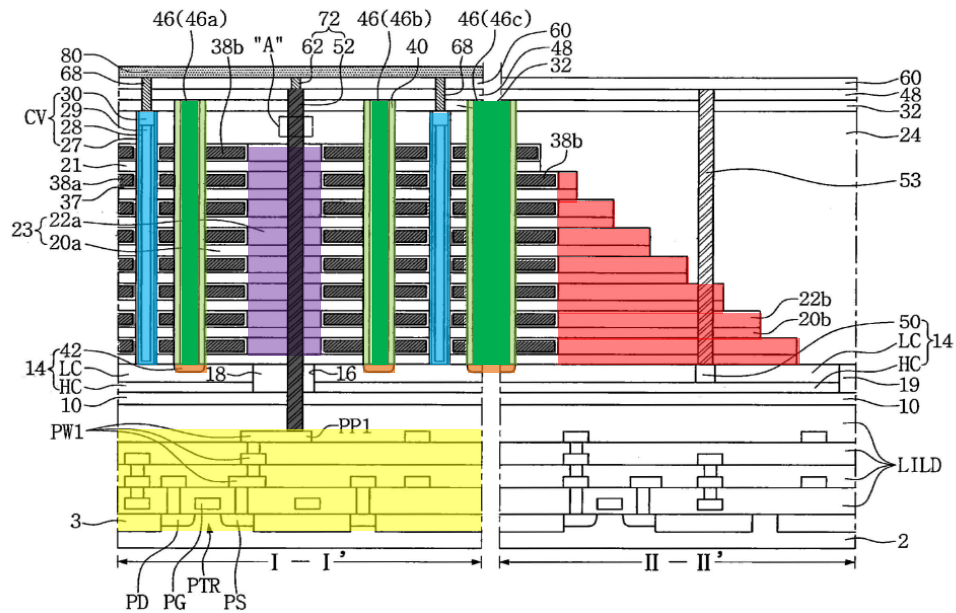
Similar to '974 patent and Lee, as shown in annotated FIGs. 2A and 3A below, Lim, in a first embodiment, discloses a semiconductor device including (i) cell array areas CA (in blue dashed boxes, “*memory cell region*”) where cell vertical structures CV (in blue, “*memory cells*”) are formed, (ii) an area (in black dashed box, “*via region*”) where bit line lower contact plugs 52 (in black, “*conductive vias*”) are formed, and (iii) step areas ST1 and ST3 (in red dashed boxes, “*stair step regions*”) at opposing ends, each having step structures (in red, “*stair step structures*”). EX1006, [0086], [0089], [0098], [0109]-[0110]; EX1008, ¶¶38, 41, 50, 61-62; EX1003, ¶¶125-131.

FIG. 2A



EX1003 — FIG. W

FIG. 3A



EX1003 — FIG. X

As shown in Lim's FIGs. 2A and 3A above, cell source patterns 46³ (in green, "slots"), including insulating spacers 40 (in light green in FIG. 3A, *e.g.*, silicon oxide, "a dielectric material within slots"), are formed to "cross the cell array area CA and to extend into the first and third step areas ST1 and ST3." EX1006, [0104]; EX1008, ¶¶56, 180, 229. Parallel cell source patterns 46 with different distances are formed along the Y-direction (bit line direction), each of which extends in the X-direction (word line direction). EX1006, [0104], [0106]; EX1008, ¶¶56, 58. Further, cell gate conductive structures GS1, GS2, and GS3 (in gray) "extend from the cell array area CA into the first and third step areas ST1 and ST3," and each cell gate conductive structure GS1, GS2, or GS3 includes cell gate conductive patterns 38a (in FIG. 3A, "access line portions"), which are stacked and spaced apart from each other so as to have a step structure in step areas ST1 and ST3. EX1006, [0087], [0089]; EX1008, ¶¶39, 41.

To improve the integration degree of the semiconductor device, Lim discloses various forms of TAVs, which "vertically pass through the memory cell array area or is disposed at a location close to the memory cell array area" to provide vertical electrical connections to underneath components. EX1006, [0321]; EX1008, ¶15;

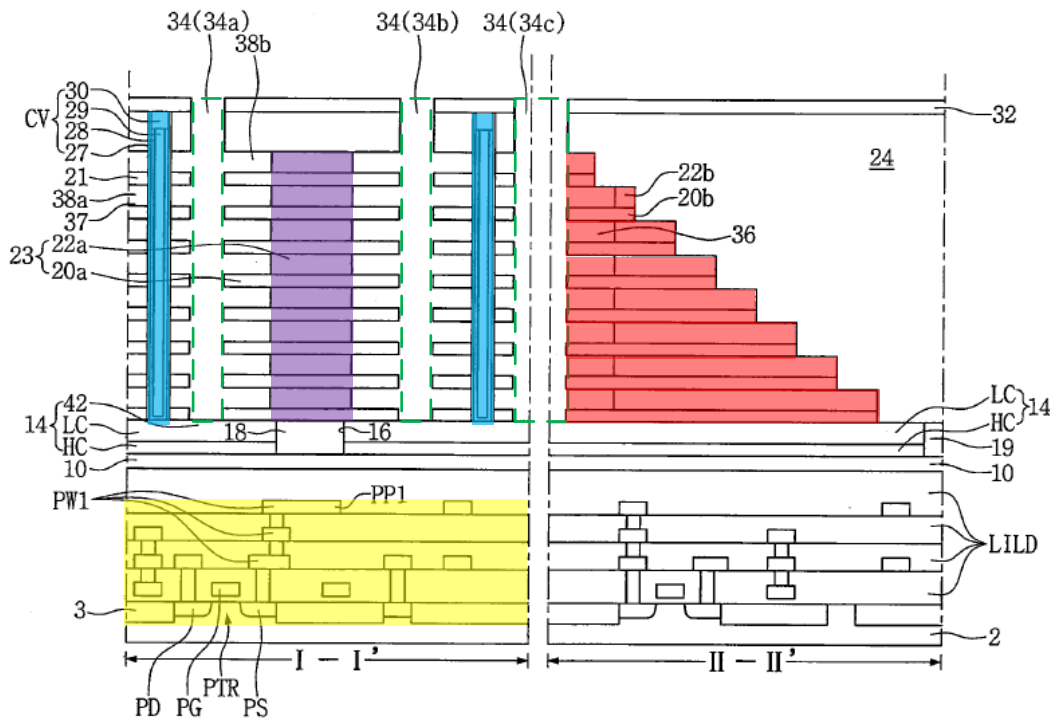
³ Cell source patterns 46 are formed by depositing a dielectric material (as insulating spacers 40) and a conductive material (as source contacts) in trenches 34. EX1006, [0228], [0230]; EX1008, ¶¶180, 182,

EX1003, ¶130. For example, as shown in FIG. 3A above, Lim discloses contact plug 52 (in black) extending vertically through an insulating structure 23 (in purple) to be electrically connected to peripheral transistor PTR (in yellow, “*sub-array circuitry*”) underneath the memory block. EX1006, [0110]; EX1008, ¶62. Particularly, like ’974 patent, insulating structure 23 through which contact plug 52 passes includes a stack of alternating first and second insulating patterns 20a and 22a (*e.g.*, silicon oxide and silicon nitride, respectively, “*a stack of alternating dielectric materials*”). EX1006, [0092]-[0093]; EX1008, ¶¶44-45; EX1003, ¶131.

Lim further discloses the detailed fabrication process of making the semiconductor device, including the process for forming the step structures. EX1006, FIGs. 19-26B, [0196]-[0197], [0208], [0227]; EX1008, ¶¶148-149, 160, 179. In particular, to form contact plugs 52 extending vertically through the stack of alternating first and second insulating patterns 20a and 22a, Lim discloses, with respect to FIG. 23A, a partial gate replacement process modified from the well-known gate replacement process. EX1003, ¶133. As shown in annotated FIG. 23A below, forming “second and third trenches 34b and 34c in FIG. 23A [] more closely spaced apart from each other than the first and second trenches 34a and 34b,” results in partial etching of second molding layers 22 (*e.g.*, silicon nitride) exposed by trenches 34 (highlighted in green dashed boxes). EX1006, [0219], [0221]-[0222], [0225]; EX1008, ¶¶171, 173-174, 177. Consequently, portions of second molding

layers 22 that lie between the more widely spaced first and second trenches 34a and 34b remain **partially etched**, ultimately forming a stack of alternating first and second insulating patterns 20a and 22a (collectively referred to as insulating structure 23, in purple). EX1003, ¶¶134-135.

FIG. 23A



EX1003 — FIG. Y

Eventually, contact plugs 52 passing through insulating structure 23 are formed by “forming contact holes by performing a photolithography process and an etching process, and forming a conductive material layer which fills the contact holes” at the same processing steps with other contact structures 53, 54, and 55. EX1006, [0233]-[0234], [0240], FIGs. 26A-26B; EX1008, ¶¶185-186, 192, FIGs.

26A-26B; EX1003, ¶138.

B. Reasons to Combine Lee and Lim

A POSITA would have found it obvious to combine Lee and Lim for various reasons discussed below in detail.

Specifically, a POSITA would have been motivated to modify Lee in view of Lim to form Lee's contact plugs 52 in the remaining alternating dielectric stack, instead of blocking layers 31, of the memory block, thereby simplifying the manufacturing process. EX1003, ¶340.

1. The teaching, suggestion, and motivation in Lee and Lim would have led a POSITA to apply Lim's partial gate replacement process to form Lee's contact plugs in the remaining alternating dielectric stack.

Lee aims to reduce semiconductor device size and improve integration degree, as well as simplify the manufacturing process and reduce costs. EX1004, [0009]. While Lee discloses forming contact plugs 32 in blocking layers 31, which "may be formed of an insulating material such as an oxidization layer," Lee does not specify the timing of forming blocking layers 31 and contact plugs 32 within its fabrication process flow. EX1004, [0077]; EX1003, ¶341.

As discussed in Section IX.A, Lim, in the first embodiment, discloses the partial gate replacement process for forming insulating structure 23 having a stack of alternating first and second insulating patterns 20a and 22a (FIG. 23A). In

contrast, Lim, in a second embodiment in connection with FIGs. 10, 11A, 11B, and 29-32B, discloses forming contact plugs 52 through insulating structure 123 formed of silicon oxide, analogous to Lee's contact plugs 32 formed through blocking layers 31. EX1006, [0140], [0144], FIG. 11A; EX1008, ¶¶92, 96, FIG. 11A; EX1003, ¶342. Comparing the process flows of these two embodiments, a POSITA would have understood that, to form insulating structure 123, Lim added an extra step (340 in FIG. 29, FIG. 30A) prior to gate replacement in the second embodiment. EX1006, [0269]; EX1008, ¶222; EX1003, ¶343. That is, Lim teaches or at least suggests saving extra steps for forming insulating structure 123 by performing a partial gate replacement process that results in simultaneously forming insulating structure 23, allowing contact plugs 52 to be formed later through the existing dielectric materials of insulating structure 23. EX1003, ¶¶343-344.

Since Lee's contact plugs 32 are formed in blocking layers 31, which are analogous to Lim's insulating structure 123 in the second embodiment, a POSITA would have understood, or at least found it obvious, that Lee also employs an analogous process to form blocking layers 31 as Lim's second embodiment. EX1003, ¶345. Therefore, a POSITA would have found it obvious to apply Lim's partial gate replacement process in its first embodiment to eliminate the need to form blocking layers 31, thereby reducing the number of processing steps to advance Lee's goal of simplifying manufacturing and reducing costs. EX1003, ¶¶346-347.

Moreover, a POSITA would have been further motivated to incorporate a partial gate replacement process into Lee's fabrication method to avoid mechanical failures. EX1003, ¶348. As illustrated in FIG. 23A of Lim, the remaining stack of alternating dielectric materials (insulating structure 23) can provide mechanical support to insulating patterns 20a/20b. This support prevents collapsing or bending when empty spaces 36 are formed between insulating patterns 20a/20b during gate replacement. EX1006, [0221], FIG. 23A; EX1008, ¶173, FIG. 23A. By leveraging this structural support, additional supporting structures become unnecessary, thereby reducing device size and simplifying the manufacturing process. EX1003, ¶348.

2. A POSITA would have a reasonable expectation of success in applying Lim's known partial gate replacement technique to Lee's fabrication process to form Lee's contact plugs in an alternating dielectric stack.

Lim's partial gate replacement technique is applicable to Lee's fabrication process flow for forming contact plugs 32 because of the great similarities between Lee and Lim. As discussed in Sections VII.A and IX.A, both Lee and Lim's semiconductor devices have substantially the same features in terms of the claimed invention. EX1003, ¶349. Particularly, both Lee and Lim have under-array circuits, as well as TAVs (*e.g.*, contact plugs 32 of Lee and contact plugs 52 of Lim) to access the under-array circuits. Additionally, both Lee and Lim share the same integration goals, utilizing TAVs to achieve these objectives.

It is well within a POSITA's capabilities to apply partial gate replacement to Lee's fabrication process without undue burdens and with a reasonable expectation of success. Lim provides explicit guidance, particularly setting the distance between adjacent trenches 34 to control the location and extent of the partial gate replacement. EX1006, [0219], [0222], FIGs. 2A, 3A; EX1008, ¶¶171, 174, FIGs. 2A, 3A; EX1003, ¶350. Based on this guidance, along with other common knowledge in the art, a POSITA would be able to easily implement various viable designs of applying a partial gate replacement process to Lee's device and process. EX1003, ¶350.

For instance, the adjacent slots in Lee can be spaced apart at a sufficient distance in contact region CR21 to enable partial gate replacement. EX1003, ¶351. This design would result in the stack of alternating dielectric materials remaining in contact region CR21 after gate replacement, serving as the insulating structure for contact plugs 32. A POSITA would have understood, or at least found it obvious, to adjust the spacing between adjacent slots in different regions (e.g., by designing the slots in non-straight lines) to selectively prevent partial gate replacement where necessary. EX1003, ¶352. For example, in memory region MC, this approach could help avoid reducing cell density.

Additionally, a POSITA would have recognized that this approach would not introduce additional processing steps. EX1003, ¶353. After partial gate replacement, Lee's contact plugs 32 can be formed through the remaining stack of

alternating dielectric materials alongside other contact plugs, using the same contact hole etching and conductive material deposition steps—similar to Lim’s TAV formation process shown in FIGs. 26A-26B.

C. Dependent Claim 13

As discussed in Section VII.E, Lee anticipates or otherwise renders obvious independent claim 7 on which claim 13 depends.

Claim 13 additionally recites [13.a] and [13.b]. As discussed in Section VII.I, Lee alone discloses or suggests [13.a] and [13.b].

Additionally, Lim discloses forming a molding structure MS, including alternating first and second dielectric molding layers 20 (*e.g.*, silicon oxide) and 22 (*e.g.*, silicon nitride) (“*a stack of alternating dielectric materials*”). EX1006, [0208]-[0209], [0216], FIGs. 21A-21B; EX1008, ¶¶160-161, 168, FIGs. 21A-21B. Lim further discloses forming cell vertical structures CV (“*vertical memory cell pillars*”) within molding structure MS. EX1006, [0211]-[0214], FIGs. 22A-22B; EX1008, ¶¶163-166, FIGs. 22A-22B. Lim thus also discloses [13.a].

To the extent [13.b] requires the timing of “*forming the conductive vias in the via region*” and “*isolating the conductive vias,*” especially when “*the stack of alternating dielectric materials*” still exists (which Petitioner does not concede as explained in Section VII.I.2), Lim discloses the partial gate replacement process in forming its semiconductor device, as explained above in Section IX.A. EX1006,

[0221]-[0222], [0225], FIG. 23A; EX1008, ¶¶173-174, 177, FIG. 23A; EX1003, ¶360. The partial gate replacement process results in insulating structure 23 having alternating first and second insulating patterns 20a and 22a, which is part of molding structure MS. EX1003, ¶361. Lim further discloses forming contact plugs 52 (“*conductive vias*”) by etching contact holes through insulating structure 23 (“*stack of alternating dielectric materials*”), and forming a conductive material layer filling the contact holes, thereby isolating contact plugs 52 from cell gate conductive patterns 38a. EX1006, [0233]-[0234], [0240], FIG. 26A; EX1008, ¶¶185-186, 192, FIG. 26A; EX1003, ¶361.

Therefore, Lim discloses [13.b] even under a narrower interpretation.

As discussed in Section IX.B, a POSITA would have found it obvious to form Lee’s contact plugs 32 (“*conductive vias*”) using Lim’s partial gate replacement process, such that the number of processing steps can be reduced, thereby simplifying the manufacturing process and reducing costs. EX1003, ¶363.

Accordingly, Lee in view of Lim renders obvious claim 13.

X. DISCRETIONARY DENIAL DOES NOT APPLY

A. 35 U.S.C. § 325(d)

Under the two-part *Advanced Bionics* framework, the Board should not exercise discretion to deny institution under 35 U.S.C. § 325(d).

Lee and Lim have never been presented or otherwise considered by the Office during the original examination of '974 patent or any parent patents. *See generally* EX1002. As to Freeman, while its issued patent (U.S. Patent No. 8,530,350) was cited in an IDS submitted by PO during the prosecution of '974 patent, there was no substantive discussion regarding any of the challenged claims. EX1002, 82, 103. None of the grounds raised in this Petition have ever been presented, much less discussed, during the original examination.

Even if any of the cited art or arguments in this Petition were considered the same or substantially the same as those raised during the prosecution of '974 patent or any parent patents, the Examiner erred in a manner material to the patentability of the challenged claims by not rejecting the challenged claims over the prior art and arguments presented herein. For instance, at least the alleged allowable subject matters related to “*stair step structures*,” “*conductive vias*,” and “*a dielectric material within slots*” (Section V.B) are anticipated or otherwise rendered obvious in view of the cited art in Grounds 1-4.

Specifically, the Examiner overlooked the disclosures of Freeman during the original examination, as demonstrated in Ground 3, which clearly shows the alleged allowable mask limitations. Sections VIII.C and VIII.D. Here, the new and additional evidence and facts presented in Ground 3 with respect to Freeman warrant reconsideration of Freeman.

B. 35 U.S.C. § 314(a)

As stated in Section II.B, there is no currently pending parallel district court litigation addressing '974 patent. To the extent the potential addition of '974 patent to the NDCA case warrants a *Fintiv* analysis⁴, discretionary denial would be improper due to exceptional circumstances. *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020).

As noted above at FN1, after the Court dismissed PO's counterclaims for alleged infringement of '974 patent with leave to amend, PO declined to amend its pleadings and instead withdrew its assertion of '974 patent in August 2024. Moreover, minimal investment was made in '974 patent before its dismissal—indeed, PO's counterclaims were dismissed due to deficiencies in pleading infringement. EX1022, 1.

This Petition is being filed before the Court decides whether to allow PO to amend its counterclaims, and PO's motion to reassert '974 patent was filed only two weeks before this Petition. EX1024. In addition to the compelling merits of the grounds in this Petition—including the anticipation and single-reference obviousness grounds—these exceptional circumstances warrant institution as a

⁴ Petitioner reserves the right to address *Fintiv* in view of the facts and the law as they stand following the POPR, should the PO argue for denial under *Fintiv*.

matter of fairness.⁵

XI. CONCLUSION

Based on the grounds specified above, IPR of all challenged claims is respectfully requested.

Respectfully submitted,

BAYES PLLC

/Zhiwei Zou/

Zhiwei (Wayne) Zou

Registration No. 66,041

Lead Counsel for Petitioner

Date: February 13, 2025

8260 Greensboro Drive, Suite 625

McLean, VA 22102

(703) 995-9887

⁵ To the extent '974 patent becomes reasserted in the NDCA case, if this IPR is instituted, Petitioner will not pursue the same grounds of invalidity in the district court litigation. *Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 11-12 (PTAB June 16, 2020).

CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

This Petition complies with the requirements of 37 C.F.R. § 42.24. As calculated by the word count feature of Microsoft Word, it contains 13,974 words, excluding the words contained in the following: Table of Contents, Table of Authorities, List of Exhibits, Mandatory Notices, Certification Under § 42.24(d), and Certificate of Service.

/Zhiwei Zou/

Zhiwei (Wayne) Zou

Registration No. 66,041

Lead Counsel for Petitioner

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing **Petition for *Inter Partes* Review**, **the associated Power of Attorney, and Exhibits 1001-1024** are being served on February 13, 2025, by U.S. Priority Express Mail at the following address of record for the subject patent.

63162 - TRASK BRITT, P.C./ MICRON TECHNOLOGY
230 South 500 East
Suite 300
Salt Lak City, UT 84102

A courtesy copy was also sent via electronic mail to Patent Owner's litigation counsel at the following addresses:

Jared Bobrow (CA State Bar No. 133712)
jbobrow@orrick.com
J. Jason Lang (CA State Bar No. 255642)
jlang@orrick.com
Diana Rutowski (CA State Bar No. 233878)
drutowski@orrick.com
ORRICK, HERRINGTON & SUTCLIFFE LLP

/Ashley F. Cheung/
Ashley F. Cheung
Paralegal for Petitioner's Counsel