
UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.

Petitioner

v.

MICRON TECHNOLOGY, INC.

Patent Owner

IPR2025-00501

U.S. PATENT 10,373,974

**DECLARATION OF DR. MARIUSZ K. ORLOWSKI IN SUPPORT OF
PETITION FOR *INTER PARTES REVIEW* OF U.S. PATENT 10,373,974**

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I, Mariusz Orlowski of Pembroke, Virginia, declare that:

I. Introduction

1. My name is Mariusz Orlowski, and I have been retained by counsel for Petitioner Yangtze Memory Technologies Company, Ltd. (“YMTC” or “Petitioner”) as an expert witness to provide assistance regarding U.S. Patent No. 10,373,974 (“the ’974 Patent”) assigned to Micron Technology, Inc. (“Micron” or “Patent Owner”). Specifically, I have been asked to consider the validity of claims 1, 4, 5, 7, 9, and 11-19 of the ’974 Patent (the “Challenged Claims”) in view of prior art, anticipation and obviousness considerations, and understanding of a person of ordinary skill in the art at the time of the invention (“POSITA”) as it relates to the ’974 Patent. I have personal knowledge of the facts and opinions set forth in this declaration and believe them to be true. If called upon to do so, I would testify competently thereto.

2. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or on the pending litigation between Petitioner and Patent Owner.

3. My analysis here is based on my years of education, research and

experience, as well as my investigation and study of relevant materials, including those cited herein.

4. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

5. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. Background and Qualifications

6. I am an expert in the field of semiconductor devices. I have studied, taught, practiced, and researched this field for over 40 years. I have summarized in this section my educational background, work experience, and other relevant qualifications. Attached hereto as Appendix A, is a true and correct copy of my *curriculum vitae* describing my background and experience.

7. I am currently a Professor in the Bradley Department of Electrical and Computer Engineering at Virginia Polytechnic Institute and State University (“Virginia Tech”) in Blacksburg, Virginia, where I held for ten years the prestigious

Virginia Microelectronics Consortium Chair. Established in 1997 by the State of Virginia, the Virginia Microelectronics Consortium includes six universities and two semiconductor companies.

8. I earned a Master's degree in Experimental Physics in 1976 and a Ph.D. in Theoretical Physics in 1979, both from Tuebingen University, Germany. I have over 25 years of experience in the semiconductor industry, specializing in the physics and manufacturing of semiconductor devices.

9. At the beginning of my career (1979–1984), I held technical positions at Stanford University, Purdue University, and the German Space Agency in Stuttgart-Vaihingen, Germany. I then spent 25 years in the semiconductor industry, first at Siemens Laboratories (1984–1989) and later at Motorola Laboratories (1989–2004), whose semiconductor division became Freescale Semiconductor (2004–2008). Since 2008, I have been a professor at Virginia Tech, continuing my research in semiconductor device physics and technology.

10. While at Siemens in the 1980s, I conducted pioneering research on the physics of metal-oxide-semiconductor field-effect transistors (MOSFETs), the fundamental building blocks of all mainstream integrated circuits. In 1987, I published the first explanation of the “reverse short channel effects,” now a standard feature of advanced MOSFETs. In 1989, I provided an in-depth analysis predicting degradation effects in MOSFETs, further advancing the understanding of these

devices.

11. At Motorola, my research focused on nonvolatile memories and associated phenomena, including band-to-band tunneling. In 1990, I was the first to calculate and correctly predict new modes of band-to-band tunneling in MOSFETs, along with its impact on nonvolatile memory technologies.

12. In addition to my research, I successfully managed the development of numerous technologies. While working with the Crolles consortium in Grenoble, France, comprising Motorola (Freescale), Philips (NXP), and STMicroelectronics, I led the development of a 50 nm fully-depleted silicon-on-insulator (SOI) MOSFET with a TiN/HfO₂ gate stack and a 30 nm gate length SOI MOSFET. At Motorola, I established and managed several R&D groups, including the first Technology Computer-Aided Design (TCAD) Modeling and Simulation group (1989–1995) and the first Equipment Modeling and Simulation group (1992–1995). I also led a Motorola-Freescale collaboration with SOFT-TEC, a company founded by prominent Russian scientists, comprising over 100 engineers and scientists.

13. In 1997, I was elected a Fellow of the Institute of Electrical and Electronics Engineers (IEEE) for my “contributions to MOSFET devices and technology.” This distinction is awarded to individuals who have made significant contributions to IEEE-designated fields, with Fellows representing no more than one-tenth of 1% of the total voting membership.

14. My work in semiconductors spans device development, process development, and process integration. I have made advancements in poly gate modules, LOCOS and trench isolation, gate oxide formation, spacer and liner processes, implantation, diffusion, and both isotropic and anisotropic etching.

15. I hold over 99 patents (including 72 U.S. patents). Many of these patents focus on nonvolatile device structures and manufacturing processes. My innovative contributions have been recognized with Motorola's Distinguished Innovator Award (1998) and Freescale's Master Innovator Award (2007). I have authored over 230 publications in referred journals and conference proceedings, with the majority focusing on semiconductor devices and processing technologies.

16. I also made significant contributions to the development of embedded NAND and NOR memory technologies at Motorola, particularly regarding floating gate memory cell performance, design, and manufacturing. My work addressed numerous device challenges, including:

- SONOS and nanocrystal non-volatile memory cells Two-bit charge storage and split-gate memory cells;
- Programming techniques such as Fowler-Nordheim tunneling, avalanche injection, and channel electrons;
- Band-to-band tunneling issues and their implications for device operation Incremental Step Pulse Programming (ISPP);
- Array disturb, program disturb, and program inhibit mechanisms over-

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- programming, over-erase issues, and multibit storage;
 - Self-boost and local self-boost techniques for program inhibit; and
 - Threshold voltage outliers and accidental programming of unselected cells LOCOS and trench isolation, tunnel oxide, gate etching, and spacer formation.

17. At Virginia Tech, my research focuses on developing a successor to the Floating-Gate transistor approach for nonvolatile memory (NVM) technology, specifically resistive RAM (ReRAM or RRAM). I am actively involved in manufacturing these devices in the university's cleanroom, employing advanced thin-film deposition techniques such as Physical Vapor Deposition (PVD), Chemical Vapor Deposition (CVD), Sputtering, and Atomic Layer Deposition (ALD).

18. In addition to my research, I delivered a keynote talk on the application of dielectric materials in CMOS technology, highlighting the use of these deposition techniques, at the 2020 International Electron Device Meeting (IEDM, paper 40.1). I also recently published a paper on stacked ReRAM memory and taught an annual semester-long lecture on CMOS manufacturing and nonvolatile memory operation.

19. My comprehensive expertise bridges the gap between device physics, manufacturing processes, and technology development, contributing to both the academic and industrial advancement of semiconductor technologies.

III. Level of Ordinary Skill in the Art

20. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a POSITA at the time of the alleged invention, which I understand is asserted to be November 16, 2015—the priority date of the earliest patent application. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art, including the art cited below.

21. Taking these factors into consideration, on or before November 16, 2015, a POSITA of the '974 Patent would have had a Bachelor's degree in electrical engineering, materials science, or physics, or a closely related field, along with at least two years of experience in semiconductor fabrication. A higher level of education might make up for less experience, and vice versa.

22. Before November 16, 2015, my level of skill in the art was at least that of a POSITA. I am qualified to provide opinions concerning what a POSITA would have known and understood at that time, and my analysis and conclusions herein are

from the perspective of a POSITA as of that date. A different priority date would not change my opinions as long as the identified prior art were still prior art.

IV. Materials Considered and Relied Upon

23. In reaching the conclusions described in this declaration, I have relied on the documents and materials cited herein as well as those identified in this declaration, including the '974 Patent, the prosecution history of the '974 Patent, and prior art references cited herein. These materials comprise patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions.

24. In the cited references, all emphasis is added unless otherwise noted.

25. I have also relied on my education, training, research, knowledge, and personal and professional experience in the relevant technologies that were already in use prior to the claimed invention.

- EX1001: U.S. Patent No. 10,373,974 (“the '974 Patent”)
- EX1002: Prosecution History of the '974 Patent (“the '974 File History”)
- EX1004: U.S. Patent Application Publication No. 2016/0322376 in the name of Lee (“Lee”)
- EX1005: U.S. Patent Application Publication No. 2012/0306089 in the name of Freeman *et al.* (“Freeman”)
- EX1006: U.S. Patent Application Publication No. 2016/0163732 in the

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- name of Lim *et al.* (“Lim”)
- EX1007: Korean Patent Application No. 10-2014-0176089 (“Lim-KR”)
 - EX1008: Certified English Translation of Korean Patent Application No. 10-2014-0176089 (“Lim-KR_trans”)
 - EX1009: U.S. Patent Application Publication No. 2015/0129878 in the name of Shin *et al.* (“Shin”)
 - EX1010: U.S. Patent Application Publication No. 2010/0133598 in the name of Chae *et al.* (“Chae”)
 - EX1011: U.S. Patent Application Publication No. 2015/0137216 in the name of Lee *et al.* (“Lee-2”)
 - EX1012: “Adjacent” – Merriam-Webster Online Dictionary 2015, Retrieved September 12, 2015, from <https://web.archive.org/web/20150912031420/https://www.merriam-webster.com/dictionary/adjacent> (“MW”)
 - EX1013: U.S. Patent Application Publication No. 2015/0279852 in the name of Mizutani *et al.* (“Mizutani”)
 - EX1014: J. Jang *et al.*, “Vertical cell array using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory,” 2009 Symposium on VLSI Technology, Kyoto, Japan, 2009, pp. 192-193. (“Jang”)
 - EX1015: Y. Noh *et al.*, “A New Metal Control Gate Last process (MCGL process) for High Performance DC-SF (Dual Control Gate with Surrounding Floating Gate) 3D NAND Flash Memory,” *2012 Symposium on VLSI Technology (VLSIT)*, Honolulu, HI, USA, 2012, pp. 19-20. (“Noh”)
 - EX1016: U.S. Patent Application Publication No. 2014/0138840 in the

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- name of Ha *et al.* (“Ha”)
- EX1017: U.S. Patent Application Publication No. 2009/0310415 in the name of Jin *et al.* (“Jin”)
 - EX1018: U.S. Patent Application Publication No. 2016/0218059 in the name of Nakada *et al.* (“Nakada”)
 - EX1019: U.S. Patent Application Publication No. 2016/0365351 in the name of Nishikawa *et al.* (“Nishikawa”)
 - EX1020: R. Muller *et al.*, “Device Electronics for Integrated Circuits,” 3rd Edition, John Wiley & Sons, pp. 97-99. (“Muller”)

V. Legal Standards

26. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

27. In formulating my opinions, I have been informed of certain legal understandings relevant to my opinions. In formulating my opinions, I have relied on the legal understandings I have been provided with as set forth in this declaration.

28. I have been informed that in *inter partes review* proceedings, invalidity must be shown under a preponderance of the evidence standard.

A. My Understanding of Claim Construction

29. I have been informed that patent claims are construed from the viewpoint of a POSITA of the patent at the time of the invention. I have been

informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a POSITA in the relevant time period (i.e., at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification, and the prosecution history (i.e., the intrinsic record).

30. I have further been informed that a POSITA must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner’s rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or clearly and unambiguously disavowing claim coverage.

31. In interpreting the meaning of the claim language, I understand that a POSITA may also consider “extrinsic” evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly

publications. I understand this evidence is considered to ensure that a claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. For example, this can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

B. My Understanding of Anticipation

32. I understand that a patent claim is invalid as “anticipated” if all the limitations of the claim are present, either expressly or inherently, in a single prior art publication or patent.

33. I also understand that a prior art reference can disclose a claimed feature because the feature is expressly described or because the feature is inherent in the disclosure. I understand that something is inherent in a prior art reference if the missing descriptive matter must necessarily be present, not merely probably or possibly present, and it would be so recognized by a POSITA as of the priority date of the patent. I understand that it is acceptable to examine evidence outside of the prior art reference (i.e., extrinsic evidence) in determining whether a feature, while not expressly discussed in the reference, is necessarily present in it.

34. I have further been informed that where a reference discloses multiple

embodiments, the reference should not be limited to a preferred embodiment. Instead, each disclosed embodiment may anticipate.

35. Moreover, I have been informed that as part of an anticipation analysis, it is proper to take into account not only specific teachings of the reference, but also the inferences that one skilled in the art would reasonably be expected to draw therefrom. A reference can anticipate a claim even if it does not expressly spell out all the limitations arranged or combined as in the claim, if a POSITA, reading the reference, would at once envisage the claimed arrangement or combination.

C. My Understanding of Obviousness

36. I understand that a claim may be invalid if the subject matter described by the claim as a whole would have been obvious to a hypothetical POSITA in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a hypothetical POSITA and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical POSITA is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

37. I have been informed that there are two criteria for determining whether prior art is analogous and thus can be considered prior art: (1) whether the art is from

the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not within the field of the patentee's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the patentee is involved. I have also been informed that the field of endeavor of a patent is not limited to the specific point of novelty, the narrowest possible conception of the field, or the particular focus within a given field. I have also been informed that a reference is reasonably pertinent if, even though it may be in a different field from that of the patentee's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to a patentee's attention in considering their problem.

38. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

39. I have also been advised that in considering whether a claimed invention would have been obvious over a combination of prior art references, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the

marketplace, and/or the background knowledge possessed by a POSITA. I understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;
- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a POSITA can implement a predictable variation, the variation is likely obvious;
- If a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls whether the claim is obvious;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;

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- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
 - “Common sense” teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a POSITA will be able to fit the teachings of multiple patents together like pieces of a puzzle;
 - A POSITA is also a person of ordinary creativity, and is not an automaton;
 - A patent claim can be proved obvious by showing that the claimed combination of elements was “obvious to try,” particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a POSITA would have had good reason to pursue the known options within his or her technical grasp; and
 - One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

40. I further understand that, in making a determination as to whether the claimed invention would have been obvious to a POSITA, the Board may consider certain objective factors if they are present, such as: commercial success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be

relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence, and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with predictable results) that is sufficiently strong.

VI. Technology Background

A. Architecture of Three-Dimensional (3D) NAND Flash Memory

41. The semiconductor industry has continually faced the dual challenges of increasing chip performance and reducing the physical footprint of integrated circuits. An important innovation in overcoming these challenges is the concept of vertical integration, where components of a circuit are stacked vertically to enhance density and performance without increasing the horizontal footprint. This approach is important in the development of 3D integrated circuits (ICs) and, more recently, in the 3D NAND memory, which has enabled rapid advancements in processing power and memory capacity.

42. The development of 3D NAND flash memory has revolutionized data storage by enabling higher memory storage capacities within smaller physical footprints. At the heart of this advancement lies a memory stack that supports the vertical integration of multiple memory cell levels. The memory stack may include

vertical channels extending through a stack of alternating conductive layers and dielectric layers, which is formed from a stack of alternating silicon nitride layers and silicon oxide layers by replacing at least portions of the silicon nitride layers with a conductive material.

43. A Terabit Cell Array Transistor (TCAT) flash memory is an example of the 3D NAND flash memory. A birds-eye view of the TCAT flash memory is shown in FIG. A below, which includes annotated FIG. 1 of EX1014. The TCAT flash memory may include a memory cell array having vertical channels (in yellow, a.k.a. semiconductor pillars) extending through a stack of alternating conductive layers (in green) and oxide layers. The conductive layers may form gate lines including top select lines SSL, control gates (word lines W/L), and bottom select lines GSL extending across the memory cell array in the word line direction. Memory cells may be formed between the vertical channels and the control gates, whereas top select transistors are formed between the vertical channels and the top select lines SSL, and bottom select transistors are formed between the vertical channels and the bottom select lines GSL. EX1014, Section “Architecture and Key Features of TCAT Flash,” ¶1.

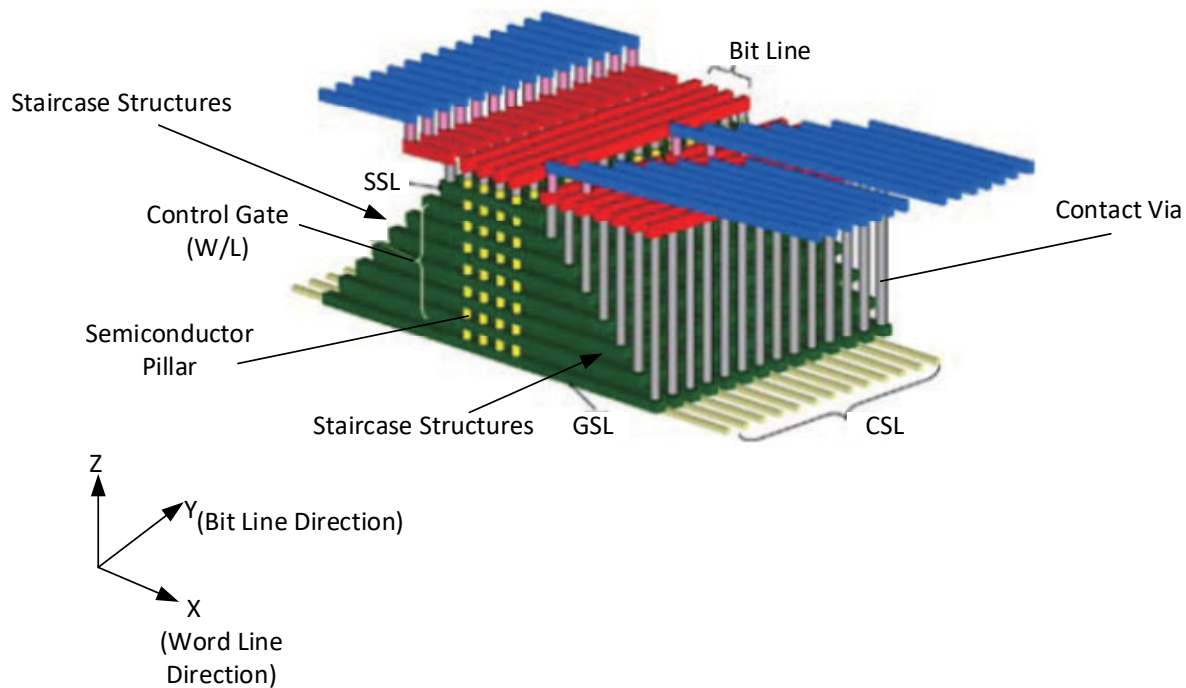


FIG. A – FIG. 1 of EX1014 (annotated)

44. As shown in FIG. A, the memory cell array also includes staircase structures (a.k.a stair-like structures) at the two opposite array edges in the X-direction (the word line direction), with exposed ends of the conductive layers forming contact regions in steps of the staircase structures. EX1014, FIG. 3, FIG. 6, Section “Architecture and Key Features of TCAT Flash,” ¶1. The memory cell array further includes contact vias landing onto word lines on different levels of the stair-like structures to connect respective conductive layers to peripheral circuits. *See also* EX1014, FIG. 6.

B. Overview of Fabrication Process of 3D NAND Flash Memory

45. A fabrication process of the TCAT flash memory shown in FIG. A

above is illustrated below in FIG. B, which includes annotated FIG. 3 of EX1014. The process sequence includes: (a) depositing a stack of alternating sacrificial nitride layers and oxide layers; (b) forming channel holes extending through the stack and forming the vertical channels (in yellow) in the channel holes, respectively; (c) etching the stack of alternating sacrificial nitride layers and oxide layers at the two opposite array edges in the X-direction to form stair-like structures such that gate pads are formed (“Gate Pad”); (d) etching through the stack to form trenches extending in the Z-direction and also extending along the X-direction (“W/L Cut Etch”); (e) performing a “gate replacement” process (a.k.a. gate line replacement process) to replace the sacrificial nitride layers with tungsten (W) or any other suitable conductive material; and (f) forming contact vias landing onto conductive layers at different levels of the stair-like structures. EX1014, Section “Architecture and Key Features of TCAT Flash,” ¶1, FIG. 3, FIG. 6.

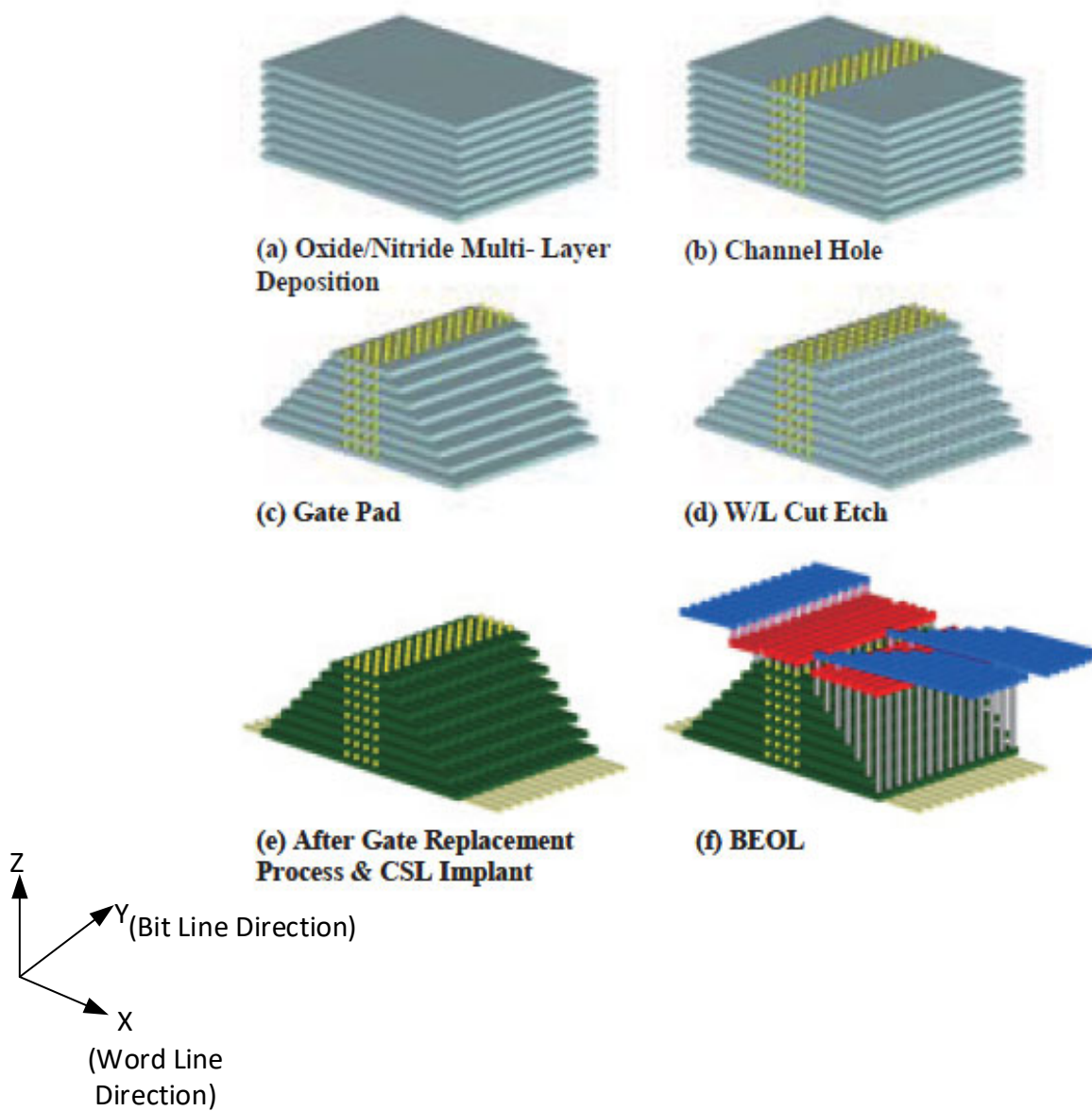


FIG. B - FIG. 3 of EX1014 (annotated)

C. Gate Replacement Process

1. *Shifting from “Gate-First” Approach to “Gate-Last” Approach*

46. The origins of 3D NAND technology trace back to a Bit Cost Scalable

(BiCS) architecture, which utilizes a gate-first approach in which the conductive material forming the gate lines is deposited before the formation of the vertical channels in vertical channel holes. This method involves a stack of alternating layers of silicon dioxide (SiO_2) and polysilicon, with the polysilicon serving as the gate lines after processing. After forming the gate lines, vertical channel holes are etched through the stack, and successive layers—including a gate dielectric layer, a charge storage layer (such as silicon nitride or floating polysilicon), a tunnel oxide layer, and a polysilicon channel—are deposited sequentially in each channel hole.

47. While this gate-first approach is effective for initial designs, scaling challenges emerge as layer counts increase. The alignment precision required for depositing the conductive material prior to forming the vertical channels limits manufacturability and performance. To overcome these limitations, the industry transitions to the gate-last approach, which reverses the sequence of gate and channel formation compared to the gate-first approach. In the gate-last approach, the conductive material forming the gate lines is deposited after the channels have been fully formed. This enables greater flexibility and precision in fabricating complex multi-layer structures. This gate-last approach is also known as the “gate replacement process,” which is applied in the formation of the TCAT flash memory as described above in Section VI.B.

2. *Process Flow of Gate Replacement*

48. With reference to FIG. C shown below, which includes FIG. 4 of EX1014, example stages of the gate replacement process are provided. First, as illustrated in section (a) of FIG. C, a trench is formed by performing the word line (W/L) cut on a stack of alternating sacrificial nitride layers and oxide layers, such that the sacrificial nitride layers in the stack are exposed through the trench. The trench serves as an access passage for subsequent nitride etching and material deposition. Second, in section (b) of FIG. C, a selective wet etching is used to remove the sacrificial nitride layers laterally, creating empty spaces between the oxide layers. This step results in a vertical “fence” oxide structure, where the oxide layers and empty spaces outline the intended locations for the gate lines. Third, in section (c) of FIG. C, gate dielectric (e.g., high-k dielectrics) may be deposited on sidewalls of the empty spaces, and a conductive material, such as tantalum nitride (TaN), tungsten (W), or polysilicon, can be filled in the empty spaces to form preliminary gate nodes which are interconnected. Fourth, in section (d) of FIG. C, the conductive material within the trench is selectively and vertically etched to separate the interconnected preliminary gate nodes into individual gate lines. EX1014, FIG. 4, Section “Architecture and Key Features of TCAT Flash,” ¶1; EX1015, FIG. 2, Section “MCGL” process, ¶1.

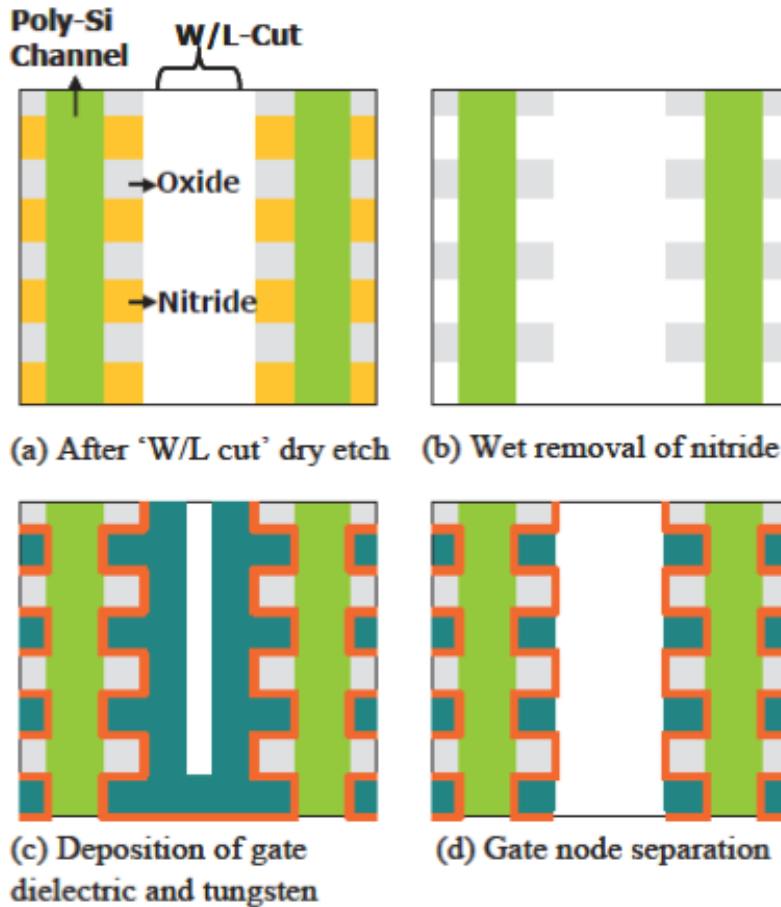


FIG. C - FIG. 4 of EX1014

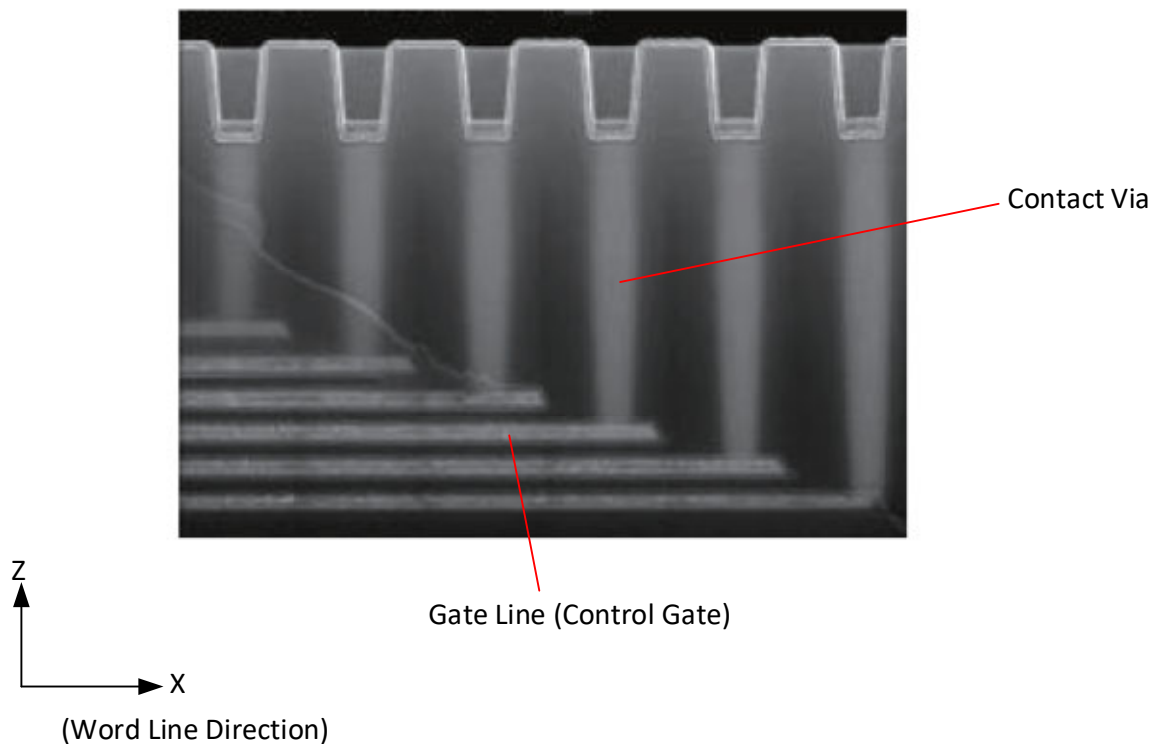
49. The gate replacement process allows for more precise control over the gate formation, enabling higher layer counts, improved scalability, and denser memory arrays. Depositing the conductive material after forming the channels ensures uniformity and reduces defects caused by earlier deposition steps. The gate replacement process minimizes alignment challenges and simplifies the integration of advanced materials, such as high-k dielectrics and metal gates.

D. Stair Step Structures

1. Introduction to the Stair Step Structures

50. In a conventional two-dimensional (2D) NAND flash memory, memory cells are laid out on a flat plane, with horizontal interconnects enabling access to individual cells. However, the demand for higher storage capacities and improved performance exposes the limitations of the 2D architecture, particularly in terms of physical size and scalability. To overcome these challenges, 3D NAND technology, where memory cells are vertically stacked, is adopted. 3D NAND technology significantly increases storage density while improving performance. However, as the number of stacked layers grows, addressing and connecting the gate lines of the stacked layers to the peripheral circuitry becomes increasingly complex.

51. The introduction of the stair step structures (a.k.a. staircase structures, stepped structures, stair-like structures, etc.) addresses this challenge. The terraced design of the stair step structures ensures that each gate line within the memory stack is exposed, enabling precise vertical connections via contact vias. For example, a cross-sectional scanning electron microscope (SEM) image at a cell array edge of the TCAT flash memory discussed in Section VI.A is illustrated in FIG. D below, which depicts the terraced design of the stair step structure, such that contact vias may connect to ends of the gate lines exposed by the terraced design.



52. The terraced design of the stair step structures is a cornerstone for high-density, high-performance memory arrays, supporting the scalable integration of 3D NAND flash memory as industry demand for faster and larger memory chips continues to rise.

2. Formation of Stair Step Structures: Photolithography and Etch Processing

53. The formation of the stair step structures relies on a combination of advanced photolithography and etching techniques. These processes selectively expose the gate lines and etch through the stack of alternating sacrificial layers (e.g., silicon nitride) and dielectric layers (e.g., silicon oxide) to form the desired stair step

profile. In general, photolithography begins with the application of a light-sensitive photoresist layer on the stack of alternating sacrificial layers and dielectric layers. A mask is used to expose specific regions of the photoresist layer, which are then developed to create patterns for etching. Two types of photolithography masks, step masks and chop masks, can be applied to this process.

a. Step Mask

54. A step mask can be repeatedly applied throughout the photolithography process to expose and etch specific regions of the stack of alternating sacrificial layers and dielectric layers (e.g., alternating nitride and oxide layers) in order to form the staircase profile. Specifically, a trim-etch technique is employed, allowing multiple steps to be formed with a single step mask. FIG. E below provides a detailed illustration of how the step mask is repeatedly patterned and trimmed both laterally and vertically to define steps in the staircase structure. The step mask undergoes a series of lateral and vertical trimming during the etching process, sequentially exposing corresponding underlying alternating sacrificial layers and dielectric layers in a controlled sequence.

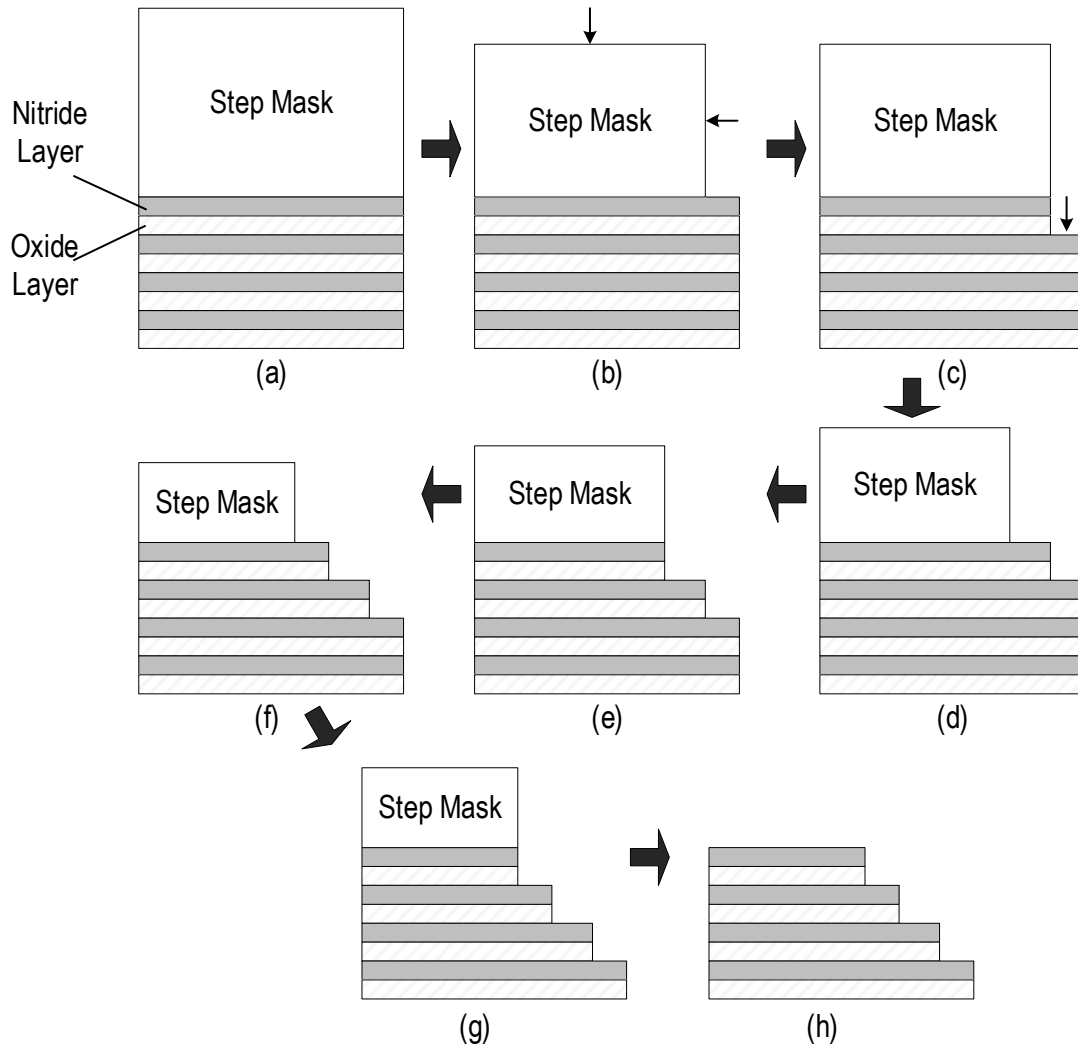


FIG. E

55. With reference to section (a) of FIG. E, a step mask is deposited on a stack of alternating sacrificial nitride layers and oxide layers. In section (b) of FIG. E, the step mask is laterally and vertically trimmed. For example, the step mask is trimmed by a width of a step in the lateral direction to expose the first topmost pair of sacrificial nitride and oxide layers. Then, in section (c) of FIG. E, the first topmost pair of sacrificial nitride and oxide layers is etched by the width of the step, and the

second topmost pair of sacrificial nitride and oxide layers is exposed. Subsequently, in section (d) of FIG. E, the step mask is pulled back (trimmed) to expose the first topmost pair of sacrificial nitride and oxide layers by the width of the step again. In section (e) of FIG. E, both the first topmost pair and the second topmost pair of sacrificial nitride and oxide layers are etched by the width of the step again to expose the third topmost pair of sacrificial nitride and oxide layers. This “trim-etch” process is iteratively performed to etch the exposed alternating sacrificial nitride and oxide layers and progressively reduces the mask’s size, as shown in sections (f) and (g) of FIG. E, and continues until the entire staircase structure is formed, as shown in section (h) of FIG. E.

56. This trim-etch approach significantly reduces the number of lithography steps required to form the staircase structure. However, it demands a thick photoresist layer capable of withstanding the multiple trimming and etching cycles. Any errors in the trimming or etching process can accumulate, potentially leading to misaligned steps or inconsistent connections. Such misalignments may adversely affect step uniformity, resulting in defective gate line connections or resistance variations that compromise device reliability.

57. After the staircase structure is defined using the step mask, a passivation layer is deposited over the staircase structure. The passivation layer serves to planarize the surface filling in the gaps and creating a flat and uniform

surface. This planarization is crucial for the subsequent application of the chop mask as it ensures that the photolithography process for defining additional areas of contacts can be performed accurately.

b. Chop Mask

58. Strategic use of a chop mask can reduce the number of photolithography steps required, thereby alleviating or preventing electrical mismatches or defects caused by the step mask and meanwhile enabling connectivity across multiple tiers of the memory stack without compromising reliability. Depending on the complexity of the memory stack, a chop mask may be reused iteratively or combined with other masks (e.g., step masks or other chop masks) to expose gate lines across different tiers. EX1016, FIGs. 8A-8L, [0069]-[0077]; EX1017, FIGs. 6A-8B, [0036]-[0041]. By enabling reliable vertical connectivity, the chop mask is a fundamental enabler of the 3D NAND architecture, ensuring the proper functioning of these intricate multi-tiered memory structures.

59. Different from the step mask, which adopts the iterative trim-etch process to form consecutive steps in the staircase structure, the chop mask may be applied to etch (“chop off”) one or multiple pairs (or tiers) of sacrificial nitride and oxide layers in a chopping process. For example, with reference to FIG. F shown below, which includes annotated FIGs. 6A, 6B, 7B, and 8B of Jin (EX1017), three chopping processes with three chop masks M1, M2, and M3 are respectively applied

to form stair step structures in a contact region of a stack of alternating word line layers 30 (word line layers 31-38) and interlayer dielectric layers 20. FIGs. 6B, 7B, and 8B of Jin are cross sections along a line I-I of FIG. 6A.

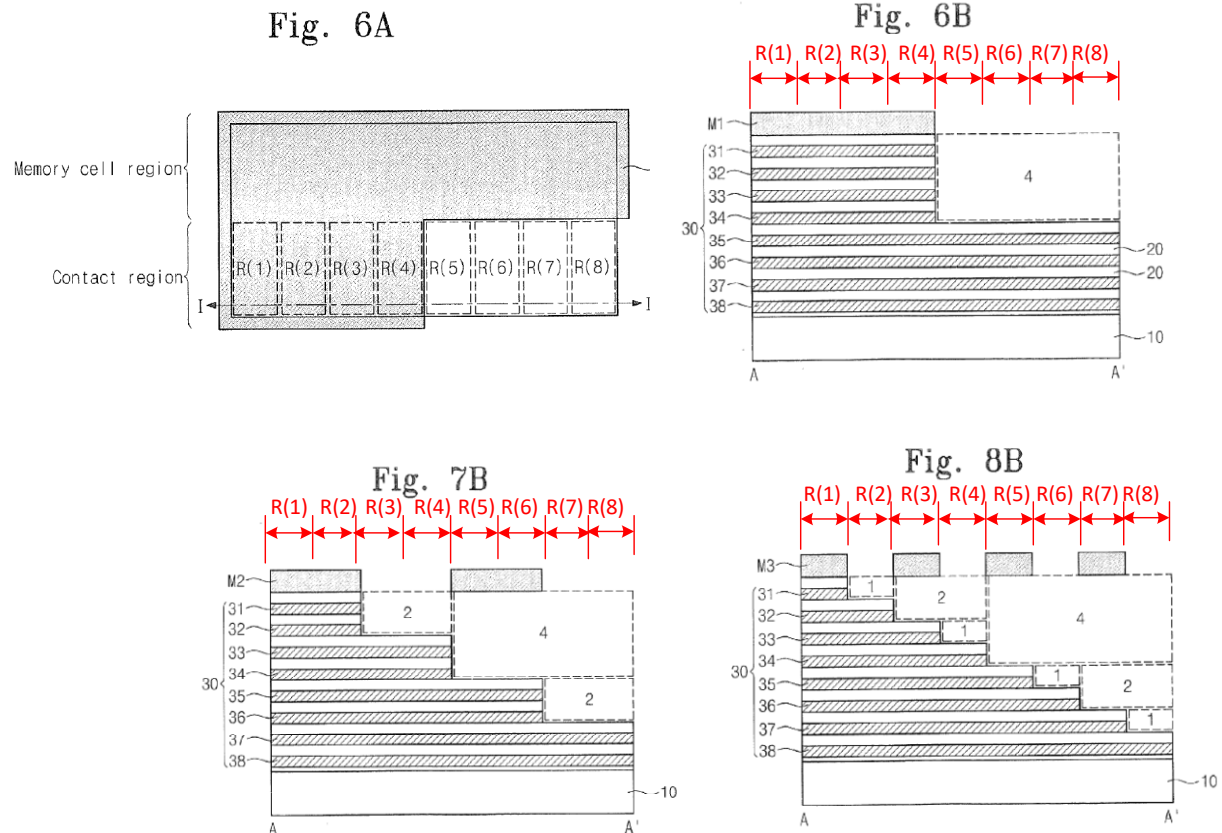


FIG. F— FIGs. 6A, 6B, 7B, and 8B of EX1017 (annotated)

60. As shown in FIGs. 6A and 6B of Jin, the contact region is divided into eight contact portions R(1)-R(8), and a first chop mask M1 is formed on the stack to cover a memory cell region and contact regions R(1)-R(4) and to expose contact regions R(5)-R(8). The first chop mask M1 is used to etch (chop off) the four upper most word line layers 31-34 (and the intervening interlayer dielectric layers 20) in contact portions R(5)-R(8), while keeping the four lower most word line layers 35-

38 intact, as shown in FIG. 6B. EX1017, [0036]-[0037].

61. Next, as shown in FIG. 7B of Jin, the first chop mask M1 is removed, and a second chop mask M2 is applied to cover the memory cell region and contact regions R(1)-R(2) and R(5)-R(6) and to expose contact regions R(3)-R(4) and R(7)-R(8). The second chop mask M1 is used to etch (chop off) two word line layers 31-32 (and the intervening interlayer dielectric layers 20) in contact portions R(3)-R(4) and two word line layers 35-36 (and the intervening interlayer dielectric layers 20) in contact portions R(7)-R(8). EX1017, [0038]-[0039].

62. Subsequently, as shown in FIG. 8B of Jin, the second chop mask M2 is removed, and a third chop mask M3 is applied to cover the memory cell region and contact regions R(1), R(3), R(5), and R(7) and to expose contact regions R(2), R(4), R(6), and R(8). The third chop mask M3 is used to etch (chop off) word line layer 31 (and the intervening interlayer dielectric layer 20) in contact portion R(2), word line layer 33 (and the intervening interlayer dielectric layer 20) in contact portion R(4), word line layer 35 (and the intervening interlayer dielectric layer 20) in contact portion R(6), and word line layer 37 (and the intervening interlayer dielectric layer 20) in contact portion R(8). As a result, the sequential application of the three chop masks M1, M2, and M3, as outlined above, provides the formation of staircase structures in the contact region. EX1017, [0040]-[0041].

63. In another example, with reference to FIG. G shown below, which

includes annotated FIGs. 8C, 8D, and 8I of Ha (EX1016), a chop mask and a subsequent step mask are applied to form staircase structures in a stack 860 of alternating conductive materials 861 and insulating materials (omitted in the figures). FIGs. 8C and 8D of Ha show end views of the stack, whereas FIG. 8I shows a top view of the stack. EX1016, [0069].

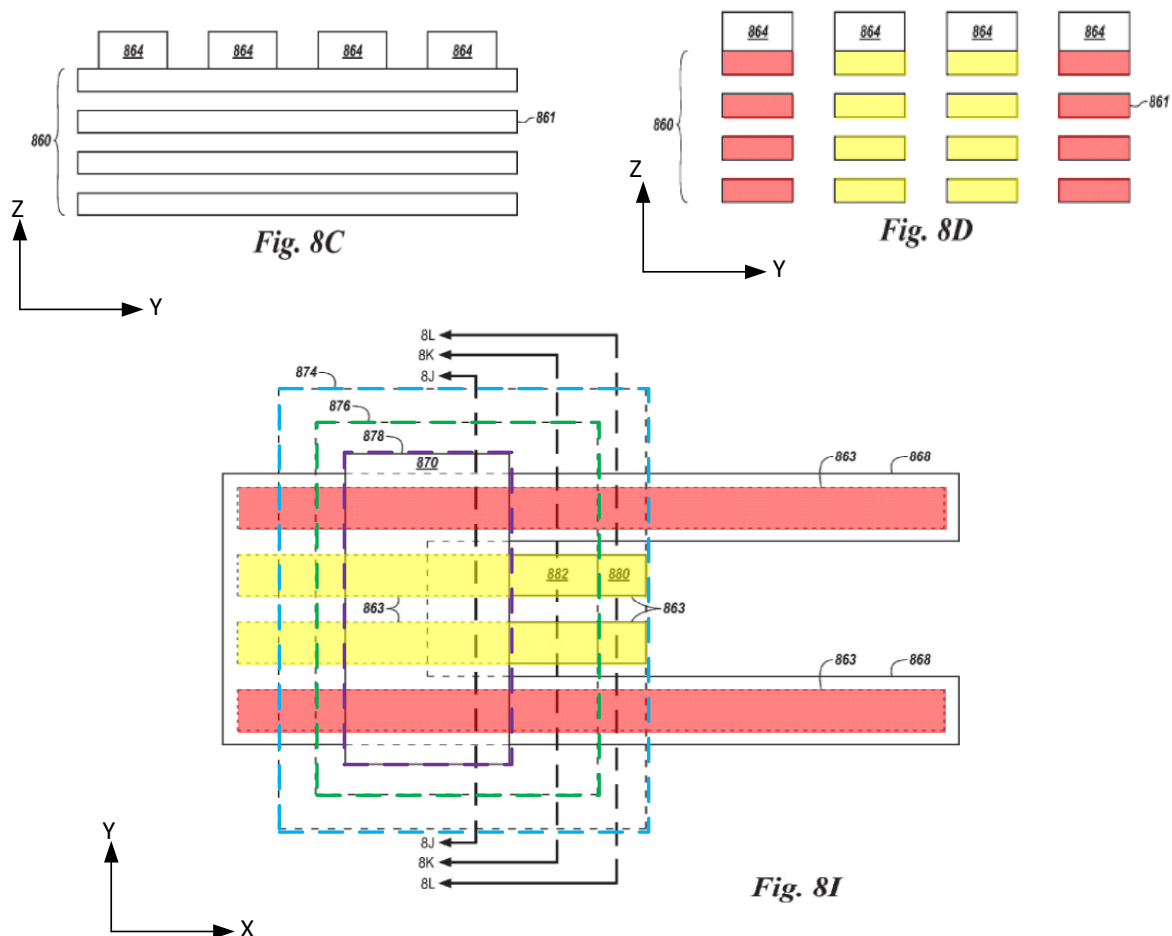


FIG. G – FIGs. 8C, 8D, and 8I of EX1016 (annotated)

64. As shown in FIG. 8C of Ha, a chop mask including area masks (864) formed of “chop mask material” is formed on stack 860. Next, as shown in FIG. 8D

of Ha, with the chop mask, stack 860 is then processed to etch conductive materials 861 (and intervening insulating materials-not shown in the figure) into a number of stack columns 863 (including outer stack columns in red, inner stack columns in yellow, as shown in annotated FIGs. 8D and 8I of Ha). EX1016, [0070].

65. Subsequently, as shown in annotated FIG. 8I of Ha, a U-shaped area mask 868 is applied to cover outer stack columns 863 (in red) and portions of inner stack column 863 (in yellow), leaving the remaining portions of inner stack columns 863 uncovered by the U-shaped area mask 868. A step mask (including first and second photoresist masks 870 and 872) can be deposited on stack 860 and used to pattern a stair step structure out of the remaining portions of inner stack columns 863, through photoresist mask configurations 874, 876, and 878 (in blue, green, and purple dashed boxes shown in the annotated FIG. 8I). That is, the step mask initially covers the remaining portions of inner stack columns 863 as shown by photoresist mask configuration 874. Next, the step mask is trimmed to photoresist mask configuration 876, such that the upmost tier (e.g., the top pair) of conductive material 861 and the insulating material in the remaining portions of inner stack columns 863 exposed by the step mask is etched. Subsequently, the step mask is trimmed to photoresist mask configuration 878, such that the two upmost tiers of conductive material 861 and the insulating material in the remaining portions of inner stack columns 863 exposed by the step mask are etched. EX1016, [0072]-[0077].

66. As shown in the annotated FIG. 8I of Ha, the use of the chop mask (area mask 864) in conjunction with the step mask (photoresist mask 870/872) can “confine stair step formation to smaller areas and/or to areas closer to other features than can be achieved, for example, if stair steps are formed around all sides of a photoresist mask used alone,” e.g., without a chop mask. EX1016, [0078]. In this manner (e.g., with the chop mask), “stair steps can be used in forming coupling from smaller and/or more precisely-located areas adjacent a memory array to driver circuitry.” EX1016, [0078].

E. Through-Array Vias (TAVs)

1. Introduction to TAVs

67. Vertical integration in semiconductor design plays an important role for achieving higher storage densities and processing speeds. The concept of connecting different layers of integrated circuits (ICs) has led to the development of Through Silicon Vias (TSVs), an interconnection technology that enables 3D IC architectures to improve performance and density of devices per square centimeter of the expensive silicon wafer real estate.

68. In early 3D NAND flash memory products, peripheral circuits (e.g., page buffers, row decoders, etc.) are located laterally outside of the cell array area, following a conventional 2D chip layout as illustrated in section (a) of FIG. H below. To increase the degree of integration of the flash memory such that the chip size as

well as the bit cost can be reduced, the peripheral circuits can be formed under a cell array as illustrated in section (b) of FIG. H below. By forming the peripheral circuits underneath the cell array area, the cell efficiency can be expected to improve significantly. The memory chip size can be drastically reduced, so that the bit cost can be reduced.

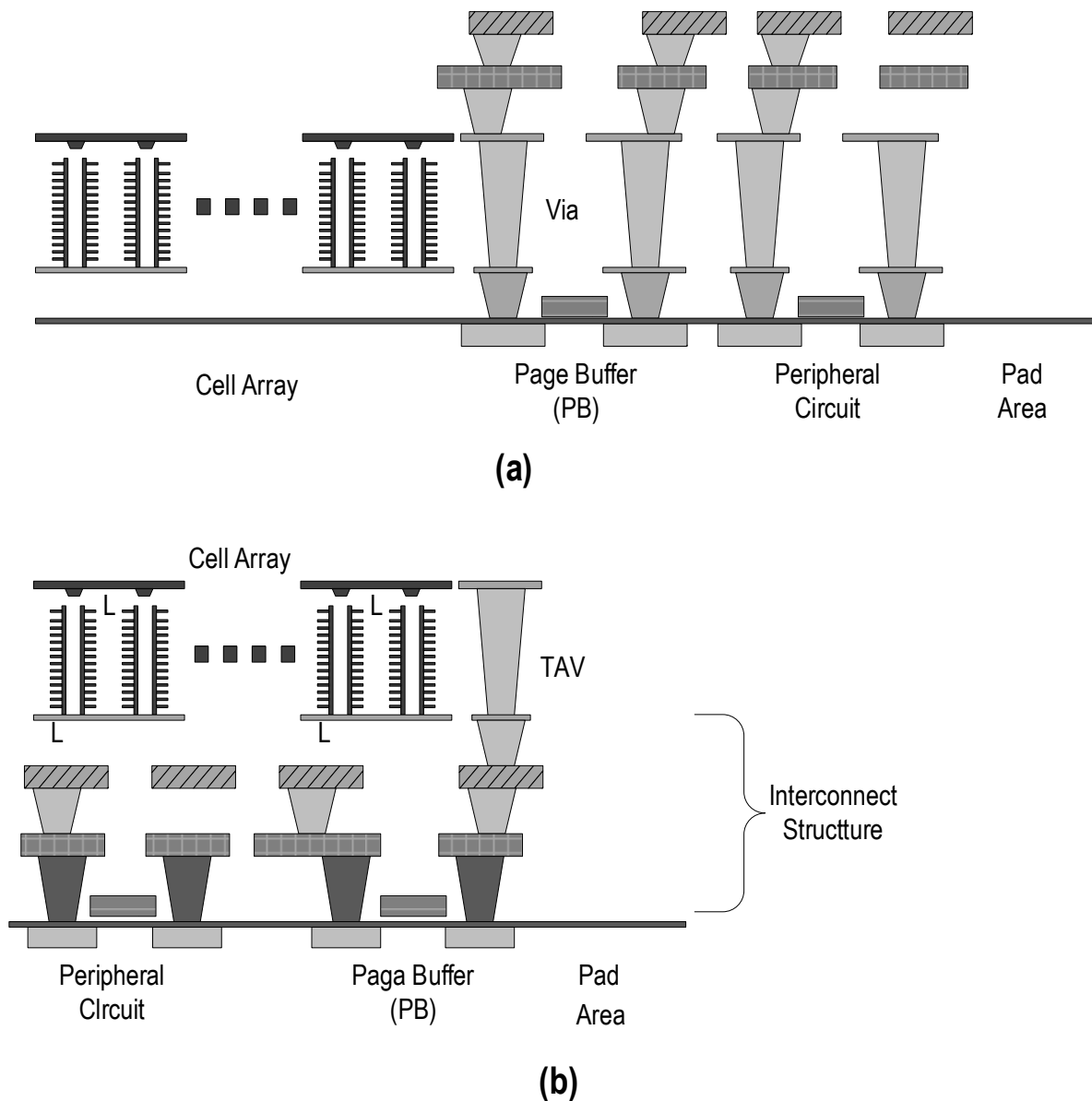


FIG. H

69. TAVs are a variation of TSVs specifically optimized for connecting peripheral circuits under the memory cell array as shown in section (b) of FIG. H above. In a 3D NAND memory, interconnects like word lines (WLs) are thin and long, leading to high resistance and nonuniformities due to statistical process variations. The high resistance and nonuniformities can degrade memory performance and functionality, even when the memory cells themselves remain intact. To mitigate this, reducing the length of interconnects (both lateral and vertical) is important. TAV structures achieve this goal by enabling vertical connections to the peripheral circuitry placed beneath the memory cell array (as shown in section (b) of FIG. H), instead of requiring long lateral interconnects to the peripheral circuitry that consume additional silicon real estate with increased interconnect lengths (as shown in the 2D layout in section (a) of FIG. H). TAV structures not only reduce resistance but also minimize parasitic capacitances to nearby structures, thereby significantly lowering the RC time delay ($t = R \times C$). The combined reduction in resistance and parasitic capacitances greatly improves the operational speed and efficiency of the 3D NAND memory.

2. *Formation of TAVs*

70. There are various approaches to accommodate TAVs in the 3D NAND architectures. In a first example approach, TAVs are formed to extend through a stack of alternating conductive and dielectric materials to connect to a peripheral

circuitry underneath the memory stack. Spacers including insulating materials are formed to surround the TAVs to provide electrical isolation between the TAVs and the conductive materials. For example, as shown in FIG. I below, which includes annotated FIG. 1B of Shin (EX1009), vertical contacts 232 (in red, TAVs) penetrate a stack of conductive lines 192, 194, 196, 198 and insulating layers 193, 195, 197, 199, and are electrically connected to a peripheral circuit gate structure 120 underneath (in a green dotted box) through a lower interconnection structure 150 (in blue). EX1009, [0049], [0073]. Spacers 240 (in yellow) are formed on sidewalls of vertical contacts 232, respectively, to provide electrical isolation between vertical contacts 232 and conductive lines 192, 194, 196, 198, as well as among conductive lines 192, 194, 196, 198. EX1009, [0074].

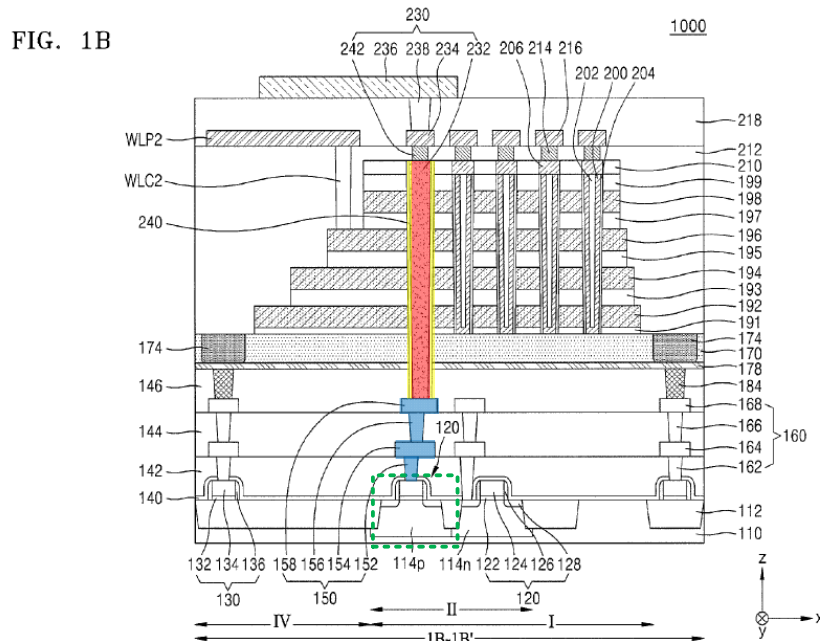


FIG. I – FIG. 1B of EX1009 (annotated)

71. In a second example approach, an insulating structure may be formed in the stack of alternating conductive and dielectric materials. A TAV can be formed to extend through the insulating structure to connect to the peripheral circuitry underneath the insulating structure. The insulating structure provides electrical isolation between the TAV and the conductive materials. For example, as shown in FIG. J below, which includes annotated FIG. 32A of Lim (EX1006), a contact plug 52 (in black, TAV) passes through an insulating structure 123 (in yellow) to connect to a peripheral transistor PTR (in a green dotted box) through a peripheral interconnection structure PW1 (in blue). EX1006, [0076], [0270], [0278]; EX1008, ¶¶28, 223, 231.

FIG. 32A

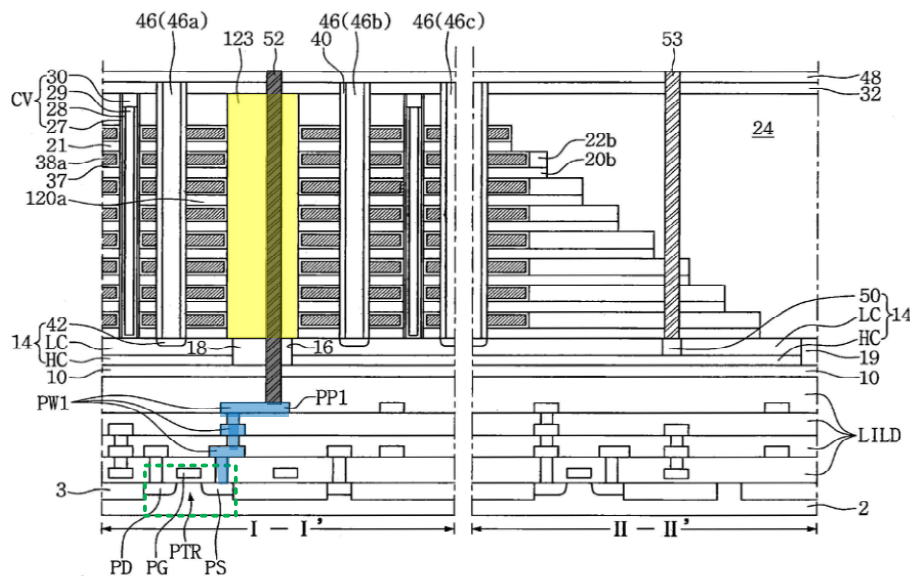


FIG. J – FIG. 32A of EX1006 and EX1008 (annotated)

72. In a third example approach, a stack of alternating dielectric layers may

remain within the stack of alternating conductive and dielectric materials. A TAV can be formed to extend through the stack of alternating dielectric layers (e.g., silicon nitride and oxide) to connect to the peripheral circuitry underneath the memory stack. The stack of alternating dielectric layers provides electrical isolation between the TAV and the conductive materials. For example, as shown in FIG. K below, which includes annotated FIG. 26A of Lim, contact plug 52 (in black, TAV) passes through a stack of alternating dielectric materials (in yellow) to connect to a peripheral transistor PTR (in a green dotted box) through a peripheral interconnection structure PW1 (in blue). EX1006, [0076], [0234]; EX1008, ¶¶28, 186.

FIG. 26A

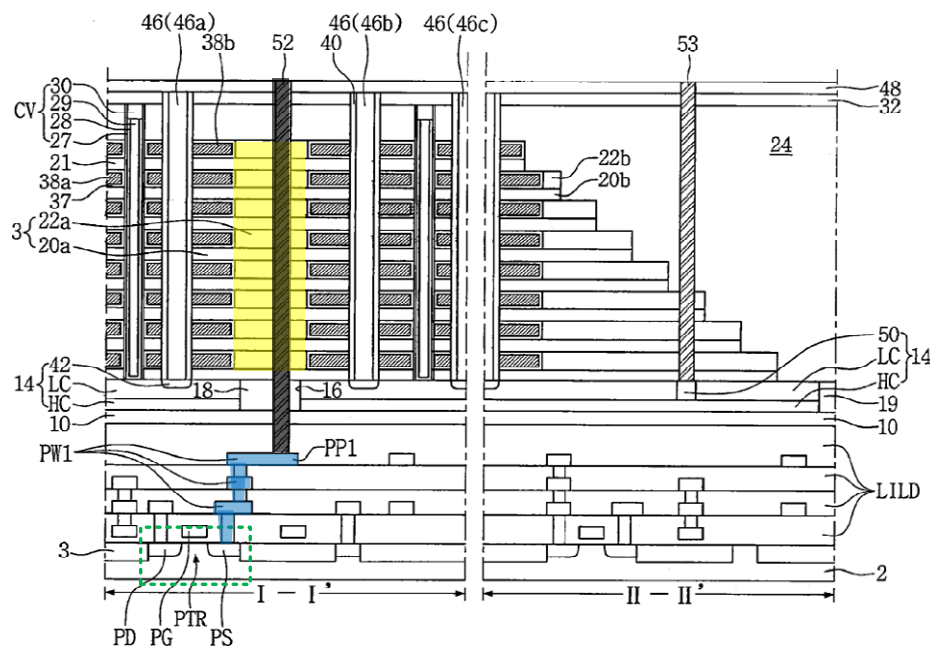


FIG. K –FIG. 26A of EX1006 and EX1008 (annotated)

VII. Overview of the '974 Patent

A. Subject Matter Overview

73. The '974 Patent is titled "Microelectronic devices and related methods." The '974 Patent was issued on August 6, 2019, from U.S. Patent Application No. 16/051,886, filed on August 1, 2018, with the earliest filing date of November 16, 2015 of its parent applications. *See* EX1001, Cover.

74. The '974 Patent relates to semiconductor devices having vertical memory blocks with slots and conductive through-array vias. EX1001, 1:17-22. The '974 Patent "develop[s] improved structures and methods of forming vertical memory arrays with through-array vias for semiconductor devices (e.g., vertical memory devices, such as NAND Flash memory devices) that reduce the number and complexity of additional processing acts practiced in conventional methods and structures." EX1001, 2:8-14.

75. The '974 Patent states that "the methods described herein enable the formation of through-array vias 120 without the need for removing conductive material 116 and other portions of the vertical memory block 100 in a separate material removal act to form the conductive vias 120." EX1001, 12:57-61.

1. Embodiments related to the Challenged Claims

76. A top view of a vertical memory block 100 of the '974 Patent is illustrated in FIG. L below, which includes annotated FIG. 1 of the '974 Patent. As

shown in FIG. L, in the longitudinal direction y , memory block 100 includes a memory array region 102 (in blue dashed box) in the middle, two stair step regions 104 (in red dashed boxes) at two opposite ends, and two via regions 106 (in black dashed boxes) between memory array region 102 and stair step regions 104, respectively. EX1001, 4:19-26. In memory array region 102, an array of memory cell pillars 108 (in blue) “may each extend vertically through the vertical memory block 100.” EX1001, 4:30-32.

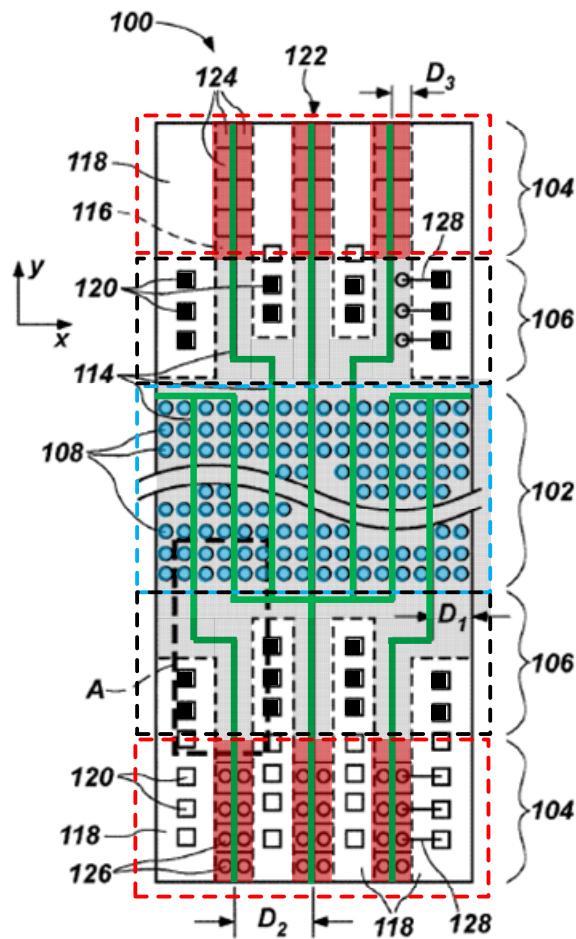


FIG. 1

FIG. L – FIG. 1 of EX1001 (annotated)

77. As shown in FIG. L above, slots 114 (in green), filled with a dielectric material (e.g., silicon oxide), “may extend through the memory array region 102 proximate to and between adjacent memory cell pillars 108.” EX1001, 4:37-40. Further, as illustrated in FIG. M below, which includes annotated FIG. 3 of the ’974 Patent, slots 114 (in green) “may vertically extend through a stack of alternating conductive word lines 116 and first dielectric materials 132.” EX1001, 6:13-15.

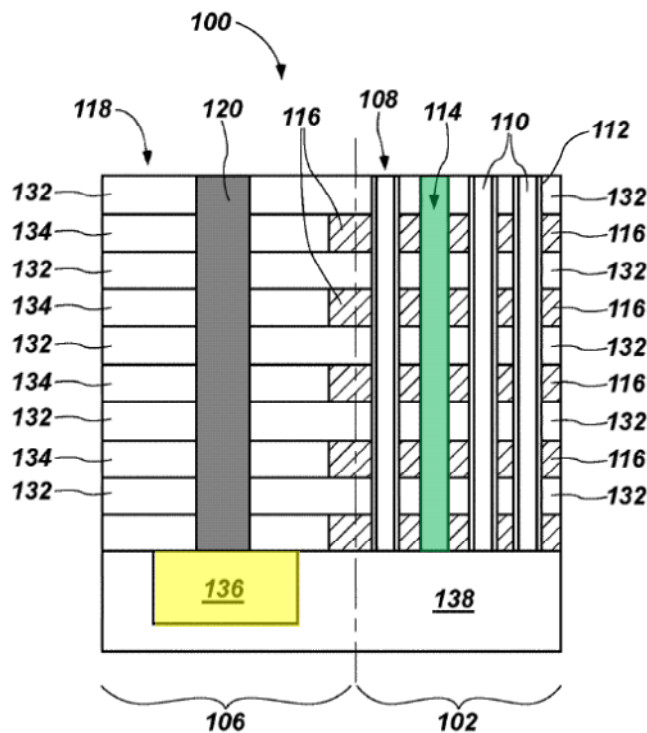


FIG. 3

FIG. M – FIG. 3 of EX1001 (annotated)

78. As shown in FIG. L above, conductive word lines 116 (in gray) “may extend along the slots 114 and be coupled to the memory cell pillars 108” to form memory cells with memory cell pillars 108. EX1001, 4:57-65. Adjacent conductive

word lines 116 in the x-direction are split by slots 114, and conductive word lines 116 and slots 114 both extend further from memory array region 102 into via regions 106 and stair step regions 104. EX1001, 5:57-61.

79. In memory array region 102, an array of memory cell pillars 108 (in blue) “may each extend vertically through the vertical memory block 100.” EX1001, 4:30-32. “Each of the memory cell pillars 108 may include a central region 110 of a semiconductor material, such as a polysilicon or silicon-germanium material, at least partially surrounded by a charge trapping material 112, such as an oxide-nitride-oxide (“ONO”) material.” EX1001, 4:32-37.

80. In each via region 106, conductive vias 120 (in black), “also referred to as ‘through-array vias’ or ‘TAVs,’” “may extend through the vertical memory block 100 within the dielectric stacks 118,” where each dielectric stack 118 includes a stack of “alternating dielectric materials (e.g., alternating oxide and nitride materials).” EX1001, 5:14-21. For instance, with reference to FIG. M shown above, conductive via 120 (in black) may operatively couple a sub-array circuitry 136 (in yellow) to vertical memory block 100. EX1001, 6:52-54. In each stair step region 104, one or more stair step structures 122 (in red) are formed “for electrically contacting and accessing different overlapping conductive word lines 116” and “may include contact regions 124 (e.g., ‘stairs’) ... arranged like a staircase.” EX1001, 5:27-33.

81. FIG. N below shows another embodiment of a vertical memory block 500, which includes annotated FIGs. 7 and 8 of the '974 Patent. Vertical memory block 500 includes features and elements similar to vertical memory block 100 described above with reference to FIGs. L and M. EX1001, 8:49-53. Additionally, as shown in FIG. N, vertical memory block 500 further includes an additional slot 514A (in blue) that further splits a conductive layer 516 in the stair step region into distinct word line portions 516B and 516C (in gray). Additional slot 514A may extend in a longitudinal y-direction to proximate but not connect with another slot 514 (in green). EX1001, 9:5-15.

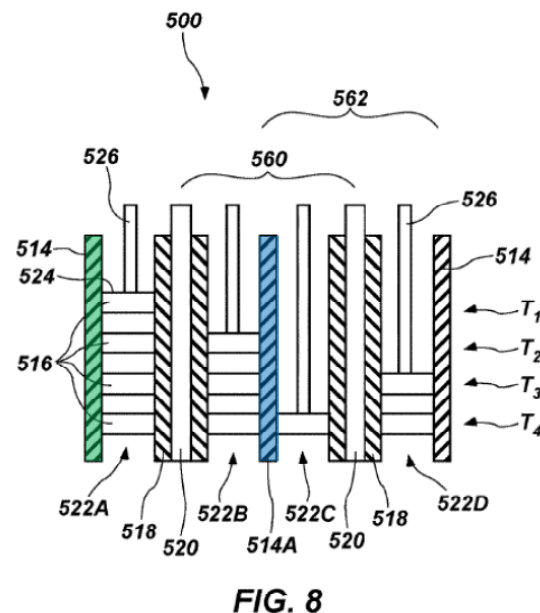
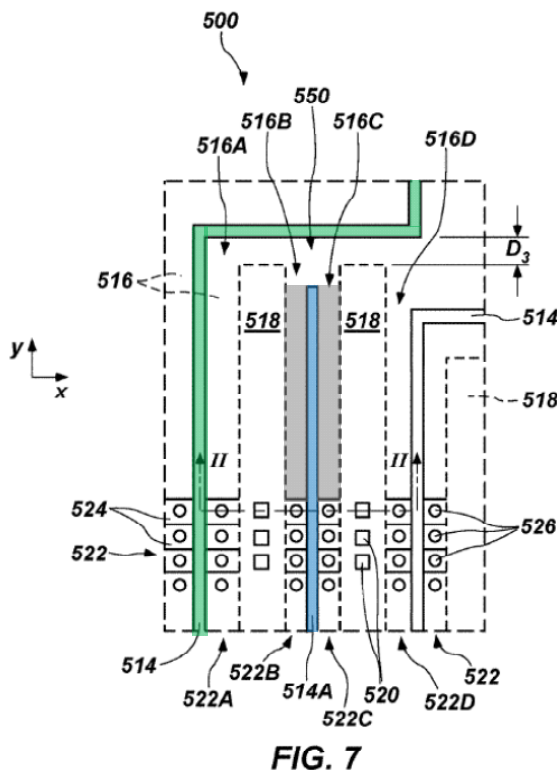


FIG. N – FIGs. 7 and 8 of EX1001 (annotated)

2. *Applicant-Admitted Prior Art*

82. I noted that, in various instances, the '974 Patent acknowledges certain technologies used in 3D NAND flash memory as well-known prior art. In my declaration, I refer to these acknowledgments as applicant-admitted prior art ("AAPA"). These self-admissions are consistent with the state of the art before the '974 Patent, as discussed in Section VI. See Section VI.

83. For example, in its Background Section, the '974 Patent expressly describes that **conventional** MONOS type memory arrays may be formed by (i) forming the semiconductor pillars through a stack of alternating first and second dielectric materials, (ii) forming slots through the stack adjacent to the semiconductor pillars, (iii) removing the second dielectric materials through the slots, and (iv) replacing the second dielectric materials with a conductive material to form word line plates. During such a process, the second dielectric material is replaced by the conductive material, such that a body of the vertical memory array includes alternating layers of the first dielectric material and the conductive word line plates. EX1001, 1:43-59. In other words, the '974 Patent explicitly acknowledges that the process of forming "alternating layers of the first dielectric material and the conductive word line plates" is "**conventional**" (referred to herein as "AAPA-1"). This process is widely recognized by a POSITA as the "gate replacement process," as I explained in Section VI.C above.

84. Further, the '974 Patent states that “[a]s is **known by those of ordinary skill in the art**, stair step structures for electrical connection to conductive word lines (or word line plates) at the tiers of vertical memory blocks may be formed by utilizing a so-called ‘stair step mask’ and, optionally, one or more so-called ‘chop masks.’” EX1001, 9:30-34. Following immediately, the '974 Patent describes a trim-etch process, which is a well-known technique to a POSITA, as I explained above in Section VI.D.2.a, for creating consecutive steps with the “stair step mask” as follows:

“A stair step mask may be formed over the vertical memory block while leaving one step-width (e.g., a width of one contact region 524 measured in the longitudinal direction y) exposed. One or more tiers of conductive material (e.g., of the conductive word lines 516) exposed through the stair step mask may be removed, such as by a first cycle of anisotropic material removal (e.g., etching). An edge of the stair step mask may be removed to recess the edge of the stair step mask and to expose another step-width, in addition to the original exposed step-width. Another cycle of material removal may be performed to remove another one or more tiers of conductive material exposed through the recessed stair step mask. The process may be repeated to form a desired number of contact regions (e.g., contact regions 524, also referred to as “stairs”).” EX1001, 9:34-49.

85. Subsequently, before “[r]eturning to methods and structures of the present disclosure” (EX1001, 10:13-14), the '974 Patent further describes a chopping process using chop masks, which is also a well-known technique to a POSITA, as I explained above in Section VI.D.2.b. Specifically, the '974 Patent describes the following:

“A chop mask may be used cover one or more particular stair step structures or portions thereof (e.g., one or more of the stair step structures 522, 522A, 522B, 522C, 522D), while leaving one or more other stair step structures or portions thereof exposed through the chop mask. The entire exposed one or more other stair step structures or portions thereof is vertically recessed, such that one or more exposed tiers is removed. Thus, the one or more stair step structures exposed through the chop mask may be vertically recessed from the one or more stair step structures that is covered by the chop mask, such that the one or more exposed stair step structures defines contact regions (“stairs”) for tiers that are lower than the tiers having contact regions (“stairs”) for the one or more stair step structures covered by the chop mask. A chop mask may be used before or after the stair step mask is used. Chop masks are used to provide contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover. In addition, process control of removing material utilizing a stair step mask to form a stair step structure, as described above, may be difficult to maintain for a large number of cycles (e.g., more than about 12 cycles) and tiers. A single chop mask may be used to double the number of contact regions (“stairs”) of a stair step structure formed using a single stair step mask. By way of a non-limiting example, a stair step mask may be used to form a stair step structure of 12 contact regions, for accessing 12 respective tiers. A chop mask may be used to expose and access 12 additional tiers underlying the 12 tiers formed by the stair step mask alone.” EX1001, 9:50-10:11.

86. Further, the '974 Patent acknowledges that “[a]s generally described above with reference to FIGS. 7 and 8, the stair step structures 122 may be formed using a stair step mask and, optionally, one or more chop masks, as is **known to one of ordinary skill in the art.**” EX1001, 12:36-39.

87. Thus, the '974 Patent provides detailed descriptions of forming staircase structures using the stair step mask and chop masks, characterizing those processes as “**known by those of ordinary skill in the art**” (referred to herein as

“AAPA-2”). AAPA-2 includes the trim-etch process for creating consecutive steps with the “stair step mask,” as well as the chopping process with the “chop masks,” both of which are well-known techniques to a POSITA. *See* Section VI.D.2.

88. I noted that the '974 Patent clearly delineates the scope of AAPA-2 (EX1001, 9:30-10:11) by explicitly prefacing it with the phrase “[a]s is known by those of ordinary skill in the art” (9:30) and concluding it immediately before the statement “[r]eturning to methods and structures of the present disclosure” (EX1001, 10:12-13). Thus, it is very clear to me that the '974 Patent acknowledges that the entire two paragraphs between column 9, line 30 and column 10, line 11 are “known by those of ordinary skill in the art.” EX1001, 9:30.

B. File History of the '974 Patent

89. I have reviewed the File History of the '974 Patent. In the first Office Action on March 19, 2019, the Examiner rejected claims 1-20 of the '974 Patent on the ground of nonstatutory double patenting over its two parent patents: U.S. Patent Nos. 9,728,548 and 10,062,708. EX1002, 66-68.

90. The Office Action also indicated allowable subject matter in independent claims 1, 7, and 14, stating that the prior art on the record failed to teach the following claim limitations (with emphasis in italics):

*stair step structures in at least one stair step region;
conductive vias in at least one via region at least partially
located between the memory cell region and the at least one stair*

step region;

...

a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region. (claim 1)

forming stair step structures in the stair step region;
forming conductive vias in the via region;

...

forming slots extending between adjacent portions of individual access lines within the stair step region; and
forming a dielectric material within the slots. (claim 7)

forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;

forming at least one stair step region comprising stair step structures using a stair step mask, ...

removing at least a portion of the stair step structures using at least one chop mask. (claim 14)

EX1002, 68-69.

91. In response, Patent Owner filed a terminal disclaimer against the parent patents without making any substantive arguments on March 26, 2019. EX1002, 56. The Examiner then issued a Notice of Allowance on April 17, 2019. EX1002, 39.

C. Interpretation of the '974 Patent Challenged Claims

92. I have been instructed that the Challenged Claims of the '974 Patent are to be given their ordinary and customary meaning as understood by a POSITA at the time of the alleged invention in light of the specification and the prosecution history pertaining to the patent. I have followed these principles in my analysis set forth in this declaration. I reserve the right to supplement my opinions in this declaration to

the extent that any parties later propose claim constructions for any claim terms in the '974 Patent.

VIII. Overview of the Cited References

93. General descriptions provided for the following references and combinations thereof are incorporated into each subsection and mapping of the claims that includes citations to these references.

A. Lee (EX1004)

94. Lee is directed to 3D semiconductor devices. EX1004, [0003]. Lee “has been made in an effort to provide a three-dimensional semiconductor device capable of reducing a size of a semiconductor device and simplifying a manufacturing process.” EX1004, [0009], [0011].

1. Memory Cell Array

95. With reference to FIG. O shown below, which includes annotated FIGs. 1 and 2 of Lee, a semiconductor device 1000 may include a memory cell array 100 (in blue) and a peripheral circuit 200 configured to perform a program operation, a read operation, or an erase operation of memory cell array 100. EX1004, [0028]. Memory cell array 100 includes memory blocks 110 (in red). Peripheral circuit 200 includes a plurality of circuits, including row decoders 220a and 220b (in yellow) disposed under memory cell array 100, which may “decrease a size of the semiconductor device.” EX1004, [0029]-[0031].

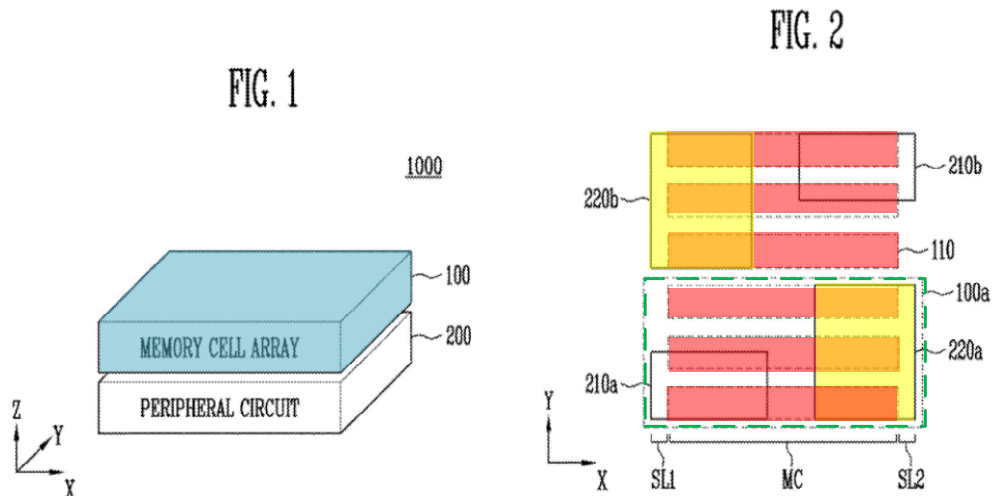


FIG. O – FIGs. 1 and 2 of EX1004 (annotated)

96. A region 100a (in a green dashed box) of memory cell array 100 shown in FIG. O is illustrated in FIG. P below. Memory cell array 100 includes a first slimming region SL1, a memory region MC, and a second slimming region SL2 arranged in the X-direction, with slimming regions SL1 and SL2 disposed on two opposite ends. The region in which memory blocks 110 are formed is defined as memory region MC. EX1004, [0034]. Vertical channel layers VC (parts of memory cell strings, see FIG. 3 of Lee) are formed in memory region MC. EX1004, [0036].

97. I noted that the “X-direction” in the figures of Lee corresponds to the “y-direction” in the ’974 patent, commonly known as the word line direction. Similarly, the “Y-direction” in the figures of Lee corresponds to the “x-direction” in the ’974 Patent, commonly known as the bit line direction. EX1004, [0045].

FIG. 4

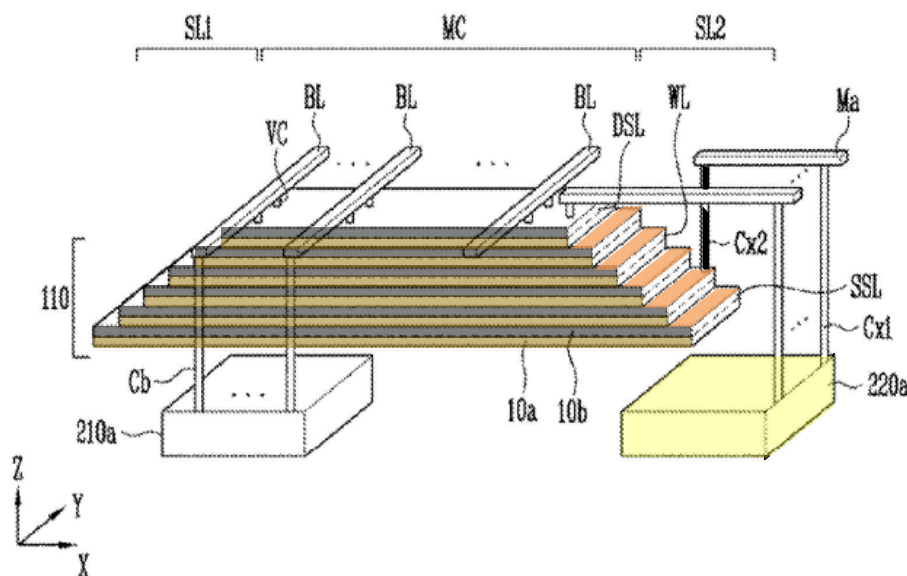


FIG. P – FIG. 4 of EX1004 (annotated)

98. In the Z-direction, memory cell array 100 includes a stack of alternating insulating layers 10a (in brown) and conductive layers 10b (in gray). EX1004, [0046]. Conductive layers 10b form source select lines SSL, word lines WL, and drain select lines DSL, which “are located in the memory region MC and extend in the X-direction hav[ing] step forms in the first slimming region SL1 and the second slimming region SL2.” EX1004, [0045], [0046]. Lee refers to source select lines SSL, word lines WL, and drain select lines DS collectively as “gate lines.” EX1004, claim 2.

2. *Contact Plugs in Second Slimming Region SL2*

99. As shown in FIG. P above, in a step structure of the second slimming

region SL2, contact plugs Cx2 (in black) are formed on the exposed ends (in orange) of gate lines SSL, WL, and DSL, which are respectively connected to row decoder 220a (in yellow) for transmitting operation voltages. EX1004, [0047].

100. Further, to reduce device size, Lee implements electrical connections between memory blocks 110 and sub-array row decoder 220a using various forms of TAVs in various contact regions arranged in the X-direction of slimming regions SL1 and SL2, as illustrated in FIGs. 11-14 of Lee.

101. For example, first contact plugs 32 (in black) are formed in a contact region CR21 of second slimming region SL2, as shown in FIG. Q below, which includes annotated FIG. 11 of Lee. FIG. Q shows detailed structures of second slimming region SL2 (also see FIG. 6 of Lee). Second slimming region SL2 includes a contact region CR21 (in light blue), a step region ST21 (in red), a contact region CR22, a step region ST22, a contact region CR23, and a step region ST23 sequentially defined in the X-direction. EX1004, [0056]. That is, with combined reference to FIGs. P and Q, contact region CR21 (in light blue) is positioned between memory region MC (in light green) and step region ST21 (in red). First contact plugs 32 (in black) are formed vertically, passing through a first blocking layer 31, in contact region CR21 to connect first row decoder 220a located below memory block 110. EX1004, [0077], [0078].

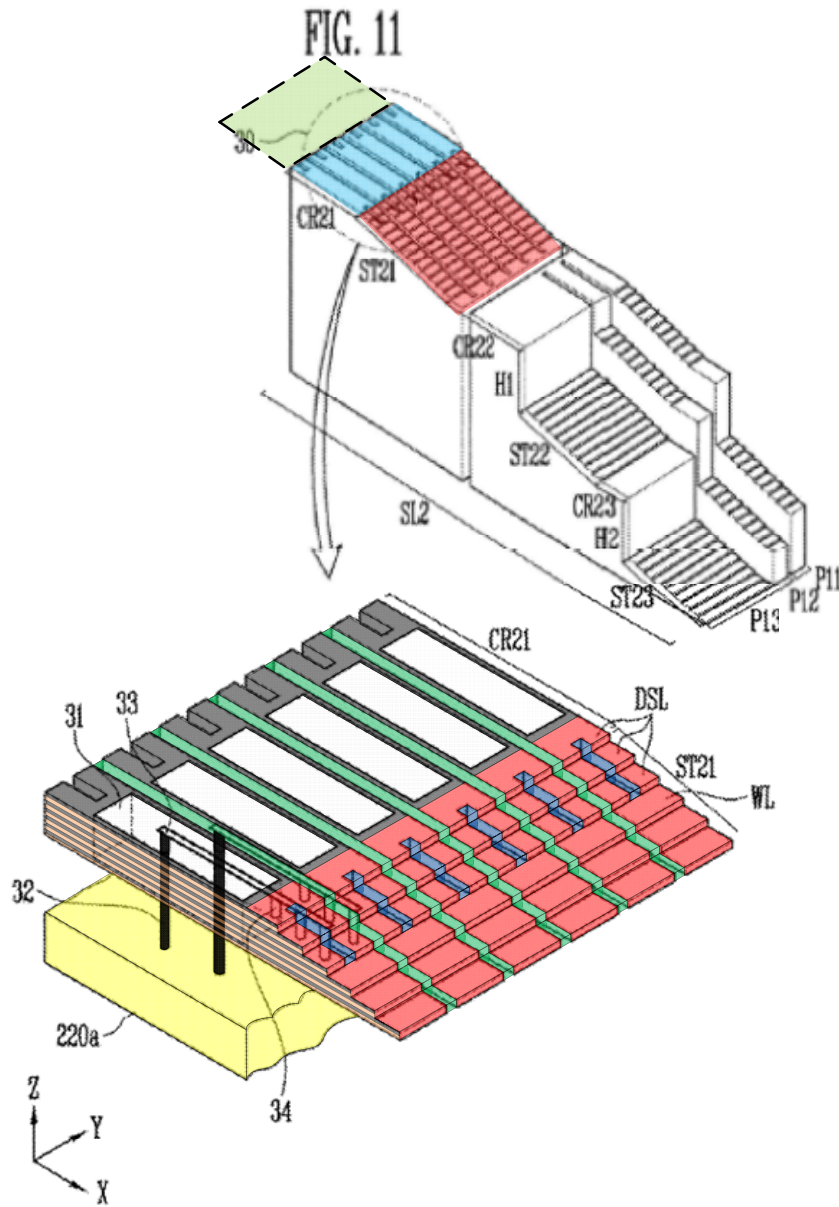


FIG. Q – FIG. 11 of EX1004 (annotated)

102. The top portion of FIG. Q also shows two additional step regions ST22 and ST23, where more exposed ends of word lines WL are formed in pad regions P11, P12, and P13 along the Y-direction to increase the degree of integration. EX1004, [0063].

3. *Slots*

103. In memory region MC, the gate lines (including source select lines SSL, word lines WL, and drain select lines DSL) formed by conductive layers 10a are **spaced apart** from each other in the Y-direction. A **spaced structure** of the respective gate lines SSL, WL, and DSL is omitted. EX1004, [0039]-[0041], [0046]. Thus, it is clear to me that, in memory region MC, parallel slots (for accommodating the spaced structure, in dark green) are present, which extend in the X-direction between adjacent gate lines and in the Z-direction through alternating insulating layers 10a and conductive layers 10b forming the gate lines.

104. Further, as shown in FIG. P above, the gate lines (including source select lines, word lines WL, and drain select lines DSL) extend across first slimming region SL1, memory region MC, and second slimming region SL2 in the X-direction. EX1004, [0049], [0050], [0053], [0054]. Thus, it is clear to me that parallel slots (parts of which are shown in dark green in FIG. Q above) are present and extend between adjacent gate lines throughout first slimming region SL1, memory region MC, and second slimming region SL2 in the X-direction (e.g., throughout memory cell array 100 in the X-direction). In the Z-direction, the parallel slots extend through alternating insulating layers 10a and conductive layers 10b.

105. For example, as illustrated in the enlarged view of contact region CR21 and part of step region ST21 in the bottom portion of FIG. Q shown above, the

parallel slots (in dark green) extend in the X-direction through contact region CR21 and step region ST21 and in the Z-direction through alternating insulating layers 10a (in brown) and conductive layers 10b (in gray). Furthermore, additional parallel slots (in dark blue) extend along the X-direction in part of step region ST21, further dividing conductive layers 10b at the drain select lines (DSL) levels into DSL portions.

106. Lee further discloses that the gate lines (e.g., word lines WL) formed on the same conductive layer 10b, though divided by the slots (in dark green), remain connected. EX1004, [0082]. Specifically, Lee explains that as “unit[s] of the cell string,” the word lines WL within the same conductive layer 10b are connected through various connecting structures, including but not limited to contact plugs 41 and wires 42. EX1004, [0082], [0087], FIGs. 12-13. Additionally, the DSL portions divided by the additional slot (in dark blue) are electrically connected to row decoder 220a via contact plugs 32 and 34, as shown in the bottom portion of FIG. Q above. EX1004, [0079]. Also, as illustrated in the bottom portion of FIG. Q above, the two DSL portions, although divided by the same additional slot (in dark blue) at the same vertical level, remain interconnected through the still-connected area in contact region CR21. *See also* EX1004, FIG. 12.

4. Fabrication Process for Forming Stair Step Structures

107. Lee also discloses the fabrication process for forming its first and

second slimming regions SL1 and SL2, including stair step structures. EX1004, [0064]-[0074], FIGs. 7-10. Specifically, Lee provides detailed descriptions of the “slimming process of etching gate lines extended from the memory region MC to the first slimming region SL1 and the second slimming region SL2, respectively, in a step form or a pad form,” as I will further explain in detail below in Section IX.G. EX1004, [0065]-[0066]; *see* Section IX.G.

B. Freeman (EX1005)

108. Freeman is directed to 3D semiconductor devices, in particular, methods for forming stair-step structures and devices including stair-step structures. EX1005, [0001]. Freeman discloses “[s]everal embodiments of stair-step structures and methods for forming stair-step structures,” by which “a margin of error in forming the plurality of stair-steps may be kept to a more reasonable and attainable level,” “a stair-step structure of the present disclosure may cover less area than some conventional stair-step structures,” and “a space between adjacent stair-step structures may be reduced in size.” EX1005, [0061].

109. Freeman’s methods for forming stair-step structures, specifically, the usage of a stair step mask and chop masks, matches well with AAPA-2, as well as the state-of-the-art discussed in Section VI.D.2, and supplements additional details to AAPA-2, as I will explain below in more detail in Section X.A.

1. First Embodiment of Forming Stair-Step Structure

110. FIGs. 2 through 10 of Freeman illustrate a first embodiment of a process for forming a stair-step structure. EX1005, [0009]. In the first embodiment, a first mask 116, “referred to as a stair-step mask 116,” is used to form an intermediate stair-step structure 150 in a stair-step region 124 (shown in FIG. 6 of Freeman), and a second mask, “referred to as a chop mask 126,” is then used to form a stair-step structure 100 having two regions 170 and 180 with separate contact regions (shown in FIG. 9 of Freeman). EX1005, [0028], [0035], [0036], [0038].

111. Specifically, a trim-etch process to form intermediate stair-step structure 150 is illustrated in FIG. R below, which includes FIGs. 2-5 of Freeman. First, in FIG. 2, stair-step mask 116 is patterned over a stack of conductive material 112 and insulating material 114b such that stair-step mask 116 is trimmed vertically and laterally. For example, stair-step mask 116 is trimmed laterally by removing a portion thereof at an outer edge of stair-step region 124, with a width 111 of a step. EX1005, [0028].

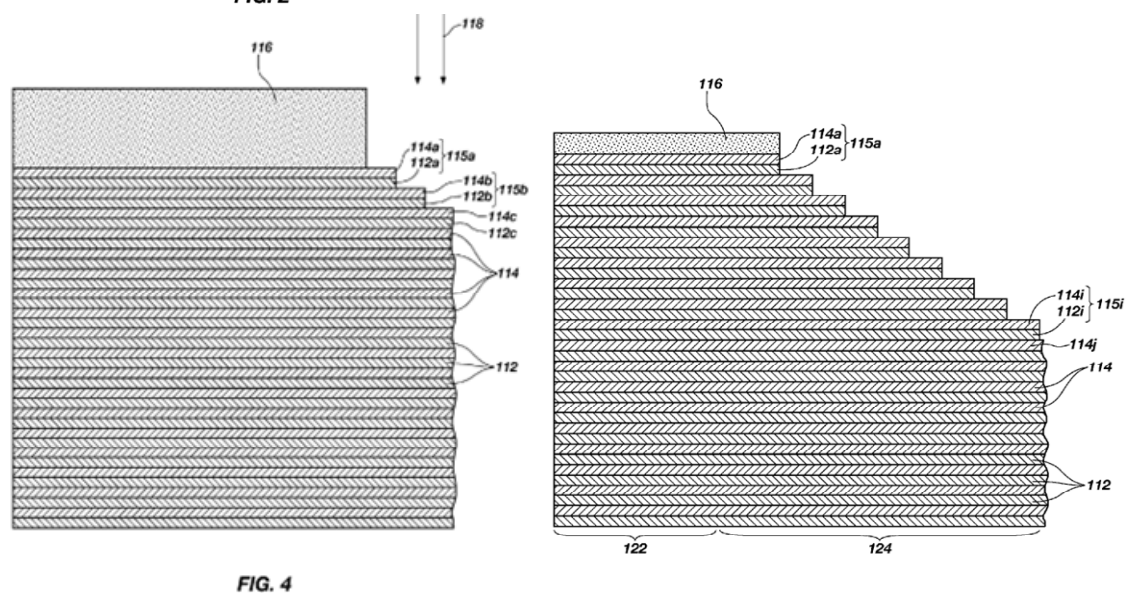
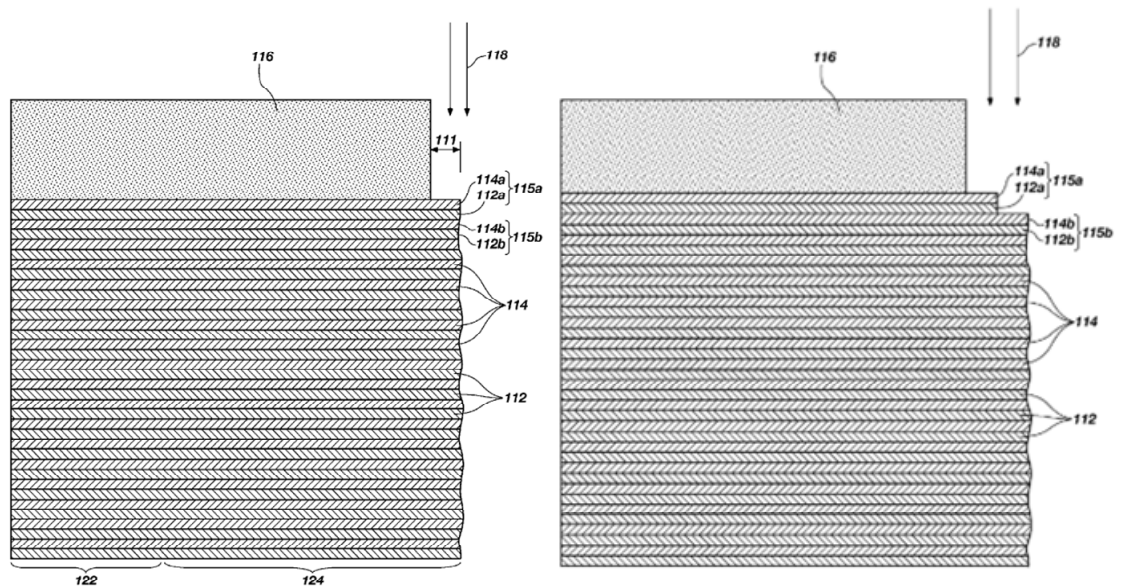


FIG. R – FIGs. 2-5 of EX1005

112. Second, in FIG. 3, a portion of a first set 115a of insulating material 114a and conductive material 112a exposed through stair-step mask 116 is removed by one cycle of anisotropic etch 118. EX1005, [0030], [0031].

113. Third, still in FIG. 3, stair-step mask 116 is patterned again by removing

another portion thereof (recessed) to expose another portion of insulating material 114a in first set 115a, with the width of a step. EX1005, [0032].

114. Fourth, in FIG. 4, the exposed portions of both first and second sets 115a and 115b are removed by one cycle of anisotropic etch 118. EX1005, [0033].

115. The processes described above with reference to FIGs. 2-4 of Freeman are repeated multiple times, as illustrated in FIG. 5, to form intermediate stair-step structure 150 shown in FIG. 6. EX1005, [0034]-[0035].

116. Further, a chopping process to form stair-step structure 100 is illustrated in FIG. S below, which includes FIGs. 7 and 8 of Freeman. To begin with, Freeman discloses, “[r]eferring now to FIG. 7, a second mask 126 (also referred to as a chop mask 126) may be formed over the insulating materials 114a through 114i and patterned to cover the array region 122 (not shown in FIG. 7) and a first region 170 of the stair-step region 124, while leaving a second region 180 of the stair-step region 124 exposed.” EX1005, [0036]. That is, Freeman further discloses chop mask 126 is patterned over insulation layers 114, covering a first region 170 of stair-step region 124 while leaving a second region 180 exposed. EX1005, [0036].

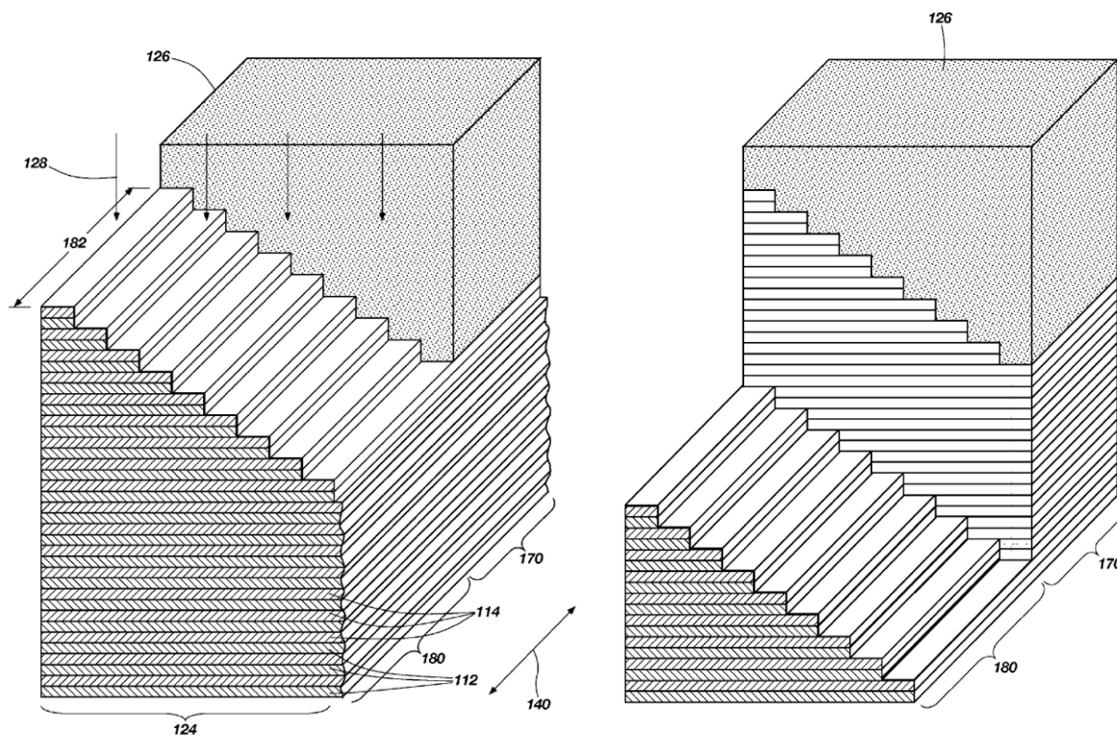


FIG. 7

FIG. 8

FIG. S – FIGs. 7 and 8 of EX1005

117. Next, as shown in FIG. 8, Freeman discloses “[t]he second region 180 may then be subjected to an anisotropic etch 128, including enough cycles to remove material from a number of sets 115 to expose the sets 115 of the bottom half of the stack, as shown in FIG. 8,” where anisotropic etch 128 may include: “a first dry etch act that selectively removes exposed portions of the insulating material 114; a second dry etch act that removes portions of the conductive material 112 that are exposed by the first dry etch act; a third dry etch act that removes portions of the insulating material 114 that are exposed by the second dry etch act; and so forth until the desired amount of material is removed.” EX1005, [0037]. That is, Freeman discloses that the exposed second region 180 is then etched to remove materials from

a number of sets 115 to expose sets 115 in the bottom portion of the stack, while leaving first region 170 covered by chop mask 126 intact. EX1005, [0037]. Once chop mask 126 is removed, stair-step structure 100, having separate contact regions in regions 170 and 180, is formed. EX1005, [0038], FIG. 9.

2. *Second Embodiment of Forming Stair-Step Structure*

118. FIGs. 11 through 14 of Freeman illustrate a second embodiment of a process for forming a stair-step structure. EX1005, [0043]. FIG. T below includes FIGs. 11 and 12 of Freeman, FIG. U below includes FIG. 13 of Freeman, and FIG. V below includes FIG. 14 of Freeman.

119. First, as shown in FIG. 11, an intermediate stair-step structure 250 may be formed using stair-step mask 116 by performing operations like those described above with reference to FIG. R. Steps are formed in the topmost four sets 215 (215a through 215d) of insulating materials 214 (214a through 214d) and conductive materials 212 (212a through 212d). EX1005, [0043]. A second mask 236 (a first chop mask 236) is formed over intermediate stair-step structure 250 by covering a first region 240 while exposing a second region 260. EX1005, [0043].

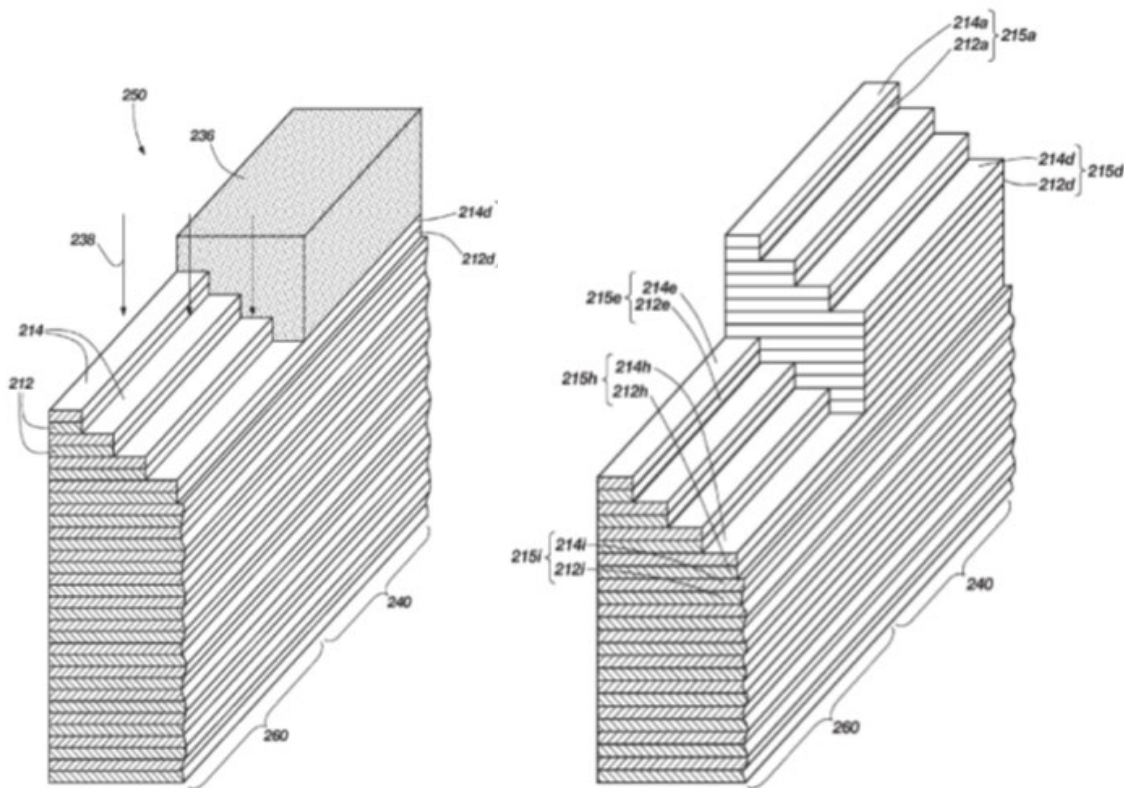


FIG. 11

FIG. 12

FIG. T – FIGs. 11 and 12 of EX1005

120. Second, as shown in FIG. 12, an anisotropic etch 238 including four cycles of removing insulating material 214 and conductive material 212 is performed on intermediate stair-step structure 250 to expose and form steps in the next four sets 215 (215e through 215h) in the exposed second region 260. A stair-step structure in the current form shown in FIG. 12 is formed. EX1005, [0043], [0044].

121. Third, with reference to FIG. 13 (shown in FIG. U below), a third mask 246 (a second chop mask 246 in addition to second mask/first chop mask 236) may be formed (i) over exposed insulating material 214a through 214d of a first portion

241 of first region 240 (FIG. 12) and (ii) over exposed insulating material 214e through 214h of a first portion 261 of second region 260 (FIG. 12). Third mask 246 (second chop mask 246) is patterned to expose a second portion 243 of first region 240 and a second portion 263 of second region 260. EX1005, [0045].

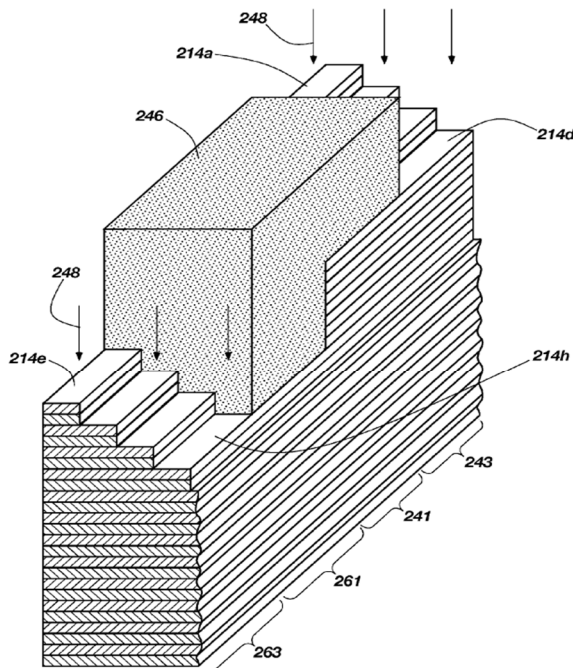


FIG. 13

FIG. U – FIG. 13 of EX1005

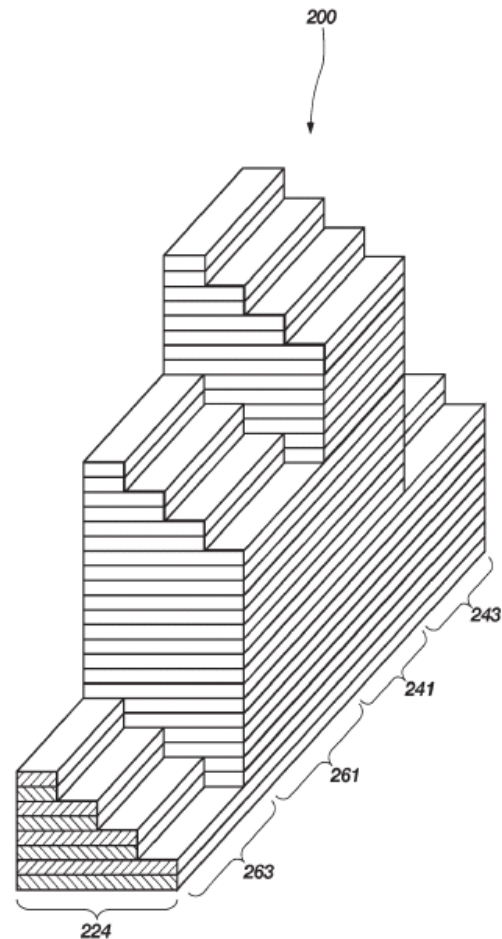


FIG. 14

FIG. V – FIG. 14 of EX1005

122. Fourth, with reference to FIG. 14 (shown in FIG. V above), another anisotropic etch 248 including eight cycles of removing insulating material 214 and conductive material 212 is performed to remove material from eight sets 215 in each

of the exposed portions 243 and 263. EX1005, [0046]. A resulting stair-step structure 200 includes four distinct regions 243, 241, 261, and 263 laterally adjacent one another, each providing exposure to a distinct one-fourth of the total number of sets 215. EX1005, [0046].

123. Freeman explains that the second embodiment “may begin in a similar fashion to that illustrated in FIGS. 2 through 6 to form an intermediate stair-step structure 250.” EX1005, [0043]. It is clear to me that Freeman’s second embodiment of forming stair-step structures uses two chop masks (e.g., 236 and 246) for the chopping process, as well as a single stair-step mask (e.g., 116) for the trim-etch process.

C. Lim (EX1006, EX1008)

124. Lim is directed to semiconductor devices and manufacturing methods thereof. EX1006, [0003]; EX1008, ¶1. Lim acknowledges the need for increasing semiconductor devices’ degree of integration in reducing their costs. EX1006, [0005]; EX1008, ¶2. To meet such a need, Lim discloses various designs and fabrication processes related to TAVs. EX1006, [0320]-[0321]; EX1008, ¶¶14-15.

1. First Embodiment of Semiconductor Device

125. A plan view of a first embodiment of a semiconductor device is shown in FIG. W below, which includes annotated FIG. 2A of Lim. A cross-sectional view showing areas taken along the lines I-I’ and II-II’ of FIG. 2A is shown in FIG. X

below, which includes annotated FIG. 3A of Lim. EX1006, [0074]; EX1008, ¶26.

FIG. 2A

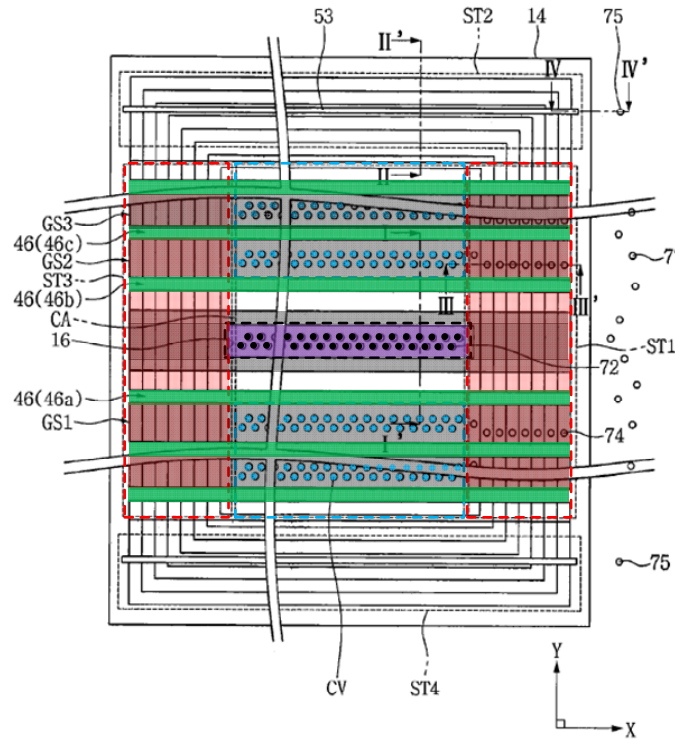


FIG. W – FIG. 2A of EX1006 and EX1008

FIG. 3A

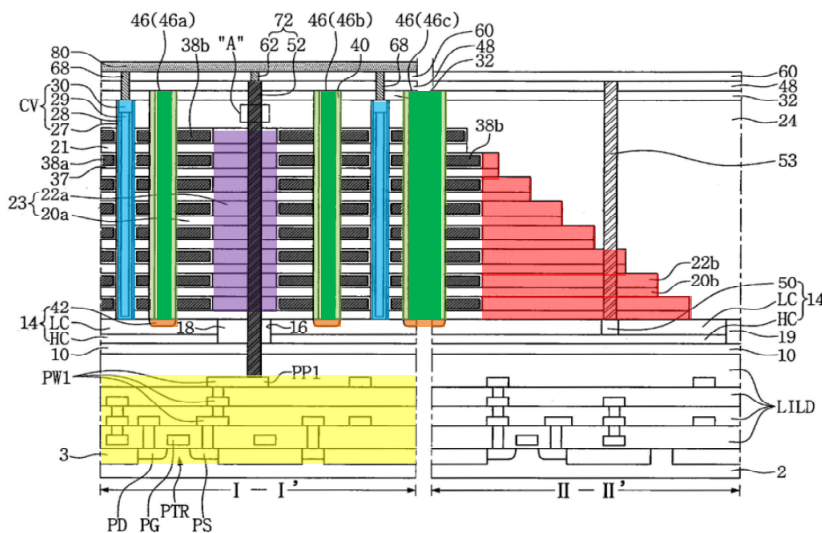


FIG. X – FIG. 3A of EX1006 and EX1008

126. As shown in FIGs. W and X above, the semiconductor device includes

(i) cell array areas CA (in blue dashed boxes) where cell vertical structures CV (in blue) are formed, (ii) an area (in black dashed box) where bit line lower contact plugs 52 in bit line contact structures 72 (in black) are formed, and (iii) step areas ST1 and ST3 (in red dashed boxes) at opposing ends each having step structures (in red). EX1006, [0086], [0089], [0098], [0109]-[0110]; EX1008, ¶¶38, 41, 50, 61-62.

a. Cell Source Patterns

127. As shown in FIGs. W and X above, cell source patterns 46 (in green), each including a conductive material (in dark green in FIG. 3A) and an insulating spacer 40 (in light green in FIG. 3A, e.g., silicon oxide) surrounding the conductive material, are formed to “cross the cell array area CA and to extend into the first and third step areas ST1 and ST3.” EX1006, [0104]; EX1008, ¶¶56, 180, 229.

128. Parallel cell source patterns 46 with different distances are formed along the Y-direction (bit line direction), each of which extends in the X-direction (word line direction). EX1006, [0104], [0106]; EX1008, ¶¶56, 58.

b. Cell Gate Conductive Structures GS1, GS2, and GS3

129. As shown in FIGs. W and X above, cell gate conductive structures GS1, GS2, and GS3 (in gray) “may extend from the cell array area CA into the first and third step areas ST1 and ST3.” EX1006, [0087]; EX1008, ¶39. Each cell gate conductive structure GS1, GS2, or GS3 includes cell gate conductive patterns 38a (shown in FIG. 3A), which are stacked and spaced apart from each other so as to

have a step structure in step areas ST1 and ST3. EX1006, [0089]; EX1008, ¶41.

c. TAVs

130. To enhance the integration density of semiconductor devices, Lim discloses various types of through-array vias (TAVs) that “vertically pass through the memory cell array area or are disposed near the memory cell array area” to establish vertical electrical connections to underlying components. EX1006, [0321]; EX1008, ¶15.

131. For example, as illustrated in FIG. X above, Lim describes contact plug 52 (black) passing through insulating structure 23 (purple) to electrically connect with peripheral transistors PTR (yellow) located beneath the memory block. EX1006, [0110]; EX1008, ¶62. Notably, similar to the '974 Patent, insulating structure 23, through which contact plug 52 passes, also includes a stack of alternating first and second insulating patterns 20a and 22a (e.g., alternating layers of silicon oxide and silicon nitride). EX1006, [0092], [0093]; EX1008, ¶¶44, 45.

2. *Fabrication Process of First Embodiment of Semiconductor Device*

132. Lim further discloses the detailed fabrication process of forming the first embodiment of the semiconductor device shown in FIGs. W and X above, such as the process for forming the stair step structures. EX1006, FIGs. 19-26B, [0196], [0197], [0208], [0227]; EX1008, FIGs. 19-26B, ¶¶148, 149, 160, 179.

133. To form contact plugs 52 passing through the stack of alternating first and second insulating patterns 20a and 22a, Lim discloses a “partial gate replacement” process modified from the well-known gate replacement process. Specifically, with reference to FIG. Y below, which includes annotated FIG. 23A of Lim, a first trench 34a, a second trench 34b, and a third trench 34c (collectively “trenches 34,” in green dash boxes) are formed to pass through a molding structure MS, among others, to expose a semiconductor pattern 14 underneath molding structure MS. EX1006, [0216]; EX1008, ¶168. Molding structure MS includes alternating first molding layers 20 (silicon oxide) and second molding layers 22 (silicon nitride). EX1006, [0208], [0209]; EX1008, ¶¶160, 161.

FIG. 23A

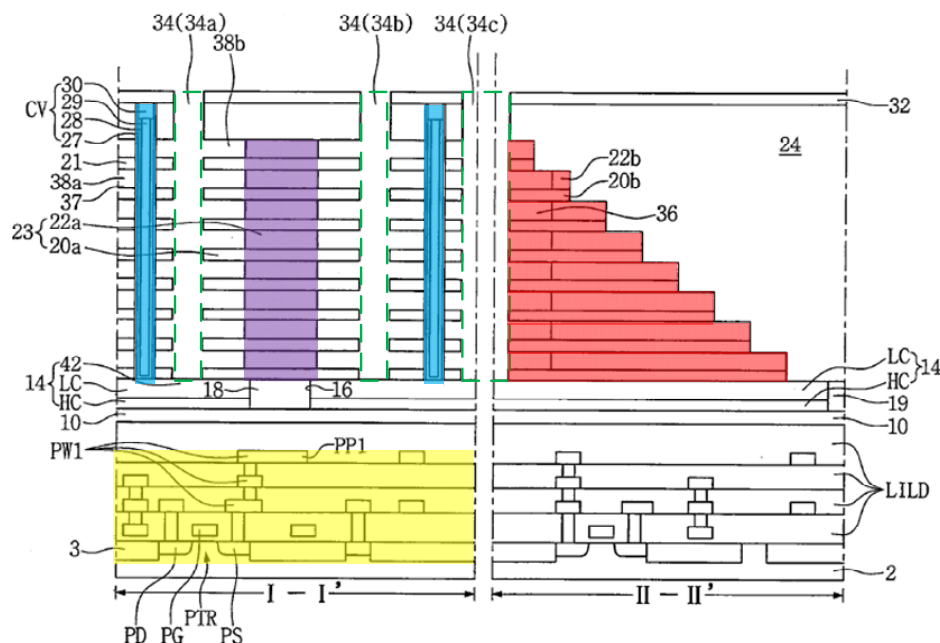


FIG. Y – FIG. 23A of EX1006 and EX1008 (annotated)

134. Lim also discloses etching parts of second molding layers 22 through trenches 34a, 34b, and 34c to form empty spaces 36. EX1006, [0221]; EX1008, ¶173. Because a distance between adjacent first and second trenches 34a and 34b is greater than a distance between adjacent second and third trenches 34b and 34c, second molding layers 22 between adjacent second and third trenches 34b and 34c are completely etched, whereas parts of second molding layers 22 which are located between first and second trenches 34a and 34b may “remain by **partially etching**” second molding layers 22 between first and second trenches 34a and 34b. EX1006, [0219], [0222]-[0224]; EX1008, ¶¶171, 174-176. Thus, insulating structure 23 (in purple) is “defined” herein to include a stack of alternating first insulating patterns 20a (parts of first molding layers 20) and second insulating patterns 22a (parts of second molding layers 22). EX1006, [0225]; EX1008, ¶177.

135. In other words, by forming “second and third trenches 34b and 34c in FIG. 23A [] more closely spaced apart from each other than the first and second trenches 34a and 34b,” after etching second molding layers 22 (e.g., silicon nitride) exposed by trenches 34 (in green dashed boxes), parts of second molding layers 22 that are “located between first and second trenches 34a and 34b, which are more widely spaced apart from each other, may remain by partially etching,” thereby forming the stack of alternating first and second insulating patterns 20a and 22a (defined as insulating structure 23, in purple). EX1006, [0219], [0221], [0222],

136. Next, with reference to FIG. Z below, which includes annotated FIG. 24A, Lim discloses forming gate conductive patterns (highlighted in gray) in empty spaces 36 between trenches 34. EX1006, [0226], [0227]; EX1008, ¶¶178, 179. That is, empty spaces 36 are filled with a conductive material to form gate conductive patterns. EX1006, [0226], [0227]; EX1008, ¶¶178, 179.

b. Formation of Cell Source Patterns 46

81

to fill trenches 34, thereby forming cell source patterns 46 connecting to source impurity regions 42. EX1006, [0228]-[0231]; EX1008, ¶¶180-183.

FIG. 25A

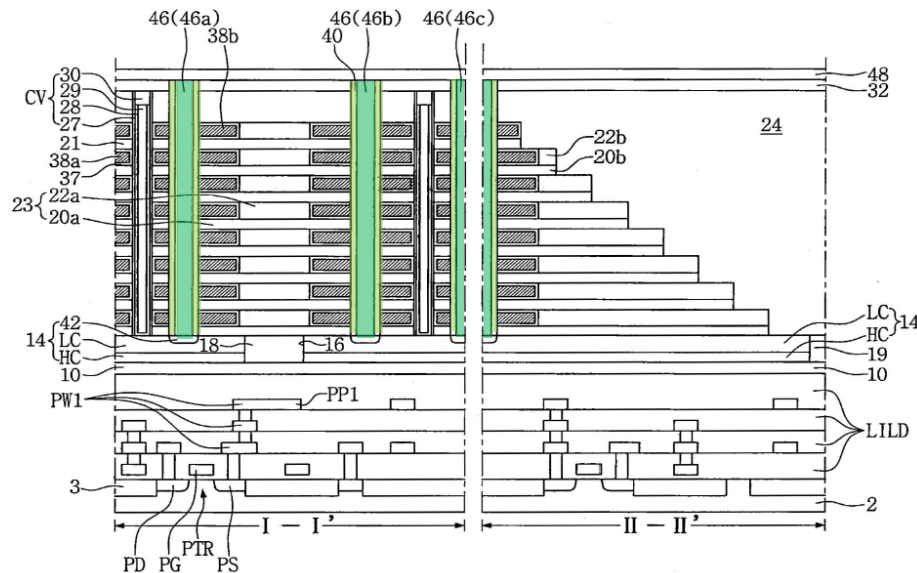


FIG. AA – FIG. 25A of EX1006 and EX1008 (annotated)

c. Formation of Contact Plugs 52 Passing Through Alternating Dielectric Materials

138. Eventually, with reference to FIG. AB shown below, which includes annotated FIG. 26A of Lim, contact plugs 52 (in black) passing through insulating structure 23 (in purple, e.g., a stack of alternating nitride and oxide materials) are formed by “forming contact holes by performing a photolithography process and an etching process, and forming a conductive material layer which fills the contact holes,” at the same processing steps with other contact structures 53, 54, and 55. EX1006, [0233], [0234], [0240], FIGs. 26A, 26B; EX1008, ¶¶185, 186, 192, FIGs. 26A, 26B.

FIG. 26A

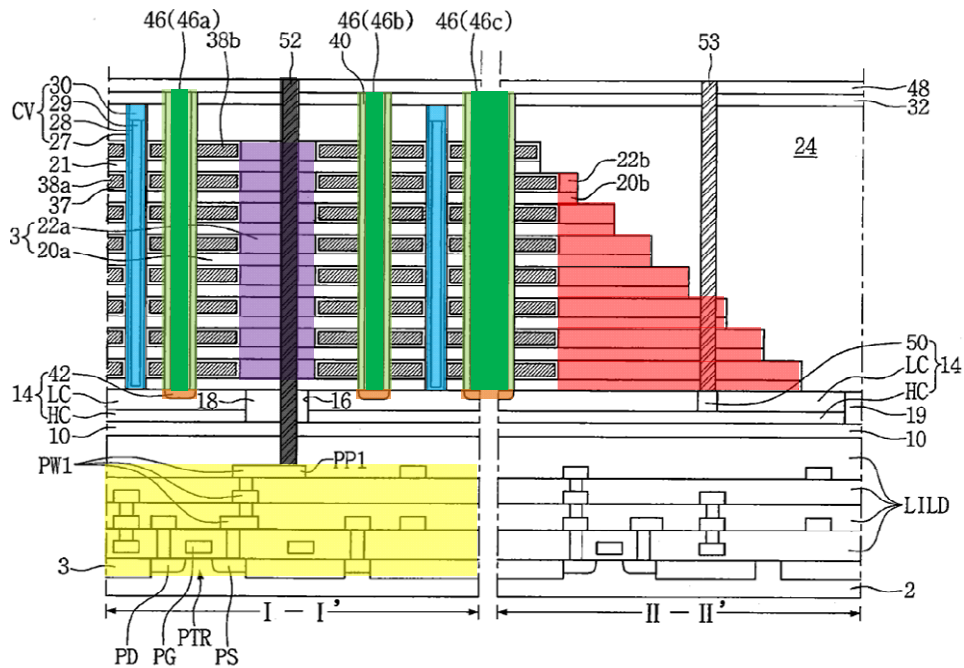


FIG. AB – FIG. 26A of EX1006 and EX1008 (annotated)

3. *Fabrication Process of Second Embodiment of Semiconductor Device*

139. A second embodiment of the semiconductor device is shown in FIG. J below, which includes annotated FIG. 32A of Lim (*see also* FIG. 11A of Lim). The second embodiment may have features and elements like that of the first embodiment. EX1006, [0137], [0138], FIG. 11A, FIG. 32A; EX1008, ¶¶89, 90, FIG. 11A, FIG. 32A.

FIG. 32A

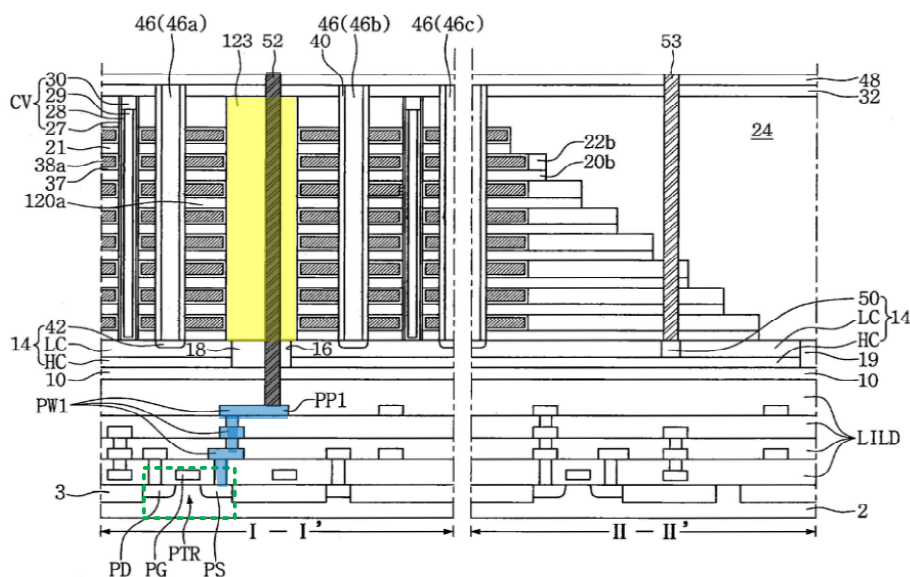


FIG. J – FIG. 32A of EX1006 and EX1008 (annotated)

140. As shown in FIG. J above, an insulating structure 123 (formed of silicon oxide, in yellow) may be formed between first and second source patterns 46a and 46b that are two of the source patterns 46 spaced apart from each other by a relatively long distance. EX1006, [0140], [0270]; EX1008, ¶¶92, 223. Contact plugs 52 penetrate insulating structure 123 to connect to underlying peripheral circuits such as a peripheral transistor PTR (in the green dotted box shown in FIG. J). EX1006, [0076], [0278]; EX1008, ¶¶28, 231. Comparing the first embodiment shown in FIG. AB with the second embodiment shown in FIG. J, insulating structure 123 (formed of silicon oxide) of the second embodiment is replaced by insulating structure 23 (formed of alternating silicon nitride and silicon oxide materials) of the first embodiment.

141. A method for forming the second embodiment of the semiconductor device is shown in FIG. AC below, which includes annotated FIG. 29 of Lim. EX1006, [0263]; EX1008, ¶216. With reference to FIG. AC, Lim discloses (i) forming insulating structure 123, which passes through molding structure MS (Block 340, in yellow), and (ii) forming contact structures (e.g., forming contact plug 52 in insulating structure 123) (Block 350). EX1006, [0264]; EX1008, ¶217.

FIG. 29

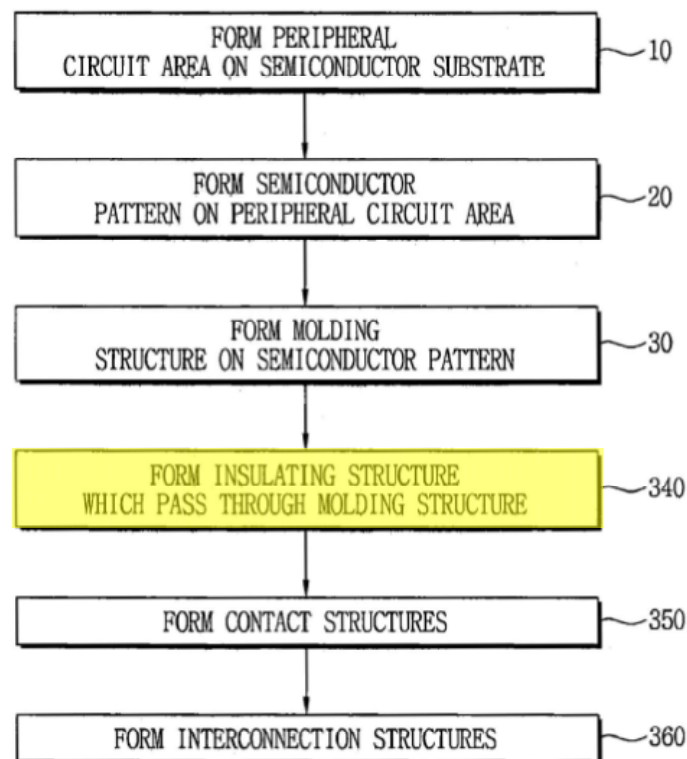


FIG. AC – FIG. 29 of EX1006 and EX1008 (annotated)

142. For example, with reference to FIG. AD below, which includes

annotated FIG. 30A, Lim discloses forming insulating structure 123 (in yellow) to pass through molding structure MS, among others. EX1006, [0269]; EX1008, ¶222. Then, as shown in FIG. J above, contact plugs 52 (in black) are formed to pass through insulating structure 123. EX1006, [0277], [0278], FIGs. 32A, 32B; EX1008, ¶¶230, 231, FIGs. 32A, 32B.

FIG. 30A

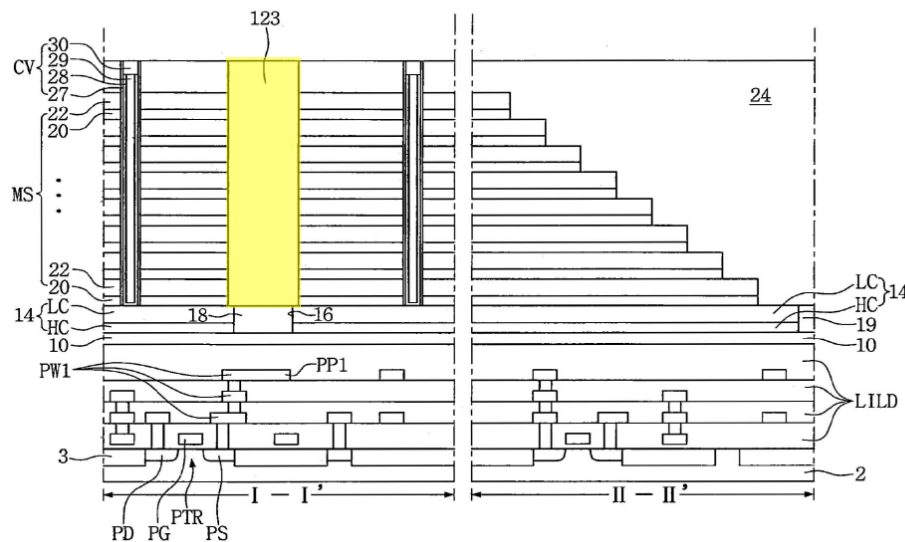


FIG. AD – FIG. 30A of EX1006 and EX1008 (annotated)

143. Comparing the process flows of the first and second embodiments, Lim introduces an additional step (340 in FIG. 29, FIG. 30A) before gate replacement in the second embodiment to form insulating structure 123. In contrast, the first embodiment eliminates this extra step by utilizing the partial gate replacement process, which simultaneously forms insulating structure 23. This approach allows contact plugs 52 to be subsequently formed through the pre-existing dielectric

materials of insulating structure 23, streamlining the fabrication process.

IX. Grounds 1 And 2: Lee Anticipates or Otherwise Renders Obvious Claims 1, 4, 5, 7, 9, and 11-19

144. As described in the following paragraphs, Lee anticipates or otherwise renders obvious all of the limitations found in claims 1, 4, 5, 7, 9, and 11-19 of the '974 Patent.

A. Independent Claim 1

145. Claim 1 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[1.P] A microelectronic device comprising:

[1.a] at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:

[1.a.1] an array of memory cells in a memory cell region;

[1.a.2] stair step structures in at least one stair step region;

[1.a.3] conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region;

[1.a.4] access lines extending through the at least one memory block; and

[1.a.5] a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.

[1.P] A microelectronic device comprising:

146. Specifically, Lee discloses a semiconductor device 1000, which is a “microelectronic device.” EX1004, [0028].

[1.a] at least one memory block operatively coupled to sub-array circuitry, the at least one memory block comprising:

147. Lee discloses “at least one memory block operatively coupled to sub-array circuitry.”

148. Specifically, Lee discloses that “semiconductor device 1000 may include memory cell array 100 in which data is stored and a peripheral circuit 200 configured to perform program, read operation, or erase operations on the memory cell array 100.” EX1004, [0028]. For example, with reference to FIG. O below (including annotated FIGs. 1 and 2 of Lee), semiconductor device 1000 includes (i) a memory cell array 100 (in blue) and (ii) peripheral circuit 200 configured to perform program, read operation, or erase operations on the memory cell array 100. EX1004, [0028].

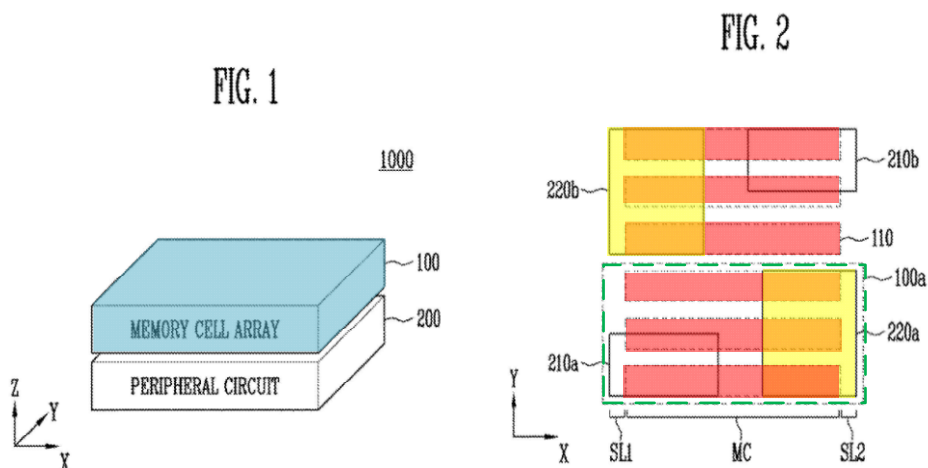


FIG. O – FIGs. 1 and 2 of EX1004 (annotated)

149. Lee further discloses that peripheral circuit 200 may include a plurality of circuits, which may decrease a size of semiconductor device 1000, and some of the circuits included in peripheral circuit 200 may be disposed **under** memory cell array 100. EX1004, [0029]. For example, peripheral circuit 200 includes row decoders 220a and 220b (in yellow shown in FIG. O above) disposed under the memory cell array 100. EX1004, [0030].

150. Likewise, the '974 Patent describes a sub-array circuitry (e.g., circuit 136) as a circuit positioned under vertical memory block 100. EX1001, 6:49-54, FIG. 3. Thus, it is clear to me that row decoder 220a is the claimed “sub-array circuitry,” consistent with the '974 Patent, because row decoder 220a is also positioned under memory cell array 100.

151. Lee also discloses that memory cell array 100 may include a plurality of memory blocks 110. Each of row decoders 220a and 220b may be divided into a plurality of circuit units for connection with memory blocks 110. EX1004, [0031]. For example, first row decoder 220a may be connected to some of memory blocks 110. EX1004, [0033].

152. Lee further discloses memory block 110 of memory cell array 100 may include source select lines SSL, word lines WL, drain select lines DSL, and bit lines BL. EX1004, [0036]. The source select lines, the word lines, and the drain select lines extended in slimming regions SL1 and SL2 may be connected to row decoders

220a and 220b through contacts. EX1004, [0035]. For example, row decoder 220a transmits operation voltages through the lines SSL, WL, and DSL extended in first and second slimming regions SL1 and SL2. EX1004, [0047]. Particularly, as shown in FIG. AJ below, (i) first contact plugs Cx1 are formed on first row decoder 220a, (ii) second contact plugs Cx2 (in black) are formed on the lines SSL, WL, and DSL exposed in a step structure in second slimming region SL2, and (iii) the upper portions of the first and second contact plugs Cx1 and Cx2 are connected to each other through wires MA, thereby achieving the connection between row decoder 220a and the lines SSL, WL, and DSL in a region 100a of memory cell array 100 shown in FIG. AJ. EX1004, [0034]-[0036], [0046], [0047].

FIG. 4

FIG. AJ –FIG. 4 of EX1004 (annotated)

153. Because the lines SSL, WL, and DSL in region 100a of memory cell array 100 are operatively coupled to row decoder 220a, a POSITA would have understood that memory cell array 100 is operatively coupled to row decoder 220a.

[1.a.1] an array of memory cells in a memory cell region

154. Lee discloses “an array of memory cells in a memory cell region.”

155. Firstly, Lee discloses that “memory cell array 100 may include a plurality of memory blocks 110.” EX1004, [0031]. Lee also discloses that “[t]he region in which the memory blocks 110[] are formed is defined as a memory region MC.” EX1004, [0034]. Thus, Lee discloses that memory cell array 100 includes memory block 110 formed in the memory region MC.

156. Secondly, Lee discloses that “memory blocks of the three-dimensional structure include memory cells stacked in a vertical direction to a substrate.” EX1004, [0005]. Lee also explains that a memory block includes a plurality of cell strings arranged in a direction vertical, where the memory strings include source select transistors, memory cells, and drain select transistors connected between bit lines and a source line, and “[t]he memory cells may be formed between the vertical channel layers and the word lines.” EX1004, [0006]. Thus, Lee discloses that memory block 110 includes an array of memory cells. For example, with reference to FIG. AE below, which includes annotated FIG. 3 of Lee, a POSITA would have understood that memory block 110 includes an array of memory cells (pointed to by

blue arrows) formed between vertical channel layers VC and word lines WL.

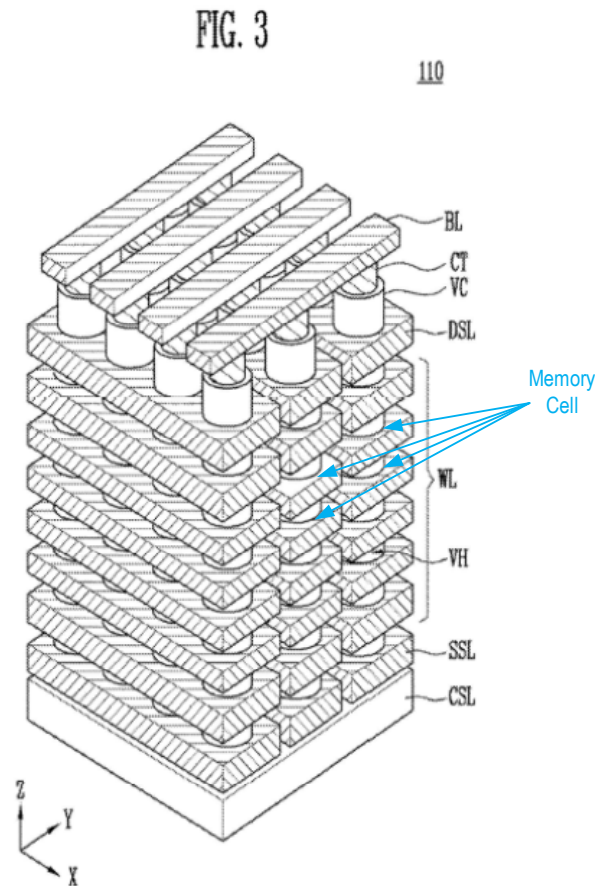


FIG. AE – FIG. 3 of EX1004 (annotated)

157. Because Lee discloses that (i) memory cell array 100 includes memory block 110 in memory region MC, and (ii) memory block 110 includes an array of memory cells, a POSITA would have understood that Lee discloses memory cell array 100 includes an array of memory cells in the memory region MC.

[1.a.2] stair step structures in at least one stair step region

158. Lee discloses “stair step structures in at least one stair step region.”

159. Specifically, Lee discloses that memory cell array 100 includes

multiple “step regions, wherein gate lines are included in the step regions and arranged **in a step form** in the first direction.” EX1004, [0009].

160. For example, as shown in FIG. AF below, which includes annotated FIG. 6 of Lee, second slimming region SL2 may include a contact region CR21, a **step region ST21**, a contact region CR22, a **step region ST22**, a contact region CR23, and a **step region ST23** sequentially defined in the X-direction (the word line direction). EX1004, [0056]. The source select lines SSL, the word lines WL, and the drain select lines DSL (collectively “gate lines,” see EX1004, claim 2) extended from the memory region MC are “formed in a step structure” in second slimming region SL2, such that the word lines WL may be stacked on the source lines SSL, and the drain select lines DSL may be sequentially stacked on the word lines WL “in a **step form**.” EX1004, [0054]. Lee further discloses that “**steps** may be generated between two neighboring contact regions,” i.e., in each step region ST21, ST22, or ST23. EX1004, [0055]. Thus, Lee discloses multiple step regions (e.g., ST21, ST22, ST23), each of which includes at least one structure formed by steps (referred to herein as “stepped structure,” in red in FIG. AF).

FIG. 6

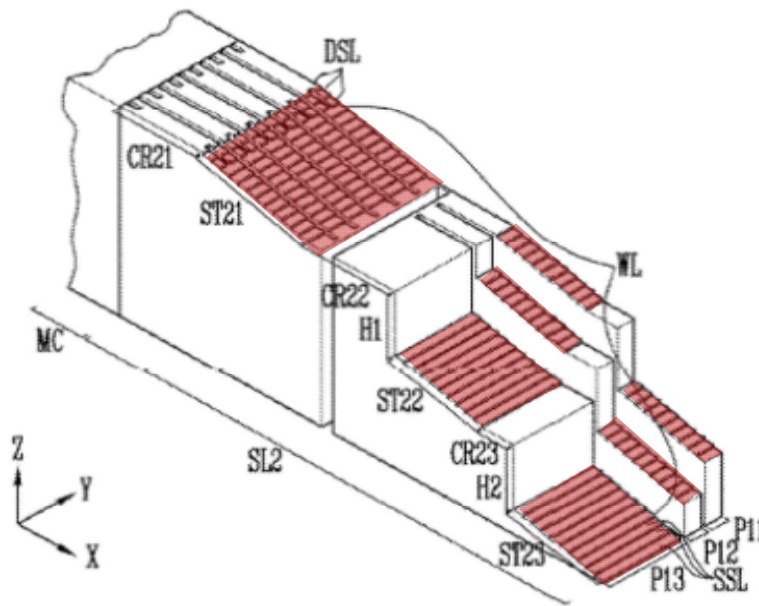


FIG. AF – FIG. 6 of EX1004 (annotated)

161. Thus, a POSITA would have understood that the stepped structures (in red) in the step regions ST21, ST22, and ST23 are the claimed “stair step structures in at least one stair step region,” consistent with the ’974 Patent—“[t]he stair step structures 122 may include contact regions 124 (“stairs”) ... **arranged like a staircase.**” EX1001, 5:30-33.

162. To the extent (not conceding) that claim limitation [1.a.2] further requires multiple stair step structures in one stair step region and/or along the bit line direction, Lee further discloses that second slimming region SL2 may include a pad region P11, a pad region P12, and a pad region P13 sequentially defined in the Y-

direction (the bit line direction). For example, pad region P11, pad region P12, and pad region P13 “overlap the 21st step region ST21, the 22nd contact region CR22, the 22nd step region ST22, the 23rd contact region CR23, and the 23rd step region ST23 within the second sliming region SL2.” EX1004, [0056]. Each pad region P11, P12, or P13 includes one or more stepped structures as “the step is formed in the word lines WL for each pad region within the step region.” EX1004, [0063].

FIG. 6

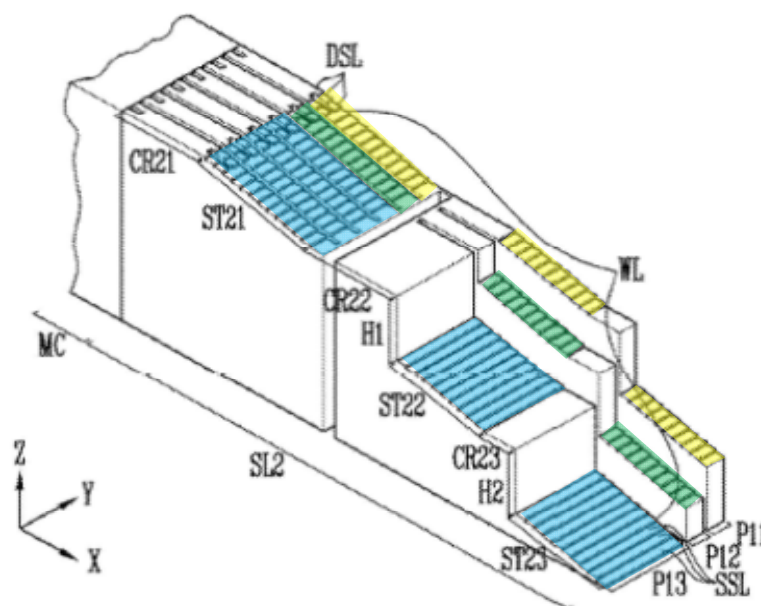


FIG. AG – FIG. 6 of EX1004 (annotated)

163. A POSITA thus would have understood, as depicted in FIG. AG shown above, which includes annotated FIG. 6 of Lee, (i) each step region ST21, ST22, or ST23 includes multiple pad regions (e.g., P11, P12, and P13) overlapping along the

bit line direction, and (ii) each overlapping pad region P11, P12, or P13 has steps formed therein, e.g., having stepped structures therein (in yellow, green, and blue, respectively).

[1.a.3] conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region

164. Lee discloses “conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region.”

165. For example, with reference to FIG. AH shown below, Lee discloses “the second slimming region SL2 may include a **21st contact region CR21**, a 21st step region ST21, a 22nd contact region CR22, a 22nd step region ST22, a 23rd contact region CR23, and a 23rd step region ST23 **sequentially defined in the X-direction.**” EX1004, [0056]. Thus, Lee discloses that contact region CR21 (in blue) is located between memory region MC (in light green) and step regions ST21, ST22, and ST23 (in red) in the X-direction. Also, since contact region 22, step region ST22, contact region CR23, and step region ST23 are sequentially defined in the X-direction, Lee also discloses that (i) contact region CR22 is also located between memory region MC and step regions ST22 and ST23, and (ii) contact region CR23 is further located between memory region MC and step region ST23. EX1004, [0056].

FIG. 6

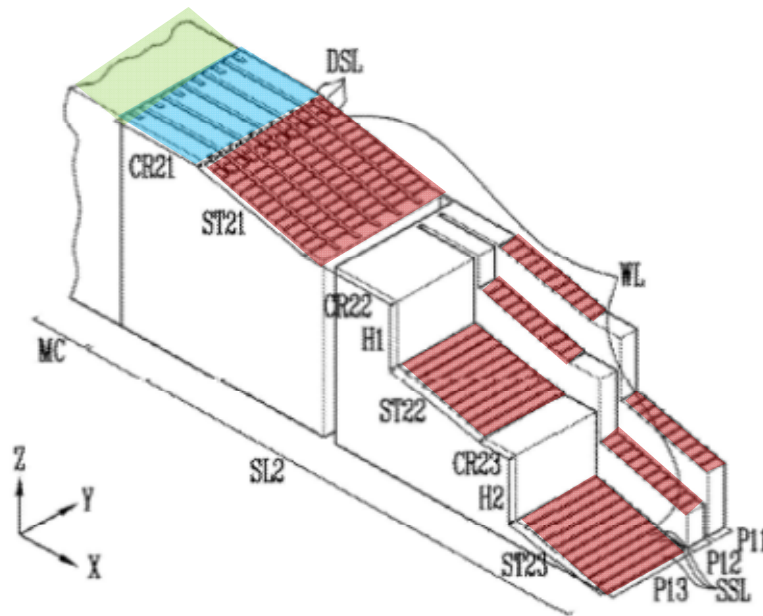


FIG. AH – FIG. 6 of EX1004 (annotated)

166. With reference to FIG. AI shown below (which includes the bottom portion of FIG. 11 of Lee, illustrating “an enlarged view of a portion 30 of the 21st contact region CR21 and the 21st step region ST21”), first blocking layers 31 are formed within contact region CR21 (in blue). Contact plugs 32 “positioned vertically that is, in a [Z]-direction passing through the first blocking layers 31 are formed” in contact region CR21 (in blue). EX1004, [0077]. Lee explains that contact plugs 32 are “connected to the first row decoder 220a located at the lower portion of the memory block” and “formed of conductive layers.” EX1004, [0078], [0079].

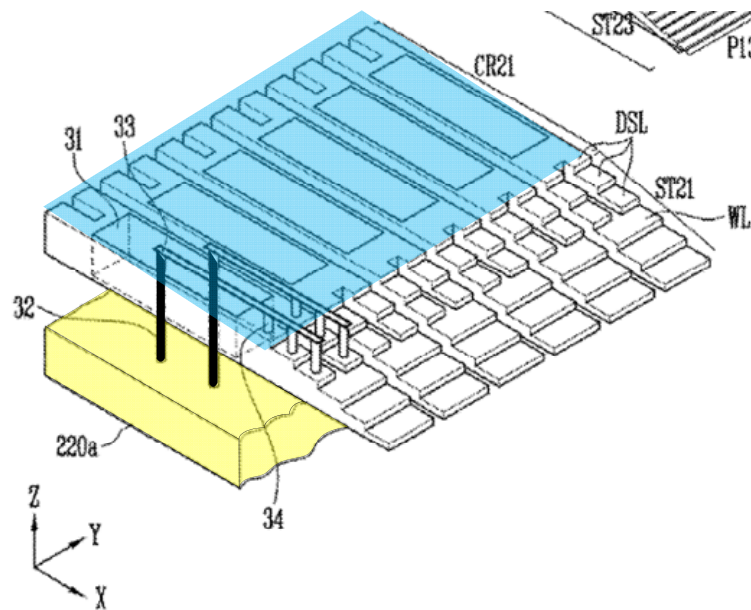


FIG. AI – Bottom portion of FIG. 11 of EX1004 (annotated)

167. Likewise, the '974 Patent discloses that conductive vias 120 “extend through the vertical memory block 100” to be “electrically coupled to sub-array circuitry 136” and have “a conductive via material.” EX1001, 5:17-21, 6:49-52, 12:22-27. Thus, a POSITA would have understood that first contact plugs 32 are the claimed “conductive vias,” as they are also formed of conductive materials and extend vertically through first blocking layer 31 to connect underneath row decoder 220a, just like conductive vias 120 of the '974 Patent.

[1.a.4] access lines extending through the at least one memory block

168. Lee discloses “access lines extending through the at least one memory block.”

169. Specifically, Lee discloses memory cell array 100 further includes

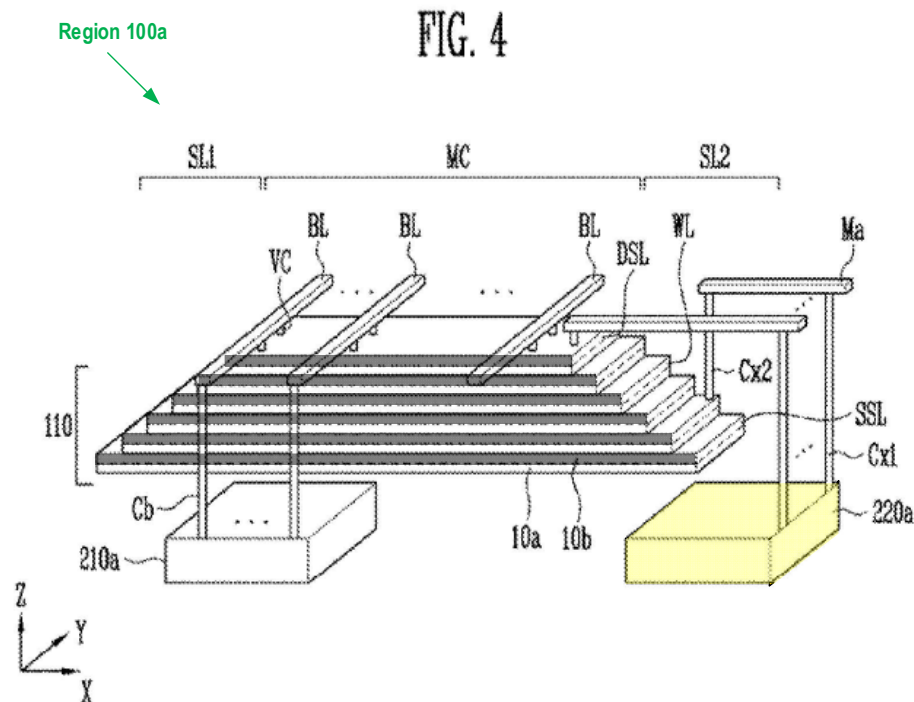
conductive layers 10b forming gate lines and extending through memory cell array 100. EX1004, [0045]-[0047].

170. Lee discloses that “[t]he source select lines SSL, the word lines WL, and the drain select lines DSL may be formed of conductive layers 10b, and insulating layers 10a may be formed between the respective lines.” EX1004, [0046]. Lee also discloses that row decoder 220a “transmits operation voltages through the first or second slimming region SL1 or SL2, or the lines SSL, WL, and DSL extended in the first and second slimming regions SL1 and SL2.” EX1004, [0047]. Lee further discloses “row decoder may transmit the operation voltages to source lines, word lines, and drain select lines connected to a selected memory block.” EX1004, [0008].

171. It is clear to me from those disclosures that conductive layers 10b, which form gate lines, are used to access the select transistors and memory cells in the memory region MC by “transmit[ting] operation voltages” to the select transistors and memory cells of a selected memory block in the memory region MC. EX1004, [0008], [0047]. Therefore, a POSITA would have understood that conductive layers 10b of Lee qualify as the claimed “access lines.”

172. Lee further discloses that the gate lines formed of conductive layers 10b are “located in the memory region MC and extend in the X-direction have step forms in the first slimming region SL1 and the second slimming region SL2.” EX1004,

[0045]. As shown in FIG. AJ below, a POSITA would have understood that conductive layers 10b (in black) at different vertical levels are the claimed “access lines,” respectively, and extend across memory region MC into slimming regions SL1 and SL2 in the X-direction.



[1.a.5] a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region

173. Lee discloses or at least suggests “a dielectric material within slots extending between adjacent access line portions of individual access lines within the at least one stair step region.”

174. Firstly, with reference to FIG. AK shown below, which includes

annotated FIG. 3 of Lee, Lee discloses that gate lines (e.g., source select lines SSL, word lines SSL, and drain select lines DSL) included in memory block 110 are **“spaced apart from each other in the Y-direction.”** EX1004, [0036], [0039]-[0041]. FIG. 3 is “a perspective view illustrating a memory block” in general. It is clear to me that FIG. 3 provides a general illustration of the 3D positions of various types of gate lines in a memory block, which applies to detailed examples in the later figures, such as FIG. 6, which depicts one example of second slimming region SL2 within the memory block. EX1004, [0036], [0053].

175. As shown in FIG. AK, slots (in dark green) are present and extend between adjacent gate lines in memory block 110 of memory region MC, such that the adjacent gate lines can be “spaced apart from each other in the Y-direction.” EX1004, [0039]-[0041]. For example, a POSITA would have understood or found it obvious that, in memory block 110 of memory region MC, the slots (in dark green) are trenches that (i) extend in the X-direction and Z-direction between adjacent gate lines and (ii) are arranged apart in the Y-direction by vertical channel layers (VC).

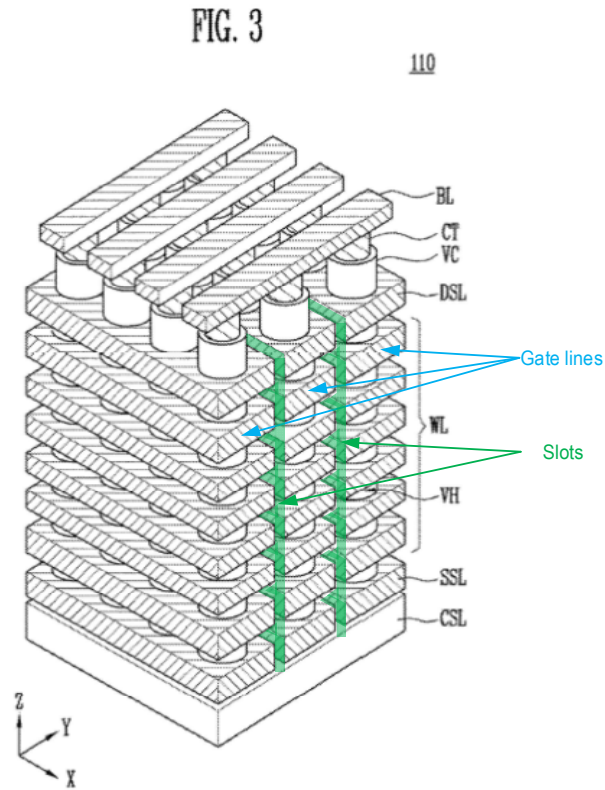


FIG. AK –FIG. 3 of EX1004 (annotated)

176. Further, as shown in FIG. AL below (which includes annotated FIG. 6 of Lee), multiple parallel slots (in dark green) are present and extend in the X-direction in step regions ST21, ST22, and ST23 in slimming region SL2.

FIG. 6

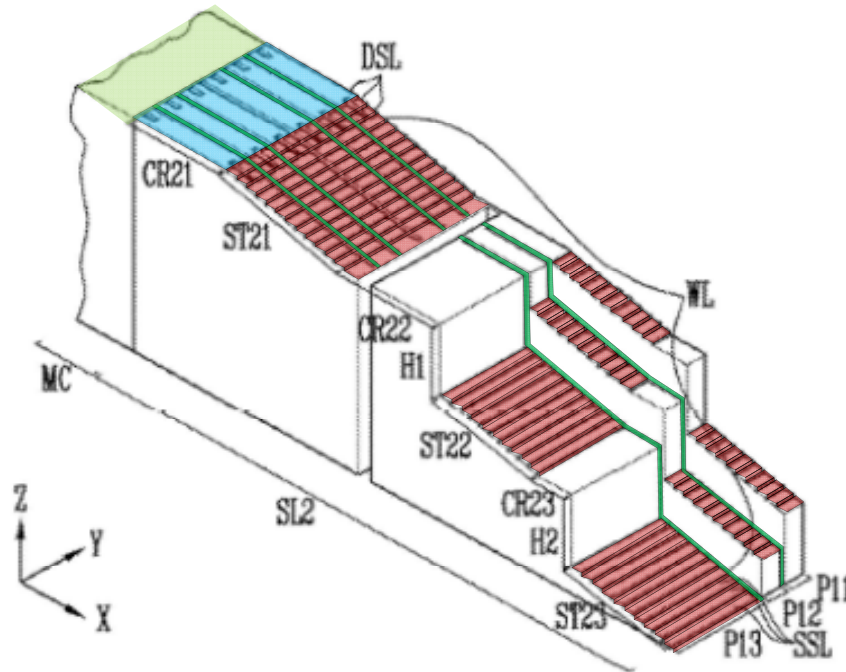


FIG. AL –FIG. 6 of EX1004 (annotated)

177. The presence of the slots extending between adjacent gate lines has numerous benefits. For example, the slots physically separate memory blocks, and safeguard adjacent structures from damage during fabrication steps such as etching, annealing, and material deposition, thereby achieving process isolation in the fabrication steps. In another example, the slots simplify the fabrication of complex, vertically stacked layers by facilitating precise etching and addressing high aspect ratio challenges. They also enable the integration of peripheral circuitry, thereby improving the overall scalability of the device. In still another example, dividing

the memory stack into smaller sections using slots improves process uniformity, reduces defects, and enhances manufacturing yields. In yet another example, slots aid in heat dissipation by distributing thermal loads more evenly, minimizing hotspots, and improving overall thermal stability.

178. With combined reference to FIG. AK and FIG. AL shown above, a POSITA would have understood, or at least found it obvious, that the slots (in dark green) extend in both the Z-direction and X-direction and divide each conductive layer 10b (shown in FIG. AJ) into adjacent gate lines of the respective conductive layer 10b, which are “spaced apart from each other in the Y-direction.” EX1004, [0039]-[0041].

179. For example, for word lines WL, Lee discloses that “the word lines WL formed **on the same layer** may so be electrically connected to each other,” “the third contact plugs 41 ... are formed on the word lines WL **divided** in the unit of the cell string, respectively” (FIG. 12 of Lee), and that “the 11th pad region P11 has the same width as a width of the word lines WL **divided** in the unit of the cell string” (FIG. 13 of Lee). EX1004, [0082], [0087]. A POSITA would have understood, or at least found it obvious, that at each word line level, a respective conductive layer 10b is divided by the slots into word lines in the Y-direction.

180. In an example, as shown in FIG. AM below (which includes the enlarged portion of FIG. 11), five slots (in dark green) divide three conductive layers

10b each into six word lines (in yellow) along the Y-direction.

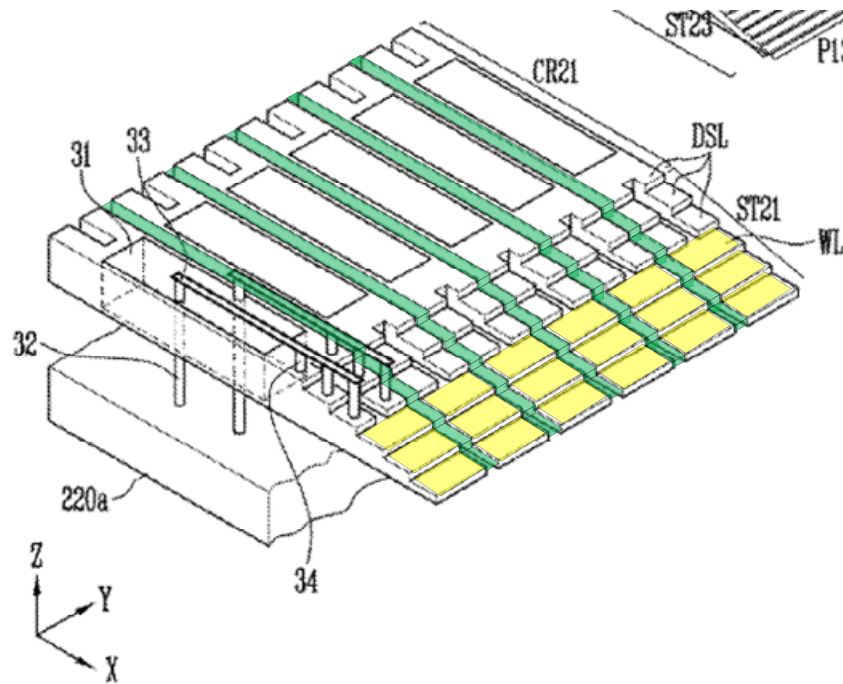


FIG. AM – Bottom portion of FIG. 11 of EX1004 (annotated)

181. Thus, Lee discloses, or at least suggests, “slots extending between adjacent access line portions of individual access lines within the at least one step region.”

182. As to the claimed “dielectric material within slots,” Lee explains, regarding FIG. 3 in which the slots are not shown as being filled— “[a]lthough not illustrated, insulating layers may be formed between ... the source select lines SSL, the word lines WL, the drain select lines DSL, and the bit lines VL.” EX1004, [0043]. Similarly, Lee explains that “[a] detailed structure, such as a spaced structure of the respective lines SSL, WL, and DSL, is omitted” from the schematic drawing of FIG. 4. EX1004, [0046]. Thus, it is clear to me that Lee discloses, or at a minimum

suggests, the claimed “dielectric material” within the slots.

183. In any event, a POSITA would have understood, or at least found it obvious, that the spaced structure includes a dielectric material in the slots, at least for the following reasons. Firstly, the slots have to be sealed in semiconductor device 1000 to avoid damage and contamination to other structures through the opened slots during the later fabrication process and provide mechanical stability to the structures above the slots. EX1013, [0064]. Open slots would expose underlying layers to external contaminants, oxidation, or chemical reactions, which could compromise device performance and reliability.

184. Also, slots mitigate stress caused by lattice and thermal mismatches during fabrication to prevent deformation, warping, or collapse of the memory stack. Filling the slots with dielectric materials can further enhance the mechanical stability and structural integrity of the device. This becomes increasingly critical as memory stacks incorporate higher numbers of layers, where stress accumulation is more pronounced.

185. Moreover, the slots need to be filled to ensure a smooth and even upper surface, which is essential for subsequent photolithography and patterning steps. The presence of open or uneven slots could lead to variations in focus during lithographic exposure, resulting in patterning defects, misalignment, or non-uniform etching.

186. Secondly, the sealing materials used to fill the slots must include at least a dielectric material (e.g., silicon oxide) to prevent electrical connections between gate lines at different vertical levels. This is a well-established practice in the memory industry, as evidenced by numerous examples in prior art. EX1006, [0228], [0276]; EX1008, ¶¶180, 229; EX1009, [0071], FIG. 1C; EX1010, [0139], FIG.16B; EX1011, [0093], FIG. 5; EX1018, [0095], [0105]; EX1019; [0143].

187. Specifically, filling the slots with dielectric materials serves a critical role in ensuring electrical isolation between vertically stacked gate lines, preventing electrical interference, crosstalk, and unintended conduction between adjacent levels. In fact, dielectric material filled in a trench has long been employed to form isolation regions in integrated circuits. EX1020, Figure 2.27, p. 99. These principles naturally extend to 3D NAND flash memory as well. In 3D NAND flash memory devices, multiple gate layers are stacked vertically, and any unintended electrical connectivity between these layers could lead to logic errors, signal degradation, or even device failure. By incorporating a dielectric material, the slots act as effective electrical barriers, blocking charge leakage and unwanted capacitive coupling between adjacent layers. This ensures reliable memory cell operation by maintaining signal integrity and preventing short circuits across vertical levels. Without this isolation, the stored data in a memory cell could become corrupted due to parasitic interference, leading to decreased performance and reliability of the device.

188. Furthermore, the use of silicon oxide or other insulating materials to seal the slots also contributes to the mechanical reinforcement of the memory stack, further enhancing structural stability during fabrication and operation.

B. Dependent Claim 4

189. Claim 4 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[4.P] The microelectronic device of claim 1, wherein at least some of the stair step structures comprise:

[4.a] individual tiers aligned at different vertical levels from one another within a respective stair step structure; and

[4.b] contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.

[4.P] The microelectronic device of claim 1, wherein at least some of the stair step structures comprise:

190. Lee discloses or at least renders obvious the microelectronic device of claim 1. I incorporate my discussion for claim 1.

[4.a] individual tiers aligned at different vertical levels from one another within a respective stair step structure

191. Lee discloses, “individual tiers aligned at different vertical levels from one another within a respective stair step structure.”

192. At the outset, the '974 Patent describes “tiers of conductive structures

(e.g., word line plates, control gate plates, access lines, word lines) and dielectric materials” and “tiers of conductive structures (e.g., access lines, word lines) separated by dielectric materials.” EX1001, 1:35-37, 43-45. The ’974 Patent also explains that “five overlying conductive word lines 116 and five overlying first dielectric materials 132 between the conductive word lines 116” form “five tiers” in FIG. 3. EX1001, FIG. 3, 6:19-23.

193. With reference to FIG. AQ shown below, which includes annotated FIG. 4 of Lee, Lee discloses that insulating layers 10a are formed between conductive layers 10b forming the gate lines, and conductive layers 10b and insulating layers 10a are “paired to form one layer.” EX1004, [0046]. Like the ’974 Patent’ examples, a POSITA would have understood that each pair of conductive layer 10b and insulating layer 10a (referred to herein as “layer pair,” in purple) qualifies as the claimed “individual tier.”

194. As shown in FIG. AQ, layer pairs (in purple) are stacked at different levels in the Z-direction. Under either mapping to “stair step structure,” as I discussed above in Section IX.A([1.a.2]), within each stepped structure of step regions ST21, ST22, and/or ST23 in slimming region SL2, layer pairs are “aligned at different vertical levels from one another.” See EX1004, FIG. 6.

FIG. 4

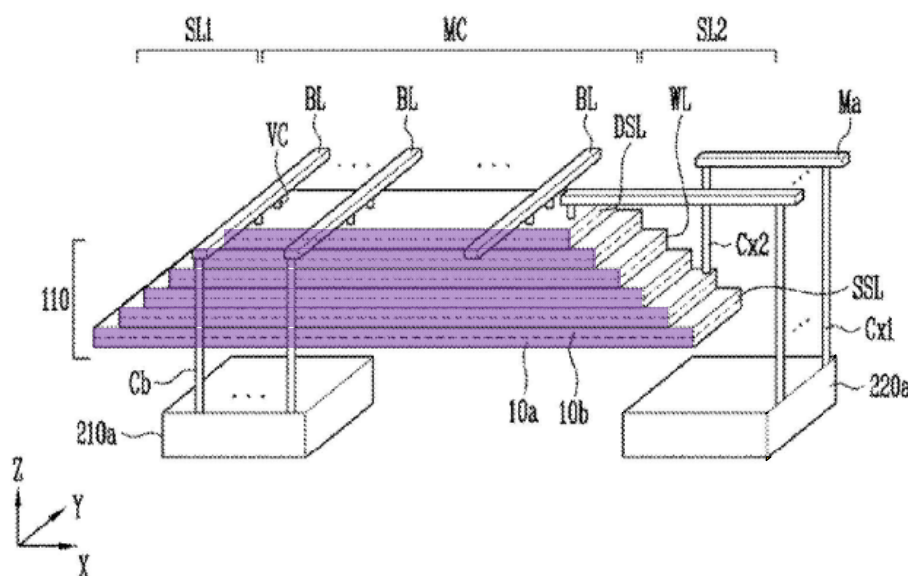


FIG. AQ –FIG. 4 of EX1004 (annotated)

195. To the extent (not conceding) that claim limitation [4.a] requires tiers in different stair step structures in the bit line direction to be aligned at different vertical levels from one another, with reference to FIG. AR shown below, which includes annotated FIG. 6 of Lee, Lee discloses that, in step region ST22, pad region P12 has “a smaller height than” that of pad region P11, and pad region P13 has “a smaller height than” that of pad region P12. EX1004, [0057]. That is, Lee discloses that, in step region ST22, pad regions P11, P12, and P13 have different heights.

196. For example, referring to FIG. 6, Lee further explains that “the uppermost word lines WL included in the 22nd step region ST22 and the 12th pad region P12 is located at a lower level than a word line located at the lowermost word

line WL included in the 22nd step region ST22 and the 11th pad region P11” and that “the uppermost word lines WL included in the 22nd step region ST22 and the 13th pad region P13 are located at a lower level than the lowermost word lines WL included in the 22nd step region ST22 and the 12th pad region P12.” EX1004, [0058]. That is, Lee discloses that, in step region ST22, the uppermost word line in pad region P12 is located at a level lower than the lowermost word line in pad region P11, and the uppermost word line in pad region P13 is located at a level lower than the lowermost word line in pad region P13.

FIG. 6

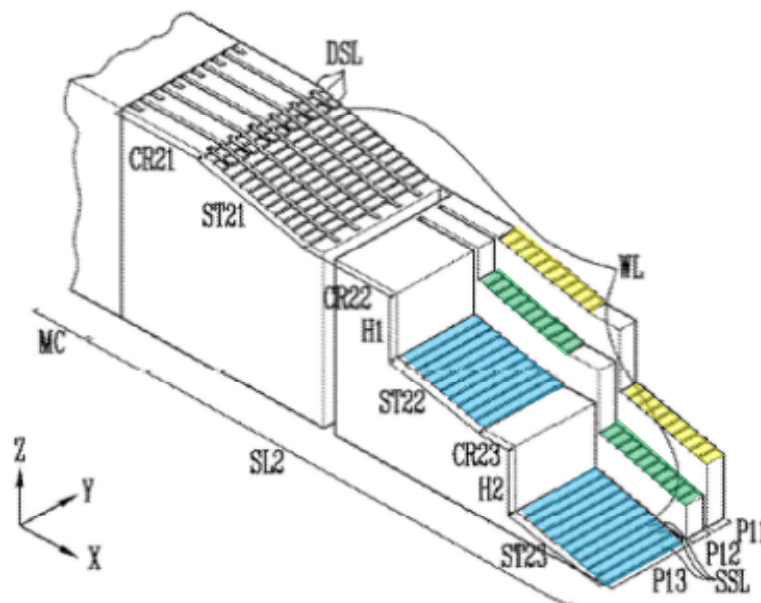


FIG. AR –FIG. 6 of EX1004 (annotated)

197. Lee also explains that “[t]he uppermost word line WL included in the

region, in which the 23rd step region ST23 and the 12th pad region P12 overlap each other, is located at a lower level than the lowermost word lines WL included in the region in which the 23rd step region ST23 and the 11th pad region P11 overlap each other,” and that “[t]he uppermost word line WL included in the region, in which the 23rd step region ST23 and the 13th pad region P13 overlap each other, is located at a lower level than the lowermost word line WL included in the region, in which the 23rd step region ST23 and the 12th pad region P12 overlap each other.” EX1004, [0061]. That is, Lee discloses that, in step region ST23, the uppermost word line in pad region P12 is located at a level lower than the lowermost word line in pad region P11, and the uppermost word line in pad region P13 is located at a level lower than the lowermost word line in pad region P12. In step region ST23, pad regions P11, P12, and P13 also have different heights like that in step region ST22.

198. Thus, at least in each of step regions ST22 and ST23, layer pairs in the different stepped structures in pad regions P11, P12, and P13 (in yellow, green, and blue) in the Y-direction are aligned at different vertical levels from one another as well.

[4.b] contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines

199. Lee discloses or at least suggests “contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective

access line portion of the individual access lines.”

200. Specifically, with reference to FIG. AS shown below, which includes annotated FIG. 4 of Lee, Lee explains that “contact plugs Cx2 are formed on the lines SSL, WL, and DSL **exposed in a step structure** in the second slimming region SL2.” EX1004, [0047]. Each layer pair (in purple) has a respective exposed end (in orange) on which contact plug Cx2 (in black) is formed. EX1004, [0047]. Lee also explains that “more **word lines WL are exposed** within the same step region” and “contact plugs may be connected to the plurality of word lines” in the step region. EX1004, [0063]. Thus, a POSITA would have understood, or at least found it obvious, that each layer pair has exposed ends of gate lines (e.g., word lines WL), where the exposed ends of gate lines are the claimed “contact regions” on which contact plugs (e.g., contact plugs Cx2) are formed in the stepped structures.

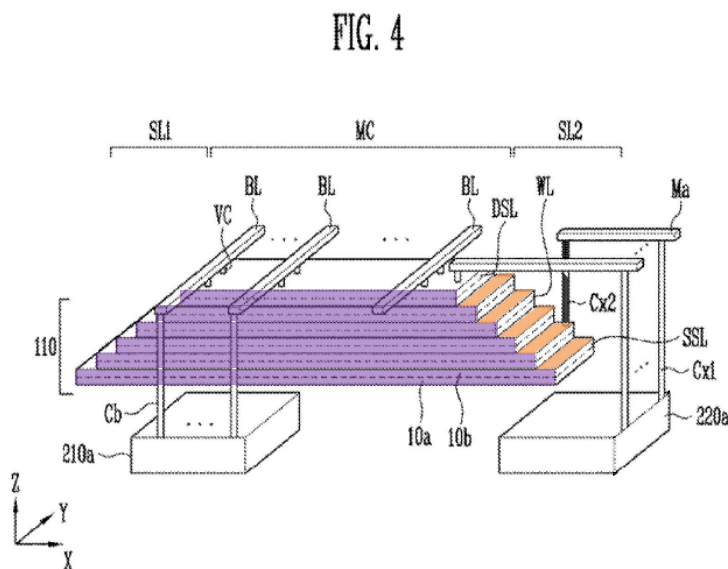


FIG. AS –FIG. 6 of EX1004 (annotated)

201. Further, with reference to FIG. 12, Lee further discloses that contact plugs 41 are formed on the word lines WL. EX1004, [0082]. With reference to FIG. 13, Lee also discloses contact plugs 52 are formed on the word lines WL, respectively. EX1004, [0087]. As shown in the enlarged views of FIGs. 12 and 13, each contact plug 41 or 52 is formed on the only exposed end of a respective word line WL of a respective layer pair.

C. Dependent Claim 5: The microelectronic device of claim 1, wherein the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region.

202. Lee discloses “*wherein the at least one stair step region comprises two stair step regions at opposing ends of the at least one memory block, each of the two stair step regions located remote from the memory cell region.*”

203. Specifically, Lee discloses “first and second slimming regions SL1 and SL2 are defined at both ends of the memory blocks,” and “[t]he first slimming region SL1 is defined at one end of the memory region MC and the second slimming region SL2 is defined at the other end of the memory region MC.” EX1004, [0034]. For example, with reference to FIG. AS shown above, memory cell array 100 has memory region MC in the middle and first and second slimming regions SL1 and SL2 at its two opposite ends in the X-direction. EX1004, [0034].

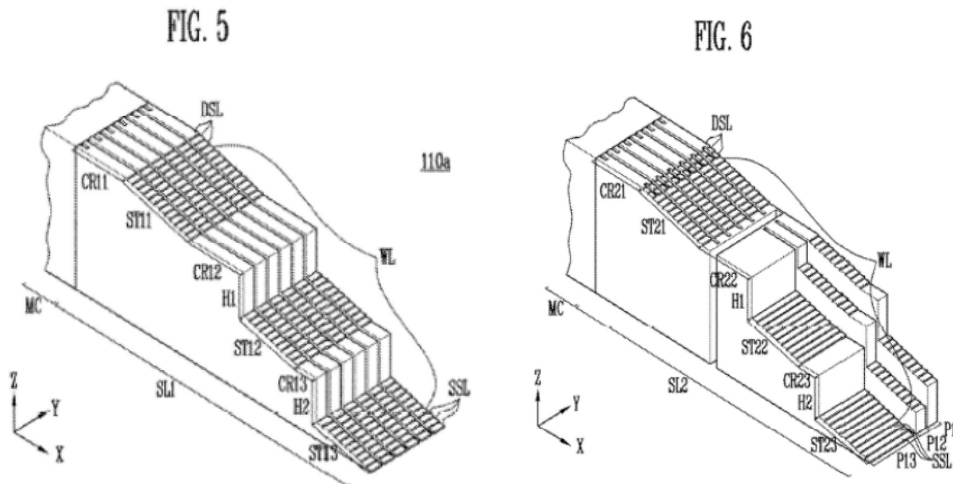


FIG. AV –FIGs. 5 and 6 of EX1004

204. FIG. AV shown above includes (i) FIG. 5 of Lee illustrating first slimming region SL1 and (ii) FIG. 6 of Lee illustrating second slimming region SL2. EX1004, [0018], [0019]. Referring to FIG. 5, Lee further discloses “the first slimming region SL1 may include an 11th contact region CR11 and an 11th step region ST11, a 12th contact region CR12 and a 12th step region ST12, and a 13th contact region CR13 and a 13th step region ST13.” EX1004, [0051]. That is, Lee discloses step regions ST11, ST12, and ST13 in first slimming region SL1. Further, as discussed in Section IX.A([1.a.2]) and also referring to FIG. 6, Lee discloses step regions ST21, ST22, and ST23 in second slimming region SL2.

205. As a result, Lee discloses step regions ST11, ST12, and ST13 of first slimming region SL1 and step regions ST21, ST22, and ST23 of second slimming region SL2 at two opposing ends of memory cell array 100.

206. Further, as explained in Section IX.A([1.a.3]) and also referring to FIG.

6, Lee discloses contact region CR21 between memory region MC and step regions ST21, ST22, and ST23 in the X-direction. For example, step regions ST21, ST22, and ST23 are separated from memory region MC by contact region CR21. Similarly, referring to FIG. 5, another contact region CR11 is located between memory region MC and step regions ST11, ST12, and ST13 in the X-direction. EX1004, [0051]. That is, step regions ST11, ST12, and ST13 are separated from memory region MC by contact region CR11. Thus, each of step regions ST21, ST22, and ST23 and step regions ST11, ST12, and ST13 are located remotely from memory region MC by contact region CR21 or CR11.

D. Independent Claim 7

207. Claim 7 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[7.P] A method of forming a microelectronic device, the method comprising:

[7.a] forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region;

[7.b] forming an array of memory cells in the memory cell region;

[7.c] forming stair step structures in the stair step region;

[7.d] forming conductive vias in the via region;

[7.e] forming access lines extending through the memory block;

[7.f] forming slots extending between adjacent portions of individual access lines within the stair step region; and

[7.g] forming a dielectric material within the slots.

[7.P] A method of forming a microelectronic device

208. Lee discloses a method for manufacturing a semiconductor device 1000 having slimming regions SL1 and SL2. EX1004, [0028], [0064]-[0065].

[7.a] forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region

209. Lee discloses or at least suggests “forming a memory block operatively coupled to sub-array circuitry, the memory block comprising a memory cell region, a stair step region, and a via region at least partially between the memory cell region and the stair step region.”

210. As I explained above with respect to claim limitation [1.a], Lee discloses memory blocks 110 in a memory cell array 100 operatively coupled to row decoder 220a. As I also explained above with respect to claim limitations [1.a.1], [1.a.2], and [1.a.3], Lee discloses memory cell array 100 includes (i) memory region MC, (ii) step regions ST21, ST22, and ST23, and (iii) contact region CR21 between memory region MC and step regions ST21, ST22, and ST23. I incorporate my discussion for claim limitations [1.a] and [1.a.1]-[1.a.3].

211. Lee specifically discloses “a method of forming the first slimming region and the second slimming region,” which include step regions (e.g., ST21, ST22, and ST23) and contact regions (e.g., CR21). EX1004, [0065], FIGs. 7-10.

212. Although Lee does not explicitly describe the method of forming memory region MC, it does teach the formation of step regions and contact regions, both of which are part of the same memory cell array 100 as memory region MC. Accordingly, a POSITA would have understood that memory region MC is also formed as part of memory cell array 100 during the formation of step regions and contact regions. Moreover, claim limitation **[7.a]** does not require any particular manufacturing processes; it simply requires the formation of a memory block in general, which is a well-established practice in the art. For example, Lee discloses “memory blocks may be **formed** in a two-dimensional or three-dimensional structure.” EX1004, [0005]. The presence of memory blocks 110 in memory cell array 100 itself discloses, or at the very least suggests, the process for forming them.

[7.b] forming an array of memory cells in the memory cell region

213. Lee discloses, or at least suggests, “forming an array of memory cells in the memory cell region.”

214. Specifically, Lee discloses that “memory cell array 100 may include a plurality of memory blocks 110” and “[t]he region in which the memory blocks 110[] are **formed** is defined as a memory region MC.” EX1004, [0031], [0034].

215. Moreover, claim limitation [7.b] does not require any particular manufacturing processes; it simply requires the formation of an array of memory cells in general, which is a well-established practice in the art. For example, Lee discloses “memory blocks may be **formed** in a two-dimensional or three-dimensional structure ... the memory blocks of the three-dimensional structure include memory cells stacked in a vertical direction to a substrate.” EX1004, [0005]. The presence of memory cells in memory cell array 100 itself discloses, or at the very least suggests, the process for forming them. See Section IX.A([1.a.1]).

[7.c] forming stair step structures in the stair step region;

216. Lee discloses “forming stair step structures in the stair step region.”

217. As I explained above with respect to claim limitation [1.a.2], Lee discloses “stair step structures in the stair step region.” I incorporate my discussion for claim limitation [1.a.2]. Moreover, Lee specifically discloses “FIGS. 7 and 10 are perspective views for illustrating a method of forming the first slimming region and the second slimming region,” which include the step regions. EX1004, [0065], FIGs. 7-10. Specifically, Lee discloses “a slimming process of etching gate lines extended from the memory region MC to the first slimming region SL1 and the second slimming region SL2, respectively, in a step form or a pad form, is performed.” EX1004, [0066], see also [0067]-[0074].

[7.d] forming conductive vias in the via region

218. Lee discloses, or at least suggests, “forming conductive vias in the via region.”

219. As I explained above with respect to claim limitation [1.a.3], Lee discloses contact plugs 32 in contact region CR21. I incorporate my discussion for claim limitation [1.a.3].

220. Lee specifically discloses that “[f]irst contact plugs 32 positioned vertically that is, in a [Z]-direction passing through the first blocking layers 31 are **formed**,” “first blocking layers 31 may be **formed** of an insulating material such as an oxidization layer,” and “first and second contact plugs 32 and 34 and the first wires are **formed** of conductive layers.” EX1004, [0077], [0079].

221. Moreover, claim limitation [7.d] does not require any particular manufacturing processes; it simply requires the formation of conductive vias in general, which is a well-established practice in the art. The presence of contact plugs 32 in blocking layer 31 itself, along with the usages of the term “formed,” discloses, or at the very least suggests, the process for forming them. See Section IX.A([1.a.3]).

[7.e] forming access lines extending through the memory block

222. Lee discloses, or at least suggests, “forming access lines extending through the memory block.”

223. As I explained above with respect to claim limitation [1.a.4], Lee

discloses conductive layers 10b, which form gate lines (e.g., source select lines SSL, word lines WL, and drain select lines DSL) extending across memory region MC into slimming regions SL1 and SL2 in the X-direction. I incorporate my discussion for claim limitation [1.a.4].

224. Lee specifically discloses that “source select lines SSL, the word lines WL, and the drain select lines DSL may be **formed** of conductive layers 10b,” and “in the first slimming region SL1 and the second slimming region SL2, the drain select lines DSL and some word lines WL are **formed** in the 11th step region ST11 and the 21st step region ST21.” EX1004, [0046], [0066]. Lee further discloses forming word lines in step regions ST12, ST22, ST13, and ST23. EX1004, [0067], [0068].

225. Moreover, claim limitation [7.e] does not require any particular manufacturing processes; it simply requires the formation of access lines in general, which is a well-established practice in the art. The presence of conductive layers 10b itself, along with the usages of the term “formed,” discloses, or at the very least suggests, the process for forming them. See Section IX.A([1.a.4]).

[7.f] forming slots extending between adjacent portions of individual access lines within the stair step region

226. Lee discloses, or at least suggests, “forming slots extending between adjacent portions of individual access lines within the stair step region.”

227. As I explained above with respect to claim limitation **[1.a.5]**, Lee discloses or at least suggests slots extending between adjacent gate lines within the step region. I incorporate my discussion for claim limitation **[1.a.5]**.

228. Claim limitation **[7.f]** does not require any particular manufacturing processes; it simply requires the formation of slots in general, which is a well-established practice in the art. The presence of slots itself discloses, or at the very least suggests, the process for forming them. See Section IX.A([1.a.5]).

[7.g] forming a dielectric material within the slots.

229. Lee discloses, or at least suggests, “forming a dielectric material within the slots.”

230. As I explained above with respect to claim limitation **[1.a.5]**, Lee discloses or at least suggests a dielectric material within the slots. I incorporate my discussion for claim limitation **[1.a.5]**.

231. Claim limitation **[7.g]** does not require any particular manufacturing processes; it simply requires the formation of a dielectric material in general, which is a well-established practice in the art. The presence of the dielectric material itself discloses, or at the very least suggests, the process for forming it. See Section IX.A([1.a.5]).

E. Dependent Claim 9: The method of claim 7, wherein forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.

232. Lee discloses or at least suggests “wherein forming the conductive vias comprises forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.”

233. Lee discloses “[f]irst contact plugs 32 positioned vertically that is, in a [Z]-direction passing through the first blocking layers 31 are **formed**,” and “first contact plugs 32 are connected to the first row decoder 220a located at the lower portion of the memory block.” EX1004, [0077], [0078]. As further shown in FIG. AI below (the enlarged view of FIG. 11 of Lee), the two contact plugs 32 (in black) are formed substantially vertically aligned over row decoder 220a (in yellow).

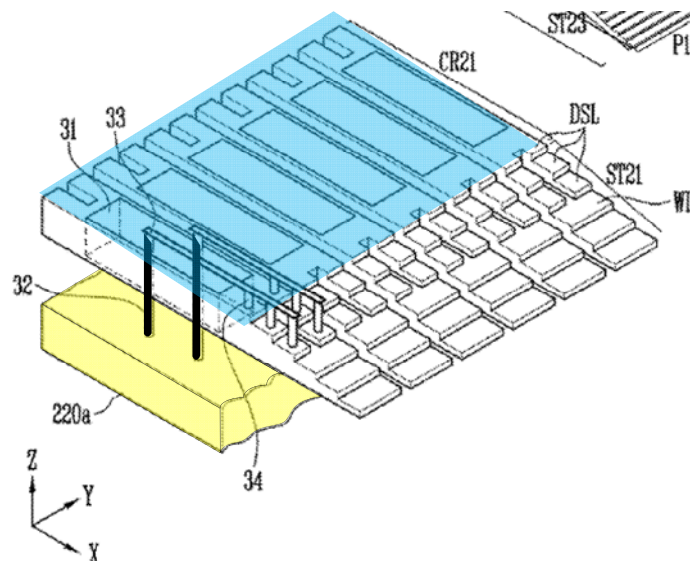


FIG. AI –Bottom portion of FIG. 11 of EX1004 (annotated)

234. Thus, a POSITA would have understood, or at least found it obvious, forming contact plugs 32 to be vertically aligned over row decoder 220a. See Section IX.D([7.d]).

F. Dependent Claim 11: The method of claim 7, wherein forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots.

235. Lee discloses, or at least suggests, “wherein forming the slots comprises forming an additional slot extending between the adjacent portions of the individual access lines without intersecting any other slot of the slots.”

236. At the outset, when describing the formation of slots 114 with reference to FIGs. 9A and 9B, the '974 Patent describes (i) “slots 114 may be formed by anisotropically removing portions of the first dielectric material 132 and second dielectric material 134,” (ii) “slots 114 may be formed to be separated from adjacent slots 114 by a first distance D1 in the memory array region 102,” and (iii) “at least some of the slots 114 in the stair step region 104 and the via region 106 may be separated by a second distance D2 greater than the first distance D1.” EX1001, 11:31-38, FIGs. 9A-9B. The '974 Patent, as well as the plain and ordinary meaning of claim 11, does not require forming some slots before or after any other slots (e.g., not requiring forming the additional slot before or after any other slot).

237. As I discussed above with respect to claim limitation [7.f], Lee

discloses or at least suggests “forming slots extending between adjacent portions of individual access lines.” In a first example, as shown in FIG. AW below (which includes annotated FIG. 6 of Lee), a POSITA would have understood, or at least found it obvious, that Lee forms an additional slot (in dark blue) in the middle and other slots (in dark green) extending in the X-direction between the adjacent gate lines in parallel.

FIG. 6

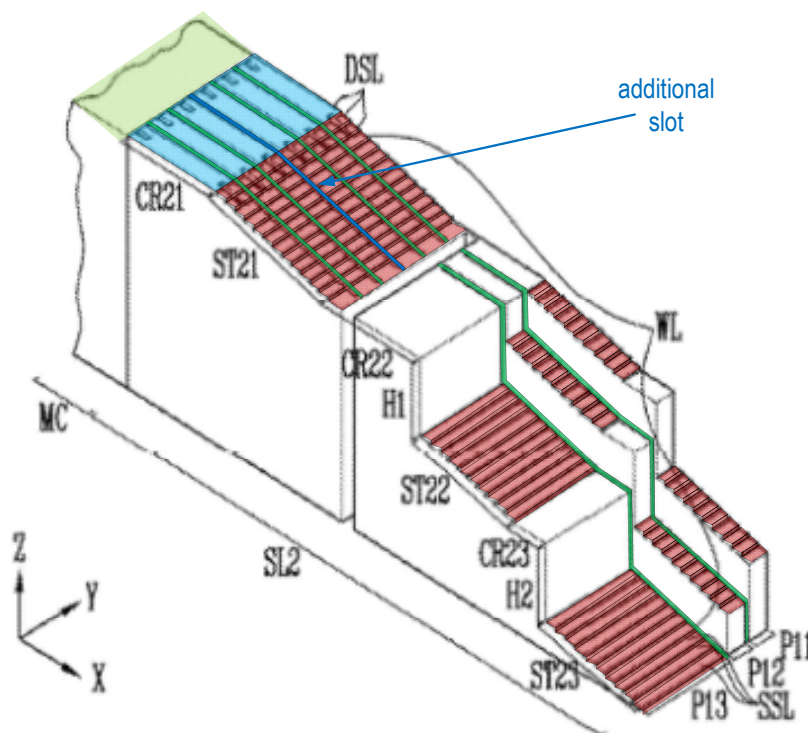


FIG. AW –FIG. 6 of EX1004

238. In a second example depicted in FIG. AX below (which includes the annotated enlarged portion of FIG. 11), a POSITA would have understood, or at least

found it obvious, that Lee also forms an additional slot (in dark blue) extending in the Z-direction through only conductive layers 10b forming drain select lines DSL and extending in the X-direction only in part of step region ST21 between the adjacent drain select lines DSL portions (in yellow) without intersecting the existing slots (in dark green).

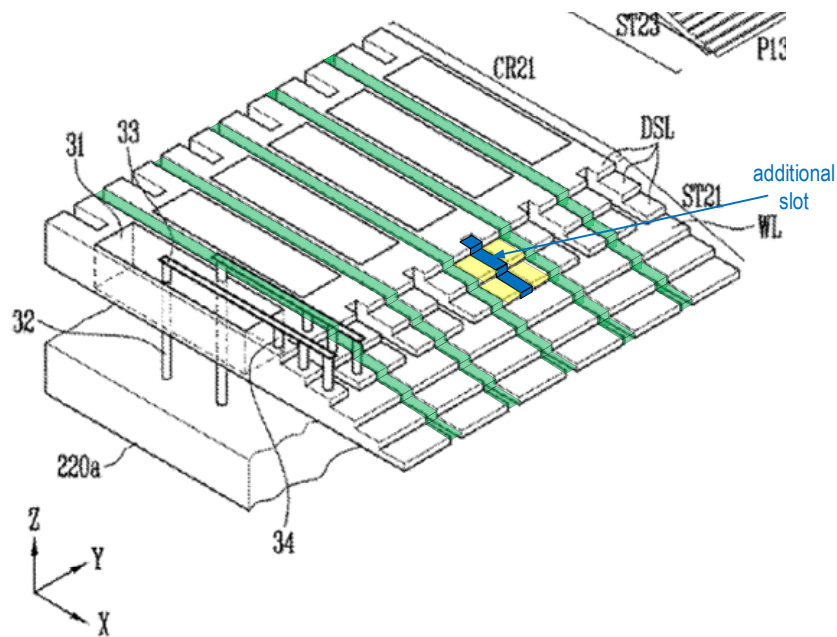


FIG. AX –FIG. 6 of EX1004 (annotated)

G. Dependent Claim 12: The method of claim 7, wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.

239. Lee discloses, or at least suggests, “wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.”

240. As I discussed above with respect to claim limitation [1.a.2] and further

shown in FIG. AF below, Lee discloses second slimming region SL2 having multiple stepped structures (in red), including the three adjacent stepped structures in the Y-direction in each of step regions ST22 and ST23 overlapping pad regions P11, P12, and P13, which have different heights in the Z-direction.

FIG. 6

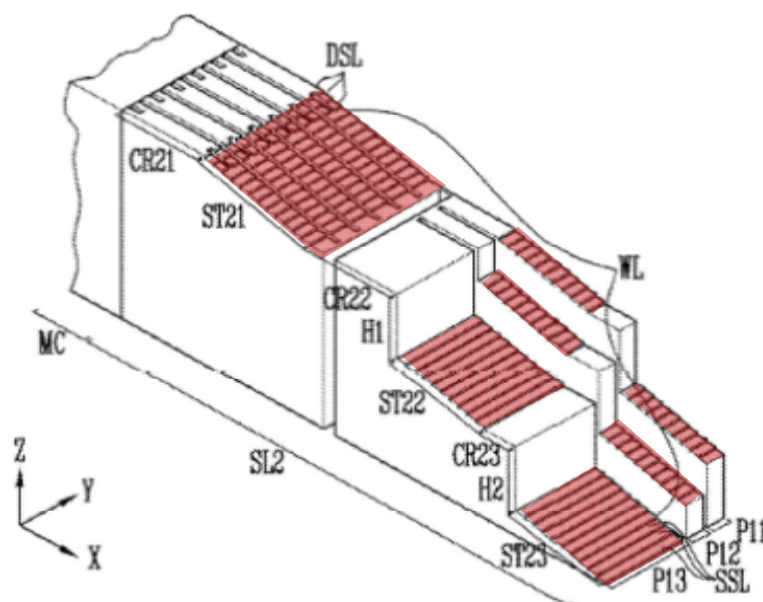


FIG. AF –FIG. 6 of EX1004 (annotated)

241. Lee specifically discloses the “method of manufacturing the first and second slimming regions SL1 and SL2 shown in FIGS. 5 and 6” in FIGS. 7-10. EX1004, [0020], [0064]. Regarding this method, Lee discloses “a slimming process of **etching** gate lines ... in a step form or a pad form” and “[b]y the aforementioned **etching** process, all of the drain select lines DSL, the word lines WL, and the source select lines SSL may be exposed.” EX1004, [0066], [0074], *see also* [0067]-[0073].

Thus, Lee discloses “removing at least a portion of the stair step structures.”

242. Specifically, Lee discloses a progression with respect to FIGs. 7-9, indicating, or at least suggesting, the usage of “a single stair step mask and two chop masks” in its “slimming process of etching gate lines” to form its stepped structures in slimming region SL2.

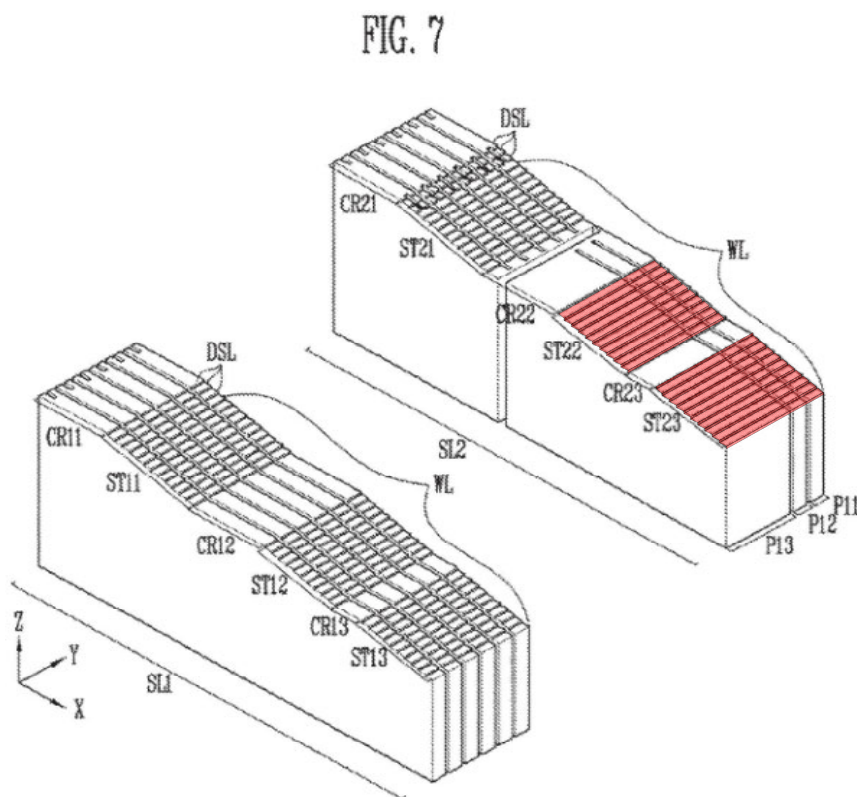


FIG. AZ –FIG. 7 of EX1004 (annotated)

243. First, referring to FIG. 7, gate lines are formed “in a step form” in step regions ST22 and ST23 by etching the gate lines therein. EX1004, [0067], [0068]. From FIG. AZ above, which includes annotated FIG. 7 of Lee, a POSITA would have understood, or at least found it obvious, that the etching process to form the

gate lines in the step regions ST22 and ST23 in the current **step form** (in red) uses a single stair step mask.

244. Second, referring to FIG. 8, Lee discloses “heights of the lines are decreased by etching the word lines included in the regions in which the 22nd step region ST22, ... and the 23rd step region ST23 of the second slimming region SL2 overlap the 12th pad region P12 and the 13th pad region P13.” EX1004, [0069].

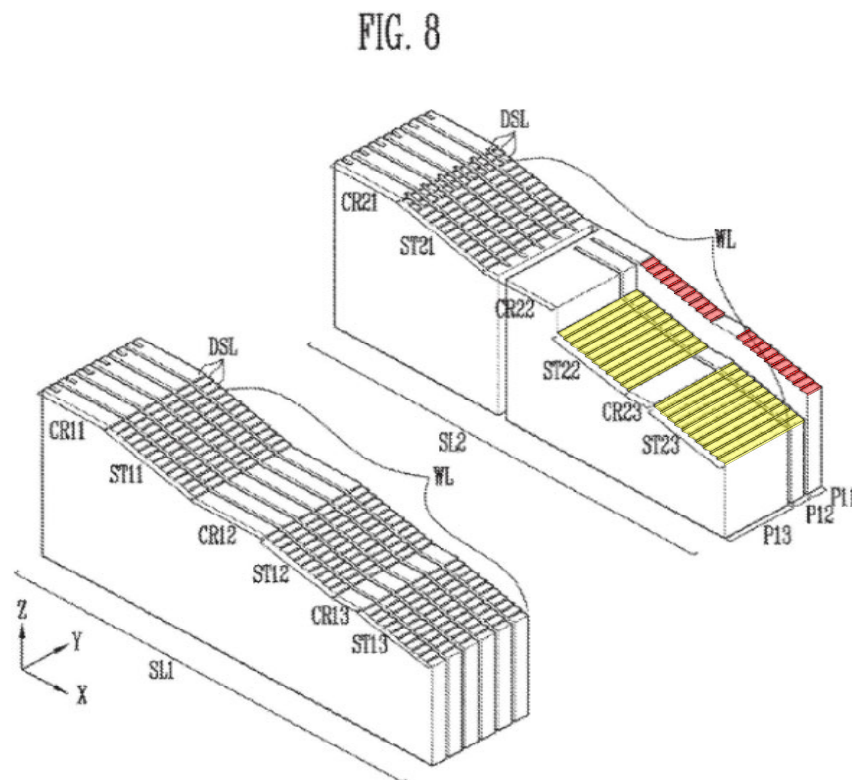


FIG. BA –FIG. 8 of EX1004 (annotated)

245. As shown in FIG. BA above (which includes annotated FIG. 8 of Lee), the gate lines in the area overlapping pad regions P12 and P13 (in yellow) are “chopped off” to become lower than the other area overlapping pad region P11 (in

red). Thus, a POSITA would have understood, or at least found it obvious, that the etching process applied to the gate lines in step regions ST22 and ST23 in the current **pad form** uses a first chop mask that covers pad region P11, such that the etching applies to pad regions P12 and P13 but not pad region P11.

246. Third, referring to FIG. 9, Lee discloses “a height of the region is decreased by etching the word lines WL [i]ncluded in the regions, in which the 22nd step region ST22, ... and the 23rd step region ST23 of the second slimming region SL2 overlap the 13th pad region P13.” EX1004, [0072]. As shown in FIG. BB below, which includes annotated FIG. 9 of Lee, the gate lines in the area overlapping pad region P13 (in blue) are “chopped off” again to become lower than the other area overlapping pad region P12 (in yellow). Thus, a POSITA would have understood, or at least found it obvious, that the etching process applied to the gate lines in step regions ST22 and ST23 in the current **pad form** uses a second chop mask that covers pad regions P11 and P12, such that the etching applies to pad region P13 but not pad regions P11 and P12.

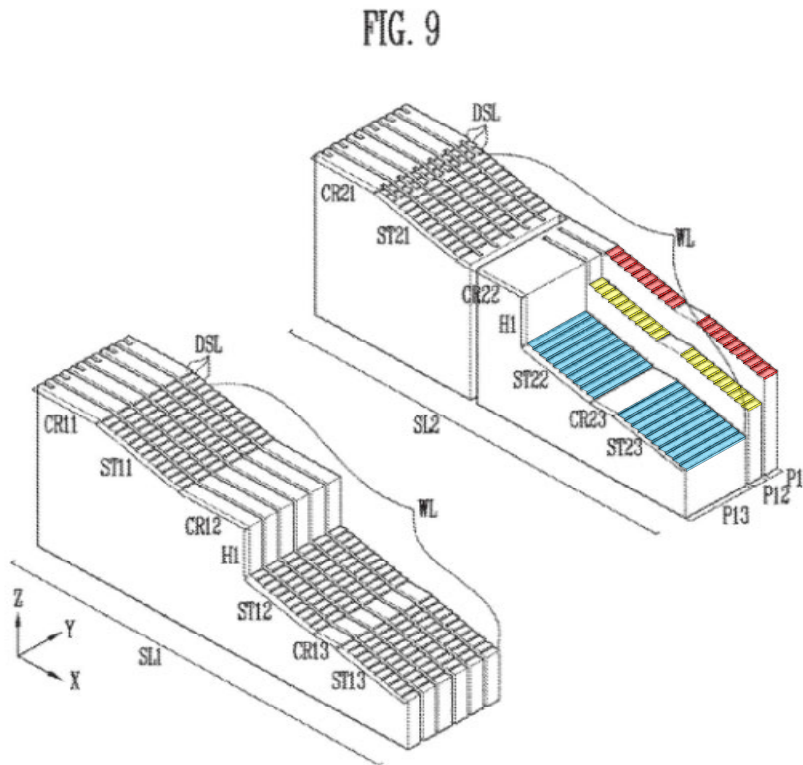


FIG. BB –FIG. 8 of EX1004 (annotated)

247. Even the '974 patent itself admits that the use of a stair step mask in combination with chop masks to create such stepped structures is “known by those of ordinary skill in the art” (AAPA-2), and further provides details of how to use the step mask and chop masks in forming stair step structures. EX1001, 9:30-10:12, 12:37-39. See Section VII.A.2. AAPA-2, as evidence of common knowledge of a POSITA, strongly supports that a POSITA would have understood Lee discloses, or at least suggests, the usage of a stair step mask and chop masks in forming its stepped structures. See Section VI.D.2.

H. Dependent Claim 13

248. Claim 13 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[13.P] The method of claim 7, wherein:

[13.a] forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials; and

[13.b] forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

[13.P] The method of claim 7

249. Lee discloses or at least renders obvious the method of claim 7. I incorporate my discussion for claim 7.

[13.a] forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials

250. Lee discloses or at least suggests “forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials.”

251. I noted that claim limitation [13.a] requires nothing more than what has been characterized as “**conventional**” in AAPA-1. EX1001, 1:43-59. This is also well known in the art as part of the conventional gate replacement process. See

Section VI.C, e.g., FIG. C(a).

252. Lee discloses (i) “the vertical channel layers VC may include circular channel layers and memory layers surrounding the channel layers,” (ii) “[t]he channel layers may be formed of a doped polysilicon layer,” and (iii) “[t]he memory layers may include gate insulating layers surrounding the channel layers, charge trap layers surrounding the gate insulating layers, and blocking layers surrounding the charge trapping layers.” EX1004, [0038]. Lee also discloses vertical channel layers VC “extend in a Z-direction.” EX1004, [0037]. A POSITA would have understood that vertical channel layers VC are the claimed “vertical memory cell pillars,” consistent with the ’974 Patent—“[e]ach of the memory cell pillars 108 may include a central region 110 of a semiconductor material, such as a polysilicon or silicon-germanium material, at least partially surrounded by a charge trapping material 112, such as an oxide-nitride-oxide (“ONO”) material.” EX1001, 4:32-37.

253. Lee further explains that the source select lines SSL, the word lines WL, and the drain select lines “surround the vertical channel layers VC” in memory region MC. EX1004, [0039]-[0041], [0045], FIG. 3. Lee also discloses that the source select lines SSL, the word lines WL, and the drain select lines DSL are formed of conductive layers 10b from a stack of alternating insulating layers 10a and conductive layers 10b. EX1004, [0046], FIG. 4. Thus, a POSITA would have understood that vertical channel layers VC are surrounded by conductive layers 10b

from a stack of alternating insulating layers 10a and conductive layers 10b.

254. To the extent Lee does not explicitly disclose forming vertical channel layers VC within a stack of alternating dielectric materials, Lee, at a minimum, suggests it because it is well-known in the art that Lee's stack of alternating insulating layers 10a and conductive layers 10b (collectively referred to herein as "a stack of alternating dielectric/conductive materials") is formed by the well-known gate replacement process—first forming vertical channel layers VC within a stack of alternating dielectric materials (including insulating layers 10a and sacrificial layers having a different dielectric material than insulating layers 10a), followed by replacing the sacrificial layers with conductive layers 10b—resulting in the stack of alternating dielectric/conductive materials, as evidenced by AAPA-1 and state of the art before the '974 Patent. EX1001, 1:49-59; see Section VI.C.

[13.b] forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials

255. Lee discloses or at least suggests "forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials."

256. At the outset, the '974 Patent describes "[a]lthough the formation of the conductive vias 120 has been explained and illustrated as occurring subsequent to the formation of the conductive word lines 116 and the filling of the slots 114 with

a dielectric material, **the present disclosure is not so limited**. For example, the conductive vias 120 may be formed **prior to, during, or after** the formation of the conductive word lines 116 and the filling of the slots 114 with a dielectric material.” EX1001, 12:46-53.

257. A POSITA would have understood that the description of the '974 Patent, as well as the plain and ordinary meaning of claim limitation **[13.b]**, does not specify the timing of “forming the conductive vias in the via region” or “isolating the conductive vias” much less with respect to the timing of forming “the stack of alternating dielectric materials.”

258. Thus, under the plain and ordinary meaning of claim limitation **[13.b]**, Lee discloses or at least suggests claim limitation **[13.b]** because Lee also discloses, or at least suggests, contact plugs 32 are formed in contact region CR21, extending into the stack of alternating dielectric/conductive materials, which has alternating dielectric materials before the gate replacement process, as explained above with respect to claim limitations **[1.a.3]** and **[13.a]**. It is clear to me that contact plugs 32 are isolated from the stack of alternating dielectric/conductive materials by first block layer 31 before the gate replacement process. EX1004, [0077].

I. Independent Claim 14

259. Claim 14 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[14.P] A method of forming a microelectronic device, the method comprising:

[14.a] forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials;

[14.b] forming access lines coupled to memory cells of the array of memory cells;

[14.c] forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;

[14.d] forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and

[14.e] removing at least a portion of the stair step structures using at least one chop mask.

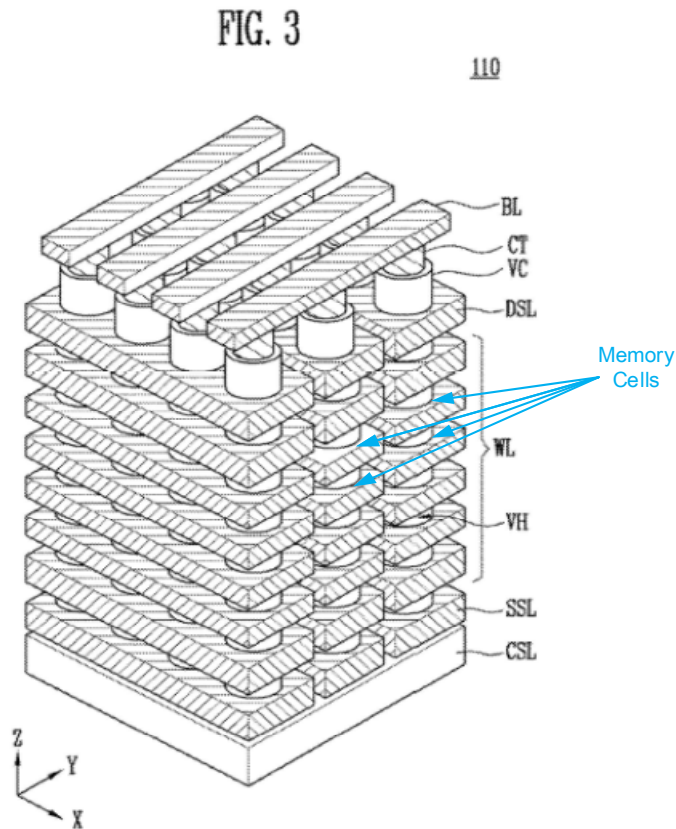
[14.P] A method of forming a microelectronic device, the method comprising

260. I incorporate the discussion provided above with respect to claim limitation [7.P], Lee discloses or at least renders obvious claim limitation [14.P].

[14.a] forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials

261. As explained above with respect to claim limitation [7.b], Lee discloses or at least suggests “*forming an array of memory cells.*” For example, as illustrated in FIG. AE shown below, an array of memory cells, each at a respective junction between word lines WL and vertical channel layers VC, are formed in memory

region MC.



262. Further, as explained above with reference to claim limitation **[13.a]**, Lee discloses vertical channel layers VC within a stack of alternating insulating layers 10a and conductive layers 10b. EX1004, [0039]-[0041], [0046] Thus, Lee also discloses, or at least suggests, that the memory cells are formed within a stack of alternating insulating layers 10a and conductive layers 10b. From FIG. BC shown below, which includes annotated FIG. 4 of Lee, a POSITA would have understood, or at least found it obvious, that memory cells in memory region MC (e.g., shown in FIG. AE above) are formed in a stack of alternating insulating layers 10a (in brown)

and conductive layers 10b (in gray).

FIG. 4

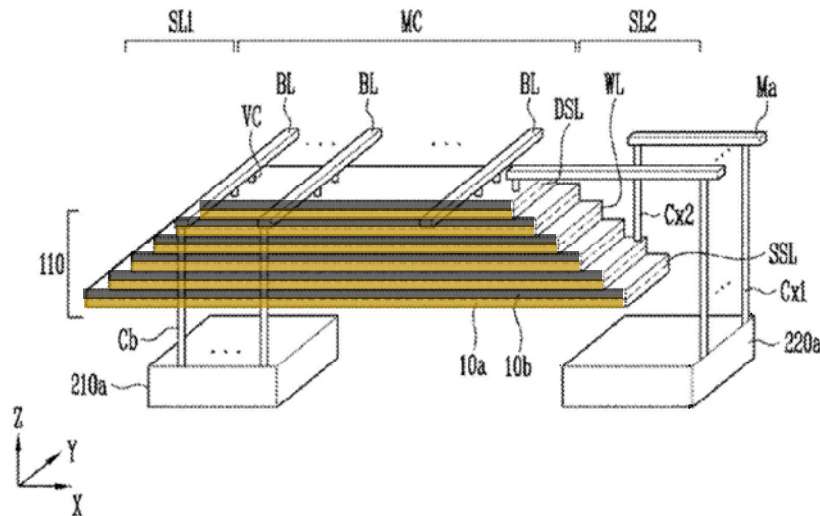


FIG. 5

FIG. BC –FIG. 4 of EX1004 (annotated)

[14.b] forming access lines coupled to memory cells of the array of memory cells

263. Lee discloses or at least suggests “forming access lines coupled to memory cells of the array of memory cells.”

264. As I explained above with respect to claim limitation [7.e], Lee discloses or at least suggests “forming access lines extending through the memory block.” As illustrated in FIG. AE shown above, each memory cell is formed at a respective junction between word lines WL and vertical channel layers VC. Further, Lee discloses “[t]he row decoder may transmit the operation voltages to source lines,

word lines, and drain select lines connected to a selected memory block.” EX1004, [0008], *see also* [0047]. Thus, a POSITA would have understood or found it obvious that conductive layers 10b forming the word lines WL are formed “coupled to memory cells of the array of memory cells” in order to “transmit operation voltages” to the memory cells in the selected memory block through word lines WL.

***[14.c] forming conductive vias adjacent the array of memory cells,
the conductive vias formed adjacent sub-array circuitry underlying
the stack***

265. Lee discloses or at least suggests “forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack.”

266. As I explained above with reference to claim limitation [7.d] and claim 9, Lee discloses or at least suggests “forming conductive vias in the via region” and “forming at least some of the conductive vias to be substantially vertically aligned over portions of the sub-array circuitry.”

267. The plain and ordinary meaning of the claim term “adjacent” includes “not distant.” EX1012, 1a. Specifically, Lee discloses forming contact plugs 32 in contact region CR21, which is next to, i.e., “not distant,” memory region MC in which the array of memory cells is formed. EX1004, FIG, 6. A POSITA would have understood or at least found it obvious that contact plugs 32 in contact region CR21 are formed “adjacent the array of memory cells” in memory region MC.

268. The plain and ordinary meaning of the claim term “adjacent” also includes “having a common endpoint or border.” EX1012, 1b. Since “first contact plugs 32 are **connected to** the first row decoder 220a located at the lower portion of the memory block,” first contact plugs 32 and first row decoder 220a are “adjacent” in that they share “a common endpoint or border” where they are connected. EX1004, [0078], FIG. 11. Thus, first contact plugs 32 are formed “adjacent sub-array circuitry underlying the stack.”

[14.d] forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines

269. Lee discloses or at least suggests “forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines.”

270. As I explained above with respect to claim limitation [7.c], claim 12, and claim limitation [4.b], Lee discloses or at least suggests “forming stair step structures in the stair step region,” “removing at least a portion of the stair step structures using a single stair step mask and two chop masks,” and “contact regions on the individual tiers, each tier comprising a single contact region operatively connected to a respective access line portion of the individual access lines.”

271. Specifically, Lee discloses that “**steps** may be generated between two neighboring contact regions,” i.e., the stepped structures in step regions ST21, ST22,

and ST23 in slimming region SL2. EX1004, [0055]. Lee further discloses contact plugs are formed on “the lines SSL, WL, and DSL **exposed in a step structure** in the second slimming region SL2.” EX1004, [0045], [0047]. Thus, Lee discloses the exposed ends of conductive layers 10b on which contact plugs (e.g., contact plugs Cx2) are formed.

[14.e] removing at least a portion of the stair step structures using at least one chop mask

272. Lee discloses or at least suggests “removing at least a portion of the stair step structures using at least one chop mask.”

273. As I explained above with respect to claim 12, Lee discloses or at least suggests “removing at least a portion of the stair step structures using a single stair step mask and two chop masks.” I incorporate my discussion here.

J. Dependent Claim 15: The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.

274. Lee discloses or at least suggests “removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.”

275. Specifically, claim 15 would have been known by a POSITA in AAPA-

2 as “provid[ing] contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover.” In view of the common knowledge evidenced by AAPA-2 and as further explained above with respect to claim 12, referring to FIGs. 7-9 of Lee, a POSITA would have understood, or at least found it obvious, that in each etching process using a chop mask to form the gate lines in a pad form, more gate lines are exposed in the newly “chopped” pad regions, thereby forming additional exposed ends in step regions ST22 and T23. EX1004, [0069], [0072], [0074]. Each etching process using a chop mask also results in the reduction of the area in the X-Y plane of the newly “chopped” stepped structures.

276. For example, as shown in FIG. BA above, when the gate lines in the area overlapping pad regions P12 and P13 (in yellow) are “chopped” to become lower than the other area overlapping pad region P11 (in red), word lines in the area overlapping pad regions P12 and P13 (in yellow) are “etched in a step form.” EX1004, [0069]-[0071]. As a result, additional exposed ends of the word lines are formed in the area where step regions ST22 and ST23 overlap with pad regions P12 and P13 (in yellow). With combined reference to FIG. BA and FIG. AZ shown above, by chopping the gate lines in the area overlapping pad regions P12 and P13 (in yellow) in FIG. BA, an X-Y-plane area of the newly “chopped” stepped structures overlapping pad regions P12 and P13 (in yellow) is reduced as shown in

FIG. BA, when compared with an X-Y-plane area of the stepped structures overlapping pad regions P11, P12, and P13 (in red) as shown in FIG. AZ. See Section IX.G.

277. In another example, as shown in FIG. BB above, when the gate lines in the area overlapping pad region P13 (in blue) are “chopped” again to become lower than the other area overlapping pad region P12 (in yellow), word lines in the area overlapping pad regions P12 and P13 (in blue) are exposed. EX1004, [0072]. As a result, additional exposed ends of the word lines (*“additional contact regions”*) are formed in the area where step regions ST22 and ST23 overlap pad region P13 (in blue). With combined reference to FIG. BA and FIG. BB shown above, by chopping the gate lines in the area overlapping pad region P13 (in blue) in FIG. BB, an X-Y-plane area of the newly “chopped” stepped structures overlapping pad region P13 (in blue) is reduced, as shown in FIG. BB, when compared with the X-Y-plane area of the stepped structures overlapping pad regions P12 and P13 (in yellow) as shown in FIG. BA. See Section IX.G.

K. Dependent Claim 16: The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.

278. Lee discloses or at least suggests “wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using

the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.”

279. Specifically, like claim 15, claim 16 would have been known by a POSITA in AAPA-2 as “provid[ing] contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover.” In view of the common knowledge evidenced by AAPA-2 and as further explained above with respect to claim 12, referring to FIGs. 7-8 of Lee, a POSITA would have understood, or at least found it obvious, that after the etching process using the single step mask to form the gate lines in a step form (FIG. 7), a second etching process using the first chop mask is performed to form the gate lines in a pad form (FIG. 8).

280. For example, with combined reference to FIG. BA and FIG. AZ shown above, when the gate lines in the area overlapping pad regions P12 and P13 (in yellow) shown in FIG. BA are “chopped off” to become lower than the other area overlapping pad region P11 (in red) shown in FIG. BA, a total number of (i) exposed ends of the word lines formed in the area overlapping pad regions P11 (in red) shown in FIG. BA and (ii) exposed ends of the word lines formed in the area overlapping pad regions P12 and P13 (in yellow) shown in FIG. BA is twice the number of exposed ends of the word lines formed in the area overlapping pad regions P11, P12, and P13 (in red), as shown in FIG. AZ. See Section IX.G.

281. Thus, as a result of the second etching process, the number of exposed

ends of the gate lines in step regions ST22 and ST23 is doubled, comparing FIG. BA with FIG. AZ. Or equivalently, the number of exposed ends of the gate lines in each step region ST22 or ST23 is doubled, comparing FIG. BA with FIG. AZ. See Section IX.G.

L. Dependent Claim 17

282. Claim 17 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[17.P] The method of claim 14, wherein forming the at least one stair step region comprises:

[17.a] forming the stair step mask over the stack while exposing a width of a first step;

[17.b] removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask;

[17.c] recessing an edge of the stair step mask to expose a width of a second step; and

[17.d] removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.

283. Lee discloses or otherwise renders obvious “forming the at least one stair step region comprises:” [7.P] “forming the stair step mask over the stack while exposing a width of a first step” [17.a], “removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask” [17.b],

recessing an edge of the stair step mask to expose a width of a second step” [17.c], and “removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask” [17.d].

284. Claim 17 requires nothing more than the well-known “trim-etch” process with a stair step mask used in forming stair step structures, which is also part of AAPA-2. Sections VI.D.2.a and VII.A.2. Specifically, claim limitation [17.a] would have been known by a POSITA in AAPA-2 as “[a] stair step mask may be formed over the vertical memory block while leaving one step-width (*e.g.*, a width of one contact region 524 measured in the longitudinal direction *y*) exposed”; claim limitation [17.b] would have been known by a POSITA in AAPA-2 as “[o]ne or more tiers of conductive material (*e.g.*, of the conductive word lines 516) exposed through the stair step mask may be removed”; claim limitation [17.c] would have been known by a POSITA in AAPA-2 as “[a]n edge of the stair step mask may be removed to recess the edge of the stair step mask and to expose another step-width, in addition to the original exposed step-width”; claim limitation [17.c] would have been known by a POSITA in AAPA-2 as “[a]nother cycle of material removal may be performed to remove another one or more tiers of conductive material exposed through the recessed stair step mask.”

285. I noted that Freeman (EX1005), one of Micron’s own patents that shares the same first inventor as the ’974 Patent but was published almost three years

prior to the earliest possible effective filing date of the '974 patent, in its Background section when describing FIGs. 1A-1D, which are labeled as **PRIOR ART** and “show one **conventional** method of creating a stair-step structure 10,” describes almost the identical trim-etch process using a stair-step mask 16 as AAPA-2. EX1005, [0004]-[0005], FIGs. 1A-1D.

286. For example, as shown below in FIG. BD, which includes FIGs. 1A-1D of EX1005, Freeman discloses: (i) “[a]s shown in FIG. 1A, ... [a] mask 16 (e.g., photoresist material) is formed over the topmost insulating material 14 and patterned to expose a portion of the insulating material 14a, the exposed portion having a width of one so-called “step” of the stair-step structure 10 to be formed;” (ii) as shown in FIG. 1B, “[t]he exposed insulating material 14a is removed by one dry etch process that stops on the conductive material 12a, and the exposed conductive material 12a is then removed by another dry etch process that stops on the insulating material 14b;” (iii) still with reference to FIG. 1B, “the mask 16 is reduced in size by removing a portion of the mask (also known as “trimming”), such as by isotropic etching, to expose another portion of the insulating material 14a;” and (iv) with reference to FIG. 1C, “[t]he process is repeated by ... including removing the exposed portions of the two insulating materials 14a and 14b and subsequently removing exposed portions of the two conductive materials 12a and 12b.” EX1005, [0004], [0005]. Freeman further discloses “[a]s shown in FIG. 1C, the successive

reduction in size of the mask 16 and the repeated dry etch processes are continued until the insulating material 14c and conductive material 12c is exposed, the mask 16 is removed, and a stair-step structure 10 remains.” EX1005, [0005]. Thus, it is clear to me that the trim-etch process using stair-step mask 16 described in Freeman is almost identical to that using the stair step mask as described in AAPA-2.

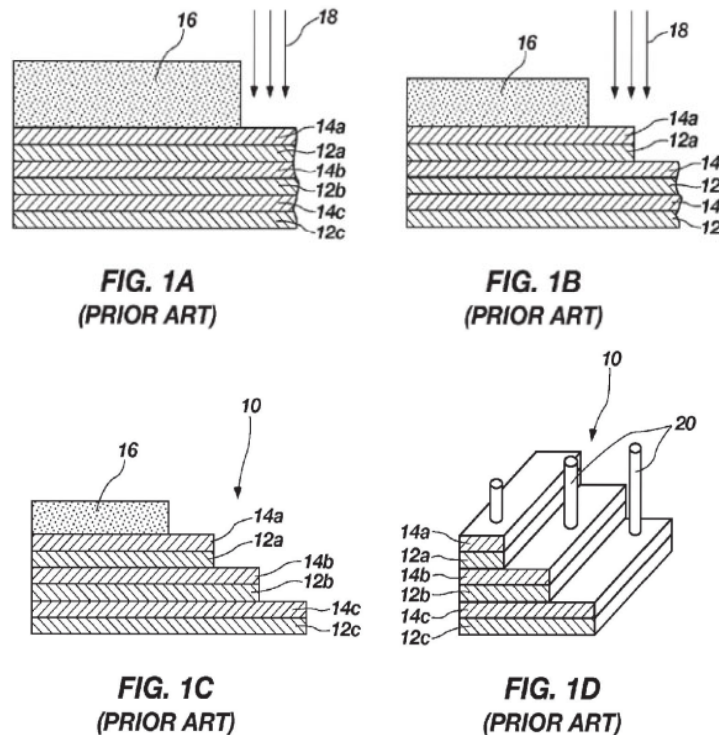


FIG. BD –FIGs. 1A-1D of EX1005

287. As I explained above with respect to claim limitation [14.d], Lee discloses or at least suggests “forming at least one stair step region comprising stair step structures using a stair step mask” by disclosing the process shown in FIG. 7. Thus, in view of the common knowledge in the art of using the trim-etch process and the stair step mask to form stair step structures, as evidenced by AAPA-2 and

Freeman, a POSITA would have understood that Lee discloses or at least suggests claim 17.

M. Dependent Claim 18

288. Claim 18 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[18.P] The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises:

[18.a] covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask; and

[18.b] vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed.

289. Lee discloses or at least suggests “[t]he method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises:” **[18.P]** “covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask” **[18.a]**, and “vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed” **[18.b]**.

290. Like claims 15 and 16, claim 18 requires nothing more than the well-

known “chopping” process for “provid[ing] contact to additional tiers of the vertical memory block while reducing the size of an area that the stair step structures cover,” which is part of AAPA-2. EX1001, 9:50-10:11. Claim limitation [18.a] would have been known by a POSITA in AAPA-2 as “[a] chop mask may be used cover one or more particular stair step structures or portions thereof ... while leaving one or more other stair step structures or portions thereof exposed through the chop mask.” Claim limitation [18.b] would have been known by a POSITA in AAPA-2 as “[t]he entire exposed one or more other stair step structures or portions thereof is vertically recessed, such that one or more exposed tiers is removed.”

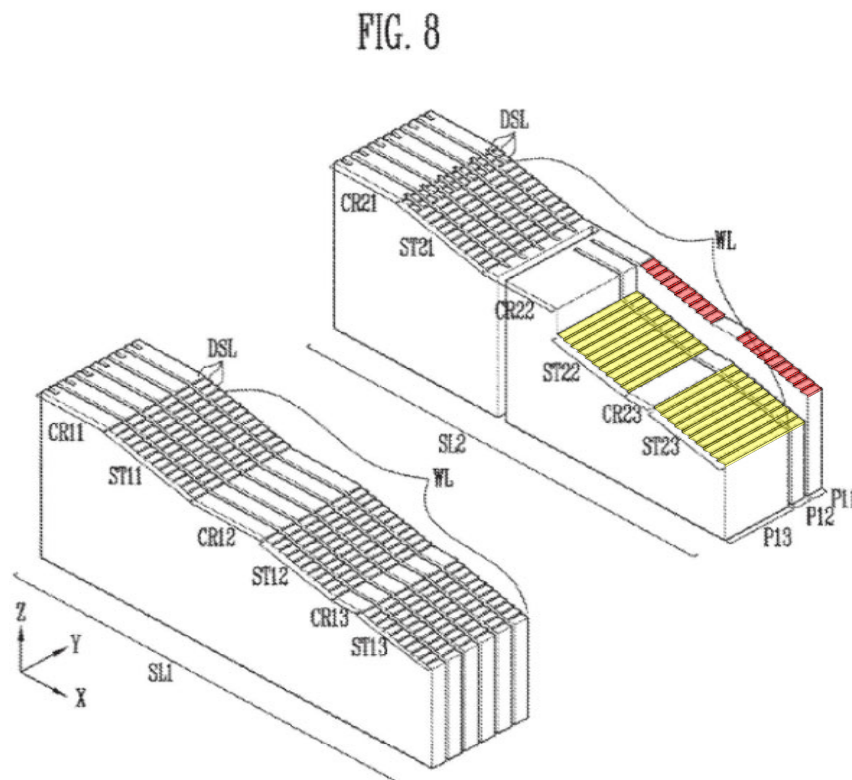


FIG. BA –FIG. 8 of EX1004 (annotated)

291. In view of the common knowledge evidenced by AAPA-2, and as further explained above with respect to claim [12], a POSITA would have understood, or at least found it obvious, that as shown in FIG. BA above, in the etching process using the first chop mask, the first areas of step regions ST22 and ST23 overlapping pad region P11 (in red) are covered by the first chop mask, while the second areas of step regions ST22 and ST23 overlapping pad regions P12 and 13 (in yellow) are exposed, such that only the second areas are etched (“chopped off”). See Section IX.G.

292. Similarly, in view of the common knowledge evidenced by AAPA-2, and as further explained above with respect to claim [12], a POSITA would have understood, or at least found it obvious, that as shown in FIG. BB above, in the etching process using the second chop mask, the third areas of step regions ST22 and ST23 overlapping pad regions P11 and P12 (in red and yellow) are covered by the second chop mask, while the fourth areas of step regions ST22 and ST23 overlapping pad region 13 (in blue) are exposed, such that only the fourth areas are etched (“chopped off”). See Section IX.G.

293. Further, as I discussed above with respect to claim limitation [4.a], a pair of conductive layer 10b (including gate lines) and insulating layer 10a is a claimed “tier.” Lee specifically discloses “[r]eferring to FIG. 8, heights of the lines are decreased by etching the word lines included in the regions in which the 22nd

step region ST22, ... and the 23rd step region ST23 of the second slimming region SL2 overlap the 12th pad region P12 and the 13th pad region P13.” EX1004, [0069]. That is, as shown in FIG. BA, in the etching process using the first chop mask, the second areas of step regions ST22 and ST23 overlapping pad regions P12 and 13 (in yellow) are etched (“chopped off”), such that at least a pair of conductive layer 10b (forming gate lines) and insulating layer 10a is removed. See Section IX.G.

294. Similarly, Lee also discloses “[r]eferring to FIG. 9, a height of the region is decreased by etching the word lines WL [i]ncluded in the regions, in which the 22nd step region ST22, ... and the 23rd step region ST23 of the second slimming region SL2 overlap the 13th pad region P13.” EX1004, [0072]. That is, as shown in FIG. BB, in the etching process using the second chop mask, the fourth areas of step regions ST22 and ST23 overlapping pad region 13 (in blue) are etched (“chopped off”), such that at least a pair of conductive layer 10b (forming gate lines) and insulating layer 10a is removed. See Section IX.G.

N. Dependent Claim 19: The method of claim 14, wherein forming the conductive vias comprises forming at least some of the conductive vias between the array of memory cells and the at least one stair step region.

295. Lee discloses or at least suggests “wherein forming the conductive vias comprises forming at least some of the conductive vias between the array of memory cells and the at least one stair step region.”

296. As I discussed above with respect to claim limitations [14.c] and [1.a.3], Lee discloses “forming conductive vias adjacent the array of memory cells” and “conductive vias in at least one via region at least partially located between the memory cell region and the at least one stair step region.” I incorporate my discussion about claim limitations [14.c] and [1.a.3].

X. Ground 3: Lee in View of Freeman Renders Obvious Claims 12 and 14-19

297. As I discussed above in Section IX, Lee discloses or otherwise renders obvious claims 12 and 14-19. To the extent further disclosures are required, Lee in view of Freeman renders these claims obvious in my opinion.

A. Reasons to Combine Lee and Freeman

298. As I discussed above in Section IX, Lee discloses, or at least suggests, the various claim limitations related to using “a stair step mask” (claim limitation [14.d] and claim 17) and “at least one chop mask” (claim limitation [14.e], claims 15, 16, and 18) in “forming at least one stair step region” (collectively “mask limitations”) in particular, in view of AAPA-2 and common knowledge of a POSITA.

299. Lee and Freeman provide complementary teachings regarding the mask limitations. While Lee does not explicitly use the terms “stair-step mask” or “chop mask,” it describes the formation of stepped structures in FIGs. 7-10. A POSITA,

considering these teachings alongside Freeman’s explicit disclosure of using “stair-step mask” and “chop mask” to form similar stair-step structures in FIGs. 2-14, would have understood—or at the very least, found it obvious—that Lee also employs stair-step and chop masks in its stepped structure formation method.

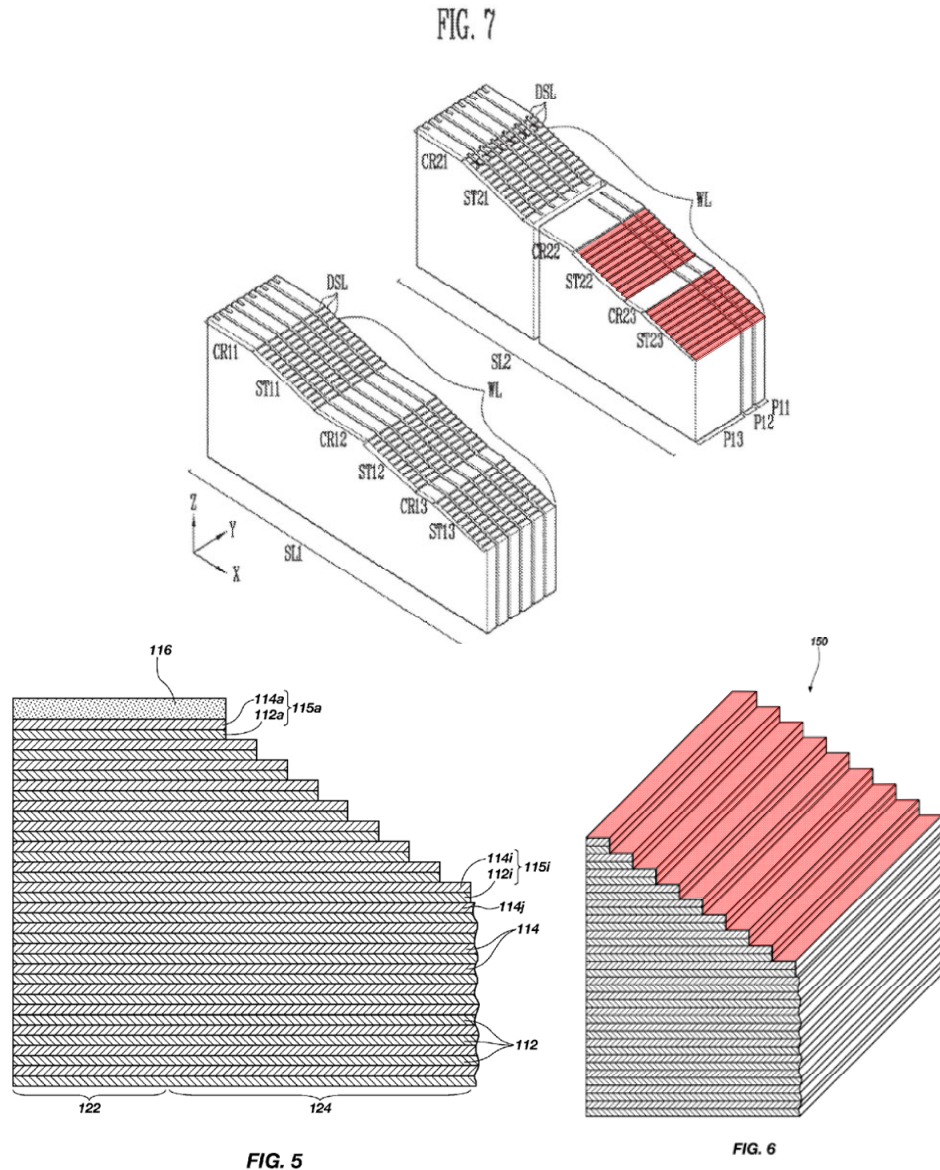


FIG. BE –Comparison of FIG. 7 of EX1004 with FIGs. 5 and 6 of EX1005 (annotated)

300. By comparing FIG. 7 of Lee (top) with FIGs. 5-6 of Freeman (bottom),
154

as shown in FIG. BE above, a POSITA would readily appreciate Lee's current stepped structures (in red) in step regions ST22 and ST23 in FIG. 7 are substantially the same as Freeman's intermediate stair-step structure 100 (in red) in FIG. 6. Thus, a POSITA would have found it obvious to combine Freeman's teachings of the process (as shown in FIG. 5), which would also form the same stepped structure of Lee, to supplement any missing details of Lee, including the usage of stair-step mask 116 because it is necessary to form intermediate stair-step structure 100 using stair-step mask 116. See Sections VIII.B and IX.G.

301. Similarly, as shown in FIG. BF, by comparing FIG. 8 of Lee (top) and FIGs. 11-12 of Freeman (bottom), a POSITA would readily appreciate that Lee's current stepped structures (in red and yellow) in step regions ST22 and ST23 in FIG. 8 are substantially the same as Freeman's current stair-step structures (in red and yellow) in FIG. 12. Thus, a POSITA would have found it obvious to combine Freeman's teachings of the process (as shown in FIG. 11), which would also form the same stepped structures of Lee, to supplement any missing details of Lee, particularly the usage of first chop mask 236 because it is necessary to form the current stair-step structure using first chop mask 236. See Sections VIII.B and IX.G.



302. Likewise, as shown in FIG. BG below, by comparing FIG. 9 of Lee (top) and FIGs. 13 and 14 of Freeman (bottom), a POSITA would readily appreciate that Lee's stepped structures (in red, yellow, and blue) in step regions ST22 and ST23 in FIG. 9 are substantially the same as Freeman's stair-step structure 200 (in

red, yellow, and blue) in FIG. 14. Thus, a POSITA would have found it obvious to combine Freeman's teachings of the process (as shown in FIG. 13), which would also form the same stepped structures of Lee, to supplement any missing details of Lee, particularly the usage of second chop mask 246 because it is necessary to form stair-step structure 200 using second chop mask 246. See Sections VIII.B and IX.G.

FIG. 9

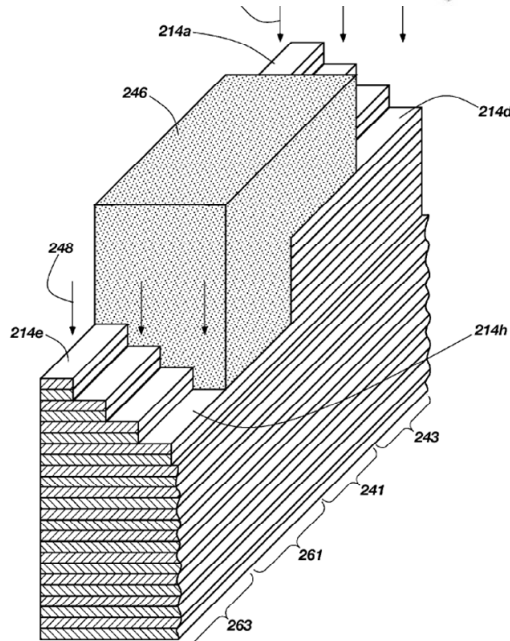
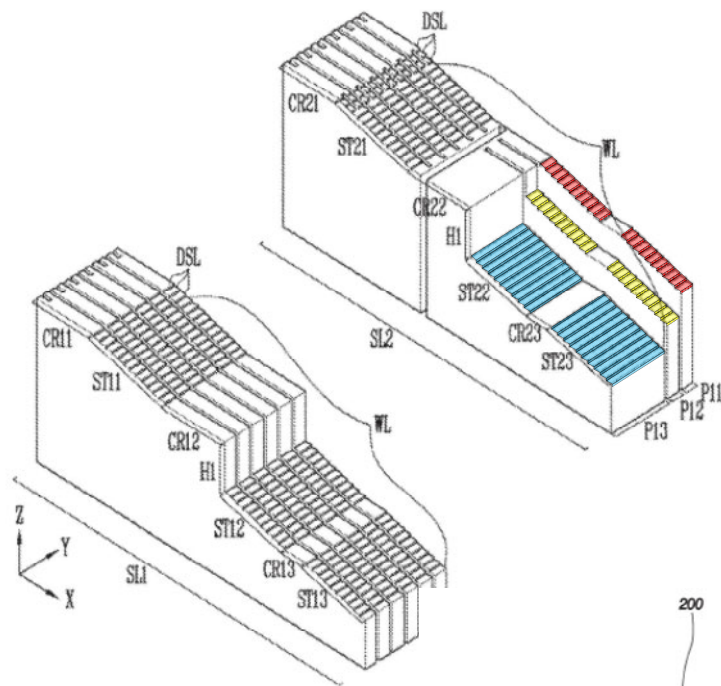


FIG. 13

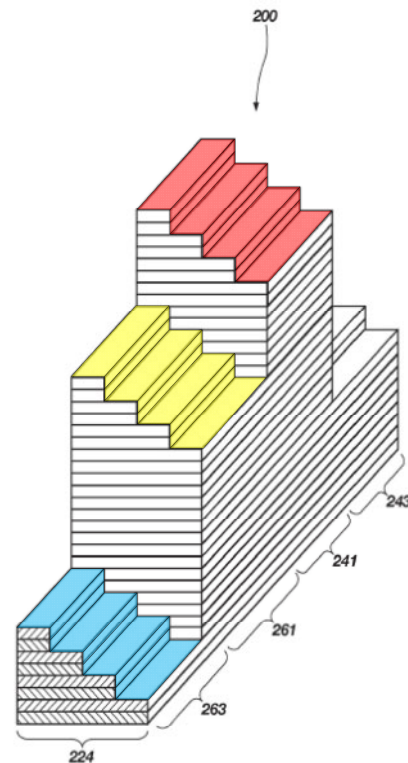


FIG. 14

FIG. BG – Comparison of FIG. 9 of EX1001 with FIGs. 13 and 14 of EX1005 (annotated)

303. For the reasons stated above, a POSITA would have found it obvious to incorporate Freeman's explicit teachings on using stair-step masks and chop masks for forming stair-step structures into Lee's stepped structure formation method.

B. Dependent Claim 12: The method of claim 7, wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks.

304. Lee in view of Freeman renders obvious "wherein forming the stair step structures comprises removing at least a portion of the stair step structures using a single stair step mask and two chop masks."

305. As I explained above with respect to claim 12 in Grounds 1 and 2, Lee discloses or at least suggests "removing at least a portion of the stair step structures," and a POSITA would have understood that Lee discloses, or at least suggests, the usage of a stair step mask and chop masks in forming its stepped structures. *See* Section IX.G.

306. To the extent that additional disclosures are required to render obvious claim 12 besides Lee's disclosures and suggestions explained in Section IX.G, Freeman provides explicit teachings of using a stair-step mask 116, a first chop mask 236, and a second chop mask 246 to form its intermediate stair-step structure 100 in FIG. BE shown above, its current stair-step structure in FIG. BF shown above, and

its stair-step structures 200 in FIG. BG shown above, respectively. *See* Sections VIII.B and X.A. A POSITA would have found it obvious to combine Lee and Freeman to arrive at the claimed invention as recited in claim 12.

C. Independent Claim 14

307. Claim 14 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[14.P] A method of forming a microelectronic device, the method comprising:

[14.a] forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials;

[14.b] forming access lines coupled to memory cells of the array of memory cells;

[14.c] forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack;

[14.d] forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines; and

[14.e] removing at least a portion of the stair step structures using at least one chop mask.

[14.P] A method of forming a microelectronic device

308. I incorporate the discussion provided above with respect to claim limitation **[14.P]** in Grounds 1 and 2, Lee discloses or at least suggests claim

limitation [14.P]. Thus, Lee in view of Freeman renders obvious claim limitation [14.P].

[14.a] forming an array of memory cells within a stack comprising alternating dielectric materials and conductive materials

309. I incorporate the discussion provided above with respect to claim limitation [14.a] in Grounds 1 and 2, Lee discloses or at least suggests claim limitation [14.a]. Thus, Lee in view of Freeman renders obvious claim limitation [14.a].

[14.b] forming access lines coupled to memory cells of the array of memory cells

310. I incorporate the discussion provided above with respect to claim limitation [14.b] in Grounds 1 and 2, Lee discloses or at least suggests claim limitation [14.b]. Thus, Lee in view of Freeman renders obvious claim limitation [14.b].

[14.c] forming conductive vias adjacent the array of memory cells, the conductive vias formed adjacent sub-array circuitry underlying the stack

311. I incorporate the discussion provided above with respect to claim limitation [14.c] in Grounds 1 and 2, Lee discloses or at least suggests claim limitation [14.c]. Thus, Lee in view of Freeman renders obvious claim limitation [14.c].

[14.d] forming at least one stair step region comprising stair step structures using a stair step mask, the stair step structures including steps having contact regions comprising ends of the access lines

312. As I explained above with respect to claim 12, Lee in view of Freeman renders obvious “removing at least a portion of the stair step structures using a single stair step mask and two chop masks.” As explained above with respect to claim 12 in Grounds 1 and 2, Lee discloses “the stair step structures including steps having contact regions comprising ends of the access lines.” Thus, Lee in view of Freeman renders obvious claim limitation **[14.d]**.

[14.e] removing at least a portion of the stair step structures using at least one chop mask

313. As I explained above with respect to claim 12, Lee in view of Freeman renders obvious “removing at least a portion of the stair step structures using a single stair step mask and two chop masks.” I incorporate my discussion here. Lee in view of Freeman renders obvious claim limitation **[14.e]**.

D. Dependent Claim 15: The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.

314. Lee in view of Freeman renders obvious “removing the at least a portion of the stair step structures using the at least one chop mask comprises forming additional contact regions within the at least one stair step region while

reducing a cross-sectional area of the stair step structures.”

315. As I explained above with respect to claim 15 in Grounds 1 and 2, Lee discloses or at least suggests “forming additional contact regions within the at least one stair step region while reducing a cross-sectional area of the stair step structures.” See Section IX.J.

316. To the extent that additional disclosures are required to render obvious claim 15 besides Lee’s disclosures and suggestions explained in Section IX.J, Freeman provides explicit teachings of forming additional contact regions in its stair-step region and reducing the size of the stair-step structure to achieve space-saving. See Sections VIII.B and X.A; see also EX1005, [0042], [0048].

317. For example, as discussed above in Section VIII.B.1 above and with reference to FIG. BH shown below, which includes FIGs. 6 and 9 of Freeman, Freeman discloses (i) using stair-step mask 116 to form intermediate stair-step structure 150 in stair-step region 124 as shown in FIG. 6 and then (ii) using chop mask 126 to form stair-step structure 100 as shown in FIG. 9. Freeman also discloses “[a]s can be seen in FIG. 6, an intermediate stair-step structure 150 may be formed in which **half the number** of sets 115 of the total number of sets 115 includes steps formed therein.” EX1005, [0035]. Freeman also discloses, as shown in FIG. 9, “stair-step structure 100 may include a first region 170 providing exposure to a **first half** of the sets 115 and a second region 180 laterally adjacent the first region 170

providing exposure to a **second half** of the sets 115,” where “an exposed portion of each set 115 may be referred to as a ‘contact region.’” EX1005, [0038]. That is, Freeman discloses by using chop mask 126 to form stair-step structure 100 shown in FIG. 9, the second half of the sets 115 are exposed to form additional contact regions in second region 180 of stair-step region 124. EX1005, [0038]. As a result, the contact regions formed in FIG. 9 are doubled when compared to the contact regions formed in FIG. 6 by using stair-step mask 116.

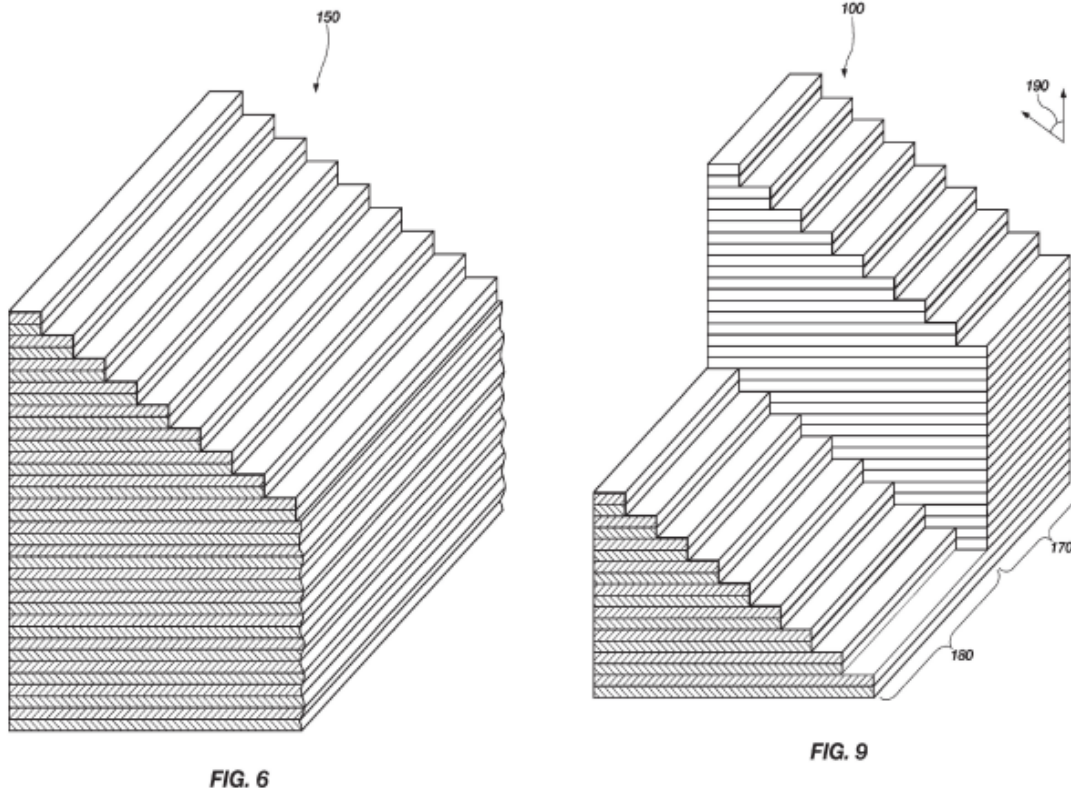


FIG. BH – FIGs. 6 and 9 of EX1005

318. Additionally, Freeman discloses “the method described in this disclosure may include forming two masks (first mask 116 and second mask 126) to

achieve ... space savings.” EX1005, [0042]. With reference to FIG. BH shown above, by exposing the second half of sets 115 to form additional contact regions in second region 180 in FIG. 9, an X-Y-plane area of the newly “chopped” stair-step structure in second region 180 in FIG. 9 is reduced when compared with an X-Y-plane area of intermediate stair-step structure 150 shown in FIG. 6.

E. Dependent Claim 16: The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises using the at least one chop mask after using the stair step mask to double a number of contact regions formed by using a single stair step mask.

319. As I discussed in Section IX.K, Lee discloses or at least suggests claim 16. To the extent that additional disclosures are required, as explained in Section X.D, Freeman discloses that the contact regions formed in FIG. 9 are doubled by using chop mask 126 when compared to the contact regions formed in FIG. 6 by using stair-step mask 116. A POSITA would have found it obvious to combine Lee and Freeman to arrive at the claimed invention as recited in claim 16.

F. Dependent Claim 17

320. Claim 17 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[17.P] The method of claim 14, wherein forming the at least one stair step region comprises:

[17.a] forming the stair step mask over the stack while exposing a width

of a first step;

[17.b] removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask;

[17.c] recessing an edge of the stair step mask to expose a width of a second step; and

[17.d] removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.

321. As discussed in Section IX.L, Lee discloses or at least suggests claim limitations [17.a]-[17.d]. To the extent that additional disclosures are required, a POSITA would have found it obvious to combine Lee and Freeman to supplement Freeman's additional processing details of using the stair step mask regarding [17.a]-[17.d], as discussed below, to Lee's process in FIG. 7. See Sections VIII.B, IX.L, and X.A.

[17.P] The method of claim 14, wherein forming the at least one stair step region comprises:

322. I incorporate the discussion provided above with respect to claim limitation [14.d] in Ground 3, Lee in view of Freeman renders obvious claim limitation [17.p].

[17.a] forming the stair step mask over the stack while exposing a width of a first step

323. Lee in view of Freeman renders obvious "forming the stair step mask over the stack while exposing a width of a first step."

324. In addition to the prior art shown in its FIG. 1A as discussed in Section IX.L, Freeman also discloses forming stair-step mask 116 “over the topmost set 115a of conductive material 112a and insulating material 114a” to “expose a portion of a major surface of the topmost insulating material 114a in the stair-step region 124 that has a width 111 of approximately a desired width of the step to be formed.” EX1005, [0004], [0028], FIG. 2; *see* Section VIII.B.1.

[17.b] removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask

325. Lee in view of Freeman renders obvious “removing at least one tier of the dielectric materials and the conductive materials exposed through the stair step mask.”

326. In addition to the prior art shown in its FIG. 1B as discussed in Section IX.L, Freeman further discloses removing a portion of first set 115a of conductive material 112a and insulating material 114a exposed through stair step mask 116. EX1005, [0004], [0030], FIG. 3; *see* Section VIII.B.1.

[17.c] recessing an edge of the stair step mask to expose a width of a second step

327. Lee in view of Freeman renders obvious “recessing an edge of the stair step mask to expose a width of a second step.”

328. In addition to the prior art shown in its FIG. 1B as discussed in Section IX.L, Freeman further discloses removing an end portion of staircase mask 116 “to

the extent that the portion of the first insulating material 114a that is exposed exhibits a width that is approximately a desired width of a step.” EX1005, [0004], [0032], FIG. 3; *see* Section VIII.B.1.

[17.d] removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask

329. Lee in view of Freeman renders obvious “removing at least another tier of the dielectric materials and the conductive materials exposed through the stair step mask.”

330. In addition to the prior art shown in FIG. 1C as discussed in Section IX.L, Freeman further discloses removing a portion of second set 115b of conductive material 112b and insulating material 114b exposed through stair step mask 116. EX1005, [0005], [0033], FIG. 4; *see* Section III.B.1.

G. Dependent Claim 18

331. Claim 18 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[18.P] The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises:

[18.a] covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask; and

[18.b] vertically recessing the second portion of the stair step

structures such that at least one exposed tier is removed.

[18.P] The method of claim 14, wherein removing the at least a portion of the stair step structures using the at least one chop mask comprises:

332. I incorporate the discussion provided above with respect to claim limitation [14.e] in Ground 3, Lee in view of Freeman renders obvious claim limitation [18.P].

[18.a] covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask

333. Lee in view of Freeman renders obvious “covering a first portion of the stair step structures with the at least one chop mask while exposing a second portion of the stair step structures through the at least one chop mask.”

334. As I explained in Section VIII.B.1, Freeman discloses that chop mask 126 is patterned over insulation layers 114, covering a first region 170 of stair-step region 124, while leaving a second region 180 exposed. EX1005, FIG. 7, [0036].

[18.b] vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed

335. Lee in view of Freeman renders obvious “vertically recessing the second portion of the stair step structures such that at least one exposed tier is removed.”

336. As I explained in Section VIII.B.1, Freeman discloses that the exposed second region 180 is then etched to remove materials from a number of sets 115 to expose sets 115 in the bottom portion of the stack, while leaving first region 170 covered by chop mask 126 intact. EX1005, FIG. 7, [0037].

H. Dependent Claim 19

337. I incorporate the discussion provided above with respect to claim 19 in Grounds 1 and 2, Lee discloses or at least suggests claim 19. Thus, Lee in view of Freeman renders obvious claim 19.

XI. Ground 4: Lee in View of Lim Renders Obvious Claim 13

338. As discussed above in Section IX.H, Lee discloses or at least suggests claim 13. To the extent claim limitation [13.b] of claim 13 requires “forming the conductive vias in the via region” and “isolating the conductive vias,” when “the stack of alternating dielectric materials” still exists, Lee in view of Lim suggests claim limitation [13.b] and thus, renders claim 13 obvious in my opinion.

339. An overview of Lim is provided above in Section VIII.C.

A. Reasons to Combine Lee and Lim

340. A POSITA would have found it obvious to combine Lee and Lim for various reasons discussed below in detail. Specifically, a POSITA would have been motivated to modify Lee in view of Lim to form Lee’s contact plugs 52 in the remaining alternating dielectric stack, instead of blocking layers 31, of the memory

block, thereby simplifying the manufacturing process.

1. Teaching, suggestion, and motivation in prior art

341. Lee's stated objectives include minimizing semiconductor device size, enhancing integration density, and streamlining the manufacturing process to reduce costs. EX1004, [0009]. While Lee discloses forming contact plugs 32 in blocking layers 31, which "may be formed of an insulating material such as an oxidation layer," Lee does not specify the timing of forming blocking layers 31 and contact plugs 32 within its fabrication process flow. EX1004, [0077].

342. As discussed in Section VIII.C.2, Lim, in its first embodiment, discloses the partial gate replacement process for forming insulating structure 23 having a stack of alternating first and second insulating patterns 20a and 22a (FIG. 23A). In contrast, as discussed in Section VIII.C.3, Lim, in the second embodiment, discloses forming contact plugs 52 through insulating structure 123 of silicon oxide, which is analogous to Lee's contact plugs 32 formed through blocking layers 31. EX1006, [0140], [0144], FIG. 11A; EX1008, ¶¶92, 96, FIG. 11A.

343. Comparing the process flows of these two embodiments, a POSITA would readily appreciate that, to form insulating structure 123, Lim introduces an additional processing step (step 340 in FIG. 29, FIG. 30A) before the gate replacement step in its second embodiment. EX1006, [0269]; EX1008, ¶222; see also Section VIII.C.3. This additional step is not required in Lim's first embodiment,

where insulating structure 23 is formed as part of a more streamlined process. Specifically, in the first embodiment, Lim utilizes a partial gate replacement process that inherently leads to the formation of insulating structure 23, simplifying the overall fabrication flow. By contrast, the second embodiment requires an extra step to independently form insulating structure 123 before proceeding with contact plug formation.

344. A POSITA would have recognized that Lim's first embodiment offers a more efficient alternative, reducing processing complexity and manufacturing time. Since insulating structure 23 is already present due to the partial gate replacement process, this approach eliminates the need for additional deposition and patterning steps. As a result, contact plugs 52 can be subsequently formed through the pre-existing dielectric materials of insulating structure 23, avoiding redundant fabrication steps. This optimization aligns with industry goals of minimizing process steps, improving yield, and reducing costs in semiconductor manufacturing.

345. Since Lee's contact plugs 32 are formed within blocking layers 31, which are structurally and functionally equivalent to Lim's insulating structure 123 in the second embodiment, a POSITA would have recognized, or at the very least found it obvious, that Lee likely employs an analogous process for forming blocking layers 31, akin to the fabrication approach used in Lim's second embodiment. EX1006, [0140], [0144]; EX1008, ¶¶92, 96, FIG. 11A.

346. Given this understanding, a POSITA would have been motivated to modify Lee's process by incorporating Lim's partial gate replacement approach from its first embodiment. By doing so, blocking layers 31—analogueous to Lim's insulating structure 123—could be eliminated, thereby streamlining the overall manufacturing process. Instead of separately forming blocking layers 31 and subsequently integrating contact plugs 32, the partial gate replacement process would allow for the direct formation of contact plugs through pre-existing dielectric materials, much like how Lim's first embodiment facilitates the formation of insulating structure 23.

347. This modification would not only simplify Lee's process but also directly align with its stated objectives of reducing semiconductor device size, improving integration efficiency, and minimizing fabrication complexity to lower production costs. By eliminating redundant processing steps and unnecessary material depositions, this approach would enhance manufacturing efficiency while maintaining or even improving device performance and structural reliability.

348. Moreover, a POSITA would have been further motivated to apply a partial gate replacement process to Lee's fabrication method due to the structural advantages provided by Lim's approach. As illustrated in FIG. 23A of Lim, insulating structure 23—composed of a remaining stack of alternating dielectric materials—serves as a mechanical support for insulating patterns 20a/20b. This

structural reinforcement prevents these insulating patterns from collapsing or bending when empty spaces 36 are introduced between them during the gate replacement process. EX1006, [0221], FIG. 23A; EX1008, ¶173, FIG. 23A. By utilizing this structural support, the need for additional supporting structures is eliminated, leading to a more compact device and a streamlined manufacturing process.

2. *Reasonable Expectation of Success*

349. Lim's partial gate replacement technique is applicable to Lee's fabrication process flow due to the significant similarities between Lee and Lim, which align with the requirements of the claimed invention. Specifically, both Lee and Lim disclose memory cells within a memory cell region, stair-step structures in a stair-step region, conductive vias in a via region, access lines, and dielectric material within slots, as well as the formation methods for these components, as required, for example, by claim 7. See Sections VIII.A, VIII.C. These structural and procedural similarities provide a foundation for the interchangeability of components and processes between Lee and Lim. This interchangeability enables a POSITA to modify components or processes from one reference and apply them to the counterpart in the other, facilitating a seamless integration of Lim's partial gate replacement technique into Lee's process to achieve the desired improvements in the fabrication of semiconductor devices.

350. It is well within a POSITA's capabilities to apply the partial gate replacement process to Lee's fabrication method without undue difficulty and with a reasonable expectation of success. Lim provides explicit guidance on the technique, specifically detailing how to set the distance between adjacent trenches 34 to control the location and extent of the partial gate replacement. EX1006, [0219], [0222], FIGs. 2A, 3A; EX1008, ¶¶171, 174, FIGs. 2A, 3A; see Section VIII.C.2.a. This detailed guidance, in combination with common knowledge in the field, equips a POSITA with the necessary tools to implement various viable designs for applying the partial gate replacement process to Lee's device and process. Given the clear teaching in Lim and the familiarity of a POSITA with these methods, the application of the technique to Lee's fabrication flow would be straightforward, without requiring undue experimentation or deviation from established practices.

351. For instance, the adjacent slots in Lee's device could be designed with a sufficient distance between them in contact region CR21 to enable partial gate replacement to occur in that region. This configuration would leave the stack of alternating dielectric materials intact in contact region CR21, which would then function as the insulating structure for contact plugs 32. By controlling the spacing between the slots, the partial gate replacement can be localized to only the desired region, ensuring that the insulating structure in the contact region remains functional and aligned with the intended design requirements.

352. A POSITA would have understood, or at the very least found it obvious, that the distance between adjacent slots could be adjusted in other regions as needed, for instance, by designing the slots to follow non-straight lines. This would allow the prevention of partial gate replacement in certain areas, depending on the design requirements. For example, in memory region MC, this approach could help maintain the cell density by ensuring a full gate replacement in memory region MC such that all the sacrificial dielectric layers are replaced by gate lines where memory cells can form. Such an adjustment ensures that the functional characteristics of each region are preserved, optimizing the overall device performance.

353. Furthermore, a POSITA would have recognized that implementing such adjustments to the slot design would not introduce any additional processing steps or complexity. The existing process flow of Lee for forming contact plugs 32 could still be followed without the need for new or specialized techniques. After the partial gate replacement process is completed, contact plugs 32 could be formed through the remaining stack of alternating dielectric materials using the same standard contact hole etching and conductive material deposition steps that are already employed in Lim's TAVs formation process, as shown in FIGs. 26A-26B. This allows for a seamless integration of the modification into the existing fabrication workflow, enhancing the efficiency and manufacturability of the device.

B. Dependent Claim 13

354. Claim 13 is reproduced below. For ease of discussion, I have included a label for each claim limitation.

[13.P] The method of claim 7, wherein:

[13.a] forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials; and

[13.b] forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

[13.P] The method of claim 7, wherein:

355. Lee in view of Lim renders obvious the method of claim 7. I incorporate my discussion for claim 7.

[13.a] forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials

356. I incorporate the discussion provided above with respect to claim limitation **[13.a]** in Grounds 1 and 2, Lee discloses or at least suggests claim limitation **[13.a]**.

357. Lim also discloses “forming the array of memory cells in the memory cell region comprises forming vertical memory cell pillars within a stack of alternating dielectric materials.”

358. Specifically, Lim discloses forming a molding structure MS, including alternating first and second dielectric molding layers 20 (e.g., silicon oxide) and 22 (e.g., silicon nitride). EX1006, [0208], [0209], [0216], FIGs. 21A, 21B; EX1008, ¶¶160, 161, 168, FIGs. 21A, 21B. Lim further discloses forming cell vertical structures CV within molding structure MS. EX1006, [0211]-[0214], FIGs. 22A, 22B; EX1008, ¶¶163-166, FIGs. 22A, 22B. Lim's cell vertical structures CV also qualify as the claimed "vertical memory cell pillars," consistent with the '974 Patent. EX1006, [0212]-[0214]; EX1008, ¶¶164-166; EX1001, 4:32-37.

[13.b] forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials.

359. I incorporate the discussion provided above with respect to claim limitation **[13.b]** in Grounds 1 and 2, Lee discloses or at least suggests claim limitation **[13.b]**.

360. To the extent (not conceding) claim limitation **[13.b]** requires the timing of "forming the conductive vias in the via region" and "isolating the conductive vias," specifically, when "the stack of alternating dielectric materials" still exists, Lim discloses the partial gate replacement process in forming its semiconductor device, as explained above in Section VIII.C.2.a. EX1006, [0221], [0222], [0225], FIG. 23A; EX1008, ¶¶173, 174, 177, FIG. 23A.

361. The partial gate replacement process results in insulating structure 23

having alternating first and second insulating patterns 20a and 22a, which is part of molding structure MS. Lim further discloses forming contact plugs 52 by etching contact holes through insulating structure 23 and forming a conductive material layer filling the contact holes, thereby isolating contact plugs 52 from cell gate conductive patterns 38a. EX1006, [0233], [0234], [0240], FIG. 26A; EX1008, ¶¶185, 186, 192, FIG. 26A. See also Sections VIII.C.1.c and VIII.C.2.

362. Therefore, Lim discloses “forming conductive vias in the via region comprises isolating the conductive vias within the stack of alternating dielectric materials,” even under a narrower interpretation.

363. As discussed in Section XI.A, a POSITA would have found it obvious to form Lee’s contact plugs 32 using Lim’s partial gate replacement and simultaneous contact structure forming processes, such that the number of processing steps can be reduced, thereby simplifying the manufacturing process and reducing costs.

XII. Secondary Considerations

364. I have seen no evidence in the ’974 Patent’s prosecution history or elsewhere supporting any secondary considerations arguments, or evidence of nexus to any of the challenged claims. See generally EX1002. Indeed, per my discussion of the prior art referenced herein, any purported solutions to problems or unexpected results in the ’974 Patent were already well known. To the extent Patent Owner

asserts the existence of any secondary considerations in its responses, I reserve my right to address any such evidence.

XIII. Additional Remarks

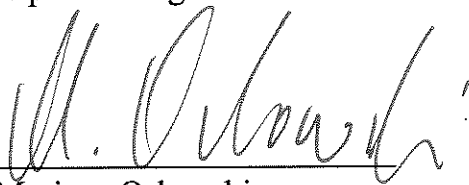
365. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

366. I have reviewed the accompanying Petition for *Inter Partes* Review of the '974 Patent and, given the information set forth in this declaration, I agree with the reasoning and conclusions of the grounds of challenge in the petition. Based on my own analysis, I agree that: (1) Lee anticipates or otherwise renders obvious claims 1, 4, 5, 7, 9, and 11-19; (2) Lee in view of Freeman also renders obvious claims 12 and 14-19; and (3) Lee in view of Lim also renders obvious claim 13.

* * *

I hereby declare that all statements made are of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this proceeding.

Dated: 2-13-2025

By: 
Dr. Mariusz Orłowski
Pembroke, Virginia

APPENDIX A

Marius K. Orlowski Ph.D. Curriculum Vitae

Professional Summary

Marius Orlowski Ph.D. has 40 years of experience in the semiconductor industry, with a specific emphasis on the physics of semiconductor devices, processes and manufacturing. He held technical positions at Stanford University, Purdue University, and the German Space Agency in Stuttgart-Vaihingen, Germany. For over 25 years he has worked in the semiconductor industry, first at Siemens and then at Motorola, whose semiconductor division later became Freescale Semiconductor. Since 2008 he has been a Professor at Virginia Tech, where he continues his research in semiconductor device physics and technology.

His research in semiconductor device physics at Motorola had a specific emphasis oxidation, diffusion, mechanical stress effects in silicon, and crystal defects, as well as on non-volatile memories and associated physical effects, such as band-to-band tunneling. In 1990, he was the first to explain the so called reverse short channel effect in MOSFET and to explain band-to-band tunneling in MOSFETs, and correctly predicted new modes of tunneling. In addition, he researched the impact of band-to-band tunneling on non-volatile memories. In addition to conducting research in semiconductor physics, he successfully managed the development of several technologies, like a 50nm fully depleted silicon-insulator (SOI) MOSFET with TiN/HfO₂ gate stack, and a 30nm gate length SOI MOSFET. He led the effort to explore the potential of GeOI for MOSFET applications.

Dr. Orlowski is the lead inventor on most of the 109 patents issued, and has over 230 publications in scientific journals and conference proceedings.

Expertise

- CMOS Devices (MOSFET, Floating Gate MOSFET, Bipolar, Diodes, Thin Film, SOI, FINFET devices)
- CMOS Process technology (oxidation, chemical and plasma etching, implantation, diffusion, photolithography, trench and LOCOS isolation, crystal defects, stress relaxation)
- Nonvolatile (NAND and NOR FLASH) memory (memory architecture, programming and erase operations, manufacturing issues), manufacturing
- Resistive Switching Memory Cells, Memristors
- Semiconductor Memory: SRAM, DRAM, NVM (see below)

Education

<u>Year</u>	<u>College or University</u>	<u>Degree</u>
1981 – 1982	Stanford University (Stanford Linear Accelerator Center)	Post-doctoral position (research associate) in theoretical physics
1980 – 1981	Tuebingen University, Germany	Wissenschaftlicher Assistent – Assistent Professor (Physics)
1977 –	Tuebingen University, Germany	Ph.D., in theoretical nuclear physics; Ph.D. thesis

Marius K. Orlowski Ph.D.

Curriculum Vitae

1979	entitled: "Resonances in Two- and Three-Cluster Systems," magna cum laude
1971 – Tuebingen University, Germany 1976	Masters, in experimental superconductivity physics; master thesis entitled: "Josephson Behavior in Microbridges of Superconductors with Large Cross Section"
1976 – Tuebingen University, Germany 1977	B.S., Business Administration
1970 Schule Schloss Salem, Lake Constance, Germany	Baccalaureate (Abitur 1970)

Professional Experience

From: 2008
 To: Present
 Organization: Virginia Polytechnic Institute and State University
 Title: Virginia Microelectronics Consortium Chair
 Full Professor
 Summary: Currently working on a restive RAM memory which is a leading candidate to replace current FLASH technology based on floating gate MOSFET transistor.

From: 1989
 To: 2008
 Organization: Motorola/Freescale Research Labs (Austin Texas, Moscow Russia, Grenoble France)
 Summary:

2006 – 2008 Co-Director of Novel Device Development, Crolles Alliance, Grenoble, France

1998 – 2006 Department Manager for CMOS and NVM Development

1995 – 1998 Director of Motorola Research Labs in Moscow, Russia

- Build up the lab from scratch
- Hired 40 scientists/engineers, business manager, two accountants, two IT administrators, receptionist, and drivers
- Hired over 50 contractors
- Administered a budget of \$4.8M
- Dealt with contract, customs, import-export, office lease, office move issues

1989 – 1995 Motorola Research Laboratories Austin Texas, CMOS Engineering

- Section MGR TCAD Modeling and Simulation Group

Conducted research in semiconductor device physics at Motorola had a specific emphasis on non-volatile memories and associated physical effects, such as band-to-

Marius K. Orlowski Ph.D. Curriculum Vitae

band tunneling. In 1990, was the first to simulate band-to-band tunneling in MOSFETs, and correctly predicted new modes of tunneling. In addition, researched the impact of band-to-band tunneling on non-volatile memories.

From: 1984
To: 1989
Organization: Siemens Research Labs, CMOS, DRAM and NVM Development (Munich, Germany)
Summary:

1987 – 1989 Project Leader in Process Simulation and Modeling

- Represented Siemens at several European consortia (Fraunhofer)/company (Philips) and university collaborations

1984 – 1987 TCAD Engineer

Conducted early research in the physics of metal-oxide-semiconductor field effect transistors (MOSFETs), which today constitute the basic building blocks of all mainstream integrated circuits. In 1987, published the first explanation of a fundamental phenomenon known as the “reverse short channel effects,” which has since become a standard feature of all advanced MOSFETs. In 1989, published an in-depth analysis that correctly predicted degradation effects in MOSFETs.

From: 1983
To: 1984
Organization: DFVLR, (now DLR Deutsches Zentrum für Luft- und Raumfahrt, The German Aerospace Center, Stuttgart-Vaihingen, Germany)
Title: Research Scientist
Summary: Research topic: flame propagation and detonations

From: 1982
To: 1983
Organization: Purdue University, Physics Department (West Lafayette Indiana USA)
Title: Faculty Staff
Summary: Lectures in quantum mechanics, electrodynamics, quantum electrodynamics; research topic: quarks in few nucleon systems

From: 1981
To: 1982
Organization: Stanford Linear Accelerator Center, Stanford University (Stanford CA USA)
Title: Research Associate
Summary: Research topic: Few-Nucleon Systems

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From: 1979
To: 1981
Organization: University of Tuebingen, Institute of Theoretical Physics (Tuebingen Germany)
Title: Assistant Professor (Wissenschaftlicher Assistant)
Summary: Research topic: Nuclear Clusters, Few-Body Systems; teaching: seminars for graduate physics student in quantum mechanics and in numerical methods in mathematical physics

From: 1972
To: 1979
Organization: University of Tuebingen, Teaching Assistant, (Tuebingen Germany)
Title: Teaching Assistant
Summary:

- Taught seminars and exercises in advanced mathematics, applied physics, theoretical physics
- Lectured in quantum mechanics and numerical methods in physics

Litigation Support Experience

Expert Engagement:

Type of Matter: Regarding FLASH memory products
Law Firm: McDermott Will & Emery
Case Name: Spansion v. Samsung
Services Provided:

- Assessed patents and patent claim charts for device and process related patents
- Claim construction, written/reviewed interrogatories, and responded to objections of the opposing party
- Wrote rebuttal expert report regarding validity of patents in question
- Wrote expert report regarding infringement of a patent by products of the counterparty
- Wrote expert report regarding term construction of claims
- Worked on infringement issues for several patents
- Prepared infringement claim charts
- Reviewed test programs of products alleged to infringe a patent
- Analyzed programming and erase operations of Samsung NVM products
- Prepared questions for witness interrogation
- Analyzed device issues related to MOSFET transistors, floating gate devices, capacitors
- Analyzed process related issues: layer deposition, filling of cavities, LOCOS

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Curriculum Vitae

and BOX isolation techniques, ONO stacked films, stacked gate structures, sacrificial layers, doping techniques, HDP oxide deposition, isotropic and anisotropic etching techniques

- Analyzed timing diagrams of several Samsung and Spansion NAND and NOR products (core schematics, core timing)
- 27 nm Bardeen, 32 nm Coral, 42 nm Cubic, 59 nm Jasper, 63 nm Agate OneNAND, SLC, NAND, MLC NAND, 73 nm Spinel, 90 nm SLC & MLC One NAND & FLEX OneNAND
- Analyzed memory testers (probe stations): Yokogawa Tester (MT6121) operations, commands, diagnostics, redundancy operations; AL6050 tester, leakage test, monitoring of DC levels; evaluated program languages: Perl/Tk, Python, C/C++, TCL script language.
- Analyzed laser repair algorithms, e-fuse data history.

Disposition: Settled
Date: 2010 – 2011

Expert Engagement:

Type of Matter: Patent Litigation regarding FLASH memory and technology
Law Firm: King & Spalding
Case Name: Spansion v. Samsung
Services Provided:

- Claim construction, written/reviewed interrogatories, and responded to objections of the opposing party
- Wrote rebuttal expert report regarding validity of patents in question
- Wrote expert report regarding term construction of claims
- Worked on infringement issues for several patents
- Prepared questions for witness interrogation
- Analyzed device issues related to MOSFET transistors, floating gate devices, capacitors
- Analyzed process related issues: layer deposition, filling of cavities, LOCOS and BOX isolation techniques, ONO stacked films, stacked gate structures, sacrificial layers, doping techniques, HDP oxide deposition, isotropic and anisotropic etching techniques
- Circuit implementation: dummy lines, local lines
- Gave deposition (7.5 hour)
- Gave testimony at the trial (ITC court)

Date: 2009 – 2010

Expert Engagement:

Type of Matter: Patent Litigation regarding Tungsten Plug Manufacturing and Technology
Law Firm: Fish & Richardson
Case Name: Avago Technologies v. Maxim Integrated Products

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Services Provided: ▪ Worked on infringement issues for several patents
 ▪ Reviewed literature on tungsten “volcano” effect
 ▪ Reviewed and assessed several patents

Disposition: Out-of-court settlement between the parties
Date: 2015 – 2016

Expert Engagement:

Type of Matter: Patent Litigation regarding FinFET transistor
Law Firm: Glaser Weil, Los Angeles
Case Name: Kaist IP US, LLC v. Samsung Electronics Co., Ltd., Samsung Electronics
 America, Inc., Samsung Semiconductor, Inc., Samsung Austin Semiconductor,
 LLC, GlobalFoundries, Inc., GlobalFoundries US, Inc., Qualcomm, Inc.

Services Provided: ▪ Worked on infringement issues of a FinFET patent
 ▪ Analyzed Samsung process flow of a FinFET for infringement issues
 ▪

Disposition: ongoing
Date: 2016 -2018

Expert Engagement:

Type of Matter: Patent Litigation regarding Contact Formation
Law Firm: Oblon Washington, D.C.

Case Name: Mediatek vs American Patents

Services Provided: ▪ Worked on infringement issues of a Contact Barrier Layer Deposition
 ▪ Written State of the Art 2003 of Contact Formation Technology
 ▪

Disposition: Settled August 2019
Date: July-August 2019

Expert Engagement:

Type of Matter: Patent Litigation regarding FinFET transistor
Law Firm: Mintz, Boston

Case Name: Globalfoundries vs TSMC

Services Provided: ▪ Infringement issues and prior art for FinFET transistor

Marius K. Orlowski Ph.D.
Curriculum Vitae

- Prior art for Bit Cell with double patterned metal layer structures

Disposition: Settled October 2019

Date: July-October 2019

Expert Engagement:

Type of Matter: Patent Litigation

Law Firm: Mintz, Boston (Sean Casey, Jessica

Case Name: Investigation No. 337-TA-1336 (UNITED STATES INTERNATIONAL
TRADE COMMISSION)

Services Provided:

- Evaluated Intel source materials
- Evaluated three dozens of patents related to contact resistance with SiGe-enhanced contacts to MOSFET and FinFET transistors, Self-aligned gate edges, gate-first vs gate-last approaches, gate-all-around, poly gate vs metal gate
- Worked on infringement contentions
- Worked on claim charts
-

Disposition: Settled September 2023

Date: September 2022 - September 2023

Non-Litigation Consulting Projects

- Crolles Alliance (STmicroelectronics, NXP, Freescale) MGR for FDSOI 32 nm device development
- Advanced Modules Development MGR, Freescale, 2006 – 2008.
- Crolles2 Alliance Director of Modeling and Simulation Laboratory, 2006 – 2008.
- Project Manager (MGR) for Freescale proprietary projects with LETI, MINATEC, and Grenoble University, 2006 – 2008.
- Project Manager for European and French Government sponsored projects: MEDEA+, PULLNANO, SILONIS, FORMOST, NANO2008, 2006 – 2008.
- Staff MGR for Advanced Device Development Group and Unit Process Modeling and Simulation Group, Freescale Research Labs, Austin, Texas, 2002 – 2006.

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- Project leader on GeOI (Ge-FD-MOSFETs, photodiodes, heteroepitaxy for optical applications) Freescale – SOITEC collaboration, 2005 – 2006.
- Program manager for Sarov Laboratory collaboration (Dr.V; Pavlovsky), Sarov, Russia, under the auspices and funding of the US Department of Defense and Nuclear City Initiative (NCI), 2003 – 2004.
- Program and Project Manager for SOFT-TEC (at its height over 110 scientists/engineers), Russian Academy of Science, Moscow Russia; administered a budget of max \$2.7M, dealt with contract work, intellectual property, export-import issues, purchase of computer gear, office space and furniture, 2001 – 2005.
- Program and Project MGR for KINTECH (at its height 40 scientists/engineers), Khurchatov Institute, Moscow; administered a budget of \$1.6M; dealt with contract work and intellectual property issues, 2001 – 2005
- Project MGR for several projects with SOFT-TEC (Russian Academy of Sciences), Moscow Russia, 1991 – 1995
- Staff MGR for Compact (SPICE) Simulation Group, Design Rules Manual Group, Software Platform Development, and TCAD Modeling and Simulation Group, 1998 – 2002
- Consulted with SOITEC company on engineered wafer substrates and applications. Contact: Dr. Carlos Mazure, CTO of SOITEC. SOITEC is world leader in providing SOI and other so called engineered wafers
- Consulted with Qimonda on memory cell architectures and process flows. Contact: Dr. Johann Harter, vice-president of Qimonda. Qimonda was a leading company in DRAM, NAND and NOR memory chips.
- Consulted with Qatar National Research Fund on semiconductor technology projects. Contact: Dr. Abdul Sattar Al-Taie.
- Program MGR for China Research Lab (Beijing, China); administered a budget of \$1.2M; collaboration with Beijing and Tsinghua universities, 1999 – 2001

Professional Affiliations, Achievements & Awards

Awards

- IEEE Life Fellow Status 2021
- Fulbright Fellowship for Eminent Chair Professors (Turin, Italy), 2014-2015
- Master Innovator Award Freescale (there were 15 Master Innovators at Freescale, a company of 24,000 employees), 2007
- Platinum Silver Quill (Publication) Award Motorola, 1999
- Fellow of Technical Staff Motorola/Freescale, 1998
- Distinguished Innovator Award Motorola, 1998

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- IEEE Fellow Award, citation: for contributions to the modeling of MOSFET devices and technology (IEEE - Institute of Electrical and Electronics Engineers), 1997
- Scheffel Award (Scheffelpreis of the State Baden-Wuerttemberg, Federal Republic of Germany), 1970

Major Accomplishments

- Over 230 publications in refereed scientific journals and conference proceedings
- 108 international patents including 80 US patents
- First to explain the reverse short channel effects in MOSFETs (IEDM 1987); the reverse short channel effect is a standard feature of all MOSFET generations since 1987
- In depth analysis of LDD degradation, predicted avalanche and device degradation on the source side of the MOSFET (IEEE Transactions on Electron Devices 1989)
- One of the pioneers of pair-diffusion theory or dopants in silicon, first formulation of a coupled pair-diffusion equations for dopants and point defects, predicted uphill diffusion (Appl. Phys: Letters 1989, Physics Letters A 1989, IEDM 1990, NUPAD 1990)
- First to explain band-to-band current in MOSFETs and FLASH memory devices
- Proposed three-phase segregation model, all modern segregation models are based on a three- phase approach (Appl. Phys. Letters 1989)
- First to describe microscopically diffusion on grain boundary networks; predicted dopant accumulation at the vertices of the network (Electron Device Letters 1992, SIAM 1992, IEDM 1992)
- First to simulate band-to-band tunneling in MOSFETs and correctly predicted new modes of tunneling (Electron Device Letters 1990, VLSI Symposium 1990)
- Explained anomalous boron clustering effect (IEDM 1997)
- First to show that zero-flux condition does not necessarily require zero gradient of concentration distribution at the interface (phys. stat. sol. 2003, SISPAD 2003)
- Successful development of 50 nm Fully depleted SOI MOSFET with TiN/HfO₂ gate stack; development of 30 nm gate length SOI MOSFET (SOI Conference 2003, Electron Device Letters 2003, Nanotechnology IEEE Transactions 2003)
- Invented a multichannel gate all around FinFET transistor with vastly superior performance over current transistor approaches US7112832 B2 (2006) and US6921700 B2 (2005)
- Invented silicon monocrystalline nanowires transistor using conventional CMOS process steps US20070029586 A1 (2007)
- Invented a method for uniform (across the wafer selective source/drain epitaxial growth US20060286736 A1 (2006)
- Established first TCAD Modeling and Simulation group at Motorola 1989-1995
- Established first Equipment (Unit Process) Modeling and Simulation at Motorola (1992-1995)

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- Managed successfully Motorola:Freescale program with SOFT-TEC, Russian Academy of Science (105 engineers/scientists); and with KINTECH, Khurchatov Institute (25 engineers and scientists), both in Moscow Russia; project with Sarov Laboratory, Sarov, Russia
- Build up from ground up Motorola Research Laboratory (40 scientists) in Moscow, Russia (1995-1998)
- Established the first Design Manual Group on the technology development side (2000)
- Explained the physics of the constant in multilevel switching of the resistive non-volatile cell (2013)

Teaching Experience

- Gave three graduate student classes on fundamental semiconductor concepts and advanced semiconductor devices and three undergraduate classes on electric theory, 2008 – 2011.
- Gave internal courses in device physics, semiconductor technology, process integration, and patenting skills at Motorola/Freescale, 1989 – 2008.
- Was lecturer in VLSI Process and Device Simulation, CEI Elsevier in Advanced Technology, Davos, Switzerland, 1990.

Research Activities

- 2008 – Development of resistive RAM technology as a replacement for the current floating-gate based FLASH memory; nanoscale devices including nanowire devices, nanomembranes for electronic devices and photovoltaic applications; resistive switches for memory, logic and neural network applications.
- 2006 – 2008 – Development of silicon nanocrystal thin-films for floating gates— in place of today's polysilicon floating gates—to move embedded flash to advanced processing nodes including switchover to nanocrystals from both the split-gate and single-transistor (1-T) FLASH architectures. Development of fully depleted SOI transistors with advanced gate stack (HfZrO₂ with TaC and WN and MoN metals), with elevated source/drains, and compressive/tensile stressors). Development of SON single-gate and double-gate transistors, and multichannel FinFET transistors based on sacrificial epitaxial SiGe layers; development of MOSFETs on GeOI in collaboration with SOITEC and LETI development of self-aligned Cu barriers for back-end based on CoWPB. Development of plasma etch recipes for high-k/metal gate stacks.
- 2005 – 2006 – One – person GeOI project in collaboration with SOITEC; material analysis, dopant diffusion in SiGe and Ge, photodiodes on GeOI, heteroepitaxy on GeOI substrates for optoelectronic applications.
- 2002 – 2005 – Development of novel devices for FLASH memory. Development of FinFET-like transistors, application of mechanical stressors for mobility enhancement, MOSFETs on strained SOI wafers.
- 2001 – 2006 – Modeling and simulation of plasma-based etch and deposition processes.
- 1998 – 2001 – TCAD Simulation and Modeling, Compact (SPICE) Modeling and Simulation, Design Rules Generation, Development of Platform Software (data bases, optimization engines).

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- 1995 – 1998 – Design tool development (channel router, layout cell compactification, time skew and timing analysis, clock time optimization).
- 1989 – 1995 – TCAD process and device modeling and simulation (MOSFET, NVM FLASH devices, DRAM cells, isolation, diffusion, annealing, silicidation).
- 1984 – 1989 – TCAD process and device simulation (MOSFET, DRAM), SPICE modeling of MOSFETs
- 1983 – 1984 - Combustion processes, flame propagation, detonation conditions.
- 1979 – 1982 – Nuclear and particle physics (few-body systems, cluster interactions, nucleon and quark degrees of freedom).
- 1976 – 1977 – Superconductivity, Josephson effects in weak links, installation of experimental setup for cryogenic experiments

Patents & Publications

- 109 patents issued including 81 US patents; 8 patents to be issued; additional 4 patent disclosures at Virginia Tech filed with US Patent Office, 12 defensive publications (not listed, available on request)
- Distinguished Innovator Award 1998 Motorola
- Master Innovator Award 2007 Freescale
- Patents generated with Siemens, Motorola, Freescale, STMicroelectronics, NXP, Virginia Tech
- Member of the Freescale Patent Committee
- Chairman of the Intellectual Property Brainstorming Sessions
- Member of Motorola/Freescale Patent Enforcement and Litigation Committee
- Two Trade Secrets with Freescale
- Lead inventor on the majority of the patents:
-

See also the profile Marius Orlowski at Google Scholar

Most recent: 16/168.678 Patent application, publication date: 2019/2/21 “Method to Manufacture Highly Conductive Vias and PROM Memory Cells by Application of Electric Pulses”, inventors: M. Orlowski, G. Ghosh, A. Verma

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<u>Patent</u>	<u>Date</u>	<u>Description</u>
9,792,985	10/17/2017	Resistive volatile/non-volatile floating electrode logic/memory cell
9,116,432	08/25/2015	Multiple exposure with image reversal in a single photoresist layer
8,633,515	01/21/2014	Transistor with immersed contacts
8,552,501	10/08/2013	Method of forming an inverted T shaped channel structure for an inverted T channel field effect transistor device
8,377,793	02/19/2013	Method for manufacturing a non-volatile memory, non- volatile memory device, and an integrated circuit
8,314,448	11/20/2012	Transistors with immersed contacts
8,293,608	10/23/2012	Intermediate product for a multichannel FET and process for obtaining an intermediate product
8,264,060	09/11/2012	Method of sealing an air gap in a layer of a semiconductor structure and semiconductor structure
8,202,798	06/19/2012	Improvements for reducing electromigration effect in an integrated circuit
8,158,484	04/17/2012	Method of forming an inverted T shaped channel structure for an inverted T channel field effect transistor device
8,071,459	12/06/2011	Method of sealing an air gap in a layer of a semiconductor structure and semiconductor structure
7,986,006	07/26/2011	Single Transistor Memory Cell with Reduced Recombination Rates
7,968,394	06/28/2011	Transistor with immersed contacts and methods of forming thereof
7,939,412	05/10/2011	Process for forming an electronic device including a fin-type transistor structure
7,932,189	04/26/2011	Process of forming an electronic device including a layer of discontinuous storage elements
7,928,502	04/19/2011	Transistor devices with nano-crystal gate structures
7,927,956	04/19/2011	Method for making a semiconductor structure using silicon germanium
7,872,311	01/18/2011	Method and apparatus for mobility enhancement in a semiconductor device
7,811,891	10/12/2010	Method to control the gate sidewall profile by graded material composition
7,781,840	08/24/2010	Semiconductor device structure
7,772,584	08/10/2010	Laterally grown nanotubes and method of formation
7,723,805	05/25/2010	Electronic device including a fin-type transistor structure and a process for forming the electronic device
7,700,438	04/20/2010	MOS Devices with nano-crystal gate structure
7,683,443	03/23/2010	MOS Device with Multi-Layer Gate Stack
EP 1751791	0/2/03/2010	Method for making a semiconductor structure using silicon germanium
EP1728274	06/09/2010	Method for forming a semiconductor device having a notched control electrode and structure thereof
7,629,220	12/08/2009	Method for forming a semiconductor device and structure thereof
7,608,893	10/27/2009	Multi-channel transistor structure and method of making thereof
7,592,248	09/22/2009	Method of forming semiconductor device having nanotube structures
7,575,958	08/18/2009	Programmable fuse with silicon germanium
7,544,576	06/09/2009	Diffusion barrier for nickel silicides in a semiconductor fabrication

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		process
7,535,060	05/19/2009	Charge storage structure formation in transistor with vertical channel region
7,517,741	04/14/2009	Single transistor memory cell with reduced recombination rates
7,510,956	03/31/2009	MOS device with multi-layer gate stack
7,456,055	11/25/2008	Process for forming an electronic device including semiconductor fins
7,442,621	10/28/2008	Semiconductor process for forming stress absorbent shallow trench isolation structures
7,442,590	10/28/2008	Method for forming a semiconductor device having a fin and structure thereof
7,435,639	10/14/2008	Dual surface SOI by lateral epitaxial overgrowth
7,402,476	07/22/2008	Method for forming an electronic device
7,371,677	05/13/2008	Laterally grown nanotubes and method of formation
7,364,970	04/29/2008	Method of making a multi-bit non-volatile memory (NVM) cell and structure
7,354,831	04/08/2008	Multi-channel transistor structure and method of making thereof
7,354,814	04/08/2008	Semiconductor process with first transistor types oriented in a first plane and second transistor types oriented in a second plane
7,339,241	03/04/2008	FinFET structure with contacts
7,312,129	12/25/2007	Method for producing two gates controlling the same channel
7,291,521	11/06/2007	Self-correcting suppression of threshold voltage variation in fully depleted transistors
7,288,448	10/30/2007	Method and apparatus for mobility enhancement in a semiconductor device
7,279,433	10/09/2007	Deposition and patterning of boron nitride nanotube ILD
7,271,069	09/18/2007	Semiconductor device having a plurality of different layers and method therefor
7,256,077	08/14/2007	Method for Removing a Semiconductor Layer
7,238,580	07/03/2007	Semiconductor fabrication process employing stress inducing source drain structures with graded impurity concentration
7,238,555	07/03/2007	Single transistor memory cell with reduced programming voltages
7,235,847	06/26/2007	Semiconductor device having a gate with a thin conductive layer
7,226,833	06/05/2007	Semiconductor Device Structure and Method Thereof
7,221,006	05/22/2007	GeOI Transistor with low junction current and low junction capacitance and method for making the same
EP1784854	05/16/2007	Method and Apparatus for Mobility Enhancement in a Semiconductor Device
7,217,667	05/15/2007	Processes for forming electronic devices including a semiconductor layer
WO2007047165	04/26/2007	Programmable Fuse with Silicon Germanium
7,205,202	04/17/2007	Semiconductor device and method for regional stress control
7,202,117	04/10/2007	Method of making a planar double- gated transistor
7,195,963	03/27/2007	Method for making a semiconductor structure using germanium
EP1751791	02/14/2007	Method for making a semiconductor structure using silicon germanium
7,166,897	01/23/2007	Method and apparatus for performance enhancement in an asymmetrical semiconductor device
7,163,903	01/16/2007	Method for making a semiconductor structure using silicon germanium

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EP1728274	12/06/2006	Method for forming a semiconductor device having a notched control electrode and a structure thereof
EP 1751791	03/14/2007	Method for making a semiconductor structure using silicon germanium
WO2006115588	11/02/2006	Semiconductor device and method for regional stress control
WO2006023219	03/02/2006	Method and apparatus for mobility enhancement in a semiconductor device
7,112,832	09/26/2006	Transistor having multiple channels
7,105,430	09/12/2006	Method for forming a semiconductor device having a notched control electrode and structure thereof
WO2006083401	08/10/2006	Method for making a planar double-gated transistor
EP1668691	06/14/2006	Method for forming a semiconductor device having isolation regions
WO2005104225	11/03/2005	Method for forming a semiconductor device having a notched control electrode and structure thereof
WO2005117101	12/08/2005	Method for making a semiconductor structure using silicon germanium
7,045,432	05/16/2006	Method for forming a semiconductor device with local semiconductor-on- insulator (SOI)
WO2006023183	03/02/2006	Method and apparatus for performance enhancement in an asymmetrical semiconductor device
7,037,795	05/02/2006	Low RC product transistors in SOI semiconductor process
7,029,980	04/18/2006	Method of manufacturing SOI template layer
WO2006001915	01/05/2006	Semiconductor Device with multiple semiconductor layers
WO2006023219	03/02/2006	Method and apparatus for mobility enhancement in a semiconductor device
WO2005076795	08/25/2005	Method for forming a semiconductor device with local semiconductor-on- insulator (SOI)
WO2005112094	11/24/2005	Method for making a semiconductor structure using silicon germanium
6,964,911	11/15/2005	Method for forming a semiconductor device having isolation regions
WO2005034186	04/14/2005	Method for forming a semiconductor device having isolation regions
6,921,700	07/26/2005	Method of forming a transistor having multiple channels
WO2005034230	04/14/2005	Semiconductor structure with different lattice constant materials and method for forming the same
6,831,350	12/14/2004	Semiconductor structure with different lattice constant materials and method for forming the same
6,573,160	06/03/2003	Method of recrystallizing an amorphous region of a semiconductor
6,433,382	08/13/2002	Split-gate vertically oriented EEPROM device and process
JP2000031139	01/28/2000	Method for arranging particle of specified species in solid and resulting structure
5,985,736	11/16/1999	Process for forming field isolation
5,741,736	04/21/1998	Process for forming a transistor with a nonuniformly doped channel
5,705,415	01/06/1998	Process for forming an electrically programmable read-only memory cell
EP730293		Process for fabricating a graded-channel MOS device
5,605,855	02/25/1997	Process for fabricating a graded-channel MOS device
JP8306925		Manufacture of semiconductor device
5,567,958	10/22/1996	High-performance thin-film transistor and SRAM memory cell

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JP8250715		Manufacture of semiconductor device
EP730293		Process for fabricating a graded-channel MOS device
5,545,575	08/13/1996	Method for manufacturing an insulated gate semiconductor device
5,539,216	07/23/1996	Monolithic semiconductor body with convex structure
5,506,161	04/09/1996	Method of manufacturing graded channels underneath the gate electrode extensions
5,432,118	07/11/1995	Process for forming field isolation
5,314,834	05/24/1994	Field effect transistor having a gate dielectric with variable thickness
5,235,203	08/10/1993	Insulated gate field effect transistor having vertically layered elevated source/drain structure
JP2114633	02/10/2004	Method of forming flat doped region
EP359852		Process for manufacturing shallow doped regions having a low layer resistivity in a silicon substrate

Pending Patents Published and to be issued

<u>Patent</u>	<u>Inventors</u>	<u>Description</u>
US2008/0182428	Tushar Merchant Marius Orlowski	Electronic Device including a layer of discontinuous storage elements and a process for forming the electronic device
US2007/0218628A1	Orlowski, Marius Venkatesan, Suresh	Electronic device including a semiconductor fin and a process for forming the electronic device
US2007/0218640A	Goktepedli, Sinan Demkov, Alexander Orlowski, Marius	Semiconductor Device having a Gate with a thin Conductive Layer
US2007/0212832A1	Orlowski, Marius	Method for Making a Multibit Transistor
US20070210338A1	Orlowski, Marius	Charge storage structure formation in transistor with vertical channel region
US20070176247A1	Liu, Chun-Li Orlowski, Marius Stoker, Mathew	MOS device with multi-layer gate stack
US20070176227A1	Liu, Chun-Li Merchant, Tushar Orlowski, Marius Stoker, Marius	MOS device with nano-crystal gate structure
US20070173024A1	Goktepedli, Sinan Hoefler, Alexander Orlowski, Marius	Method for producing two gates controlling the same channel
US20070166902A1	Orlowski, Marius Adetutu, Olubummi Stout, Philip	Method to control the gate sidewall profile by graded material composition
US2007/0161170A1	Marius, Orlowski James Burnett	Transistor with immersed contacts and methods of forming thereof
US2007/0158764A1	Marius Orlowski James Burnett	Electronic Device including a Fin-type Transistor Structure and a Process for Forming the Electronic Device
US20070148894A1	Marius Orlowski	Semiconductor Device and Method for Regional Stress

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WO2006/023219A2	Vance Adams Orlowski, Marius Venkatesan, Suresh	Control Method and Apparatus for Mobility Enhancement in a Semiconductor Device
WO2006/083401A3	Marius Orlowski	Method of Making A Planar Double- Gated Transistor
US20070096226A1	Liu, Chun Li Merchant, Tushar, P. Orlowski, Marius, K. Schaeffer, James, K. Stoker, Matthew, W.	MOSFET dielectric including a diffusion barrier
US20070077706A1	Orlowski, Marius K. Goktepli, Sinan	Method of Making a Multibit Non-Volatile Memory (NVM) Cell and Structure
US20070072334A1	Orlowski, Marius, K. Yu, Kathleen, C.	Semiconductor fabrication process employing spacer defined vias
US20070045735A1	Orlowski, Marius, K. Stephens, Tab, A	FinFET structure with contacts
US20070029586A1	Marius Orlowski	Multi-channel transistor structure and method of making thereof
US20070026593A1	Jawarani, Dharmesh Liu, Chun Li Orlowski, Marius	Diffusion barrier for nickel silicides in a semiconductor fabrication process
US20070001222A1	Orlowski, Marius Burnett, James	Single transistor memory cell with reduced recombination rates
US20070001162A1	Orlowski, Marius Burnett, James	Single transistor memory cell with reduced programming voltages
US20060286736A1	Orlowski, Marius Goolsby, Brian	Method for forming an electronic device
US7135379B2	Orlowski, Marius K. Burnett, James D.	Isolation trench perimeter implant for threshold voltage control
US20060240650A1	Orlowski, Marius Adams, Vance	Semiconductor device having a plurality of different layers and method therefor
US20060240629A1	Orlowski, Marius Shiho, Yasuhito	Self-correcting suppression of threshold voltage variation in fully depleted transistors
US20060240609A1	Orlowski, Marius Adams, Vance	Semiconductor device and method for regional stress control
US20060237746A1	Orlowski, Marius Goktepli, Sinan Liu, Chun Li	GeSOI transistor with low junction current and low junction capacitance and method for making the same
US20060194384A1	Venkatesan, Suresh Foisy, Mark Mendicino, Michael Orlowski, Marius	Semiconductor device with multiple semiconductor layers
US20060183288A1	Orlowski, Marius Vartanian, Victor	Processes for forming electronic devices including a semiconductor layer
US20060172468A1	Orlowski, Marius	Method of making a planar double-gated transistor

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US20060166492A1	Orlowski, Marius Adams, Vance Liu, Chun Li Stoker, Matthew	Semiconductor fabrication process employing stress inducing source drain structures with graded impurity concentration
US20060110892A1	Orlowski, Marius Foisy, Mark Adetutu, Olubunmi	Semiconductor process for forming stress absorbent shallow trench isolation structures
US20060094169A1	White, Ted Barr, Alexander Nguyen, Bich Yen, Orlowski, Marius Sadaka, Mariam Thean, Voon Yew	Semiconductor device structure and method therefor
US20060084235A1	Barr, Alexander Adetutu, Olubunmi Nguyen, Bich Yen Orlowski, Marius Sadaka, Mariam, Thean, Voon Yew White, Ted	Low RC product transistors in SOI semiconductor process
US20060068542A1	Orlowski, Marius Burnett, James	Isolation trench perimeter implant for threshold voltage control
US20060063392A1	Ventzek, Peter Junker, Kurt Orlowski, Marius	Deposition and patterning of boron nitride nanotube ILD
US20060060928A1	Goktepli, Sinan Demkov, Alexander Orlowski, Marius	Semiconductor device having a gate with a thin conductive layer
US20060046366A1	Orlowski, Marius Venkatesan, Suresh	Method and apparatus for mobility enhancement in a semiconductor device
US20060043498A1	Orlowski, Marius Adams, Vance Liu, Chun Li Winstead, Brian	Method and apparatus for performance enhancement in an asymmetrical semiconductor device
US20050275018A1	Venkatesan, Suresh Foisy, Mark Mendicino, Michael Orlowski, Marius	Semiconductor device with multiple semiconductor layers
US20050260816A1	Orlowski, Marius	Method for removing a semiconductor layer
US20050260807A1	Orlowski, Marius Liu, Chun Li Yeap, Choh Fei	Method for making a semiconductor structure using silicon germanium
US20050245092A1	Orlowski, Marius Barr, Alexander Sadaka, Mariam White, Ted	Method for making a semiconductor structure using silicon germanium

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US20050215008A1	Orlowski, Marius Burnett, James	Method for forming a semiconductor device having a notched control electrode and structure thereof
US20050170604A1	Orlowski, Marius Adetutu, Olubunmi Barr, Alexander	Method for forming a semiconductor device with local semiconductor-on-insulator (SOI)
US20050167650A1	Orlowski, Marius Mathew, Leo	Transistor having multiple channels
US20050070056A1	Liu, Chun Li Orlowski Marius K. Stoker Matthew W. Tobin Philip, J. Sadaka Mariam G. Barr Alexander L. Nguyen Bich Yen Thean, Voon Yew Thomas, Shawn, G. White, Ted, R.	SOI template layer
US20050064669A1	Orlowski, Marius K. Barr, Alexander L.	Method for forming a semiconductor device having isolation regions
US20050023619A1	Orlowski, Marius, K. Mathew, Leo	Method of forming a transistor having multiple channels and structure thereof
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Publications

- Over 230 publications in scientific journals and conference proceedings
- Physics Letters, IEEE Electron Device Letters, Lettere al Nuovo Cimento, Physical Review, IEEE transactions on Electron Devices, Journal of Applied Physics, phys. stat. sol (b), Microelectronic Engineering, Nuclear Physics, Journal of Electrochemical Society, Solid State Electronics, Zeitschrift fuer Physics, Helvetica Acta, Journal of Low temperature Physics, Journal de Physique, etc.) (a nearly complete list of publications is attached, non-English language publications not listed)
- First author on 84 publications
- Invited/keynote talks at premier conferences: Electrochemical Society Conference (2006), Int; Rapid Thermal Processing Conference (2005), Electrochemical Society Conference (2003), Nano Giga Challenges in Microelectronics (2002), Int. Symp. On Integrated Ferroelectrics (2000), International Electron Meeting (1994), Int. Conference on Simulation of Semiconductor Devices and Processes (1991), Electronics Materials Conference (1990), International Electron Device Meeting (1990), International Workshop on Process and Device Simulation (1989). Electrochemical Society Conference (1994) semiconductor technology (International Electron Device Meeting, Electrochemical Society Conference, SISPAD, NUPAD, NASECODE, ITEF, Electronic Materials Conference and several international workshops)
- Panelist at several conferences (IEDM, SOI Conference, SISPAD, SRC, and several international workshops)
- Co-Editor – Symposium Proceedings, “Silicon Front-End Junction Formation – Physics and Technology”, Materials Research Society, vol. 810, 2004
- Interview with Semiconductor International (L. Peters) “Double Gates Prompt Transistor Revolutions” March Issue 2005
- Published interviews with Japanese and Chinese trade publications

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