Aspects of data acquisition system design

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Analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) play an important role in the design of data acquisition systems. ADCs are used to convert analog signals like the output from a temperature transducer, a radio receiver or a video camera into digital signals for processing. Conversely, DACs are used to convert digital signals back to analog signals. For example, the DAC accepts a digital video signal and outputs analog video to drive a monitor CRT, video amplifier or LCD monitor display. Convenience, cost, power dissipation, resolution, speed, supply voltage and ease of use drive the selection of a particular ADC/DAC. Ideally, designers will select an appropriate low-power serial or parallel input CMOS DAC, apply data and control signals to the device and have differential or single-ended analog outputs. Similarly, the requirements for low-power CMOS ADCs include being able to connect single-ended or differential input and control signals to the device and have accurate digital data at the output. It turns out that this is a non-trivial issue because of the wide range of input signals.

Signal processing challenges

A composite video signal has negative horizontal and vertical synchronization signals. The signal level must be shifted before applying it to the input of a CMOS ADC operating with a +5-V AVDD supply if the intent is to digitize the video and synchronization signals. In radio communication systems the analog input signal is buried deep in noise, and interference signals from an adjacent channels can interfere with the in-band RF signal. To help maintain signal quality, modern radio communications systems use a digital receiver to process the RF input. A typical digital receiver circuit chain (see Figure 1) consists of an antenna, a low-noise amplifier (LNA), RF unit, bandpass filter, an ADC, a digital mixer, a decimating low-pass filter, a digital signal processor (DSP) and a DAC connected to an audio amplifier. The ADC is used to bring the RF signal into the digital domain for processing by the DSP. This application note provides a functional specification for designing analog-to-digital converter data acquisition systems.

Common ADC architectures

The common ADC architectures include successive approximation register (SAR), dual-slope, sigma-delta, flash, semi-flash and pipeline.

SAR and dual-slope

The SAR and dual-slope architectures are mainly used in applications requiring high resolution (10 to 22 bits) and low conversion speed in the range of 100 sps (samples per second) to 2 Msps. The SAR converter is the most popular general-purpose ADC and is used in low-to-medium frequency time domain applications. The key to SAR architecture is that it is based on a single comparator. To achieve *N* bits of resolution, a successive approximation converter must perform *N* comparator operations, each stored sequentially in the architecture's register. A successive approximation ADC with 12 bits of resolution would execute 12 comparisons on each input signal. An ADC based on a single comparator leads to a very small die size and low power consumption, however, SAR sample

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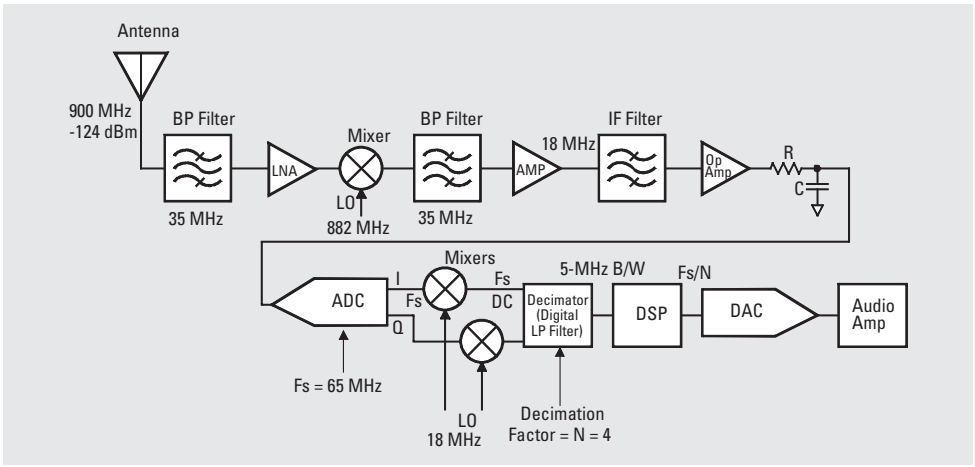
Figure 1. Simplified block diagram of a digital receiver



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rates are inversely proportional to resolution because the conversion method requires one clock cycle to produce each bit of resolution in the output data.

Sigma-delta

The sigma-delta ADC architecture is capable of much higher resolution than the SAR. The typical range is 16 to 24 bits. The tradeoff comes in the form of slower sampling speeds. The sigma delta architecture's sampling speed is limited to approximately 100 ksps. Sigma-delta converters use a technique called oversampling that is based on the theory that a very fast, low-resolution converter can be used to take a large number of samples on an analog signal. The outputs from this oversampling process are then combined into groups, and the groups are averaged using a digital filter like an accumulator-adder. This averaging operation can increase the accuracy of the conversion as long as the input signal does not vary any faster than the sampling rate. This process also eliminates any in-band noise present in the ADC by spreading the noise across the entire sampling frequency band.

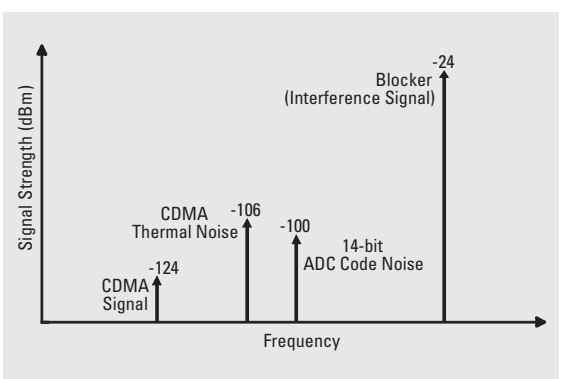
Flash

Flash ADCs are very fast with typical sampling speed ranging from 20 Msps to 800 Msps, with 6- to 8-bit resolution; however, the device power consumption and input capacitance (12 to 30 pF) are high compared to a SAR. The input capacitance issue makes it necessary to drive the flash ADC input with an op amp with very low output impedance. Flash ADCs perform multiple word-at-a-time conversions in parallel. The input signal is connected to a bank of fast comparators. For a flash converter to reach an effective resolution of N bits, the flash architecture must incorporate $2N$-1 comparators. The input capacitance is also very high due to the $2N$-1 comparators in parallel.

Semi-flash

To achieve higher resolutions in the range of 10 to12 bits, a multi-step flash or semi-flash architecture has been developed. This architecture divides the input signal range into a number of sub-ranges through the use of banks of comparators, much like the flash architecture.

Figure 2. CDMA signal and noise power relative to the blocker



Pipeline

Pipeline ADCs are used chiefly for medium- to high-speed conversion in the range of 1 to 80 million samples per second, with resolutions of 8 to 16 bits. A pipeline ADC is made up of n stages + n sampler. Each stage carries out an operation on the input sample and provides the output for the following sampler. Each stage consists of an SHA, an ADC, a DAC, a subtractor and an amplifier. A topic that has received much attention in the last few years is the use of high-speed pipeline ADCs for IF sampling in the implementation of software radio.

System requirements

The starting point for an electronic system design is the specification. Assume that the goal is to process the following code-division multiple-access (CDMA) baseband IF signal:

- 100-dB blocker at 250-kHz at the edge of the pass band
- 4 to 5 bits of resolution in the baseband—translates to an 80-dB spurious-free dynamic range (SFDR)
- An IF signal of 18 MHz (second harmonic from IF at 36 MHz)
- 6- to 12-dB attenuation of second harmonic from op amp
- The digital downconverter has a process gain of 22.4 dB
- The in-band thermal noise power at 25°C is approximately –98.4 dBm
- The sampling rate is 65 MHz
- A radio noise figure of 2 to 4 dB
- An antenna noise bandwidth of 35 MHz
- Eb/No = 5 dB

Selecting the data converter

The in-band thermal noise power

$$Gn = kTB = 1.38 \times 10^{-23} \times 300 \times 35 \times 10^{6}$$

$$= -128.4 \text{ dB or} - 98.4 \text{ dBm}$$

where

k = Boltzmann's constant, 1.38×10^{-23} (J/K),
T = temperature (K),
T(K) = T(°C) + 273.15 and
B = equivalent noise bandwidth of the system (Hz).

Figure 2 shows a representation of the power relative to the blocker.

From the specification and Figure 2 it is clear that the blocker (in-band interference signal) dominates the signal power of –124 dBm. For a typical converter full-scale (FS) input of 2Vp-p the RMS voltage required at the converter input is –3 dB. The total signal power is approximately equal to the blocker power component (–3 dB). Relating all other power components to the blocker power makes a useful simplification. Hence, the thermal noise is –77.4 dB (–98.4 dBm + 21.0 dBm) down from the blocker. The radio noise is introduced by adding the radio noise figure of +2 dB to the thermal noise = –75.4 dB. The thermal noise + the radio noise is reduced by the radio filter and decimating low-pass filter by an amount

= (baseband output B/W)÷(antenna input B/W)
= $5 \times 10^{6} \div 35 \times 10^{6}$
= 0.143
= –8.45 dB.

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The system thermal noise becomes

–75.4 dB – 8.45 dB – 3 dB = –86.85 dB.

As a first cut, use a 14-bit A/D converter with a signal-to-noise ratio (SNR) relative to the received signal power of 76 dB, and the digital downconverter and low-pass filter will reduce the ADC noise by a factor

= (baseband output B/W)÷(A/D converter output B/W)
$= 5 \times 10^6 \div (35 \times 10^6 \div 2)$
= 5 ÷ 32.5
= 0.154
= –8.13 dB.

Therefore, the new dB down for the ADC is

–76 dB – 8.13 dB – 3 dB = –87.13 dB.*

The total noise

= thermal noise + ADC code noise = –84 dB.

The in-band signal power level relative to –3 dB (full-scale) = –103 dB. The signal-to-noise ratio can be determined from

SNR = –103 dB + 84 dB = –19 dB.

The process gain for Figure 1 is 256 chips/bit or 24 dB. In such a case

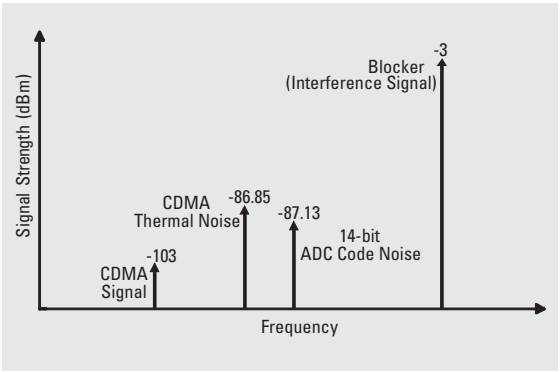
Eb/No = 24 – 19 = 5 dB.

The calculated converter noise is close to the system thermal noise; therefore, a 14-bit A/D converter with a SNR = 76 dB, SFDR = 100 dB, and a sampling rate of 65 Msps is a good choice. Figure 3 shows thermal noise contribution to the band-limited baseband noise.

In the given example of the ADC dynamic performance specifications, how well the pipeline ADC is able to digitize a high-frequency signal is the key for frequency domain applications. Other important dynamic specifications are the signal-to-noise ratio with distortion (SINAD) and effective number of bits (ENOB). Generally, designers should consider these and other performance characteristics such as the type of interface the device presents to the DSP before deciding on the ADC. New CMOS data converters are eliminating many of the compromises designers have faced and some of these devices are able to operate on lower voltages and still provide high throughput and resolution. For example, one such device is the TI THS1265, with12 bits of resolution and a sampling rate of 65 Msps.

*The theoretical SNR of a converter = n bits × 6.02 + 1.76 dB.

Figure 3. CDMA signal and ADC thermal noise contribution to the baseband noise



Interfacing the data converter

Figure 1 illustrates a conventional digital receiver.

Signal conditioning op amp selection

In the type of application shown in Figure 1, the op amps perform the critical function of conditioning signals. The designer must be careful that the op amp does not introduce any additional electrical noise and distortion into the system. As was the case with data converters, a lower voltage level reduces the effective speed of an op amp. This adversely effects the device's output signal slew rate, bandwidth, the settling times and the maximum value of ADCs input capacitance the op amp can drive. An op amp with unity gain 3-dB bandwidth of 450 MHz, SFDR range of 100 to 110 dB, SNR of 90 dB, THD (total harmonic distortion) of –95 dB, slew rate of 1500 V/µs and 40-ns settling time would be a good choice for driving 3 to 15 pF of converter input capacitance. The higher an op amp's slew rate (SR = 2piVpBw), the more accurately the device's output signal will conform to its input signal. An op amp with a fast slew rate means that after a signal transition from high to low or low to high, the signal will transition into its new state quickly with little noise-generating signal bounce. A fast settling time reduces signal bounce following a transition and limits any ringing in the signal. The op amp bandwidth affects the signal phase shift through of the device. The first-order low-pass filter at the output of the op amp is used to attenuate the 18-MHz IF signal second harmonic component by 8 dB. The filter's 3-dB cutoff frequency is set to 20 MHz.

Issues of board layout

Limiting the electrical noise as well as the electromagnetic interference (EMI) on the analog voltage plane of a data acquisition system is always important because ADCs use the supply voltage as a reference point for converting analog waveforms into digital signals. Electrical noise can interfere with the supply voltage and perturb the ADC's reference voltage. One common design mistake is failing to isolate the analog voltage plane from the digital plane. When this happens, the voltage fluctuations in the digital plane can couple to the analog plane and interfere with the accuracy and performance of the system's ADCs. ADCs operate most efficiently from a very clean, steady power supply.

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