

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND WESTERN DIGITAL
TECHNOLOGIES, INC.,
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00515
U.S. Patent No. 9,183,085

**PATENT OWNER PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107(a)**

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Patent Trial and Appeal Board
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I. INTRODUCTION

The Board should deny institution of *inter partes* review of the challenged claims of U.S. Patent No. 9,183,085 (“the ’085 patent”) because Petitioners fail to demonstrate a reasonable likelihood that the Li-Cideciyan combination discloses or renders obvious key elements of independent claims 1, 15, and 24. Petitioners’ invalidity challenges are conclusory, fail to explain how relevant claim terms should be construed, and are contrary to express teachings in the art. Compounding these deficiencies, Dr. Dolecek’s opinions supporting the Petition’s arguments for these elements are conclusory or merely repeat Petitioners’ arguments, and thus add no probative value over Petitioners’ attorney argument. At bottom, the merits of Petitioners’ invalidity challenges are weak and the Petition should be denied.

II. THE ’085 PATENT

A. Summary

The ’085 patent generally describes a flash memory system that selects between multiple error correction coding (ECC) schemes, referred to as “gears.” EX1001, 5:39-41. The specification describes a “gear” as “a set of parameter(s) specifying an error correction coding scheme, including one or more of the payload capacity, the type and parameters of each component code, the interleaving scheme, and parameters used for determining whether the gear is appropriate for a particular situation.” EX1001, 20:18-23. Gears may vary in ECC strength and data payload capacity, where stronger ECC schemes allocate more parity bits. EX1001,

4:18-36. In one embodiment, the flash memory system selects among these gears based on a bit error rate (BER) for a region that includes a fixed number of flash memory pages or integer fractions thereof. EX1001, 4:38-41. The region may contain both the data payload and associated primary and secondary ECC parity symbols, enabling multi-level error correction. EX1001, 6:30-46. The flash memory system can simultaneously read pages within the region, allowing efficient determination of the BER across the region. EX1001, 19:58-61. It then compares the determined BER to one or more predetermined thresholds to select an appropriate gear for the region, thereby balancing error correction strength and read latency. EX1001, 4:28-30.

B. Level of Skill in the Art

For the purposes of this preliminary response, Patent Owner applies Petitioners' proffered level of skill in the art with a caveat regarding the last sentence:

A Person of Ordinary Skill in The Art ("POSITA") as of May 22, 2012[,] would have had a working knowledge of the flash memory system art, including flash memories, memory controllers, and ECC art as applied to flash memory systems that is pertinent to the '085 patent. A POSITA would have had a bachelor's degree in electrical engineering, or an equivalent, and approximately two years of professional experience relating to the field of flash memory systems, including ECC technologies as applied to flash memory systems. Lack

of professional experience can be remedied by additional education,
and vice versa.

Pet., 9. To the extent the last sentence means that additional education could completely supplant experience, Patent Owner disagrees. A POSITA would be a professional with active work experience in the field of memory technologies, including at least some hands-on experience in that domain.

C. Claim Construction

Claim terms need only be construed to the extent necessary to resolve the controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Because none of the issues in this preliminary response turn on the construction of a claim term, Patent Owner takes no position at this time.

III. PETITIONERS FAIL TO DEMONSTRATE A REASONABLE LIKELIHOOD THE CHALLENGED CLAIMS WERE OBVIOUS.

Petitioners present the following Grounds of Unpatentability:

Grounds	Claims	Basis
#1	1-2, 4-5, 14-17, 22-25, 29-33	Obvious under §103 over Li and Cideciyan
#2	1-2, 4-5, 14-17, 22-25, 29-33	Obvious under §103 over Li, Cideciyan, and Frost
#3	6-7, and 18	Obvious under §103 over Li, Cideciyan, and Leung
#4	6-7, and 18	Obvious under §103 over Li, Cideciyan, Frost, and Leung

Pet., 12.

The Board should deny institution because Petitioners fail to demonstrate a reasonable likelihood that the Li-Cideciyan and Li-Cideciyan-Frost combinations disclose or render obvious at least two key claims elements of independent claims 1, 15, and 24. Specifically, Petitioners fail to demonstrate that: (A) Li teaches a region comprising a “fixed number” of two or more flash memory pages or integer fractions thereof, as recited in claim element [1.1.1]; and (B) the Li-Cideciyan combination renders obvious claim element [1.2.2]. Petitioners rely on Frost in Ground 2 to address only the requirement of element [1.1.1] that pages “can be read simultaneously,” Pet., 76-80, and thus Ground 2 rises and falls with Ground 1 with respect to the arguments below.

A. Petitioners fail to demonstrate that Li teaches a region comprising a “fixed number” of two or more flash memory pages or integer fractions thereof, as recited in claim element [1.1.1].

Claim element [1.1.1] requires “a region” that “compris[es] a *fixed number of two or more flash memory pages* or integer fractions thereof.”¹ Petitioners map Li’s “portion” to the claimed “region,” Pet., 17-19 (subsection (a)), and allege that Li teaches that the portion comprises a “fixed number” of multiple pages, Pet., 19 (subsection (b)). Citing paragraphs 38, 97, and 99 of Li, Petitioners’ posit that Li’s portion “is fixed by the ‘predetermined amount of information’ of the portion and

¹ Emphasis added unless otherwise stated.

the predetermined fixed size for each page.” Pet., 19. As best understood, Petitioners’ theory is that (i) a portion has a fixed size, (ii) a page has a fixed size, and (iii) because a portion may be comprised of multiple pages, any such portion must comprise a fixed number of two or more pages.

This theory fails at least because Petitioners fail to show that Li’s pages have a fixed size. Pet., 19 (cursory analysis with no showing regarding pages of fixed size). They do not. Rather, Li teaches that its pages can be operated differently depending on conditions like raw bit error rate (BER) or the lifetime (age) of the memory system. Specifically, Li teaches that a page may be operated as either Multi-Level Cell (MLC) or Single-Level Cell (SLC). EX1005, ¶19 (“For another example, during an operating period of a page of a flash memory, the page is operated as an MLC page, and then during a subsequent operating period, the page is operated as an SLC page.”); ¶103 (“For example, when a raw BER exceeds a threshold, a portion (such as a page) of flash memory previously operated as an MLC page is thereafter operated as an SLC page (such as by operating the page as a ‘lower only’ page). For another example, during an early part of a lifetime of a portion of a flash memory, the portion is operated as an MLC portion, and during a later part of the lifetime, the portion is operated as an SLC portion.”). Li explains that “[i]n MLC technology, each bit cell is enabled to store multiple bits of information,” whereas “[i]n SLC technology, each bit cell (e.g. floating gate

transistor) is enabled to store one bit of information.” EX1005, ¶15. Thus, the size of a page in Li (the amount of information it can store) varies (it is not fixed), storing more information when operated as an MLC page than as an SLC page. And Petitioners’ theory fails because it hinges on Li’s portion being comprised of pages of fixed size.

Petitioners cite paragraphs 79-80 of Dr. Dolecek’s declaration as allegedly supporting their argument. Pet., 19. Dr. Dolecek relies only on paragraphs 97 and 99 of Li, opining (without support) that “[t]ypically a flash page has a fixed size.” EX1003, ¶79. But she fails to consider Li’s teachings that its pages are operated in different modes having different storage sizes (are not fixed). *See, e.g.*, EX1005, ¶¶19, 103. So even if flash pages typically have fixed size (which Patent Owner does not concede), they do not in Li. Dr. Dolecek’s opinion is inconsistent with Li’s express teachings, and thus should not be credited.

Accordingly, Petitioners fail to demonstrate that Li teaches a region comprising a “fixed number” of two or more flash memory pages or integer fractions thereof, as recited in claim element [1.1.1]. Petitioners refer back to their analysis of claim 1 to address analogous elements of independent claims 15 and 24, and thus Petitioners’ invalidity challenge to claims 15 and 24 likewise fail. Pet., 60-61, 67-68.

B. Petitioners fail to demonstrate that the Li-Cideciyan combination renders obvious claim element [1.2.2].

Claim element [1.2.2] recites two “wherein” clauses: (1) “wherein the first gear has a different *data payload size* and correction capability than the second gear” and (2) “wherein the *amount of memory space allocated for the storage of data payload* within the region varies between the first gear and the second gear to accommodate a varying number of parity symbols between the first gear and the second gear.” As emphasized above, the first wherein clause refers to (among other things) the “data payload size” (the “data payload size requirement”); whereas the second wherein clause refers to the “amount of memory space allocated for the storage of data payload” (the “memory space allocation requirement”).

Petitioners address claim element [1.2.2.] in three points (“First,” “Second, “Third”) spanning pages 46-50 of the Petition. Petitioners’ first point reiterates their analysis for claim element [1.2.1].a, alleging that the Li-Cideciyan combination renders obvious the claimed first and second “gears.” Pet., 46-47. Petitioners’ second point addresses the first wherein clause, alleging it is taught by claim 2 of Li. Pet., 47. In their third point, Petitioners allege that claims 3 and 4 of Li teach both (i) the data payload size requirement of the first wherein clause as well as (ii) the second wherein clause. Pet., 48-50. Without conceding that the art teaches the first and second “gears” of claim element [1.2.1].a, Patent Owner focuses on the defects in Petitioners’ arguments for the first and second wherein

clauses of claim element [1.2.2], i.e., Petitioners’ second and third points.

Regarding the first wherein clause of claim element [1.2.2], Petitioners allege that claim 2 of Li teaches first and second gears that have different (1) data payload sizes and (2) correction capabilities. Pet., 47. But claim 2 of Li refers only to the “number of error correcting bits to store in the portion” for different error correcting codes; it does not mention different data payload sizes:

2. The system of claim 1, wherein encoding according to a **first** one of the error correcting codes results in a number of **error correcting bits** to **store in the portion** that is **less than** when encoding according to a **second** one of the error correcting codes.

Pet., 47 (annotating claim 2 of Li, EX1005).

Petitioners provide no explanation how Li’s claim language related to the number of error correcting bits teaches or suggests different “data payload sizes,” as claimed. *See In re Magnum Oil Tools International, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements.”). Petitioners’ expert, Dr. Doleck, repeats Petitioners’ conclusory analysis (or vice versa), EX1003, ¶139, and thus her opinion provides no probative value to Petitioners’ position on the first wherein clause of claim element [1.2.2], *TQ Delta, LLC v. Cisco Systems, Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019) (“[C]onclusory expert testimony is inadequate to

support an obviousness determination”); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-17 (P.T.A.B. Aug. 24, 2022) (precedential) (a declaration is entitled to little weight when it contains an exact restatement of the petition’s unsupported, conclusory assertions without any additional supporting evidence or reasoning).

Accordingly, Petitioners’ second point fails to demonstrate that Li teaches first and second gears that have different “data payload size[s].”

Turning to their third point, Petitioners allege that claims 3 and 4 of Li teach both the data payload size requirement of the first wherein clause *and* the memory space allocation requirement of the second wherein clause. Pet., 49-50.

Paraphrasing, claims 3 and 4 of Li require that the number of bits of a portion of memory that are used to store user data are increased (claim 3) or decreased (claim 4) depending on the error correcting code (ECC) scheme that is used. Pet., 48-49 (reproducing and annotating claims 3 and 4 of Li). Petitioners argue that this increase or decrease of the number of bits used for user data teach both the data payload size requirement of the first wherein clause and the memory space allocation requirement of the second clause. *Id.*

Petitioners’ argument fails because claim element [1.2.2] recites both the data payload size requirement and the memory space allocation requirement.

“[U]se of both terms in close proximity in the same claim gives rise to an inference

that a different meaning should be assigned to each.” *Bancorp Services, LLC v. Hartford Life Ins. Co.*, 359 F.3d 1367, 1373 (Fed. Cir. 2004). Petitioners, who bear the burden to explain how the challenged claims should be construed, 37 C.F.R. § 42.104(b)(3), do not attempt to construe these terms or present any argument to rebut the inference that they carry different meanings, *see* Pet., 10-11 (addressing claim construction). Rather, Petitioners treat (i) the size of a data payload and (ii) the amount of memory allocated to store a data payload as the same without explaining why that is appropriate based on the patent and the current record. At bottom, Petitioners arguments are mere conclusory assertions that certain claims (not even the disclosure) of the Li reference teach the disputed features. Dr. Dolecek again repeats Petitioners’ conclusory arguments (or vice versa) without any additional reasoning or explanation. EX1003, ¶¶141-145. Such conclusory arguments are insufficient to demonstrate obviousness, and should be rejected. *Magnum Oil Tools*, 829 F.3d at 1380; *TQ Delta*, 942 F.3d at 1352.

Petitioners’ third point thus fails to demonstrate that Li teaches both the data payload size and the memory space allocation requirements. Accordingly, the Board should deny institution because Petitioners fail to demonstrate that the Li-Cideciyan combination renders obvious claim element [1.2.2]. Petitioners refer back to their analysis of claim 1 to address analogous elements of independent claims 15 and 24, and thus Petitioners’ invalidity challenge to claims 15 and 24

likewise fail. Pet., 62, 69.

IV. CONCLUSION

The Petition fails to show a reasonable likelihood that any of the challenged claims is unpatentable as obvious in view of the cited art and, therefore, the Board should deny institution.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

1. This Patent Owner Preliminary Response complies with the type-volume limitation of 14,000 words, comprising 2,283 words, excluding the parts exempted by 37 C.F.R. § 42.24(a)(1).

2. This Patent Owner Preliminary Response complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman font.

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