

Declaration and Power of Attorney

IDT-2730C-UT

My residence/post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY
CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE**

the specification of which is attached hereto.

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION	FILING DATE
61/374242	8/16/10

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) listed below to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Kenneth Glass, Reg. No. 42,587
Randall Krause, Reg. No. 53,158
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Greg Warder, Reg. No. 50,208
Jaya Nair, Reg. No. 46,454

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(408) 354-4448

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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03/21/11
Date

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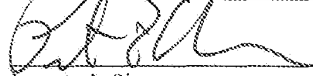
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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3/21/2011

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SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE
MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims benefit of United States provisional patent application serial number 61/374,242 filed August 16, 2010 and entitled “Non Volatile Memory Host Controller Interface Device,” which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] Fault-tolerant computing systems often employ data storage techniques for recovery of data lost as a result of a disk drive failure. These data storage techniques often involve a redundant array of independent disks (RAID). In some of these data storage techniques, a disk drive controller performs a data stripe operation by dividing data into data blocks and generating parity data based on the data blocks. In this way, the disk drive controller generates redundancy data based on the data blocks. The disk drive controller distributes the data blocks and the parity data among an array of disk drives. In event of a hardware failure of a disk drive in the array, the disk drive controller reconstructs the data in the failed disk drive based on the data stored in the other disk drives of the array, and stores the reconstructed data into a replacement disk drive.

[0003] Because generation of parity data in a RAID operation is often a computationally intensive task, some types of disk drive controllers include a dedicated processor for generating parity data. In these types of disk drive controllers, the dedicated processor stores data blocks into individual data buffers of the disk drive controller, executes computing instructions to generate parity data, and stores the parity data into yet another data

buffer. Although use of a dedicated processor for generating parity data generally improves throughput of a disk drive controller, generation of parity data is still a performance bottleneck in many disk drive controllers. Moreover, the data buffers consume a considerable amount of area and power in integrated circuit implementations of the disk drive controller.

SUMMARY

[0004] In various embodiments, a nonvolatile memory controller performs a data stripe operation by processing a collection of commands. The collection of commands includes data update commands and a parity write command. The nonvolatile memory controller includes a number of command processing units, each of which receives a command in the collection of commands. Each of the command processing units receiving a data update command requests a data block from a controller memory, receives the data block from the controller memory through a data path in response to the request, and writes the data block to a nonvolatile memory device.

[0005] The parity calculator receives the data blocks as a sequence of data blocks through the same data path from which the command processing units receive the data blocks. The parity calculator generates a parity block by storing a first data block of the sequence of data blocks into a page frame and updating the data block stored in the page frame with each remaining data block in the sequence of data blocks. In this way, the parity calculator generates the parity block on the fly as the command processing units are receiving the data blocks for the data stripe operation.

[0006] Because the nonvolatile memory controller performs a data stripe operation by using a plurality of command processing units, the nonvolatile memory controller performs a data stripe operation more quickly than other methods using only a single dedicated processor to perform a data stripe operation. Moreover, because the parity calculator generates the parity block in the page frame as the parity calculator is receiving the data blocks for the data stripe operation, the parity calculator need not store all the data blocks of the data stripe at the same

time when generating a parity block. As a result, the nonvolatile memory controller consumes less power and area than other nonvolatile memory controllers in which data blocks of a data stripe operation are stored in individual data buffers when computing a parity block.

[0007] A nonvolatile memory controller, in accordance with one embodiment, performs a data stripe operation on block blocks. The nonvolatile memory controller includes command processing units and a parity calculator. The parity calculator is coupled to the command processing units. Each of the command processing units is configured to receive a command of a plurality of commands for performing the data stripe operation. The commands include data update commands and a parity write command. Each command processing unit receiving a data update command is configured to request a data block of the data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device. The parity calculator is configured to receive the data blocks and generate a parity block based on the data blocks. The command processing unit receiving the parity write command is configured to write the parity block to a nonvolatile memory based on the parity write command.

[0008] A nonvolatile memory controller, in accordance with one embodiment, includes a command distribution unit, command processing units, and a parity calculator. The command processing units are coupled to the command distribution unit and the parity calculator. The command distribution unit is configured to receive commands for performing a data stripe operation on data blocks. The commands include data update commands and a parity write command. The command distribution unit is further configured to distribute the data update commands among at least some of the command processing units. Each of the

command processing units receiving a data update command is configured to request a data block based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device. The parity calculator includes a context memory including a page frame. Moreover, the parity calculator is configured to receive the data blocks as a sequence of data blocks. Further, the parity calculator is configured to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks. The command distribution unit is further configured to determine generation of the parity block is complete and distribute the parity write command to a command processing unit in response to determining the parity block is complete. The command processing unit receiving the parity write command is configured to write the parity block into the nonvolatile memory device.

[0009] A method for generating parity data, in accordance with one embodiment, includes distributing commands for performing a data stripe operation among a number of command processing units in the nonvolatile memory controller. The commands include a number of data update commands and a parity write command. The method further includes generating data requests by the command processing units based on data update commands, and receiving data blocks at the command processing units and at a parity calculator of the nonvolatile memory controller in response to the data requests. Additionally, the method includes writing the data blocks to nonvolatile memory devices by the command processing units. The method also includes generating a parity block in a page frame of a context memory based on the data blocks. Further, the method includes determining generation of the parity

block is complete and writing the parity block to a nonvolatile memory device based on the parity write command after generation of the parity block is complete. Because the method performs a data stripe operation by using a plurality of command processing units, the method performs a data stripe operation more quickly than other methods using only a single dedicated processor to generate parity data.

BRIEF DESCRIPTION OF THE DRAWINGS

[00010] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.

[00011] FIG. 1 is a block diagram of a computing system, in accordance with an embodiment of the present invention.

[00012] FIG. 2 is a block diagram of a network module, in accordance with an embodiment of the present invention.

[00013] FIG. 3 is a block diagram of a control module, in accordance with an embodiment of the present invention.

[00014] FIG. 4 is a block diagram of a storage controller, in accordance with an embodiment of the present invention.

[00015] FIG. 5 is a block diagram of a context module, in accordance with an embodiment of the present invention.

[00016] FIG. 6 is a block diagram of a parity calculator, in accordance with an embodiment of the present invention.

[00017] FIG. 7 is a block diagram of a processing unit, in accordance with an embodiment of the present invention.

[00018] FIG. 8 is a block diagram of a nonvolatile memory device, in accordance with an embodiment of the present invention;

[00019] FIG. 9 is a flow chart of a portion of a method of generating a parity block, in accordance with an embodiment of the present invention.

[00020] FIG. 10 is a flow chart of a portion of a method of generating a parity block, in accordance with an embodiment of the present invention.

[00021] FIG. 11 is a flow chart of a portion of a method of generating a parity block, in accordance with an embodiment of the present invention.

[00022] FIG. 12 is a flow chart of a portion of a method of generating a parity block, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[00023] In various embodiments, a nonvolatile memory controller includes command processing units and a parity calculator for performing a data stripe operation. Each of the command processing units independently requests a data block from a controller memory, receives the data block from the controller memory through a data path in response to the request, and writes the data block to a nonvolatile memory device. The parity calculator receives the data blocks as a sequence of data blocks through the same data path from which the command processing units receive the data blocks. The parity calculator generates a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each remaining data block in the sequence of data blocks in response to receiving the data block. In this way, the parity calculator generates the parity block on the fly as the command processing units and the parity calculator are receiving the data blocks for the data stripe operation.

[00024] FIG. 1 illustrates a computing system 100, in accordance with an embodiment of the present invention. The computing system 100 includes a host processing unit 110, a communication network 115, a nonvolatile memory controller 105, and a nonvolatile memory device 140. The communication network 115 is coupled (e.g., connected) to the host processing unit 110 and the nonvolatile memory controller 105. Additionally, the nonvolatile memory controller 105 is coupled (e.g., connected) to the nonvolatile memory device 140. In various embodiments, the nonvolatile memory device 140 is a flash storage device and the nonvolatile memory controller 105 is a flash controller.

[00025] The communication network 115 facilitates communication between the host processing unit 110 and the nonvolatile memory controller 105. For example, the communication network 115 may be a packet communication network, such as a Peripheral Component Interconnect Express (PCIe) network. The nonvolatile memory controller 105 manages data stored in the nonvolatile memory device 140 and communicates with the host processing unit 110 through the communication network 115 for transferring data between the host processing unit 110 and the nonvolatile memory device 140. In various embodiments, the nonvolatile memory controller 105 processes nonvolatile memory commands generated by the host processing unit 110 for controlling operation of the nonvolatile memory controller 105. In some embodiments, the host processing unit 110 generates Non-Volatile Memory Express (NVMe) commands and the nonvolatile memory controller 105 processes the (NVMe) commands to manage operation of the nonvolatile memory controller 105.

[00026] In various embodiments, the nonvolatile memory controller 105 includes a host controller interface 120, a network module 125, a control module 130, a processor module 145, and a controller memory 160. The network module 125 is coupled (e.g., connected) to the host controller interface 120, the control module 130, the processor module 145, and the controller memory 160. Additionally, the host controller interface 120 is coupled (e.g., connected) to the communication network 115, and the control module 130 is coupled (e.g., connected) to the nonvolatile memory device 140. Furthermore, the processor module 145 includes processors 150 coupled (e.g., connected) to the network module 125. In these embodiments, each of the host controller interface 120, the control module 130, the processors 150, and the controller memory 160 is a functional unit of the nonvolatile memory controller 105.

[00027] In various embodiments, each of the host controller interface 120, the control module 130, the processor module 145, and the controller memory 160 is source node or a destination node of the nonvolatile memory controller 105. In this way, each functional unit of the nonvolatile memory controller 105 may be a source node or a destination node. In some embodiments, one or more of the host controller interface 120, the control module 130, the processor module 145, and the controller memory 160 is both a source node and a destination node of the nonvolatile memory controller 105. In this way, a functional unit of the nonvolatile memory controller 105 may be both a source node and a destination node.

[00028] The host controller interface 120 facilitates communication between the communication network 115 and the functional units of the nonvolatile memory controller 105 through the network module 125. The control module 130 manages data in the nonvolatile memory device 140. For example, the control module 130 may read data from the nonvolatile memory device 140 and write data into the nonvolatile memory device 140.

[00029] The controller memory 160 stores data being transferred from the host processing unit 110 to the nonvolatile memory device 140. Additionally, the controller memory 160 stores data being transferred from the nonvolatile memory device 140 to the host processing unit 110. In this way, the controller memory 160 is an intermediate storage location for temporarily storing data being transferred between the host processing unit 110 and the nonvolatile memory device 140. In various embodiments, the controller memory 160 includes a random access memory (RAM), such as a static random access memory (SRAM) or a dynamic random access memory (DRAM).

[00030] In various embodiments, the host controller interface 120 retrieves a request packet including a nonvolatile memory command from the host processing unit 110 through the communication network 115, generates a request message packet including the nonvolatile memory command based on the request packet, and provides the request message packet to the network module 125. In turn, the network module 125 routes the request message packet to the processor module 145. The processor module 145 processes the nonvolatile memory command in the request message packet, generates a completion message packet including a completion status (e.g., a completion entry) based on the request message packet, and provides the completion message packet to the network module 125. The network module 125 routes the completion message packet to the host controller interface 120.

[00031] The host controller interface 120 generates a request packet including the completion status based on the completion message packet and transmits the request packet to the host processing unit 110 through the communication network 115. In turn, the host processing unit 110 stores the completion status of the request message packet received from the host controller interface 120 and processes the completion status to determine the status of processing the nonvolatile memory command (i.e., a processing status).

[00032] In various embodiments, a processor module 145 processes the nonvolatile memory command in a request message packet by generating additional request message packets, each of which includes a command. The processor 150 provides the request message packets to the network module 125. In turn, the network module 125 routes each of the request message packets received from the processor module 145 to a functional unit of the nonvolatile memory

controller 105 identified in the request message packet. In this way, the processor 150 functions as a source node and the functional unit receiving the request message packet functions as a destination node.

[00033] The functional unit receiving a request message packet from the processor 150 through the network module 125 processes the command in the request message packet, generates a completion message packet including a completion status based on the request packet, and provides the completion message packet to the network module 125. The completion status of the completion message packet indicates a status of the command processed by the functional unit (i.e., a processing status). The network module 125 routes the completion message packet to the processor 150.

[00034] In various embodiments, the processor module 145 processes the nonvolatile memory command in the request message packet received from the host controller interface 120 by generating a request message packet including a data transfer command for transferring data between the host processing unit 110 and the controller memory 160, and generating another request message packet including a data transfer command for transferring data between the controller memory 160 and the nonvolatile memory device 140. In this way, the processor module 145 generates request message packets for transferring data in a piecemeal manner between the host processing unit 110 and the nonvolatile memory device 140 based on the request message packet including the nonvolatile memory command.

[00035] In some cases, each functional unit receiving a request message packet from the processor module 145 generates one or more request data packets based on the request

message packet. Each of the request data packets is a request for transferring data between functional units of the nonvolatile memory controller 105 through the network module 125 or transferring data between the host processing unit 110 and the host controller interface 120. For example, the control module 130 may generate request data packets and provide the request data packets to the network module 125 for routing to the controller memory 160. In this example, the controller memory 160 generates completion packets including data stored in the controller memory 160 and provides the completion packets to the network module 125 for routing to the control module 130.

[00036] In various embodiments, the nonvolatile memory controller 105 is implemented in an integrated circuit of an integrated circuit device which may include an integrated circuit package containing the integrated circuit. In some embodiments, the nonvolatile memory controller 105 is implemented in more than one integrated circuit of an integrated circuit device which may include a multichip package containing the integrated circuits.

[00037] FIG. 2 illustrates the network module 125, in accordance with an embodiment of the present invention. The network module 125 includes a message network 200 and a data network 205. Each of the message network 200 and the data network 205 is coupled (e.g., connected) to the host controller interface 120, the control module 130, the processor module 145. Additionally, the data network 205 is coupled (e.g., connected) to the controller memory 160.

[00038] The message network 200 routes message packets, such as request message packets and completion message packets, between functional units of the nonvolatile memory

controller 105. In various embodiments, the message network 200 routes message packets among functional units of the nonvolatile memory controller 105 by using an inter-processor communication (IPC) protocol.

[00039] The data network 205 routes data packets, such as data request packets and data completion packets, between functional units of the nonvolatile memory controller 105. In various embodiments, the data network 205 routes data packets among functional units of the nonvolatile memory controller 105 by using an inter-processor communication (IPC) protocol.

[00040] FIG. 3 illustrates the control module 130, in accordance with an embodiment of the present invention. The control module 130 includes a storage controller 300 and a correction module 305. The storage controller 300 is coupled (e.g., connected) to the network module 125, the nonvolatile memory device 140, and the correction module 305. The correction module 305 is also coupled (e.g., connected) to the network module 125.

[00041] The storage controller 300 manages data in the nonvolatile memory device 140. For example, the storage controller 300 may read data from the nonvolatile memory device 140 and write data into the nonvolatile memory device 140. The correction module 305 generates an error correction code (ECC) for data to be stored into the nonvolatile memory device 140 and provides the error correction code to the storage controller 300. In turn, the storage controller 300 writes the data and the error correction code associated with the data into the nonvolatile memory device 140. Additionally, the storage controller 300 reads data and an error correction code associated with the data from the nonvolatile memory device 140 and provides the data and the error correction code to the correction module 305. In turn, the

correction module 305 detects data bit errors in the data, if any, and corrects the data bit errors based on the error correction code associated with the data.

[00042] FIG. 4 illustrates the storage controller 300, in accordance with an embodiment of the present invention. The storage controller 300 includes a command processing module 400, a command input queue 405, a command distribution unit 410, a parity calculator 420, a context module 430, a data distribution unit 440, and a data request router 445. The command input queue 405 is coupled (e.g., connected) to the message network 200 and the command distribution unit 410. Additionally, the command distribution unit 410 is coupled (e.g., connected) to the command processing unit 415 and the context module 430. The parity calculator 420 is coupled to the data network 205, the context module 430, the data distribution unit 440, and the data request router 445. The data request router 445 is coupled (e.g., connected) to the data network 205 and the command processing module 400. Additionally, the command processing module 400 is coupled (e.g., connected) to the data distribution unit 440, the nonvolatile memory device 140, and the correction module 305.

[00043] As illustrated in FIG. 4, the command processing module 400 includes command processing units 415. The command processing units 415 process commands for managing data in the nonvolatile memory device 140, as is described more fully herein. Although three command processing units 415 are illustrated in FIG. 4, the command processing module 400 may have more or fewer than three command processing units 415 in other embodiments.

[00044] The parity calculator 420 includes page frames 425. Moreover, the parity calculator 420 generates parity blocks in the page frames 425, as is described more fully herein. The

context module 430 includes contexts 435 corresponding to the page frames 425 in the parity calculator 420. Moreover, each of the page frames 425 is associated with the corresponding context 435 in the context module 430. The contexts 435 includes data for controlling processing of the commands of a data stripe operation by the storage controller 300, as is described more fully herein. Although three page frames 425 and three contexts 435 are illustrated in FIG. 4, the parity calculator 420 may have more or fewer than three page frames 425 and the context module 430 may have more or fewer than three contexts 435 in other embodiments.

[00045] In various embodiments, a processor 150 in the processor module 145 generates commands for performing a data stripe operation (i.e., data stripe commands). The commands include data update commands for writing data blocks into the nonvolatile memory device 140 and a parity write command for writing a parity block into the nonvolatile memory device 140. The processor 150 generates request message packets, each of which includes a command of the data stripe operation. The command includes a command identifier for identifying the type of the command as either a data update command or a parity write command. Additionally, the command includes a flow identifier, a request tag, and a destination address of a storage location in the nonvolatile memory device 140. Each of the commands of the data stripe operation has a same flow identifier. In this way, the commands of the data stripe operation form a collection of commands associated with each other through the flow identifier. The processor 150 provides the request message packets including the commands for the data stripe operation to the message network 200. In turn, the message network 200 route the request message packets to the storage controller 300.

[00046] The storage controller 300 receives the request message packets of the data stripe operation from the message network 200 and stores the request message packets in the command input queue 405. In various embodiments, the command input queue 405 is a first-in-first-out (FIFO) queue and the storage controller 300 stores the request message packets of the data stripe operation at a tail of the command input queue 405. Because the command input queue 405 receives and stores other packets (e.g., request message packets including data read commands or data erase commands) from the message network 200, the request message packets of the data stripe operation may be interleaved with other packets in the command input queue 405.

[00047] The command distribution unit 410 reads a request message packet at a head of the command input queue 405 and determines whether the request message packet includes a command of a data stripe operation (i.e., a data stripe command). If the request message packet includes a data update command of a data stripe operation, the command distribution unit 410 determines whether the data update operation is associated with a context 435 in the context module 430 based on a flow identifier in the request message packet. If the data update operation is not associated with a context 435, the command distribution unit 410 associates the data stripe operation with a context 435 based on the flow identifier in the request message packet. Moreover, the command distribution unit 410 associates commands having a same flow identifier with the same context 435, as is also described more fully herein. In this way, the command distribution unit 410 associates commands of a data stripe operation with a context 435 based on the flow identifier.

[00048] Additionally, the command distribution unit 410 selects a command processing unit 415 in the command processing module 400 for the request message packet including the data update command and provides (e.g., routes) the request message packet to the selected command processing unit 415. In this way, the command distribution unit 410 distributes the data update command in the request message to the selected processor. In various embodiments, the command distribution unit 410 distributes data update commands of a data stripe operation to a number of command processing units 415 such that each of those command processing units 415 receives one of the data update commands of the data stripe operation. In this way, the command distribution unit 410 stripes the commands of the data stripe operation among command processing units 415 in the command processing module 400.

[00049] If the request message packet at the head of the command input queue 405 includes a parity write command of a data stripe operation, the command distribution unit 410 determines whether the data update commands of the data stripe operation are complete. If the data update commands of the data stripe operation are complete, the command distribution unit 410 distributes the write parity command of the data stripe operation to a command processing unit 415 in the command processing module 400. Otherwise, the command distribution unit 410 monitors the data update commands of the data stripe operation and distributes the write parity command to a command processing unit 415 in the command processing module 400 when the data update commands are complete.

[00050] Each command processing unit 415 receiving a request message packet including a data update command from the command distribution unit 410 generates a data request packet including the data update command based on the request message packet. The data request message includes the flow identifier contained in the request message packet as well as the request tag contained in the request message packet. Additionally, the data request message includes a destination address of a storage location in the controller memory 160. The command processing unit 415 provides the data request packet to the data request router 445. In some embodiments, the command processing unit 415 arbitrates for access to the data request router 445 by providing an arbitration request to the data request router 445. In these embodiments, the command processing unit 415 provides the data request packet to the data request router 445 in response to receiving a grant from the data request router 445.

[00051] The data request router 445 routes (e.g., forwards) the data request packet including the data update command to the data network 205. In turn, the data network 205 routes the data request packet to the controller memory 160, for example based on an identifier of the controller memory 160 contained in the data request packet. In various embodiments, the data request router 445 identifies a type of the command in the data request message packet received from the data request router 445. If the command in the data request packet is a parity write command, data request router 445 routes the data request packet to the parity calculator 420. Otherwise, the data request router 445 routes the data request packet to the data network 205.

[00052] The controller memory 160 reads a data block at a storage location identified by the destination address in the data request packet and generates a completion packet including the data block. For example, the controller memory 160 may read the data block from a dynamic random access memory (DRAM) in the controller memory 160. The completion block also includes the flow identifier contained in the data request packet and the request tag contained in the data request packet. In this way the completion packet is associated with the data request packet. The controller memory 160 provides the completion packet to the data network 205. In turn, the data network 205 routes the completion packet to the storage controller 300, for example based on an identifier of the storage controller 300 in the completion packet.

[00053] The parity calculator 420 receives the completion packet routed to the storage controller 300 and forwards the completion packet to the data distribution unit 440. In turn, the data distribution unit 440 distributes the completion packet to the command processing unit 415 that generated the data request message associated with the completion packet (i.e., the data request message including the same request tag contained in the completion packet). In this way the parity calculator 420 and the command processing unit 415 receive the completion packet including the data block from the data network 205 at substantially the same time (i.e., substantially simultaneously). The command processing unit 415 receiving the completion packet writes the data block of the completion packet to the nonvolatile memory device 140 at the address of the nonvolatile memory device 140 contained in the request message packet associated with the completion packet (i.e., the request message packet containing the same request tag contained in the completion packet).

[00054] Additionally, the parity calculator 420 processes the completion packet as part of a process of generating a parity block for the data stripe operation. In response to receiving the completion packet, the parity calculator 420 identifies the context 435 of the data stripe operation associated with the data block. Additionally, the parity calculator 420 identifies the page frame 425 associated with the context 435. If the data block contained in the completion packet is the first data block of the data stripe operation received by the parity calculator 420, the parity calculator 420 stores the data block into the page frame 425. In this way, the parity calculator 420 initializes a parity block in the page frame 425.

[00055] Otherwise, if the data block contained in the completion packet is not the first data block of the data stripe operation received by the parity calculator 420, the parity calculator 420 generates an updated data packet by performing an operation on the data block stored in the page frame 425 and the data block contained in the completion packet. Further, the parity calculator 420 replaces the data block stored in the page frame 425 associated with the updated data block. In this way, the parity calculator 420 updates the parity block stored in the page frame 425.

[00056] The updated data block generated by the parity calculator 420 based on last data block of the data stripe operation is a parity block of the data stripe operation. Moreover, the parity calculator 420 completes generation of the parity block for the data stripe operation by storing the updated data block of the data stripe operation into the page frame 425. In this way, the parity calculator 420 generates the parity block of the data operation on the fly as

completion packets including data blocks of the data operation are received by the storage controller 300 and forwarded to the command processing units 415.

[00057] In some embodiments, the operation performed by the parity calculator 420 is a logical exclusive-or (XOR) operation. In these embodiments, the parity block generated by parity calculator 420 is an exclusive-or of the data blocks in the data stripe operation. In some embodiments, the parity calculator 420 generates more than one parity block for a data stripe operation. For example, the parity calculator 420 may generate a p-parity block and a q-parity block according to a level 6 redundant array of independent disk (RAID Level 6) algorithm. In this example, the operation performed by the parity calculator 420 includes a logical exclusive-or operation and a logical shift operation. In various embodiments, the operation performed by the parity calculator includes other logical or mathematical functions in addition to a logical exclusive-or operation, for example to implement a RAID Level 5 or RAID Level 6 algorithm.

[00058] In some embodiments, a size of a data block received by the parity calculator 420 is less than a size of the parity block generated by the parity calculator 420. For example, the size of the data block may be half the size of the parity block. In these embodiments, the completion packet indicates a position of the data block for performing the operation on the data block and the parity block. For example, the completion packet may indicate that the operation is to be performed on the data block and a first half of the parity block. As another example, the completion packet may indicate that the operation is to be performed on the data block and a second half of the parity block. In this way, the parity calculator 420 updates the

parity block in a piecemeal manner based on data blocks having a smaller size than the parity block.

[00059] A command processing unit 415 receiving a request message packet including a parity write command from the command distribution unit 410 generates a data request packet including the parity write command based on the request message packet. The data request packet includes the flow identifier of the request message packet and the request tag contained in the request message packet. The command processing unit 415 provides the data request packet to the data request router 445. In some embodiments, the command processing unit 415 arbitrates for access to the data request router 445 by providing an arbitration request to the data request router 445. In these embodiments, the command processing unit 415 provides the data request packet to the data request router 445 in response to receiving a grant from the data request router 445.

[00060] The parity calculator 420 identifies the context 435 of the data stripe operation associated with the write parity command based on the flow identifier in the data request packet. Further, the parity calculator 420 reads the parity block from the page frame 425 associated with the context 435 and generates a completion packet including the parity block. The completion packet also includes the flow identifier contained in the data request packet and the request tag contained in the data request packet. The parity calculator 420 provides the completion packet to the data distribution unit 440.

[00061] The data distribution unit 440 distributes the completion packet including the parity block to the command processing unit 415 in the command processing module 400 that

generated the data request packet including the parity write command. For example, the data distribution unit 440 may identify the command processing unit 415 based on the request tag in the completion packet. The command processing unit 415 receiving the completion packet writes the parity block of the completion packet to the nonvolatile memory device 140 at the address of the storage location in the nonvolatile memory device 140 contained in the request message packet associated with the completion packet (i.e., the request message packet containing the same request tag contained in the completion packet).

[00062] In various embodiments, the data network 205 is a data path for transmitting data packets (e.g., completion packets) from the controller memory 160 to the parity calculator 420 and the command processing units 415 of the storage controller 300. In this way, both the parity calculator 420 and the command processing units 415 receive packets from the controller memory 160 through the data path.

[00063] FIG. 5 illustrates the context module 430, in accordance with an embodiment of the present invention. In addition to the contexts 435, the context module 430 includes a context module controller 520 coupled to the contexts 435 for controlling access to the context 435. Each context 435 includes a context state 505, a flow identifier 510, and a stripe count 515. In various embodiments, the context 435 includes storage locations for storing the context state 505, the flow identifier 510, and the stripe count 515 of the context 435. For example, the storage locations of the context 435 may be registers or a portion of a random access memory (RAM).

[00064] The context state 505 of the context 435 is a value indicating a state of context 435. In one embodiment, the context state 505 is an idle state, an allocated state, an initialized state, or a computed state, as is described more fully herein. The flow identifier 510 is a value for associating commands of a data stripe operation with the context 435 and for identifying the context 435 associated with a data stripe operation. The stripe count 515 is value for determining when a data stripe operation is complete, as is also described more fully herein.

[00065] In operation, the command distribution unit 410 receives a request message packet from the command input queue 405 and determines whether the request message packet includes a data update command. If the request message packet includes a data update command, the command distribution unit 410 determines whether the data stripe operation associated with the data update command has been allocated to a page frame 425 in the parity calculator 420. In this process, the command distribution unit 410 identifies each context 435 in the allocated state or the initialized state. For each identified context 435, the command distribution unit 410 determines whether a flow identifier in the request message packet is the same as the flow identifier 510 of the context 435. If the flow identifier in the request message packet is the same as the flow identifier 510 of an identified context 435, the command distribution unit 410 determines the data stripe operation is associated with the context 435. In this way, command distribution unit 410 also determines the page frame 425 associated with the context 435 is allocated to the data stripe operation.

[00066] If the command distribution unit 410 determines that a page frame 425 in the parity calculator 420 has not been allocated to the data stripe operation associated with the update

command in the request message packet, the command distribution unit 410 identifies a context 435 in the idle state. Further, the command distribution unit 410 allocates the page frame 425 associated with the context 435 to the data stripe operation by modifying (e.g., updating) the context state 505 of the context 435 to the allocated state and modifying the flow identifier 510 of the context 435 to the flow identifier contained the request message packet.

[00067] In addition to allocating the page frame 425 in the parity calculator 420 to the data stripe operation, the command distribution unit 410 initializes the stripe count 515 to an initial stripe count based on the number of data blocks in the data stripe operation. In various embodiments, the stripe count 515 is a predetermined value. In one embodiment, the initial stripe count is equal to the number of data blocks in the data stripe operation. In this embodiment, the parity calculator 420 decrements the stripe count 515 when initializing a parity block in the page frame 425 associated with the context 435 and when updating the parity block in the page frame 425, as is described more fully herein. In another embodiment, the initial stripe count 515 is one less than the number of data blocks in the data stripe operation. In this embodiment, the parity calculator 420 decrements the stripe count 515 when updating a parity block in the page frame 425 associated with the context 435 but does not decrement the stripe count 515 when initializing the parity block in the page frame 425, as is also described more fully herein.

[00068] In various embodiments, the parity calculator 420 determines an operation to perform on a data block of a data stripe operation received by the parity calculator 420 based on the context state 505 of the context 435 associated with the data stripe operation. If the context

state 505 is the allocated state, the parity calculator 420 initializes a parity block in the page frame 425 associated with the context 435 by storing the data block into the page frame 425, as is described more fully herein. Additionally, the parity calculator 420 changes the context state 505 from the allocated state to the initialized state. In some embodiments, the parity calculator 420 also updates (e.g., decrements) the stripe count 515 of the context 435 to indicate the parity calculator 420 processed the data block received by the parity calculator 420.

[00069] Otherwise, if the parity calculator 420 receives a data block of a data stripe operation and the context state 505 of the context 435 associated with the data stripe operation is the initialized state, the parity calculator 420 updates the data block (e.g., parity block) stored in the page frame 425 associated with the context 435 by performing an operation on the data block received by the parity calculator 420 and the data block stored in the page frame 425, as is described more fully herein. Additionally, the parity calculator 420 updates (e.g., decrements) the stripe count 515 in the context module 430 associated with the data operation to indicate the parity calculator 420 processed the data block received by the parity calculator 420.

[00070] Further, the parity calculator 420 determines whether the data block received by the parity calculator 420 is the last data block of the data stripe operation based on the stripe count 515 of the context 435. In various embodiments, the parity calculator 420 determines the data block received by the parity calculator 420 is the last data block of the data stripe operation by determining the stripe count 515 has reached a threshold value (e.g., zero). If the parity calculator 420 determines the data block received by the parity calculator 420 is the last data

block of the data stripe operation, the parity calculator 420 modifies (e.g., updates) the context state 505 of the context 435 associated with the data stripe operation to the completed state. In this way, the parity calculator 420 indicates generation of the parity block is complete.

[00071] The command distribution unit 410 determines generation of the parity block for the data stripe operation is complete by determining the context state 505 of the context 435 associated with the data stripe operation is in the completed state. In this way, the command distribution unit 410 also determines the stripe count 515 of the context 435 associated with the data stripe operation has reached a threshold value. Furthermore, the command distribution unit 410 modifies (e.g., updates) the context state 505 of the context 435 associated with the data stripe operation to the idle state to indicate the stripe count 515 of the context 435 associated with the data stripe operation has reached the threshold value. In this way, the command distribution unit 410 releases the context 435 for use in another data stripe operation.

[00072] Because the storage controller 300 includes multiple page frames 425 and multiple contexts 435 associated with the page frames 425, the storage controller 300 may process more than one data stripe operation at the same time. In this way, the storage controller 300 is capable of performing multiple data stripe operations in parallel. As a result, throughput of the nonvolatile memory controller 105 is higher than throughput of other nonvolatile memory controllers capable of processing only a single data stripe operation at a time.

[00073] FIG. 6 illustrates the parity calculator 420, in accordance with an embodiment of the present invention. The parity calculator 420 includes a context memory 600, a parity calculator controller 605, a computation block 620, and a selector (MUX) 630. For example,

the selector 630 may be a multiplexer. The context memory 600 is coupled (e.g., connected) to data network 205, the parity calculator controller 605, the computation block 620, and the selector 630. The computation block 620 is coupled (e.g., connected) to the data network 205 and the selector 630. The selector 630 is coupled (e.g., connected) to the data network 205, the parity calculator controller 605, and the data distribution unit 440. Additionally, the parity calculator controller 605 is coupled (e.g., connected) to the data network 205, the data request router 445, and the context module 430. As illustrated in FIG. 6, the context memory 600 includes the page frames 425 of the parity calculator 420.

[00074] In operation, the parity calculator 420 receives a completion packet from the data network 205. In response to receiving the completion packet, the parity calculator controller 605 generates a control signal and provides the control signal to the selector 630. In response to the control signal received from the parity calculator controller 605, the selector 630 passes the completion packet to the data distribution unit 440. In turn, the data distribution unit 440 distributes the completion packet to a command processing unit 415, as is described more fully herein. In this way, the parity calculator 420 forwards the completion packet to the command processing unit 415.

[00075] Additionally, the context module controller 520 determines whether the completion packet includes a data update command. If the completion packet includes a data update command, the parity calculator controller 605 identifies the context 435 of the data stripe operation associated with the data update command based on a flow identifier in the completion packet. In this process, the parity calculator controller 605 identifies the context

435 containing a flow identifier 510 that is the same as the flow identifier contained in the completion packet.

[00076] If the context state 505 of the context 435 is the allocated state, the parity calculator controller 605 generates a control signal and provides the control signal to the context memory 600. In response to the control signal received from the parity calculator controller 605, the context memory 600 stores the data block contained in the completion packet into the page frame 425 associated with the context 435. The data block stored in the page frame 425 is an initial parity block for the data stripe operation associated with the data block. Further, the parity calculator controller 605 modifies (e.g., updates) the context state 505 of the context 435 to the initialized state. In some embodiments, the parity calculator controller 605 also modifies (e.g., decrements) the stripe count 515 of the context 435, as is described more fully herein.

[00077] Otherwise, if the context state 505 of the context 435 is the initialized state, the controller generates a control signal and provides the control signal to context memory 600. In response to the control signal received from the parity calculator controller 605, the context memory 600 provides the data block stored in the page frame 425 associated with the context 435 to the computation block 620. In turn, the computation block 620 generates an updated data block (i.e., an updated parity block) by performing a parity operation (e.g., an exclusive-or operation) on the data block received from the context memory 600 and the data block in the completion packet.

[00078] The parity calculator controller 605 generates another control signal and provides the control signal to the context memory 600. In response to the control signal, the context

memory 600 stores the updated data block into the page frame 425 associated with the context 435. In this way, the parity calculator 420 performs an update operation on the parity block (i.e., data block) stored in the page frame 425. Additionally, the parity calculator controller 605 modifies (e.g., decrements) the stripe count 515 of the context 435, as is described more fully herein. In this way, the parity calculator controller 605 counts a number of update operations performed on the initial data block stored in the page frame 425. Moreover, if the stripe count 515 has reached a threshold value (e.g., a value of zero), the parity calculator controller 605 updates the context state 505 of the context 435 to a completed state. In this way, the context module controller 520 indicates generation of the parity block is complete.

[00079] If the parity calculator controller 605 receives a data request packet including a write parity command from the data request router 445, the context module controller 520 identifies the context 435 containing the flow identifier contained in the data request packet.

Additionally, the parity calculator controller 605 generates a control signal and provides the control signal to context memory 600. In response to the control signal received from the parity calculator controller 605, the context memory 600 provides the parity block stored in the page frame 425 associated with the context 435 to the selector 630. Additionally, the parity calculator controller 605 provides the request tag in the data request packet including the write parity command to the selector 630.

[00080] The parity calculator controller 605 generates another control signal and provides the control signal to the selector 630. In response to the control signal received from the parity calculator controller 605, the selector 630 passes the parity block and the request tag received

from the parity calculator controller 605 to the data distribution unit 440. In this way, the parity calculator 420 provides a completion packet including the parity block and the request tag to the data distribution unit 440.

[00081] In some instances, the parity calculator controller 605 may receive a data completion packet including a data update command from the data network 205 and a data request packet include a write parity command from the data request router 445 at the same time. In these embodiments, the parity calculator controller 605 processes the packets sequentially. In other embodiments, the parity calculator controller 605 processes the packets substantially simultaneously. For example, the context memory 600 may be a dual-port memory and the parity calculator controller 605 may store an updated parity block into the context memory 600 for a data stripe operation and at the same time read a parity block from the context memory 600 for another data stripe operation.

[00082] FIG. 7 illustrates the processing unit, in accordance with an embodiment of the present invention. The command processing unit 415 includes a command processor queue 700 and a command processor 705 coupled (e.g., connected) to the command processor queue 700. The command processor queue 700 stores packets (e.g., request message packets) received from the command distribution unit 410. In various embodiments, the command distribution unit 410 writes a command to the command processing unit 415 by writing a request message packet including the command at a tail of the command processor queue 700. For example, the command processor queue 700 may be a first-in-first-out (FIFO) queue.

[00083] The command processor 705 reads a command at head of the command processor queue 700, for example by reading a request packet including the command at the head of the command processor queue 700. The command processor 705 processes the command by generating nonvolatile memory commands based on the command in the request packet. Further, the command processor 705 provides the nonvolatile memory commands to the nonvolatile memory device 140. In turn, the nonvolatile memory device 140 processes the commands.

[00084] In various embodiments, the nonvolatile memory commands generated by the command processor 705 are specific to a type of the nonvolatile memory device 140. For example, the nonvolatile memory commands may be specific to a particular manufacturer of the nonvolatile memory device 140. In some embodiments, the command processor 705 is programmable to generate nonvolatile memory commands for a variety of different types of nonvolatile memory devices 140.

[00085] FIG. 8 illustrates the nonvolatile memory device 140, in accordance with an embodiment of the present invention. The nonvolatile memory device 140 includes nonvolatile memory units 800. Each of the nonvolatile memory units 800 is coupled (e.g., connected) to a corresponding command processing unit 415 in the command processing module 400. For example, each of the nonvolatile memory units 800 may be a nonvolatile memory device, such as a flash storage device.

[00086] In various embodiments, the storage controller 300 distributes the commands of a data stripe operation (i.e., data update commands and a parity write command) among the

command processing units 415. In turn, each of the command processing units 415 writes a data block or a parity block into nonvolatile memory unit 800 corresponding to the command processing unit 415. In this way, the storage controller 300 performs the data stripe operation.

[00087] FIG. 9 illustrates a portion of a method 900 of generating parity data, in accordance with an embodiment of the present invention. In various embodiments, the portion of the method 900 illustrated in FIG. 9 is performed by the command distribution unit 410 in the storage controller 300.

[00088] In step 905, a command is received at the command distribution unit. In various embodiments, the command distribution unit 410 receives the command of the data stripe operation by receiving a request message packet including the command. For example, the command distribution unit 410 may receive the request message packet from the command input queue 405. The portion of the method 900 then proceeds to step 910.

[00089] In step 910, it is determined whether the command is a data update command. In various embodiments, the command distribution unit 410 determines whether the command in the request message packet is a data update command. If the command in the request message packet is a data update command, the portion of the method proceeds to step 915. Otherwise, the portion of the method 900 proceeds to step 940.

[00090] In step 915, arrived at from the determination in step 910 that the command is a data update command, a determination is made as to whether a page frame is allocated to the data stripe operation associated with the data update command. In various embodiments, the

command distribution unit 410 determines whether a page frame 425 is allocated to the data stripe operation associated with the command based on a flow identifier in the request message packet, as is described more fully herein. If a page frame 425 is allocated to the data stripe operation associated with the command, the portion of the method 900 proceeds to step 940. Otherwise, the portion of the method 900 proceeds to step 920.

[00091] In step 920, arrived at from the determination in step 915 that a page frame is not allocated to the data operation associated with the data update command, it is determined whether a page frame is available. In various embodiments, the command distribution unit 410 determines whether a page frame 425 is available by determining whether a context 435 is in the idle state. If the command distribution unit 410 identifies at least one context 435 in the idle state, the command distribution unit 410 determines a page frame 425 is available. If a page frame 425 is available, the portion of the method 900 proceeds to step 925. Otherwise, the portion of the method 900 returns to step 920.

[00092] In step 925, arrived at from the determining in step 920 that a page frame is available, a page frame associated with a context is allocated to the data stripe operation. In various embodiments, the command distribution unit 410 allocates a page frame 425 to the data stripe operation by selecting a context 435 in the idle state, setting the context state 505 of the context 435 to the allocated state, and modifying (i.e., setting) the flow identifier 510 in the context 435 to the flow identifier contained in the request message packet. The portion of the method 900 then proceeds to step 930.

[00093] In step 930, a stripe count is initialized in the context. In various embodiments, the command distribution unit 410 initializes the stripe count 515 in the context 435 associated with the data operation to an initial stripe count. For example, the initial stripe count may be equal to the number of data blocks associated with the data stripe operation. The portion of the method 900 then proceeds to step 935.

[00094] In step 935, the context is set to an allocated state. In various embodiments, the command distribution unit 410 sets the context 435 associated with the data operation to the allocated state. For example, the command distribution unit 410 may modify (i.e., set) the context state 505 of the context 435 to the allocated state. The portion of the portion of the method 900 then proceeds to step 940.

[00095] In step 940, arrived at from the determination in step 910 that the command is not a data update command, the determination in step 915 that a page frame is allocated to the stripe operation, or step 935 in which the context is set to the allocated state, it is determined whether the command is a parity write command. In various embodiments, the command distribution unit 410 determines whether the command is a parity write command. If the command is a parity write command, the method 900 proceeds to step 945. Otherwise, if the command is not a parity write command, the method 900 proceeds to step 950.

[00096] In step 945, arrived at from the determination in step 940 that the command is a parity write command, it is determined whether the data update commands of the data stripe operation are complete. In various embodiments, the command distribution unit 410 determines whether the data update commands of the data stripe operation are complete based

on the stripe count 515 of the context 435 associated with the data stripe. If the stripe count 515 of the context 435 associated with the data stripe operation has reached a threshold value, the command distribution unit 410 determines the data update commands of the data stripe operation are complete and the method 900 proceeds to step 950. Otherwise, if the command distribution unit 410 determines the stripe count 515 of the context 435 associated with the data stripe has not reached a threshold value, the command distribution unit 410 determines the data update commands of the data stripe operation are not complete and the method 900 returns to step 945.

[00097] In step 950, arrived at from the determination in step 940 that the command is not a parity write command or from the determination in step 945 that the data update commands of the data stripe operation are complete, the command is distributed to a processing unit. In various embodiments, the command distribution unit 410 distributes the command to a command processing unit 415 by selecting the command processing unit 415 and providing the command to the command processing unit 415. The portion of the method 900 then proceeds to step 955.

[00098] In step 955, it is determined whether an additional command is received. In various embodiments, if the command distribution unit 410 receives an additional command of the data stripe operation, the portion of the portion of the method 900 returns to step 910. Otherwise, the portion of the method 900 ends.

[00099] In various embodiments, the portion of the method 900 illustrated in FIG. 9 may include more or fewer than the steps 905-955 illustrated in FIG. 9 and described above. In

some embodiments, the steps 905-955 in the portion of the method 900 illustrated in FIG. 9 may be performed in a different order than the order illustrated in FIG. 9 and described above. In some embodiments, some of the steps 905-955 of the portion of the method 900 illustrated in FIG. 9 may be performed in parallel or substantially simultaneously. In various embodiments, one or more of the steps 905-955 may be performed more than once in the portion of the method 900 illustrated in FIG. 9.

[000100] FIG. 10 illustrates a portion of a method 1000 of generating parity data, in accordance with an embodiment of the present invention. In various embodiments, the portion of the method 1000 illustrated in FIG. 10 is performed by the command processing module 400 in the storage controller 300. In step 1005, a command is received by a command processing unit. In various embodiments, a command processing unit 415 in the command processing module 400 receives a command by receiving a request message packet including the command from the command distribution unit 410. The portion of the method 1000 then proceeds to step 1010.

[000101] In step 1010, it is determined whether the command is a data stripe command. In various embodiments, the command processing unit 415 determines whether the command is a data stripe command by determining whether the command is a data update command or a parity write command. If the command is a data stripe command, the portion of the method 1000 proceeds to step 1015. Otherwise, the portion of the method 1000 proceeds to step 1030.

[000102] In step 1015, arrived at from the determination in step 1010 that the command is a data stripe command, a request is generated for a block based the command. In various embodiments, the command processing unit 415 generates a request for the block by

generating a data request packet including the command based on the request message packet.

If the command is a data update command, the command processing unit 415 generates the data request for a data block based the data update command. Otherwise, if the command is a parity write command, the command processing unit 415 generates the data request for a parity block based the parity write command. Further, the command processing unit 415 provides the data request packet to the data request router 445 for routing to the controller memory 160 or the parity calculator 420, as is described more fully herein. The portion of the method 1000 then proceeds to step 1020.

[000103] In step 1020, a block is received in response to the request for the block. In various embodiments, the command processing unit 415 receives a completion packet including the block in response to the data request packet including the command. For example, the command processing unit 415 may receive a completion packet including a data block or a completion packet including a parity block. The portion of the method 1000 then proceeds to step 1025.

[000104] In step 1025, the block is written to a nonvolatile memory device. In various embodiments, the command processing unit 415 writes the block of the completion packet to the nonvolatile memory device 140 at the address of the storage location of the nonvolatile memory device 140 contained in the request message packet associated with the completion packet. For example, the completion packet may include a data block and the command processing unit 415 may write the data block to the nonvolatile memory device 140. As another example, the completion packet may include a parity block and the command

processing unit 415 may write the parity block to the nonvolatile memory device 140. The portion of the method 1000 then proceeds to step 1035.

[000105]In step 1030, arrived at from the determination in step 1010 that the command is not a data stripe command, the command is processed. In various embodiments, the command processing unit 415 receiving the command processes the command. For example, the command may be a read request command for reading data from the nonvolatile memory device 140 or an erase request for erasing data from the nonvolatile memory device 140. The portion of the method 1000 then proceeds to step 1035.

[000106]In step 1035, arrived at from step 1025 in which a block is written to the nonvolatile memory or step 1030 in which a command is processed, it is determined whether an additional command of the data stripe operation is received by a command processing unit 415. In various embodiments, if a command processing unit 415 in the command processing module 400 receives an additional command of the data stripe operation, the portion of the method 1000 returns to step 1010. Otherwise, the portion of the method 1000 ends.

[000107]In various embodiments, the portion of the method 1000 illustrated in FIG. 10 may include more or fewer than the steps 1005-1035 illustrated in FIG. 10 and described above. In some embodiments, the steps 1005-1035 in the portion of the method 1000 illustrated in FIG. 10 may be performed in a different order than the order illustrated in FIG. 10 and described above. In some embodiments, some of the steps 1005-1035 of the portion of the method 1000 illustrated in FIG. 10 may be performed in parallel or substantially simultaneously. In various

embodiments, one or more of the steps 1005-1035 may be performed more than once in the portion of the method 1000 illustrated in FIG. 10.

[000108] FIG. 11 illustrates a portion of a method 1100 of generating parity data, in accordance with an embodiment of the present invention. In various embodiments, the portion of the method 1100 illustrated in FIG. 11 is performed by the parity calculator 420 in the storage controller 300.

[000109] In step 1105, a data block is received by the parity calculator. In various embodiments, the parity calculator 420 receives a data block by receiving a completion packet including the data block. For example, the parity calculator 420 may receive the completion packet from the data network 205. In addition to the data block, the completion packet includes a flow identifier contained in a data request packet associated with the completion packet and a request tag contained in the data request packet. The portion of the method 1100 then proceeds to step 1110.

[000110] In step 1110, the data block is forwarded to a processing unit. In various embodiments, the parity calculator 420 forwards the data block to a command processing unit 415 by forwarding a completion packet including the data block to the data distribution unit 440. In turn, the data distribution unit 440 distributes the completion packet including the data block to the command processing unit 415 based on the request tag contained in the completion packet. The portion of the method 1100 then proceeds to step 1115.

[000111]In step 1115, it is determined whether the command is a data update command. In various embodiments, the parity calculator 420 determines whether the command is a data update command. For example, the parity calculator controller 605 may determine based on command in the completion packet containing the data block whether the command is a data update command. If the command is a data update command, the portion of the method 1100 proceeds to step 1120. Otherwise, if the command is not a data update command, the portion of the method 1100 proceeds to step 1150.

[000112]In step 1120, arrived at from the determination in step 1115 that the command is a data update command, the context of the data update command is identified. In various embodiments, the parity calculator 420 identifies the context 435 of the data update command by matching the flow identifier contained in the completion packet with the flow identifier 510 in the context 435. The portion of the method 1100 then proceeds to step 1125.

[000113]In step 1125, it is determined whether the context state of the context is in an initialized state. In various embodiments, the parity calculator 420 determines whether the context 435 associated with the data block of the data operation is in the initialized state based on the context state 505 of the context 435. If the context 435 is in the initialized state, the portion of the method 1100 then proceeds to step 1145. Otherwise, if the context 435 is not in the initialized state, the portion of the method 1100 proceeds to step 1130.

[000114]In step 1130, arrived at from the determination in step 1125 that the context is not in the initialized state, a parity block is initialized in the page frame associated with the context. In various embodiments, the parity calculator 420 initializes a parity block in the page frame

425 associated with the context 435 of the data block by writing the data block into the page frame 425. The portion of the method 1100 then proceeds to step 1135. In step 1135, the context is set to an initialized state. In various embodiments, the parity calculator 420 sets the context 435 associated with the data stripe operation to the initialized state. For example, the parity calculator 420 may set context state 505 of the context 435 associated with the data stripe operation to the initialized state. The portion of the method 1100 then proceeds to step 1140.

[000115] In step 1140, the stripe count of the context is updated. In various embodiments, the parity calculator 420 updates the stripe count 515 of the context 435 associated with the data stripe operation, for example by decrementing the stripe count 515 of the context 435. The portion of the method 1100 then proceeds to step 1150.

[000116] In step 1145, arrived at from the determination in step 1125 that the context is in the initialized state, the parity block in the page frame is updated. In various embodiments, the parity calculator 420 generates an updated data block (i.e., an updated parity block) by performing an operation on the data block (i.e., parity block) in the page frame 425 and the data block in the data request packet received by the parity calculator 420. Further, the parity calculator 420 replaces the data block (i.e., parity block) in the page frame 425 with the updated data block (i.e., updated parity block). The portion of the method 1100 then proceeds to step 1140.

[000117] In step 1150, arrived at from the determination in step 1115 that the command is not a data update command or from step 1140 in which the stripe count of the context is updated, it

is determined whether the parity calculator 420 receives an additional data block of the data stripe operation. In various embodiments, if the parity calculator 420 receives an additional data block of the data stripe operation, the portion of the method 1100 returns to step 1110. Otherwise, the portion of the method 1100 ends.

[000118] In various embodiments, the portion of the method 1100 illustrated in FIG. 11 may include more or fewer than the steps 1105-1150 illustrated in FIG. 11 and described above. In some embodiments, the steps 1105-1150 of the portion of the method 1100 illustrated in FIG. 11 may be performed in a different order than the order illustrated in FIG. 11 and described above. In some embodiments, some of the steps 1105-1150 of the portion of the method 1100 illustrated in FIG. 11 may be performed in parallel or substantially simultaneously. In various embodiments, one or more of the steps 1105-1150 may be performed more than once in the portion of the method 1100 illustrated in FIG. 11.

[000119] FIG. 12 illustrates a portion of a method 1200 of generating parity data, in accordance with an embodiment of the present invention. In various embodiments, the portion of the method 1200 illustrated in FIG. 12 is performed by the parity calculator 420 in the storage controller 300. In step 1205, the parity calculator receives a parity write command. In various embodiments, the parity calculator 420 receives the parity write command from the data request router 445 by receiving a data packet including the parity write command. For example, the parity calculator controller 605 of the parity calculator 420 may receive the data packet including the parity write command from the data request router 445. The portion of the method 1200 then proceeds to step 1210.

[000120] In step 1210, the context of the parity write command is identified. In various embodiments, the parity calculator 420 identifies the context 435 of the parity write command based on a flow identifier in the data request packet including the parity write command. For example, the parity calculator controller 605 of the parity calculator 420 may identify a context 435 containing a flow identifier 510 which is the same as the flow identifier contained in the data request packet. The portion of the method 1200 then proceeds to step 1215.

[000121] In step 1215, a parity block is read from the page frame associated with the context. In various embodiments, the parity calculator 420 reads the parity block stored in the page frame 425 associated with the context 435 of the data stripe operation. For example, the parity calculator controller 605 of the parity calculator 420 may provide a control signal to the context memory 600 for reading the parity block from the page frame 425 associated with the context 435. The portion of the method 1200 then proceeds to step 1220.

[000122] In step 1220, the parity block is provided to a command processing unit. In various embodiments, the parity calculator 420 provides the command to a command processing unit 415 by providing the parity block read from the page frame 425 and the request tag in the data request packet including the parity write command to the data distribution unit 440. In this way, the parity block provides a completion packet including the parity block to the data distribution unit 440. In turn, the data distribution unit 440 distributes the completion packet including the parity block to the command processing unit 415 based on the request tag. For example, the data distribution unit 440 may distribute the completion packet to the command

processing unit 415 that generated the data request message including the parity write operation. The portion of the method 1200 then ends.

[000123] In various embodiments, the portion of the method 1200 illustrated in FIG. 12 may include more or fewer than the steps 1200-1220 illustrated in FIG. 12 and described above. In some embodiments, the steps 1200-1220 of the portion of the method 1200 illustrated in FIG. 12 may be performed in a different order than the order illustrated in FIG. 12 and described above. In some embodiments, some of the steps 1200-1220 of the portion of the method 1200 illustrated in FIG. 12 may be performed in parallel or substantially simultaneously. In various embodiments, one or more of the steps 1200-1220 may be performed more than once in the portion of the method 1200 illustrated in FIG. 12.

[000124] In various embodiments, the nonvolatile memory controller 105 performs a data stripe operation by using a distributed processing technique in which the data distribution unit 440 performs the portion of the method 900, the command processing module 400 performs the portion of the method 1000, and the parity calculator 420 performs the portion of the method 1100 and the portion of the method 1200. In this way, the nonvolatile memory controller 105 is a distributed processing system for performing the data stripe operation. Furthermore, because the nonvolatile memory controller 105 includes contexts 435 for processing data stripe operations, the nonvolatile memory controller 105 may process multiple data stripe operation in parallel.

[000125] Although the invention has been described with reference to particular embodiments thereof, it will be apparent to one of ordinary skill in the art that modifications to the described

embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.

CLAIMS

What is claimed is:

1. A nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, the nonvolatile memory controller comprising:

a plurality of command processing units, each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe operation, the plurality of commands including a plurality of data update commands and a parity write command, each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator configured to receive the data blocks of the plurality of data blocks and generate a parity block based on the data blocks, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command.

2. The nonvolatile memory controller of claim 1, wherein the parity calculator includes a context memory including a page frame, and the parity calculator is further configured to receive the plurality of data blocks as a sequence of data blocks and to generate the parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks.
3. The nonvolatile memory controller of claim 2, wherein the parity calculator is further configured to update the data block stored in the page frame by performing a logical operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks.
4. The nonvolatile memory controller of claim 3, wherein the logical operation includes an exclusive-or operation.
5. The nonvolatile memory controller of claim 2, further comprising a context associated with the page frame and including a stripe count for counting each occurrence of updating the parity block, the nonvolatile memory controller further comprising a command distribution unit configured to determine the parity block is generated by determining the stripe count has reached a threshold value.

6. The nonvolatile memory controller of claim 1, wherein the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units, determine generation of the parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete.

7. The nonvolatile memory controller of claim 1, further comprising:
a controller memory configured to store the plurality of data blocks; and
a data network coupled to the controller memory, the plurality of command processing units, and the parity calculator, wherein the plurality of command processing units is further configured to request the plurality of data blocks by generating a plurality of data request packets, the controller memory is further configured to generate a plurality of completion packets including the plurality of data blocks, and both the parity calculator and the plurality of command processing units are further configured to receive the plurality of data blocks through the data network.

8. The nonvolatile memory controller of claim 7, wherein the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units, determine generation of the parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete.

9. The nonvolatile memory controller of claim 8, wherein each command processing unit of the plurality of command processing units comprises a command processing unit command queue for storing commands distributed to the command processing unit from the command distribution unit.

10. The nonvolatile memory controller of claim 8, further comprising a context memory including a plurality of page frames, wherein each command of the plurality of commands includes a flow identifier, and the command distribution unit is further configured to allocate a page frame of the context memory to the data stripe operation by associating the flow identifier with the page frame.

11. The nonvolatile memory controller of claim 1, wherein the plurality of command processing units is further configured to perform a plurality of data stripe operations in parallel.

12. A nonvolatile memory controller comprising:

a command distribution unit configured to receive a plurality of commands for performing a data stripe operation on a plurality of data blocks, the plurality of commands comprising a plurality of data update commands and a parity write command;

a plurality of command processing units coupled to the command distribution unit, the command distribution unit further configured to distribute the plurality of data update commands among command processing units of the plurality of command processing units, each command processing unit receiving a data update command configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator including a context memory including a page frame, the parity calculator configured to receive the data blocks of the plurality of data blocks as a sequence of data blocks, generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete, the command processing unit receiving the parity write command configured to write the parity block into the nonvolatile memory device.

13. The nonvolatile memory controller of claim 12, wherein the plurality of command processing units is further configured to process the plurality of data update commands in an arbitrary order.

14. The nonvolatile memory controller of claim 13, wherein the context memory includes a plurality of page frames for storing a plurality of parity blocks of a plurality of data stripe operations, and wherein the plurality of command processing units is further configured to perform the plurality of data stripe operations in parallel.

15. A method of generating parity data, the method comprising:
- distributing a plurality of commands for performing the data stripe operation among a plurality of command processing units in the nonvolatile memory controller, the plurality of commands including a plurality of data update commands and a parity write command;
 - generating a plurality of data requests by the plurality of command processing units based on the plurality of data update commands;
 - receiving a plurality of data blocks at the plurality of command processing units and at a parity calculator of the nonvolatile memory controller in response to the plurality of data requests;
 - writing the plurality of data blocks to a plurality of nonvolatile memory devices by the plurality of command processing units;
 - generating a parity block in a page frame of a context memory by the parity calculator based on the plurality of data blocks;
 - determining that generation of the parity block is complete; and
 - writing the parity block to a nonvolatile memory device by a command processing unit of the plurality of command processing units based on the parity write command after determining generation of the parity block is complete.

16. The method of claim 15, wherein the plurality of data blocks is a sequence of data blocks, and wherein generating the parity block in the page frame of the context memory comprises:

initializing a parity block in the page frame by the parity calculator storing a first data block of the sequence of data blocks into the page frame; and

updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks.

17. The method of claim 16, wherein updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks comprises performing an operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks.

18. The method of claim 17, wherein the operation includes an exclusive-or operation.

19. The method of claim 16, further comprising:

initializing a stripe count to a predetermined value; and

decrementing the stripe count in response to each occurrence of updating the parity block, wherein determining generation of the parity block is complete comprises determining the stripe count has reached a threshold value.

20. The method of claim 15, wherein the context memory includes a plurality of page frames and each command of the plurality of commands includes a flow identifier, the method further comprising allocating a page frame in the context memory to the data stripe operation by associating the flow identifier with the page frame.

ABSTRACT OF THE DISCLOSURE

A nonvolatile memory controller performs a data stripe operation on data blocks by processing a collection of commands. The nonvolatile memory controller includes command processing units, each of which processes a command of the data stripe operation to store a data block into a nonvolatile memory device. A parity calculator in the nonvolatile memory controller receives the data blocks of the data stripe operation by receiving a sequence of data blocks. The parity calculator generates a parity block in a page frame as the parity calculator receives the sequence of the data blocks. A command processing unit in the nonvolatile memory controller determines when the parity calculator has completed generating the parity block and writes the parity block to a nonvolatile memory device.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IDT-2730C-UT
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Peter	Z.	Onufryk		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Flanders	State/Province	NJ	Country of Residence i	US
Citizenship under 37 CFR 1.41(b) i		US			
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Mailing Address of Applicant:					
Address 1	1368 Yukon Terrace				
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IDT-2730C-UT
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
Customer Number	33087		
Email Address	glass@patentforce.com	Add Email	Remove Email

Application Information:

Title of the Invention	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
Attorney Docket Number	IDT-2730C-UT	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	12	Suggested Figure for Publication (if any)	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☒	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Mr.	Greg		Warder		
Registration Number		50208			

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IDT-2730C-UT	
		Application Number		
Title of Invention	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE			

Prefix	Given Name	Middle Name	Family Name	Suffix	Remove
Mrs.	Jaya		Nair		
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Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	61374242	2011-08-16
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			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☐ No
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Assignee Information:

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Assignee 1			Remove
If the Assignee is an Organization check here. ☒			
Organization Name	Integrated Device Technology, Inc.		
Mailing Address Information:			
Address 1	6024 Silver Creek Valley Road		
Address 2			
City	San Jose	State/Province	CA
Country ⁱ	US	Postal Code	95138
Phone Number		Fax Number	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IDT-2730C-UT
		Application Number	
Title of Invention	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
Email Address			
Additional Assignee Data may be generated within this form by selecting the Add button.			
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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Kenneth Glass/			Date (YYYY-MM-DD)	2011-03-21
First Name	Kenneth	Last Name	Glass	Registration Number	42587

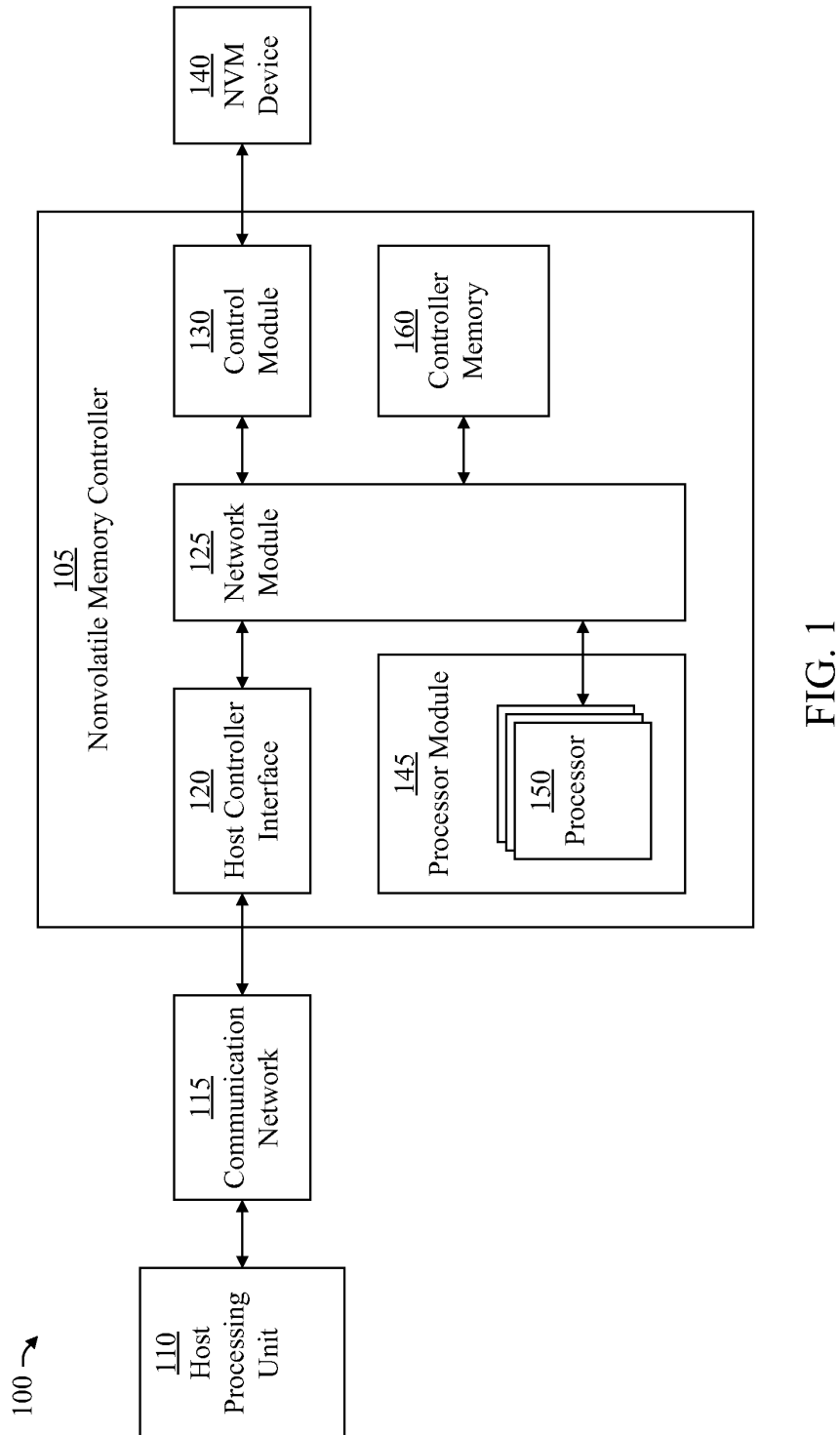
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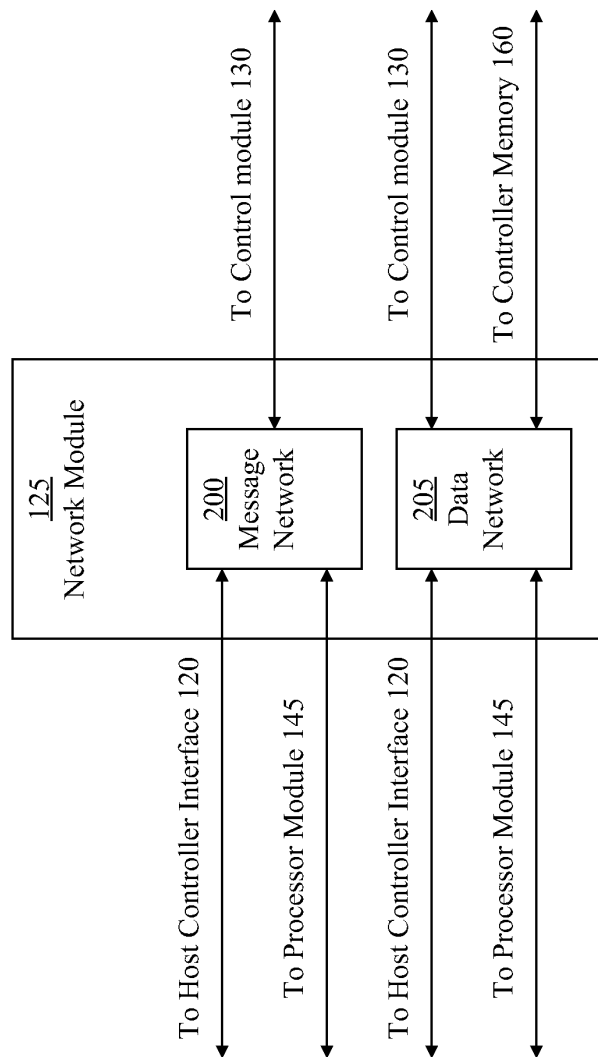


FIG. 2

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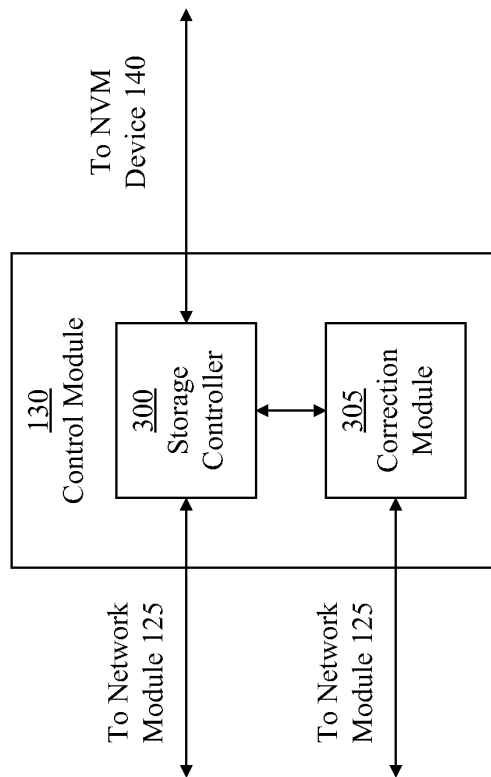
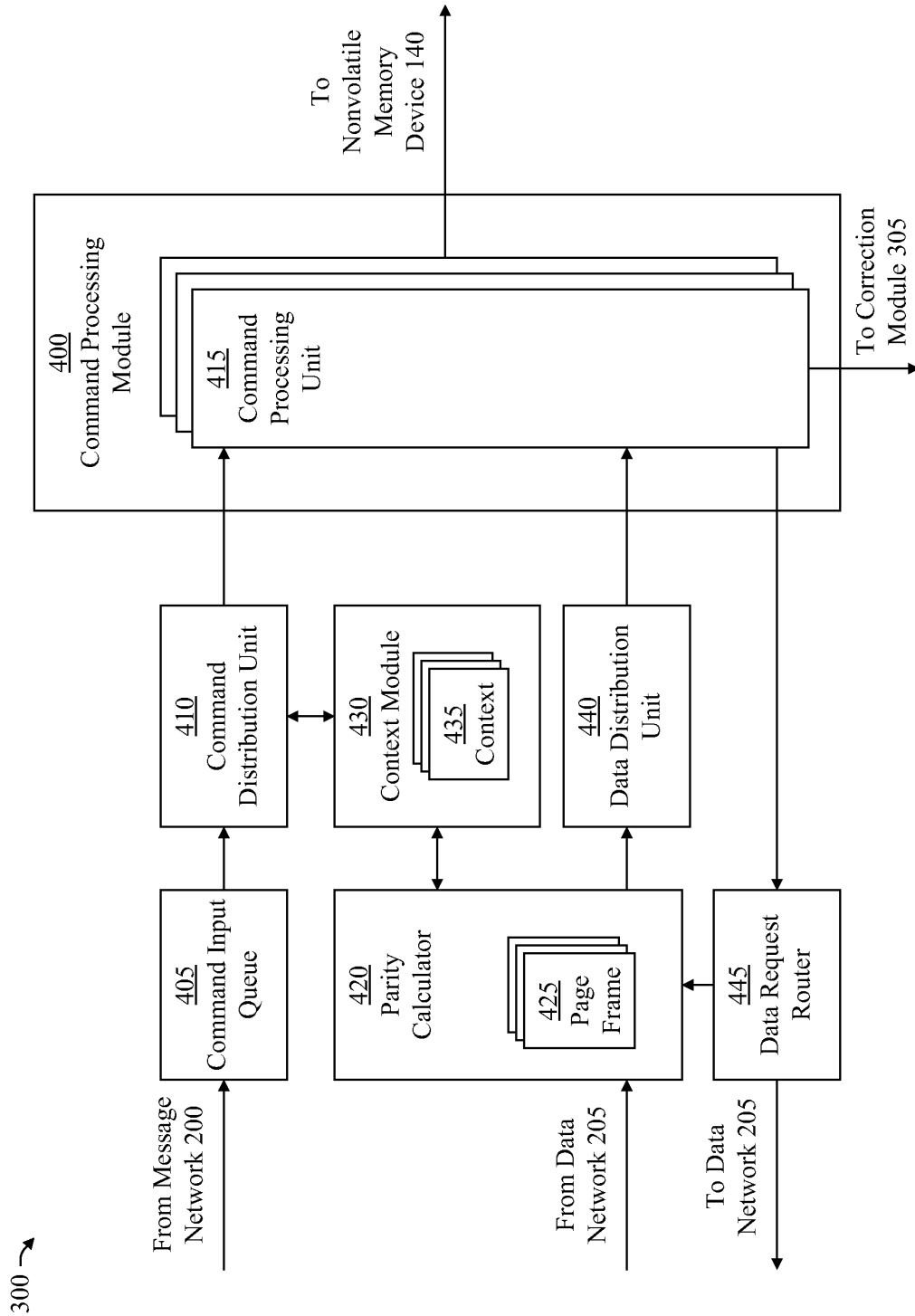


FIG. 3

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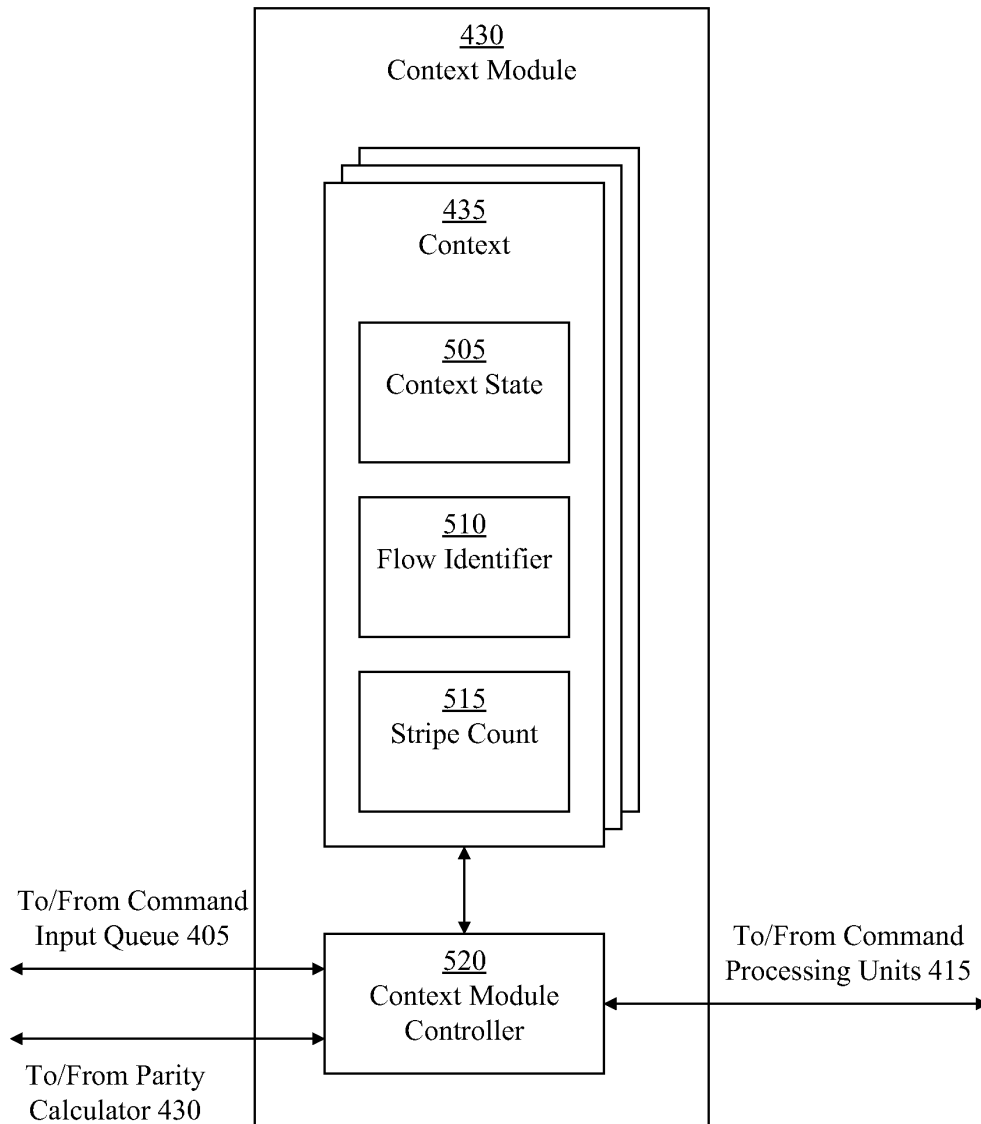


FIG. 5

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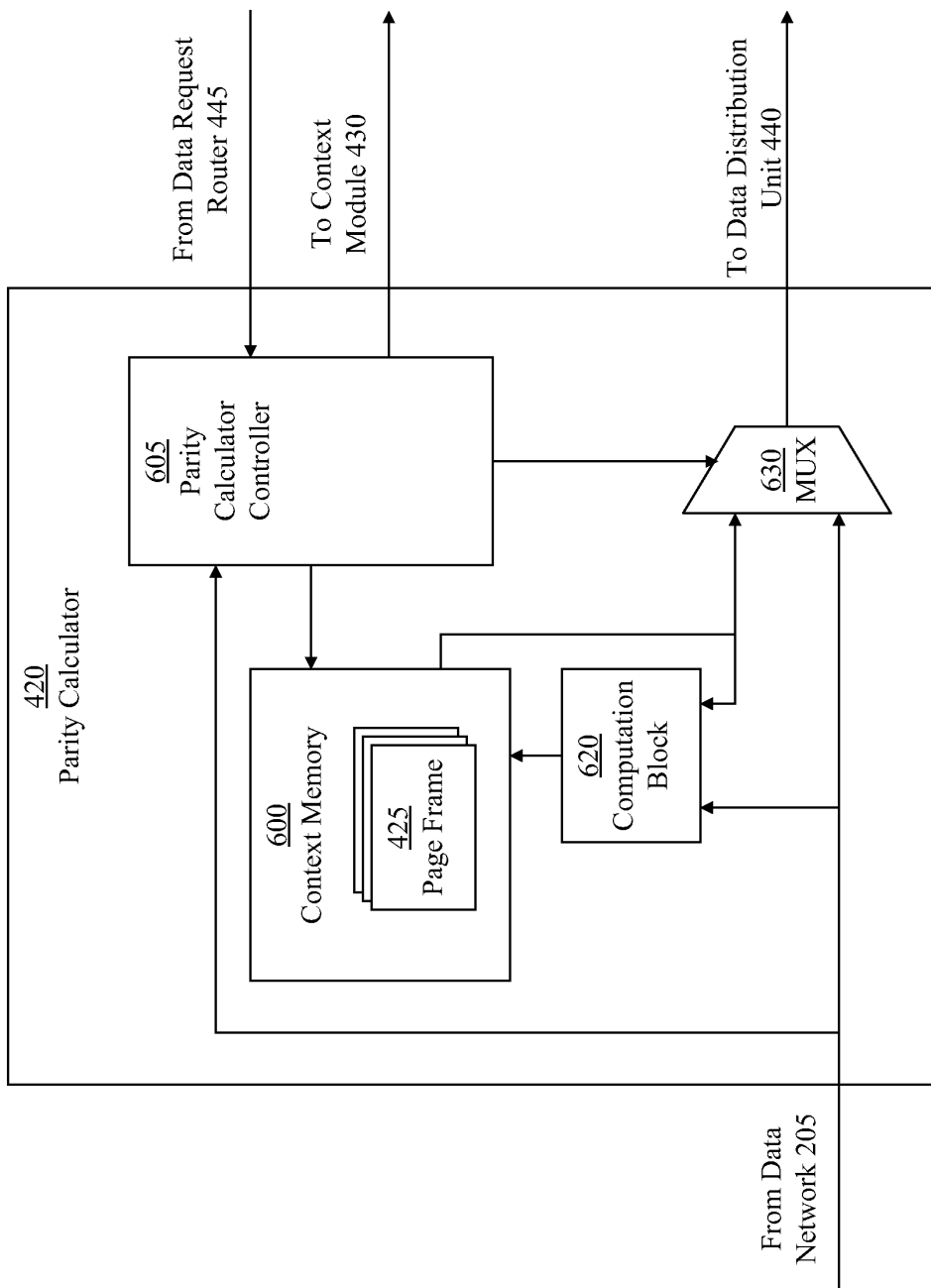


FIG. 6

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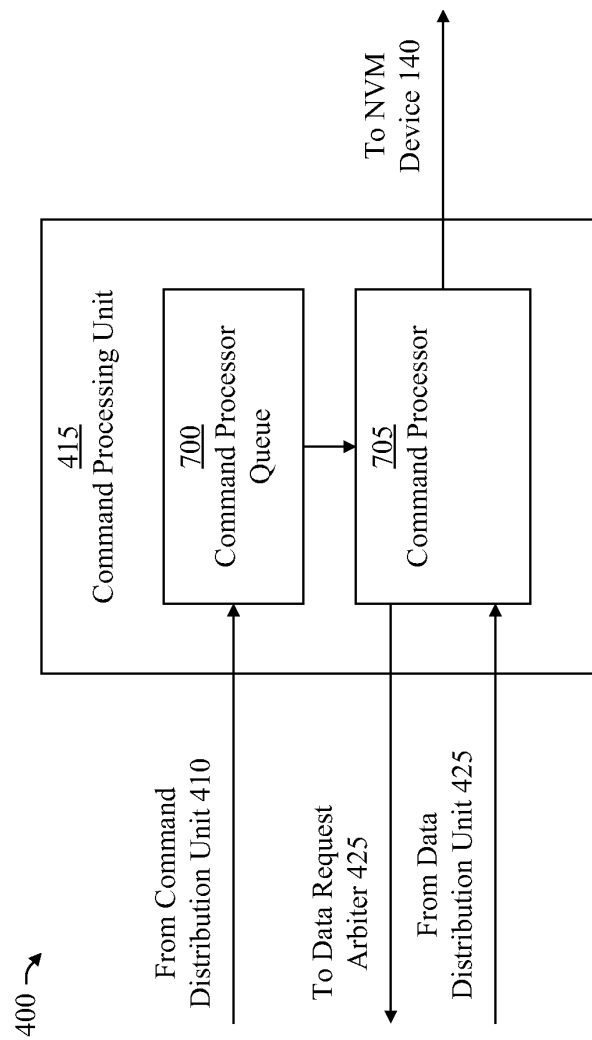


FIG. 7

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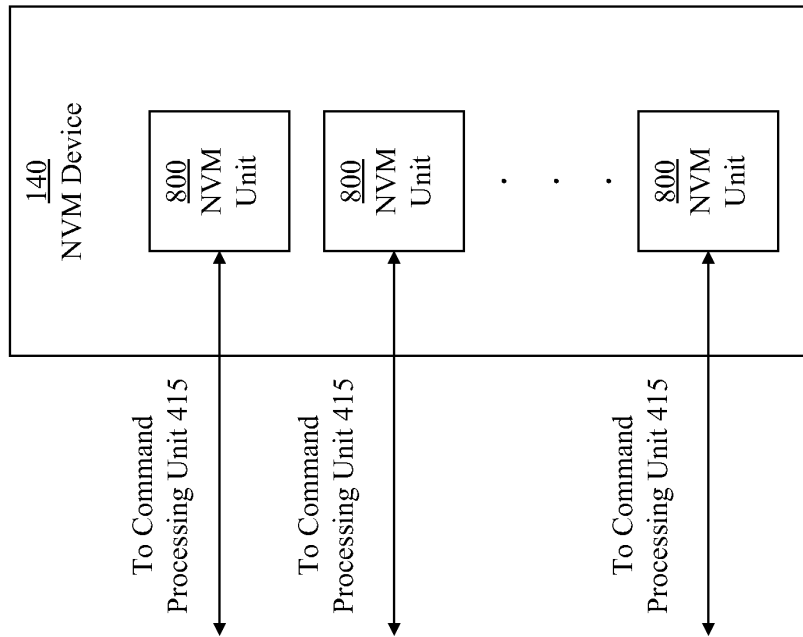


FIG. 8

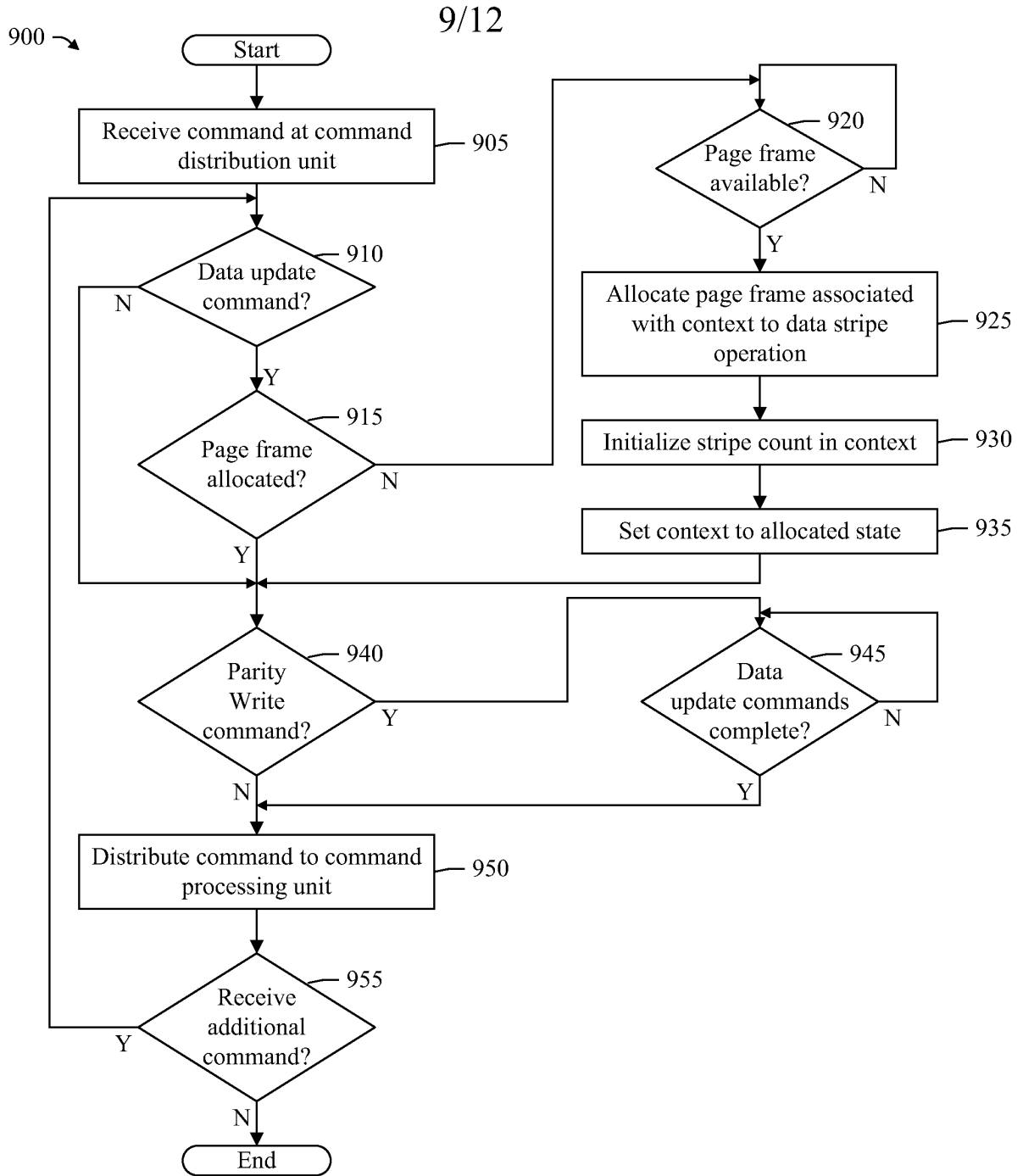


FIG. 9

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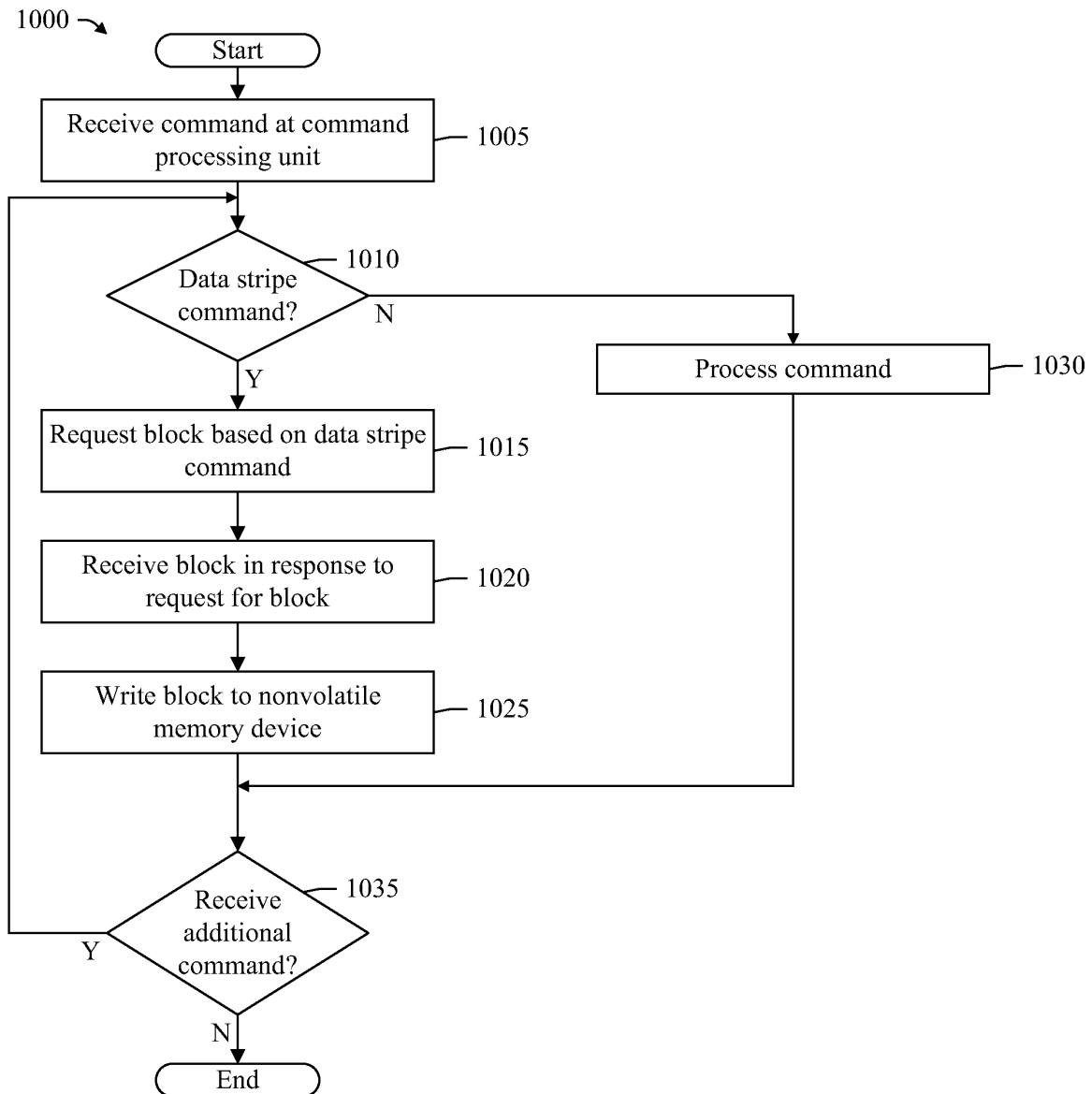


FIG. 10

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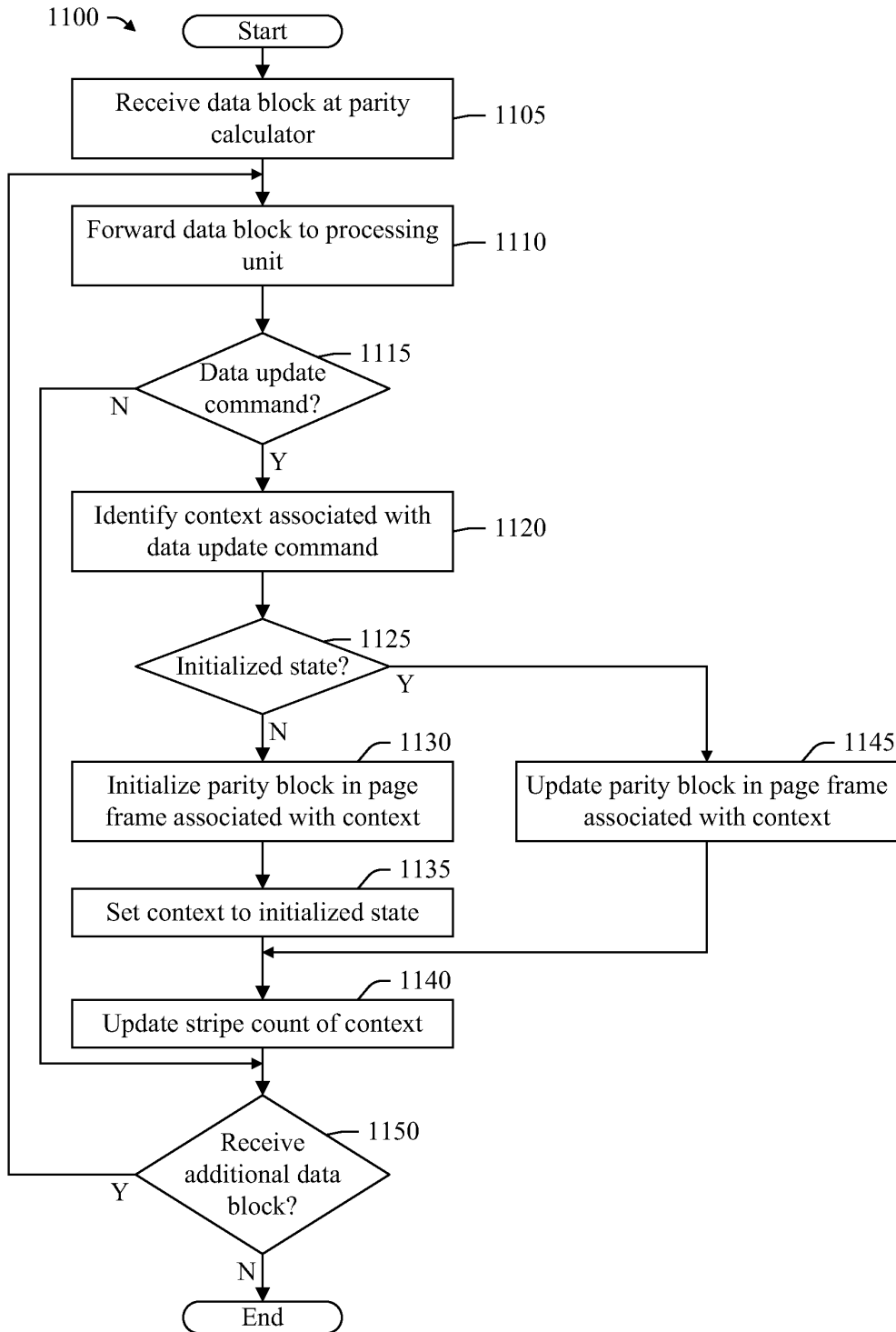


FIG. 11

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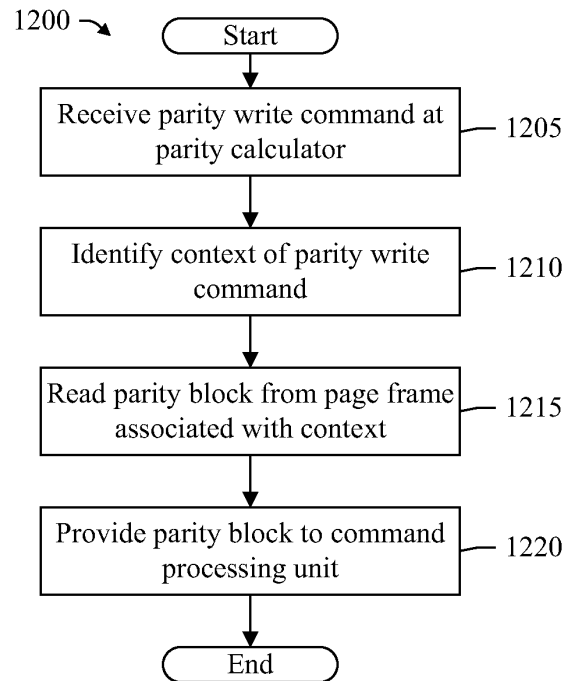


FIG. 12

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
First Named Inventor/Applicant Name:		Peter Z. Onufryk		
Filer:		Kenneth Glass		
Attorney Docket Number:		IDT-2730C-UT		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt	
EFS ID:	9703498
Application Number:	13052835
International Application Number:	
Confirmation Number:	7182
Title of Invention:	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730C-UT
Receipt Date:	21-MAR-2011
Filing Date:	
Time Stamp:	17:25:26
Application Type:	Utility under 35 USC 111(a)

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	2730C-Dec-n-POA.pdf	1147842	no	4
			3ef24c907a4bcffc163a306f25f1dbe763eb4511		
Warnings:					
Information:					
2		IDT-2730C- Specification-20110318-01f.pdf	163573	yes	58
			47ce60a53611b477ed75ec677d1bb4aa8b0f8fd51		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	48	
	Claims		49	57	
	Abstract		58	58	
Warnings:					
Information:					
3	Application Data Sheet	IDT-2730C-sb0014f.pdf	1031864	no	5
			706df11596ab11c99b6834030a01c64251bc3a14		
Warnings:					
Information:					
4	Drawings-only black and white line drawings	IDT-2730C- Drawings-20110321-01.pdf	45165	no	12
			794e86fe4052a110aeacf7e0cc4b5e38d1c53801		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	33176	no	2
			37f3cc237130370f39b8ba1d598233a9a47e5772		
Warnings:					
Information:					
Total Files Size (in bytes):			2421620		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	9703498
Application Number:	13052835
International Application Number:	
Confirmation Number:	7182
Title of Invention:	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730C-UT
Receipt Date:	21-MAR-2011
Filing Date:	
Time Stamp:	17:25:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1090
RAM confirmation Number	4709
Deposit Account	501006
Authorized User	GLASS,KENNETH
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	2730C-Dec-n-POA.pdf	1147842	no	4
			3ef24c907a4bcffc163a306f25f1dbe763eb4511		
Warnings:					
Information:					
2		IDT-2730C- Specification-20110318-01f.pdf	163573	yes	58
			47ce60a53611b477ed75ec677d4b4aa8b0f8fd51		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	48	
	Claims		49	57	
	Abstract		58	58	
Warnings:					
Information:					
3	Application Data Sheet	IDT-2730C-sb0014f.pdf	1031864	no	5
			706df11596ab11c99b6834030a01c64251bc3a14		
Warnings:					
Information:					
4	Drawings-only black and white line drawings	IDT-2730C- Drawings-20110321-01.pdf	45165	no	12
			794e86fe4052a110aeacf7e0cc4b5e38d1c53801		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	33176	no	2
			37f3cc237130370f39b8ba1d598233a9a47e5772		
Warnings:					
Information:					
Total Files Size (in bytes):			2421620		

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/052,835	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *			OR	x 52 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *			OR	x 220 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1090
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		OTHER THAN SMALL ENTITY	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/052,835	03/21/2011	2112	1090	IDT-2730C-UT	20	3

CONFIRMATION NO. 7182

33087
GLASS & ASSOCIATES
P.O. BOX 1220
LOS GATOS, CA 95031-1220

FILING RECEIPT



OC000000046865768

Date Mailed: 04/04/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Peter Z. Onufryk, Flanders, NJ;
Inna Levit, Sunnyvale, CA;

Assignment For Published Patent Application

INTEGRATED DEVICE TECHNOLOGY, INC., San Jose, CA

Power of Attorney:

Kenneth Glass--42587

Jaya Nair--46454

Stanley Pawlik--47850

Greg Warder--50208

Randall Krause--53158

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/374,242 08/16/2010 *

(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 03/30/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/052,835**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE

Preliminary Class

714

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835
	Filing Date		2011-03-21
	First Named Inventor	Peter Z. Onufryk	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		IDT-2730C-UT

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	7708195		2010-05-04	Yoshida et al.			
	2	7620784		2009-11-17	Panabaker, Ruston			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S. PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20100262979		2010-10-14	Borchers et al.			
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835
	Filing Date		2011-03-21
	First Named Inventor	Peter Z. Onufryk	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		IDT-2730C-UT

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

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Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13052835
	Filing Date	2011-03-21
	First Named Inventor	Peter Z. Onufryk
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IDT-2730C-UT

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kenneth Glass/	Date (YYYY-MM-DD)	2013-01-29
Name/Print	Kenneth Glass	Registration Number	42587

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	14824967
Application Number:	13052835
International Application Number:	
Confirmation Number:	7182
Title of Invention:	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730C-UT
Receipt Date:	29-JAN-2013
Filing Date:	21-MAR-2011
Time Stamp:	19:36:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2730C_IDS-1.pdf	611659 0a6b6d79398f37879c0afdbff7bd86a428f1a6b2	no	4

Warnings:

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13052835
	Filing Date	2011-03-21
	First Named Inventor	Peter Z. Onufryk
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IDT-2730C-UT

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	5875343		1999-02-23	Binford et al.			
	2	8244946		2012-08-14	Gupta et al.			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835
	Filing Date		2011-03-21
	First Named Inventor	Peter Z. Onufryk	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		IDT-2730C-UT

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	NVM Express, revision 1.0; Intel Corporation; pages 103-106 and 110-114; July 12, 2011.	☐

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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13052835
	Filing Date	2011-03-21
	First Named Inventor	Peter Z. Onufryk
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IDT-2730C-UT

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kenneth Glass/	Date (YYYY-MM-DD)	2013-02-14
Name/Print	Kenneth Glass	Registration Number	42587

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
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Electronic Acknowledgement Receipt	
EFS ID:	14963598
Application Number:	13052835
International Application Number:	
Confirmation Number:	7182
Title of Invention:	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730C-UT
Receipt Date:	14-FEB-2013
Filing Date:	21-MAR-2011
Time Stamp:	16:38:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	12730D-ref-cited-3052388.pdf	1067797 53dc44737dea06eb0190c61900f8f666e534c3e	no	10

Warnings:

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2	Information Disclosure Statement (IDS) Form (SB08)	2730C_IDS-2.pdf	611743 f13c694b93124e78ab983f8757ed381a3c283e33	no	4
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,835	03/21/2011	Peter Z. Onufryk	IDT-2730C-UT	7182
33087 7590 04/26/2013 GLASS & ASSOCIATES P.O. BOX 1220 LOS GATOS, CA 95031-1220			EXAMINER CHAUDRY, MUJTABA M	
			ART UNIT 2112	PAPER NUMBER
			MAIL DATE 04/26/2013	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/052,835	Applicant(s) ONUFTRYK ET AL.	
	Examiner MUJTABA K. CHAUDRY	Art Unit 2112	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 March 2011.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-20 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 21 March 2011 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some * c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

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- a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413) |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08) | Paper No(s)/Mail Date. ____. |
| Paper No(s)/Mail Date <u>1/29/13,2/14/13</u> . | 4) ☐ Other: ____. |

DETAILED ACTION

Application filed 3/21/2011 has examined.

- Claims 1-20 are pending.
- IDS have been considered.
- Specification and drawings are accepted.

Application is pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda

USPAP 20090077302 A1 in view of Yu et al. (USPAP 20100185808, herein: Yu).

As per claim 1, Fukuda substantially teaches (i.e., title and abstract) a nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks (i.e., Figure 1, reference number 3 and paragraph 0035), the nonvolatile memory controller comprising: a plurality of command processing units (i.e., Figure 1, reference number 17 and paragraph 0037), each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe operation (i.e., paragraphs 0036-0038), the plurality of commands including a plurality of data commands and a parity write command (i.e., Figure 2, reference number 21 and paragraphs 0044-0047), each command processing unit of the plurality of command processing units receiving a data command of the plurality of data commands configured to request a data block of the plurality of data blocks based on the data command (i.e., Figure 1, reference number 17, Figure 2 and paragraphs 0046-0051), receive the data block in response to the request, and write the data block to a nonvolatile memory device (i.e., paragraphs 0036-0038); and a parity calculator coupled to the plurality of command processing units (i.e., Figure 2, reference number 21), the parity calculator configured to receive the data blocks of the plurality of data blocks and generate a parity block based on the data blocks, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command (i.e., Figure 2, reference number 21 and paragraph 0045).

Fukuda does not explicitly teach the plurality of commands to include "data update commands" as stated in the present application.

However, Yu teaches in an analogous art (i.e., title and abstract) method and systems for storing and accessing data in UAS based flash memory device are disclosed. UAS based flash

memory device comprises a controller and a plurality of non-volatile memories (e.g., flash memory) it controls. Controller is configured for connecting to a UAS host via a physical layer (e.g., plug and wire based on USB 3.0) and for conducting data transfer operations via two sets of logical pipes. Controller further comprises a random-access-memory (RAM) buffer configured for enabling parallel and duplex data transfer operations through the sets of logical pipes. In addition, a Smart Storage Switch configured for connecting multiple non-volatile memory devices is included in the controller. Finally, a security module/engine/unit is provided for data security via user authentication data encryption/decryption of the device. Furthermore, the flash memory device includes an optical transceiver configured for optical connection to a host also configured with an optical transceiver. Particularly, Yu teaches (i.e., paragraph 0032) data transfer operations are sent from EUSB host as information unit (IU) with a specific tag number. Upon receiving the IU, EUSB device determines whether corresponding logic pipe is available. If so, physical flash memory channels are checked to ensure the data transfer operations can be performed. Multiple commands are kept in a queue and corresponding data sector buffer in the EUSB device's controller. Data update commands (e.g., write, erase/trim) are reordered and regrouped in the queue to increase the efficiency of overall data transfer operations when data ranges of data update commands overlap each other. Parallel data transfer operations are conducted with logical memory unit (e.g., unit having a different logical unit number (LUN). Each logical memory unit can be homogeneous or heterogeneous. A Smart Storage Switch is configured for accommodating such parallel operations. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to include "data update commands" within the list of commands of Fukuda. This would have been obvious to one having

ordinary skill because one of ordinary skill would have recognized that by including data update commands in the teachings of Fukuda would have improved the over efficiency of the transfer system.

As per claim 2, Fukuda substantially teaches, in view of above rejections, the parity calculator includes a context memory including a page frame, and the parity calculator is further configured to receive the plurality of data blocks as a sequence of data blocks and to generate the parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks (i.e., Figure 2, reference number 21 and paragraphs 0044-0045, 0103-0108).

As per claim 3, Fukuda substantially teaches, in view of above rejections, wherein the parity calculator is further configured to update the data block stored in the page frame by performing a logical operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks (i.e., Figure 2, reference number 21 and paragraph 0111).

As per claim 4, Fukuda substantially teaches, in view of above rejections, the logical operation includes an exclusive-or operation (i.e., Figure 2, reference number 21).

As per claim 5, Fukuda substantially teaches, in view of above rejections, a context associated with the page frame and including a stripe count for counting each occurrence of updating the parity block, the nonvolatile memory controller further comprising a command distribution unit configured to determine the parity block is generated by determining the stripe count has reached a threshold value (i.e., Figure 1, reference number 19, and paragraph 0111).

As per claim 6, Fukuda substantially teaches, in view of above rejections, the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units, determine generation of the parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete (i.e., Figure 1, reference numbers 17, 19 and Figure 2, reference number 21).

As per claim 7, Fukuda substantially teaches, in view of above rejections, a controller memory configured to store the plurality of data blocks; and a data network coupled to the controller memory, the plurality of command processing units, and the parity calculator, wherein the plurality of command processing units is further configured to request the plurality of data blocks by generating a plurality of data request packets, the controller memory is further configured to generate a plurality of completion packets including the plurality of data blocks, and both the parity calculator and the plurality of command processing units are further

configured to receive the plurality of data blocks through the data network (i.e., Figure 1, reference numbers 17, 19 and Figure 2, reference number 21).

As per claim 8, Fukuda substantially teaches, in view of above rejections, the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units, determine generation of the parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete (i.e., Figure 1, reference numbers 17, 19 and Figure 2, reference number 21).

As per claim 9, Fukuda substantially teaches, in view of above rejections, each command processing unit of the plurality of command processing units comprises a command processing unit command queue for storing commands distributed to the command processing unit from the command distribution unit (i.e., Figure 1, reference numbers 17, 19 and Figure 2, reference number 21).

As per claim 10, Fukuda substantially teaches, in view of above rejections, a context memory including a plurality of page frames, wherein each command of the plurality of commands includes a flow identifier, and the command distribution unit is further configured to allocate a page frame of the context memory to the data stripe operation by associating the flow

identifier with the page frame (i.e., Figure 1, reference numbers 17, 19 and Figure 2, reference number 21 and paragraph 0074).

As per claim 11, Fukuda substantially teaches, in view of above rejections, to perform a plurality of data stripe operations in parallel (i.e., Figure 1, reference number 17 in parallel).

As per claim 12, Fukuda substantially teaches (i.e., title and abstract) a nonvolatile memory controller comprising: a command distribution unit configured to receive a plurality of commands for performing a data stripe operation on a plurality of data blocks (i.e., Figure 1, reference number 3 and paragraph 0035), the plurality of commands comprising a plurality data commands and a parity write command (i.e., Figure 2, reference number 21 and paragraphs 0044-0047); a plurality of command processing units coupled to the command distribution unit (i.e., Figure 1, reference number 17 and paragraph 0037), the command distribution unit further configured to distribute the plurality of data commands among command processing units of the plurality of command processing units (i.e., Figure 1, reference number 19), each command processing unit receiving a data command configured to request a data block of the plurality of data blocks based on the data command (i.e., paragraphs 0036-0038), receive the data block in response to the request, and write the data block to a nonvolatile memory device (i.e., Figure 1, reference number 17, Figure 2 and paragraphs 0046-0051); and a parity calculator coupled to the plurality of command processing units (i.e., Figure 2, reference number 21), the parity calculator including a context memory including a page frame, the parity calculator configured to receive the data blocks of the plurality of data blocks as a sequence of data blocks, generate a parity

block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks (i.e., Figure 2, reference number 21 and paragraph 0045), the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete, the command processing unit receiving the parity write command configured to write the parity block into the nonvolatile memory device (i.e., Figure 2, reference number 21 and paragraph 0045).

Fukuda does not explicitly teach the plurality of commands to include "data update commands" as stated in the present application.

However, Yu teaches in an analogous art (i.e., title and abstract) method and systems for storing and accessing data in UAS based flash memory device are disclosed. UAS based flash memory device comprises a controller and a plurality of non-volatile memories (e.g., flash memory) it controls. Controller is configured for connecting to a UAS host via a physical layer (e.g., plug and wire based on USB 3.0) and for conducting data transfer operations via two sets of logical pipes. Controller further comprises a random-access-memory (RAM) buffer configured for enabling parallel and duplex data transfer operations through the sets of logical pipes. In addition, a Smart Storage Switch configured for connecting multiple non-volatile memory devices is included in the controller. Finally, a security module/engine/unit is provided for data security via user authentication data encryption/decryption of the device. Furthermore, the flash memory device includes an optical transceiver configured for optical connection to a

host also configured with an optical transceiver. Particularly, Yu teaches (i.e., paragraph 0032) data transfer operations are sent from EUSB host as information unit (IU) with a specific tag number. Upon receiving the IU, EUSB device determines whether corresponding logic pipe is available. If so, physical flash memory channels are checked to ensure the data transfer operations can be performed. Multiple commands are kept in a queue and corresponding data sector buffer in the EUSB device's controller. Data update commands (e.g., write, erase/trim) are reordered and regrouped in the queue to increase the efficiency of overall data transfer operations when data ranges of data update commands overlap each other. Parallel data transfer operations are conducted with logical memory unit (e.g., unit having a different logical unit number (LUN)). Each logical memory unit can be homogeneous or heterogeneous. A Smart Storage Switch is configured for accommodating such parallel operations. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to include "data update commands" within the list of commands of Fukuda. This would have been obvious to one having ordinary skill because one of ordinary skill would have recognized that by including data update commands in the teachings of Fukuda would have improved the over efficiency of the transfer system.

As per claim 13, Fukuda substantially teaches, in view of above rejections, the plurality of command processing units is further configured to process the plurality of data update commands in an arbitrary order (i.e., Figure 1, reference numbers 17 and 19).

As per claim 14, Fukuda substantially teaches, in view of above rejections, the context memory includes a plurality of page frames for storing a plurality of parity blocks of a plurality of data stripe operations, and wherein the plurality of command processing units is further configured to perform the plurality of data stripe operations in parallel (i.e., Figure 1, reference numbers 17 and 19).

As per claim 15, Fukuda substantially teaches (i.e., title and abstract) a method of generating parity data (i.e., Figure 2, reference number 21), the method comprising: distributing a plurality of commands for performing the data stripe operation among a plurality of command processing units in the nonvolatile memory controller (i.e., Figure 1, reference numbers 3, 19 and paragraph 0035), the plurality of commands including a plurality of data commands and a parity write command (i.e., Figure 2, reference number 21 and paragraphs 0044-0047); generating a plurality of data requests by the plurality of command processing units based on the plurality of data commands (i.e., Figure 1, reference number 17 and paragraph 0037); receiving a plurality of data blocks at the plurality of command processing units (i.e., paragraphs 0036-0038) and at a parity calculator of the nonvolatile memory controller in response to the plurality of data requests (i.e., Figure 2, reference number 21); writing the plurality of data blocks to a plurality of nonvolatile memory devices by the plurality of command processing units (i.e., Figure 1, reference number 17, Figure 2 and paragraphs 0046-0051); generating a parity block in a page frame of a context memory by the parity calculator based on the plurality of data blocks ; determining that generation of the parity block is complete (i.e., Figure 2, reference number 21 and paragraph 0045); and writing the parity block to a nonvolatile memory device by a command

processing unit of the plurality of command processing units based on the parity write command after determining generation of the parity block is complete (i.e., Figure 2, reference number 21 and paragraph 0045).

Fukuda does not explicitly teach the plurality of commands to include "data update commands" as stated in the present application.

However, Yu teaches in an analogous art (i.e., title and abstract) method and systems for storing and accessing data in UAS based flash memory device are disclosed. UAS based flash memory device comprises a controller and a plurality of non-volatile memories (e.g., flash memory) it controls. Controller is configured for connecting to a UAS host via a physical layer (e.g., plug and wire based on USB 3.0) and for conducting data transfer operations via two sets of logical pipes. Controller further comprises a random-access-memory (RAM) buffer configured for enabling parallel and duplex data transfer operations through the sets of logical pipes. In addition, a Smart Storage Switch configured for connecting multiple non-volatile memory devices is included in the controller. Finally, a security module/engine/unit is provided for data security via user authentication data encryption/decryption of the device. Furthermore, the flash memory device includes an optical transceiver configured for optical connection to a host also configured with an optical transceiver. Particularly, Yu teaches (i.e., paragraph 0032) data transfer operations are sent from EUSB host as information unit (IU) with a specific tag number. Upon receiving the IU, EUSB device determines whether corresponding logic pipe is available. If so, physical flash memory channels are checked to ensure the data transfer operations can be performed. Multiple commands are kept in a queue and corresponding data sector buffer in the EUSB device's controller. Data update commands (e.g., write, erase/trim) are

reordered and regrouped in the queue to increase the efficiency of overall data transfer operations when data ranges of data update commands overlap each other. Parallel data transfer operations are conducted with logical memory unit (e.g., unit having a different logical unit number (LUN). Each logical memory unit can be homogeneous or heterogeneous. A Smart Storage Switch is configured for accommodating such parallel operations. Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to include "data update commands" within the list of commands of Fukuda. This would have been obvious to one having ordinary skill because one of ordinary skill would have recognized that by including data update commands in the teachings of Fukuda would have improved the over efficiency of the transfer system.

As per claim 16, Fukuda substantially teaches, in view of above rejections, the plurality of data blocks is a sequence of data blocks, and wherein generating the parity block in the page frame of the context memory comprises: initializing a parity block in the page frame by the parity calculator storing a first data block of the sequence of data blocks into the page frame; and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks (i.e., Figure 2, reference number 21 and paragraphs 0044-0045, 0103-0108).

As per claim 17, Fukuda substantially teaches, in view of above rejections, wherein updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks comprises performing an operation on the data block stored

in the page frame and a data block following the first data block in the sequence of data blocks (i.e., Figure 2, reference number 21 and paragraph 0111).

As per claim 18, Fukuda substantially teaches, in view of above rejections, the operation includes an exclusive-or operation (i.e., Figure 2, reference number 21).

As per claim 19, Fukuda substantially teaches, in view of above rejections, initializing a stripe count to a predetermined value; and decrementing the stripe count in response to each occurrence of updating the parity block, wherein determining generation of the parity block is complete comprises determining the stripe count has reached a threshold value (i.e., Figure 1, reference number 19, and paragraph 0111).

As per claim 20, Fukuda substantially teaches, in view of above rejections, the context memory includes a plurality of page frames and each command of the plurality of commands includes a flow identifier, the method further comprising allocating a page frame in the context memory to the data stripe operation by associating the flow identifier with the page frame (i.e., Figure 1, reference numbers 17, 19 and Figure 2, reference number 21 and paragraph 0074).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See Pto-892 attached.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MUJTABA K. CHAUDRY whose telephone number is (571)272-3817. The examiner can normally be reached on Mon-Fri 9-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MUJTABA K CHAUDRY
Primary Examiner
Art Unit 2112

/MUJTABA K CHAUDRY/
Primary Examiner, Art Unit 2112

Notice of References Cited	Application/Control No. 13/052,835		Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.	
	Examiner MUJTABA K. CHAUDRY		Art Unit 2112	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2011/0161678 A1	06-2011	NIWA, Yasuyuki	713/193
*	B	US-2008/0320214 A1	12-2008	Ma et al.	711/103
*	C	US-2009/0077302 A1	03-2009	Fukuda, Hideaki	711/103
*	D	US-2010/0185808 A1	07-2010	Yu et al.	711/103
	E	US-			
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Doc description: Information Disclosure Statement (IDS) Filed

13052835 - GAU:2112

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835	
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730C-UT	

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	1	7708195		2010-05-04	Yoshida et al.			
	2	7620784		2009-11-17	Panabaker, Ruston			
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	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730C-UT	

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	1	5875343		1999-02-23	Binford et al.			
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	First Named Inventor	Peter Z. Onufryk	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		IDT-2730C-UT

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	1	NVM Express, revision 1.0; Intel Corporation; pages 103-106 and 110-114; July 12, 2011.	☐

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SERIAL NUMBER 13/052,835	FILING or 371(c) DATE 03/21/2011 RULE	CLASS 714	GROUP ART UNIT 2112	ATTORNEY DOCKET NO. IDT-2730C-UT		
APPLICANTS Peter Z. Onufryk, Flanders, NJ; Inna Levit, Sunnyvale, CA; ** CONTINUING DATA ***** This appln claims benefit of 61/374,242 08/16/2010 * (*)Data provided by applicant is not consistent with PTO records. ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/30/2011						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /M. MUJTABA M Acknowledged CHAUDRY/ Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY NJ	SHEETS DRAWINGS 12	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS GLASS & ASSOCIATES P.O. BOX 1220 LOS GATOS, CA 95031-1220 UNITED STATES						
TITLE SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

<i>Index of Claims</i> 	Application/Control No. 13052835	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
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✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
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☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	04/24/2013								
	1	✓								
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	18	✓								
	19	✓								
	20	✓								

Search Notes 	Application/Control No. 13052835	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
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Class	Subclass	Date	Examiner
711	103	4/23/2013	MC
714	764	4/23/2013	MC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST DATABASE	4/23/2013	MC
USPAT	4/23/2013	MC
USPGPUBS	4/23/2013	MC
EPO	4/23/2013	MC
JPO	4/23/2013	MC
DERWANT	4/23/2013	MC
IBM-TDB	4/23/2013	MC
GOOGLE NPL/IEEE	4/23/2013	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7416	711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 18:20
L2	532	714/764.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 18:20
L3	4	("5875343" "8244946").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 18:22
L4	3	"20080256280"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 18:23
L5	4	("5875343" "8244946" "7708195" "7620784").pn.	USPAT	OR	OFF	2013/04/24 18:23
L6	1	"20080256280" "20100262979"	USPAT	OR	OFF	2013/04/24 18:24
L7	2	"20080256280" "20100262979"	US-PGPUB	OR	OFF	2013/04/24 18:24
S1	6183	(memory) with (read\$3 and compar\$3 and writ\$3 and error\$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 06:54
S2	286	memory with read\$3 with compar\$3 with writ\$3 with error\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 06:54
S3	88	(memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 07:08

S4	16	(memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC) and interleav\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 06:56
S5	13	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 10:24
S6	1	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 07:09
S7	12	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 07:09
S8	13	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).ab. not ((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 11:08
S9	1	(read and write) near (memory) near (ECC "error detection" "error correction")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/01/27 17:00
S10	1	(read and write) near (memory) near (ECC "error detection" "error correction")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/27 17:01
S11	2	"5784393".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/04 13:35
S12	987	714/763.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/23 20:27
S13	58	714/763.ccls. and (read near request)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/23 20:27
S14	64	714/763.ccls. and (read near request) and process\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/23 20:27
S15	67	714/763.ccls. and (read near request) and process\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2006/07/17 19:17

			IBM_TDB			
S16	2	"5485473".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 11:38
S17	4	("5313464" "5343426").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/05 14:40
S18	1581	714/758.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:22
S19	109	714/768.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:20
S20	80	714/767.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:19
S21	1075	714/763.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:20
S22	1	((writ\$3 read\$3) near memory) and interleav\$3 and "error correction algorithm").clm.	US-PGPUB	OR	OFF	2006/12/05 15:24
S23	31178	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:09
S24	650	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3)) and (page near buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:09
S25	15028	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3)) and (buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:09
S26	1062	((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (error near information))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:10
S27	388	((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (error adj information))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:10

S28	51	((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (reduc\$3 near (data bit))) and (buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:12
S29	261	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3)) and (error with correct\$3 with (stor\$3 restor\$3 rewrite) with (reduc\$3 compress\$3 less) with (bits data))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:14
S30	9	((nonvolatile "non-volatile") with memory) and (error with correct\$3 with (after then restor\$3) with ((reduc\$3 short\$5 less compress) near (data amount bits)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:15
S31	379	Noguchi.in. and Mitsuhiro.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 19:49
S32	1	((((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (reduc\$3 near (data bit))) and (buffer) and (control near circuit) and (reduc\$3 with bits)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 19:51
S33	6	("5475693" "6353553" "6549459").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/24 16:47
S34	3	("5475693" "6353553" "6549459").pn.	USPAT	OR	ON	2010/02/24 16:47
S35	615	714/763.ccls.	USPAT	OR	ON	2010/02/24 19:23
S36	623	714/710.ccls.	USPAT	OR	ON	2010/02/24 19:23
S38	0	mujtaba.xa. and chaudry.xa. and MPEFEC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/02/25 14:51
S39	0	mujtaba.xa. and chaudry.xa. and MPEFEC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:51
S40	0	mujtaba.xa. and chaudry.xa. and MPE-FEC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:51
S41	0	mujtaba.xa. and chaudry.xa. and (multi adj protocol) and (error near (detect\$3 correct\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:52
S42	123	mujtaba.xa. and chaudry.xa. and (error near (detect\$3 correct\$3))	US-PGPUB; USPAT;	OR	ON	2010/02/25 14:52

			EPO; JPO; DERWENT; IBM_TDB			
S43	186	mujtaba.xa. and chaudry.xa.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:52
S44	2	mujtaba.xa. and chaudry.xa. and tuner	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:53
S45	17	mujtaba.xa. and chaudry.xa. and (tuner (radio near frequency))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:54
S46	1	mujtaba.xa. and chaudry.xa. and (tuner and(radio near frequency))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:54
S47	0	(nonvolatile near (stor\$3 memory) near controller) and (command near processing near units) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:12
S48	25	(nonvolatile near (stor\$3 memory) near controller) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:15
S49	131	((nonvolatile flash) near (stor\$3 memory) near controller) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:16
S50	162	((((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:16
S51	14	((((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (command near (plurality multiple several two various)) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:17
S52	14	((((nonvolatile flash) near (stor\$3	US-PGPUB;	OR	ON	2013/04/23

		memory) near controller)((nonvolatile flash) near controller)) and (commands near (plurality multiple several two various)) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:18
S53	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (commands near (plurality multiple several two various)) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3)) and (data near command) and (parity near command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:18
S54	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:19
S55	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 15:23
S56	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3)) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 15:37
S57	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 07:49
S58	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (update adj (command instruction)) and (parity near command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 14:53
S59	0	((nonvolatile flash) near (stor\$3	US-PGPUB;	OR	ON	2013/04/24

		memory) near controller)((nonvolatile flash) near controller)) and (update near (command instruction)) and (parity near command)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			14:53
S60	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (update near (command instruction)) and (parity near (instruction command))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 14:53
S61	48	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:04
S62	29	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller)) and ((data update) near (command instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:05
S63	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller)) and ((data update) near (command instruction)) and (parity near (command instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:05
S64	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller)) and ((data update) near (command instruction)) and (parity near (generat\$3 calculat\$3 determin\$5))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:08
S65	566651	((nonvolatile flash) near (stor\$3 memory))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:23
S66	6015	((nonvolatile flash) near (stor\$3 memory)) and (controller with ((plurality multiple several two) near (process\$3 units)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:23
S67	383	((nonvolatile flash) near (stor\$3 memory)) and (controller with ((plurality multiple several two) near (process\$3 units))) and parity	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/04/24 15:24

			EPO; JPO; DERWENT; IBM_TDB			
S68	4	((nonvolatile flash) near (stor\$3 memory)) and (controller with ((plurality multiple several two) near (process\$3 units))) and (parity near command) and ((data update) near command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:25
S69	127	(data adj update adj command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 16:50
S70	57	(data adj update adj command) and (flash non-volatile nonvolatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:54
S71	2	(data adj update adj command) and (flash non-volatile nonvolatile) and parity	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:54
S72	5	(data adj update adj command) same (flash non-volatile nonvolatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:56
S73	36	(data adj update adj command) and ((flash non-volatile nonvolatile) near memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:58
S74	8	(data adj update adj command) and (((flash non-volatile nonvolatile) near memory) same controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:59
S75	8	(data adj update adj commands) and (((flash non-volatile nonvolatile) near memory) same controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 17:02
S76	3	"20100185808"	US-PGPUB; USPAT;	OR	ON	2013/04/24 17:07

EAST Search History

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
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EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S37	8	(((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (reduc\$3 near (data bit))) and (buffer) and (control near circuit) and (reduc\$3 with bits))	USPAT; UPAD	OR	ON	2010/02/24 19:47

4/ 24/ 2013 6:26:47 PM

C:\Users\mchaudry\Documents\EAST\Workspaces\13052835.wsp

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835	
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730C-UT	

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	1	20110161678		2011-06-30	Niwa, Yasuyuki			
	2	20080320214		2008-12-25	Ma et al.			
	3	20090077302		2009-03-19	Fukuda, Hideaki			
	4	20100185808		2010-07-22	Yu et al.			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835	
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number	IDT-2730C-UT		

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	1	NVM Express, Revision 1.0; Intel Corporation; March 1, 2011.	☐

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Examiner Signature		Date Considered	
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13052835
	Filing Date	2011-03-21
	First Named Inventor	Peter Z. Onufryk
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IDT-2730C-UT

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kenneth Glass/	Date (YYYY-MM-DD)	2013-05-06
Name/Print	Kenneth Glass	Registration Number	42587

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13052835		
Filing Date:		21-Mar-2011		
Title of Invention:		SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
First Named Inventor/Applicant Name:		Peter Z. Onufryk		
Filer:		Kenneth Glass		
Attorney Docket Number:		IDT-2730C-UT		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	15695844
Application Number:	13052835
International Application Number:	
Confirmation Number:	7182
Title of Invention:	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730C-UT
Receipt Date:	06-MAY-2013
Filing Date:	21-MAR-2011
Time Stamp:	12:21:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$180
RAM confirmation Number	10304
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Information Disclosure Statement (IDS) Form (SB08)	2730C_IDS-3.pdf	611823 3e4bf41ed045919d5a4d00ca2e949d5bde56f260	no	4
Warnings:					
Information:					
2	Non Patent Literature	NVM_Express_1_0_Gold-pdfprint.pdf	16740013 180f22fa03f3454fd07b57af190264b2431dbfdf	no	122
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30584 34c424f19e7184cf16b3e1cebbda55b7a99777ac	no	2
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Total Files Size (in bytes):			17382420		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Peter Z. Onyfryk

Practitioner's Docket No.: IDT-2730C-UT

Filing Date: 03/21/2011

For: SYSTEM AND METHOD FOR
GENERATING PARITY DATA IN A
NONVOLATILE MEMORY CONTROLLER
BY USING A DISTRIBUTED PROCESSING
TECHNIQUE

Serial No.: 13/052,835

Examiner: Chaudry, Mujtaba M.

Art Unit: 2112

Confirmation No. 7182

Mail Stop Amendment
Commissioner for Patent
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following response is presented in response to the Non-Final Examiner's Action having an electronic notification date of April 26, 2013.

AMENDMENT A

(37 C.F.R. § 1.121)

Amendments to the claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.

Serial No.: 13/052, 835

1 of 17

IDT-2730C-UT

AMENDMENTS TO THE CLAIMS:

Please replace the claim set with the following complete set of claims.

Claim 1 (Currently Amended) A nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, the nonvolatile memory controller comprising:

a plurality of command processing units, each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe operation, the plurality of commands including a plurality of data update commands and a parity write command, each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator further comprising a context memory including a page frame, the parity calculator configured to receive the data blocks of the plurality of data blocks as a sequence of data blocks, and to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer, based on the data blocks, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command.

Claim 2 (Cancelled)

Claim 3 (Cancelled) The nonvolatile memory controller of claim 12, wherein the parity calculator is further configured to update the data block stored in the page frame by performing a logical operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks.

Claim 4 (Original) The nonvolatile memory controller of claim 3, wherein the logical operation includes an exclusive-or operation.

Claim 5 (Currently Amended) The nonvolatile memory controller of claim 12, further comprising a context associated with the page frame and including a stripe count for counting each occurrence of updating the parity block, the nonvolatile memory controller further comprising a command distribution unit configured to determine the parity block is generated by determining the stripe count has reached a threshold value.

Claim 6 (Original) The nonvolatile memory controller of claim 1, wherein the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units, determine generation of the parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete.

Claim 7 (Original) The nonvolatile memory controller of claim 1, further comprising:

a controller memory configured to store the plurality of data blocks; and

a data network coupled to the controller memory, the plurality of command processing units, and the parity calculator, wherein the plurality of command processing units is further configured to request the plurality of data blocks by generating a plurality of data request packets, the controller memory is further configured to generate a plurality of completion packets including the plurality of data blocks, and both the parity calculator and the plurality of command processing units are further configured to receive the plurality of data blocks through the data network.

Claim 8 (Original) The nonvolatile memory controller of claim 7, wherein the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units, determine generation of the parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete.

Claim 9 (Original) The nonvolatile memory controller of claim 8, wherein each command processing unit of the plurality of command processing units comprises a command processing unit command queue for storing commands distributed to the command processing unit from the command distribution unit.

Claim 10 (Original) The nonvolatile memory controller of claim 8, further comprising a context memory including a plurality of page frames, wherein each command of the plurality of commands includes a flow identifier, and the command distribution unit is further configured to allocate a page frame of the context memory to the data stripe operation by associating the flow

identifier with the page frame.

Claim 11 (Original) The nonvolatile memory controller of claim 1, wherein the plurality of command processing units is further configured to perform a plurality of data stripe operations in parallel.

Claim 12 (Currently Amended) A nonvolatile memory controller comprising:

a command distribution unit configured to receive a plurality of commands for performing a data stripe operation on a plurality of data blocks, the plurality of commands comprising a plurality of data update commands and a parity write command;

a plurality of command processing units coupled to the command distribution unit, the command distribution unit further configured to distribute the plurality of data update commands among command processing units of the plurality of command processing units, each command processing unit receiving a data update command configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator including a context memory including a page frame, the parity calculator configured to receive the data blocks of the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks by performing an

exclusive-or operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks, the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete, the command processing unit receiving the parity write command configured to write the parity block into the nonvolatile memory device.

Claim 13 (Original) The nonvolatile memory controller of claim 12, wherein the plurality of command processing units is further configured to process the plurality of data update commands in an arbitrary order.

Claim 14 (Original) The nonvolatile memory controller of claim 13, wherein the context memory includes a plurality of page frames for storing a plurality of parity blocks of a plurality of data stripe operations, and wherein the plurality of command processing units is further configured to perform the plurality of data stripe operations in parallel.

Claim 15 (Currently Amended) A method of generating parity data, the method comprising:

distributing a plurality of commands for performing the data stripe operation among a plurality of command processing units in the nonvolatile memory controller, the plurality of commands including a plurality of data update commands and a parity write command;

generating a plurality of data requests by the plurality of command processing units based on the plurality of data update commands;

receiving a plurality of data blocks at the plurality of command processing units and at a parity calculator of the nonvolatile memory controller in response to the plurality of data requests;

writing the plurality of data blocks to a plurality of nonvolatile memory devices by the plurality of command processing units;

generating a parity block in a page frame of a context memory by the parity calculator based on the plurality of data blocks by initializing a parity block in the page frame by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer;

determining that generation of the parity block is complete; and

writing the parity block to a nonvolatile memory device by a command processing unit of the plurality of command processing units based on the parity write command after determining generation of the parity block is complete.

Claim 16 (Cancelled)

Claim 17 (Currently Amended) The method of claim 15 ~~46~~, wherein updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks comprises performing an operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks.

Claim 18 (Original) The method of claim 17, wherein the operation includes an exclusive-or

operation.

Claim 19 (Currently Amended) The method of claim 15 ~~46~~, further comprising:

initializing a stripe count to a predetermined value; and

decrementing the stripe count in response to each occurrence of updating the parity block,
wherein determining generation of the parity block is complete comprises determining
the stripe count has reached a threshold value.

Claim 20 (Original) The method of claim 15, wherein the context memory includes a plurality of
page frames and each command of the plurality of commands includes a flow identifier, the
method further comprising allocating a page frame in the context memory to the data stripe
operation by associating the flow identifier with the page frame.

REMARKS:

Applicant has carefully studied the Non-Final Examiner's Action mailed on April 26, 2013 and all references cited therein.

These explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Claim Rejections – 35 U.S.C. § 103

Applicant acknowledges the quotation of 35 U.S.C § 103(a).

Claims 1-20 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Fukuda (USPAP 10090077302 A1) in view of Yu et al. (USPAP 201000185808).

Independent claim 1 has been amended to more clearly describe that which the Applicant regards as the invention. Amended claim 1 recites:

A nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, the nonvolatile memory controller comprising:

a plurality of command processing units, each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe operation, the plurality of commands including a plurality of data update commands and a parity write command, each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands

configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator further comprising a context memory including a page frame, the parity calculator configured to receive the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command.

The elements of claim 2 have been incorporated into independent claim 1. Claim 2 has been cancelled.

In accordance with amended independent claim 1, the parity calculator is configured to “receive the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command”. As such, the parity calculator updates the data block stored

in the page frame with each data block in the sequence of data blocks, without storing each data block in a data buffer.

Applicant contends, that neither Fukuda nor Yu, alone or in combination, teach the claim element of amended claim 1 which recites, “a parity calculator coupled to the plurality of command processing units, the parity calculator further comprising a context memory including a page frame, the parity calculator configured to receive the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command”.

For the reasons presented above, Applicant contends that amended claim 1 is patentable over Fukuda in view of Yu et al., and is believed to be in condition for allowance.

Claims 3-11 are dependent upon claim 1, which has been shown to be allowable, and are therefore allowable as a matter of law.

Independent claim 12 has been amended to more clearly describe that which the Applicant regards as the invention. Amended claim 12 recites:

A nonvolatile memory controller comprising:

a command distribution unit configured to receive a plurality of commands for performing a data stripe operation on a plurality of data blocks, the plurality of commands comprising a plurality of data update commands and a parity write command;

a plurality of command processing units coupled to the command distribution unit, the command distribution unit further configured to distribute the plurality of data update commands among command processing units of the plurality of command processing units, each command processing unit receiving a data update command configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator including a context memory including a page frame, the parity calculator configured to receive the data blocks of the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame by performing an exclusive-or operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks, the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete, the

command processing unit receiving the parity write command configured to write the parity block into the nonvolatile memory device.

In accordance with amended independent claim 12, the parity calculator is configured to “receive the data blocks of the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame by performing an exclusive-or operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks, the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete, the command processing unit receiving the parity write command configured to write the parity block into the nonvolatile memory device”. As such, the parity calculator updates the data block stored in the page frame with each data block in the sequence of data blocks by performing an exclusive-or operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks.

The elements of claim 4 have been incorporated into independent claim 12. Claim 4 recites, “The nonvolatile memory controller of claim 3, wherein the logical operation includes an exclusive-or operation.” The Office argues that claim 4 is not patentable over Fukuda in view of Yu et al., because Fukuda teaches “the logical operation includes an exclusive-or operation”, with reference to Figure 2, reference number 21. Applicant respectfully disagrees with the finding of the Office.

Applicant contends that reference number 21 of Figure 2 of Fukuda is merely a “parity creation unit”, and Fukuda does not teach or suggest performing an exclusive-or operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks as is described and claimed by the present invention.

Applicant contends, that neither Fukuda nor Yu, alone or in combination, teach the claim element of amended claim 12 which recites, “a parity calculator coupled to the plurality of command processing units, the parity calculator further comprising a context memory including a page frame, the parity calculator is configured to receive the data blocks of the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame by performing an exclusive-or operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks, the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete, the command processing unit receiving the parity write command configured to write the parity block into the nonvolatile memory device”, as is recited in amended independent claim 12.

For the reasons presented above, Applicant contends that amended claim 12 is patentable over Fukuda in view of Yu et al., and is believed to be in condition for allowance.

Claims 13-14 are dependent upon claim 12, which has been shown to be allowable, and are therefore allowable as a matter of law.

Independent claim 15 has been amended to more clearly describe that which the Applicant regards as the invention. Amended claim 15 recites:

A method of generating parity data, the method comprising:

distributing a plurality of commands for performing the data stripe operation among a plurality of command processing units in the nonvolatile memory controller, the plurality of commands including a plurality of data update commands and a parity write command;

generating a plurality of data requests by the plurality of command processing units based on the plurality of data update commands;

receiving a plurality of data blocks at the plurality of command processing units and at a parity calculator of the nonvolatile memory controller in response to the plurality of data requests;

writing the plurality of data blocks to a plurality of nonvolatile memory devices by the plurality of command processing units;

generating a parity block in a page frame of a context memory by the parity calculator based on the plurality of data blocks by initializing a parity block in the page frame by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing

each data block in a data buffer;

determining that generation of the parity block is complete; and

writing the parity block to a nonvolatile memory device by a command processing

unit of the plurality of command processing units based on the parity write

command after determining generation of the parity block is complete.

The elements of claim 16 have been incorporated into independent claim 15. Claim 16 has been cancelled.

In accordance with amended independent claim 16, the method includes “generating a parity block in a page frame of a context memory by the parity calculator based on the plurality of data blocks by initializing a parity block in the page frame by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer”. As such, generating the parity block is performed without storing each data block in a data buffer.

Applicant contends, that neither Fukuda nor Yu, alone or in combination, teach the claim element of amended claim 1 which recites, “generating a parity block in a page frame of a context memory by the parity calculator based on the plurality of data blocks by initializing a parity block in the page frame by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer”.

For the reasons presented above, Applicant contends that amended claim 15 is patentable over Fukuda in view of Yu et al., and is believed to be in condition for allowance.

Claims 17-20 are dependent upon claim 15, which has been shown to be allowable, and are therefore allowable as a matter of law.

If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned at (408) 354-4448 is requested.

Respectfully Submitted,

August 26, 2013
Date

/Kenneth Glass/
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Electronic Patent Application Fee Transmittal				
Application Number:		13052835		
Filing Date:		21-Mar-2011		
Title of Invention:		SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
First Named Inventor/Applicant Name:		Peter Z. Onufryk		
Filer:		Kenneth Glass		
Attorney Docket Number:		PMCS-2730C-UT		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 1 month with \$0 paid	1251	1	200	200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				200

Electronic Acknowledgement Receipt	
EFS ID:	16689926
Application Number:	13052835
International Application Number:	
Confirmation Number:	7182
Title of Invention:	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	PMCS-2730C-UT
Receipt Date:	26-AUG-2013
Filing Date:	21-MAR-2011
Time Stamp:	18:21:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$200
RAM confirmation Number	6325
Deposit Account	501006
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDT-2730C-Amendment-Av1.pdf	136906 b5d58235de881d69d339bca66cfd98acbf8158	yes	17
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1		
	Claims	2	8		
	Applicant Arguments/Remarks Made in an Amendment	9	17		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30621 6e6b143596a14d2ddf4a79a9d85adce3e26e15ff	no	2
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/052,835	Filing Date 03/21/2011	☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO							
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)					
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A		
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A			N/A		
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A		
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL		
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT	08/26/2013	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	* 17	Minus	** 20	= 0	X \$80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE						0	
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
TOTAL ADD'L FEE							
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

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EXAMINER

CHAUDRY, MUJTABA M

ART UNIT

PAPER NUMBER

2112

DATE MAILED: 09/13/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,835	03/21/2011	Peter Z. Onufryk	PMCS-2730C-UT	7182

TITLE OF INVENTION: SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	12/13/2013

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THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,835	03/21/2011	Peter Z. Onufryk	PMCS-2730C-UT	7182

TITLE OF INVENTION: SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	12/13/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHAUDRY, MUJTABA M	2112	714-805000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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13/052,835	03/21/2011	Peter Z. Onufryk	PMCS-2730C-UT	7182

33087	7590	09/13/2013
GLASS & ASSOCIATES P.O. BOX 1220 LOS GATOS, CA 95031-1220		

EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/13/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 309 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 309 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/052,835 Examiner MUJTABA K. CHAUDRY	Applicant(s) ONUFYK ET AL. Art Unit 2112 AIA (First Inventor to File) Status No
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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed 8/26/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1,3-15 and 17-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
 a) ☐ All b) ☐ Some *c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>5/6/2013</u>	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/MUJTABA K CHAUDRY/ Primary Examiner, Art Unit 2112	
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Issue Classification 	Application/Control No. 13052835	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.	
	Examiner M. MUJTABA K CHAUDRY	Art Unit 2112	

CPC			Type	Version
Symbol				

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	18	
/M. MUJTABA K CHAUDRY/ Primary Examiner.Art Unit 2112	08/30/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification 	Application/Control No. 13052835	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner M. MUJTABA K CHAUDRY	Art Unit 2112

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
714		764				G	1	1	C	29 / 00 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
711	103																		

NONE		Total Claims Allowed:	
		18	
(Assistant Examiner)	(Date)		
/M. MUJTABA K CHAUDRY/ Primary Examiner.Art Unit 2112	08/30/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

Issue Classification 	Application/Control No. 13052835	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner M. MUJTABA K CHAUDRY	Art Unit 2112

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17												
-	2	16	18												
2	3	17	19												
3	4	18	20												
4	5														
5	6														
6	7														
7	8														
8	9														
9	10														
10	11														
11	12														
12	13														
13	14														
14	15														
-	16														

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 18	
/M. MUJTABA K CHAUDRY/ Primary Examiner.Art Unit 2112 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 4

Search Notes 	Application/Control No. 13052835	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner M. MUJTABA K CHAUDRY	Art Unit 2112

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	103	4/23/2013	MC
714	764	4/23/2013	MC

SEARCH NOTES		
Search Notes	Date	Examiner
EAST DATABASE	4/23/2013	MC
USPAT	4/23/2013	MC
USPGPUBS	4/23/2013	MC
EPO	4/23/2013	MC
JPO	4/23/2013	MC
DERWANT	4/23/2013	MC
IBM-TDB	4/23/2013	MC
GOOGLE NPL/IEEE	4/23/2013	MC
updated search	8/30/2013	MC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
Interference searched		8/30/2013	MC

	/M. MUJTABA K CHAUDRY/ Primary Examiner.Art Unit 2112
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	99031	(flash non-volatile nonvolatile) and ((plurality several multiple two) near (controller CPU (command near processing) processor microprocessor micro-processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 12:25
L4	0	(flash non-volatile nonvolatile) and ((plurality several multiple two) near (controller CPU (command near processing) processor microprocessor micro-processor)) and ((parity near (calculat\$3 determin\$3 generat\$3 comput\$7)) with (context memory page frame) with sequence with updat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 12:26
L5	0	(flash non-volatile nonvolatile) and ((plurality several multiple two) near (controller CPU (command near processing) processor microprocessor micro-processor)) and ((parity near (calculat\$3 determin\$3 generat\$3 comput\$7)) with ((context adj memory) page frame) with sequence with updat\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/30 12:26
L7	4	"20110161678" "20080320214" "20090077302" "20100185808"	US-PGPUB	OR	OFF	2013/08/30 12:30
S1	6183	(memory) with (read\$3 and compar\$3 and writ\$3 and error\$2)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 06:54
S2	286	memory with read\$3 with compar\$3 with writ\$3 with error\$2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 06:54
S3	88	(memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 07:08
S4	16	(memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC) and interleav\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 06:56
S5	13	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).ab.	US-PGPUB; USPAT; EPO; JPO; DERWENT;	OR	ON	2004/08/12 10:24

			IBM_TDB			
S6	1	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).ti.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 07:09
S7	12	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 07:09
S8	13	((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).ab. not ((memory with read\$3 with compar\$3 with writ\$3 with error\$2) and ((error adj correction) ECC)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/12 11:08
S9	1	(read and write) near (memory) near (ECC "error detection" "error correction")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/01/27 17:00
S10	1	(read and write) near (memory) near (ECC "error detection" "error correction")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/01/27 17:01
S11	2	"5784393".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/04/04 13:35
S12	987	714/763.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/23 20:27
S13	58	714/763.ccls. and (read near request)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/01/23 20:27
S14	64	714/763.ccls. and (read near request) and process\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/01/23 20:27
S15	67	714/763.ccls. and (read near request) and process\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/17 19:17
S16	2	"5485473".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/07/18 11:38
S17	4	("5313464" "5343426").pn.	US-PGPUB; USPAT; EPO; JPO;	OR	ON	2006/12/05 14:40

			DERWENT; IBM_TDB			
S18	1581	714/758.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:22
S19	109	714/768.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:20
S20	80	714/767.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:19
S21	1075	714/763.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2006/12/05 15:20
S22	1	((writ\$3 read\$3) near memory) and interleav\$3 and "error correction algorithm").clm.	US-PGPUB	OR	OFF	2006/12/05 15:24
S23	31178	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:09
S24	650	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3)) and (page near buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:09
S25	15028	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3)) and (buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:09
S26	1062	((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (error near information))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:10
S27	388	((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (error adj information))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:10
S28	51	((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (reduc\$3 near (data bit))) and (buffer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:12
S29	261	((nonvolatile "non-volatile") with memory) and (error near (detect\$3 correct\$3)) and (error with correct\$3 with (stor\$3 restor\$3 rewrite) with (reduc\$3 compress\$3 less) with (bits	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:14

		data))				
S30	9	((nonvolatile "non-volatile") with memory) and (error with correct\$3 with (after then restor\$3) with ((reduc\$3 short\$5 less compress) near (data amount bits)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 18:15
S31	379	Noguchi.in. and Mitsuhiro.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 19:49
S32	1	((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (reduc\$3 near (data bit))) and (buffer) and (control near circuit) and (reduc\$3 with bits)).clm.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/23 19:51
S33	6	("5475693" "6353553" "6549459").pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/24 16:47
S34	3	("5475693" "6353553" "6549459").pn.	USPAT	OR	ON	2010/02/24 16:47
S35	615	714/763.ccls.	USPAT	OR	ON	2010/02/24 19:23
S36	623	714/710.ccls.	USPAT	OR	ON	2010/02/24 19:23
S38	0	mujtaba.xa. and chaudry.xa. and MPEFEC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/02/25 14:51
S39	0	mujtaba.xa. and chaudry.xa. and MPEFEC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:51
S40	0	mujtaba.xa. and chaudry.xa. and MPE-FEC	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:51
S41	0	mujtaba.xa. and chaudry.xa. and (multi adj protocol) and (error near (detect\$3 correct\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:52
S42	123	mujtaba.xa. and chaudry.xa. and (error near (detect\$3 correct\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:52
S43	186	mujtaba.xa. and chaudry.xa.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:52
S44	2	mujtaba.xa. and chaudry.xa. and tuner	US-PGPUB; USPAT;	OR	ON	2010/02/25 14:53

			EPO; JPO; DERWENT; IBM_TDB			
S45	17	mujtaba.xa. and chaudry.xa. and (tuner (radio near frequency))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:54
S46	1	mujtaba.xa. and chaudry.xa. and (tuner and(radio near frequency))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/02/25 14:54
S47	0	(nonvolatile near (stor\$3 memory) near controller) and (command near processing near units) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:12
S48	25	(nonvolatile near (stor\$3 memory) near controller) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:15
S49	131	((nonvolatile flash) near (stor\$3 memory) near controller) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:16
S50	162	((((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:16
S51	14	((((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (command near (plurality multiple several two various)) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:17
S52	14	((((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (commands near (plurality multiple several two various)) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:18
S53	0	((((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (commands near (plurality multiple several two	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2013/04/23 11:18

		various)) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command and (parity near (calculat\$3 determin\$5 generat\$3)) and (data near command) and (parity near command))	EPO; JPO; DERWENT; IBM_TDB			
S54	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 11:19
S55	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3)) and (command) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 15:23
S56	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3)) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/23 15:37
S57	14	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((commands near (plurality multiple several two various))((data near command) and (parity near command) and (updat\$3 near command))) and (parity near (calculat\$3 determin\$5 generat\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 07:49
S58	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (update adj (command instruction)) and (parity near command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 14:53
S59	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (update near (command instruction)) and (parity near command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 14:53
S60	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and (update near (command instruction)) and (parity near (instruction command))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/04/24 14:53

			DERWENT; IBM_TDB			
S61	48	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:04
S62	29	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller)) and ((data update) near (command instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:05
S63	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller)) and ((data update) near (command instruction)) and (parity near (command instruction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:05
S64	0	((nonvolatile flash) near (stor\$3 memory) near controller)((nonvolatile flash) near controller)) and ((plurality multiple several two) near (command instruction) near (process\$3 unit controller)) and ((data update) near (command instruction)) and (parity near (generat\$3 calculat\$3 determin\$5))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:08
S65	566651	((nonvolatile flash) near (stor\$3 memory))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:23
S66	6015	((nonvolatile flash) near (stor\$3 memory)) and (controller with ((plurality multiple several two) near (process\$3 units)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:23
S67	383	((nonvolatile flash) near (stor\$3 memory)) and (controller with ((plurality multiple several two) near (process\$3 units))) and parity	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:24
S68	4	((nonvolatile flash) near (stor\$3 memory)) and (controller with ((plurality multiple several two) near (process\$3 units))) and (parity near command) and ((data update) near command)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 15:25
S69	127	(data adj update adj command)	US-PGPUB;	OR	OFF	2013/04/24

			USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:50
S70	57	(data adj update adj command) and (flash non-volatile nonvolatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:54
S71	2	(data adj update adj command) and (flash non-volatile nonvolatile) and parity	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:54
S72	5	(data adj update adj command) same (flash non-volatile nonvolatile)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:56
S73	36	(data adj update adj command) and (((flash non-volatile nonvolatile) near memory)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:58
S74	8	(data adj update adj command) and (((flash non-volatile nonvolatile) near memory) same controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 16:59
S75	8	(data adj update adj commands) and (((flash non-volatile nonvolatile) near memory) same controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 17:02
S76	3	"20100185808"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/04/24 17:07
S77	7416	711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2013/04/24 18:20

			IBM_TDB			
S78	532	714/764.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 18:20
S79	4	("5875343" "8244946").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 18:22
S80	3	"20080256280"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2013/04/24 18:23
S81	4	("5875343" "8244946" "7708195" "7620784").pn.	USPAT	OR	OFF	2013/04/24 18:23
S82	1	"20080256280" "20100262979"	USPAT	OR	OFF	2013/04/24 18:24
S83	2	"20080256280" "20100262979"	US-PGPUB	OR	OFF	2013/04/24 18:24

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	0	((flash non-volatile nonvolatile) and ((plurality several multiple two) near (controller CPU (command near processing) processor microprocessor micro-processor)) and ((parity near (calculat\$3 determin\$3 generat\$3 comput\$7)) with ((context adj memory) page frame) with sequence with updat\$3)	USPAT; UPAD	OR	ON	2013/08/30 12:29
S37	8	((((nonvolatile "non-volatile") with memory) and ((error near (detect\$3 correct\$3)) with (reduc\$3 near (data bit))) and (buffer) and (control near circuit) and (reduc\$3 with bits))	USPAT; UPAD	OR	ON	2010/02/24 19:47

8/ 30/ 2013 12:34:28 PM**C:\Users\mchaudry\Documents\EAST\Workspaces\13052835.wsp**

Receipt date: 05/06/2013

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13052835 - GAU: 2112

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835	
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730C-UT	

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	2	20080320214		2008-12-25	Ma et al.			
	3	20090077302		2009-03-19	Fukuda, Hideaki			
	4	20100185808		2010-07-22	Yu et al.			
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Receipt date: 05/06/2013 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052835	13052835 - GAU: 2112
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730C-UT	

	1							☐
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	NVM Express, Revision 1.0; Intel Corporation; March 1, 2011.	☐

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Examiner Signature	/Mujtaba Chaudry/	Date Considered	08/30/2013
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33087 7590 09/13/2013
GLASS & ASSOCIATES
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LOS GATOS, CA 95031-1220

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,835	03/21/2011	Peter Z. Onufryk	PMCS-2730C-UT	7182

TITLE OF INVENTION: SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	12/13/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHAUDRY, MUJTABA M	2112	714-805000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

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1 Kenneth Glass
2 Stanley J. Pawlik
3 Glass & Associates

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PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

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Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

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NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

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Authorized Signature /Kenneth Glass/

Date 10/29/13

Typed or printed name Kenneth Glass

Registration No. 42,587

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For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

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OR



The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	13/052,835

Completed by (check one):



Applicant/Inventor

/Kenneth Glass/

Signature



Attorney or Agent of record 42,587
(Reg. No.)

Kenneth Glass

Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

408-354-4448

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Assignee recorded at Reel _____ Frame _____

October 29, 2013

Date

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* Total of 1 forms are submitted.

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Electronic Patent Application Fee Transmittal				
Application Number:		13052835		
Filing Date:		21-Mar-2011		
Title of Invention:		SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE		
First Named Inventor/Applicant Name:		Peter Z. Onufryk		
Filer:		Kenneth Glass		
Attorney Docket Number:		PMCS-2730C-UT		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				1780

Electronic Acknowledgement Receipt	
EFS ID:	17260654
Application Number:	13052835
International Application Number:	
Confirmation Number:	7182
Title of Invention:	SYSTEM AND METHOD FOR GENERATING PARITY DATA IN A NONVOLATILE MEMORY CONTROLLER BY USING A DISTRIBUTED PROCESSING TECHNIQUE
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	PMCS-2730C-UT
Receipt Date:	29-OCT-2013
Filing Date:	21-MAR-2011
Time Stamp:	18:43:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

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Payment Type	Deposit Account
Payment was successfully received in RAM	\$1780
RAM confirmation Number	6173
Deposit Account	501006
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	PMCS-2730CPTOL85.pdf	114196	no	2
			aaffc9f45f8391ff12eed8c197281c1301286c28		
Warnings:					
Information:					
2	Change of Address	sb0047.pdf	210352	no	2
			e8c4dabdc06696d0298960fb1b376a56dc8d461		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30271	no	2
			2fd80fd38318565b87380291edfe8068cd34f38		
Warnings:					
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Total Files Size (in bytes):			354819		
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,835	12/03/2013	8601346	PMCS-2730C-UT	7182

33087 7590 11/13/2013
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 309 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Peter Z. Onufryk, Flanders, NJ;
Inna Levit, Sunnyvale, CA;

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