

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND WESTERN DIGITAL
TECHNOLOGIES, INC.,
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00516
U.S. Patent No. 8,601,346

**PATENT OWNER PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107(a)**

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I. INTRODUCTION

The Board should deny institution of *inter partes* review of the challenged claims of U.S. Patent No. 8,601,346 (“the ’346 patent”) because Petitioners fail to demonstrate a reasonable likelihood that the asserted combination of Jeddeloh, Klieman, and Ma discloses or renders obvious three elements of independent claims 1, 11, and 14. Petitioners’ invalidity challenges are conclusory, fail to explain how relevant claim terms should be construed, and are contrary to express teachings in the references. Compounding these deficiencies, Dr. Min’s opinions supporting the Petition repeat the conclusory arguments in the Petition (or vice versa), and thus add no probative value over Petitioners’ attorney argument. Dr. Min also appears to lack professional experience in the field of memory systems, further demonstrating that his opinions, particularly those on disputed claim elements, are entitled to little or no weight. At bottom, the merits of Petitioners’ invalidity challenges are weak and the Petition should be denied.

II. THE ’346 PATENT

A. Summary of the ’346 patent

In general, the ’346 patent describes a system for data recovery that manages data in nonvolatile memory using a plurality of data blocks organized into stripes and stored across multiple memory devices. EX1001, 2:40-42. The system employs multiple command processing units, each configured to receive commands, including data update commands and a parity write command, for

executing a data stripe operation. EX1001, 1:52-53. Each command processing unit processes incoming commands by generating data requests based on the data update commands, receiving the corresponding data blocks, and writing them to nonvolatile memory devices. EX1001, 2:46-50. After all data update commands have been processed, the system issues a parity write command to generate and store a parity block. EX1001, 8:66-9:3. This parity block is created by first storing the initial data block, and then successively updating that stored block with each subsequent data block in sequence as they are received. EX1001, 4:2-7. The command processing unit receiving the parity write command writes the parity block to the appropriate nonvolatile memory location to complete the data stripe operation. EX1001, 2:33-35.

B. Level of Skill in the Art

For the purposes of this preliminary response, Patent Owner applies Petitioners' proffered level of skill in the art with a caveat regarding the last sentence:

A Person of Ordinary Skill in The Art ("POSITA") in August of 2010 would have had a working knowledge of the memory system art that is pertinent to the '346 patent, including memory systems and memory controllers. A POSITA would have had a bachelor's degree in electrical engineering[,] computer science, or an equivalent, and approximately two years of professional experience working in the

field of memory systems. Lack of professional experience can be remedied by additional education, and vice versa.

Pet., 11-12. To the extent the last sentence means that additional education could completely supplant experience, Patent Owner disagrees. A POSITA would be a professional with active work experience in the field of memory technologies, including at least some hands-on experience in that domain.

Petitioners' expert, Dr. Min, does not appear to have any "professional experience working in the field of memory systems." *See* EX1003, ¶¶7-22; EX1004 (Dr. Min's CV). While Dr. Min appears to have expertise in networking and wireless communications, his experience with memory is limited to incorporating high speed memory modules into network chips that he has designed, based on his description in Section II, Qualifications and Professional Experience. *See* EX1003, ¶19. His lack of experience in the field of memory is reflected in the opinions in his declaration, which follow the basic formula of providing a block quote from a reference followed by a conclusory statement that a claim element is taught or obvious. *See, e.g.,* EX1003, ¶¶87-92. As discussed below, such conclusory opinions are insufficient to demonstrate obviousness and are entitled to little weight.

C. Claim Construction

Claim terms need only be construed to the extent necessary to resolve the

controversy. *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011). Because none of the issues in this preliminary response turn on the construction of a claim term, Patent Owner takes no position at this time.

III. PETITIONERS FAIL TO DEMONSTRATE A REASONABLE LIKELIHOOD THE CHALLENGED CLAIMS WERE OBVIOUS.

Petitioners present the following two Grounds of Unpatentability:

Grounds	Claims	Basis
#1	1-3, 5-11, 13-16, and 18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Jeddeloh, Kleiman, and Ma
#2	4 and 17	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Jeddeloh, Kleiman, Ma, and Yashiro

Pet., 15. Ground 1, based on Jeddeloh, Klieman, and Ma, is the only Ground that addresses independent claims 1, 11, and 14.

The Board should deny institution because Petitioners fail to demonstrate a reasonable likelihood that the Jeddeloh-Klieman-Ma combination discloses or renders obvious at least three key claim elements of independent claims 1, 11, and 14. Specifically, Petitioners fail to demonstrate that: (A) Jeddeloh discloses or renders obvious the performance of a data stripe operation on “*a plurality of data blocks*”;¹ (B) Jeddeloh discloses or renders obvious “*a plurality of data update commands and a parity write command*”; and (C) the Jeddeloh-Ma combination

¹ Emphasis added unless otherwise noted.

renders obvious command processing units that are “configured to request a data block ... based on the data update command.” Each of these defects are fatal to Petitioners’ case, and thus the Board is on firm ground denying institution based on any of these defects.

Patent Owner also notes that claim 13 depends on claim 12, but Petitioners did not challenge claim 12. Because a dependent claim cannot be shown to be unpatentable if the claim from which it depends has not been shown to be unpatentable, Petitioners have not shown that claim 13 is obvious.

A. Jeddelloh does not disclose or render obvious performing a data stripe operation on “*a plurality of data blocks*.”

Petitioners fail to demonstrate that Jeddelloh discloses or renders obvious performing a data stripe operation on “*a plurality of data blocks*.” See Pet., 29-31. The preamble of claim 1 recites “performing a data stripe operation on a plurality of data blocks,” EX1001, 22:7-9, and other elements in the body of claim 1 refer back to “the data stripe operation,” EX1001, 22:13, and to “the plurality of data blocks,” EX1001, 22:19. Claim 11 recites “performing a data stripe operation on a plurality of data blocks.” EX1001, 23:35-36. And claim 14 similarly recites “performing the data stripe operation” that requires “writing the plurality of data blocks to a plurality of non-volatile memory devices” and “generating a parity block ... based on the plurality of data blocks.” EX1001, 24:14-15, 24:26-27,

24:29-31.²

Petitioners allege that Jeddeloh teaches “performing a data stripe operation on a plurality of data blocks.” Pet., 29-31. Specifically, Petitioners present three conflicting theories alleging that Jeddeloh’s teachings related to performing a stripe operation on memory *pages* satisfies “performing a data stripe operation on a plurality of data blocks.” *Id.* Each of Petitioners’ theories fails.

First, Petitioners suggest that there were “various ways a POSITA would have understood the term ‘block,’” and then conclude that “a memory page is a structured form of data and is thus a ‘block’ as claimed.” Pet., 30. This argument fails procedurally and on the merits. Under Rule 42.104(b)(3), a petition must set forth “[h]ow the challenged claim is to be construed.” Here, Petitioners take the opposite tack, suggesting that there are “various ways” to construe the term without explaining which way is correct based on the evidence. To be sure, neither Petitioners nor Dr. Min provide any claim construction analysis of “block.” *See* Pet., 30; EX1003, ¶88 (Dr. Min repeating the Petition’s conclusory arguments (or vice versa)); *see also Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-17 (P.T.A.B. Aug. 24, 2022) (precedential) (holding declaration is entitled to

² The Petition generally refers back to Petitioners’ analysis of claim 1 to address these elements of claims 11 and 14. *See* Pet., 64, 68-69.

little weight when it contains an exact restatement of the petition’s unsupported, conclusory assertions without any additional supporting evidence or reasoning).

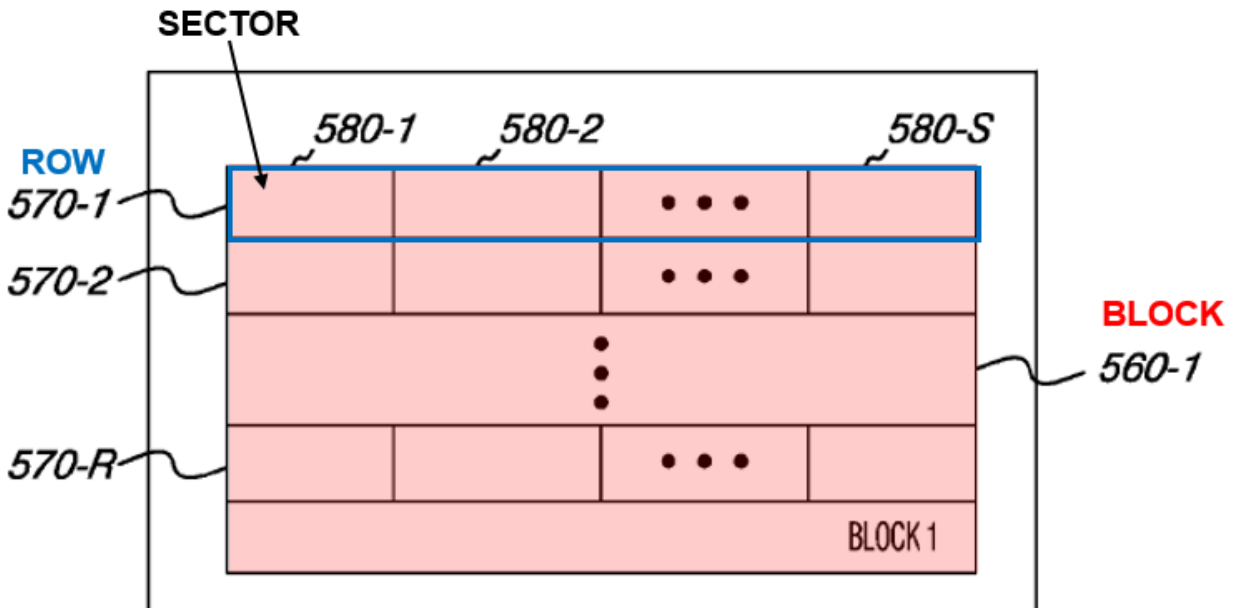
This procedural defect is fatal to the Petition and supports denial.

Even so, as best understood, Petitioners’ position is that “a structured form of data” is one of the “various” ways a POSITA would have construed the term “block,” and that a single memory page in Jeddeloh satisfies this construction. *See* Pet., 30. This position—which equates a page (or any other unit of memory, for that matter) with a “block”—fails because (i) Petitioners have not shown that such a broad construction of “block” is supported by the record and (ii) it contradicts Jeddeloh’s express teachings about units of memory. *See HP Inc. v. Universal Connectivity Techs., Inc.*, IPR2024-01429, Paper 11 at 15-16 (P.T.A.B. Apr. 16, 2025) (finding petitioner’s showing “not ‘particularly strong’” when it was unclear based on the “preliminary record whether the specification supports Petitioner’s broad claim construction”).

Jeddeloh discloses a memory hierarchy in which a plurality of memory pages (each of which is made up of smaller units such as cells or sectors) form a data block. In the Background, for example, Jeddeloh discloses that “memory arrays can include a number of memory cells organized into a number of physical pages, and the physical pages can be organized into a number of blocks.” EX1005, ¶5. Similarly, Jeddeloh explains that “some memory arrays can include a number

of pages of memory cells that make up a block of memory cells.” EX1005, ¶19.

But Jeddelloh’s description of Figure 5, upon which Petitioner’s rely, is particularly instructive. *See* Pet., 30. Jeddelloh explains that the “memory device 510” of Figure 5, which is shown in-part below, “can include a number of physical blocks 560-1 (BLOCK 1), 560-2 (BLOCK 2), ..., 560-M (BLOCK M) of memory cells.” EX1005, ¶59. As shown, “a physical block, e.g., 560-1, 560-2, ..., 560-M, can include a number of rows,” such as “570-1, 570-2, ..., 570-R.” EX1005, ¶61. Jeddelloh discloses that “each row 570-1, 570-2, ..., 570-R, in FIG. 5 includes only one physical and logical page” EX1005, ¶61. “[A] page,” in turn, “can store data in a number of sectors 580-1, 580-2, ..., 580-S.” EX1005, ¶62.



EX1005, FIG. 5 (reproduced in-part and annotated).

Accordingly, as shown above, Jeddelloh discloses that a plurality of sectors

(at least three in Figure 5) form a page, and a plurality of pages (at least three physical and three logical pages in Figure 5) form a block. And Petitioners' first theory—that a memory page in Jeddeloh is a claimed “block,” and thus performing a stripe operation on a plurality of memory pages teaches performing a stripe operation on a plurality of blocks—fails because it is inconsistent with Jeddeloh's express teachings. Dr. Min's opinions merely repeat the conclusory arguments in the Petition (or vice versa), and thus are entitled to little or no weight. *Xerox*, IPR2022-00624, Paper 9 at 15-17.

Second, Petitioners argue that “Jeddeloh's memory pages include logical blocks,” which Petitioners allege are “the smallest unit of addressable memory,” citing paragraph 62 of Jeddeloh as alleged support. Pet., 30. So while Petitioners' first theory equated a memory page in Jeddeloh to a claimed “block,” Petitioners' second theory asserts that a page in Jeddeloh is comprised of blocks. But Petitioners' second theory mischaracterizes Jeddeloh. In paragraph 62, Jeddeloh discloses that “a page can store data in a number of sectors,” and that “a sector is the smallest addressable portion of a storage volume.” EX1005, ¶62. Thus, a page in Jeddeloh is comprised of smaller units called sectors, not data blocks, as shown and discussed above with respect to Figure 5 of Jeddeloh.

Petitioners also emphasize Jeddeloh's disclosure of “logical block *addressing*” in paragraph 62 as allegedly supporting its second theory. Pet., 30. But

Jeddeloh discloses that “logical block *addressing* is a scheme that can be used by a host for identifying a *sector* of information” EX1005, ¶62. Petitioners fail to explain how a scheme for addressing sectors in any way suggests that a memory page in Jeddeloh is comprised of blocks, or that performing a stripe operation on a memory page (comprised of a plurality of sectors) teaches performing a stripe operation on the claimed “plurality of data blocks.”

Accordingly, Petitioners’ second theory fails because, like its first theory, it is inconsistent with Jeddeloh’s teachings. And, again, Dr. Min’s opinions repeat the arguments of the Petition (or vice versa), EX1003, ¶¶88-89, and thus are entitled to little weight, *Xerox*, IPR2022-00624, Paper 9 at 15-17.

Third, rounding out the possibilities, Petitioners concede that Jeddeloh teaches that “memory pages can be organized into a larger structure referred to as a block.”³ Pet., 30. This concession confirms that Petitioners’ first and second theories are wrong and should be rejected. And while Petitioners’ description of pages and blocks here is consistent with Jeddeloh’s teachings regarding memory

³ Petitioners’ first theory posited that a page is equal to a block; their second theory that a plurality of blocks form a page; and their third theory that a plurality of pages form a block. Pet., 30-31. Petitioners’ inconsistent theories demonstrate that the merits are weak and institution should be denied.

hierarchy (sectors form a page, pages form a block), that does not end the matter.

Petitioners still fail to show that Jeddeloh performs a stripe operation on a “*plurality* of data blocks.” That is, because a plurality of pages form a block (not the other way around), performing a stripe operation on a plurality of memory pages is not the same as performing a stripe operation on a *plurality* of data blocks, and neither Petitioners nor Dr. Min have demonstrated otherwise. *Compare* Pet., 30-31 *with* EX1003, ¶90 (repeating the arguments in the Petition). On the contrary, they provide only conclusory statements that are insufficient to demonstrate obviousness. *In re Magnum Oil Tools International, Ltd.*, 829 F.3d 1364, 1380 (Fed. Cir. 2016) (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements.”).

Accordingly, Petitioners’ three theories present conflicting interpretations of the term “block” in violation of Rule 42.104(b)(3), and fail to demonstrate that Jeddeloh teaches performing a stripe operation on a *plurality* of data blocks.

B. Jeddeloh does not disclose or render obvious “a plurality of data update commands *and a parity write command*.”

Petitioners fail to demonstrate that Jeddeloh discloses or renders obvious “a plurality of data update commands *and a parity write command*.” *See* Pet., 34-36. Claims 1, 11, and 14 recite “a plurality of commands for performing the[/a] data stripe operation,” wherein “the plurality of commands including[/comprising] a plurality of data update commands *and a parity write command*.” EX1001, 22:12-

15, 23:34-38, 24:13-17. Each independent claim thus explicitly recites two different types of commands: “data update commands” and “a parity write command.”

“[U]se of both terms in close proximity in the same claim gives rise to an inference that a different meaning should be assigned to each.” *Bancorp Services, LLC v. Hartford Life Ins. Co.*, 359 F.3d 1367, 1373 (Fed. Cir. 2004). Petitioners, who carry the burden to explain how the challenged claims should be construed, 37 C.F.R. § 42.104(b)(3), do not attempt to construe these terms or present any argument to rebut the inference that “data update command” and “parity write command” carry different meanings, *see* Pet., 12-15 (addressing claim construction), 34-36 (addressing the commands). Accordingly, Petitioners must show that the art discloses or renders obvious the two distinct commands. Petitioners fail to do so with respect to the claimed “parity write command.”

Petitioners first allege that Jeddeloh teaches the claimed “parity write command.” Pet., 35-36. Claim element [1.1] requires “a plurality of command processing units,” each of which is “configured to receive a command of a plurality of commands for performing the data stripe operation.” Petitioners map Jeddeloh’s channel memory circuits 338 of Figure 3 to the claimed “command processing units.” Pet., 33. Turning to claim element [1.2], Petitioners map certain write commands in Jeddeloh that are used to write updated data to the claimed

“data update commands.” Pet., 34-35.

Regarding the claimed “parity write command,” Petitioners argue that “Jeddeloh explains that one memory channel and its associated memory device may be dedicated to parity data.” Pet., 35-36. Without further explanation or support in the record, Petitioners then conclude that “a *write command* processed by the channel memory controller 338 for the dedicated parity device is a ‘*parity write command*’ as claimed.” Pet., 36; *see* EX1003, ¶102 (same conclusory statement). Petitioners thus map Jeddeloh’s write commands to *both* of the claimed “data update commands” and the “parity write command” without any explanation or evidence as to how a single type of command in Jeddeloh satisfies two distinct commands, which is critical in light of the inference that these claim terms carry different meanings. *Bancorp*, 359 F.3d at 1373. Jeddeloh makes no such distinction between write commands sent to different memory channels, including to any memory channel that is dedicated to parity. In any event, it is Petitioners’ burden to explain how the challenged claims are to be construed and how the construed claims are unpatentable. 37 C.F.R. §§ 42.104(b)(3)-(4). Petitioners’ and Dr. Min’s conclusory statements are insufficient to carry that burden, and thus should be rejected.

Tacitly acknowledging that Jeddeloh’s write commands are insufficient, Petitioners next argue that “a POSITA would have found it obvious to use parity

write commands when writing parity data.” Pet., 36. Here, Petitioners do not rely on teachings in any of the references in the asserted combination; rather, Petitioners rely on the alleged knowledge of a POSITA as evidenced by some background statements in a patent to Hodges. Pet., 36 (citing Exhibit 1014). But even if Hodges demonstrates that a POSITA would have been aware of parity write commands, which Patent Owner does not concede, that alone does not establish obviousness.

Although art outside the asserted combination (such as Hodges) “can legitimately serve to document the knowledge that skilled artisans would bring to bear in reading the prior art identified as producing obviousness,” *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1365 (Fed. Cir. 2015), that does not relieve Petitioners of their burden to show that a POSITA would have modified Jeddeloh to implement this allegedly known command. “An obviousness determination requires finding that a person of ordinary skill in the art would have been motivated to combine or modify the teachings in the prior art and would have had a reasonable expectation of success in doing so.” *Regents of University of California v. Board Institute, Inc.*, 903 F.3d 1286, 1291 (Fed. Cir. 2018); *see also In re Stepan Co.*, 868 F.3d 1342, 1346 n.1 (Fed. Cir. 2017) (“Whether a rejection is based on combining disclosures from multiple references, combining multiple embodiments from a single reference, or selecting from large lists of elements in a

single reference, there must be a motivation to make the combination and a reasonable expectation that such a combination would be successful, otherwise a skilled artisan would not arrive at the claimed combination.”).

Here, Petitioners allege that parity write commands were known (based on Hodges), but fails to perform any analysis to demonstrate the requisite motivation to combine or reasonable expectation of success for modifying Jeddelloh to include such commands. Pet., 31. Dr. Min again repeats the conclusory argument in the Petition (or vice versa) without further elaboration. EX1003, ¶103. Accordingly, Petitioners fail to demonstrate that Jeddelloh discloses or renders obvious “a plurality of data update commands *and a parity write command*.”

C. The Jeddelloh-Ma combination does not render obvious command processing units that are “configured to request a data block ... based on the data update command.”

Petitioners fail to demonstrate that the Jeddelloh-Ma combination renders obvious command processing units that are “configured to request a data block ... based on the data update command.” *See* Pet., 36-38 (addressing claim element [1.3a]), 65-66 (addressing claim element [11.4] by reference to claim 1), 68 (addressing claim element [14.2] by reference to claim 1). Claims 1 and 11 recite that the command processing units are “configured to request a data block of the plurality of data blocks based on the data update command.” EX1001, 22:15-20, 23:43-47. Claim 14 similarly recites “generating a plurality of data requests by the

plurality of command processing units based on the plurality of data update commands.” EX1001, 24:19-21.

Again, Petitioners map Jeddeloh’s channel memory circuits 338 of Figure 3 to the claimed “command processing units.” Pet., 33. Jeddeloh does not disclose that its channel memory circuits request data blocks based on a data update command, nor do Petitioners allege that Jeddeloh discloses this element.⁴ See Pet., 36-37. Instead, Petitioners allege that Ma discloses such requests, and that it would have been obvious to modify Jeddeloh to implement Ma’s alleged requests. Pet., 37-38. Specifically, Petitioners allege that the “DMA activate”⁵ message disclosed in column 11, lines 40-44 of Ma is a request for a data block based on a data update command. It is not and thus Petitioners’ argument fails.

Ma discloses that the “DMA activate” message is sent from a flash-memory device to a host “to indicate that it is ready for the DMA transfer to begin.”

⁴ Notably, Petitioners allege that it would have been obvious for Jeddeloh to “request and receive *pages* for writing to memory” in light of Ma. Pet., 36-37. As discussed in Section III.A, Petitioner fails to demonstrate that a *page* of memory is the same as a data block, and thus Petitioners’ position with respect to element [1.3a] is facially deficient and should be rejected.

⁵ DMA stands for direct memory access. EX1007, 10:60.

EX1007, 11:40-44. Ma’s “DMA activate” is not a request for a data block, let alone a request for a data block that is based on a data update command. Neither Petitioners nor Dr. Min attempt to explain how Ma’s “DMA activate” message satisfies the claim element. *See* Pet., 37; EX1003, ¶¶107-108. Rather, as with their other analysis, their arguments rest on conclusory statements that are insufficient to demonstrate obviousness. *Magnum Oil Tools*, 829 F.3d 1364 at 1380. Accordingly, Petitioners fail to demonstrate that the Jeddeloh-Ma combination renders obvious command processing units that are “configured to request a data block ... based on the data update command.”

IV. THE BOARD SHOULD NOT CREDIT DR. MIN’S OPINIONS.

The Board should not credit Dr. Min’s opinions because they are conclusory and merely repeat Petitioners’ arguments. “[C]onclusory expert testimony is inadequate to support an obviousness determination” *TQ Delta, LLC v. Cisco Systems, Inc.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019); *see also Magnum Oil Tools*, 829 F.3d at 1380 (“To satisfy its burden of proving obviousness, a petitioner cannot employ mere conclusory statements.”). Accordingly, the Board does not credit declaration testimony that “merely repeats, verbatim, the conclusory assertion for which it is offered to support.” *Xerox*, IPR2022-00624, Paper 9 at 15-16 (emphasis omitted); *see also id.* at 15 (“[T]he cited declaration testimony is conclusory and unsupported, adds little to the conclusory assertion for which it is

offered to support, and is entitled to little weight.”); 37 C.F.R. § 42.65(a).

Key opinions in Dr. Min’s declaration are conclusory and merely repeat the Petition’s equally conclusory arguments, with the primary difference between the declaration and Petition being that Dr. Min block quotes the references while the Petition provides in-line quotes. For example, Dr. Min’s opinions regarding the claimed “plurality of data blocks” tracks the Petition’s arguments while merely substituting lengthy block quotes from the same paragraphs of Jeddeloh that Petitioners rely on. *Compare* Pet., 29-31 *with* EX1003, ¶¶87-92. The same is true of Dr. Min’s opinions for the claimed “parity write command,” *compare* Pet., 34-36 *with* EX1003, ¶¶98-104, and for the claimed command processing units that are “configured to request a data block ... based on the data update command,” *compare* Pet., 36-38 *with* EX1003, ¶¶105-109.

At bottom, Dr. Min’s declaration is the quintessential cut-and-paste copy of conclusory attorney argument that *TQ Delta*, *Magnum Oil Tools*, and *Xerox* instructs should be given little or no weight.

V. CONCLUSION

The Petition fails to show a reasonable likelihood of success in proving that any of the challenged claims is unpatentable as anticipated/obvious in view of the cited art. Therefore, the Board should deny institution.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

1. This Patent Owner Preliminary Response complies with the type-volume limitation of 14,000 words, comprising 3,982 words, excluding the parts exempted by 37 C.F.R. § 42.24(a)(1).

2. This Patent Owner Preliminary Response complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman font.

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CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER PRELIMINARY
RESPONSE UNDER 37 C.F.R. § 42.107(a)** was served in its entirety on May 27,
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