

Declaration and Power of Attorney

IDT-2730D-UT

My residence/post office address and citizenship are as stated below next to my name;
I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER

the specification of which is attached hereto.

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION	FILING DATE
61/374242	8/16/10

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) listed below to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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Randall Krause, Reg. No. 53,158
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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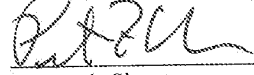
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INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims benefit of United States provisional patent application serial number 61/374,242 filed August 16, 2010 and entitled “Non Volatile Memory Host Controller Interface Device,” which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] Nonvolatile Memory Express (NVMe) is a standard defining a register interface, command set, and feature set for high-performance Peripheral Component Interconnect Express (PCIe) based solid-state drives (SSDs). An NVMe interface includes a register interface defined by the NVMe standard and allows a host computer to communicate with a non-volatile memory subsystem such as a Flash storage device. Typically, the NVMe interface is implemented as a stand-alone Peripheral Component Interconnect (PCI) device.

[0003] In a typical computing system including an NVMe interface, a host computer provides nonvolatile memory commands to a non-volatile memory subsystem including the NVMe interface. In turn, the NVMe interface processes the nonvolatile memory commands to manage data in a non-volatile memory device of the non-volatile memory subsystem.

Although the NVMe standard specifies a register set and a standard command set for designing an NVMe interface, the NVMe standard leaves other implementation details open to a designer of the non-volatile memory subsystem.

SUMMARY

[0004] In various embodiments, a nonvolatile memory controller includes a processor and an interrupt manager. The processor processes a nonvolatile memory command. Additionally, the processor generates a completion status based on the nonvolatile memory command for storage of the completion status in a completion queue of a host processing unit. The interrupt manager determines the completion queue in the host processing unit includes an unprocessed completion status. Further, the interrupt manager generates an interrupt message packet for triggering an interrupt in the host processing unit. In this way, the nonvolatile memory controller alerts the host processing unit to the unprocessed completion status in the completion queue. Because the interrupt manager alerts the host processing unit of the unprocessed completion status in the completion queue, the host processing unit need not include resources for monitoring the completion queue for an unprocessed completion status.

[0005] A nonvolatile memory controller, in accordance with one embodiment, includes an interrupt manager. The interrupt manager is configured to determine a completion queue in a host processing unit contains an unprocessed completion status. The interrupt manager is further configured to generate a completion queue state for indicating the occurrence of a completion queue event associated with the completion queue, generate an interrupt vector state based on the completion queue state, determine the completion queue of the host processing unit contains an unprocessed completion status based on the interrupt vector state, and generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.

[0006] A nonvolatile memory controller, in accordance with one embodiment, includes a completion queue state memory, an interrupt vector state memory, and an interrupt manager controller. The interrupt manager controller is coupled to the completion queue state memory and the interrupt vector state memory. The completion queue state memory is configured to store completion queue states corresponding to completion queues in a host processing unit. The interrupt vector state memory is configured to store interrupt vector states corresponding to interrupt vectors in the host processing unit. The interrupt manager controller is configured to map at least one of the completion queue states to an interrupt vector state. The interrupt manager is further configured to generate the interrupt vector state based on each completion queue state mapped to the interrupt vector state. Additionally, the interrupt manager controller is configured to determine a completion queue corresponding to a completion queue state mapped to the interrupt vector state includes an unprocessed completion status based on the interrupt vector state. Further, the interrupt manager controller is configured to generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.

[0007] A method, in accordance with one embodiment, includes generating a completion queue state by a nonvolatile memory controller for indicating the occurrence of a completion queue event associated with a completion queue in a host processing unit. The method further includes generating an interrupt vector state by the nonvolatile memory controller based on the completion queue state. The interrupt vector state is associated with an interrupt vector in the host processing unit. Additionally, the method includes determining by the nonvolatile memory controller based on the interrupt vector state that the completion queue

contains an unprocessed completion status. The method also includes generating an interrupt message packet by the nonvolatile memory interface for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.

[0009] FIG. 1 is a block diagram of a computing system, in accordance with an embodiment of the present invention.

[00010] FIG. 2 is a block diagram of a network module, in accordance with an embodiment of the present invention.

[00011] FIG. 3 is a block diagram of a computing system, in accordance with an embodiment of the present invention.

[00012] FIG. 4 is a block diagram of a processor, in accordance with an embodiment of the present invention.

[00013] FIG. 5 is a block diagram of a host processing unit, in accordance with an embodiment of the present invention.

[00014] FIG. 6 is a block diagram of a submission queue, in accordance with an embodiment of the present invention.

[00015] FIG. 7 is a block diagram of a completion queue, in accordance with an embodiment of the present invention.

[00016] FIG. 8 is a block diagram of a host controller interface, in accordance with an embodiment of the present invention.

[00017] FIG. 9 is a block diagram of a submission manager, in accordance with an embodiment of the present invention.

[00018] FIG. 10 is a block diagram of a completion manager, in accordance with an embodiment of the present invention.

[00019] FIG. 11 is a block diagram of an interrupt manager, in accordance with an embodiment of the present invention.

[00020] FIG. 12 is a block diagram of a completion queue state, in accordance with an embodiment of the present invention.

[00021] FIG. 13 is a block diagram of an interrupt vector state, in accordance with an embodiment of the present invention.

[00022] FIG. 14 is a block diagram of an aggregate time indicator, in accordance with an embodiment of the present invention.

[00023] FIG. 17 is a flow chart for a method of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention.

[00024] FIG. 18 is a flow chart for a method of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention.

[00025] FIG. 19 is a flow chart for a portion of a method of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention.

[00026] FIG. 20 is a flow chart for a portion of a method of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention.

[00027] FIG. 21 is a flow chart for a portion of a method of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention.

[00028] FIG. 22 is a flow chart for a portion of a method of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION

[00029] In various embodiments, a nonvolatile memory controller includes an interrupt manager that identifies a completion queue containing an unprocessed completion status in a host processing unit. The interrupt manager generates an interrupt message packet for generating an interrupt in the host processing unit. Moreover, the interrupt is associated with the completion queue containing the unprocessed completion status. In this way, the interrupt manager alerts the host processing unit to the unprocessed completion status in the completion queue.

[00030] FIG. 1 illustrates a computing system 100, in accordance with an embodiment of the present invention. The computing system 100 includes a host processing unit 110, a communication network 115, a nonvolatile memory controller 105, and a nonvolatile memory device 140. The communication network 115 is coupled (e.g., connected) to the host processing unit 110 and the nonvolatile memory controller 105. Additionally, the nonvolatile memory controller 105 is coupled (e.g., connected) to the nonvolatile memory device 140. In various embodiments, the nonvolatile memory device 140 is a flash storage device and the nonvolatile memory controller 105 is a flash controller.

[00031] In various embodiments, the computing system 100 is a desktop computer, a server, a computer workstation, or the like. In some embodiments, the computing system 100 is a portable electronic device, such as a portable computer, a mobile phone, a digital camera, a media player, a personal digital assistant, a pager, a global positioning system, or the like.

[00032] The communication network 115 facilitates communication between the host processing unit 110 and the nonvolatile memory controller 105. For example, the communication network 115 may be a packet communication network, such as a Peripheral Component Interconnect Express (PCIe) network. The nonvolatile memory controller 105 manages data stored in the nonvolatile memory device 140 and communicates with the host processing unit 110 through the communication network 115 for transferring data between the host processing unit 110 and the nonvolatile memory device 140. In various embodiments, the nonvolatile memory controller 105 processes nonvolatile memory commands generated by the host processing unit 110 for controlling operation of the nonvolatile memory controller 105. In some embodiments, the host processing unit 110 generates Enterprise Non-Volatile Memory Host Control Interface (eNVMHCI) commands from the host processing unit 110 and the nonvolatile memory controller 105 processes the eNVMHCI commands to manage operation of the nonvolatile memory controller 105.

[00033] In various embodiments, the nonvolatile memory controller 105 includes a host controller interface 120, a network module 125, a control module 130, a processor module 145, and a controller memory 160. The network module 125 is coupled (e.g., connected) to the host controller interface 120, the control module 130, the processor module 145, and the controller memory 160. Additionally, the host controller interface 120 is coupled (e.g., connected) to the communication network 115, and the control module 130 is coupled (e.g., connected) to the nonvolatile memory device 140. Furthermore, the processor module 145 includes processors 150 coupled (e.g., connected) to the network module 125. In these embodiments, each of the

host controller interface 120, the control module 130, the processors 150, and the controller memory 160 is a functional unit of the nonvolatile memory controller 105.

[00034] In various embodiments, each of the host controller interface 120, the control module 130, the processor module 145, and the controller memory 160 is source node or a destination node of the nonvolatile memory controller 105. In this way, each functional unit of the nonvolatile memory controller 105 may be a source node or a destination node. In some embodiments, one or more of the host controller interface 120, the control module 130, the processor module 145, and the controller memory 160 is both a source node and a destination node of the nonvolatile memory controller 105. In this way, a functional unit of the nonvolatile memory controller 105 may be both a source node and a destination node.

[00035] The host controller interface 120 facilitates communication between the communication network 115 and the functional units of the nonvolatile memory controller 105 through the network module 125. The control module 130 manages data in the nonvolatile memory device 140. For example, the control module 130 may read data from the nonvolatile memory device 140 and write data into the nonvolatile memory device 140.

[00036] The controller memory 160 stores data being transferred from the host processing unit 110 to the nonvolatile memory device 140. Additionally, the controller memory 160 stores data being transferred from the nonvolatile memory device 140 to the host processing unit 110. In this way, the controller memory 160 is an intermediate storage location for temporarily storing data being transferred between the host processing unit 110 and the nonvolatile memory device 140. In various embodiments, the controller memory 160 includes

a random access memory (RAM), such as a static random access memory (SRAM) or a dynamic random access memory (DRAM).

[00037] In various embodiments, the host processing unit 110 generates nonvolatile memory commands and stores the nonvolatile memory commands in one or more submission queues contained in the host processing unit 110. The host controller interface 120 determines that a submission queue in the host processing unit 110 contains a nonvolatile memory command, generates a request packet, and transmits the request packet to the host processing unit 110 through the communication network 115. In response to the request packet generated by the host controller interface 120, the host processing unit 110 generates a completion packet including a nonvolatile memory command contained in a submission queue and transmits the completion packet to the host controller interface 120 of the nonvolatile memory controller 105 through the communication network 115.

[00038] The host controller interface 120 retrieves the completion packet including the nonvolatile memory command, generates a request message packet including the nonvolatile memory command based on the request packet, and provides the request message packet to the network module 125. In turn, the network module 125 routes the request message packet to the processor module 145. The processor module 145 processes the nonvolatile memory command in the request message packet, generates a completion message packet including a completion status (e.g., a completion entry) based on the request message packet, and provides the completion message packet to the network module 125. The network module 125 routes the completion message packet to the host controller interface 120.

[00039] The host controller interface 120 generates a request packet including the completion status based on the completion message packet and transmits the request packet to the host processing unit 110 through the communication network 115. In turn, the host processing unit 110 stores the completion status of the request message packet received from the host controller interface 120 in a completion queue contained in the host processing unit 110. Additionally, the host processing unit 110 processes the completion status to determine the status of processing the nonvolatile memory command (i.e., a processing status).

[00040] In various embodiments, a processor module 145 processes the nonvolatile memory command in a request message packet by generating additional request message packets, each of which includes a command. The processor 150 provides the request message packets to the network module 125. In turn, the network module 125 routes each of the request message packets received from the processor module 145 to a functional unit of the nonvolatile memory controller 105 identified in the request message packet. In this way, the processor 150 functions as a source node and the functional unit receiving the request message packet functions as a destination node.

[00041] The functional unit receiving a request message packet from the processor 150 through the network module 125 processes the command in the request message packet, generates a completion message packet including a completion status based on the request packet, and provides the completion message packet to the network module 125. The completion status of the completion message packet indicates a status of the command processed by the functional unit (i.e., a processing status). The network module 125 routes the completion message packet to the processor 150.

[00042] In various embodiments, the processor module 145 processes the nonvolatile memory command in the request message packet received from the host controller interface 120 by generating a request message packet including a data transfer command for transferring data between the host processing unit 110 and the controller memory 160, and generating another request message packet including a data transfer command for transferring data between the controller memory 160 and the nonvolatile memory device 140. In this way, the processor module 145 generates request message packets for transferring data in a piecemeal manner between the host processing unit 110 and the nonvolatile memory device 140 based on the request message packet including the nonvolatile memory command.

[00043] In some cases, each functional unit receiving a request message packet from the processor module 145 generates one or more request data packets based on the request message packet. Each of the request data packets is a request for transferring data between functional units of the nonvolatile memory controller 105 through the network module 125 or transferring data between the host processing unit 110 and the host controller interface 120. For example, the control module 130 may generate request data packets and provide the request data packets to the network module 125 for routing to the controller memory 160. In this example, the controller memory 160 generates completion packets including data stored in the controller memory 160 and provides the completion packets to the network module 125 for routing to the control module 130.

[00044] In various embodiments, the nonvolatile memory controller 105 is implemented in an integrated circuit of an integrated circuit device which may include an integrated circuit package containing the integrated circuit. In some embodiments, the nonvolatile memory

controller 105 is implemented in a single integrated circuit die. In other embodiments, the nonvolatile memory controller 105 is implemented in more than one integrated circuit die of an integrated circuit device which may include a multichip package containing the integrated circuit die.

[00045] In some embodiments, the host processing unit 110, the communication network 115, and the nonvolatile memory controller 105 are mounted to a printed circuit board. In these embodiments, the host processing unit 110 and the nonvolatile memory controller 105 are directly coupled to the communication network 115. For example, the host processing unit 110 and the nonvolatile memory controller 105 may be directly connected to the communication network 115 through wires in the printed circuit board.

[00046] FIG. 2 illustrates the network module 125, in accordance with an embodiment of the present invention. The network module 125 includes a message network 200 and a data network 205. Each of the message network 200 and the data network 205 is coupled (e.g., connected) to the host controller interface 120, the control module 130, the processor module 145, and the controller memory 160.

[00047] The message network 200 routes message packets, such as request message packets and completion message packets, between functional units of the nonvolatile memory controller 105. In various embodiments, the message network 200 routes message packets among functional units of the nonvolatile memory controller 105 by using an inter-processor communication (IPC) protocol.

[00048] The data network 205 routes data packets, such as data request packets and data completion packets, between functional units of the nonvolatile memory controller 105. In various embodiments, the data network 205 routes data packets among functional units of the nonvolatile memory controller 105 by using an inter-processor communication (IPC) protocol.

[00049] FIG. 3 illustrates a computing system 100, in accordance with an embodiment of the present invention. In this embodiment, the control module 130 includes a storage controller 300. The storage controller 300 is coupled (e.g., connected) to the network module 125 and the nonvolatile memory device 140. Furthermore, the controller memory 160 includes a buffer memory 315 coupled to the network module 125. Each of the storage controller 300 and the buffer memory 315 is a functional unit of the nonvolatile memory controller 105.

[00050] The storage controller 300 manages data in the nonvolatile memory device 140. For example, the storage controller 300 may read data from the nonvolatile memory device 140 and write data into the nonvolatile memory device 140. The buffer memory 315 stores data being transferred from the host processing unit 110 to the nonvolatile memory device 140. Additionally, the buffer memory 315 stores data being transferred from the nonvolatile memory device 140 to the host processing unit 110. In this way, the buffer memory 315 is a temporary storage location for data being transferred between the host processing unit 110 and the nonvolatile memory device 140. In various embodiments, the buffer memory 315 includes a random access memory (RAM), such as a static random access memory (SRAM).

[00051] In some embodiments, the controller memory 160 includes a memory interface 325 coupled (e.g., connected) to a memory module 320 external of the nonvolatile memory controller 105. For example, the nonvolatile memory controller 105 may be implemented in an

integrated circuit and the memory module 320 may be implemented in another integrated circuit. In these embodiments, the controller memory 160 includes the memory interface 325 and the memory module 320 in addition to the buffer memory 315. Moreover, the memory interface 325 is a functional unit of the nonvolatile memory controller 105.

[00052] The memory interface 325 facilitates communication between the network module 125 and the memory module 320. The memory module 320 stores data being transferred from the host processing unit 110 to the nonvolatile memory device 140. Additionally, the memory module 320 stores data being transferred from the nonvolatile memory device 140 to the host processing unit 110. In this way, the memory module 320 is a temporary storage location for data being transferred between the host processing unit 110 and the nonvolatile memory device 140. In various embodiments, the memory module 320 includes a random access memory (RAM), such as a dynamic random access memory (DRAM).

[00053] In various embodiments, a processor 150 receives a request message packet including a nonvolatile memory command from the host controller interface 120 through the network module 125 and processes the nonvolatile memory command in the request message packet by generating additional request message packets, each of which includes a command. The processor 150 provides the request message packets generated by the processor 150 to the network module 125. In turn, the network module 125 routes each of the request message packets to a functional unit of the nonvolatile memory controller 105. Each of the functional units receiving a request message packet from the processor 150 through the network module 125 processes the command in the request message packet, generates a completion message packet based on the request message packet, and provides the completion message packet to

the network module 125. The completion message packet includes a completion status indicating a processing status of the request message packet processed by the functional unit. The network module 125 routes the completion message packet to the processor 150.

[00054] In various embodiments, the processor 150 processes the nonvolatile memory command in the request message packet received from the host controller interface 120 by generating a request message packet including a data transfer command for transferring data between the host processing unit 110 and the controller memory 160, and generating another request message packet including a data transfer command (e.g., a flash command) for transferring data between the controller memory 160 and the nonvolatile memory device 140. For example, the processor 150 may generate a request message packet including a flash read command and a destination identifier that identifies the storage controller 300. In this example, the processor 150 provides the request message packet to the network module 125, and the network module 125 routes the request message packet to the storage controller 300 based on the destination identifier in a request message packet of the request message packet received from the processor 150. In turn, the storage controller 300 transfers the data from the nonvolatile memory device 140 to the buffer memory 315 based on the flash read command in the request message packet received from the processor 150.

[00055] Further in this example, the processor 150 generates a request message packet including a data transfer command and a destination identifier that identifies the host controller interface 120. In this example, the processor 150 provides the request message packet to the network module 125, and the network module 125 routes the request message packet to the host controller interface 120 based on the destination identifier. In turn, the host controller

interface 120 transfers the data from the buffer memory 315 to the host processing unit 110 based on the data transfer command in the request message packet received from the processor 150.

[00056] As another example, the processor 150 may generate a request message packet including a data transfer command and a destination identifier that identifies the host controller interface 120. In this example, the processor 150 provides the request message packet to the network module 125, and the network module 125 routes the request message packet to the host controller interface 120 based on the destination identifier. In turn, the host controller interface 120 transfers the data from the host processing unit 110 to the buffer memory 315 based on the data transfer command in the request message packet received from the processor 150.

[00057] Further in this example, the processor 150 generates a request message packet including a flash write command and a destination identifier that identifies the storage controller 300. In this example, the processor 150 provides the request message packet to the network module 125, and the network module 125 routes the request message packet to the storage controller 300 based on the destination identifier in the request message packet. In turn, the storage controller 300 transfers the data from the buffer memory 315 to the nonvolatile memory device 140 based on the flash write command in the request message packet received from the processor 150.

[00058] FIG. 4 illustrates the processor 150, in accordance with an embodiment of the present invention. The processor 150 includes a processing unit 400, a message network interface 405, a data network interface 410, an instruction memory 415, and a data memory 420. The

processing unit 400 is coupled (e.g., connected) to the message network interface 405, the data network interface 410, the instruction memory 415, and the data memory 420.

[00059] The message network interface 405 facilitates communication of message packets between the processing unit 400 and the message network 200. The data network interface 410 facilitates communication of data between the processing unit 400 and the data network 205. The instruction memory 415 stores computing instructions for the processing unit 400. The data memory 420 stores data for the processing unit 400. In various embodiments, the processing unit 400 receives a request message packet including a nonvolatile memory command from the host controller interface 120 through the message network interface 405 and writes data into the data memory 420 based on the nonvolatile memory command in the request message packet. For example, the processing unit 400 may write a nonvolatile memory command of the request message packet into the data memory 420. As another example, the processing unit 400 may write data contained in the request message packet into the data memory 420 based on the nonvolatile memory command.

[00060] Additionally, the processing unit 400 reads the data from the data memory 420 and provides the data to the data network 205 through the data network interface 410 for routing to the buffer memory 315. In this way, the processing unit 400 transfers the data received from the host controller interface 120 in the request message packet to the buffer memory 315. Alternatively, the processing unit 400 reads the data from the data memory 420 and provides the data to the data network 205 through the data network interface 410 for routing to the memory interface 325. In turn, the memory interface 325 writes the data into the memory

module 320. In this way, the processing unit 400 transfers the data received from the host controller interface 120 in the request message packet to the memory module 320.

[00061] In various embodiments, the processors 150 in the processor module 145 function as a pool of processors, a pipeline of processors (i.e., a processor pipeline), or some combination thereof. In some embodiments, one of the processors 150 in the processor module 145 is a control processor. In these embodiments, the control processor boots the nonvolatile memory controller 105 and performs overall control and management functions in the nonvolatile memory controller 105. For example, the control processor may generate interrupt requests and process interrupt requests. In some embodiments, the processing unit 400 of the processor 150 implements a Tensilica LX2 32-bit instruction set developed by the Tensilica Corporation of Santa Clara, California.

[00062] FIG. 5 illustrates the host processing unit 110, in accordance with an embodiment of the present invention. The host processing unit 110 includes a computing processor 500, a communication interface 510, and a memory system 515 coupled (e.g., connected) to each other through a computer bus 505. Moreover, the memory system 515 includes submission queues 520 and completion queues 525. The submission queues 520 store nonvolatile memory commands for controlling operation of the nonvolatile memory controller 105. The completion queues 525 store completion statuses corresponding to nonvolatile memory commands stored in the submission queues 520. In some embodiments, each of the completion queues 525 may be associated with one or more submission queues 520.

[00063] In various embodiments, the computing processor 500 generates nonvolatile memory commands for controlling the nonvolatile memory controller 105 and writes the nonvolatile

memory commands into the submission queues 520. The nonvolatile memory controller 105 obtains the nonvolatile memory commands stored in the submission queues 520 and processes the nonvolatile memory commands to manage operation of the nonvolatile memory controller 105, as is described more fully herein. Further, the nonvolatile memory controller 105 generates completion statuses corresponding to the nonvolatile memory commands stored in the submission queues 520 and provides the completion statuses to the host processing unit 110 for storage in the completion queues 525. In this way, the nonvolatile memory controller 105 writes the completion statuses to the completion queues 525 in the host processing unit 110.

[00064] FIG. 6 illustrates the submission queue 520, in accordance with an embodiment of the present invention. The submission queue 520 includes storage locations 600 for storing nonvolatile memory commands. In various embodiments, the submission queue 520 is a circular queue and includes a head 605 and a tail 610. For example, the submission queue 520 may include storage locations 600 of a PCIe memory in the memory system 515.

[00065] In operation, the computing processor 500 writes a nonvolatile memory command for controlling operation of the nonvolatile memory controller 105 to a storage location 600 at the tail 610 of the submission queue 520. Further, the computing processor 500 generates a write request packet including a tail pointer identifying the tail 610 of the submission queue 520. The host processing unit 110 transmits the write request packet to the nonvolatile memory controller 105 through the communication network 115. In this way, the host processing unit 110 writes the tail pointer to the nonvolatile memory controller 105 and updates a tail pointer stored in the nonvolatile memory controller 105 which also identifies the tail 610 of the submission queue 520.

[00066] The nonvolatile memory controller 105 determines the submission queue 520 contains at least one nonvolatile memory command based on the tail pointer stored in the nonvolatile memory controller 105 and based on a head pointer stored in the nonvolatile memory controller 105 that identifies the head 605 of the submission queue 520 stored in the host processing unit 110. Further, the nonvolatile memory controller 105 retrieves one or more nonvolatile memory commands from storage locations 600 starting at the tail 610 of the submission queue 520 and processes the nonvolatile memory commands, as is described more fully herein.

[00067] In various embodiments, the nonvolatile memory controller 105 initializes the head pointer stored in the nonvolatile memory controller 105 for identifying the head of the submission queue 520 to the tail pointer of the submission queue 520 received from the host processing unit 110. Further, the nonvolatile memory controller 105 updates the head pointer based on nonvolatile memory commands retrieved from the host processing unit 110, as is described more fully herein.

[00068] FIG. 7 illustrates the completion queue 525, in accordance with an embodiment of the present invention. The completion queue 525 includes storage locations 700 for storing completion statuses. In various embodiments, the completion queue 525 is a circular queue and includes a head 705 and a tail 710. For example, the completion queue 525 may include storage locations 700 of a PCIe memory in the memory system 515.

[00069] In operation, the host processing unit 110 receives a request packet including a completion status from the host controller interface 120 through the communication network 115. The computing processor 500 writes the completion status into the storage location 700 at

the tail 710 of the completion queue 525. Additionally, the host processing unit 110 reads completion statuses from storage locations 700 starting at the head 705 of the completion queue 525 to determine the status of the nonvolatile commands associated with the completion statuses that have been processed by the nonvolatile memory controller 105.

[00070] Further, the computing processor 500 generates a write request packet including a head pointer identifying the next storage location 700 at the head 705 of the completion queue 525 storing the next completion status. The host processing unit 110 transmits the write request packet to the nonvolatile memory controller 105 through the communication network 115. In this way, the host processing unit 110 writes the head pointer to the nonvolatile memory controller 105 and updates a head pointer stored in the nonvolatile memory controller 105 which also identifies the head 705 of the completion queue 525.

[00071] FIG. 8 illustrates the host controller interface 120, in accordance with an embodiment of the present invention. The host controller interface 120 includes a submission manager 800 and a completion manager 805. The submission manager 800 and the completion manager 805 are each coupled (e.g., connected) to the communication network 115 and the message network 200.

[00072] The submission manager 800 retrieves nonvolatile memory commands stored in the submission queues 520 of the memory system 515 in the host processing unit 110, generates request message packets based on the nonvolatile memory commands, and provides the request message packets to the message network 200 for routing to processors 150 of the nonvolatile memory controller 105. In various embodiments, the submission manager 800 retrieves a nonvolatile memory command stored in the memory system 515 of the host processing unit

110 by generating a request packet (e.g., a host memory read request packet), transmitting the request packet to the host processing unit 110 through the communication network 115, and receiving a completion packet containing the nonvolatile memory command from the host processing unit 110 through the communication network 115..

[00073] In some embodiments, the submission manager 800 retrieves nonvolatile memory commands stored in the submission queues 520 of the memory system 515 in the host processing unit 110 by retrieving the nonvolatile memory commands in parallel. In this way, the submission manager 800 retrieves the nonvolatile memory commands from the submission queues 520 substantially simultaneously.

[00074] The completion manager 805 receives completion message packets from processors 150 of the nonvolatile memory controller 105 through the message network 200, generates write request packets (e.g., memory write request packets) based on the completion message packets, and transmits the write request packets to the host processing unit 110 through the communication network 115. Moreover, the completion message packets each include a completion status associated with a nonvolatile memory command processed by a processor 150. The host processing unit 110 processes the write request packets including the completion statuses received from the completion manager 805 by storing the completion statuses into completion queues 525 of the host processing unit 110.

[00075] In some embodiments, the completion status indicates whether processing of the nonvolatile memory command by the nonvolatile memory controller 105 was a success or a failure. In these embodiments, the host controller interface 120 may perform additional operations based on the completion status in the completion message packet. For example, if

the completion status indicates a failure then the host controller interface 120 may perform error recovery operations based on the completion message packet.

[00076] FIG. 9 illustrates the submission manager 800, in accordance with an embodiment of the present invention. The submission manager 800 includes a command fetch module 900, command assembly buffers 905, a command dispatch module 910, message output queues 915, and a memory unit 920. The command fetch module 900 is coupled (e.g., connected) to the communication network 115, the command assembly buffers 905, and the memory unit 920. Additionally, the memory unit 920 is coupled (e.g., connected) to the communication network 115. The command dispatch module 910 is coupled (e.g., connected) to the command assembly buffers 905 and the message output queues 915. Further, each of the message output queues 915 is coupled (e.g., connected) to the message network 200.

[00077] The memory unit 920 stores submission queue head pointers 925 corresponding to the submission queues 520 stored in the memory system 515 of the host processing unit 110. The memory unit 920 also stores submission queue tail pointers 930 corresponding to the submission queues 520.

[00078] In various embodiments, the host processing unit 110 maintains (e.g., updates) the submission queue tail pointers 930 so that each of the submission queue tail pointers 930 identifies the storage location 600 at the tail 610 of the corresponding submission queue 520. In these embodiments, the command fetch module 900 maintains (e.g., updates) the submission queue head pointers 925 so that each of the submission queue head pointers 925 identifies the storage location 600 at the head 605 of the corresponding submission queue 520. The command fetch module 900 determines whether a submission queue 520 contains a

nonvolatile memory command based on both the submission queue head pointer 925 and the submission queue tail pointer 930 of the submission queue 520.

[00079] For example, the command fetch module 900 may determine that the submission queue 520 contains at least one nonvolatile memory command if the submission queue head pointer 925 and the submission queue tail pointer 930 of the submission queue 520 identify different storage locations 600 in the submission queue 520. Further in this example, the command fetch module 900 determines the submission queue 520 does not contain any nonvolatile memory command (i.e., the submission queue 520 is empty) if the submission queue head pointer 925 and the submission queue tail pointer 930 of the submission queue 520 identify the same storage location 600 in the submission queue 520.

[00080] In operation, the command fetch module 900 monitors the submission queue head pointers 925 and the submission queue tail pointers 930. If the command fetch module 900 identifies a submission queue 520 storing at least one nonvolatile memory command, the command fetch module 900 generates a read request packet including an identifier identifying a storage location 600 in the submission queue 520 and transmits the read request packet to the host processing unit 110 through the communication network 115. The host processing unit 110 reads the nonvolatile memory command from the storage location 600 of the submission queue 520 based on the identifier of the read request packet, generates a completion packet including the nonvolatile memory command, and transmits the completion packet to the command fetch module 900 through the communication network 115.

[00081] The command fetch module 900 selects a command assembly buffer 905 and writes the nonvolatile memory command contained in the completion packet to the selected command

assembly buffer 905. Additionally, the command fetch module 900 updates the submission queue head pointer 925 of the submission queue 520 containing the nonvolatile memory command to indicate that the host controller interface 120 retrieved the nonvolatile memory command from the submission queue 520. For example, the command fetch module 900 may update (e.g., increment) the submission queue head pointer 925 of the submission queue 520 to point to the storage location 600 of the submission queue 520 containing the next nonvolatile memory command to be retrieved by the host controller interface 120.

[00082] The command dispatch module 910 monitors the command assembly buffers 905, identifies the command assembly buffer 905 storing the nonvolatile memory command, selects a processor 150 of the nonvolatile memory controller 105, and generates a request message packet including the nonvolatile memory command and an identifier of the processor 150. Further, the command dispatch module 910 selects a message output queue 915 and writes the request message packet into the selected message output queue 915. In this way, the command dispatch module 910 transfers the content of the command assembly buffer 905 to the selected message output queue 915. In turn, the message output queue 915 provides the request message packet to the message network 200 for routing to the processor 150 identified by the identifier in the request message packet.

[00083] FIG. 10 illustrates the completion manager 805, in accordance with an embodiment of the present invention. The completion manager 805 includes a completion queue update module 1000, a completion queue engine 1010, message input queues 1015, a memory unit 1020, message output queues 1035, and an interrupt manager 1040. The completion queue update module 1000 is coupled (e.g., connected) to the communication network 115, the

memory unit 1020, and the completion queue engine 1010. Additionally, the memory unit 1020 is coupled (e.g., connected) to the communication network 115 and the interrupt manager 1040. Each of the message input queues 1015 and each of the message output queues 1035 is coupled (e.g., connected) to the completion queue engine 1010 and the message network 200. Further, the interrupt manager 1040 is coupled (e.g., connected) to the communication network 115 and the completion queue engine 1010.

[00084] The memory unit 1020 stores completion queue head pointers 1025 corresponding to the completion queues 525 stored in the memory system 515 of the host processing unit 110. The memory unit 1020 also includes completion queue tail pointers 1030 corresponding to the completion queues 525.

[00085] In various embodiments, the host processing unit 110 maintains (e.g., updates) the completion queue head pointers 1025 so that each of the completion queue head pointers 1025 identifies the storage location 700 at the head 705 of the corresponding completion queue 525. In these embodiments, the completion queue update module 1000 maintains (e.g., updates) the completion queue tail pointers 1030 so that each of the completion queue tail pointers 1030 identifies the storage location 700 at the tail 710 of the corresponding completion queue 525.

[00086] In operation, a message input queue 1015 receives a completion message packet from a processor 150 of the nonvolatile memory controller 105 through the message network 200 and stores the completion message packet. The completion message packet is associated with a request message packet including a nonvolatile memory command processed by the processor 150. Moreover, the completion message packet includes a completion status indicating a processing status of the nonvolatile memory command in the request message

packet. The completion queue engine 1010 monitors the message input queues 1015, identifies the message input queue 1015 storing the completion message packet, reads the completion message packet from the message input queue 1015 storing the completion message packet, and provides the completion message packet to the completion queue update module 1000.

[00087] The completion queue update module 1000 generates a write request packet (e.g., a memory write request packet) based on the completion message packet and transmits the write request packet to the host processing unit 110 through the communication network 115. The write request packet includes the completion status of the nonvolatile memory command and a completion queue tail pointer 1030 identifying a storage location 700 at the tail 710 of a completion queue 525 for storing the completion status. Additionally, the completion queue update module 1000 updates the completion queue tail pointer 1030 in the nonvolatile memory controller 105 to identify the storage location 700 in the completion queue 525 for storing the next completion status. In some embodiments, the completion queue update module 1000 inserts the current submission queue head pointer 925 of the submission queue 520 associated with the completion queue 525 into the write request packet. In this way, the completion queue update module 1000 provides an update of the submission queue head pointer 925 to the host processing unit 110.

[00088] The host processing unit 110 receives the write request packet and stores the completion status contained in the write request packet into the storage location 700 at the tail 710 of the completion queue 525 identified by the completion queue tail pointer 1030 in the write request packet. The host processing unit 110 also updates a tail pointer of the completion

queue 525 maintained in the host processing unit 110 (i.e., a local tail pointer) to identify the storage location 700 in the completion queue 525 for storing the next completion status.

[00089] Additionally, the host processing unit 110 receives an alert from the host controller interface 120 of the nonvolatile memory controller 105 indicating that a completion queue 525 contains an unprocessed completion status. In turn, the host processing unit 110 reads the completion status at the head 705 of the completion queue 525. In this way, the host processing unit 110 processes the completion status. Additionally, the host processing unit 110 updates a head pointer of the completion queue 525 maintained in the host processing unit 110 (i.e., a local head pointer) to identify the storage location 700 of the completion queue 525 containing the next completion status for processing. In this way, the host processing unit 110 frees the storage location 600 containing the processed completion status.

[00090] Further, the host processing unit 110 generates a write request packet including the head pointer of the completion queue 525 (i.e., a local head pointer) and transmits the request packet to the host controller interface 120 of the nonvolatile memory controller 105 through the communication network 115. In turn, the completion queue update module 1000 updates the completion queue head pointer 1025 of the completion queue 525 stored in the memory unit 1020 of the completion manager 805 with the head pointer of the request packet. In this way, the host processing unit 110 updates the completion queue head pointer 1025 in the memory unit 1020 of the completion manager 805.

[00091] Additionally, the host processing unit 110 updates a head pointer of the submission queue 520 maintained in the host processing unit 110 (i.e., a local head pointer) based on the submission queue head pointer 925 contained in the request packet, for example by setting the

head pointer maintained in the host processing unit 110 to the submission queue head pointer 925 contained in the write request packet. In this way, the host processing unit 110 frees storage locations 600 containing nonvolatile memory commands processed by the nonvolatile memory controller 105 from the submission queue 520.

[00092] The completion queue engine 1010 also generates a notification message packet based on the completion message packet read from the message input queue 1015 and writes the notification message packet into a message output queue 1035. The notification message packet includes a completion status indicating the processing status of the completion message packet read from the message input queue 1015. For example, the completion status of the notification message packet may indicate whether processing of the completion message packet by the completion manager 805 was a success or a failure. The message output queue 1035 provides the notification message packet to the message network 200. In turn, the message network 200 routes the notification message packet to the processor 150 of the nonvolatile memory controller 105 that generated the completion message packet read from the message input queue 1015.

[00093] FIG. 11 illustrates the interrupt manager 1040, in accordance with an embodiment of the present invention. The interrupt manager 1040 includes an interrupt manager controller 1100, a completion queue state memory 1105, and an interrupt vector state memory 1110. The interrupt manager controller 1100 is coupled (e.g., connected) to the completion manager 805, the communication network 115, the completion queue state memory 1105, and the interrupt vector state memory 1110.

[00094] In various embodiments, the interrupt manager 1040 (e.g., the interrupt manager controller 1100) monitors completion queue events and generates completion queue states 1115, each of which is associated with a corresponding completion queue 525 in the host processing unit 110. The completion queue state 1115 indicates the occurrence of completion queue events associated with the completion queue 525, as is described more fully herein. The interrupt manager 1040 stores the completion queue states 1115 into the completion queue state memory 1105.

[00095] Additionally, the interrupt manager 1040 generates interrupt vector states 1125 based on the completion queue states. Each of interrupt vector states 1125 is associated with a corresponding interrupt vector in the host processing unit 110. The interrupt vector state 1125 of an interrupt vector indicates whether one or more completion queues 525 associated with the interrupt vector state 1125 contain an unprocessed completion status, as is described more fully herein. The interrupt manager 1040 stores the interrupt vector states 1125 into the interrupt vector state memory 1110. In various embodiments, the interrupt manager 1040 maps one or more completion queues 525 to an interrupt vector in the host processing unit 110. In this way, the interrupt manager 1040 associates each of the completion queues 525 as well as the completion queue state 1115 of the completion queue 525 with the interrupt vector state 1125 of the interrupt vector.

[00096] Additionally, the interrupt manager 1040 includes configuration registers 1120, each of which is associated with a corresponding completion queue state 1115. The configuration register 1120 associated with a completion queue state 1115 stores configuration data for the completion queue state 1115. The configuration data stored in the configuration register 1120

includes an interrupt vector identifier of the interrupt associated with the completion queue state 1115. Moreover, the interrupt vector identifies an interrupt vector state 1125 associated with the interrupt vector. In this way, the interrupt vector identifies an interrupt vector state 1125 associated with the completion queue state 1115. In various embodiments, more than one completion queue state 1115 may be associated with the same interrupt vector state 1125.

[00097] Further, the interrupt manager 1040 includes configuration registers 1130, each of which is associated with a corresponding interrupt vector state 1125. The configuration register 1130 associated with an interrupt vector state 1125 stores configuration data for the interrupt vector state 1125. The configuration data stored in the configuration register 1130 includes the interrupt vector associated with the interrupt vector state 1125. Additionally, the configuration data may include other information for generating an interrupt message packet to trigger an interrupt in the host processing unit 110, as is described more fully herein. For example, the configuration data may include an interrupt type indicating a type of the interrupt associated with the interrupt vector state 1125. As another example, the configuration data may include one or more threshold values or enable values for controlling a rate at which interrupts are triggered in the host processing unit 110, as is described more fully herein.

[00098] The interrupt manager 1040 determines based on the interrupt vector state 1125 whether any completion queue 525 associated with the interrupt vector state 1125 contains an unprocessed completion status. If the interrupt manager 1040 determines at least one of the completion queues 525 contains an unprocessed completion status, the interrupt manager 1040 generates an interrupt message packet, which includes the interrupt vector associated with the interrupt vector state 1125. In some embodiments, the interrupt manager 1040 refrains from

generating further interrupt message packets unless one or more conditions in the interrupt vector state 1125 are satisfied, as is described more fully herein. In this way, the interrupt manager 1040 controls a transmission rate of interrupt packets transmitted to the host processing unit 110.

[00099] The interrupt manager 1040 transmits the interrupt message packet to the host processing unit 110 through the communication network 115. In turn, the communication interface 510 of the host processing unit 110 generates an interrupt in the computing processor 500 based on the interrupt vector contained in the interrupt message packet. In this way, the interrupt message packet generates (i.e., triggers) the interrupt in the host processing unit 110 for alerting the host processing unit 110 of an unprocessed completion status in the completion queue 525 associated with the interrupt vector. Because the nonvolatile memory controller 105 alerts the host processing unit 110 to an unprocessed completion status in the completion queue 525, the host processing unit 110 need not include resources for monitoring the completion queue 525 for an unprocessed completion status. Furthermore, because the interrupt manager 1040 generates interrupt message packets for alerting the host processing unit 110 of unprocessed completion statuses in the completion queues 525 of the host processing unit 110, the processors 150 of the nonvolatile memory controller 105 need not consume computing resources for determining whether the completion queues 525 of the host processing unit 110 contain unprocessed completion statuses or for alerting the host processing unit 110 of unprocessed completion statuses in the completion queues 525.

[000100] In response to generation of the interrupt, the computing processor 500 identifies and processes any unprocessed completion status in one or more completion queues 525 associated

with the interrupt vector. For example, the interrupt vector may indicate an address of an interrupt service routine (ISR) for identifying and processing any unprocessed completion queue status in the completion queue 525 associated with the interrupt vector. In this example, the computing processor 500 executes the interrupt service routine in response to generation of the interrupt.

[000101]In various embodiments, the host processing unit 110 generates a hardware interrupt in response to receiving an interrupt message packet. In some embodiments, the communication interface 510 generates the hardware interrupt by asserting a signal on a dedicated line (e.g., wire) connected to the communication interface 510 and the computing processor 500. For example, the dedicated line may be connected to an interrupt pin of the computing processor 500.

[000102]In some embodiments, the hardware interrupt generated in the host processing unit 110 is a message signal interrupt (MSI) or an extended message signal interrupts (MSI-X) as defined in the PCI Specification 3.0. In some embodiments, the hardware interrupt generated in the host processing unit 110 is an INTx interrupt as defined in a PCIe specification, such as the PCIe Specification 3.0.

[000103]In some embodiments, the interrupt manager controller 1100 generates and updates the completion queue states 1115 in response to completion queue events occurring in the nonvolatile memory controller 105. An example of a completion queue event is the host processing unit 110 updating a completion queue head pointer 1025 in the completion manager 805 for a completion queue 525 in the host processing unit 110. Another example of a completion queue event is the completion manager 805 receiving a completion message

including a completion status to be stored in a completion queue 525 of the host processing unit 110 and in which a completion queue event flag is set. In various embodiments, the interrupt manager controller 1100 updates the completion queue states 1115 on an ongoing basis as the completion queue events occur. For example, the interrupt manager controller 1100 may include a state machine for monitoring completion queue events and updating the completion queue states 1115 in the completion queue state memory 1105 in response to detecting the occurrence of a completion queue event.

[000104] The interrupt manager controller 1100 generates and updates the interrupt vector states 1125 based on the completion queue states 1115. The interrupt vector state 1125 indicates whether a completion queue 525 associated with the interrupt vector state 1125 contains a completion status that has not been processed by the host processing unit 110 (i.e., an unprocessed completion statuses). In various embodiments, the interrupt manager controller 1100 periodically updates the interrupt vector states 1125 based on the completion queue states 1115.

[000105] In some embodiments, the interrupt manager 1040 performs a scan of the completion queue state memory 1105 (i.e., a completion queue scan) as well as a scan of the completion queue head pointers 1025 and the completion queue tail pointers 1030. Further, the interrupt manager 1040 updates the interrupt vector states 1125 based on the completion queue states 1115, the completion queue head pointers 1025, and completion queue tail pointers 1030. The interrupt manager 1040 then performs a scan of the interrupt vector state memory 1110 (i.e., an interrupt vector scan) and determines based on each of the interrupt vector states 1125 whether to generate an interrupt message packet for the interrupt associated with the interrupt vector

state 1125. In this way, the interrupt manager 1040 determines whether to generate interrupt message packets in two distinct phases of operation (i.e., a completion queue scan and an interrupt vector scan).

[000106] In various embodiments, the interrupt manager 1040 transmits an interrupt message packet to the host processing unit 110 through the communication network 115 and clears the interrupt vector state 1125. For example, the interrupt manager 1040 may clear the interrupt vector state 1125 by clearing the interrupt event indicators 1300 and the interrupt status 1330 in the interrupt vector state 1125.

[000107] In various embodiments, the interrupt manager 1040 is a hardware mechanism for generating interrupt message packets. For example, the interrupt manager controller 1100 in the interrupt manager 1040 may be a sequential logic circuit (e.g., a state machine). Because the interrupt manager 1040 is a hardware mechanism, the interrupt manager 1040 generates interrupt message packets more quickly than a software mechanism executing computing instructions to perform the same function.

[000108] FIG. 12 illustrates the completion queue state 1115, in accordance with an embodiment of the present invention. The completion queue state 1115 includes one or more completion queue event indicators 1200. In the embodiment of FIG. 12, the completion queue event indicators 1200 include a doorbell update status 1205 and an event count 1210.

[000109] The doorbell update status 1205 indicates whether the host processing unit 110 has performed a doorbell update event since the last time the interrupt manager 1040 cleared the completion queue state 1115. In the doorbell update event, the host processing unit 110

updates the completion queue head pointer 1025 of the completion queue 525 associated with the completion queue state 1115. In various embodiments, the interrupt manager controller 1100 detects occurrences of the host processing unit 110 writing a head pointer 1025 into the memory unit 1020 of the completion manager 805 and sets the doorbell update status 1205 for a completion queue 525 to indicate at least one doorbell update event has occurred for the completion queue 525. In turn, the interrupt manager 1040 stores the doorbell update status 1205 into the completion queue state 1115 associated with the completion queue 525.

[000110] In various embodiments, a processor 150 generates a completion message packet including a completion status for a completion queue 525. Additionally, the processor 150 sets a completion queue event flag in the completion message packet. In these embodiments, the event count 1210 in the completion queue state 1115 associated with the completion queue 525 indicates a number of completion packets generated by the processors 150 in which a completion queue event flag is set since the last time the interrupt manager 1040 cleared the completion queue state 1115. Moreover, the completion queue manager 1040 generates a write request packet based on the completion message packet and transmits the write request packet to the host processing unit 110. In response to the completion queue manager 1040 transmitting the write request packet to the host processing unit 110, the interrupt manager controller 1100 updates the event count 1210 to indicate an completion queue update event has occurred.

[000111] FIG. 13 illustrates the interrupt vector state 1125, in accordance with an embodiment of the present invention. The interrupt vector state 1125 includes one or more interrupt event indicators 1300, an aggregate time indicator 1325, and an interrupt status 1330. In the

embodiment of FIG. 13, the interrupt event indicators 1300 include an empty queue indicator 1310, an aggregate doorbell update status 1315, and an aggregate event count 1320.

[000112] The interrupt status 1330 indicates a state of the interrupt associated with the interrupt vector state 1125. The interrupt manager 1040 initializes the interrupt status 1330 to an idle state. Moreover, the interrupt manager 1040 updates the interrupt status 1330 of the interrupt vector state 1125 based on the interrupt event indicators 1300 in the interrupt vector state 1125 when updating the interrupt vector state 1125. Further, the interrupt manager 1040 generates an interrupt message packet for the interrupt vector state 1125 if the interrupt status 1330 indicates the interrupt associated with the interrupt vector state 1125 is pending (i.e., the interrupt status 1330 is set to a pending state). Moreover, the interrupt message packet includes the interrupt vector associated with the interrupt vector state 1125.

[000113] In various embodiments, the interrupt manager 1040 sets the empty queue indicator 1310 of the interrupt vector state 1125 if all completion queues 525 associated with the interrupt vector state 1125 are empty. The interrupt manager 1040 determines a completion queue 525 associated with a completion queue state 1115 is empty by determining the completion queue head pointer 1025 and the completion queue tail pointer 1030 of the completion queue 525 identify the same storage location 700 in the completion queue 525. Moreover, the interrupt manager 1040 does not generate an interrupt message packet based on the interrupt vector state 1125 when the empty queue indicator 1310 is set. In this way, the interrupt manager 1040 is inhibited from generating the interrupt message packet.

[000114] In some embodiments, the interrupt manager 1040 clears the interrupt status 1330 to inhibit generation of an interrupt message. For example, if the interrupt status 1330 is set

during a previous scan of the interrupt vector state memory 1110 and the empty queue indicator 1310 is set during a current scan of the interrupt vector state memory 1110, the interrupt manager controller 1100 clears the interrupt status 1330 to prevent generation of another interrupt associated with interrupt vector state 1125.

[000115] In various embodiments, the interrupt manager 1040 generates the aggregate event count 1320 in the interrupt vector state 1125 by summing the event counts 1210 contained in the completion queue states 1115 associated with the interrupt vector state 1125. Further, the interrupt manager 1040 aggregates (i.e., adds together) the sum of event counts 1210 for each update of the interrupt vector state 1125 since that last time the interrupt vector state 1125 was cleared. The interrupt manager 1040 sets the interrupt status 1330 of the interrupt vector state 1125 to a pending state if the aggregate event count 1320 of the interrupt vector state 1125 has reached an aggregate event count threshold and all conditions in the interrupt vector state 1125 are satisfied (e.g., the empty queue indicator 1310 is clear). In this way, the interrupt manager 1040 controls a transmission rate of interrupt message packets to the host processing unit 110 based on the aggregate event count threshold. In some embodiments, the aggregate event count threshold is a user programmable value in the interrupt manager 1040.

[000116] The aggregate time indicator 1325 indicates a time period between the last time the interrupt manager 1040 generated an interrupt message packet for all completion queues 525 associated with an interrupt vector state 1125. In various embodiments, the interrupt manager 1040 does not set the interrupt status 1330 to the pending state if the aggregate time indicator 1325 is enabled but has not reached an aggregate time threshold. In this way, the interrupt manager 1040 is inhibited from generating an interrupt message packet. In various

embodiments, the interrupt manager 1040 sets the aggregate doorbell update status 1315 to indicate the host processing unit 110 has updated the completion queue head pointer 1025 for all completion queues 525 associated with the interrupt vector state 1125 since the last time the interrupt manager 1040 processed the interrupt vector state 1125.

[000117] When the aggregate time indicator 1325 is enabled, the interrupt manager 1040 controls a transmission rate of interrupt message packets to the host processing unit 110 based on the aggregate time threshold. In some embodiments, the aggregate time threshold is a user programmable value in the interrupt manager 1040. In various embodiments, one or more of the empty queue indicator 1310, the aggregate doorbell update status 1315, the aggregate event count 1320, and the aggregate time indicator 1325 is optional.

[000118] FIG. 14 illustrates the aggregate time indicator 1325, in accordance with an embodiment of the present invention. The aggregate time indicator 1325 includes an aggregate time counter 1400, a time stamp 1405, and a timer active indicator 1410. The interrupt manager controller 1100 sets the time stamp 1405 to a time generated by a timer (e.g., a global timer) in the nonvolatile memory controller 105 when clearing the interrupt vector state 1125 and when updating the interrupt vector state 1125. When updating the interrupt vector state 1125, the interrupt manager controller 1100 computes a difference between the timer in the nonvolatile memory controller 105 (e.g., the global timer) and the time stamp 1405, updates the aggregate time counter 1400 by adding the result to the aggregate time counter 1400, and sets the time stamp 1405 to the timer (e.g., global timer). In this way, the interrupt manager controller 1100 determines a time period between the last time the interrupt manager 1040

updated the interrupt vector state 1125 during an interrupt vector scan and the current time generated by the timer.

[000119] The timer active indicator 1410 indicates whether the aggregate time indicator 1325 is active counting time. In various embodiments, the interrupt manager controller 1100 sets the timer active indicator 1410 to indicate the aggregate time indicator 1325 is active when the interrupt manager 1040 sets the interrupt status 1330 to pending. In this way, the interrupt manager controller 1100 starts the aggregate time counter 1400 in the aggregate time indicator 1325. Moreover, the interrupt manager controller 1100 refrains from setting the interrupt status 1330 in the interrupt vector state 1125 when the aggregate time indicator 1325 is enabled but has not reached a threshold value.

[000120] FIG. 15 illustrates the configuration register 1120, in accordance with an embodiment of the present invention. The configuration register 1120 includes an interrupt vector identifier 1500 identifying the interrupt vector associated with the completion queue state 1115 that is associated with the configuration register 1120. The interrupt vector identifier 1500 identifies the interrupt associated with the completion queue 525 that is associated with the completion queue state 1115. Further, the interrupt vector identifier 1500 identifies the interrupt vector state 1125 associated with the interrupt. In this way, the interrupt vector identifier 1500 identifies the interrupt vector state 1125 associated with the completion queue state 1115.

[000121] FIG. 16 illustrates the configuration register 1130, in accordance with an embodiment of the present invention. The configuration register 1130 is associated with an interrupt vector state 1125 and includes an interrupt vector 1600 associated with that interrupt vector state 1125. In this way, the interrupt vector 1600 identifies the interrupt associated with the

interrupt vector state 1125. The configuration register 1130 also includes an interrupt type 1605 indicating a type of the interrupt. For example, the interrupt may be a message signal interrupt (MSI), an extended message signal interrupts (MSI-X), or an INTx virtual wire interrupt.

[000122]In some embodiments, the configuration register 1130 includes an event aggregation threshold 1610 and an event aggregation enable 1615. The event aggregation threshold 1610 is a threshold value for inhibiting generation of a subsequent interrupt status 1330 of an interrupt vector state 1125 for a period of time after generation of a previous interrupt status 1330 of that interrupt vector state 1125. For example, the event aggregation threshold 1610 may be a threshold for an aggregate event count (i.e., an aggregate event count threshold). The event aggregation enable 1615 indicates whether the aggregate event count 1320 is enabled.

[000123]In various embodiments, the interrupt manager 1040 performs a scan of the interrupt vector state memory 1110 and sets the interrupt status 1330 of an interrupt vector state 1125 to indicate the interrupt associated with the interrupt vector state 1125 is pending if one or more of the interrupt event indicators 1300 indicate a completion queue event has occurred. If the aggregate event count 1320 of the interrupt vector state 1125 has not reached the event aggregation threshold 1610 on a subsequent scan of the interrupt vector state memory 1110, the interrupt manager 1040 refrains from setting the interrupt status 1330 to pending. In this way, the interrupt manager 1040 controls a transmission rate of interrupt packets transmitted to the host processing unit 110. Furthermore, if the aggregate event count 1320 of the interrupt vector state 1125 has reached the event aggregation threshold 1610 on a subsequent scan of the interrupt vector state memory 1110, the interrupt manager 1040 sets the interrupt status 1330

of the interrupt vector state 1125 to pending and clears the aggregate event count 1320 in the interrupt vector state 1125. As a result, the aggregate event count 1320 may begin aggregating new completion queue events.

[000124] In some embodiments, the configuration register 1130 includes an time aggregation threshold 1620 and a time aggregation enable 1625. The time aggregation threshold 1620 is a threshold value for inhibiting generation of a subsequent interrupt status 1330 of an interrupt vector state 1125 for a period of time after generation of a previous interrupt status 1330 of that interrupt vector state 1125. The time aggregation enable 1625 indicates whether the aggregate time indicator 1325 is enabled.

[000125] In various embodiments, the interrupt manager 1040 performs a scan of the interrupt vector state memory 1110 and sets the interrupt status 1330 of an interrupt vector state 1125 to indicate the interrupt associated with the interrupt vector state 1125 is pending if one or more of the interrupt event indicators 1300 indicate a completion queue event has occurred.

Additionally, the interrupt manager 1040 enables the aggregate timer indicator 1325 by setting the timer active indicator 1410 of the aggregate timer indicator 1325. If the aggregate timer indicator 1325 of the interrupt vector state 1125 has not reached the time aggregation threshold 1620 on a subsequent scan of the interrupt vector state memory 1110, the interrupt manager 1040 refrains from setting the interrupt status 1330 to pending. In this way, the interrupt manager 1040 controls a transmission rate of interrupt packets transmitted to the host processing unit 110. Furthermore, if the aggregate timer indicator 1325 of the interrupt vector state 1125 has reached the time aggregation threshold 1620 on a subsequent scan of the interrupt vector state memory 1110 and at least one completion queue 525 associated with the

interrupt vector state 1125 contains at least one unprocessed completion status, the interrupt manager 1040 sets the interrupt status 1330 of the interrupt vector state 1125 to pending, keeps the timer active indicator 1410 of the aggregate timer indicator 1325 set, but clears the aggregate time counter 1400. As a result, the aggregate time counter 1400 begins to count from an initial value (e.g., zero).

[000126] FIG. 17 illustrates a method 1700 of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention. In step 1705, interrupt event indicators of interrupt vector states are updated based on the completion queue states. In various embodiments, the interrupt manager 1040 updates the interrupt event indicators 1300 of the interrupt vector states 1125 based on the completion queue states 1115, as is described more fully herein. For example, the interrupt manager 1040 may update the interrupt event indicators 1300 of each interrupt vector state 1125 based on the completion queue event indicators 1200 of each completion queues state 1115 associated with the interrupt vector state 1125. Additionally, the interrupt manager 1040 clears the completion queue states 1115, for example by setting each of the completion queue event indicators of the completion queue states 1115 to an initial value (e.g., zero). In this way, the interrupt manager 1040 resets the completion queue states 1115. The method 1700 then proceeds to step 1710.

[000127] In step 1710, interrupt statuses of the interrupt vector states are updated based on the interrupt event indicators. In various embodiments, the interrupt manager 1040 updates the interrupt statuses 1330 of the interrupt vector states 1125 based on interrupt event indicators 1300 of the interrupt vector states 1125, as is described more fully herein. For example, the interrupt manager 1040 may update the interrupt status 1230 of each interrupt vector state 1125

based on the interrupt event indicators 1300 of the interrupt vector state 1125 to indicate whether the interrupt status 1330 of the interrupt vector state 1125 is in an idle state or a pending state. In some embodiments, the interrupt manager 1040 updates the interrupt statuses 1330 of the interrupt vector states 1125 based on interrupt event indicators 1300 and the aggregate time indicators 1325 of the interrupt vector states 1125, as is described more fully herein. The method 1700 then proceeds to step 1715.

[000128]In step 1715, interrupt message packets are selectively generated based on the interrupt statuses. In various embodiments, the interrupt manager 1040 in the host controller interface 120 of the nonvolatile memory controller 105 selectively generates interrupt message packets based on the interrupt statuses 1330 of the interrupt vector states 1125. For example, the interrupt manager 1040 may generate an interrupt message packet for each interrupt vector state 1125 in which the interrupt status 1330 is pending (i.e., set to a pending state). The method 1700 then ends. In various embodiments, the method 1700 includes more than one iteration of the steps 1705-1715. In these embodiments, the method 1700 returns to step 1705 after step 1715 for each additional iteration of the steps 1705-1715.

[000129]In various embodiments, the method 1700 illustrated in FIG. 17 may include more or fewer than the steps 1705-1715 illustrated in FIG. 17 and described above. In some embodiments, the steps 1705-1715 of the method 1700 illustrated in FIG. 17 may be performed in a different order than the order illustrated in FIG. 17 and described above. In some embodiments, some of the steps 1705-1715 of the method 1700 illustrated in FIG. 17 may be performed in parallel or substantially simultaneously. For example, step 1715 may be

performed in parallel with steps 1705 and 1710. In various embodiments, one or more of the steps 1705-1715 may be performed more than once in the method 1700 illustrated in FIG. 17.

[000130] FIG. 18 illustrates the method 1700, in accordance with another embodiment of the present invention. In this embodiment, the step 1715 is performed in parallel with steps 1705 and 1710. In various embodiments, the sequence of steps 1705 and 1710 is an iteration of a loop in the method 1700. Moreover, the method 1700 may include more than one iteration of the loop including the steps 1705 and 1710. Furthermore, the step 1715 is an iteration of a loop in the method 1700, and the method 1700 may include more than one iteration of the loop including the step 1715. Because the step 1715 is performed in parallel with the steps 1705 and 1710, the overall loop time is decreased in the method 1700 of FIG. 18 in comparison to the method 1700 of FIG. 17. As a result, the method of the FIG. 18 may control generation of interrupts in the host processing unit 110 more precisely than the method of FIG. 17.

[000131] FIG. 19 illustrates a portion of the method 1700 of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention. The portion of the method 1700 illustrated in FIG. 19 illustrates embodiments of the step 1705 illustrated in FIG. 17 and FIG. 18.

[000132] In step 1905, a completion queue state is selected. In various embodiments, the interrupt manager 1040 selects a completion queue state 1115. For example, the interrupt manager 1040 may select a completion queue state 1115 for processing based on a predetermined selection order. The portion of the method 1700 then proceeds to step 1910.

[000133] In step 1910, the interrupt vector state associated with the completion queue state is identified. In various embodiments, the interrupt manager 1040 identifies the interrupt vector state 1125 associated with the completion queue state 1115 (i.e., the selected completion queue state). For example, the interrupt manager 1040 may identify the interrupt vector state 1125 associated with the completion queue state 1115 based on the interrupt vector identifier 1500 in the configuration register 1120 associated with the completion queue state 1115. The portion of the method 1700 then proceeds to step 1915.

[000134] In step 1915, it is determined whether the completion queue associated with the completion queue state is empty. In various embodiments, the interrupt manager 1040 determines whether the completion queue 525 associated with the completion queue state 1115 is empty. In various embodiments, the interrupt manager 1040 determines whether the completion queue 525 associated with the completion queue state 1115 is empty based on the completion queue head pointer 1025 and the completion queue tail pointer 1030 of the completion queue 525, as is described more fully herein. If the completion queue 525 associated with the completion queue state 1115 is empty, the portion of the method 1700 proceeds to step 1935. Otherwise, the portion of the method 1700 proceeds to step 1920.

[000135] In step 1920, arrived at from the determination in step 1915 that the completion queue is not empty, the event count of the completion queue state is added to the aggregate event count of the interrupt vector state. In various embodiments, the interrupt manager 1040 adds the event count 1210 of the completion queue state 1115 to the aggregate event count 1320 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 1925.

[000136] In step 1925, the empty queue indicator of the interrupt vector state 1125 is cleared.

In various embodiments, the interrupt manager 1040 clears the empty queue indicator 1310 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 1930.

[000137] In step 1930, it is determined whether the doorbell update status of the completion queue state is set. In various embodiments, the interrupt manager 1040 determines whether the doorbell update status 1205 of the completion queue state 1115 is set. If the doorbell update status 1205 of the completion queue state 1115 is set, the portion of the method 1700 proceeds to step 1940. Otherwise, the portion of the method 1700 proceeds to step 1935.

[000138] In step 1935, arrived at from the determination in step 1915 that the completion queue associated with the completion queue state is empty or the determination in step 1930 that the doorbell update status of the completion queue state is not set, the aggregate doorbell update status of the interrupt vector state 1125 is cleared. In various embodiments, the interrupt manager 1040 clears the aggregate doorbell update status 1315 of the interrupt vector state 1125. For example, the interrupt manager 1040 may clear the aggregate doorbell update status 1315 of the interrupt vector state 1125 by setting the aggregate doorbell update status 1315 to a value of zero. The portion of the method 1700 then proceeds to step 1940.

[000139] In step 1940, the completion queue event indicators 1200 are cleared in the completion queue state. In various embodiments, the interrupt manager 1040 clears the completion queue event indicators 1200 in the completion queue state 1115. For example, the interrupt manager 1040 may clear the doorbell update status 1205 and the event count 1210 in the completion queue state 1115. The portion of the method 1700 then proceeds to step 1945.

[000140] In step 1945, it is determined whether an additional completion queue state is to be processed. In various embodiments, the interrupt manager 1040 determines whether an additional completion queue state 1115 is to be processed. If an additional completion queue state 1115 is to be processed, the portion of the method 1700 returns to step 1905. Otherwise, the portion of the method 1700 ends.

[000141] In various embodiments, the portion of the method 1700 illustrated in FIG. 19 may include more or fewer than the steps 1905-1945 illustrated in FIG. 19 and described above. In some embodiments, the steps 1905-1945 of the portion of the method 1700 illustrated in FIG. 19 may be performed in a different order than the order illustrated in FIG. 19 and described above. In some embodiments, some of the steps 1905-1945 of the portion of the method 1700 illustrated in FIG. 19 may be performed in parallel or substantially simultaneously. In various embodiments, one or more of the steps 1905-1945 may be performed more than once in the portion of the method 1700 illustrated in FIG. 19.

[000142] FIG. 20 illustrates a portion of the method 1700 of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention. The portion of the method 1700 illustrated in FIG. 19 illustrates embodiments of the step 1710 illustrated in FIG. 17 and FIG. 18.

[000143] In step 2005, an interrupt vector state 1125 is selected. In various embodiments, the interrupt manager 1040 selects an interrupt vector state 1125. For example, the interrupt manager 1040 may select an interrupt vector state 1125 for processing based on a predetermined selection order. The portion of the method 1700 then proceeds to step 2010.

[000144]In step 2010, it is determined whether the empty queue indicator is set. In various embodiments, the interrupt manager 1040 determines whether the empty queue indicator 1310 of the interrupt vector state 1125 is set. If the empty queue indicator 1310 is set, the portion of the method 1700 proceeds to step 2040. Otherwise, the portion of the method 1700 proceeds to step 2015.

[000145]In step 2015, arrived at from the determination in step 2010 that the empty queue indicator is not set, it is determined whether the timer active indicator in the aggregated time indicator of the interrupt vector state is set. In various embodiments, the interrupt manager 1040 determines whether the timer active indicator 1410 in the aggregate time indicator 1325 of the interrupt vector state 1125 is set. If the timer active indicator 1410 is set, the portion of the method 1700 proceeds to step 2030. Otherwise, the portion of the method 1700 proceeds to step 2020.

[000146]In step 2020, arrived at from the determination in step 2015 that the timer active indicator 1410 is not set, the timer active indicator 2020 is set. In various embodiments, the interrupt manager 1040 sets the timer active indicator 1410 of the aggregate time indicator 1325 of the interrupt vector state 1125 to indicate the aggregate time indicator 1325 is active. The portion of the method 1700 then proceeds to step 2025.

[000147]In step 2025, the interrupt status of the interrupt vector state is set. In various embodiments, the interrupt manager 1040 sets the interrupt status 1330 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2035.

[000148] In step 2030, arrived at from the determination in step 2015 that the timer active indicator is set, it is determined whether the aggregate doorbell update status of the interrupt vector state is set. In various embodiments, the interrupt manager 1040 determines whether the aggregate doorbell update status 1315 of the interrupt vector state 1125 is set. If the aggregate doorbell update status 1315 is set, the portion of the method 1700 proceeds to step 2035. Otherwise, the portion of the method 1700 proceeds to step 2055.

[000149] In step 2035, arrived at from the determination in step 2030 that the aggregate doorbell update status is set, the time stamp of the aggregate time indicator 1325 is updated. In various embodiments, the interrupt manager 1040 updates the time stamp 1405 of the aggregate time indicator 1325 in the interrupt vector state 1125 by setting the time stamp 1405 to the value of a timer (e.g., a global timer) in the nonvolatile memory controller 105. The portion of the method 1700 then proceeds to step 2075.

[000150] In step 2040, arrived at from the determination in step 2010 that the empty queue indicator is set, the aggregate event count is cleared. In various embodiments, the interrupt manager 1040 clears the aggregate event count 1320 in the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2045.

[000151] In step 2045, the timer active indicator is cleared. In various embodiments, the interrupt manager 1040 clears the timer active indicator 1410 in the aggregate time indicator 1325 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2050.

[000152]In step 2050, the interrupt status of the interrupt vector state is cleared. In various embodiments, the interrupt manager 1040 clears the interrupt status 1330 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2085.

[000153]In step 2055, arrived at from the determination in step 2030 that the aggregate doorbell update status is not set, the aggregate time counter is updated. In various embodiments, the interrupt manager 1040 updates the aggregate time counter 1400 in the aggregate time indicator 1325 of the interrupt vector state 1125. For example, the interrupt manager 1040 may compute a difference between the time stamp 1405 in the aggregate time indicator 1325 and a timer in the nonvolatile memory controller 105 (e.g., the global timer), and add the result to the aggregate time counter 1400. The portion of the method 1700 then proceeds to step 2060.

[000154]In step 2060, the time stamp of the aggregate time indicator 1325 is updated. In various embodiments, the interrupt manager 1040 updates the time stamp 1405 of the aggregate time indicator 1325 in the interrupt vector state 1125 by setting the time stamp 1405 to the value of a timer (e.g., a global timer) in the nonvolatile memory controller 105. The portion of the method 1700 then proceeds to step 2065.

[000155]In step 2065, it is determined whether the time aggregation threshold is reached. In various embodiments, the interrupt manager 1040 determines whether the aggregate time counter 1400 has reached an aggregate time threshold. For example, the interrupt manager 1040 may determine whether the aggregate time counter 1400 has reached the time aggregation threshold 1620 in the configuration register 1130 associated with the interrupt vector state 1125. If the aggregate time counter 1400 has reached the time aggregation

threshold 1620, the portion of the method 1700 proceeds to step 2070. Otherwise, the portion of the method 1700 proceeds to step 2080.

[000156] In step 2070, arrived at from the determination in step 2065 that the time aggregation threshold is reached, the interrupt status of the interrupt vector state 1125 is set. In various embodiments, the interrupt manager 1040 sets the interrupt status 1330 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2075.

[000157] In step 2075, arrived at from step 2035 in which the time stamp is updated or from step 2070 in which the interrupt status is set, the aggregate time counter is cleared. In various embodiments, the interrupt manager 1040 clears the aggregate time counter 1400 in the aggregate time indicator 1325 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2080.

[000158] In step 2080, arrived at from step 2065 in which it is determined that the aggregate time threshold is not reached or from step 2075 in which the aggregate time counter is cleared, the empty queue indicator of the interrupt vector state 1125 is set. In various embodiments, the interrupt manager 1040 sets the empty queue indicator 1310 of the interrupt vector state 1125. In this way, the interrupt manager 1040 initializes the empty queue indicator 1310. The portion of the method 1700 then proceeds to step 2085.

[000159] In step 2085, arrived at from step 2050 in which the interrupt status is cleared or from step 2080 in which the empty queue indicator is set, the aggregate doorbell update status of the interrupt vector state 1125 is set. In various embodiments, the interrupt manager 1040 sets the aggregate doorbell update status 1315 of the interrupt vector state 1125. In this way, the

interrupt manager 1040 initializes the aggregate doorbell update status 1315. The portion of the method 1700 then proceeds to step 2090.

[000160] In step 2090, it is determined whether an additional interrupt vector state is to be processed. In various embodiments, the interrupt manager 1040 determines whether an additional interrupt vector state 1125 is to be processed. If an additional interrupt vector state 1125 is to be processed, the portion of the method 1700 returns to step 2005. Otherwise, the portion of the method 1700 ends.

[000161] In various embodiments, the portion of the method 1700 illustrated in FIG. 20 may include more or fewer than the steps 2005-2090 illustrated in FIG. 20 and described above. In some embodiments, the steps 2005-2090 of the portion of the method 1700 illustrated in FIG. 20 may be performed in a different order than the order illustrated in FIG. 20 and described above. In some embodiments, some of the steps 2005-2090 of the portion of the method 1700 illustrated in FIG. 20 may be performed in parallel or substantially simultaneously. In various embodiments, one or more of the steps 2005-2090 may be performed more than once in the portion of the method 1700 illustrated in FIG. 20.

[000162] FIG. 21 illustrates a portion of the method 1700 of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention. The portion of the method 1700 illustrated in FIG. 21 illustrates embodiments of the step 1710 illustrated in FIG. 17 and FIG. 18.

[000163] In step 2105, an interrupt vector state 1125 is selected. In various embodiments, the interrupt manager 1040 selects an interrupt vector state 1125. For example, the interrupt

manager 1040 may select an interrupt vector state 1125 for processing based on a predetermined selection order. The portion of the method 1700 then proceeds to step 2110.

[000164] In step 2110, it is determined whether the empty queue indicator is set. In various embodiments, the interrupt manager 1040 determines whether the empty queue indicator 1310 of the interrupt vector state 1125 is set. If the empty queue indicator 1310 is set, the portion of the method 1700 proceeds to step 2135. Otherwise, the portion of the method 1700 proceeds to step 2115.

[000165] In step 2115, arrived at from the determination in step 2110 that the empty queue indicator is not set, it is determined whether the event aggregation threshold is reached. In various embodiments, the interrupt manager 1040 determines whether the aggregate event count 1320 has reached an event aggregation threshold. For example, the interrupt manager 1040 may determine whether the aggregate event count 1320 has reached the event aggregation threshold 1610 in the configuration register 1130 associated with the interrupt vector state 1125. If the aggregate event count 1320 has reached the event aggregation threshold 1610, the portion of the method 1700 proceeds to step 2120. Otherwise, the portion of the method 1700 proceeds to step 2130.

[000166] In step 2120, arrived at from the determination in step 2115 that the event aggregation threshold is reached, the interrupt status is set. In various embodiments, the interrupt manager 1040 sets the interrupt status 1330 of the interrupt vector state 1125 to indicate the interrupt status 1330 is pending. For example, the interrupt manager 1040 may set the interrupt status 1330 of the interrupt vector state 1125 to the pending state. The portion of the method 1700 then proceeds to step 2125.

[000167]In step 2125, the aggregate event count is cleared. In various embodiments, the interrupt manager 1040 clears the aggregate event count 1320 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2130.

[000168]In step 2135, arrived at from the determination in step 2110 that the empty queue indicator is set, the aggregate event count is cleared. In various embodiments, the interrupt manager 1040 clears the aggregate event count 1320 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2140.

[000169]In step 2140, the interrupt status of the interrupt vector state is cleared. In various embodiments, the interrupt manager 1040 clears the interrupt status 1330 of the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2130.

[000170]In step 2130, arrived at from the determination in step 2115 that the event aggregation threshold is not reached, step 2125 in which the aggregate event count is cleared, or step 2140 in which the interrupt status is cleared, the empty queue indicator of the interrupt vector state 1125 is set. In various embodiments, the interrupt manager 1040 sets the empty queue indicator 1310 of the interrupt vector state 1125. In this way, the interrupt manager 1040 initializes the empty queue indicator 1310. The portion of the method 1700 then proceeds to step 2145.

[000171]In step 2145, it is determined whether an additional interrupt vector state is to be processed. In various embodiments, the interrupt manager 1040 determines whether an additional interrupt vector state 1125 is to be processed. If an additional interrupt vector state

1125 is to be processed, the portion of the method 1700 returns to step 2105. Otherwise, the portion of the method 1700 ends.

[000172]In various embodiments, the portion of the method 1700 illustrated in FIG. 21 may include more or fewer than the steps 2105-2145 illustrated in FIG. 21 and described above. In some embodiments, the steps 2105-2145 of the portion of the method 1700 illustrated in FIG. 21 may be performed in a different order than the order illustrated in FIG. 21 and described above. In some embodiments, some of the steps 2105-2145 of the portion of the method 1700 illustrated in FIG. 21 may be performed in parallel or substantially simultaneously. In various embodiments, one or more of the steps 2105-2145 may be performed more than once in the portion of the method 1700 illustrated in FIG. 21.

[000173]In various embodiments, the portion of the method 1700 illustrated in FIG. 20 and the portion of the method 1700 illustrated in FIG. 21 are performed substantially simultaneously (e.g., in parallel) in the method 1700. In these embodiments, the interrupt manager 1040 performs time based aggregation and completion queue event based aggregation for determining whether to generate an interrupt message packet for a completion queue 525 associated with an interrupt vector state 1125.

[000174]FIG. 22 illustrates a portion of the method 1700 of alerting a host processing unit of an unprocessed completion status, in accordance with an embodiment of the present invention. The portion of the method 1700 illustrated in FIG. 20 illustrates embodiments of the step 1715 illustrated in FIG. 17 and FIG. 18.

[000175]In step 2205, an interrupt vector state is selected. In various embodiments, the interrupt manager 1040 selects the interrupt vector state 1125. For example, the interrupt manager 1040 may select a completion queue state 1115 for processing based on a predetermined selection order. The portion of the method 1700 then proceeds to step 2210.

[000176]In step 2210, it is determined whether the interrupt status of the interrupt vector state is set. In various embodiments, the interrupt manager 1040 in the host controller interface 120 of the nonvolatile memory controller 105 determines whether the interrupt status 1330 is set in the interrupt vector state 1125 (i.e., the selected interrupt vector state 1125). For example, the interrupt manager 1040 may determine the interrupt status 1330 of the interrupt vector state 1125 is set by determining the interrupt status 1330 is in the pending state. In this way, the interrupt manager 1040 determines whether the completion queue 525 in the host processing unit 110 associated with the interrupt vector state 1125 contains one or more unprocessed completion statuses. If the interrupt status 1330 of the interrupt vector state 1125 is set, the portion of the method 1700 proceeds to step 2215. Otherwise, the portion of the method 1700 proceeds to step 2230.

[000177]In step 2215, arrived at from the determination in step 2210 that the interrupt status of the interrupt vector state is set, an interrupt message packet is generated for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue. In various embodiments, the interrupt manager 1040 generates the interrupt message packet for generating an interrupt in the host processing unit 110. The interrupt in the host processing unit 110 is associated with an interrupt vector in the host processing unit 110. Moreover, the interrupt vector is associated with the completion

queue 525 associated with the interrupt vector state 1125 in which the interrupt status 1330 is set. The portion of the method 1700 then proceeds to step 2220.

[000178] In step 2220, the interrupt message packet is sent to the host processing unit. In various embodiments, the interrupt manager 1040 sends the interrupt message packet to the host processing unit 110. In this way, the interrupt manager 1040 alerts the host processing unit 110 of the unprocessed completion status in the completion queue 525 associated with the interrupt. The portion of the method 1700 then proceeds to step 2225.

[000179] In step 2225, the interrupt status is cleared in the interrupt vector state 1125. In various embodiments, the interrupt manager 1040 clears the interrupt status 1330 in the interrupt vector state 1125. The portion of the method 1700 then proceeds to step 2330.

[000180] In step 2230, arrived at from the determination in step 2210 that the interrupt status is not set or from step 2225 in which the interrupt status is cleared, it is determined whether an additional interrupt vector state is to be processed. In various embodiments, the interrupt manager 1040 in the host controller interface 120 of the nonvolatile memory controller 105 determines whether an additional interrupt vector state 1125 is to be processed. If an additional interrupt vector state 1125 is to be processed, the portion of the method 1700 returns to step 2205. Otherwise, the portion of the method 1700 ends.

[000181] In various embodiments, the portion of the method 1700 illustrated in FIG. 22 may include more or fewer than the steps 2205-2230 illustrated in FIG. 22 and described above. In some embodiments, the steps 2205-2230 of the portion of the method 1700 illustrated in FIG. 22 may be performed in a different order than the order illustrated in FIG. 22 and described

above. In some embodiments, some of the steps 2205-2230 of the portion of the method 1700 illustrated in FIG. 22 may be performed in parallel or substantially simultaneously. In various embodiments, one or more of the steps 2205-2230 may be performed more than once in the portion of the method 1700 illustrated in FIG. 22.

[000182] Although the invention has been described with reference to particular embodiments thereof, it will be apparent to one of ordinary skill in the art that modifications to the described embodiment may be made without departing from the spirit of the invention. Accordingly, the scope of the invention will be defined by the attached claims not by the above detailed description.

CLAIMS

What is claimed is:

1. A nonvolatile memory controller for alerting a host processing unit to an unprocessed completion status contained in a completion queue of the host processing unit, the nonvolatile memory controller comprising:

an interrupt manager configured to generate a completion queue state for indicating the occurrence of a completion queue event associated with the completion queue, generate an interrupt vector state based on the completion queue state, determine the completion queue of the host processing unit plurality of completion queues contains an unprocessed completion status based on the interrupt vector state, and generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.

2. The nonvolatile memory controller of claim 1, wherein the interrupt is a hardware interrupt.

3. The nonvolatile memory controller of claim 1, wherein the interrupt message packet includes an interrupt vector associated with the completion queue for triggering the interrupt in the host processing unit.

4. The nonvolatile memory controller of claim 3, wherein the completion queue state includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.
5. The nonvolatile memory controller of claim 3, wherein completion queue state includes an event count indicating a number of completion message packets received by the host controller interface for the completion queue associated with the completion queue state.
6. The nonvolatile memory controller of claim 5, wherein the interrupt vector state includes an aggregate event count for aggregating event counts of the completion queue state over a plurality of update operations, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate event count is below an aggregate event count threshold.
7. The nonvolatile memory controller of claim 3, wherein the interrupt vector state includes an aggregate time indicator for indicating an aggregate time over update operations performed on the interrupt vector state, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate time indicator is below an aggregate time threshold.

8. The nonvolatile memory controller of claim 3, wherein the completion queue state includes an empty queue indicator for indicating whether the completion queue is empty, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the empty queue indicator indicates the completion queue is empty.

9. A nonvolatile memory controller comprising:

a completion queue state memory configured to store a plurality of completion queue states corresponding to a plurality of completion queues in a host processing unit;

an interrupt vector state memory configured to store a plurality of interrupt vector states corresponding to a plurality of interrupt vectors in the host processing unit; and

an interrupt manager controller coupled to the completion queue state memory and the interrupt vector state memory, the interrupt manager controller configured to map at least one completion queue state of the plurality of completion queue states to an interrupt vector state of the plurality of interrupt vector states, generate the interrupt vector state based on each completion queue state mapped to the interrupt vector state, determine a completion queue corresponding to a completion queue state mapped to the interrupt vector state contains an unprocessed completion status based on the interrupt vector state, and to generate an interrupt message packet based on the interrupt vector state for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.

10. The nonvolatile memory controller of claim 9, wherein the interrupt manager controller is configured to map at least two completion queue states of the plurality of completion queue states to the interrupt vector state.

11. The nonvolatile memory controller of claim 9, wherein the interrupt manager controller is a sequential logic circuit.

12. The nonvolatile memory controller of claim 9, wherein a completion queue state of the plurality of completion queue states includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.

13. The nonvolatile memory controller of claim 9, wherein a completion queue state of the plurality of completion queue states includes an event count indicating a number of completion message packets received by the host controller interface and including a completion status for the completion queue associated with the completion queue state.

14. The nonvolatile memory controller of claim 13, wherein the interrupt vector state includes an aggregate event count for aggregating event counts of the completion queue state over a plurality of update operations, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate event count is below an aggregate event count threshold.

15. The nonvolatile memory controller of claim 9, wherein the interrupt vector state includes an aggregate time indicator for indicating an aggregate time over update operations performed on the interrupt vector state, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate time indicator is below an aggregate time threshold.

16. The nonvolatile memory controller of claim 9, wherein a completion queue state of the plurality of completion queue states includes an empty queue indicator for indicating whether the completion queue is empty, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the empty queue indicator indicates the completion queue is empty.

17. A method comprising:
- generating a completion queue state by a nonvolatile memory controller for indicating the occurrence of a completion queue event associated with a completion queue in a host processing unit;
 - generating an interrupt vector state by the nonvolatile memory controller based on the completion queue state, the interrupt vector state associated with an interrupt vector in the host processing unit;
 - determining by the nonvolatile memory controller based on the interrupt vector state that the completion queue contains an unprocessed completion status; and
 - generating an interrupt message packet by the nonvolatile memory interface for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.
18. The method of claim 17, further comprising sending the interrupt message packet to the host processing unit.
19. The method of claim 17, wherein the completion queue event is the host processing unit updating a head pointer stored in the nonvolatile memory controller for the completion queue.
20. The method of claim 17, wherein the completion queue event is detecting a completion queue event flag set in a completion message packet containing a completion status.

ABSTRACT OF THE DISCLOSURE

[000183] A nonvolatile memory controller processes a nonvolatile memory command and generates a completion status for the nonvolatile memory command. The nonvolatile memory controller transmits the completion status to a host processing unit for storage in a completion queue of the host processing unit. An interrupt manager in the nonvolatile memory controller determines the completion queue contains an unprocessed completion status and generates an interrupt message packet. The nonvolatile memory controller transmits the interrupt message packet to the host processing unit for triggering an interrupt in the host processing unit and alerting the host processing unit to the unprocessed completion status.

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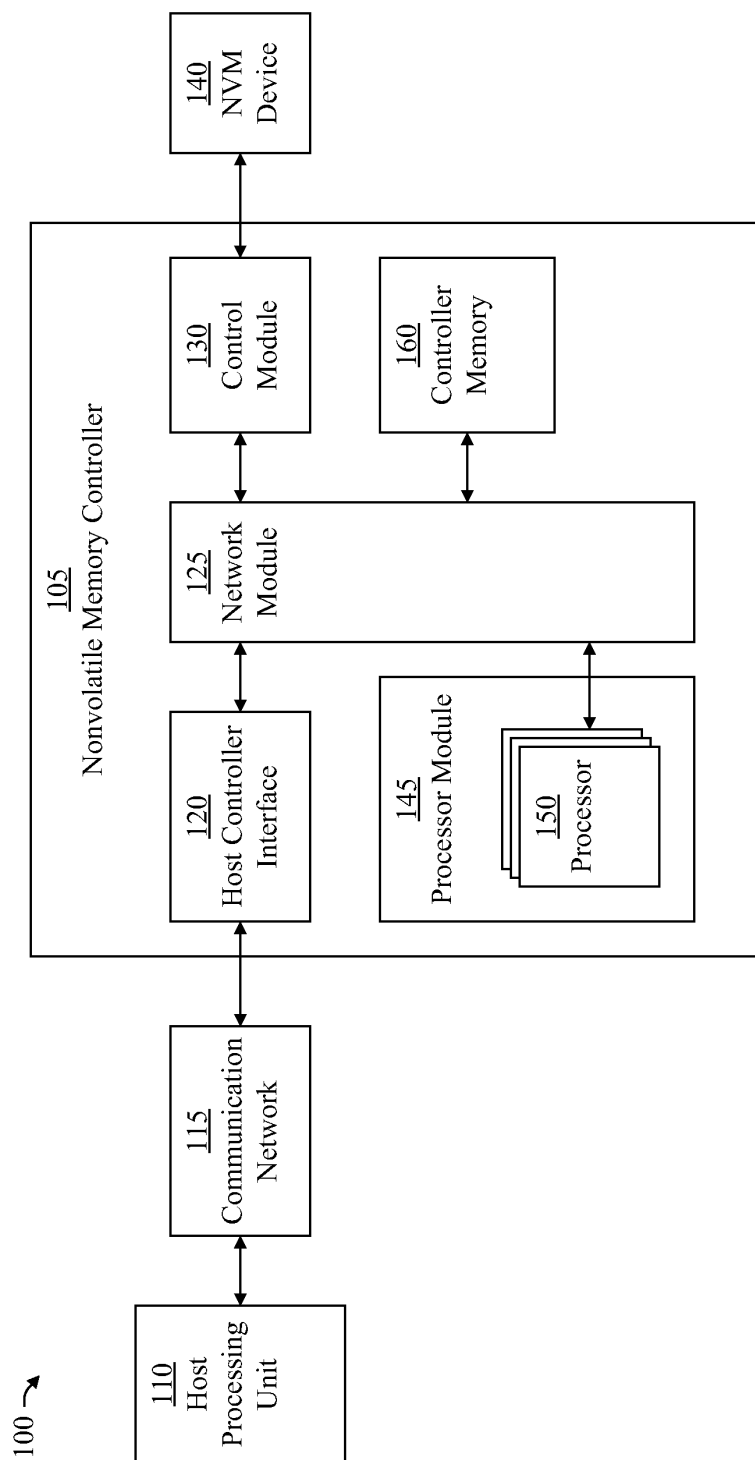


FIG. 1

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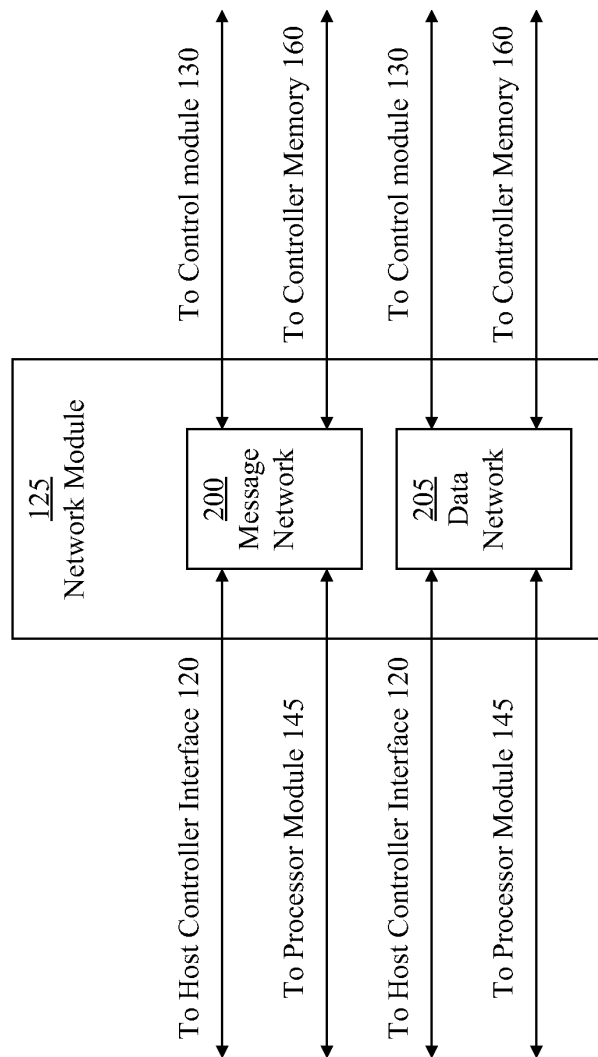


FIG. 2

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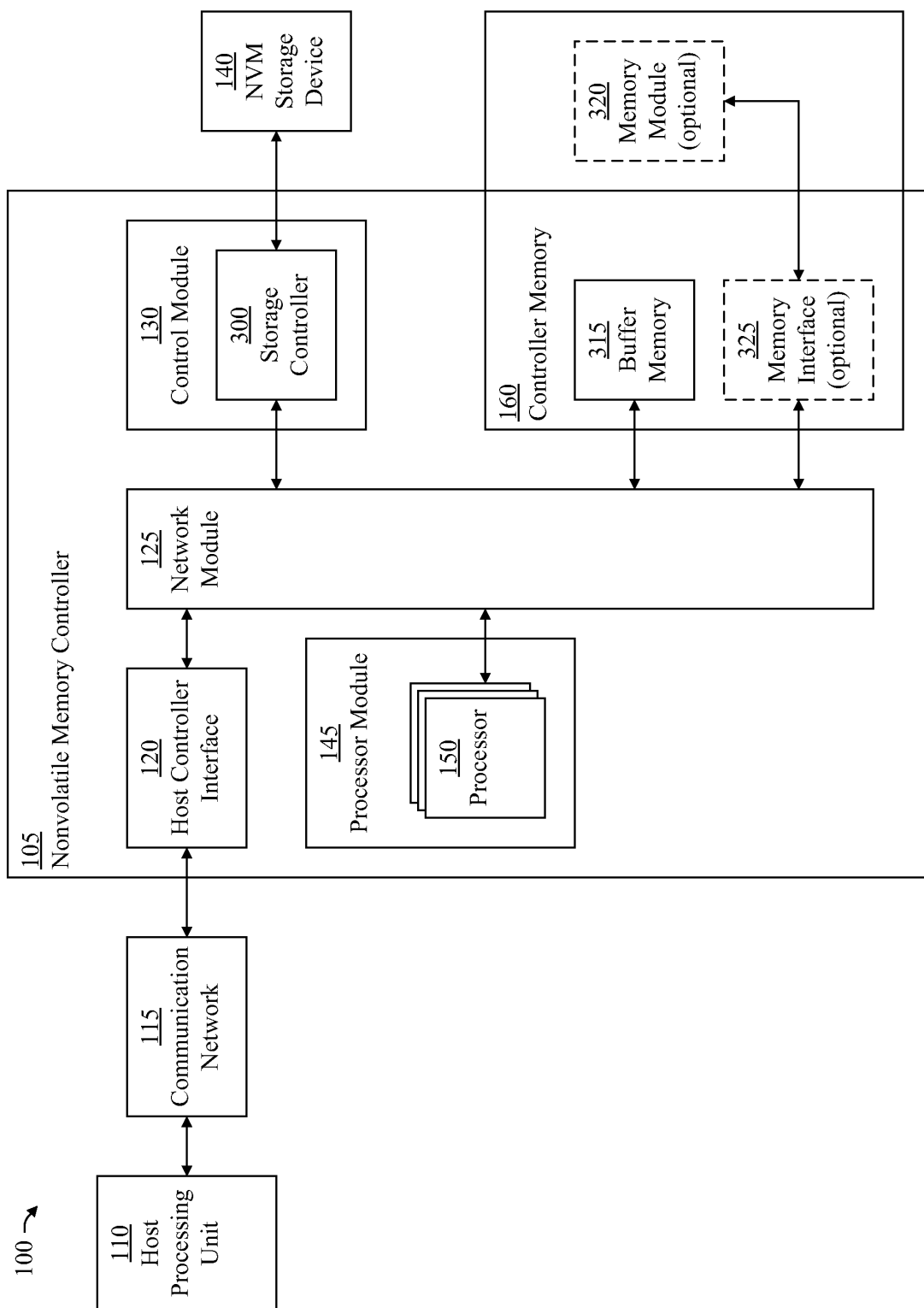


FIG. 3

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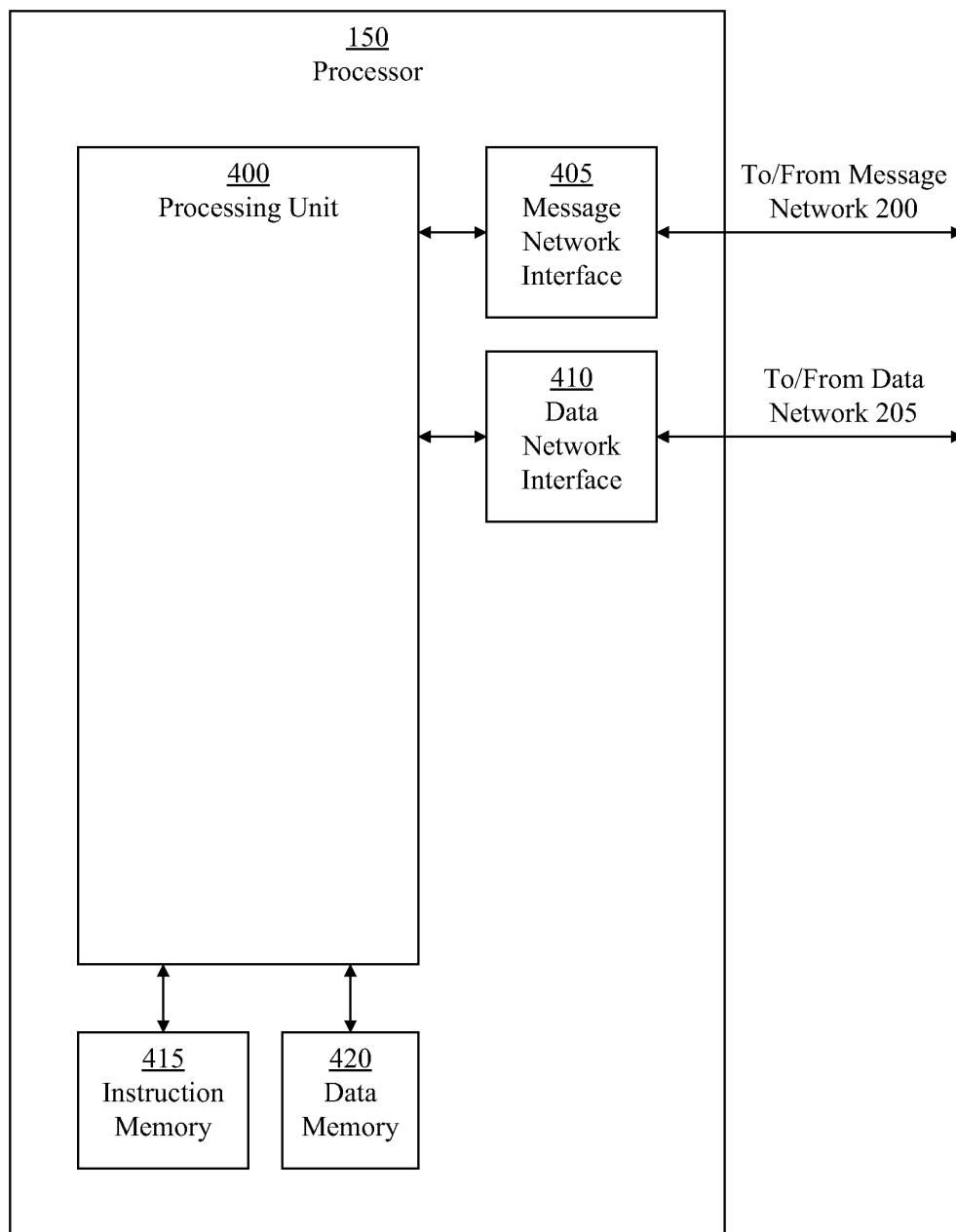


FIG. 4

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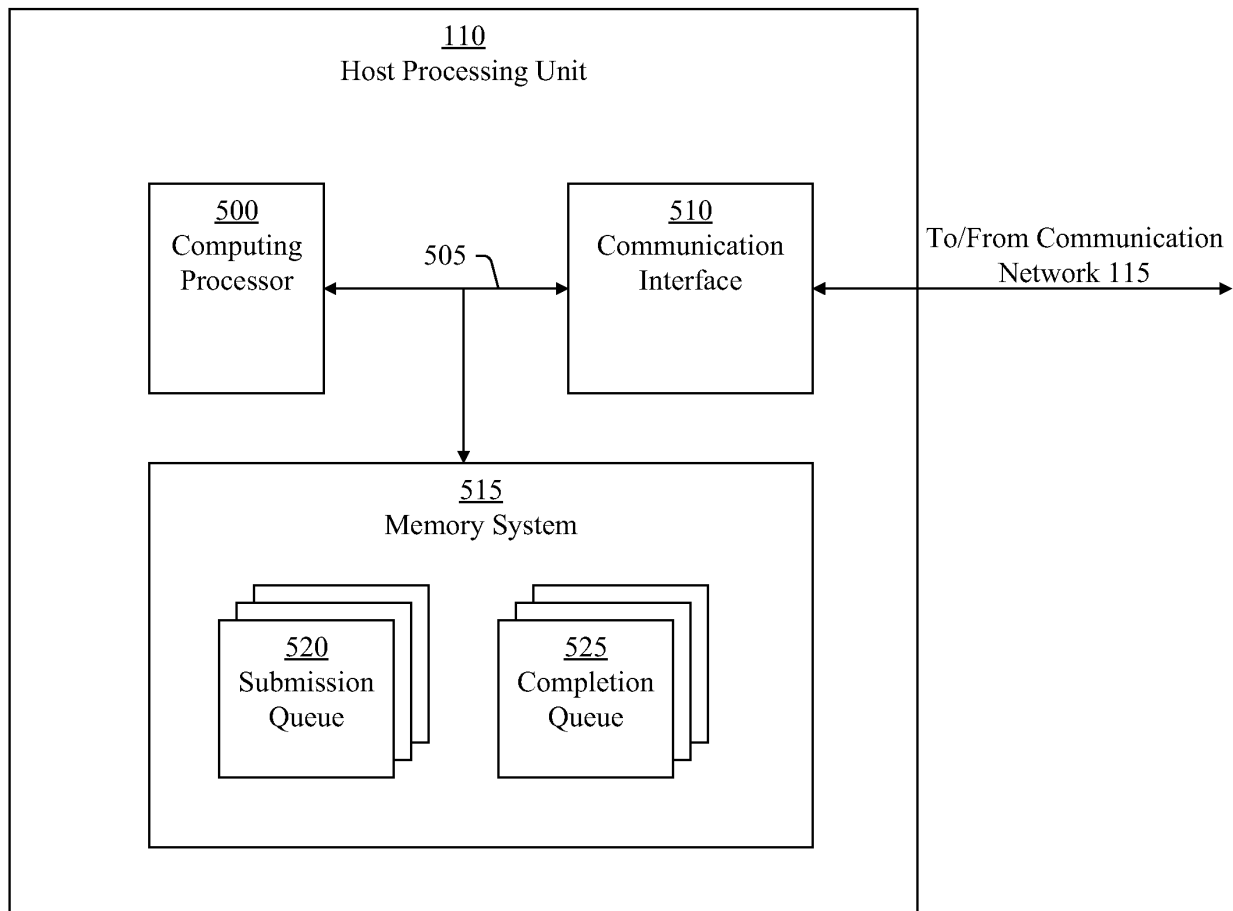


FIG. 5

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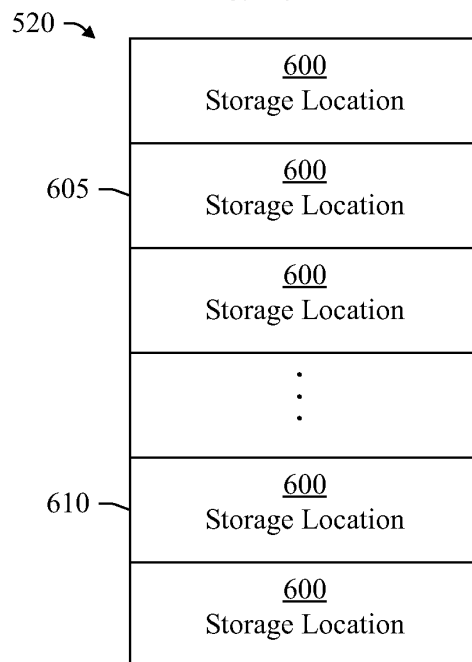


FIG. 6

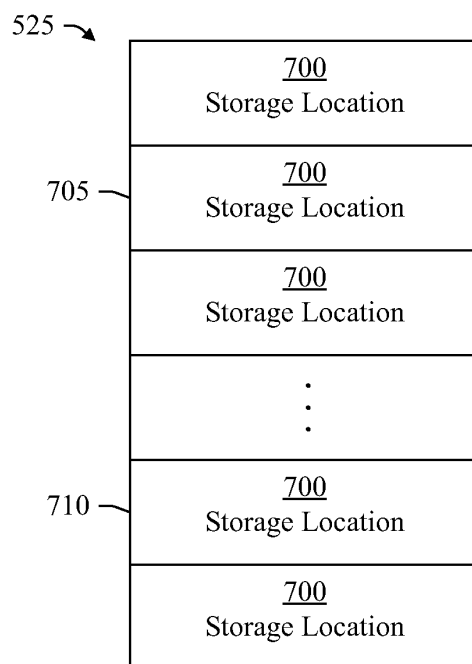


FIG. 7

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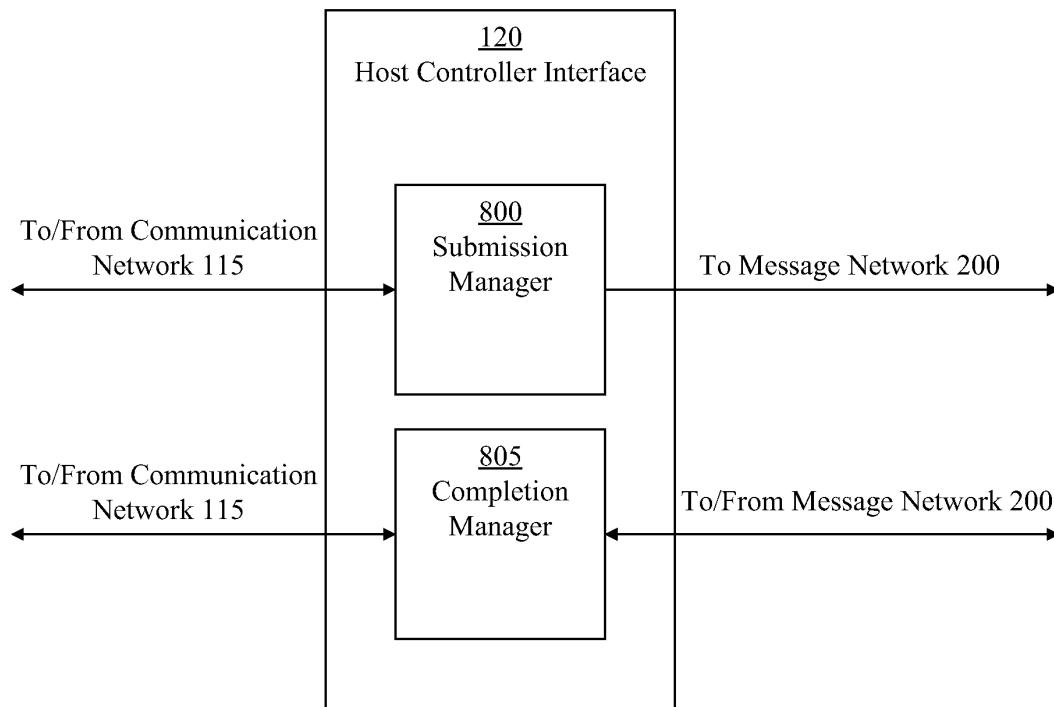


FIG. 8

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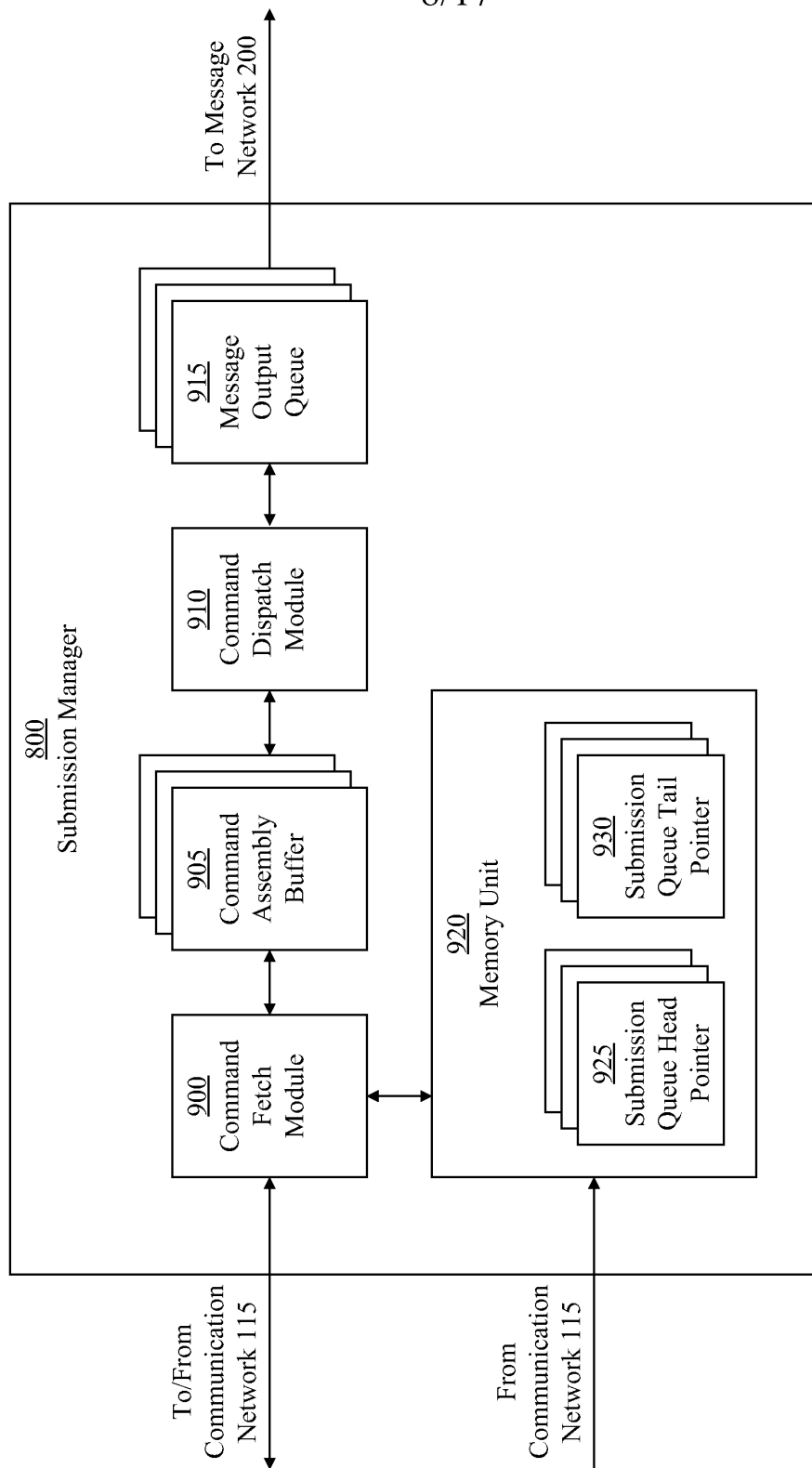


FIG. 9

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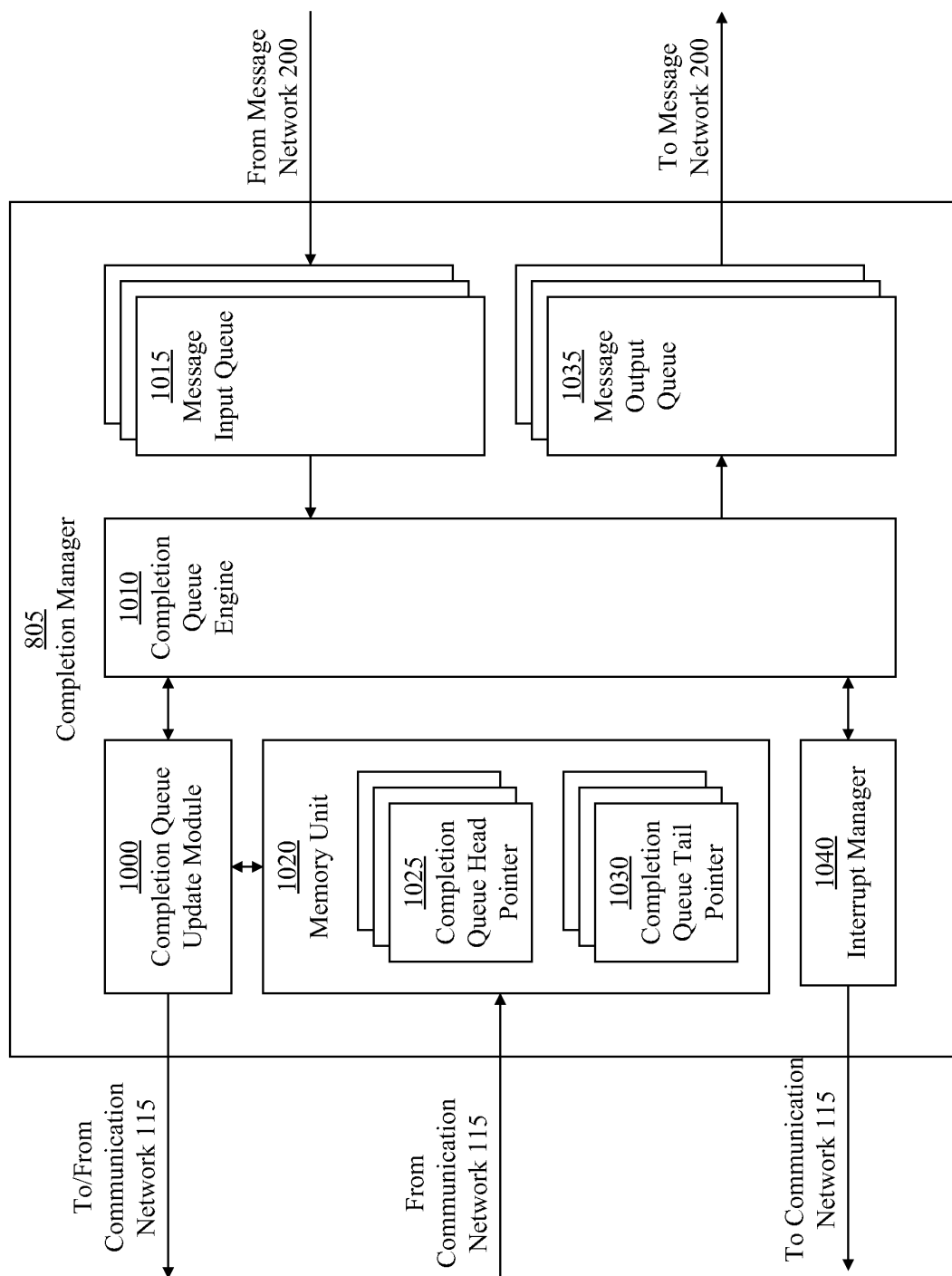


FIG. 10

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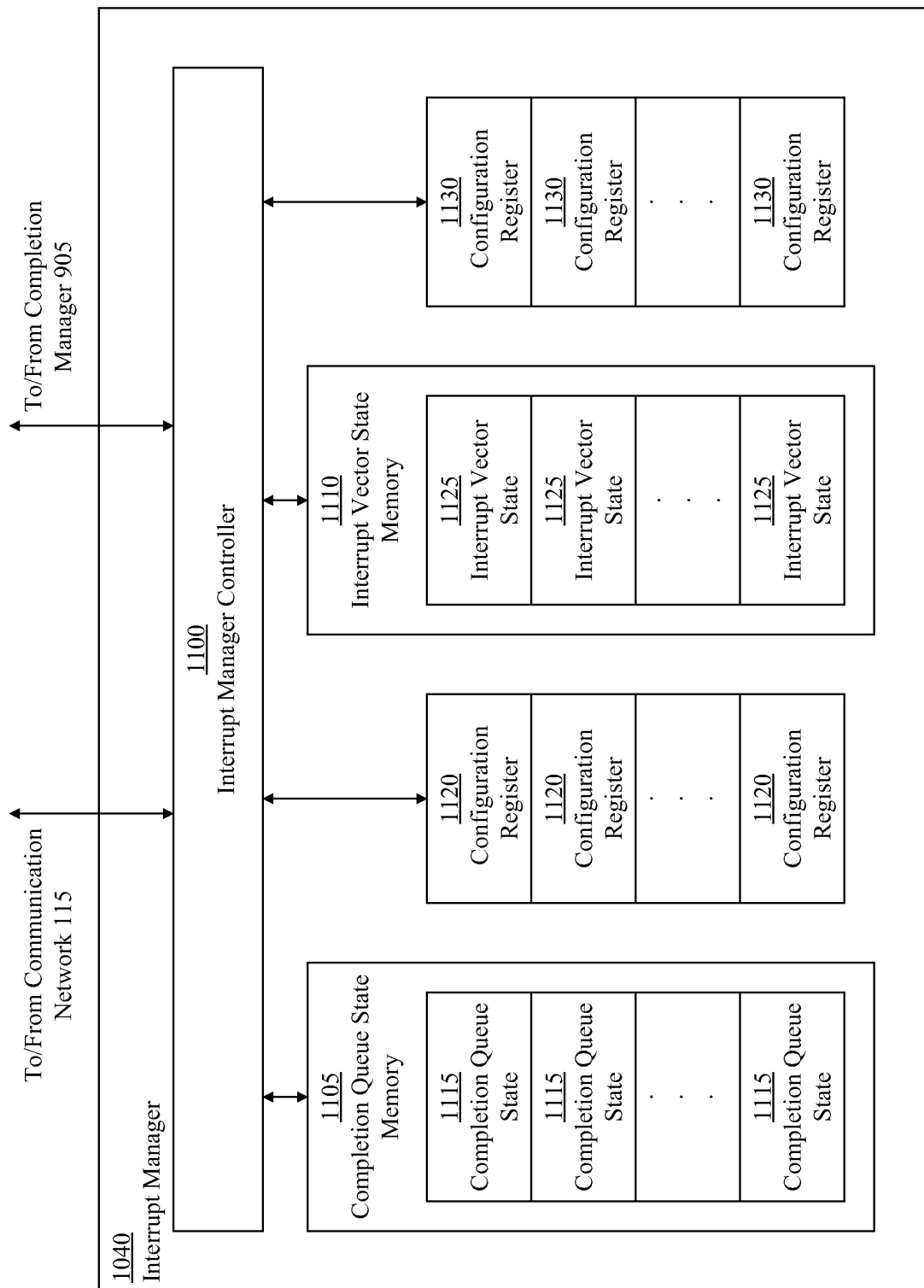


FIG. 11

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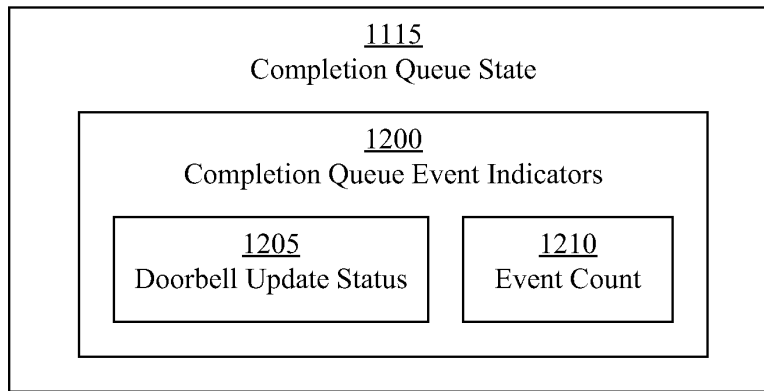


FIG. 12

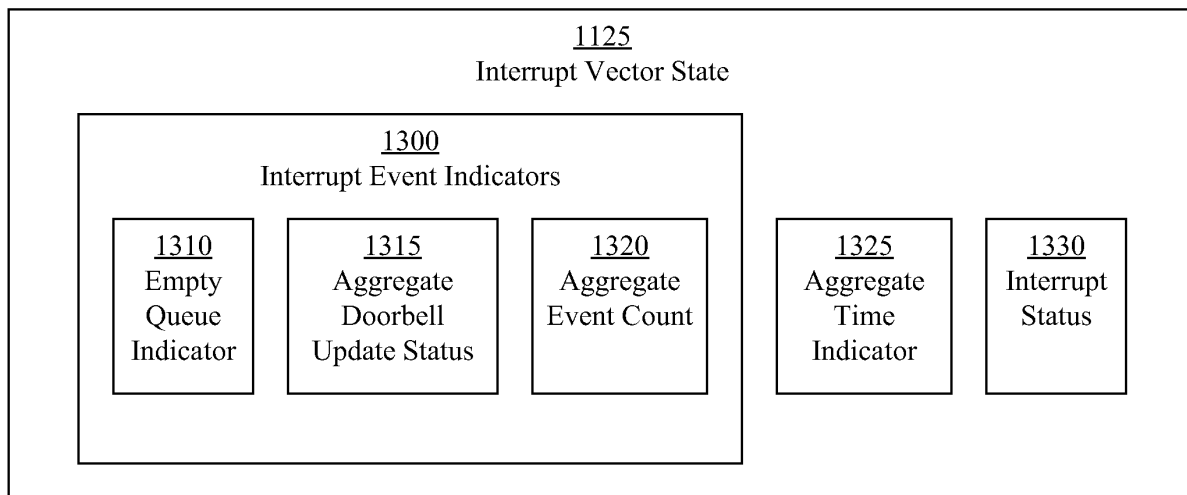


FIG. 13

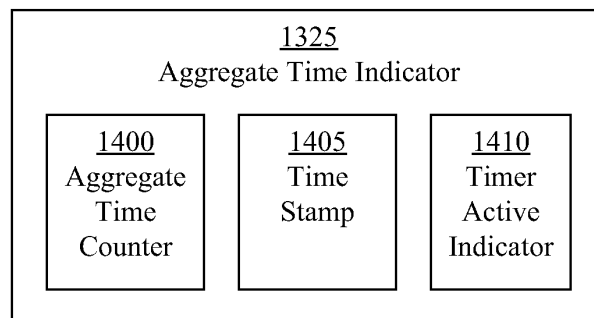


FIG. 14

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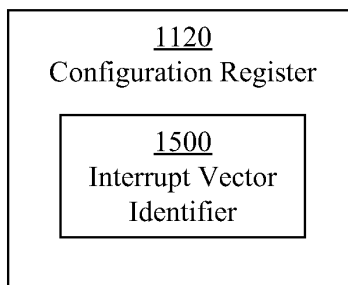


FIG. 15

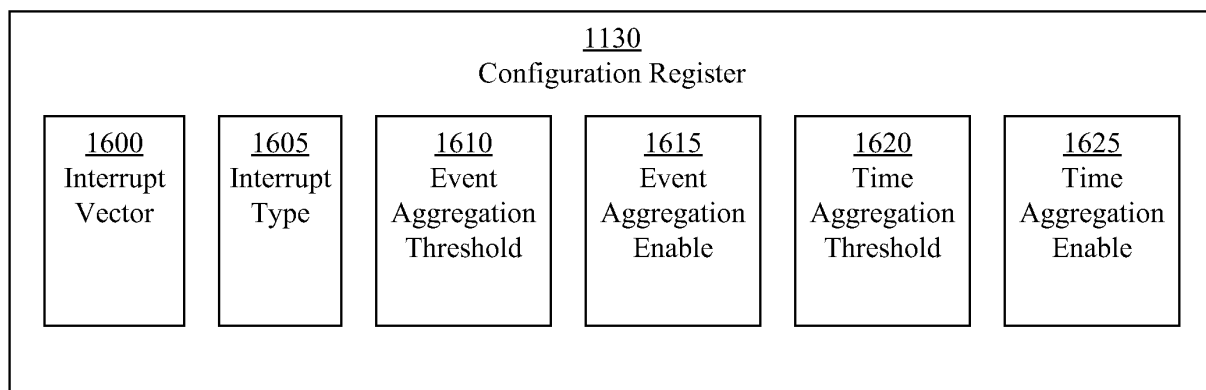


FIG. 16

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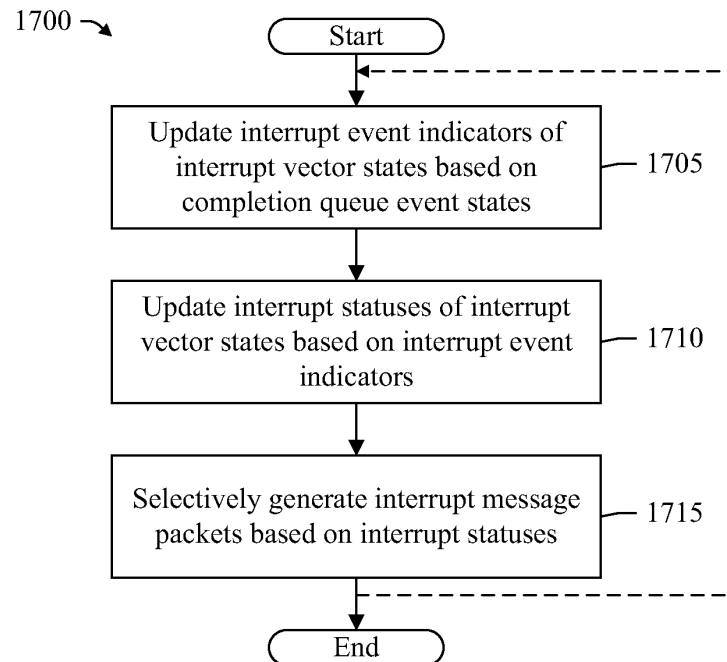


FIG. 17

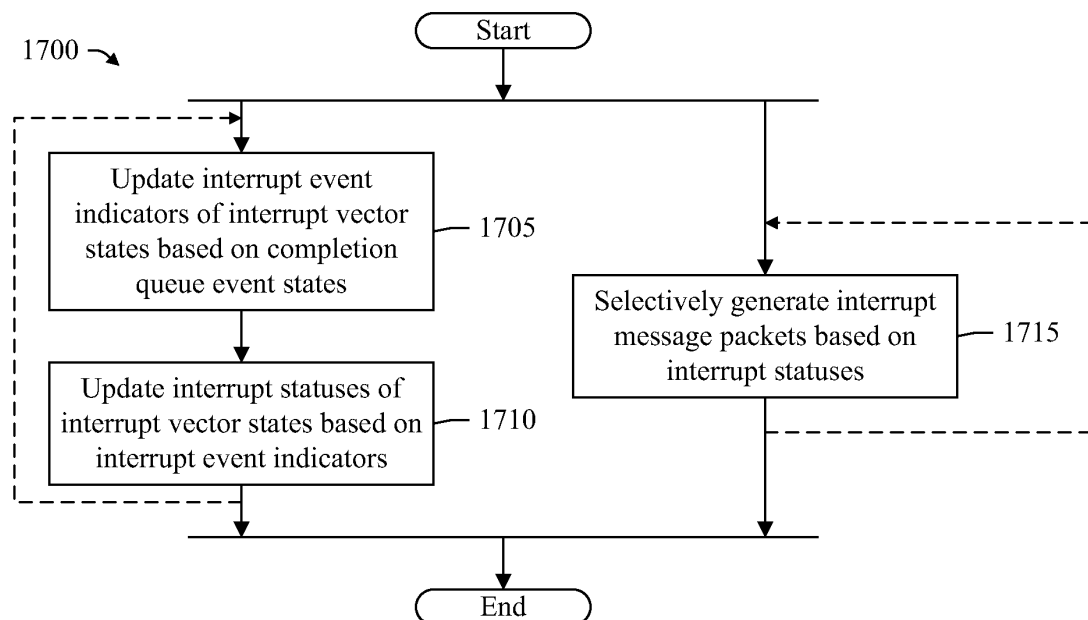
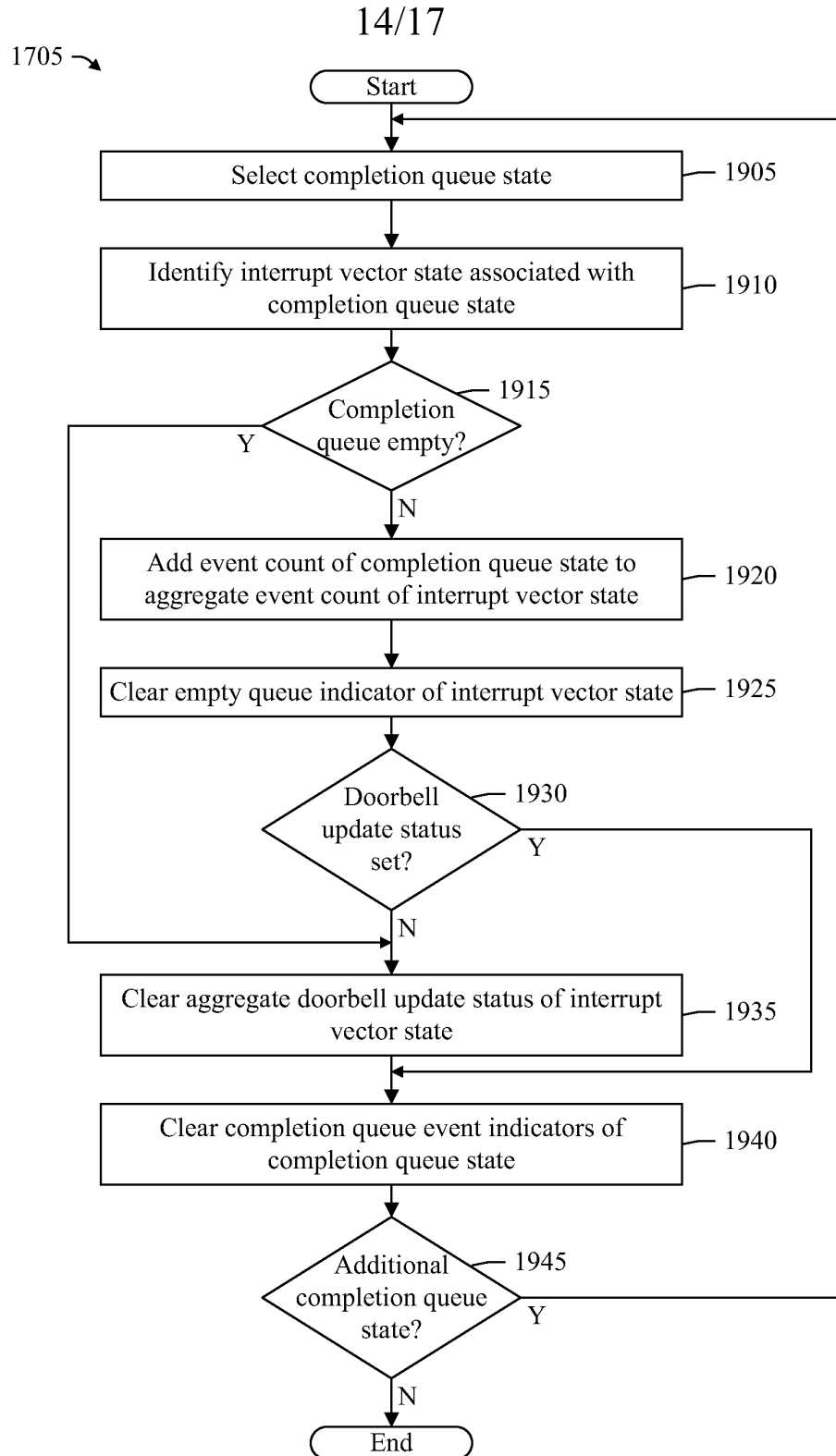


FIG. 18



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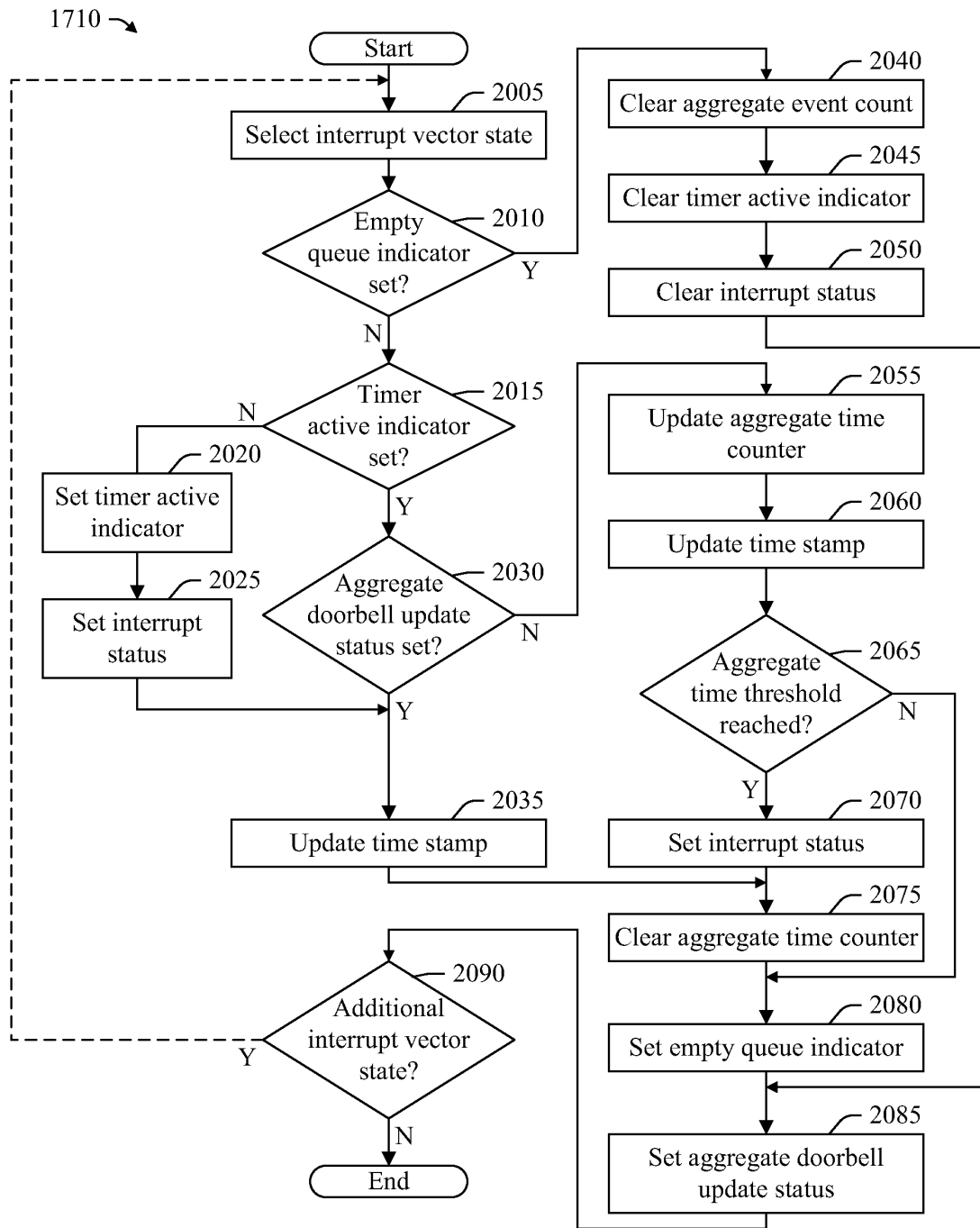


FIG. 20

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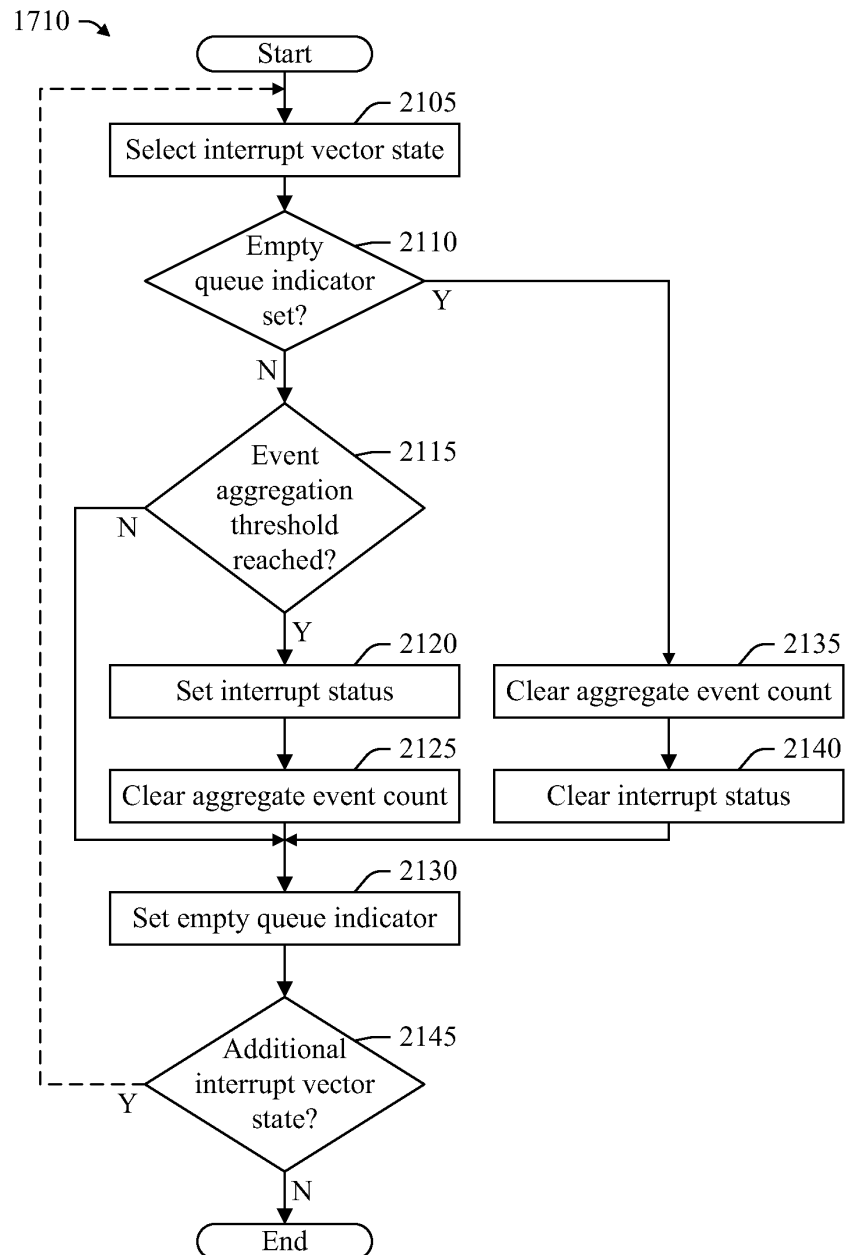


FIG. 21

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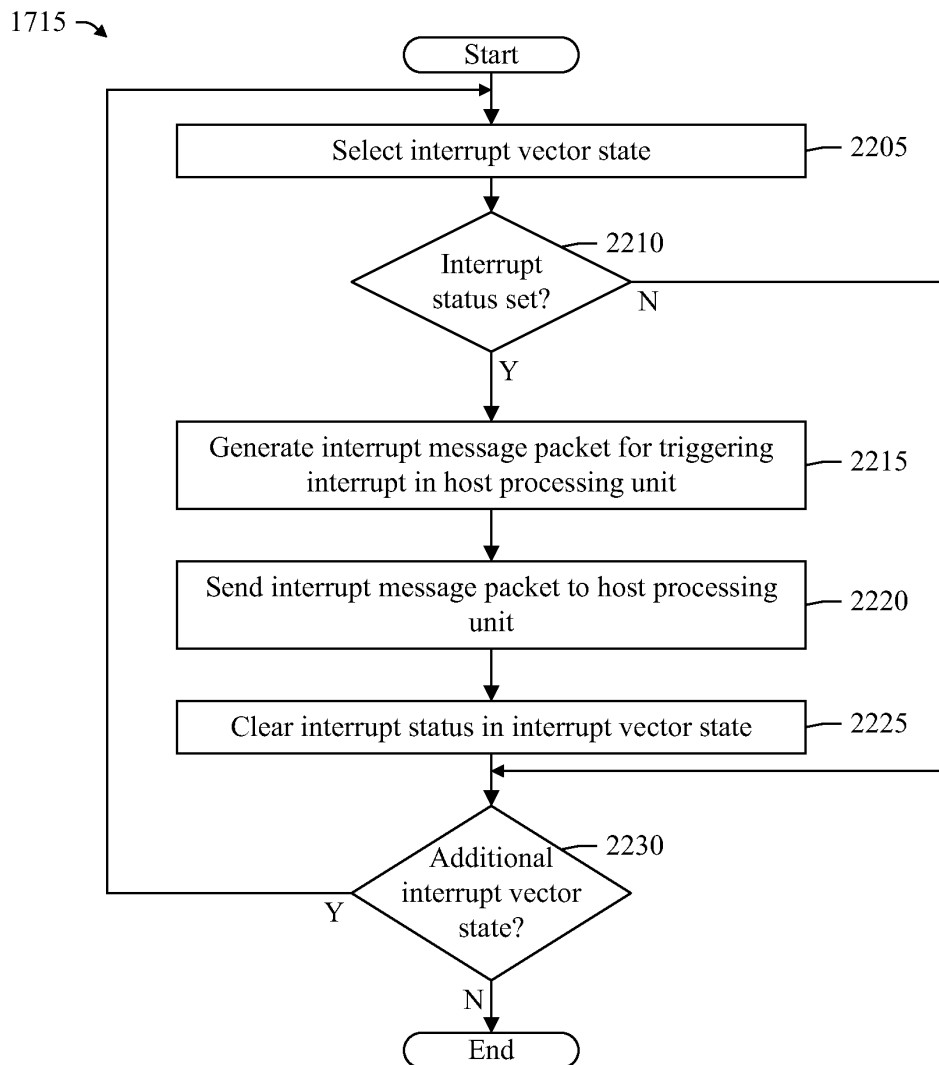


FIG. 22

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IDT-2730D-UT
		Application Number	
Title of Invention	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Peter	Z.	Onufryk		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Flanders	State/Province	NJ	Country of Residence i	US
Citizenship under 37 CFR 1.41(b) i		US			
Mailing Address of Applicant:					
Address 1		20 Saint Andrews Court			
Address 2					
City	Flanders	State/Province	NJ		
Postal Code	07836	Country i	US		
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jayesh		Patel		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	San Jose	State/Province	CA	Country of Residence i	US
Citizenship under 37 CFR 1.41(b) i		US			
Mailing Address of Applicant:					
Address 1		6157 Iowa Drive			
Address 2					
City	San Jose	State/Province	CA		
Postal Code	95123	Country i	US		
Applicant 3					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Ihab		Jaser		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	San Jose	State/Province	CA	Country of Residence i	US

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IDT-2730D-UT	
		Application Number		
Title of Invention	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER			
Citizenship under 37 CFR 1.41(b) i		US		
Mailing Address of Applicant:				
Address 1	2907 Mitton Dr.			
Address 2				
City	San Jose	State/Province	CA	
Postal Code	95148	Countryi	US	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence Information of this application.			
Customer Number	33087		
Email Address	glass@patentforce.com	Add Email	Remove Email

Application Information:

Title of the Invention	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER		
Attorney Docket Number	IDT-2730D-UT	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	17	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☒ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☐ Customer Number	☒ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number		IDT-2730D-UT	
		Application Number			
Title of Invention		INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER			

Prefix	Given Name	Middle Name	Family Name	Suffix	Remove
Mr.	Kenneth		Glass		
Registration Number		42587			
Prefix	Given Name	Middle Name	Family Name	Suffix	Remove
Mr.	Randall		Krause		
Registration Number		53158			
Prefix	Given Name	Middle Name	Family Name	Suffix	Remove
Mr.	Greg		Warder		
Registration Number		50208			
Prefix	Given Name	Middle Name	Family Name	Suffix	Remove
Mrs.	Jaya		Nair		
Registration Number		46454			
Prefix	Given Name	Middle Name	Family Name	Suffix	Remove
Mr.	Stanley	J.	Pawlik		
Registration Number		47850			
Additional Representative Information blocks may be generated within this form by selecting the Add button.					Add

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	61374242	2011-08-16
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☐ No
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	IDT-2730D-UT
		Application Number	
Title of Invention	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER		

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

If the Assignee is an Organization check here. ☒

Organization Name Integrated Device Technology, Inc.

Mailing Address Information:

Address 1 6024 Silver Creek Valley Road

Address 2

City San Jose

State/Province CA

Country ⁱ US

Postal Code 95138

Phone Number

Fax Number

Email Address

Additional Assignee Data may be generated within this form by selecting the Add button.

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Kenneth Glass/		Date (YYYY-MM-DD)	2011-03-21
First Name	Kenneth	Last Name	Glass	Registration Number
				42587

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER		
First Named Inventor/Applicant Name:		Peter Z. Onufryk		
Filer:		Kenneth Glass		
Attorney Docket Number:		IDT-2730D-UT		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1090

Electronic Acknowledgement Receipt	
EFS ID:	9698802
Application Number:	13052388
International Application Number:	
Confirmation Number:	6393
Title of Invention:	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730D-UT
Receipt Date:	21-MAR-2011
Filing Date:	
Time Stamp:	14:04:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1090
RAM confirmation Number	436
Deposit Account	501006
Authorized User	GLASS,KENNETH
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	2730D-Dec-n-POA.pdf	1201011	no	4
			974b9ca41420f57e6d16850628edf93e8280a730		
Warnings:					
Information:					
2		IDT-2730D-Specification-20110316-01f.pdf	193415	yes	68
			3d4b9d76f77b4efa61f96e9a836dc93de4865778		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	61	
	Claims		62	67	
	Abstract		68	68	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	IDT-2370D-Drawings-20110321-01.pdf	62877	no	17
			361d4221c65000aff16eab5cb4902335812c2a01		
Warnings:					
Information:					
4	Application Data Sheet	IDT-2730D--sb0014fs.pdf	1032027	no	5
			3ab09764bc423d243aa0134ca5640c6765d554fc		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	33002	no	2
			a2997ae9c88fdbc7032ec11e73d7d686123ee950		
Warnings:					
Information:					
Total Files Size (in bytes):			2522332		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	9698802
Application Number:	13052388
International Application Number:	
Confirmation Number:	6393
Title of Invention:	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730D-UT
Receipt Date:	21-MAR-2011
Filing Date:	
Time Stamp:	14:04:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1090
RAM confirmation Number	436
Deposit Account	501006
Authorized User	GLASS,KENNETH
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	2730D-Dec-n-POA.pdf	1201011	no	4
			974b9ca41420f57e6d16850628edf93e8280a730		
Warnings:					
Information:					
2		IDT-2730D-Specification-20110316-01f.pdf	193415	yes	68
			3d4b9d76f77b4efa61f96e9a836dc93de4865778		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	61	
	Claims		62	67	
	Abstract		68	68	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	IDT-2370D-Drawings-20110321-01.pdf	62877	no	17
			361d4221c65000aff16eab5cb4902335812c2a01		
Warnings:					
Information:					
4	Application Data Sheet	IDT-2730D--sb0014fs.pdf	1032027	no	5
			3ab09764bc423d243aa0134ca5640c6765d554fc		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	33002	no	2
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Warnings:					
Information:					
Total Files Size (in bytes):			2522332		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/052,388				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	540			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220			
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 52 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 220 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1090			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE				TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
					TOTAL ADD'L FEE				TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/052,388	03/21/2011	2182	1090	IDT-2730D-UT	20	3

CONFIRMATION NO. 6393

33087
GLASS & ASSOCIATES
P.O. BOX 1220
LOS GATOS, CA 95031-1220

FILING RECEIPT



Date Mailed: 04/01/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Peter Z. Onufryk, Flanders, NJ;
Jayesh Patel, San Jose, CA;
Ihab Jaser, San Jose, CA;

Assignment For Published Patent Application

INTEGRATED DEVICE TECHNOLOGY, INC., San Jose, CA

Power of Attorney:

Kenneth Glass--42587
Jaya Nair--46454
Stanley Pawlik--47850
Greg Warder--50208
Randall Krause--53158

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/374,242 08/16/2010

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 03/30/2011

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/052,388**

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

Title

INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER

Preliminary Class

710

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052388
	Filing Date		2011-03-21
	First Named Inventor	Peter Z. Onufryk	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		IDT-2730D-UT

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	7708195		2010-05-04	Yoshida et al.			
	2	7620784		2009-11-17	Panabaker, Ruston			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20100262979		2010-10-14	Borchers et al.			
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐
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NON-PATENT LITERATURE DOCUMENTS							Remove	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052388
	Filing Date		2011-03-21
	First Named Inventor	Peter Z. Onufryk	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		IDT-2730D-UT

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13052388
	Filing Date	2011-03-21
	First Named Inventor	Peter Z. Onufryk
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IDT-2730D-UT

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kenneth Glass/	Date (YYYY-MM-DD)	2013-01-29
Name/Print	Kenneth Glass	Registration Number	42587

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	14825016
Application Number:	13052388
International Application Number:	
Confirmation Number:	6393
Title of Invention:	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730D-UT
Receipt Date:	29-JAN-2013
Filing Date:	21-MAR-2011
Time Stamp:	19:44:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	2730D_IDS-1.pdf	611652 126b541906bce3d913cfb020f14e71e868c0cd6e	no	4

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,388	03/21/2011	Peter Z. Onufryk	IDT-2730D-UT	6393
33087 7590 02/06/2013 GLASS & ASSOCIATES P.O. BOX 1220 LOS GATOS, CA 95031-1220			EXAMINER AUVE, GLENN ALLEN	
			ART UNIT 2111	PAPER NUMBER
			MAIL DATE 02/06/2013	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	13/052,388		ONUFRYK ET AL.	
	Examiner		Art Unit	
	GLENN A. AUVE		2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on ____.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☒ Claim(s) 9-12 and 16 is/are allowed.

7) ☒ Claim(s) 1-8, 13-15 and 17-20 is/are rejected.

8) ☐ Claim(s) ____ is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☐ The specification is objected to by the Examiner.

11) ☒ The drawing(s) filed on 21 March 2011 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 1/29/2013.

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.

4) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of 35 U.S.C. 112(b):

(B) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-8, 13-15 and 17-20 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 1 is rejected because it is not clear what is meant by “determine the completion queue of the host processing unit plurality [sic] of completion queues contains an unprocessed completion status based on the interrupt vector state” on lines 6-8. There appears to be something missing from this part of the claim.

Claims 2-8 are rejected because they depend on claim 1.

Claim 7 is also rejected because it is not clear what is meant by “indicating an aggregate time over update operations performed on the interrupt vector state” on lines 2-3.

Claim 13 is rejected based on lack of positive antecedent basis of “the host controller interface” on line 3.

Claim 14 is rejected because it depends on claim 13.

Claim 15 is also rejected because it is not clear what is meant by “an aggregate time indicator for indicating an aggregate time over update operations performed on the interrupt vector state” on lines 2-3.

Claim 17 is rejected based on lack of positive antecedent basis of "the nonvolatile memory interface" on line 10.

Claims 18-20 are rejected because they depend on claim 17.

Allowable Subject Matter

3. Claims 9-12 and 16 are allowed.

4. The following is a statement of reasons for the indication of allowable subject matter: The prior art does not show the claimed completion queue in combination with the interrupt manager controller and their details.

5. It is noted that the NVM Express specification generally shows the subject matter claimed in at least the independent claims in section 7.5.1.1.1. However the examiner has only been able to locate Revision 1.0b of the specification which is dated July 12, 2011. This document does not indicate what changes were made between version 1.0 and 1.0b. Version 1.0 was published March 1, 2011 which does pre-date the application filing date. Applicant claims priority to provisional application 61/374242 which was filed August 16, 2010, however the examiner is unable to find basis for the claimed subject matter in the provisional application. Applicant is invited to point out where the provisional application provides a basis for the claimed subject matter in order to receive the benefit of the filing date of the provisional.

Requirement for Information under 37 CFR 1.105

6. Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application.

7. In response to this requirement, please provide the title, citation and copy of each publication that any of the applicants relied upon to draft the claimed subject matter. For each publication, please provide a concise explanation of the reliance placed on that publication in distinguishing the claimed subject matter from the prior art.

8. In particular, applicant's specification makes reference to the Nonvolatile Memory Express (NVMe) standard. It appears that the assignee is a "Promoter" of the NVM Express standard and a permanent member of the Promoters Group. The claimed subject matter is related to various elements of the NVM Express standard as noted above with respect to the NVM Express Revision 1.0b. It is presumed that applicant had access to the initial published version of the standard (NVM Express Revision 1.0) which predates applicant's filing date. Applicant should provide at least relevant portions of that document as well as any others relied upon in drafting the claims as indicated above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The cited references to Ma, Gupta et al., and Binford et al. show handling interrupts using completion queues. However none of these references show the claimed interrupt manager to generate a completion queue state and an interrupt message packet for triggering an interrupt in the host processing unit to alert it of the unprocessed completion status in the completion queue.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GLENN A. AUVE whose telephone number is (571)272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

Application Number: 13/052,388

5

Art Unit: 2111

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached on (571) 272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GLENN A. AUVE/
Primary Examiner
Art Unit 2111

/TIM VO/
Supervisory Patent Examiner
Art Unit 2111

gaa

Notice of References Cited	Application/Control No. 13/052,388	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.	
	Examiner GLENN A. AUVE	Art Unit 2111	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,875,343 A	02-1999	Binford et al.	710/263
*	B	US-8,244,946 B2	08-2012	Gupta et al.	710/263
*	C	US-2008/0256280 A1	10-2008	Ma, Xiuling	710/263
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	NVM Express, Revision 1.0b; Intel Corporation; pages 103-106 and 110-114; July 12, 2011.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052388
	Filing Date		2011-03-21
	First Named Inventor	Peter Z. Onufryk	
	Art Unit	13052388 - GAU: 2111	
	Examiner Name		
	Attorney Docket Number	IDT-2730D-UT	

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
/GA/	1	7708195		2010-05-04	Yoshida et al.			
/GA/	2	7620784		2009-11-17	Panabaker, Ruston			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
/GA/	1	20100262979		2010-10-14	Borchers et al.			
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052388	13052388 - GAU: 2111
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730D-UT	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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EXAMINER SIGNATURE

Examiner Signature	/Glenn Auve/	Date Considered	01/30/2013
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13052388 13052388 - GAU: 2111
	Filing Date	2011-03-21
	First Named Inventor	Peter Z. Onufryk
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IDT-2730D-UT

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kenneth Glass/	Date (YYYY-MM-DD)	2013-01-29
Name/Print	Kenneth Glass	Registration Number	42587

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
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Search Notes 	Application/Control No. 13052388	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner GLENN A AUVE	Art Unit 2111

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
710	48,50,260,269	1/29/2013	/GA/
711	156	1/29/2013	/GA/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	1/29/2013	/GA/
Internet search: Nonvolatile Memory Express, NVMe	1/30/2013	/GA/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 13052388	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner GLENN A AUVE	Art Unit 2111

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	01/30/2013									
	1	✓									
	2	✓									
	3	✓									
	4	✓									
	5	✓									
	6	✓									
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	17	✓									
	18	✓									
	19	✓									
	20	✓									

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	nonvolatile adj memory adj express	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:39
L2	16	nvme	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:39
L3	1013411	interrupt\$3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
L4	1727	complet\$3 adj queue	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
L5	327	3 same L4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
L6	175	(complet\$3 adj queue).ti,ab.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
L7	42	5 and 6	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
S1	1	"20060230215".pn.	US-PGPUB; USPAT	OR	OFF	2007/02/07 13:20
S2	157845	memory adj controller	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:11
S3	2186	interrupt\$3 near manag\$3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:11
S4	1727	complet\$3 adj queue	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S5	0	S3 same S4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S6	30	S3 and S4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S7	1	S2 and S6	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S8	2423	710/260,269,48,50.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:24
S9	31	S4 and S8	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:24

EAST Search History

S10	29	S9 not S6	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:24
S11	2017	711/156.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:25
S12	8	S4 and S11	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:25
S13	37	S10 or S12	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:25
S14	2	"5875343".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:47

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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052388	
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730D-UT	

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20110161678		2011-06-30	Niwa, Yasuyuki			
	2	20080320214		2008-12-25	Ma et al.			
	3	20090077302		2009-03-19	Fukuda, Hideaki			
	4	20100185808		2010-07-22	Yu et al.			
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	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number	IDT-2730D-UT		

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	1	NVM Express, Revision 1.0; Intel Corporation; March 1, 2011.	☐

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	Filing Date	2011-03-21
	First Named Inventor	Peter Z. Onufryk
	Art Unit	
	Examiner Name	
	Attorney Docket Number	IDT-2730D-UT

CERTIFICATION STATEMENT

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☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

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Signature	/Kenneth Glass/	Date (YYYY-MM-DD)	2013-05-06
Name/Print	Kenneth Glass	Registration Number	42587

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Patent Application Fee Transmittal				
Application Number:		13052388		
Filing Date:		21-Mar-2011		
Title of Invention:		INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER		
First Named Inventor/Applicant Name:		Peter Z. Onufryk		
Filer:		Kenneth Glass		
Attorney Docket Number:		IDT-2730D-UT		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	15696077
Application Number:	13052388
International Application Number:	
Confirmation Number:	6393
Title of Invention:	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730D-UT
Receipt Date:	06-MAY-2013
Filing Date:	21-MAR-2011
Time Stamp:	12:36:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$180
RAM confirmation Number	10480
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Non Patent Literature	NVM_Express_1_0_Gold-pdfprint.pdf	16740013 180f22fa03f3454fd07b57af190264b2431dbfd	no	122
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2730D_IDS-2.pdf	611859 9d98baf8cc28eecd76348812644deb42f3b30d9	no	4
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30413 81fa969f8370059cdf90d64c9abb2b5d30854e87	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			17382285		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Peter Onufryk

Practitioner's Docket No.: IDT-2730D-UT

Filing Date: 03/21/2011

For: INTERRUPT TECHNIQUE FOR A
NONVOLATILE MEMORY CONTROLLER

Serial No.: 13/052,388

Examiner: Auve, Glen Allen

Art Unit: 2111

Mail Stop Amendment
Commissioner for Patent
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The following response is presented in response to the Non-Final Examiner's Action mailed on February 6, 2013.

AMENDMENT A
(37 C.F.R. § 1.121)

Amendments to the claims begin on page 2 of this paper.

Remarks begin on page 8 of this paper.

Serial No.: 13/052,388

1 of 10

IDT-2730D-UT

AMENDMENTS TO THE CLAIMS:

Please replace the claim set with the following complete set of claims.

1. (Currently Amended) A nonvolatile memory controller for alerting a host processing unit to an unprocessed completion status contained in a completion queue of the host processing unit, the nonvolatile memory controller comprising:

an interrupt manager configured to generate a completion queue state for indicating the occurrence of a completion queue event associated with the completion queue, generate an interrupt vector state based on the completion queue state, determine the completion queue of the host processing unit, ~~plurality of completion queues~~ unit contains an unprocessed completion status based on the interrupt vector state, and generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue, and wherein the completion queue state includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.

2. (Original) The nonvolatile memory controller of claim 1, wherein the interrupt is a hardware interrupt.

3. (Original) The nonvolatile memory controller of claim 1, wherein the interrupt message packet includes an interrupt vector associated with the completion queue for triggering the interrupt in the host processing unit.

4. Canceled

5. (Original) The nonvolatile memory controller of claim 3, wherein completion queue state includes an event count indicating a number of completion message packets received by the host controller interface for the completion queue associated with the completion queue state.

6. (Original) The nonvolatile memory controller of claim 5, wherein the interrupt vector state includes an aggregate event count for aggregating event counts of the completion queue state over a plurality of update operations, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate event count is below an aggregate event count threshold.

7. (Currently Amended) The nonvolatile memory controller of claim 3, wherein the interrupt vector state includes an aggregate time indicator for indicating ~~an aggregate time over update operations performed on the interrupt vector state~~, a time period between the last time the interrupt manager generated an interrupt message packet for the completion queues associated with the interrupt vector state.

8. (Original) The nonvolatile memory controller of claim 3, wherein the completion queue state includes an empty queue indicator for indicating whether the completion queue is empty, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the empty queue indicator indicates the completion queue is empty.

9. (Original) A nonvolatile memory controller comprising:

a completion queue state memory configured to store a plurality of completion queue states corresponding to a plurality of completion queues in a host processing unit;

an interrupt vector state memory configured to store a plurality of interrupt vector states corresponding to a plurality of interrupt vectors in the host processing unit; and

an interrupt manager controller coupled to the completion queue state memory and the interrupt vector state memory, the interrupt manager controller configured to map at least one completion queue state of the plurality of completion queue states to an interrupt vector state of the plurality of interrupt vector states, generate the interrupt vector state based on each completion queue state mapped to the interrupt vector state, determine a completion queue corresponding to a completion queue state mapped to the interrupt vector state contains an unprocessed completion status based on the interrupt vector state, and to generate an interrupt message packet based on the interrupt vector state for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.

10. (Original) The nonvolatile memory controller of claim 9, wherein the interrupt manager controller is configured to map at least two completion queue states of the plurality of completion queue states to the interrupt vector state.

11. (Original) The nonvolatile memory controller of claim 9, wherein the interrupt manager controller is a sequential logic circuit.

12. (Original) The nonvolatile memory controller of claim 9, wherein a completion queue state of the plurality of completion queue states includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.

13. (Currently Amended) The nonvolatile memory controller of claim 9, wherein a completion queue state of the plurality of completion queue states includes an event count indicating a number of completion message packets received by ~~the~~ a host controller interface and including a completion status for the completion queue associated with the completion queue state.

14. (Original) The nonvolatile memory controller of claim 13, wherein the interrupt vector state includes an aggregate event count for aggregating event counts of the completion queue state over a plurality of update operations, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate event count is below an aggregate event count threshold.

15. (Currently Amended) The nonvolatile memory controller of claim 9, wherein the interrupt vector state includes an aggregate time indicator for indicating ~~an aggregate time over update operations performed on the interrupt vector state~~ a time period between the last time the interrupt manager generated an interrupt message packet for the completion queues associated with the interrupt vector state, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate time indicator is below an aggregate time threshold.

16. (Original) The nonvolatile memory controller of claim 9, wherein a completion queue state of the plurality of completion queue states includes an empty queue indicator for indicating whether the completion queue is empty, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the empty queue indicator indicates the completion queue is empty.

17. (Currently Amended) A method comprising:

generating a completion queue state by a nonvolatile memory controller for indicating the occurrence of a completion queue event associated with a completion queue in a host processing unit, the completion queue state including a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue;

generating an interrupt vector state by the nonvolatile memory controller based on the completion queue state, the interrupt vector state associated with an interrupt vector in the host processing unit;

determining by the nonvolatile memory controller based on the interrupt vector state that the completion queue contains an unprocessed completion status; and

generating an interrupt message packet by ~~the~~ a nonvolatile memory interface for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.

18. (Original) The method of claim 17, further comprising sending the interrupt message packet to the host processing unit.

19. (Original) The method of claim 17, wherein the completion queue event is the host processing unit updating a head pointer stored in the nonvolatile memory controller for the completion queue.
20. (Original) The method of claim 17, wherein the completion queue event is detecting a completion queue event flag set in a completion message packet containing a completion status.

REMARKS:

Applicant has carefully studied the Non-Final Examiner's Action having an electronic mail date of February 6, 2013 and all references cited therein.

Applicant has amended independent claims 1 and 17 to more particularly point out Applicant's invention. Furthermore Applicant has amended claims 7, 13, 15 and 17 to overcome the 35 U.S.C. 112 rejection presented by the Office.

The present amendments and explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Claim Rejections – 35 U.S.C. § 112

Claims 1-8, 13-15 and 17-20 stand rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claims 7, 13, 15 and 17 have been amended to overcome the objection presented by the Office. Claims 2-3, 5-8, 14 and 18-20 are dependent upon one of claims 7, 13, 15 and 17, which have been amended to overcome the objection, and as such are believed to be in condition for allowance.

Requirement for Information – 37 C.F.R. § 1.105

Applicant thanks the Examiner for taking the time to discuss the present Requirement for Information. As discussed in the telephone conference on May, 3, 2012 between Applicant's representative, Kenneth Glass and the Examiner, Applicant is submitting an IDS that includes a copy of the NVM Express standard revision 1.0, published on March 1, 2011. Applicant believes that this submission is sufficient for the purpose of examination of the present application.

Applicant asserts that the Examiner's request for information is overly broad and that information regarding drafting of the NVM Express standard should be required as it is not material to patentability. However, in order to meet the requirements of 37 C.F.R. § 1.105 Applicant is submitting separately, via USPS, drafts 056 (dated 6/3/10) and 086 (dated 11/4/10) of the NVM Express standard, and email correspondence relating to drafting of the NVM Express standard. This material is provided pursuant to MPEP 724.02 and constitutes proprietary information. Applicant asserts that the material provided pursuant to MPEP 724.02 is not material to patentability. Accordingly, Applicant requests that the material provided pursuant to MPEP 724.02 be maintained as proprietary information and not be included in the case file. Moreover, after this information has been reviewed by the Examiner, and after determination by the Examiner that the information is not material to patentability, Applicant requests that the material provided pursuant to MPEP 724.02 be returned to Applicant.

Summary

Applicant thanks the Examiner for allowing claims 9-12 and 16. Applicant asserts that remaining claims 1-3, 5-8, 13-15 and 17-20 now meet the requirements of 35 U.S.C. 112.

Accordingly, Applicant asserts that claims 1-3, 5-8, 13-15 and 17-20 are now in condition for allowance as well. Therefore, Applicant requests allowance of claims 1-3, 5-8, 13-15 and 17-20.

If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned at (408) 354-4448 is requested.

Respectfully Submitted,

May 6, 2013
Date

/Kenneth Glass/
Kenneth Glass
Attorney/Agent for Applicant(s)
Reg. No. 42587

PO Box 1220
Los Gatos, CA 95031-1220
Tel. (408) 354-4448

Electronic Acknowledgement Receipt	
EFS ID:	15706183
Application Number:	13052388
International Application Number:	
Confirmation Number:	6393
Title of Invention:	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	IDT-2730D-UT
Receipt Date:	06-MAY-2013
Filing Date:	21-MAR-2011
Time Stamp:	20:45:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		IDT-2730D-UTAmendmentA.pdf	101584 7c93e9da3934ec6c7f5bc991ba377073383d362d	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	10
Warnings:			
Information:			
Total Files Size (in bytes):		101584	
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 13/052,388		Filing Date 03/21/2011		☐ To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			TOTAL			TOTAL				
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	05/06/2013	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	X \$ =		OR	X \$80=	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$ =		OR	X \$420=	0
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
	TOTAL ADD'L FEE						OR	TOTAL ADD'L FEE		0
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))							OR		
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
	TOTAL ADD'L FEE						OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/LINDA A. WASHINGTON/

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	13/052388
	Filing Date	3/21/11
	First Named Inventor	PETER Z. ONOFREYK
	Art Unit	2011
	Examiner Name	GLEN ALLEN AUBE
Total Number of Pages in This Submission	Attorney Docket Number	IDT-2730D-UT

ENCLOSURES (Check all that apply)	
Fee Transmittal Form	Drawing(s)
Fee Attached	Licensing-related Papers
Amendment/Reply	Petition
After Final	Petition to Convert to a Provisional Application
Affidavits/declaration(s)	Power of Attorney, Revocation
Extension of Time Request	Change of Correspondence Address
Express Abandonment Request	Terminal Disclaimer
Information Disclosure Statement	Request for Refund
Certified Copy of Priority Document(s)	CD, Number of CD(s)
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Remarks	
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	GLASS & ASSOCIATES		
Signature			
Printed name	KENNETH GLASS		
Date	5/6/13	Reg. No.	42,587

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13052388XA

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March 8, 2004



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33087 7590 06/13/2013
GLASS & ASSOCIATES
P.O. BOX 1220
LOS GATOS, CA 95031-1220

EXAMINER

AUVE, GLENN ALLEN

ART UNIT

PAPER NUMBER

2111

DATE MAILED: 06/13/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,388	03/21/2011	Peter Z. Onufryk	IDT-2730D-UT	6393

TITLE OF INVENTION: INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	09/13/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

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II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

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(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,388	03/21/2011	Peter Z. Onufryk	IDT-2730D-UT	6393

TITLE OF INVENTION: INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	09/13/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
AUVE, GLENN ALLEN	2111	710-260000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,388	03/21/2011	Peter Z. Onufryk	IDT-2730D-UT	6393
33087	7590	06/13/2013	EXAMINER	
GLASS & ASSOCIATES			AUVE, GLENN ALLEN	
P.O. BOX 1220			ART UNIT	
LOS GATOS, CA 95031-1220			PAPER NUMBER	

2111

DATE MAILED: 06/13/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 261 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 261 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/052,388	Applicant(s) ONUFRYK ET AL.	
	Examiner GLENN A. AUVE	Art Unit 2111	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed 6 May 2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-3 and 5-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Interim copies:
a) ☐ All b) ☐ Some c) ☐ None of the: Interim copies of the priority documents have been received.

Applicant has **THREE MONTHS FROM THE "MAILING DATE"** of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in **ABANDONMENT** of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ **CORRECTED DRAWINGS** (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ **DEPOSIT OF and/or INFORMATION** about the deposit of **BIOLOGICAL MATERIAL** must be submitted. Note the attached Examiner's comment regarding **REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL**.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>5/6/2013</u>	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/GLENN A. AUVE/ Primary Examiner, Art Unit 2111	
--	--

REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance: independent claim 1 includes the limitations of the details of the operation of the interrupt manager's operation which are not shown in the prior art.
2. Independent claim 9 includes the limitations of the details of the interrupt manager controller's operation which are not shown in the prior art.
3. Independent claim 17 includes the limitations of the details of steps performed by the nonvolatile memory controller which are not shown in the prior art.
4. The examiner appreciates being provided with the NVM Express 1.0 specification. After close review of the document it does not show the details of the steps performed by the memory controller as claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GLENN A. AUVE whose telephone number is (571)272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Vo can be reached on (571) 272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GLENN A. AUVE/
Primary Examiner
Art Unit 2111

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		1305238813052388 - GAU: 2111	
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730D-UT	

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S. PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20110161678		2011-06-30	Niwa, Yasuyuki			
	2	20080320214		2008-12-25	Ma et al.			
	3	20090077302		2009-03-19	Fukuda, Hideaki			
	4	20100185808		2010-07-22	Yu et al.			
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13052388	13052388 - GAU: 2111
	Filing Date		2011-03-21	
	First Named Inventor	Peter Z. Onufryk		
	Art Unit			
	Examiner Name			
	Attorney Docket Number		IDT-2730D-UT	

	1							☐
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If you wish to add additional Foreign Patent Document citation information please click the Add button **Add**

NON-PATENT LITERATURE DOCUMENTS

Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	NVM Express, Revision 1.0; Intel Corporation; March 1, 2011.	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/Glenn Auve/	Date Considered	06/03/2013
--------------------	--------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13052388	13052388 - GAU: 2111
	Filing Date	2011-03-21	
	First Named Inventor	Peter Z. Onufryk	
	Art Unit		
	Examiner Name		
	Attorney Docket Number	IDT-2730D-UT	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Kenneth Glass/	Date (YYYY-MM-DD)	2013-05-06
Name/Print	Kenneth Glass	Registration Number	42587

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /GA/



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BIB DATA SHEET

CONFIRMATION NO. 6393

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
13/052,388	03/21/2011	710	2111	IDT-2730D-UT		
APPLICANTS Peter Z. Onufryk, Flanders, NJ; Jayesh Patel, San Jose, CA; Ihab Jaser, San Jose, CA; ** CONTINUING DATA ***** This appln claims benefit of 61/374,242 08/16/2010 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 03/30/2011						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /GLENN ALLEN Acknowledged AUVE/ Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY NJ	SHEETS DRAWINGS 17	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS GLASS & ASSOCIATES P.O. BOX 1220 LOS GATOS, CA 95031-1220 UNITED STATES						
TITLE INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER						
FILING FEE RECEIVED 1090	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Issue Classification 	Application/Control No. 13052388	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner GLENN A AUVE	Art Unit 2111

CPC		
Symbol	Type	Version

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
710		260				G	0	6	F	13 / 24 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
710	48	269																	

NONE		Total Claims Allowed:	
(Assistant Examiner)		19	
(Date)			
/GLENN A AUVE/ Primary Examiner.Art Unit 2111		06/05/2013	
(Primary Examiner)		(Date)	
		O.G. Print Claim(s)	O.G. Print Figure
		1	3

Issue Classification 	Application/Control No. 13052388	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner GLENN A AUVE	Art Unit 2111

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/GLENN A AUVE/ Primary Examiner.Art Unit 2111	06/05/2013	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3

Issue Classification 	Application/Control No. 13052388	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner GLENN A AUVE	Art Unit 2111

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17												
2	2	17	18												
3	3	18	19												
-	4	19	20												
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10	11														
11	12														
12	13														
13	14														
14	15														
15	16														

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 19	
/GLENN A AUVE/ Primary Examiner. Art Unit 2111 (Primary Examiner) _____ (Date) _____		O.G. Print Claim(s) 1	O.G. Print Figure 3

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	2093	711/156.ccls.	US-PGPUB; USPAT	OR	OFF	2013/06/05 14:37
L3	2218	interrupt\$3 near manag\$3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/05 14:38
L4	2218	L3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/05 14:38
L5	5	1 and 3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/05 14:38
L6	1790	complet\$3 adj queue	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/05 14:38
L7	1790	L6	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/05 14:38
L8	8	1 and 6	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/05 14:38
S1	1	"20060230215".pn.	US-PGPUB; USPAT	OR	OFF	2007/02/07 13:20
S2	157845	memory adj controller	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:11
S3	2186	interrupt\$3 near manag\$3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:11
S4	1727	complet\$3 adj queue	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S5	0	S3 same S4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S6	30	S3 and S4	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S7	1	S2 and S6	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:12
S8	2423	710/260,269,48,50.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:24
S9	31	S4 and S8	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:24
S10	29	S9 not S6	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:24

			EPO; JPO; DERWENT; IBM_TDB			16:24
S11	2017	711/156.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:25
S12	8	S4 and S11	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:25
S13	37	S10 or S12	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:25
S14	2	"5875343".pn.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/29 16:47
S15	0	nonvolatile adj memory adj express	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:39
S16	16	nvme	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:39
S17	1013411	interrupt\$3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
S18	1727	complet\$3 adj queue	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
S19	327	S17 same S18	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
S20	175	(complet\$3 adj queue).ti,ab.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
S21	42	S19 and S20	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/30 14:41
S22	0	nonvolatile adj memory adj express	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/04 13:26
S23	0	S22	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/04 13:26
S24	164255	memory adj controller	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/04 13:28
S25	2216	interrupt\$3 near manag\$3	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/04 13:28
S26	1787	complet\$3 adj queue	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/04 13:28
S27	1	S24 and S25 and S26	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/04 13:28
S28	2468	710/260,269,48,50.ccls.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/06/04 13:57
S29	34	S26 and S28	US-PGPUB; USPAT; FPRS;	OR	ON	2013/06/04

		EPO; JPO; DERWENT; IBM_TDB		13:58
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EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	3	711/156.ccls.	UPAD	OR	OFF	2013/06/05 14:37
S30	2	710/260,269,48,50.ccls.	UPAD	OR	ON	2013/06/04 13:54
S31	0	nonvolatile adj memory adj express	UPAD	OR	ON	2013/06/04 13:54
S32	9	interrupt\$3 near manag\$3	UPAD	OR	ON	2013/06/04 13:54
S33	24	complet\$3 adj queue	UPAD	OR	ON	2013/06/04 13:55

6/ 5/ 2013 2:39:15 PM**C:\ Users\ gauve\ Documents\ EAST\ Workspaces\ 13052388.wsp**

Search Notes 	Application/Control No. 13052388	Applicant(s)/Patent Under Reexamination ONUFRYK ET AL.
	Examiner GLENN A AUVE	Art Unit 2111

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
710	48,50,260,269	1/29/2013	/GA/
711	156	1/29/2013	/GA/
update above		6/5/2013	/GA/

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search	1/29/2013	/GA/
Internet search: Nonvolatile Memory Express, NVMe	1/30/2013	/GA/
update above	6/5/2013	/GA/

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
710	48,50,260,269	6/5/2013	/GA/
711	156	6/5/2013	/GA/

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

33087 7590 06/13/2013
GLASS & ASSOCIATES
P.O. BOX 1220
LOS GATOS, CA 95031-1220

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,388	03/21/2011	Peter Z. Onufryk	IDT-2730D-UT	6393

TITLE OF INVENTION: INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$0	\$0	\$1780	09/13/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
AUVE, GLENN ALLEN	2111	710-260000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Kenneth Glass

2 Stanley J. Pawlik

3 Glass & Associates

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PMC-SIERRA, INC., SUNNYVALE, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 501006 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Kenneth Glass/

Date 9/4/13

Typed or printed name Kenneth Glass

Registration No. 42,587

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

000197

OR



The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	13/052,388

Completed by (check one):



Applicant/Inventor

/Kenneth Glass/

Signature



Attorney or Agent of record 42,587
 (Reg. No.)

Kenneth Glass

Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
 Statement under 37 CFR 3.73(b) is enclosed.
 (Form PTO/SB/96)

408-354-4448

Requester's telephone number



Assignee recorded at Reel _____ Frame _____

September 4, 2013

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.



* Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13052388		
Filing Date:		21-Mar-2011		
Title of Invention:		INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER		
First Named Inventor/Applicant Name:		Peter Z. Onufryk		
Filer:		Kenneth Glass		
Attorney Docket Number:		PMCS-2730D-UT		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				1780

Electronic Acknowledgement Receipt	
EFS ID:	16765211
Application Number:	13052388
International Application Number:	
Confirmation Number:	6393
Title of Invention:	INTERRUPT TECHNIQUE FOR A NONVOLATILE MEMORY CONTROLLER
First Named Inventor/Applicant Name:	Peter Z. Onufryk
Customer Number:	33087
Filer:	Kenneth Glass
Filer Authorized By:	
Attorney Docket Number:	PMCS-2730D-UT
Receipt Date:	04-SEP-2013
Filing Date:	21-MAR-2011
Time Stamp:	18:34:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1780
RAM confirmation Number	6147
Deposit Account	501006
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Issue Fee Payment (PTO-85B)	IssueFeePayment-85B.pdf	111647 4ca62866da3b6eed949a961809891fe9aaa4663e	no	2
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	sb0047.pdf	209779 8c05c0db0a3be96a8b1ae679436d3452d34be9ca	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30094 e2d5fc2db85f46f556472362583a8d6c5d150e45	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			351520		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/052,388	10/08/2013	8554968	PMCS-2730D-UT	6393

33087 7590 09/18/2013
GLASS & ASSOCIATES
P.O. BOX 1220
LOS GATOS, CA 95031-1220

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 261 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Peter Z. Onufryk, Flanders, NJ;
Jayesh Patel, San Jose, CA;
Ihab Jaser, San Jose, CA;

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