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14 **UNITED STATES DISTRICT COURT**
15 **CENTRAL DISTRICT OF CALIFORNIA**
16

17 POLARIS POWERLED
TECHNOLOGIES, LLC,

18 Plaintiff,

19 v.

20 WESTERN DIGITAL
21 CORPORATION AND WESTERN
DIGITAL TECHNOLOGIES, INC.,

22 Defendants,
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27
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CASE NO. 2:24-cv-02864-ODW-MAR

**DEFENDANTS' PROPOSED
PRELIMINARY CLAIM
CONSTRUCTIONS AND
INTRINSIC AND EXTRINSIC
EVIDENCE**

Hon. Otis D. Wright

DEFENDANTS' PROPOSED PRELIMINARY CLAIM CONSTRUCTIONS AND
INTRINSIC AND EXTRINSIC EVIDENCE

1 Pursuant to Patent Local Rule 4-2, Defendants Western Digital Corporation
2 and Western Digital Technologies, Inc. identify their proposed preliminary claim
3 constructions and supporting intrinsic and extrinsic evidence. Western Digital is
4 prepared to meet and confer with Polaris at a mutually agreeable time to finalize a
5 combined table of proposed constructions, narrow or resolve differences, and
6 facilitate the ultimate preparation of a Joint Claim Construction and Prehearing
7 Statement.

8 Western Digital discloses that it may offer expert-witness testimony, including
9 by declaration, for a variety of purposes, including to: (1) provide a background of
10 the technology at issue; (2) explain how the alleged invention(s) work; (3) describe
11 the qualifications of a person of ordinary skill in the art (“POSITA”) at the time of the
12 alleged invention; (4) describe how a POSITA would understand certain claim terms;
13 (5) describe that Western Digital’s proposed constructions are derived from the
14 intrinsic and, where applicable, extrinsic evidence; (6) rebut Polaris’s proposed
15 constructions; and/or (7) provide any tutorial that the Court may choose to conduct.

16 Western Digital’s preliminary claim constructions and identification of
17 extrinsic evidence are based on information that is currently available to Western
18 Digital. Western Digital reserves the right to add, eliminate, amend, supplement, or
19 modify the constructions, including in the event that additional information becomes
20 available through discovery, after consideration of Polaris’s proposed constructions,
21 following the meet-and-confer discussions regarding the parties’ proposed terms and
22 constructions, and/or in light of arguments Polaris makes or positions it takes as the
23 case proceeds. Western Digital also reserves the right to rely on any evidence cited by
24 Polaris and to identify additional intrinsic or extrinsic evidence, including expert
25 testimony, in rebuttal to any of Polaris’s positions, intrinsic evidence, or extrinsic
26 evidence, including expert testimony.

U.S. Patent No. 8,554,968	
Claim Term, Phrase, or Clause	Preliminary Construction and Supporting Evidence
“A nonvolatile memory controller for alerting a host processing unit to an unprocessed completion status contained in a completion queue of the host processing unit, the nonvolatile memory controller comprising:” Claim 1	The preamble is limiting ’968 Patent, Abstract, 1:26–2:26, 16:28–43; Fig. 3, Claim 1. Am. Compl., ¶¶ 37–38; 39–41.
“interrupt manager”/ “interrupt manager controller” Claims 1, 6, 7, 8, 9, 10, 14, 15	Functionality performed within the nonvolatile memory controller for alerting the host processing unit to an unprocessed completion status ’968 Patent, Abstract, 1:26–2:26; 3:33–53; 4:13–48; 6:19–28; 7:38–10:65–11:4; 11:28–41; 13:6–22; 15:3–29:14; Figs. 1–16; Claims 1, 6, 7, 8, 9, 10, 14, 15; ’968 Patent File History, 05/06/2013 Amendment and Response; ’968 Patent File History, 06/13/2013 Notice of Allowance. Am. Compl., ¶¶ 37–38; 39–41 WDTECH00009870 (A Dictionary of Computing at 543); WDTECH00009862 Dictionary of Computing (2010) at 349; WD_INV00003021–WD_INV00003142 (NVM Express, R1.0); Western Digital may also rely on expert testimony about the meaning of

1		“interrupt” to those of skill in the
2		art, the architecture of non-
3		volatile memory controllers,
4		communications between non-
5		volatile memory controllers and
6		host processing units, and/or how
7		a POSITA would understand the
8		term “interrupt manager” in light
9		of the intrinsic record.
10	“interrupt vector state”	Current conditions associated
11	Claims 1, 6, 8, 14, 16	with an interrupt vector in the
12		host processing unit used to
13		determine whether to send an
14		interrupt
15		
16		’968 Patent, 1:39–42; 15:3–
17		16:67; 17:22–54; 18:37–29:21;
18		Figs. 9–22; Claims 1, 6, 8, 14,
19		16; ’968 Patent File History,
20		05/06/2013 Amendment and
21		Response; ’968 Patent File
22		History, 06/13/2013 Notice of
23		Allowance.
24		
25		WDTECH0009847 (Newton’s
26		Telecom Dictionary at 1055);
27		WDTECH00009869 (A
28		Dictionary of Computing (2008)
		at 543); WDTECH00009862
		(Dictionary of Computing (2010)
		at 349); WD_INV00003021–
		WD_INV00003142 (NVM
		Express, R1.0); Western Digital
		may also rely on expert
		testimony about the meaning of
		“interrupt vector” and “state” to
		those of skill in the art,
		communications between non-

	volatile memory controllers and host processing units, and/or how a POSITA would understand the term “interrupt vector state” in light of the intrinsic record.
“completion queue state” Claims 1, 7, 8, 9, 11, 15, 16	Current conditions of a completion queue ’968 Patent, 1:56–2:41; 15:12–52; 17:1–31; 17:64–18:36; 21:47–24:10; 28:5–16; Figs. 5, 9–22; Claims 1, 7, 8, 9, 11, 15, 16; ’968 Patent File History, 05/06/2013 Amendment and Response; ’968 Patent File History, 06/13/2013 Notice of Allowance. WDTECH0009847 (Newton’s Telecom Dictionary at 1055); WD_INV00003021–WD_INV00003142 (NVM Express, R1.0); Western Digital may also rely on expert testimony about the meaning of “completion queue” and “state” to those of skill in the art, communications between non-volatile memory controllers and host processing units, and/or how a POSITA would understand the term “completion queue state” in light of the intrinsic record.
“generate a completion queue state for indicating the occurrence of a completion queue event associated with the completion queue, generate an interrupt vector state based on the completion queue state determine the	Steps must be performed in order ’968 Patent, 1:39–2:41; 15:3–29:14; Figs. 5, 9–22; Claim 1

1	completion queue of the host processing unit	Western Digital may also rely on
2	contains an unprocessed completion status	expert testimony about
3	based on the interrupt vector state, and generate	communications between non-
4	an interrupt message packet for triggering an	volatile memory controllers and
5	interrupt in the host processing unit to alert the	host processing units and how a
6	host processing unit of the unprocessed	POSITA would understand this
7	completion status in the completion queue,”	term in light of the intrinsic
8	Claim 1	record.
9	“map at least one completion queue state of the	Steps must be performed in order
10	plurality of completion queue states to an	’968 Patent, 1:39–2:41; 15:3–
11	interrupt vector state of the plurality of interrupt	29:14; Figs. 5, 9–22; Claim 8.
12	vector states, generate the interrupt vector state	Western Digital may also rely on
13	based on each completion queue state mapped	expert testimony about
14	to the interrupt vector state, determine a	communications between non-
15	completion queue corresponding to a	volatile memory controllers and
16	completion queue state mapped to the interrupt	host processing units and how a
17	vector state contains an unprocessed completion	POSITA would understand this
18	status based on the interrupt vector state, and to	term in light of the intrinsic
19	generate an interrupt message packet based on	record.
20	the interrupt vector state for triggering an	
21	interrupt in the host processing unit to alert the	
22	host processing unit of the unprocessed	
23	completion status in the completion queue.”	
24	Claim 8	
25	“generating a completion queue state by a	Steps must be performed in order
26	nonvolatile memory controller for indicating the	’968 Patent, 1:39–2:41; 15:3–
27	occurrence of a completion queue event	29:14; Figs. 5, 9–22; Claim 16.
28	associated with a completion queue in a host	Western Digital may also rely on
	processing unit, . . . generating an interrupt	expert testimony about
	vector state by the nonvolatile memory	communications between non-
	controller based on the completion queue state,	volatile memory controllers and
	the interrupt vector state associated with an	host processing units and how a
	interrupt vector in the host processing unit;	POSITA would understand this
	determining by the nonvolatile memory	term in light of the intrinsic
	controller based on the interrupt vector state that	record.
	the completion queue contains an unprocessed	
	completion status; and generating an interrupt	
	message packet by a nonvolatile memory	

interface for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.”

Claim 16

U.S. Patent No. 9,183,085

“gear”

Claims 1, 15

A set of predefined error correction coding parameters providing a level of error correction coding strength

’085 Patent, Abstract; 1:24–2:28; 13:49–14:49; 16:47–17:56; 18:42–62; 19:16–37; 19:45–20:3; 20:18–25; 22:65–23:3; 23:59–24:15; 24:39–27:50; 27:51–28:18; 28:28–38; 30:8–22; 34:18–25; 34:53–40:50; 41:33–52; 43:47–60:18; Table III, Table IV, Table V, Table VI, Table VII; Table VIII; Figs. 3–11, 15; claims 1, 6, 8–10, 14, 15, 18–22, 26–29; ’085 Patent File History, 05/02/2014 Applicant Arguments/Remarks Made in an Amendment; ’085 Patent File History, 07/16/2014 Final Rejection; ’085 Patent File History, 11/17/2014 Request for Continued Examination; ’085 Patent File History, 02/02/2015 Non-Final Rejection and Applicant Initiated Interview Summary; ’085 Patent File History, 06/02/2015 Amendment.

Western Digital may also rely on expert testimony about how a

1		POSITA would understand
2		“gear” in light of the intrinsic
3		record.
4		
5	“ECC schemes”/ “error correction coding	a way to encode payload data
6	(ECC) scheme(s)”	and primary and secondary
7	Claims 1, 15	parity symbols specified by
8		parameters
9		’085 Patent, Abstract; 1:24–2:28;
10		3:45–4:3; 13:49–14:49; 16:47–
11		17:56; 18:42–62; 19:16–37;
12		19:45–20:3; 20:18–25; 22:65–
13		23:3; 23:59–24:15; 24:39–27:50;
14		27:51–28:18; 28:28–38; 30:8–
15		22; 34:18–25; 34:53–40:50;
16		41:33–52; 43:47–60:18; Table
17		III, Table IV, Table V, Table VI,
18		Table VII; Table VIII; Figs. 3–
19		11, 15; claims 1, 6, 8–10, 14, 15,
20		18–22, 26–29; ’085 Patent File
21		History, 05/02/2014 Applicant
22		Arguments/Remarks Made in an
23		Amendment; ’085 Patent File
24		History, 07/16/2014 Final
25		Rejection; ’085 Patent File
26		History, 11/17/2014 Request for
27		Continued Examination; ’085
28		Patent File History, 02/02/2015
		Non-Final Rejection and
		Applicant Initiated Interview
		Summary; ’085 Patent File
		History, 06/02/2015
		Amendment.
		WDTECH00009855
		(International Dictionary of Data
		Communications at 81);
		WDTECH00009850 (Newton’s

	Telecom Dictionary (2009) at 472); WDTECH00009865 (Dictionary of Computing (2010) at 178); WDTECH00009858 (Dictionary of Computer and Internet Terms (2009) at 174); Western Digital may also rely on expert testimony about how a POSITA would understand “ECC scheme” in light of the intrinsic record.
U.S. Patent No. 8,601,346	
“parity write command” Claims 1, 5, 7, 11, 14	Command for writing a parity block generated by the parity calculator ’346 Patent, Abstract; 1:50-60; 2:18-3:20; 7:6-13; 7:61-8:4; 8:62-9:8; 9:26-38; 11:1-40; 12:51-13:10; 14:63-15:31; 16:3-10; 17:13-52; 18:16-61; 20:30-40; 20:62-21:40; Claims 5, 7; Figs. 4-6, 9-12; ’346 Patent File History, 04/26/2013 Non-Final Rejection WDTECH00009854 (International Dictionary of Data Communications at 169); WDTECH0000986 (Newton’s Telecom Dictionary (2009) at 892); WDTECH00009866 (Dictionary of Computing (2010) at 369); WDTECH00009859 (Dictionary of Computer and Internet Terms (2009) at 353); Western Digital may also rely on

expert testimony about how a POSITA would understand “parity write command” in light of the intrinsic record.

Date: May 9, 2025

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CORPORATION and WESTERN
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CERTIFICATE OF SERVICE

I, the undersigned, declare that I am over the age of 18 years and not a party to the within action. I am employed in the County of Orange, State of California, within which county the subject service occurred. My business address is 600 Anton Boulevard, Suite 700, Costa Mesa, California 92626.

On **May 9, 2025**, I served the following document described as:
DEFENDANTS' IDENTIFICATION OF CLAIM TERMS FOR CONSTRUCTION on the interested party in this action, addressed as follows, and in the manner so indicated:

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☐ **BY ELECTRONIC FILING.** I caused such document(s) to be electronically filed and served through the United States District Court's CM/ECF System for the within action. This service complies with the Federal Rules of Civil Procedure. The file transmission was reported as complete and a copy of the Court's Notice of Electronic Filing will be maintained with the original document(s) in our office.

☒ **BY ELECTRONIC DELIVERY.** I caused a true and correct copy of such document to be served via electronic delivery to the interested parties in this action as indicated above.

I declare that I am employed in the offices of a member of the bar of this Court at whose direction this service was made. Executed on **May 9, 2025**, at San Clemente, California.

/s/Tara Hamilton
Tara Hamilton