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PCI-SIG specifications define standards driving the industry-wide compatibility of peripheral component interconnects. Members regularly review them, providing commentary and change requests when necessary. These requests are considered by technical workgroups and applied as appropriate, resulting in collaboratively devised specifications benefiting millions of platforms and add-in devices.

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NCTF Ground Ball Definition for PCIe BGA SSD 11.5x13 ECN.(rename)	2.x	ECN	May 18, 2018

Specification Title	Spec Rev	Document Type	Release Date
PCIe BGA SSD 11.5x13 ECN (rename)	2.x	ECN	January 25, 2017
PCI Express® Mini Card Electromechanical Specification Revision 2.1 with Change Bar This specification defines an implementation for sma...view more This specification defines an implementation for small form factor PCI Express cards. The specification uses a qualified subset of the same signal protocol, electrical definitions, and configuration definitions as the PCI Express Base Specification, Revision 2.0. Where this specification 5 does not explicitly define PCI Express characteristics, the PCI Express Base Specification governs. show less	2.x	Specification	December 15, 2016
PCI Express® Mini Card Electromechanical Specification Revision 2.1 This specification defines an implementation for sma...view more This specification defines an implementation for small form factor PCI Express cards. The specification uses a qualified subset of the same signal protocol, electrical definitions, and configuration definitions as the PCI Express Base Specification, Revision 2.0. Where this specification 5 does not explicitly define PCI Express characteristics, the PCI Express Base Specification governs. show less	2.x	Specification	December 15, 2016
Add USB 3.0 to the Mini Card Mobile broadband peak data rates continue to increas...view more Mobile broadband peak data rates continue to increase. With LTE category 5, USB 2.0 will not meet the performance requirements. LTE category 5 peak data rates are 320 Mbps downlink; 75 Mbps uplink. Most USB 2.0 implementations achieve a maximum of about 240 Mbps throughput. Looking longer term, the ITU has set a target of 1 Gbits/s for low mobility applications for IMT Advanced. show less	2.x	ECN	August 8, 2014
Tighten Mini Card Power Rail Voltage Tolerance Modify the Mini Card specification to tighten the po...view more Modify the Mini Card specification to tighten the power rail voltage tolerance. show less	2.x	ECN	March 3, 2014
PCI Express Architecture Configuration Space Test Specification Revision 2.0a This document primarily covers PCI Express testing o...view more This document primarily covers PCI Express testing of root complexes, switches, bridges, and endpoints for the standard configuration mechanisms, registers, and features in Chapter 7 of the PCI Express Base Specification, Revision 2.0. This specification does not describe the full set of PCI Express tests and assertions for these devices. show less	2.x	Specification	September 17, 2012
PCI Express Architecture Link Layer Test Specification Revision 2.0 This test specification primarily covers testing of ...view more This test specification primarily covers testing of all PCI Express Port types for compliance with the link layer requirements in Chapter 3 of the PCI Express Base Specification. At this point, this specification does not describe the full set of PCI Express tests for all link layer requirements. Going forward, as the testing gets mature, it is expected that more tests may be added as deemed necessary. show less	2.x	Specification	September 17, 2012
PCI Express Architecture PHY Test Specification Revision 2.0 This document provides test descriptions for PCI Exp...view more This document provides test descriptions for PCI Express electrical testing. It is relevant for anyone building add-in cards or system boards to the PCI Express Card Electromechanical Specification, Revision 2.0. This specification does not describe the full set of PCI Express tests and assertions for these devices. show less	2.x	Specification	September 17, 2012
PCI Express Architecture Configuration Space Test Specification Revision 2.0a with Change Bar This document primarily covers PCI Express testing o...view more This document primarily covers PCI Express testing of root complexes, switches, bridges, and endpoints for the standard configuration mechanisms, registers, and features in Chapter 7 of the PCI Express Base Specification, Revision 2.0. This specification does not describe the full set of PCI Express tests and assertions for these devices. show less	2.x	Specification	September 17, 2012
PCI Express External Cabling Specification Revision 2.0 This is a companion specification to the PCI Express...view more This is a companion specification to the PCI Express Base Specification. Its primary focus is the implementation	2.x	Specification	June 22, 2012

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of cabled PCI Express®. The discussions are confined to copper cabling and their connector requirements to meet the PCI Express signaling needs at 5.0 GT/s. No assumptions are made regarding the implementation of PCI Express compliant Subsystems on either side of the cabled Link; e.g., PCI Express Card Electromechanical (CEM), ExpressCard5™, ExpressModule™, PXI Express™, system board, or any other form factor. Such form factors are covered in other separate specifications. show less

PCI Express External Cabling Specification Revision 2.0 with Change Bar

This is a companion specification to the PCI Express...view more This is a companion specification to the PCI Express Base Specification. Its primary focus is the implementation of cabled PCI Express®. The discussions are confined to copper cabling and their connector requirements to meet the PCI Express signaling needs at 5.0 GT/s. No assumptions are made regarding the implementation of PCI Express compliant Subsystems on either side of the cabled Link; e.g., PCI Express Card Electromechanical (CEM), ExpressCard5™, ExpressModule™, PXI Express™, system board, or any other form factor. Such form factors are covered in other separate specifications. show less

2.x Specification June 22, 2012

Combined Antenna Tuning/Coexistence Signal ECR

Modify the PCI Express Mini Card specification to de...view more Modify the PCI Express Mini Card specification to define a new interface for tunable antennas. Modify the PCI Express Mini Card specification to enable existing coexistence signals to operate simultaneously with new tuneable antenna control signals. show less

2.x ECN May 31, 2012

PCI Express Mini Card Electromechanical Specification Revision 2.0 with Change Bar

This specification defines an implementation for sma...view more This specification defines an implementation for small form factor PCI Express cards. The specification uses a qualified sub-set of the same signal protocol, electrical definitions, and configuration definitions as the PCI Express Base Specification, Revision 2.0. Where this specification does not explicitly define PCI Express characteristics, the PCI Express Base Specification governs. show less

2.x Specification April 21, 2012

PCI Express Mini Card Electromechanical Specification Revision 2.0

This specification defines an implementation for sma...view more This specification defines an implementation for small form factor PCI Express cards. The specification uses a qualified sub-set of the same signal protocol, electrical definitions, and configuration definitions as the PCI Express Base Specification, Revision 2.0. Where this specification does not explicitly define PCI Express characteristics, the PCI Express Base Specification governs. show less

2.x Specification April 21, 2012

Errata for the PCI Express Base Specification Revision 2.1

2.x Errata November 18, 2010

CEM Support Power

ECR covers proposed modification of Section 4.2 Pow...view more ECR covers proposed modification of Section 4.2 Power Consumption within the CEM Specification version 2.0. show less

2.x ECN September 8, 2009

ASPM Optionality

Prior to this ECN, all PCIe external Links were requ...view more Prior to this ECN, all PCIe external Links were required to support ASPM L0s. This ECN changes the Base Specification to permit ASPM L0s support to be optional unless the applicable formfactor specification explicitly requires it. show less

2.x ECN August 20, 2009

Optimized Buffer Flush/Fill

This ECR proposes to add a new mechanism for platfor...view more This ECR proposes to add a new mechanism for platform central resource (RC) power state information to be communicated to Devices. This mechanism enables Optimized Buffer Flush/Fill (OBFF) by allowing the platform to indicate optimal windows for device bus mastering & interrupt activity. Devices can use internal buffering to shape traffic to fit into these optimal windows, reducing platform power impact. show less

2.x ECN April 30, 2009

PCI Express Base Specification Revision 2.1

This specification describes the PCI Express® archit...view more This specification describes the PCI Express® architecture, interconnect attributes, fabric management, and

2.x Specification March 4, 2009

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the programming interface required to design and build systems and peripherals that are compliant with the PCI Express Specification. show less			
PCI Express Base Specification Revision 2.1 with Change Bar			
This specification describes the PCI Express® archit... view more This specification describes the PCI Express® architecture, interconnect attributes, fabric management, and the programming interface required to design and build systems and peripherals that are compliant with the PCI Express Specification. show less	2.x	Specification	March 4, 2009
Errata for the PCI Express Base Specification Revision 2.0			
TLP Prefix			
Emerging usage model trends indicate a requirement f... view more Emerging usage model trends indicate a requirement for increase in header size fields to provide additional information than what can be accommodated in currently defined TLP header sizes. The TLP Prefix mechanism extends the header size by adding DWORDS to the front of headers that carry additional information. show less	2.x	ECN	December 15, 2008
System Board Eye Height Specification Update			
This ECN modifies the system board transmitter path ... view more This ECN modifies the system board transmitter path requirements (VTXS and VTXS_d) at 5 GT/s. As a consequence the minimum requirements for the add-in card receiver path sensitivity at 5 GT/s are also updated. show less	2.x	ECN	December 5, 2008
TLP Processing Hints			
This optional normative ECR defines a mechanism by w... view more This optional normative ECR defines a mechanism by which a Requester can provide hints on a per transaction basis to facilitate optimized processing of transactions that target Memory Space. The architected mechanisms may be used to enable association of system processing resources (e.g. caches) with the processing of Requests from specific Functions or enable optimized system specific (e.g. system interconnect and Memory) processing of Requests. show less	2.x	ECN	September 11, 2008
Extended Tag Enable Default			
The change allows a Function to use Extended Tag fie... view more The change allows a Function to use Extended Tag fields (256 unique tag values) by default; this is done by allowing the Extended Tag Enable control field to be set by default. show less	2.x	ECN	September 5, 2008
PCI Express Architecture Configuration Space Test Specification Revision 2.0			
This document primarily covers PCI Express testing o... view more This document primarily covers PCI Express testing of root complexes, switches, bridges, and endpoints for the standard configuration mechanisms, registers, and features in Chapter 7 of the PCI Express Base Specification, Revision 2.0. This specification does not describe the full set of PCI Express tests and assertions for these devices. show less	2.x	Specification	August 25, 2008
Latency Tolerance Reporting			
This ECR proposes to add a new mechanism for Endpoin... view more This ECR proposes to add a new mechanism for Endpoints to report their service latency requirements for Memory Reads and Writes to the Root Complex such that central platform resources (such as main memory, RC internal interconnects, snoop resources, and other resources associated with the RC) can be power managed without impacting Endpoint functionality and performance. show less	2.x	ECN	August 14, 2008
PCI Express Architecture Transaction Layer Test Specification Revision 2.0			
This document contains a list of Test Assertions and... view more This document contains a list of Test Assertions and a set of Test Definitions pertaining to the Transaction Layer. Assertions are statements of spec requirements which are measured by the algorithm details as specified in the Test Definitions. “Basic Functional Tests” are Test Algorithms which perform basic tests for key elements of Transaction Layer device functionality. This document does not describe a full set of PCI Express tests and assertions and is in no way intended to measure products for full design validation. Tests described here should be viewed as tools to checkpoint the result of product validation – not as a replacement for that effort. show less	2.x	Specification	August 11, 2008

Specification Title	Spec Rev	Document Type	Release Date
ID-Based Ordering This ECN proposes to add a new ordering attribute wh...view more This ECN proposes to add a new ordering attribute which devices may optionally support to provide enhanced performance for certain types of workloads and traffic patterns. The new ordering attribute relaxes ordering requirements between unrelated traffic by comparing the Requester/Completer IDs of the associated TLPs. show less	2.x	ECN	May 29, 2008
Dynamic Power Allocation DPA (Dynamic Power Allocation) extends existing PCIe...view more DPA (Dynamic Power Allocation) extends existing PCIe device power management to provide active (D0) device power management substates for appropriate devices, while comprehending existing PCIe PM Capabilities including PCI-PM and Power Budgeting. show less	2.x	ECN	May 24, 2008
Multicast This optional normative ECN adds Multicast functiona...view more This optional normative ECN adds Multicast functionality to PCI Express by means of an Extended Capability structure for applicable Functions in Root Complexes, Switches, and components with Endpoints. The Capability structure defines how Multicast TLPs are identified and routed. It also provides means for checking and enforcing send permission with Function-level granularity. The ECN identifies Multicast errors and adds an MC Blocked TLP error to AER for reporting those errors. show less	2.x	ECN	May 8, 2008
Resizable BAR Capability This optional ECN adds a capability for Functions wi...view more This optional ECN adds a capability for Functions with BARs to report various options for sizes of their memory mapped resources that will operate properly. Also added is an ability for software to program the size to configure the BAR to. show less	2.x	ECN	April 24, 2008
Internal Error Reporting PCI Express (PCIe) defines error signaling and loggi...view more PCI Express (PCIe) defines error signaling and logging mechanisms for errors that occur on a PCIe interface and for errors that occur on behalf of transactions initiated on PCIe. It does not define error signaling and logging mechanisms for errors that occur within a component or are unrelated to a particular PCIe transaction. show less	2.x	ECN	April 24, 2008
Atomic Operations This optional normative ECN defines 3 new PCIe trans...view more This optional normative ECN defines 3 new PCIe transactions, each of which carries out a specific Atomic Operation ("AtomicOp") on a target location in Memory Space. The 3 AtomicOps are FetchAdd (Fetch and Add), Swap (Unconditional Swap), and CAS (Compare and Swap). FetchAdd and Swap support operand sizes of 32 and 64 bits. CAS supports operand sizes of 32, 64, and 128 bits. show less	2.x	ECN	April 17, 2008
Alternative Routing-ID Interpretation (ARI) For virtualized and non-virtualized environments, a ...view more For virtualized and non-virtualized environments, a number of PCI-SIG member companies have requested that the current constraints on number of Functions allowed per multi-Function Device be increased to accommodate the needs of next generation I/O implementations. This ECR specifies a new method to interpret the Device Number and Function Number fields within Routing IDs, Requester IDs, and Completer IDs, thereby increasing the number of Functions that can be supported by a single Device. show less	2.x	ECN	June 4, 2007
PCI Express Card Electromechanical Specification Revision 2.0 This specification is a companion for the PCI Expres...view more This specification is a companion for the PCI Express Base Specification, Revision 2.0. Its primary focus is the implementation of an evolutionary strategy with the current PCI™ desktop/server mechanical and electrical specifications. The discussions are confined to ATX or ATX-based form factors. Other form factors, such as PCI Express® Mini Card are covered in other separate specifications. show less	2.x	Specification	April 11, 2007
PCI Express Card Electromechanical Specification Revision 2.0 with Change Bar This specification is a companion for the PCI Expres...view more This specification is a companion for the PCI Express Base Specification, Revision 2.0. Its primary focus is the	2.x	Specification	April 11, 2007

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implementation of an evolutionary strategy with the current PCI™ desktop/server mechanical and electrical specifications. The discussions are confined to ATX or ATX-based form factors. Other form factors, such as PCI Express® Mini Card are covered in other separate specifications. [show less](#)

[PCI Express Base Specification Revision 2.0](#)

This specification describes the PCI Express® architecture, interconnect attributes, fabric management, and the programming interface required to design and build systems and peripherals that are compliant with the PCI Express Specification. [show less](#)

2.x

Specification

December
20, 2006

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