

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANALOG DEVICES, INC.,
Petitioner,

v.

NUMBER 14 B.V.,
Patent Owner.

IPR2025-00550
U.S. Patent 7,973,596

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 7,973,596

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Exhibits

Exhibit Number	Description
Ex. 1001	U.S. Patent No. 7,973,596 B2 to Eschauzier <i>et al.</i> (“the ’596 patent”)
Ex. 1002	Prosecution History of the ’596 patent
Ex. 1003	Declaration of Dr. Ion Opris
Ex. 1004	Curriculum Vitae of Dr. Ion Opris
Ex. 1005	U.S. Patent No. 6,734,723 to Huijsing (“Huijsing”)
Ex. 1006	U.S. Patent No. 6,476,671 to Tang (“Tang”)
Ex. 1007	I. Opris <i>et al.</i> , <i>A Rail-to-Rail Ping-Pong Op-Amp</i> , IEEE Journal of Solid-State Circuits, vo. 31, no. 9, September 1996
Ex. 1008	A. Tang, <i>A 3μV-Offset Operational Amplifier with 20nV/vHz Input Noise PSD at DC Employing both Chopping and Autozeroing</i> , IEEE International Solid-State Circuits Conference, 2002 (“TangPaper”)
Ex. 1009	Reserved
Ex. 1010	C. Enz <i>et al.</i> , <i>Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization</i> , Proceedings of the IEEE, Vol. 84, No. 11, November 1996 (“Enz”)
Ex. 1011	US. Patent No. 7,834,685 to Pertijs (“Pertijs”)

MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner is a real party-in-interest. Maxim Integrated Products, Inc. is also a real party-in-interest. No other party had access to or control over the filing of this Petition and Petitioner did not file this Petition for the benefit of any other entity.

B. Related Matters (37 C.F.R. §42.8(b)(2))

The '596 patent is involved in *Number 14 B.V. v. Analog Devices, Inc. and Maxim Integrated Products, Inc.*, 5:24-cv-02435-EJD (Apr. 24, 2024 NDCA). This is a licensing dispute, not a patent infringement case.

C. Lead and Back-Up Counsel (37 C.F.R. §42.8(b)(3))

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Petitioner consents to electronic service at the email addresses listed above.

I. INTRODUCTION

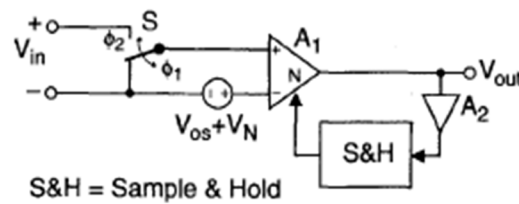
Petitioner requests *inter partes* review and cancellation of claims 21 and 22 of U.S. Patent No. 7,973,596 (“the ’596 Patent”) (Ex. 1001).

II. TECHNOLOGY OF THE ’596 PATENT

A. Technological Overview

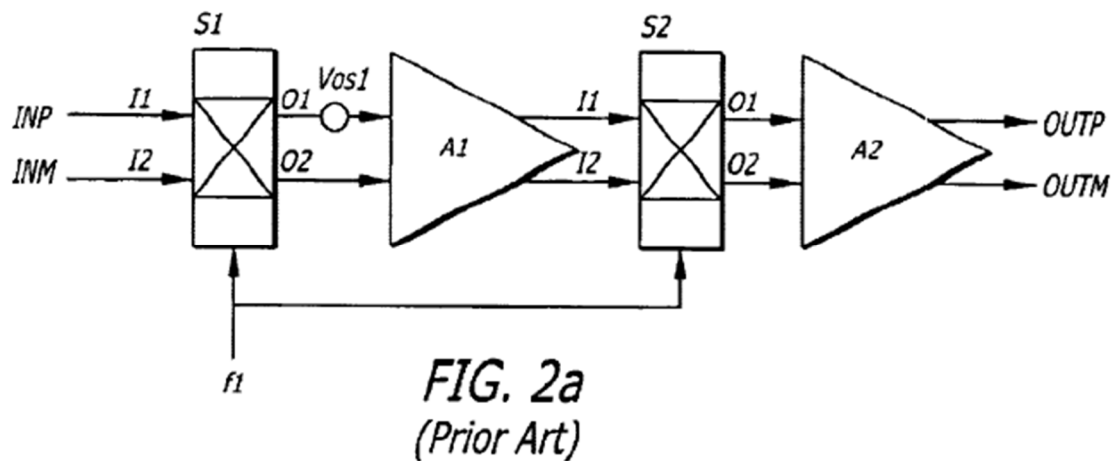
Amplifiers, and operational amplifiers (“opamp”) in particular, exhibit input voltage offsets due to technological imperfections in the circuit. Ex. 1005, 1:38-46; Ex. 1003, ¶51. Input voltage offsets (sometimes referred to as input referred offset voltage, input offset, offset voltage, or offset) refers to the mismatch between different components in a circuit, causing the circuit to not function in the intended manner. Ex. 1001, 1:21-24. Input voltage offsets manifest as an error in an amplifier output equal to the input offset times the gain between the input and the system out. Ex. 1005, 1:28-35; Ex. 1003, ¶50. As acknowledged by the ’596 Patent, various solutions known prior to the ’596 Patent counteracted voltage offsets, including chopper stabilization and auto-zeroing. Ex. 1001, 1:29-36.

In essence, auto-zeroing techniques periodically sample the effects of a voltage offset from an amplifier with shorted differential inputs and uses the sampled voltage offset to subtract from the output signal at each stage. Ex. 1011, 4:5-7. An example structure of an auto-zeroing system is provided below:



Ex. 1010 Fig. 1(a); Ex. 1003, ¶54. An auto-zeroing stage (e.g., the S&H block shown above) may include one or more capacitors and a transconductance stage. Ex. 1006, Fig. 2a; Ex. 1010, Fig. 2a; Ex. 1011, 4:12-20; Ex. 1003, ¶54. When the differential inputs of the amplifier (plus and minus terminals depicted above) are shorted, the capacitor will store the potential difference caused by the voltage offset, and the transconductance stage will be coupled to the amplifier to compensate or counteract for this voltage offset. Ex. 1003, ¶55. Other circuit designs may use alternative components to perform similar functions, like one or more switches rather than comparator A₂, for example. Ex. 1001, Fig. 3 (Applicant Admitted Prior Art); Ex. 1006, Fig. 2a; Ex. 1011, Fig. 1.

Another system to reduce voltage offset is chopper stabilization, also known before the filing of the '596 Patent. As acknowledged by the '596 Patent, “chopper stabilization relies on periodically swapping the signal paths for the negative and positive input terminals of the amplifier[,]” which “causes the offset between the two terminals to even out.” Ex. 1001, 1:42-45; *see also*, Ex. 1005, 1:53-60; Ex. 1006, 1:54-58; Ex. 1011, 4:46-51; Ex. 1003, ¶52. An example chopper stabilization system is depicted below:



Ex. 1005, Fig. 2a. Here, the amplifier A1 is chopper stabilized by choppers S1 and S2. Ex. 1003, ¶52. The signal through amplifier A1 is periodically twice inverted (being inverted by chopper S1 before the input of A1 and again inverted after the output of A1 by chopper S2) but the effect of the voltage offset is only once inverted periodically. Ex. 1005, 1:60-63; Ex. 1003, ¶52. This way, the effect of the voltage offset averages out to zero over time. Ex. 1003, ¶52.

B. The '596 Patent

The '596 Patent describes and claims an amplifier using both chopping and auto-zeroing. See, Ex. 1001, Cl. 21-22, 5:49-52; Ex. 1003, ¶76. Figure 5 of the '596 Patent describes an exemplary system which employs both chopping and auto-zeroing:

[illegible]

The embodiments and methods of the '596 Patent are nothing more than simple and obvious combinations of the known methods of chopping and auto-zeroing, each operating in a predictable manner according to their known features to produce a predictable outcome. *See generally*, Ex. 1006, Fig. 2a, 3:54-58, 4:24-37;

Ex. 1011, Fig. 1, 2:32-35. Moreover, the combination of these two (chopping and auto-zeroing) in the same system was known before the '596 Patent. *Id.*

C. Prosecution History

The '596 Patent was filed as Application No. 12/464,572, on May 12, 2009. Challenged Claims 21 and 22, were originally filed as Original Claims 26 and 27 respectively, and depended from original (independent) Claim 24. Ex. 1002, 104-105. As filed Original Claim 24 claimed auto-zeroing and chopping, performed at unequal frequencies, where the chopper stabilization frequency and an auto-zeroing frequency have a two to one ratio. Ex. 1002, 104.

During prosecution, the Examiner rejected original claims 24 to 28 (including the two claims challenged in this Petition) as being obvious over *Huijsing* (Ex. 1005). Ex. 1002, 247-249. The Examiner found that it would have been obvious to “implement the circuit wherein the second frequency being twice the first frequency and the first and second frequencies each have a 50% duty cycle or the first frequency is twice the second frequency[.]” Ex. 1002, 249. However, *Huijsing* did not expressly have these two frequency limitations.

The Applicant canceled independent Claim 24 and amended Original Claims 26-28 to be independent and include all limitations from Original Claim 24 (along with insignificant rewording). Ex. 1002, 263-264. Applicants stated “[c]laim 26 includes the limitation that the second frequency is twice the first frequency and has

a duty cycle of less than one half, whereas claim 27 is similar, though requires that the second frequency have a duty cycle of not more than one quarter, neither of which limitations is disclosed or rendered obvious by the cited art.” Ex. 1002, 268; Ex. 1003, ¶77.

The Examiner issued a notice of allowance without further rejections or objections to these claims. Ex. 1002, 277. The Petition relies on two references, *Pertijs* and *Tang*, not considered by the Examiner; each independently teaches the limitations that Applicants argued distinguished the claims from the prior art during prosecution. Ex. 1003, ¶¶56, 77.

III. GROUNDS FOR STANDING (37 C.F.R. §42.8(B)(1))

Petitioner certifies (1) the ’596 Patent is available for IPR; (2) Petitioner is not barred or estopped from requesting an IPR on the Grounds identified herein; and (3) Petitioner has not filed a complaint relating to the ’596 Patent. This Petition is filed in accordance with 37 C.F.R. § 42.106(a).

IV. PAYMENT OF FEES 37 C.F.R. (§§ 42.15 AND 42.103)

Petitioner authorizes the USPTO to charge any required fees to Deposit Account 02-1818.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) is a hypothetical person who is presumed to know the relevant prior art. *See Gnosis S.P.A et al. v. S. Ala. Med.*

Sci. Foundation, Case IPR2013-00116, Paper 68 at 9, 37 (PTAB June 20, 2014). A POSITA has ordinary creativity, is not an automaton, and is capable of combining teachings of the prior art. *Id.* (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420-421 (2007)).

A POSITA with respect to the ’596 patent would have possessed at least a four-year degree in electrical engineering or a closely related field and at least two years of experience in the design of analog integrated circuits. Ex. 1003, ¶¶47-49. Additional education could substitute for professional experience and vice versa. Ex. 1003, ¶49.

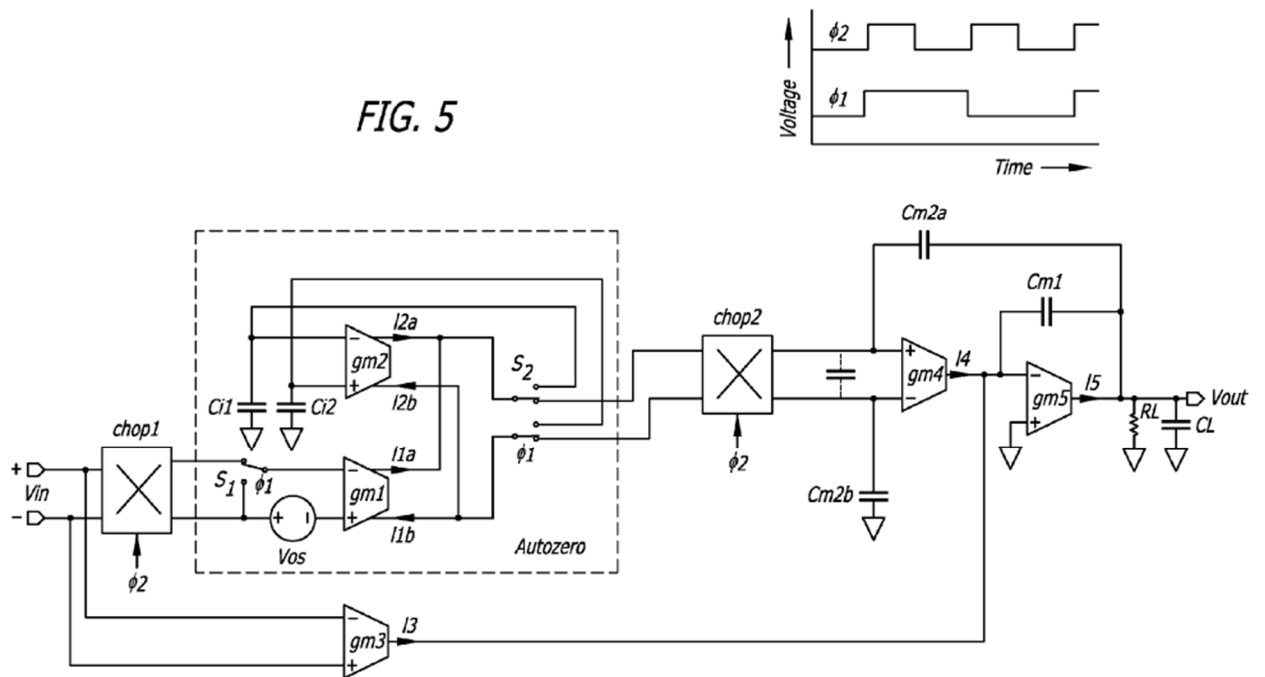
VI. CLAIM CONSTRUCTION

The Board construes claims using the standard of *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *CUPP Comput. AS v. Trend Micro Inc.*, 53 F.4th 1376, 1380 (Fed. Cir. 2022). According to this standard, claim terms receive their ordinary and customary meaning as would have been understood by one of ordinary skill in the art in light of the specification, prosecution history, and extrinsic evidence. *Phillips*, 415 F.3d at 1314-19. Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

A. “operating the chopper stabilization at a first frequency” and “operating the auto-zeroing at a second frequency”

The frequencies that chopper stabilization and auto-zeroing occur at are not expressly defined in the '596 Patent but are instead explained through examples relating the two frequencies, including in the figures. Ex. 1003, ¶79. The “first frequency,” which is the chopper stabilization frequency, should be construed as “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle.” Ex. 1003, ¶80. Likewise, the “second frequency,” which is the auto-zeroing frequency, should be construed as “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle.” Ex. 1003, ¶81.

A POSITA viewing Fig. 5 would understand that the chopper stabilizers operate at a first frequency defined by clock phase Φ_2 , while the auto-zeroing operates at a second frequency defined by clock phase Φ_1 :

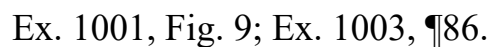


Ex. 1001, Fig. 5, 5:58-65; Ex. 1003, ¶82.

When Φ_1 is high (i.e., the pulse is “on” and voltage is applied, thereby closing switch S_1), input stage g_{m1} enters auto-zero mode; when Φ_1 is low (i.e., the pulse is “off” and voltage is removed, thereby opening the switch), the input stage g_{m1} enters normal operation while the output current is compensated for by g_{m2} . Ex. 1001, 5:55-60; Ex. 1003, ¶83. Meanwhile, the choppers chop₁ and chop₂ are controlled by Φ_2 . Ex. 1001, 5:60-65; Ex. 1003, ¶84.

Fig. 5 also depicts “the auto-zero clock phase Φ_1 , running at *half* the chopping frequency f_{chop} .” Ex. 1001, 6:60-63; Ex. 1003, ¶85. This is because in the auto-zeroing clock phase Φ_1 has one pulse in the time it takes its pulse pattern Φ_1 to repeat (i.e., one period of the signal), while the chopper stabilization clock phase Φ_2 has

Consistently, in Fig. 9, another timing arrangement is proposed:



10

pattern Φ_2 to repeat, while the auto-zeroing clock phase Φ_1 has one pulse in the time it takes its pulse pattern Φ_1 to repeat, and the Φ_1 repeats two times in the time it takes the Φ_2 pulse pattern to repeat once (i.e., a full auto-zeroing cycle is half the duration of the chopper stabilization cycle). Ex. 1003, ¶87.

Notably, the chopper stabilization frequency is not described in these examples with respect to the individual switches that may be utilized in the chopper stabilizers. However, the '596 Patent describes the inner workings of the chopper stabilizers in Fig. 11, an alternative embodiment of Fig. 9, where the chopper stabilizers are implemented as array of switches:

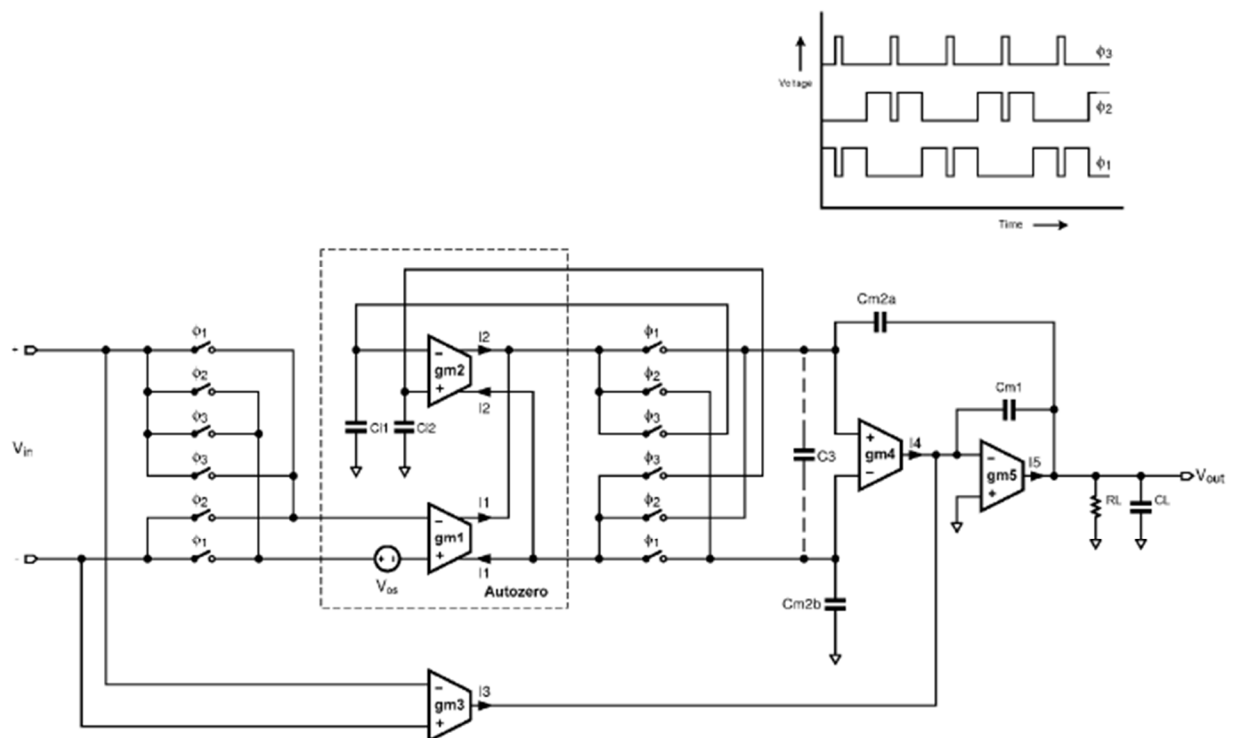
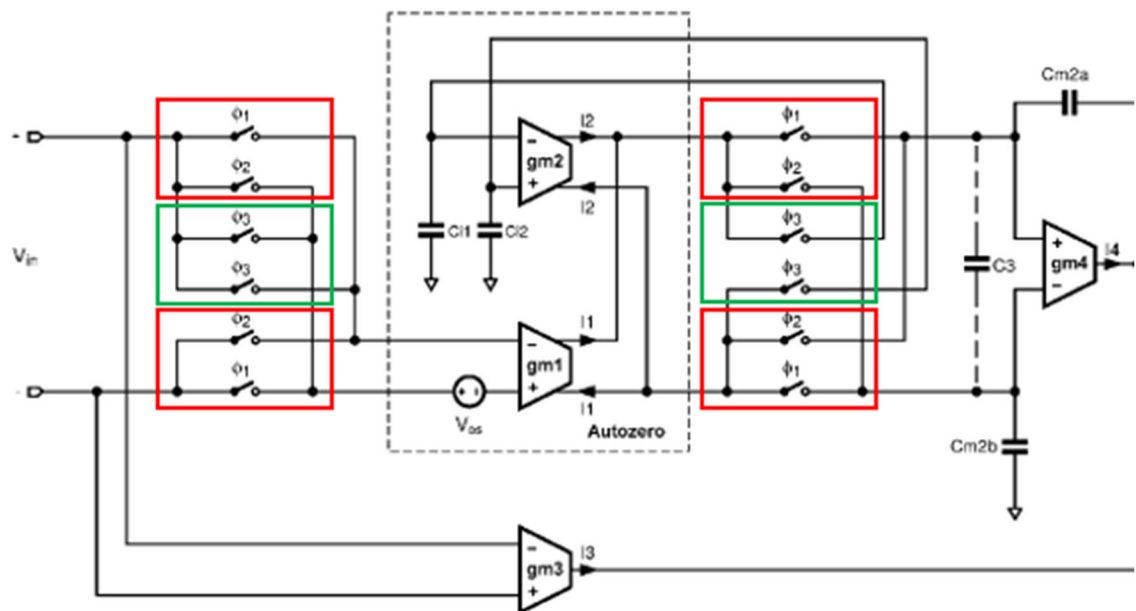


Fig. 11

Ex. 1001, Fig. 11, 7:25; Ex. 1003, ¶88.

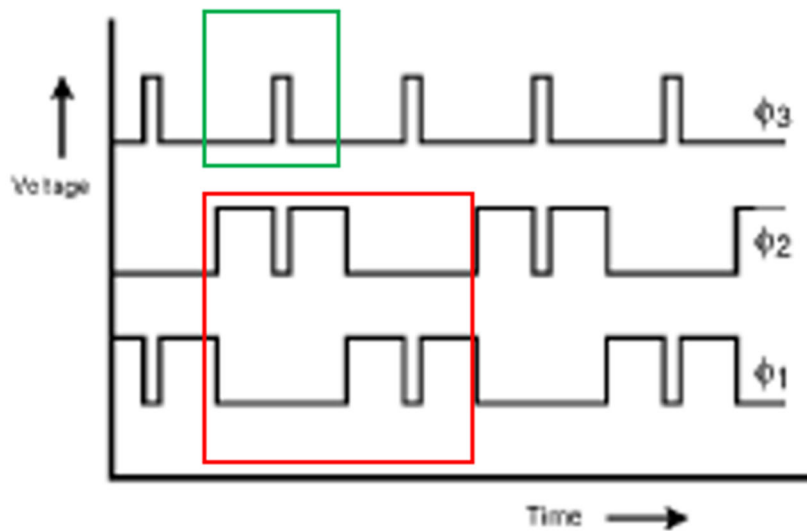
The switches controlled by Φ_3 are used to short the amplifier inputs and perform auto-zeroing. Ex. 1001, 7:32-38; Ex. 1003, ¶89. Meanwhile the switches controlled by Φ_1 and Φ_2 are used to invert the polarities of the input and output of the amplifier, performing chopper stabilization. Ex. 1001, 7:40-62; Ex. 1003, ¶89. Below, the chopping switches are shown in red and the auto-zeroing switches are shown in green:



Ex. 1001, Fig. 11¹; Ex. 1003, ¶89.

The specific timing arrangement is annotated below:

¹ All color annotations in figures are provided by Petitioner.



Ex. 1001, Fig. 11; Ex. 1003, ¶90.

Like Fig. 9, Fig. 11 has an auto-zeroing frequency operating at twice the chopping frequency. Ex. 1001, 6:60-63; 7:58-62. For example, Φ_3 has a pulse pattern (with one active pulse) annotated in green. After the green box ends, the pulse pattern repeats. Ex. 1003, ¶91. Likewise, Φ_1 and Φ_2 have a pulse pattern (with one active pulse each) annotated in red. Ex. 1003, ¶92. After the red box ends, the pulse pattern of Φ_1 and Φ_2 repeats. Ex. 1003, ¶92. While in the red period it appears that two pulses occur in Φ_1 and Φ_2 , that is not the case—instead “each half cycle of the chopping [is] temporarily interrupted by the auto-zeroing process.” Ex. 1001, 7:58-62. Therefore, both switches for the chopping stabilization system have one active pulse over the duration of its cycle period (shown in red) and the active pulse is interrupted halfway through. Ex. 1003, ¶92. Said otherwise, this pulse pattern (the active pulse with small interruption) repeats on a periodic basis, but it is the full

duration of the pattern, not the sub-spike, that defines the cycle. Ex. 1001, 7:58-62.

The switches for auto-zeroing also have one pulse over the duration of the auto-zeroing cycle (shown in green), but the auto-zeroing cycle repeats after only half of the chopping cycle has been completed. As a result, a POSITA would understand that, in Fig. 11, there is an auto-zeroing frequency operating at twice the chopping frequency. Ex. 1001, 6:60-63, 7:58-62; Ex. 1003, ¶93.

These frequency terms are not defined in the specification, but consistent with the manner in which the terms are used in the examples in the specification, a POSITA would understand the “first frequency” (the chopper stabilization frequency), to mean “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle” and, the “second frequency” (the auto-zeroing frequency) to mean “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle.” Ex. 1003, ¶94.

B. “the ratio of the two frequencies being two to one” [claim 22]

There is no antecedent basis for the term “the ratio[]” in Claim 22. Ex. 1001, Cl. 22. For the purposes of this Petition, this term should be construed as requiring a ratio between the two (first and second) frequencies, such that either the second frequency (i.e. the auto-zero frequency) be twice the first frequency (i.e. the chopper frequency), or the first frequency (the chopper frequency) being twice the second frequency (the auto-zero frequency). Ex. 1003, ¶95. This interpretation is consistent

with the specification of the '596 Patent. Ex. 1001, 6:61-62 (“Instead of the auto-zero clock phase Φ_1 , running at half the chopping frequency f_{chop} , it now operates at twice the chopping frequency f_{chop} .”); *see also*, Ex. 1001, Fig. 5, Fig. 9; Ex. 1003, ¶95.

Although this limitation is also included in Claim 21, this construction is not necessary for Claim 21. Ex. 1003, ¶96. Claim 21 includes an additional subsequent limitation that “the second frequency [is] twice the first frequency[,]” which excludes an embodiment where the second frequency (auto-zero frequency) is running at one half the first frequency (chopping frequency).

VII. STATEMENT OF PRECISE RELIEF REQUESTED

Petitioner requests the institution of IPR and cancellation of the Challenged Claims on the Grounds outlined in the table below.

Ground	Challenged Claims	Basis	Prior Art
I	21, 22	§ 103	U.S. Patent No. 7,834,685 (<i>Pertijs</i>)
II	22	§ 103	U.S. Patent No. 6,476,671 (<i>Tang</i>)

Petitioner provides the declaration of Dr. Ion Opris (Ex. 1003), an expert in the field of the '596 Patent and the prior art, in support of these Grounds. Ex. 1003, ¶¶7-21, 65; Ex. 1004; *see*, Ex. 1007; Ex. 1008, Footnote 5 (citing Dr. Opris).

VIII. GROUND I: *PERTIJS* RENDERS CLAIM 21 OBVIOUS

A. Overview

The '596 Patent describes a purportedly “alternative approach that combines the advantages of chopping and autozeroing” and in a circuit where an “autozeroed input stage... is ‘embedded’ between two choppers[.]” Ex. 1001, 5:49-55. *Pertijs* predates the '596 Patent and describes “[a]n apparatus including a plurality of amplifier stages” where “[e]ach amplifier stage also includes an auto-zeroing loop” and “[e]ach amplifier stage further includes chopping circuitry.” Ex. 1011, Abstract; *see also* Ex. 1011 2:32-33 (“Fig. 1 illustrates a first example chopped auto-zeroed ping-pong amplifier 100 according to this disclosure”); Ex. 1003, ¶57. *Pertijs* teaches or at least renders obvious each element of claims 21 and 22.

1. Pertijs

Pertijs was filed on filed Oct. 15, 2008 and issued as U.S. Patent No. 7,834,685 on November 16, 2010. Ex. 1011, Title Page. Accordingly, *Pertijs* is prior art under 35 U.S.C. § 102(e), and was not previously considered by the Examiner.

Pertijs describes a ping-pong amplifier which includes both chopping and auto-zeroing circuitry. Ex. 1011, 2:32-33; Ex. 1003, ¶¶57-60. Fig. 1, depicts an amplifier 100 in a ping-pong structure:

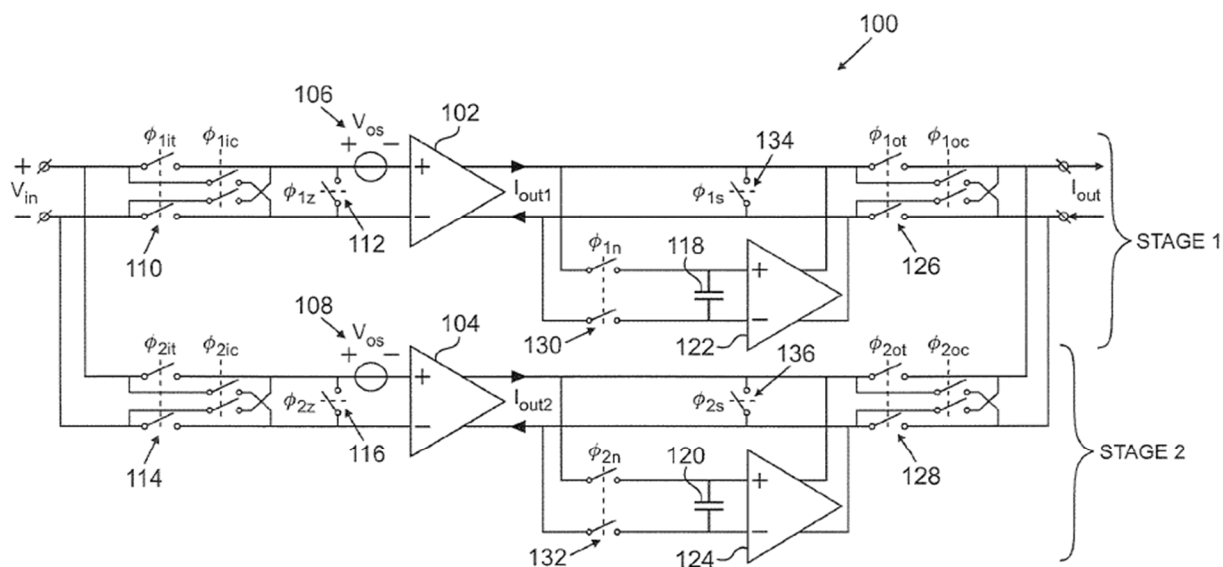


FIG. 1

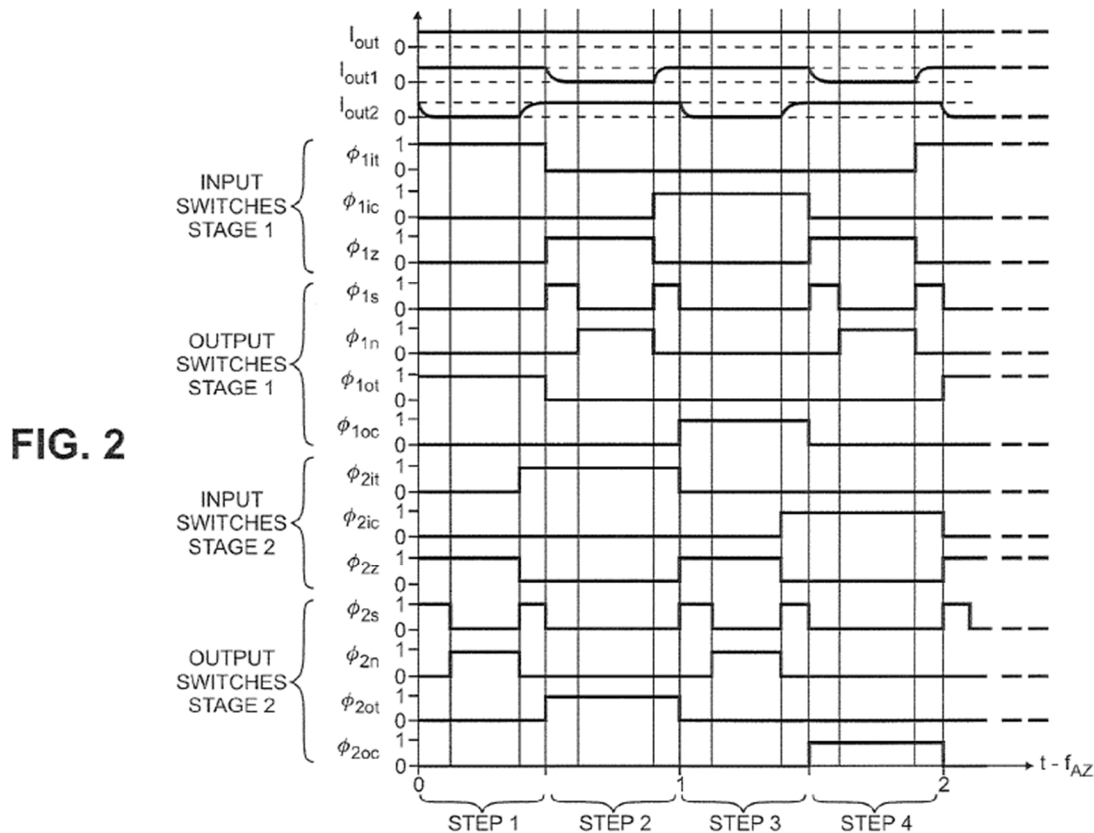
Ex. 1011, Fig. 1, 2:32-35; Ex. 1003, ¶57. The ping-pong amplifier includes transconductance amplifiers 102 and 104, a plurality of switches 110, 114, 126, 128 112, 116, 130, 132, 134, 136, differential capacitors 118, 120, and additional transconductance stages 122, 124 which function to provide both auto-zeroing and chopper stabilization. Ex. 1011, 2:54-3:3, 3:43-48, 4:5-30 4:17-20, 4:5-30; Ex. 1003, ¶¶58-60.

Switches 110, 114, 126, 128 perform chopper stabilization. Ex. 1011, 4:44-51; Ex. 1003, ¶58. Switches 110, 114, 126, and 128 provide chopping functionality by switching the polarity of the inputs and outputs of the transconductance stages 102, 104. Ex. 1011, 2:56-58, 3:1-3, 3:28-32; Ex. 1003, ¶58.

Meanwhile, the differential capacitors 118, 120 and additional

transconductance stages 122, 124, and switches 112, 116 perform auto-zeroing cycles. Ex. 1011, 4:5-30; Ex. 1003, ¶59. Switches 112, 116 short the inputs to the transconductance stages 102, 104; while switches 130, 132 provide current to capacitors 118, 120 and transconductance stages 122, 124 to auto-zero the outputs from transconductance stages 102, 104. Ex. 1011, 2:65-3:3, 4:12-20; Ex. 1003, ¶59.

In *Pertijs*, the auto-zeroing cycles and chopping cycles of the ping-pong amplifier operate according to the clock signals depicted in Fig. 2:



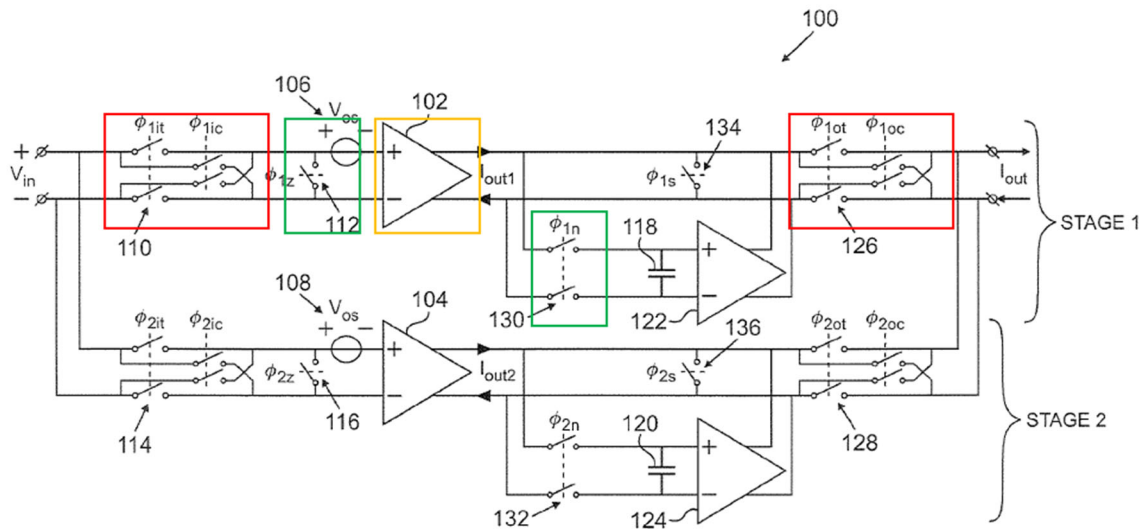
Ex. 1011, Fig. 2, 3:51-52; Ex. 1003, ¶61. As depicted, in step 1, transconductance stage 102 provides an uninverted output, while transconductance

stage 104 is auto-zeroed. Ex. 1011, 4:54-56; Ex. 1003, ¶¶62-63. In step 2, the transconductance stage 104 provides an uninverted output while the transconductance stage 12 is auto-zeroed. Ex. 1011, 4:57-59; Ex. 1003, ¶¶62-63. Steps 3 and 4 repeat steps 1 and 2 except for the transconductance stage 102 and 104 are twice inverted during step 3 and step 4 respectively. Ex. 1011, 4:60-65; Ex. 1003, ¶¶62-63.

B. Independent Claim 21

- 1. [21pre] A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:**

To the extent it is limiting, *Pertijs* renders the preamble of claim 21 obvious. Ex. 1003, ¶97. *Pertijs* provides a “chopped auto-zeroed ping-pong amplifier[.]” Ex. 1011, 2:32-35. *Pertijs* provides a circuit diagram with multiple transconductance amplifiers, including the claimed first amplifier (annotated in yellow) and switches which provide chopper stabilization (in red) and auto-zeroing capabilities (in green):

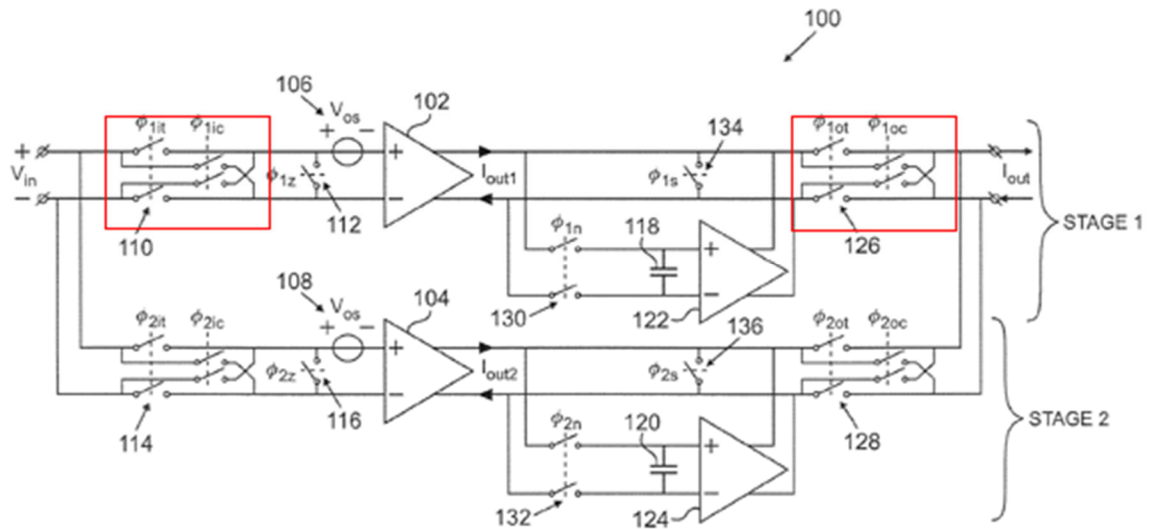


Ex. 1011, Fig. 1; Ex. 1003, ¶98. The switches 110 and 126 chopper stabilize the transconductance amplifier 102, while the capacitor 118 and additional transconductance stage 122 performs auto-zeroing. Ex. 1011, 3:59-63; Ex. 1003, ¶¶99-100. While the same structure is provided in Stage 2, Stage 1 alone is sufficient to render this limitation obvious. Ex. 1011, 2:38-45, 3:1-3, 4:29-30; Ex. 1003, ¶99.

2. [21a] operating the chopper stabilization at a first frequency; and

Pertijs renders this limitation obvious. Ex. 1003, ¶101. The chopper stabilization frequency is “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle.” Ex. 1003, ¶102; *supra* Section VI.A.

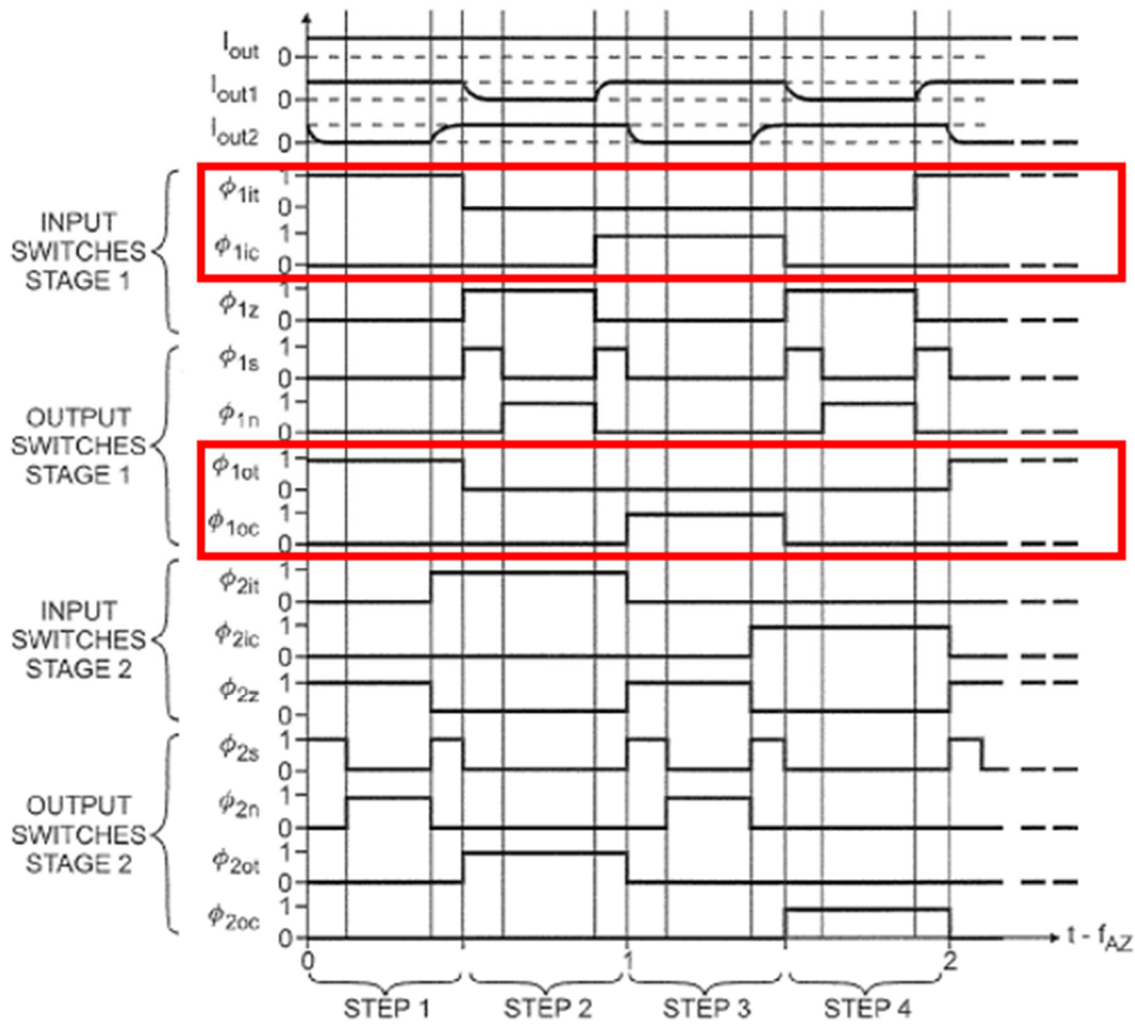
In *Pertijs*, chopper stabilization is performed on the first amplifier by switches 110 and 126 which invert the polarities of the inputs and outputs respectively:



Ex. 1011, Fig. 1, 3:59-61; Ex. 1003, ¶103. By inverting the polarities of the input voltage and the output signal, switches 110, 126 perform chopper stabilization.

Ex. 1003, ¶103.

The chopper stabilization occurs at a first frequency of one chopper stabilization cycle over the period of Step 1 through Step 4. Ex. 1011, Fig. 2; Ex. 1003, ¶108. For example, Fig. 2 depicts the clock signals used to control each switch (annotated in red), which depict switches 110 (clock signals Φ_{1it} , Φ_{1ic}) and 126 (clock signals Φ_{1ot} and Φ_{1oc}) inverting the polarity of transconductance amplifier 102 at a given frequency:

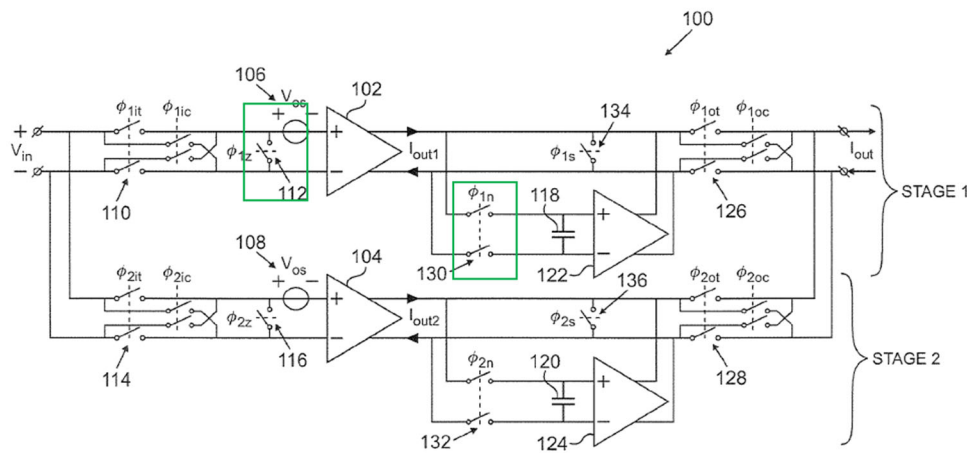


Ex. 1011, Fig. 2; Ex. 1003, ¶104. Here, transconductance amplifier 102 is in a first uninverted state at Step 1, and in a second twice inverted state at Step 3. Ex. 1011, 4:54-56. 4:60-63; Ex. 1003, ¶¶105-106. Each individual switch of the input switches 110 and output switches 126 (*i.e.*, the switches controlled by clock signals Φ_{1it} , Φ_{1ic} , Φ_{1ot} , and Φ_{1oc}) include one pulse in a full cycle (which does not repeat until after STEP 4). Ex. 1003, ¶107. Thus, the first frequency is $1/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$. Ex. 1003, ¶108.

3. [21b] operating the auto-zeroing at a second frequency;

Pertijs renders this limitation obvious. Ex. 1003, ¶109. The auto-zeroing frequency is “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle.” Ex. 1003, ¶110; *see supra* Section VI.A.

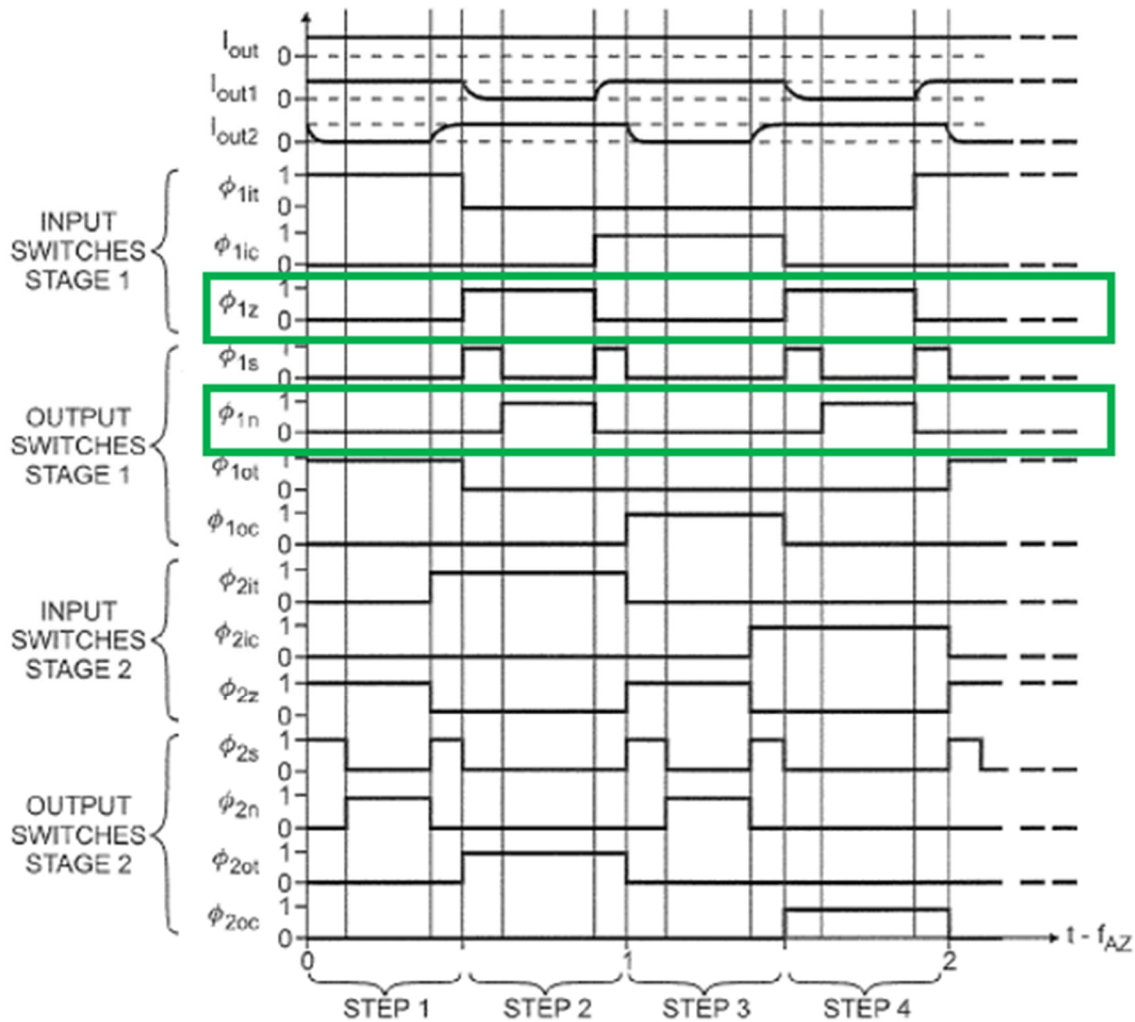
In *Pertijs*, auto-zeroing in the first stage is performed by switches 112, 130, capacitor 118, and additional transconductance stage 122 auto-zeroing. Ex. 1011, 4:5-30. The switches 112 and 130 (annotated in green) enable auto-zeroing by (1) shorting the first transconductance amplifier 102 inputs and (2) coupling the first transconductance amplifier 102 to the capacitor 118 and additional transconductance stage 122 respectively:



Ex. 1011, 2:65-3:1; Ex. 1003, ¶111.

The auto-zeroing occurs at a second frequency. For example, Fig. 2 depicts the clock signals (annotated in **green**) of switch 112 (clock signal Φ_{1z}) closing slightly before and opening slightly after the time when switches 130 (clock signal

Φ_{1n}) close to provide the capacitor 118 and transconductance stage 112:



Ex. 1011, Fig. 2; Ex. 1003, ¶112. Here, the auto-zeroing procedure is performed at Step 2 and Step 4. Ex. 1011, 4:57-60, 4:63-65; Ex. 1003, ¶112.

Switch 112 (controlled by clock signal Φ_{1z}) and switches 130 (controlled by clock signal Φ_{1n}) include two pulses in a full cycle (which does not repeat until after Step 4). Ex. 1003, ¶113. Thus, the second frequency is $2/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$. Ex. 1003, ¶114.

4. [21c] the ratio of the frequencies being two to one;

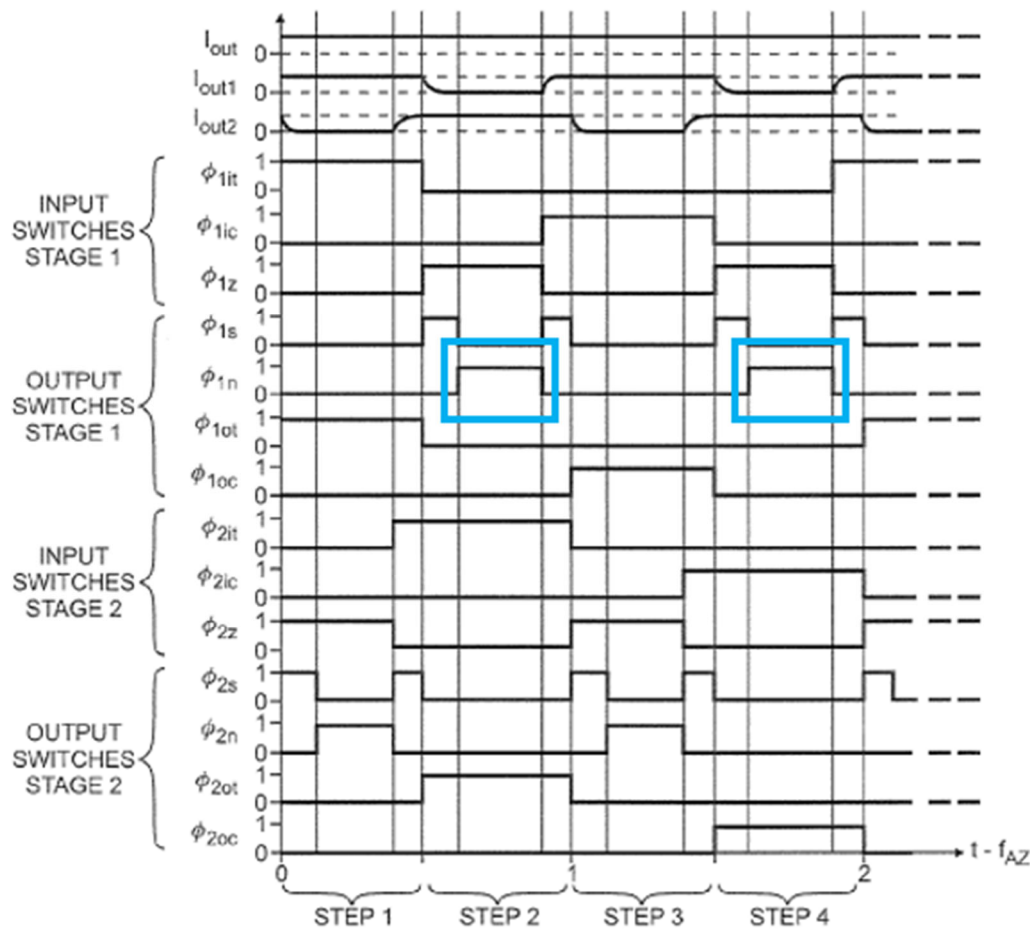
Pertijs renders this limitation obvious. Ex. 1003, ¶115. As described *supra* Section VIII.B.2 and VIII.B.3, the first frequency (the chopping frequency) is $1/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$ and the second frequency (the auto-zeroing frequency) is $2/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$. Ex. 1003, ¶115. Further, *Pertijs* expressly states that “in some embodiments, the chopping performed in the amplifier 100 is performed at half the auto-zeroing frequency f_{AZ} .” Ex. 1011, 4:44-46; Ex. 1003, ¶115. When the chopping (first frequency) happens at half the auto-zeroing (second frequency), the second frequency is twice that of the first. Accordingly, the ratio between the frequencies is two to one. Ex. 1003, ¶116.

5. [21d] the second frequency being twice the first frequency and

Pertijs renders this limitation obvious. Ex. 1003, ¶117. As explained *supra* Section VIII.B.4, the auto-zeroing frequency (the second frequency) is twice the chopping frequency (the first frequency). Ex. 1011, 4:44-46; Ex. 1003, ¶117.

6. [21e] having a duty cycle of less than one half.

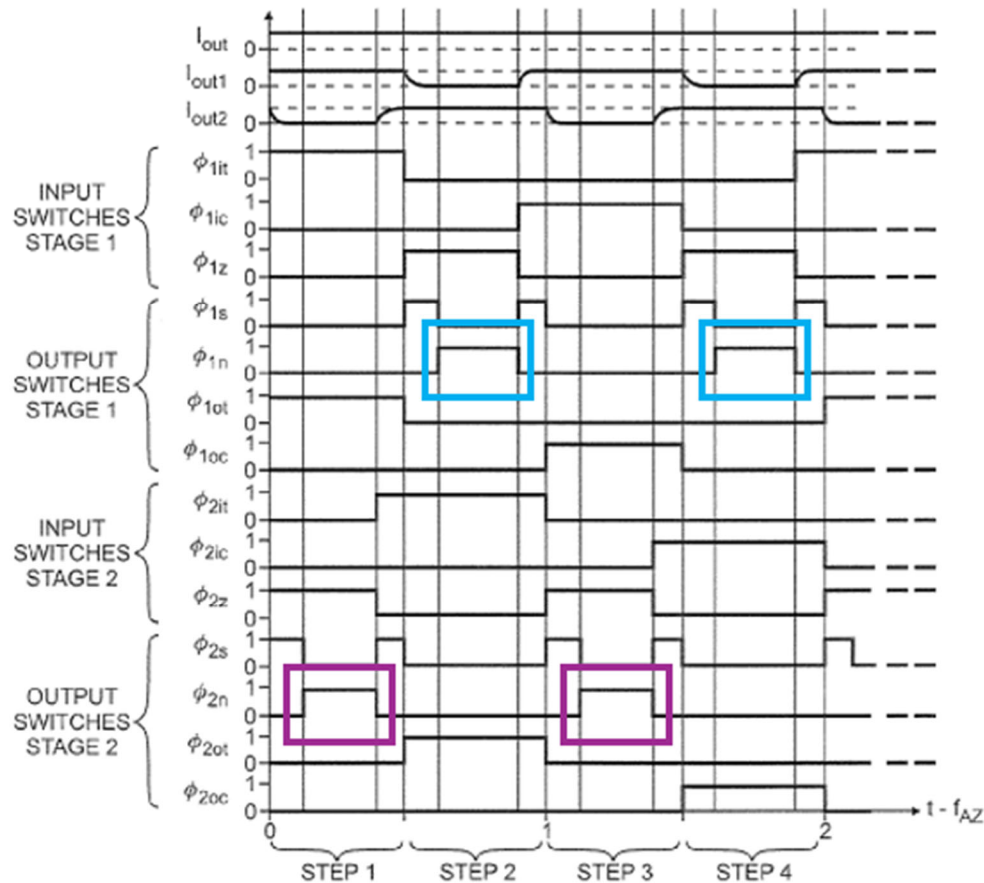
Pertijs renders this limitation obvious. Ex. 1003, ¶118. If each step is an equal length of time, the duty cycle of the auto-zeroing cycle would be less than one half. Ex. 1003, ¶119. For example, *Pertijs* depicts the auto-zeroing cycle occurring less than the entirety of Step 2 and Step 4 for the first transconductance amplifier 102 (as annotated in blue):



Ex. 1011 Fig. 2; Ex. 1003, ¶119. While switch 112 (controlled by clock signal Φ_{1z}) shorts the inputs of the first transconductance amplifier 102 at the beginning of Step 2 and Step 4, the auto-zeroing does not begin until the output of the first transconductance amplifier 102 is coupled to the capacitor 118 and additional transconductance stage 112 by switch 130. Ex. 1003, ¶119. Accordingly, the auto-zeroing duty cycle of *Pertijs* is less than one half.

There is no explicit teaching in *Pertijs* that Steps 1, 2, 3, and 4 must be equal (or unequal) lengths. However, even if *Pertijs* does not require Steps 1, 2, 3, and 4

having equal length, *Pertijs* still renders this limitation obvious. Ex. 1003, ¶120. *Pertijs* describes a ping-pong amplifier system where two amplifier systems of the same structure alternate to provide the system output. Ex. 1011, 2:38-45, 3:1-3, 4:29-30; Ex. 1003, ¶121. *Pertijs*'s Stage 2 has corresponding elements performed at corresponding (albeit staggered) clock signals. For example, *Pertijs*'s Stage 2 auto-zeroing cycle (in purple) and Stage 1 auto-zeroing cycle (in blue) are performed in alternating steps:



Ex. 1011, Fig. 2; Ex. 1003, ¶122.

So, to the extent Steps 1-4 occur over time intervals of discrete lengths that

force the duty cycle of the auto-zeroing cycle performed in Stage 1 to be more than one half (e.g., if Step 2 and Step 4 occur for longer than 50% of the time), the duty cycle of the auto-zeroing cycle of Stage 2 would be less than one half (because Step 1 and Step 3 would necessarily occur less than 50% of the time). Ex. 1003, ¶¶123-125. Accordingly, even if Steps 1-4 are different lengths, this limitation is still obvious. Ex. 1003, ¶126.

C. Independent Claim 22

- 1. [22pre] A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:**

To the extent it is limiting, *Pertijs* renders the preamble of claim 21 obvious. *See supra* Section VIII.B.1; *see also* Ex. 1011, 2:32-45, 3:1-3, 3:59-63, 4:29-30, Fig. 1; Ex. 1003, ¶¶97-100.

- 2. [22a] operating the chopper stabilization at a first frequency; and**

Pertijs renders this limitation obvious. *See supra* Section VIII.B.2; *see also* Ex. 1011, 3:59-61, 4:54-56, 4:60-63, Fig. 1, Fig. 2; Ex. 1003, ¶¶101-108.

- 3. [22b] operating the auto-zeroing at a second frequency;**

Pertijs renders this limitation obvious. *See supra* Section VIII.B.3; *see also* Ex. 1011, 2:65-3:1, 4:5-30, 4:57-60, 4:63-65; Ex. 1003, ¶¶109-114.

4. [22c] the ratio of the frequencies being two to one;

Pertijs renders this limitation obvious. *See supra* Section VIII.B.4; *see also*, Ex. 1011, 4:44-46; Ex. 1003, ¶¶115-116.

5. [22d] the second frequency having a duty cycle of not more than one-quarter.

Pertijs renders this limitation obvious. Ex. 1003, ¶131. For example, *Pertijs* teaches that its architecture could be extended to include an arbitrary number of amplification stages. Ex. 1011, 5:63-65 (“However, this architecture could be extended to an amplifier having any arbitrary number of stages.”). In these embodiments, one stage is auto-zeroed at a time while the remaining amplifiers are summed to provide an amplified output. Ex. 1011, 5:65-67; Ex. 1003, ¶132. *Pertijs* notes that additional stages reduce the overall supply current needed to obtain a given noise performance. Ex. 1011, 5:67-6:4; Ex. 1003, ¶132.

Based on *Pertijs*’s express teachings, it would be obvious to implement a system with four separate stages. Ex. 1003, ¶133. In such an implementation, a POSITA would implement the chopper stabilization to be performed at half the auto-zeroing frequency as taught by *Pertijs*. Ex. 1011, 4:44-46. Such timing arrangement for the four stages would involve 8 steps as illustrated in the chart below:

	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8
Stage 1	AZ	Uninverted			AZ	Twice Inverted		
Stage 2		AZ	Uninverted			AZ	Twice Inverted	
Stage 3	Uninverted		AZ	Twice Inverted			AZ	
Stage 4	Uninverted			AZ	Twice Inverted			AZ

Ex. 1003, ¶¶134-135.

Over the eight steps, each stage would have 3 steps with an uninverted inputs and outputs (in green), 3 steps with twice inverted inputs and outputs (in blue) and 2 steps in auto-zeroing mode (AZ, in white). Ex. 1003, ¶136. After Step 8, the timing cycle would restart the cycle at Step 1. Ex. 1003, ¶136. This timing arrangement is consistent with and taught by *Pertijs* having chopper stabilization performed at half the auto-zeroing frequency. Ex. 1011, 4:44-46; Ex. 1003, ¶137. The auto-zeroing switches would have a pulse over every 4 steps (or two pulses every 8 steps) while the chopper stabilization switches would each have one pulse over every eight steps. Ex. 1003, ¶137.

In such a system, one stage would perform auto-zeroing while the remaining three stages would provide the output signal. Ex. 1011 5:63-67; Ex. 1003, ¶133. If auto-zeroing is performed for an equal amount of time at each stage, the duty cycle of each auto-zeroing cycle would not be more than one quarter (e.g., 2 of 8 steps).

Ex. 1003, ¶138; *see* Ex. 1011, Fig. 2 (indicating the auto-zeroing cycle occupy less than a full step).

Indeed, even if the auto-zeroing cycles are performed by each stage for unequal amounts of time, then at least one of the four stages would have auto-zeroing cycles with duty cycles of less than one quarter. Ex. 1003, ¶139. Moreover, if additional amplifiers existed beyond 4, the duty cycle of the auto-zero would only continue to shrink proportionally to the number of amplifiers, such that the duty cycle would have been less than 4 for any system having more than 4 amplifiers. Accordingly, *Pertijs* renders obvious the second frequency having a duty cycle of not more than one-quarter. Ex. 1003, ¶140.

IX. GROUND II: *TANG* RENDERS CLAIMS 22 OBVIOUS

A. Overview

Like *Pertijs*, *Tang* predates the '596 Patent and discloses a ping-pong amplifier employing “auto-zeroing and chopping to simultaneously achieve low offset voltage and low frequency noise.” Ex. 1006, 1:66-2:2; Ex. 1003, ¶64. *Tang* discloses each element from Claim 22, arranged as in the claim, and was not previously considered by the Examiner.

1. *Tang*

Tang was filed on September 4, 2001 and issued as U.S. Patent No. 6,476,671 on November 5, 2002. Ex. 1006, Title Page. Accordingly, *Tang* is prior art under

35 U.S.C. §102(b).

Tang's system is used to reduce low frequency noise and offset voltage errors in ping-pong amplifiers. Ex. 1006, 1:7-9. As shown in Fig. 2a, *Tang* describes a circuit having an output amplifier A0, differential gain amplifiers A1 and A2, differential nulling amplifiers A3 and A4, switches S1-S24 (which comprise a switching network controlled by a control network C10), memory capacitors CM1-CM4, and a compensation capacitor CC:

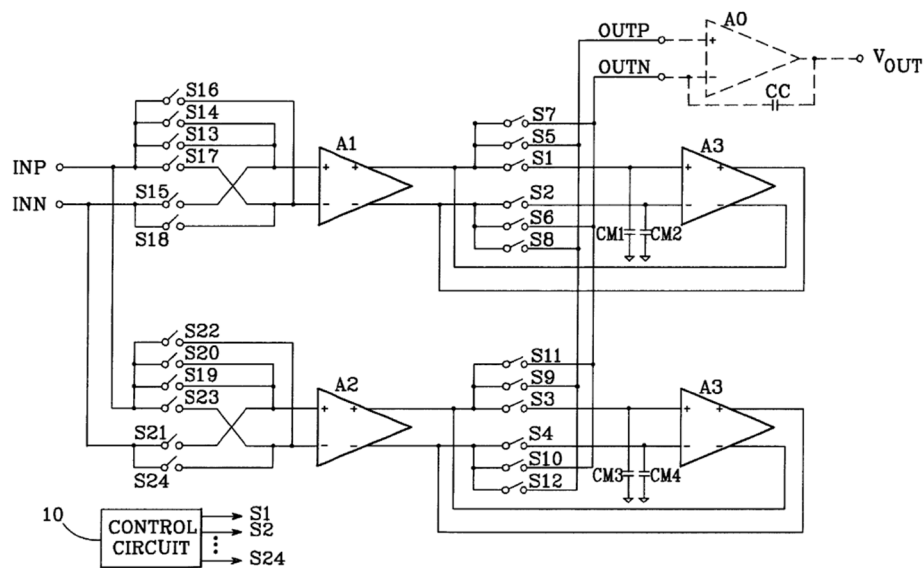


FIG. 2a

Ex. 1006, 3:5-52, Fig. 2a; Ex. 1003, ¶¶64, 66.² This circuit configuration “enables

² Fig. 2a mislabels the bottom right differential nulling amplifier A3 rather than A4. For the purposes of this Petition, reference to amplifier A4 should be understood to describe the lower differential nulling amplifier. Ex. 1003, ¶¶64.

the ping-pong amplifier to employ both auto-zeroing and chopping techniques to improve performance.” Ex. 1006, 3:48-50.

The switches S1-S24 are controlled by a four-phase timing cycle ($\Phi 1$ - $\Phi 4$). Ex. 1006, 3:50-54. In one timing operation, Amplifier A1 is auto-zeroed during $\Phi 1$ and $\Phi 2$ where switches S14 and S16 are closed to connect A1’s inputs together and switches S1 and S2 are closed to connect A1’s outputs to the inputs of nulling amplifier A3. Ex. 1006, 3:54-58; Ex. 1003, ¶67. Error signals are stored in CM1 and CM2, which are then applied to the inputs of amplifier A3, which amplifier A3 converts to corrects which serve to auto-zero A1’s output. Ex. 1006, 3:58-62; Ex. 1003, ¶67.

Also, during $\Phi 1$, switches S9, S10, S19, and S24 are closed so that signals INP and INN are not inverted before amplified by A2 and are communicated directly to output amplifier A0 without interaction with amplifier A4. Ex. 1006, 4:1-6; Ex. 1003, ¶70. During $\Phi 2$, switches S9, S10, S19, and S24 are opened, and switches S11, S12, S21, and S23 are closed which has the effect of chopping the input and output signals of A2. Ex. 1006, 4:7-14; Ex. 1003, ¶70.

During $\Phi 3$ and $\Phi 4$, A2 is auto-zeroed and A1’s signal is twice inverted by the choppers. Ex. 1006, 4:14. In other words, during $\Phi 3$ and $\Phi 4$, switches S3, S4, S20, and S22 are closed to perform the auto-zeroing on A2 with assistance from memory capacitors CM3 and CM4 and nulling amplifier A4. Ex. 1006, 4:14-18; Ex. 1003,

¶68. Likewise, during $\Phi 3$ switches S5, S6, S13, and S18 are closed and opened during $\Phi 4$ when switches S7, S8, S15, and S17 are opened to have the effect of twice inverting the signal (or inverting the input and output signals each once) through A1. Ex. 1006, 4:19-37; Ex. 1003, ¶69. Multiple alternative switch timing arrangements are provided in *Tang*. See Ex. 1006, Figs. 4a-4e. One example switch timing arrangement in *Tang's* circuit is provided below:

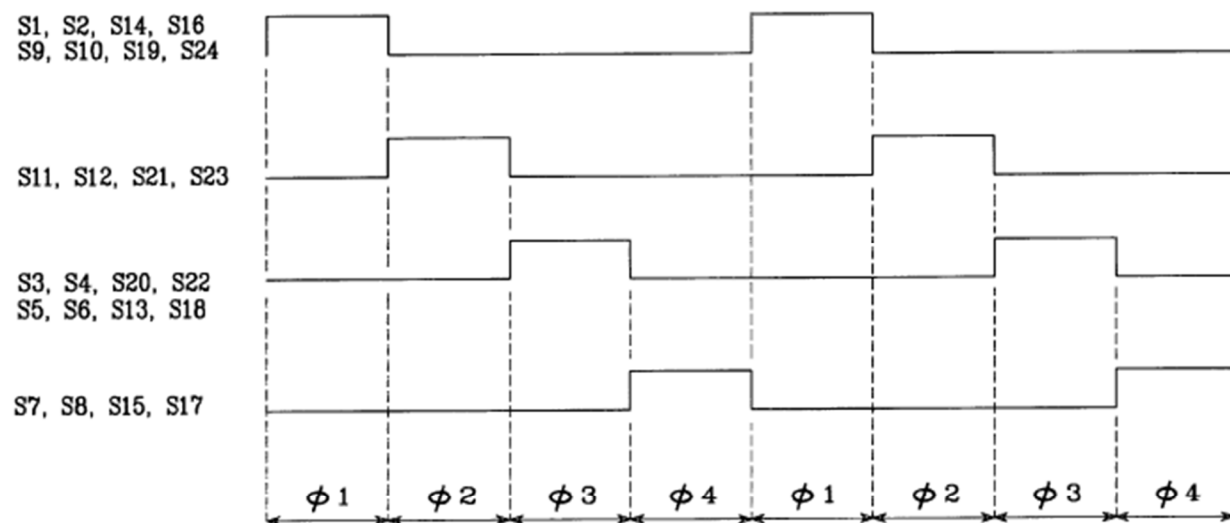


FIG.4d

Ex. 1006, Fig. 4d; 3:52-54; Ex. 1003, ¶71. Another timing arrangement provided in *Tang* includes eight separate phases, $\Phi 1$ - $\Phi 8$:

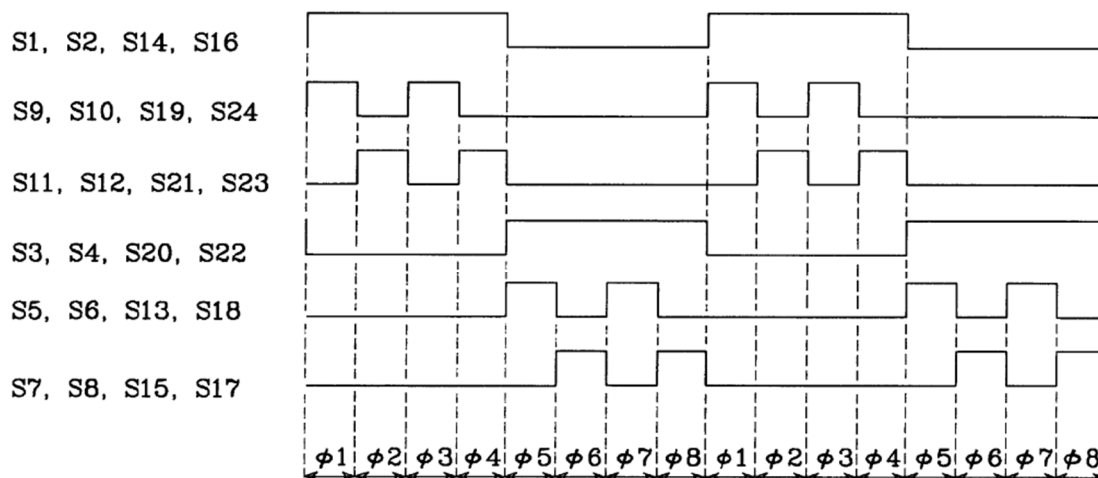
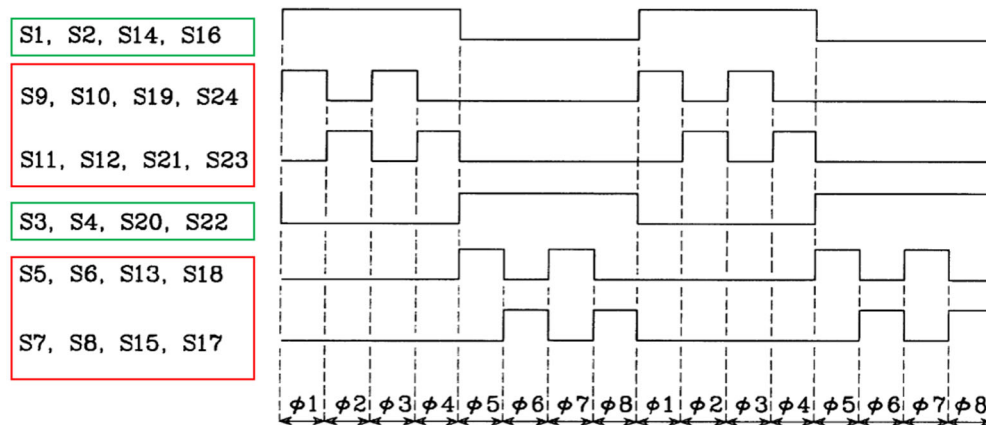


FIG.4e

Ex. 1006, Fig. 4e; Ex. 1003, ¶74. Here, two chopper stabilization cycles are performed for each auto-zero period. Ex. 1003, ¶75. For example, during $\Phi 1$ - $\Phi 4$, two chopping cycles are performed on the second amplifier A2, while only one auto-zeroing cycle is performed on the first amplifier A1. Ex. 1003, ¶¶72-73, 75. Then, during $\Phi 5$ - $\Phi 8$, two chopping cycles are performed on the first amplifier A1, while one auto-zeroing cycle is performed on the second amplifier A2. Ex. 1003, ¶75.

Fig. 4e is annotated below to show the timing arrangements of the switches used to perform auto-zeroing (in green) and chopper stabilization (in red) for both amplifiers A1 and A2:

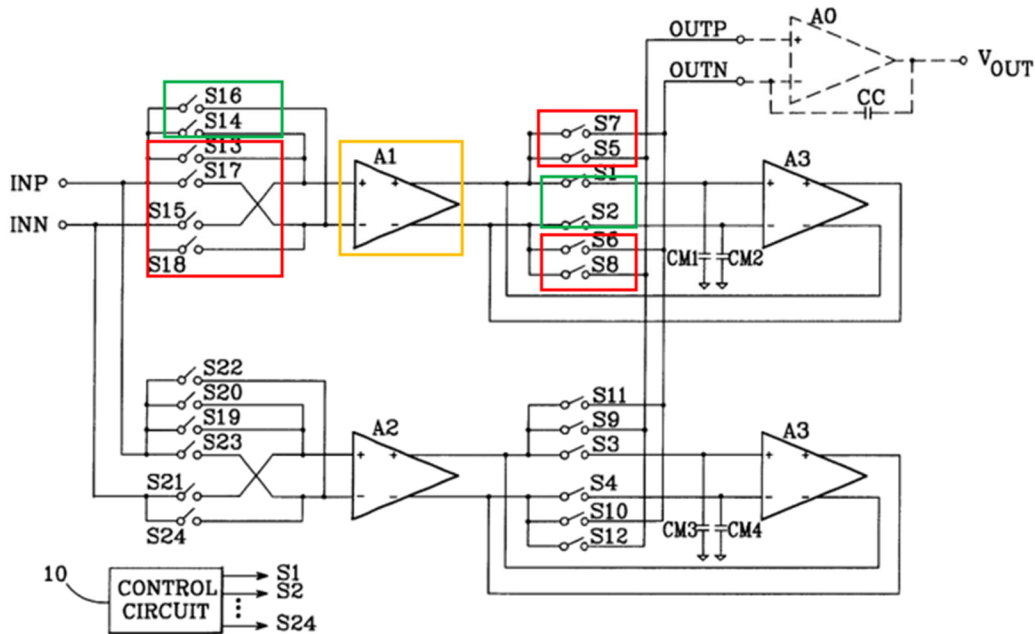


Ex. 1006, Fig. 4e; Ex. 1003, ¶74.

B. Independent Claim 22

1. [22pre] A method of operating a chopper stabilized first amplifier,
the chopper stabilized first amplifier having an auto-zeroing
capability comprising:

To the extent the preamble is limiting, *Tang* renders the preamble obvious. Ex. 1003, ¶141. For example, *Tang*'s system describes a “ping-pong amplifier.... [which] employs auto-zeroing and chopping[.]” Ex. 1006, 1:66-2:1. *Tang*'s circuit diagram also includes multiple amplifiers, (including a first amplifier A1 marked in yellow) and a switch network that enables auto-zeroing (in green) and chopping (in red) on the first amplifier A1:

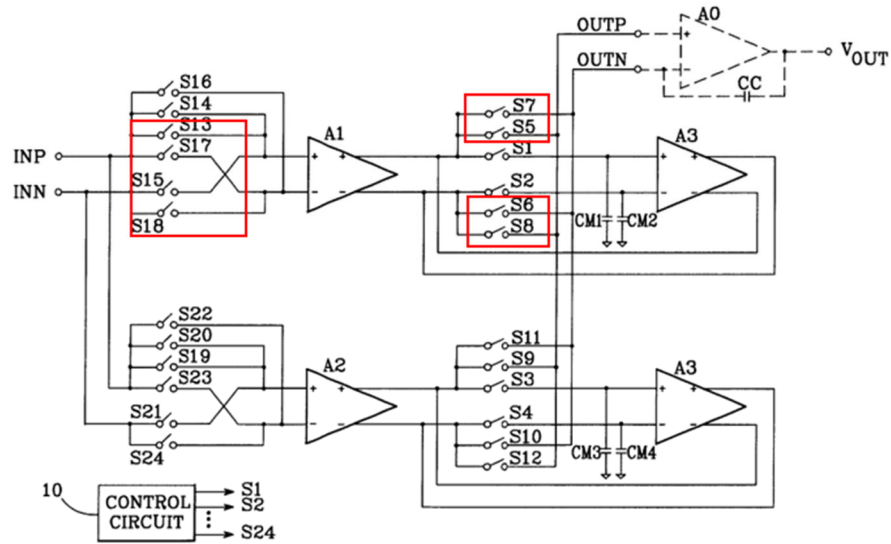


Ex. 1006, Fig. 2a; Ex. 1003, ¶142.

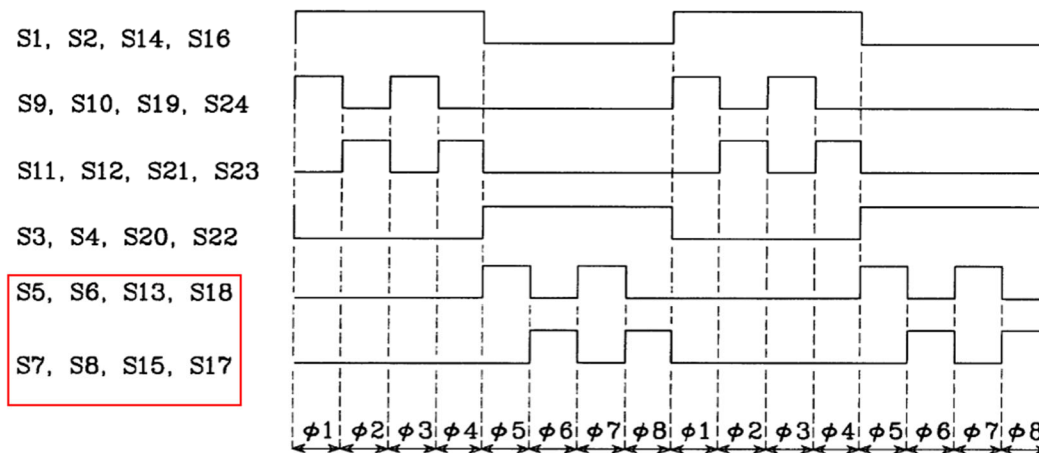
2. [22a] operating the chopper stabilization at a first frequency; and,

Tang renders this limitation obvious. Ex. 1003, ¶143. The chopper stabilization frequency is “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle.” Ex. 1003, ¶144; *see supra* Section VI.A.

Tang's switch network includes switches (in red) controlled to open or close during $\Phi 3$ and $\Phi 4$ to have “the effect of chopping the input and output signals of A1[:].”



Ex. 1006, Fig. 2a, 4:23-37; Ex. 1003, ¶145. All switches in *Tang's* circuit (S1-S24) are controlled by the control circuit 10. Ex. 1006, 3:49-51; Ex. 1003, ¶145. One timing arrangement disclosed by *Tang* describes the opening and closing of the switches during the chopping stabilization cycle (in red):



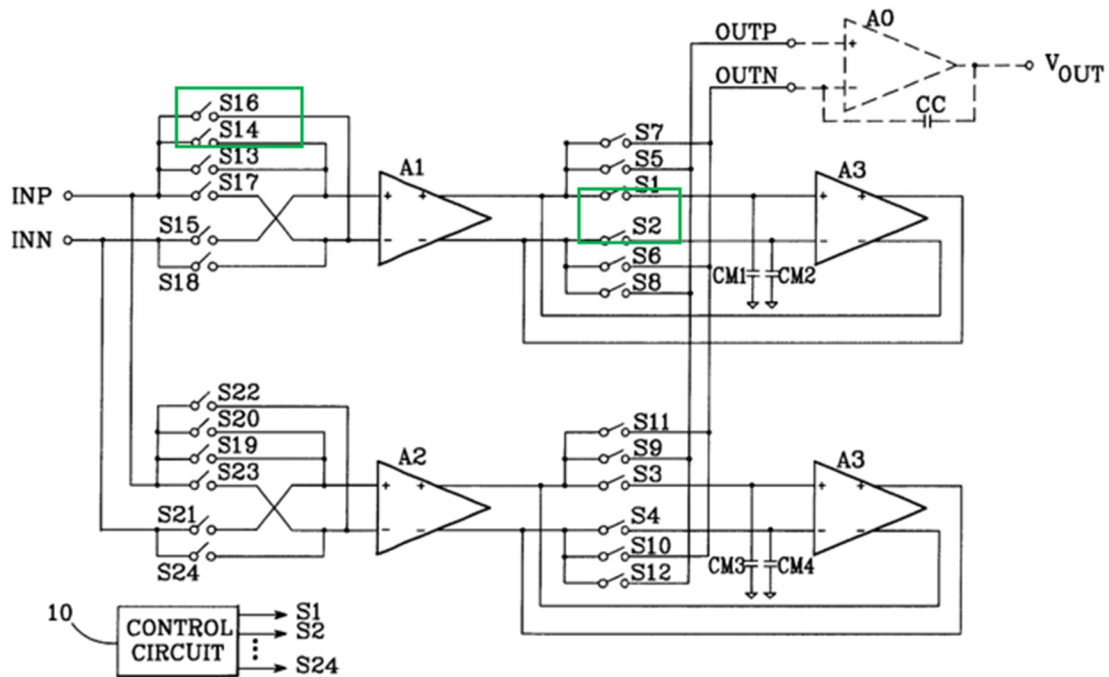
Ex. 1006, Fig. 4e; Ex. 1003, ¶146. At the beginning of $\Phi 5$, switches S5, S6, S13, and S18 are closed. Ex. 1003, ¶147. This connects the positive input voltage INP

to the positive input of the amplifier A1 (via S13) and to positive amplifier output OUTP (via S5), and the negative input voltage INN to the negative input of amplifier A1 (via S18) and to negative amplifier output OUTN (via S6). Ex. 1003, ¶147. Then, at the beginning of $\Phi 6$, switches S5, S6, S13, and S18 are opened, and switches S7, S8, S15, and S17 are closed. Ex. 1003, ¶148. This process is again repeated over $\Phi 7$ and $\Phi 8$. Ex. 1003, ¶¶147-148.

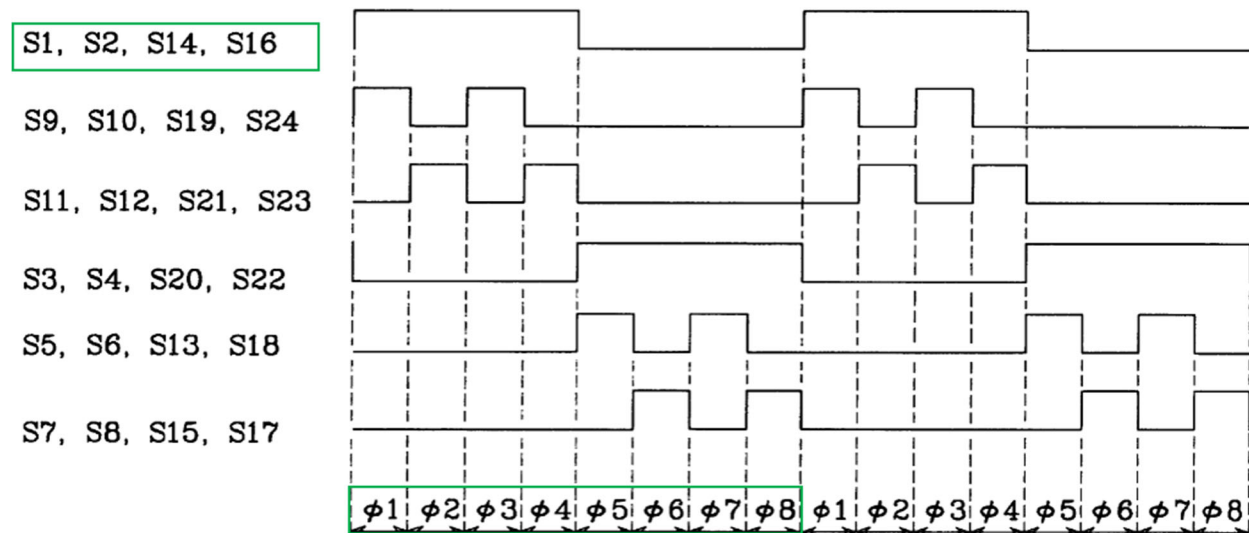
This has the effect of chopping the circuit; the positive input INP is connected to the negative input of amplifier A1 (via S17, and to positive amplifier output OUTP (via S8) while the negative input INN is connected to the positive input of amplifier A1 (via S15), and to negative amplifier output OUTN (via S7). Ex. 1003, ¶¶147-148. All switches used to perform chopper stabilization (Switches S5, S6, S7, S8, S13, S15, S17, S18) have two pulses in a full cycle (which occurs every $\Phi 1$ to $\Phi 8$ period). Ex. 1003, ¶149. Thus, the first frequency is $2/(\Phi 1 \text{ to } \Phi 8)$. Ex. 1003, ¶150.

3. [22b] operating the auto-zeroing at a second frequency;

Tang renders this limitation obvious. Ex. 1003, ¶151. The auto-zeroing frequency is “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle.” Ex. 1003, ¶152; *see supra* Section VI.A. The switches annotated in green are controlled by the control circuit to auto-zero the amplifier A1:



Ex. 1006, Fig. 2a; Ex. 1003, ¶153. One timing arrangement disclosed by *Tang* describes the opening and closing of the switches during the auto-zeroing cycle (as annotated in **green**):



Ex. 1006, Fig. 4e; Ex. 1003, ¶154.

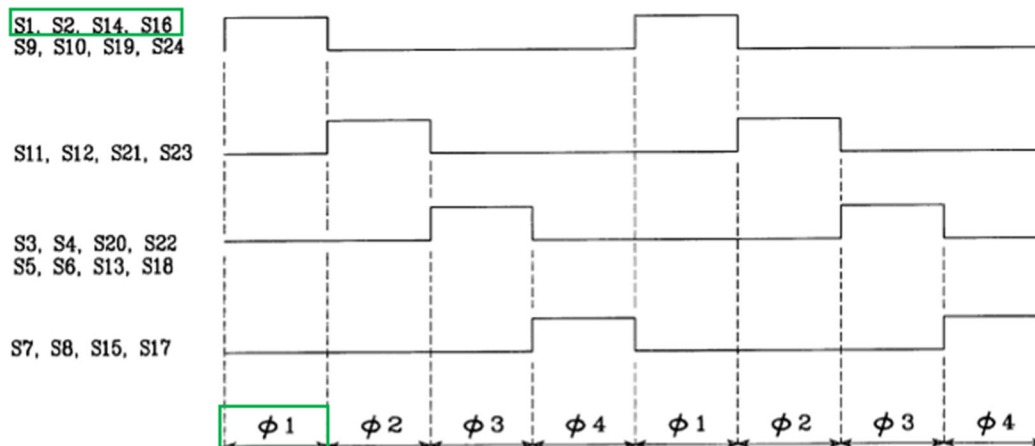
Amplifier A1 is in zeroing mode during $\Phi 1$ - $\Phi 4$. Ex. 1006, 4:53-57. The auto-zeroing is performed by closing switches S14 and S16 which have the effect of shorting the positive and negative input of amplifier A1, and closing switches S1 and S2, which communicates the outputs to the auto-zeroing subcircuit (which includes A3, CM1 and CM2). Ex. 1003, ¶154. All switches used to perform auto-zeroing (Switches S1, S2, S14, S16) have one pulse in a full cycle (which occurs every $\Phi 1$ to $\Phi 8$ period). Ex. 1003, ¶155. Thus, the second frequency is $1/(\Phi 1$ to $\Phi 8)$. Ex. 1003, ¶156.

4. [22c] the ratio of the frequencies being two to one;

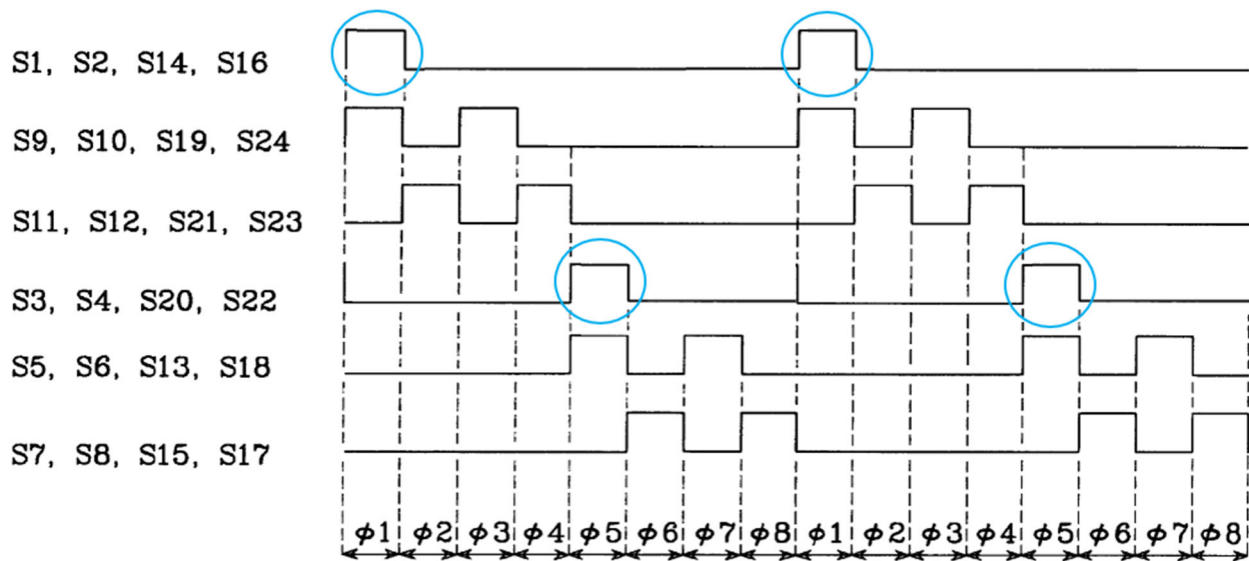
Tang renders this limitation obvious. As described *supra* Section IX.B.2 and IX.B.3, the first frequency (the chopping frequency) is $2/(\Phi 1$ to $\Phi 8)$ and the second frequency (the auto-zeroing frequency) is $1/(\Phi 1$ to $\Phi 8)$. Ex. 1003, ¶157; *see also*, Ex. 1006, 4:59-62 (“multiple chopping cycles are performed during each auto-zero period.”); Ex. 1003, ¶158. Accordingly, the ratio between the frequencies is two to one. Ex. 1003, ¶¶157-158.

5. [22d] the second frequency having a duty cycle of not more than one-quarter.

Tang renders this limitation obvious. Ex. 1003, ¶159. *Tang* describes an embodiment where the auto-zeroing function occurs over the full duration of phase $\Phi 1$ (in green):



Ex. 1006, Fig. 4d, 4:53-57 (“The timing diagram shown in FIG. 4d is intended to illustrate the auto-zeroing of one of the gain amplifiers during just one phase of the timing cycle.”); Ex. 1003, ¶160. It would be obvious to a POSITA to apply the shortened duty cycle explicitly taught in Fig. 4d to the timing arrangement of Fig. 4e in *Tang*. Ex. 1006, 3:63-66 (“Note that, though amplifier A1 is described above as being auto-zeroed during $\Phi 1$ and $\Phi 2$, it may also be auto-zeroed during $\Phi 1$ only or during $\Phi 2$ only. Each of these alternatives is functionally equivalent to auto-zeroing A1 during $\Phi 1$ and $\Phi 2$.”); Ex. 1003, ¶¶160-161. As shown (in blue) in the modified Fig. 4e below, the auto-zeroing cycles occur from during just $\Phi 1$ (or $\Phi 5$ for amplifier A2):



Ex. 1006, Fig. 4e; Ex. 1003, ¶161. In this timing arrangement, while the auto-zeroing occurs only during $\Phi 1$ (or $\Phi 5$) the auto-zeroing and chopping frequencies are unchanged compared to Fig. 4e. Ex. 1003, ¶162.

Tang does not explicitly state that the four phases $\Phi 1$ - $\Phi 8$ are equal. However, it would be obvious to a POSITA that each phase $\Phi 1$ - $\Phi 8$ is equal, or each phase is set to have an equal duration. Ex. 1003, ¶163. Each step would be configured to be one clock cycle, which would simplify the timing mechanism. Ex. 1003, ¶163.

Accordingly, the duty cycle of the second frequency (the auto-zeroing frequency) is less than one-quarter. Ex. 1003, ¶164.

X. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *Fintiv* Denial Is Improper

Fintiv does not apply as the only co-pending district court matter is not a patent infringement action, such that no other district court is presently analyzing

the validity of any claim of the '596 Patent. As a result, none of the *Fintiv* factors are applicable to this proceeding. Regardless, the compelling evidence of unpatentability in this Petition confirms that institution should occur.

Moreover, the co-pending case in NDCA, which is not a patent action, to the extent the findings in the PTAB would be helpful, is highly likely to be stayed should the request be filed. There is little, to no, duplication of efforts as infringement and invalidity are not at issue in the NDCA case.

To the extent changes are made to the now-governing standards regarding discretionary denial, Petitioner reserves its right to respond.

B. 35 U.S.C. § 325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017), favor institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-11 (PTAB Feb. 13, 2020) (precedential).

Neither *Pertijs* nor *Tang* were before the patent office and neither the same, nor substantially the same arguments were previously presented.

XI. CONCLUSION

Petitioner requests institution of *inter partes* review and cancellation of Claims 21 and 22.

Petition for *Inter Partes* Review of U.S. Patent 7,973,596

Dated: January 30, 2025

Respectfully submitted,

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CLAIM APPENDIX

[21pre] A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

[21a] operating the chopper stabilization at a first frequency; and

[21b] operating the auto-zeroing at a second frequency;

[21c] the ratio of the frequencies being two to one;

[21d] the second frequency being twice the first frequency and;

[21e] having a duty cycle of less than one half.

[22pre] A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

[22a] operating the chopper stabilization at a first frequency; and

[22b] operating the auto-zeroing at a second frequency;

[22c] the ratio of the frequencies being two to one;

[22d] the second frequency having a duty cycle of not more than one quarter.

Certification of Word Count Under 37 C.F.R. § 42.24(d)

The undersigned hereby certifies that the foregoing contains 6,872 words according to the word count of the word-processing software used to prepare the foregoing.

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CERTIFICATE OF SERVICE

A copy of this Petition for *Inter Partes* Review and supporting materials has been served at the following correspondence address of record for the subject patent via Federal Express Priority Overnight® on this 30th day of January, 2025:

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