

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANALOG DEVICES, INC.,
Petitioner,

v.

NUMBER 14 B.V.,
Patent Owner.

IPR2025-00550
U.S. Patent 7,973,596

CERTIFIED FILE HISTORY OF U.S. PATENT NO. 7,973,596
(Ex. 1002)

FILE HISTORY

US 7,973,596

PATENT: 7,973,596

INVENTORS: ESCHAUZIER RUDY G H
VAN RIJN NICO

TITLE: Low-noise, low-power, low drift offset
correction in operational and
instrumentation amplifiers

APPLICATION NO: US2009464572A

FILED: 12 MAY 2009

ISSUED: 05 JUL 2011

COMPILED: 03 JAN 2025

7,973,596

**LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN
OPERATIONAL AND INSTRUMENTATION AMPLIFIERS**

Transaction History

Date	Transaction Description
05-12-2009	Applicants have given acceptable permission for participating foreign
05-12-2009	Initial Exam Team nn
05-20-2009	Information Disclosure Statement considered
05-20-2009	Information Disclosure Statement (IDS) Filed
05-20-2009	Information Disclosure Statement (IDS) Filed
05-28-2009	Filing Receipt
05-28-2009	Corrected Paper
07-23-2009	Additional Application Filing Fees
07-23-2009	Applicant has submitted new drawings to correct Corrected Papers problems
08-04-2009	Sent to Classification Contractor
08-04-2009	Filing Receipt - Updated
08-12-2009	Application Dispatched from OIPE
04-07-2010	Case Docketed to Examiner in GAU
04-28-2010	Case Docketed to Examiner in GAU
09-17-2010	Non-Final Rejection
09-21-2010	Mail Non-Final Rejection
11-18-2010	PG-Pub Issue Notification
12-21-2010	Response after Non-Final Action
12-28-2010	Date Forwarded to Examiner
02-22-2011	Interview Summary Record
02-24-2011	Notice of Allowance Data Verification Completed
02-25-2011	Mail Examiner's Amendment
02-25-2011	Mail Notice of Allowance
05-25-2011	Issue Fee Payment Verified
05-25-2011	Issue Fee Payment Received
05-26-2011	Dispatch to FDC
05-26-2011	Application Is Considered Ready for Issue
06-15-2011	Issue Notification Mailed
07-05-2011	Recordation of Patent Grant Mailed
07-05-2011	Patent Issue Date Used in PTA Calculation
01-07-2019	Payment of Maintenance Fee, 8th Year, Large Entity
12-20-2022	Payment of Maintenance Fee, 12th Year, Large Entity
05-29-2024	Application ready for PDX access by participating foreign offices
05-29-2024	Application ready for PDX access by participating foreign offices

Issue Classification 	Application/Control No. 12464572	Applicant(s)/Patent Under Reexamination ESCHAUZIER ET AL.
	Examiner Khiem D Nguyen	Art Unit 2817

[illegible][illegible]

/Kiem D Nguyen/ Examiner.Art Unit 2817		2-22-2011	Total Claims Allowed:	
(Assistant Examiner)		(Date)	28	
/ROBERT PASCAL/ Supervisory Patent Examiner.Art Unit 2817		02/23/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)		(Date)	7	7

Index of Claims 	Application/Control No. 12464572	Applicant(s)/Patent Under Reexamination ESCHAUZIER ET AL.
	Examiner Khiem D Nguyen	Art Unit 2817

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

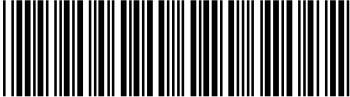
☐ Claims renumbered in the same order as presented by applicant

☐ CPA

☐ T.D.

☐ R.1.47

CLAIM		DATE								
Final	Original	09/15/2010								
	1	✓								
	2	✓								
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	4	✓								
	5	✓								
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	34	N								
	35	N								
	36	N								

Search Notes 	Application/Control No. 12464572	Applicant(s)/Patent Under Reexamination ESCHAUZIER ET AL.
	Examiner Khiem D Nguyen	Art Unit 2817

SEARCHED			
Class	Subclass	Date	Examiner
330	9,124R,295	8-26-2010	KDN
327	124, 307	8-30-2010	KDN

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor Search, see printout.	8-26-2010	KDN
EAST-search history, see printout.	8-26-2010	KDN
Consulted with Steven Mottola	8-30-2010	KDN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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Search Notes 	Application/Control No. 12464572	Applicant(s)/Patent Under Reexamination ESCHAUZIER ET AL.
	Examiner Khiem D Nguyen	Art Unit 2817

SEARCHED			
Class	Subclass	Date	Examiner
330	9,124R,295	8-26-2010	KDN
327	124, 307	8-30-2010	KDN
Research above		2-18-2011	KDN

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor Search, see printout.	8-26-2010	KDN
EAST-search history, see printout.	8-26-2010	KDN
Consulted with Steven Mottola	8-30-2010	KDN
Consulted with Steven Mottola	2/2/2011	KDN
	2-18-2011	KDN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	EAST-US-PGPUB; USPAT; UPAD, see printout.	2-18-2011	KDN

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	6	((RUDY) near2 (ESCHAUZIER)).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 08:20
S2	4	((NICO) near2 ("VAN RIJN")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 08:20
S3	0	pc was resetted before save	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 08:20
S4	58	330/9.ccls. and chop\$4 and (autozero or auto-zero or auto zero)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 08:22
S5	26	341/143.ccls. and auto zero	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 08:43
S6	138	341/143.ccls. and chopp\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 08:44
S7	2	"7132883".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 09:05
S8	3	"6456159".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 09:12

S9	2	"6989716".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 09:15
S10	5	("4931745" "5115202" "6121831" "6140872" "6407630").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 10:29
S11	6	("6476671").URPN.	USPAT	ADJ	ON	2010/08/26 10:30
S12	3	("6262626" "6456159" "6566942").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 10:37
S13	6	chopp\$3 and (khiem near2 nguyen).xa.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 10:56
S14	4	("6933781" "7292095" "7403064" "7560991").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:01
S15	1	("7733169").URPN.	USPAT	ADJ	ON	2010/08/26 11:02
S16	1	("6538503").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:21
S17	7	("4232271" "4833422" "5075633" "5276405" "5444363" "5880638" "6262626").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:21
S18	7	("4048574" "4392112" "4587443" "5410270" "5486788" "5600275" "5663680").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:22
S19	4	("4931745" "4933642" "5047727" "5486788").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:23
S20	12	("5663680").URPN.	USPAT	ADJ	ON	2010/08/26 11:23
S21	118	330/9.ccls. and (autozero or auto-zero or auto zero)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 11:58

S22	39	"330"/\$.ccls. and (autozero or auto zero) circuit	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:03
S23	368	((autozero or auto zero) (circuit or network or unit))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:44
S24	277	S23 and amplifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:45
S25	122	330/9.ccls. and (auto zero or autozero or autozeroed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:47
S26	2	"20030193367"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:51
S27	2	"6639460".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:54
S28	3	("6242974" "6380801" "6456159").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/27 15:54
S29	7	("6639460").URPN.	USPAT	ADJ	ON	2010/08/27 15:55
S30	7	("20020190734" "4881045" "6538503" "6639460" "6653894" "6753730" "6919766").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/27 15:58
S31	0	("7167051").URPN.	USPAT	ADJ	ON	2010/08/27 15:59

S32	3	"20090027116"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 16:11
S33	3	("5508656" "7167045" "7420410").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/27 16:13
S34	6	("4016557" "6188284" "6678506" "7132883" "7209000" "7397302").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/27 16:54
S35	0	("7696817").URPN.	USPAT	ADJ	ON	2010/08/27 16:54
S36	17	327/124.ccls. and (auto zero or autozero or autozeroed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 16:57
S37	4	("7262654" "7292095" "7446602" "7456684").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/27 17:00
S38	2	"20030189461"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 09:39
S39	17	330/124R.ccls. and chop\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:16
S40	65	330/124R.ccls. and auto	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:16
S41	253	330/124R.ccls. and offset\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:16

S42	537	330/9.ccls. and (chopp\$4 or switch\$3) and ((auto zero or autozero or auto-zero) or (offset\$3 voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:31
S43	103	S42 and (frequenc\$4 with (two or ratio))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:31
S44	85	327/124.ccls. and (chopp\$4 or switch\$3) and ((auto zero or autozero or auto-zero) or (offset\$3 voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:49
S45	1	327/124.ccls. and (chopp\$4 or switch\$3) and (auto zero or autozero or auto-zero) and frequency near2 twice	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 12:01
S52	624	327/307.ccls.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/30 13:18
S53	28	327/307.ccls. and chopp\$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/30 13:19
S54	83	327/307.ccls. and frequenc\$3 with (double or twice or two)	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/30 13:21
S55	76	330/124R.ccls. and half cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/02/18 05:44
S56	6	330/124R.ccls. and half cycle and chop\$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/02/18 06:02
S57	4	("6933781" "7292095" "7403064" "7560991").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/02/18 06:06

S58	1	330/124R.ccls. and second chopp\$3 and cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/02/18 06:11
S59	6	330/124R.ccls. and chopp\$3 and half cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/02/18 06:12
S60	67	330/9,51.ccls. and chopp\$3 and half cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/02/18 06:12
S61	39	327/124,307.ccls. and chopp\$3 and half cycle	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2011/02/18 06:30
S62	8	("4097806" "4559502" "4622521" "4912423" "4933642" "5442318" "5789981" "5886528").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2011/02/18 06:31

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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S47	4	("7262654" "7292095" "7446602" "7456684").PN.	US-PGPUB; USPAT	ADJ	ON	2010/08/30 08:26
S48	3	("6621334" "6788136" "7295061").PN.	US-PGPUB; USPAT	ADJ	ON	2010/08/30 08:27
S49	3	("7456684").URPN.	USPAT	ADJ	ON	2010/08/30 08:28

S50	22	("20020149506" "20050266821" "20060164073" "20070252573" "20080122457" "4939516" "5621319" "5748133" "6362618" "6380874" "6437718" "6583741" "6621334" "6777932" "6861839" "7049812" "7161520" "7342390" "7425821" "7456684" "7471134" "7492214").PN.	US-PGPUB; USPAT	ADJ	ON	2010/08/30 08:32
S51	160	amplif\$7 and chopp\$4 and (auto-zero or autozero or auto zero) and frequenc\$3 and offset\$3	US-PGPUB; USPAT; UPAD	ADJ	ON	2010/08/30 09:25
S63	1	first differential amplifier and autozero and ((first or second) chopp\$3) and half cycle	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/02/18 06:33
S64	4	amplifier and autozero and ((first or second) chopp\$3) and half cycle	US-PGPUB; USPAT; UPAD	ADJ	ON	2011/02/18 06:34

2/ 22/ 2011 4:09:47 PM
C:\ Documents and Settings\ knguyen19\ My Documents\ EAST\ Workspaces\ 12464572_9. wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	6	((RUDY) near2 (ESCHAUZIER)).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 08:20
S2	4	((NICO) near2 ("VAN RIJN")).INV.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 08:20
S3	0	pc was resetted before save	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 08:20
S4	58	330/9.ccls. and chop\$4 and (autozero or auto-zero or auto zero)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 08:22
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S6	138	341/143.ccls. and chop\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 08:44
S7	2	"7132883".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 09:05
S8	3	"6456159".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 09:12

S9	2	"6989716".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/26 09:15
S10	5	("4931745" "5115202" "6121831" "6140872" "6407630").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 10:29
S11	6	("6476671").URPN.	USPAT	ADJ	ON	2010/08/26 10:30
S12	3	("6262626" "6456159" "6566942").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 10:37
S13	6	chopp\$3 and (khiem near2 nguyen).xa.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 10:56
S14	4	("6933781" "7292095" "7403064" "7560991").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:01
S15	1	("7733169").URPN.	USPAT	ADJ	ON	2010/08/26 11:02
S16	1	("6538503").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:21
S17	7	("4232271" "4833422" "5075633" "5276405" "5444363" "5880638" "6262626").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/26 11:21
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S24	277	S23 and amplifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:45
S25	122	330/9.ccls. and (auto zero or autozero or autozeroed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:47
S26	2	"20030193367"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:51
S27	2	"6639460".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/27 15:54
S28	3	("6242974" "6380801" "6456159").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/27 15:54
S29	7	("6639460").URPN.	USPAT	ADJ	ON	2010/08/27 15:55
S30	7	("20020190734" "4881045" "6538503" "6639460" "6653894" "6753730" "6919766").PN.	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/27 15:58
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S40	65	330/124R.ccls. and auto	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:16
S41	253	330/124R.ccls. and offset\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:16

S42	537	330/9.ccls. and (chopp\$4 or switch\$3) and ((auto zero or autozero or auto-zero) or (offset\$3 voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:31
S43	103	S42 and (frequenc\$4 with (two or ratio))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:31
S44	85	327/124.ccls. and (chopp\$4 or switch\$3) and ((auto zero or autozero or auto-zero) or (offset\$3 voltage))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 11:49
S45	1	327/124.ccls. and (chopp\$4 or switch\$3) and (auto zero or autozero or auto-zero) and frequency near2 twice	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2010/08/30 12:01
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S53	28	327/307.ccls. and chopp\$3	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/30 13:19
S54	83	327/307.ccls. and frequenc\$3 with (double or twice or two)	US-PGPUB; USPAT; USOCR	ADJ	ON	2010/08/30 13:21

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S46	21	amplif\$7 and chopp\$4 and (auto-zero or autozero or auto zero) and frequenc\$3 same (doubl\$3 or twice or (rati\$3 near2 "2"))	US-PGPUB; USPAT; UPAD	ADJ	ON	2010/08/30 07:43
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S48	3	("6621334" "6788136" "7295061").PN.	US-PGPUB; USPAT	ADJ	ON	2010/08/30 08:27

S49	3	("7456684").URPN.	USPAT	ADJ	ON	2010/08/30 08:28
S50	22	("20020149506" "20050266821" "20060164073" "20070252573" "20080122457" "4939516" "5621319" "5748133" "6362618" "6380874" "6437718" "6583741" "6621334" "6777932" "6861839" "7049812" "7161520" "7342390" "7425821" "7456684" "7471134" "7492214").PN.	US-PGPUB; USPAT	ADJ	ON	2010/08/30 08:32
S51	160	amplif\$7 and chopp\$4 and (auto-zero or autozero or auto zero) and frequenc\$3 and offset\$3	US-PGPUB; USPAT; UPAD	ADJ	ON	2010/08/30 09:25

8/ 30/ 2010 3:27:17 PM
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wsp



(12) **United States Patent**
Eschauzier et al.

(10) **Patent No.:** **US 7,973,596 B2**
(45) **Date of Patent:** **Jul. 5, 2011**

(54) **LOW-NOISE, LOW-POWER, LOW DRIFT
OFFSET CORRECTION IN OPERATIONAL
AND INSTRUMENTATION AMPLIFIERS**

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(73) Assignee: **Number 14 B.V.**, Bergschenhoek (NL)

(*) Notice: Subject to any disclaimer, the term of this
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U.S.C. 154(b) by 71 days.

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(65) **Prior Publication Data**

US 2010/0289568 A1 Nov. 18, 2010

(51) **Int. Cl.**
H03F 1/02 (2006.01)

(52) **U.S. Cl.** 330/9; 330/51

(58) **Field of Classification Search** 330/9, 124 R,
330/295; 327/124, 307

See application file for complete search history.

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Assistant Examiner — Khiem D Nguyen

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Zafman LLP

(57) **ABSTRACT**

Low-noise, low-power, low drift offset correction in opera-
tional and instrumentation amplifiers and amplifiers using the
same are disclosed. The amplifiers disclosed use different
combinations of chopping and auto-zero techniques. Also
disclosed are amplifiers using on-off switches to affect the
chopping and auto-zeroing, with unique circuits for driving
the switches on the differential input to provide boot-strapped
switch controls. Other features are disclosed.

28 Claims, 17 Drawing Sheets

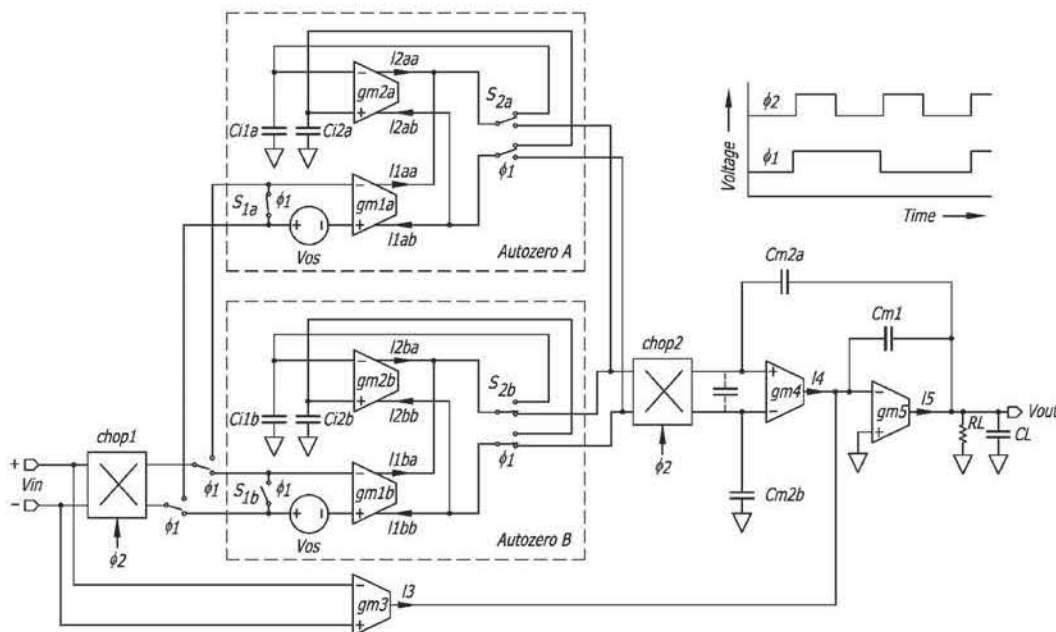


Fig. 1 (Prior Art)

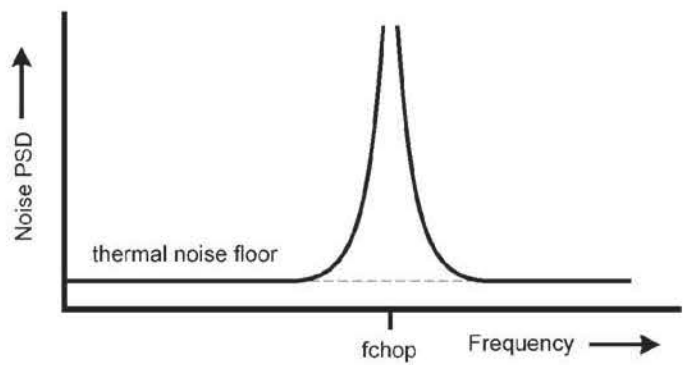


Fig. 2 (Prior Art)

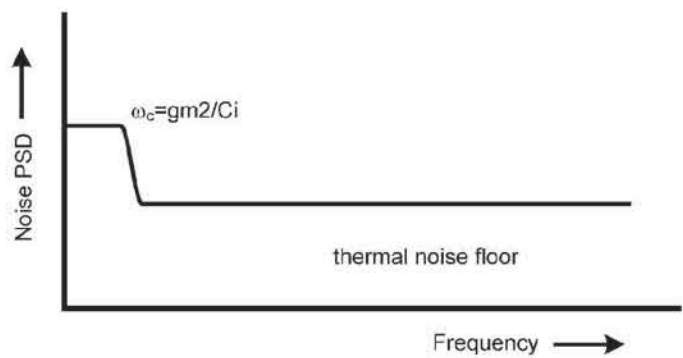


Fig. 4 (Prior Art)

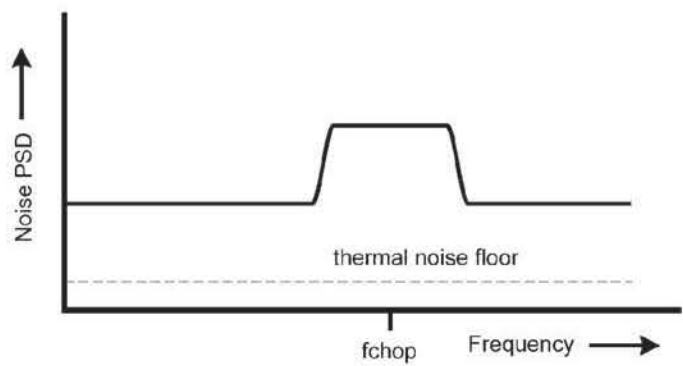


Fig. 6

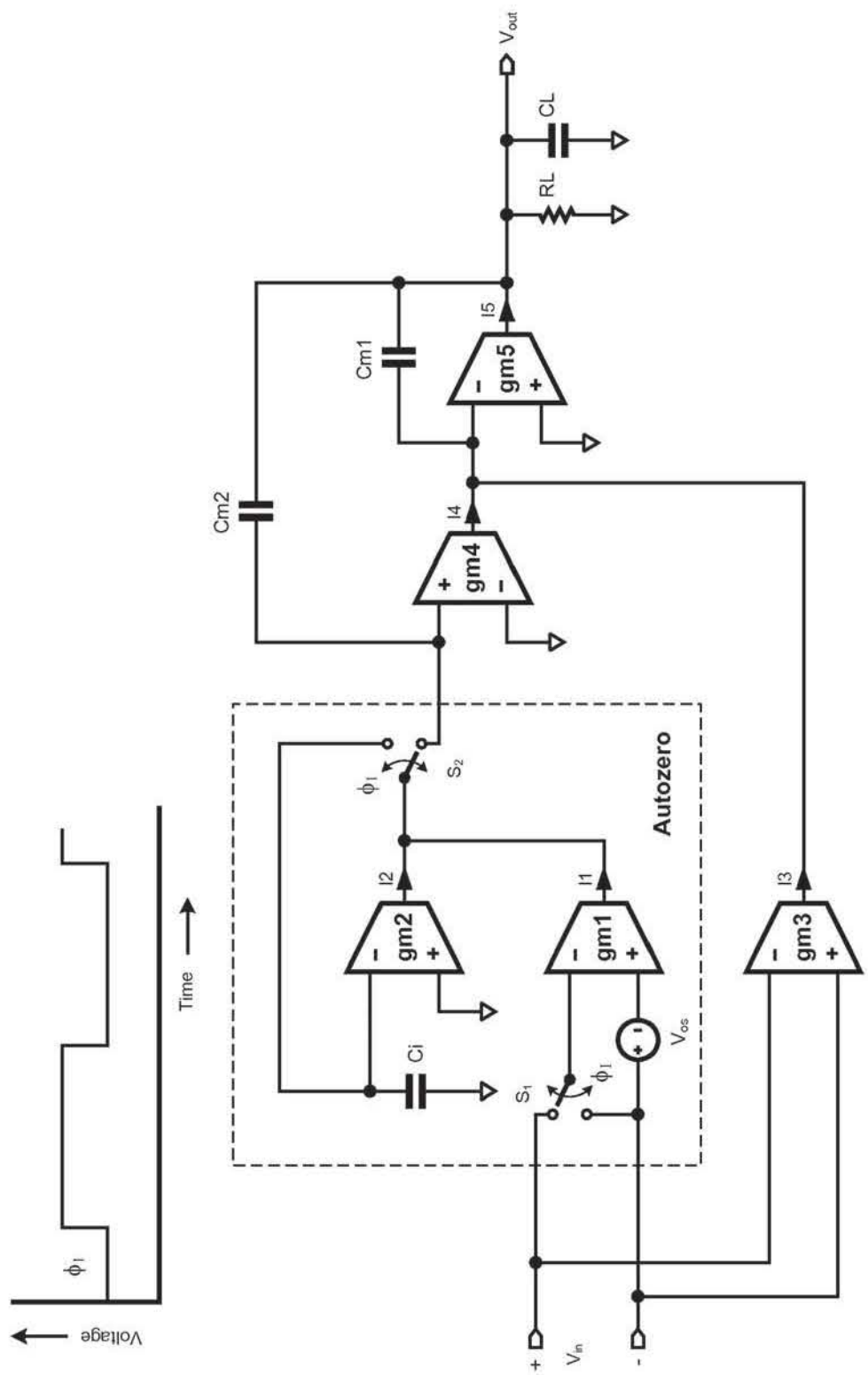
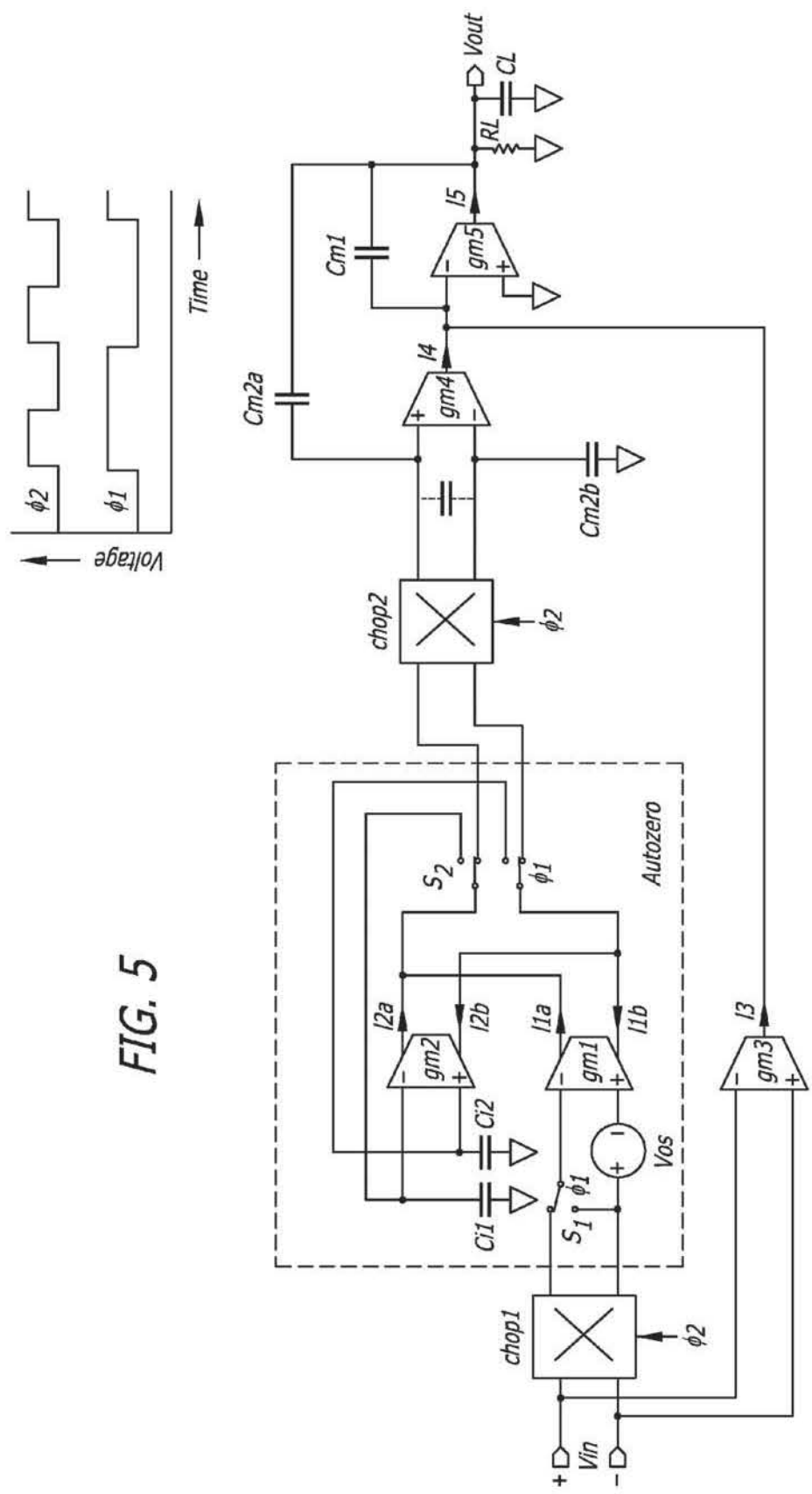


Fig. 3 (Prior Art)



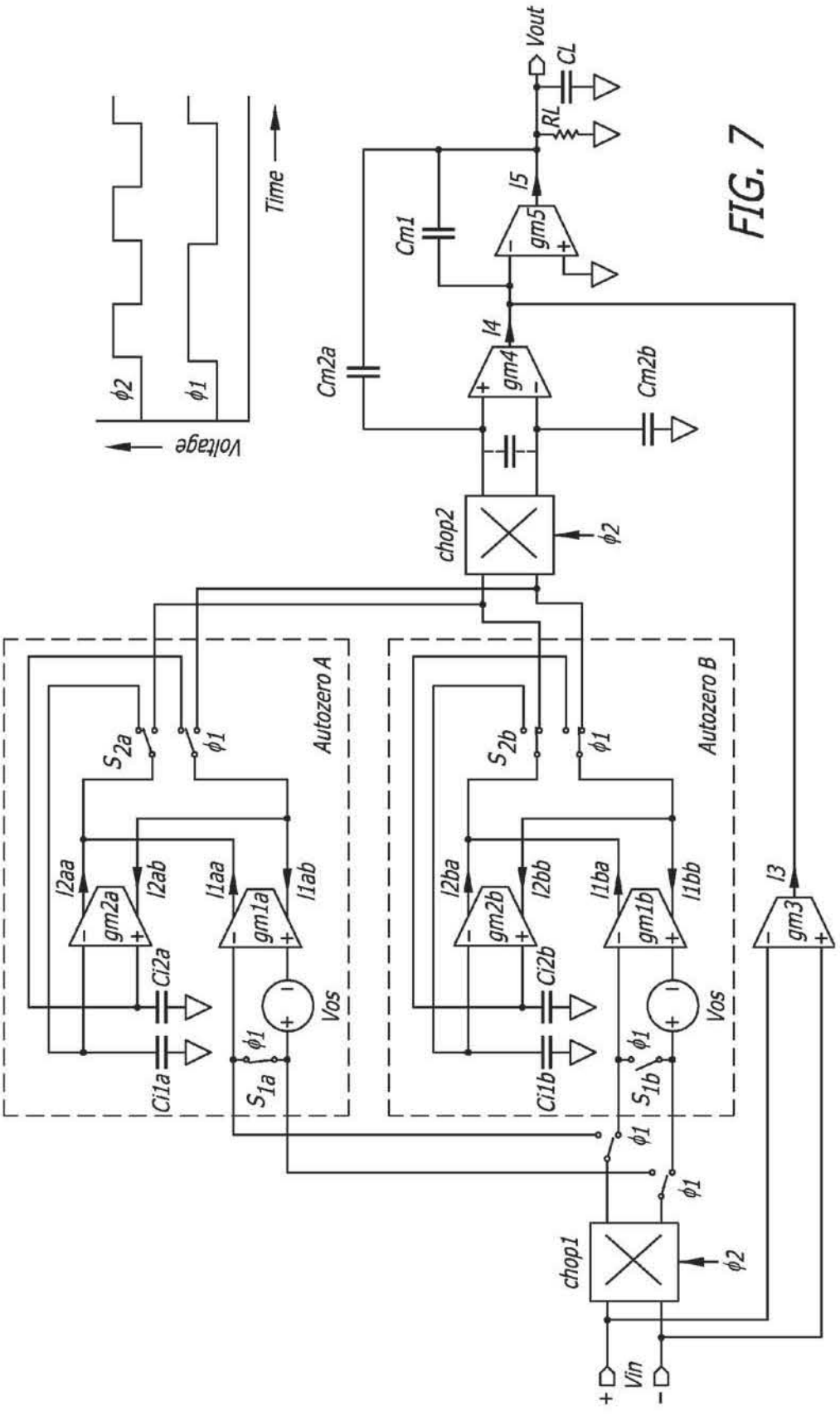


FIG. 7

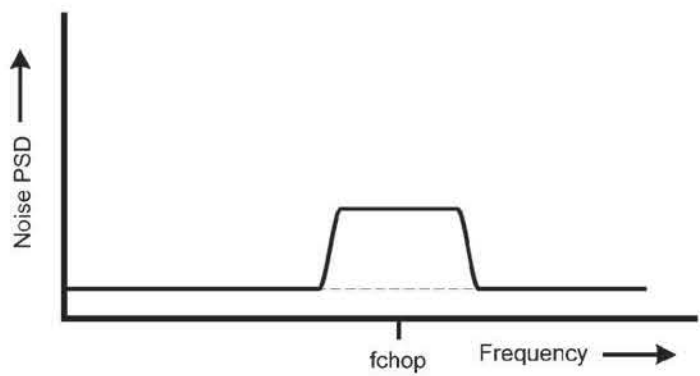


Fig. 8

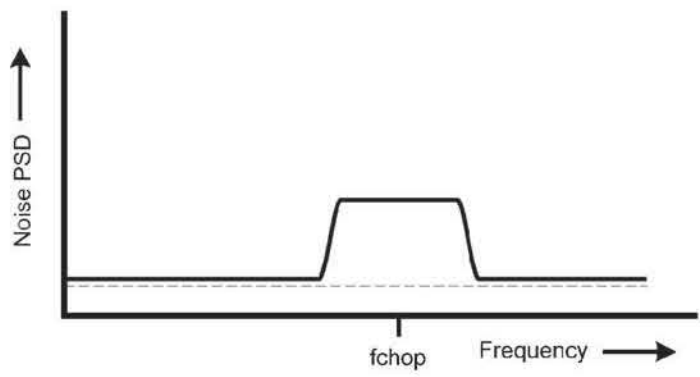


Fig. 10

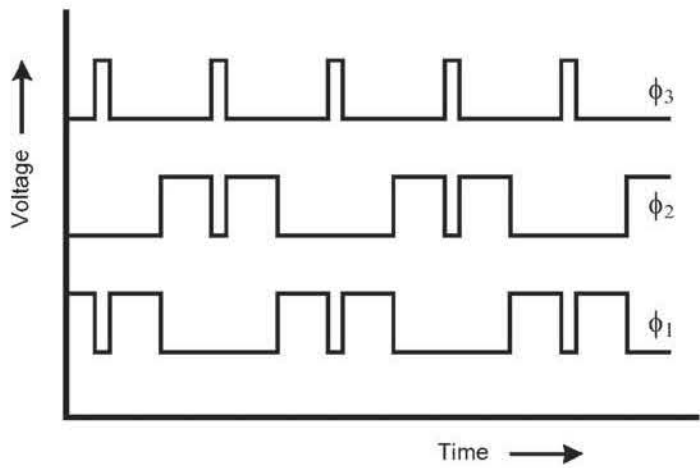
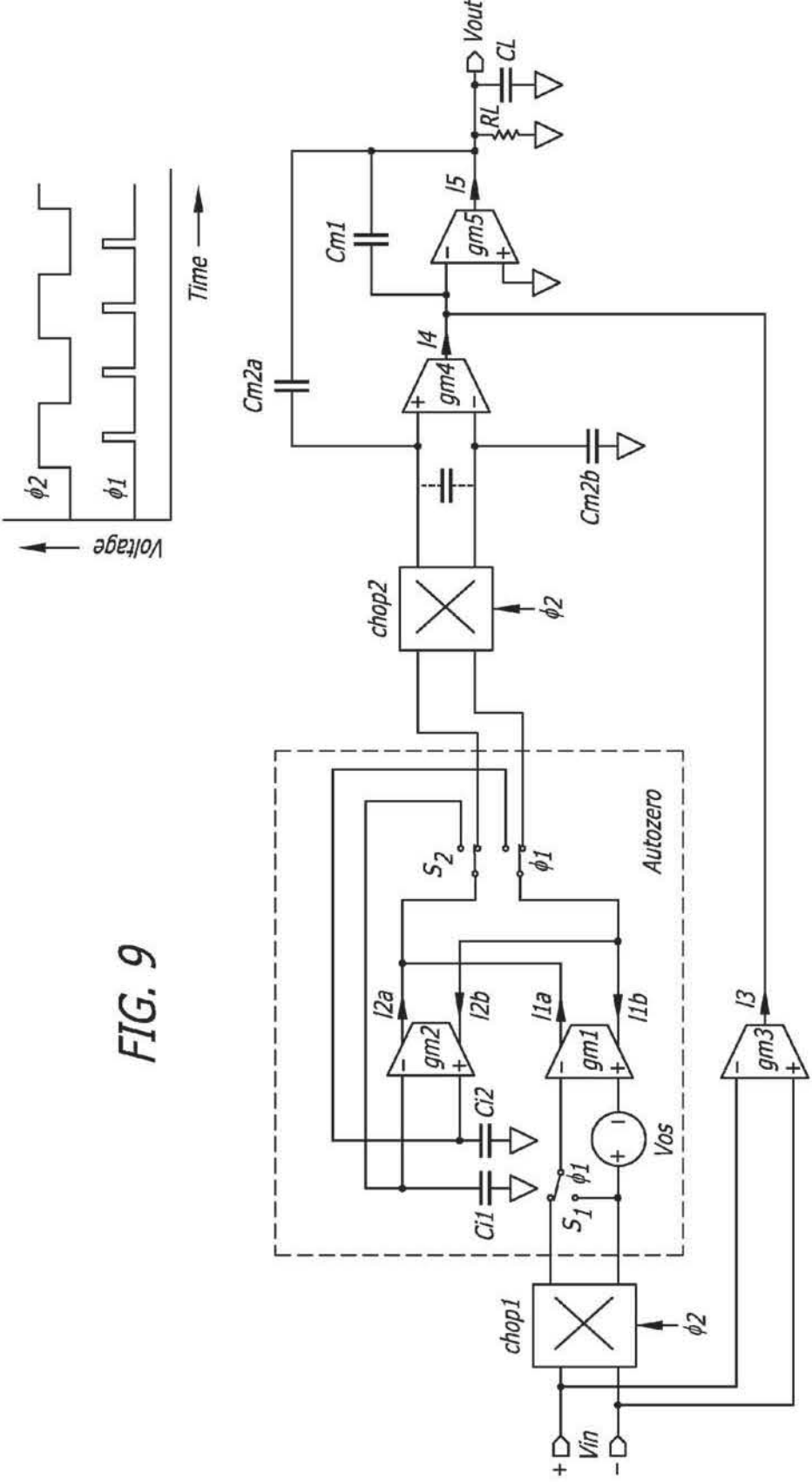


Fig. 14



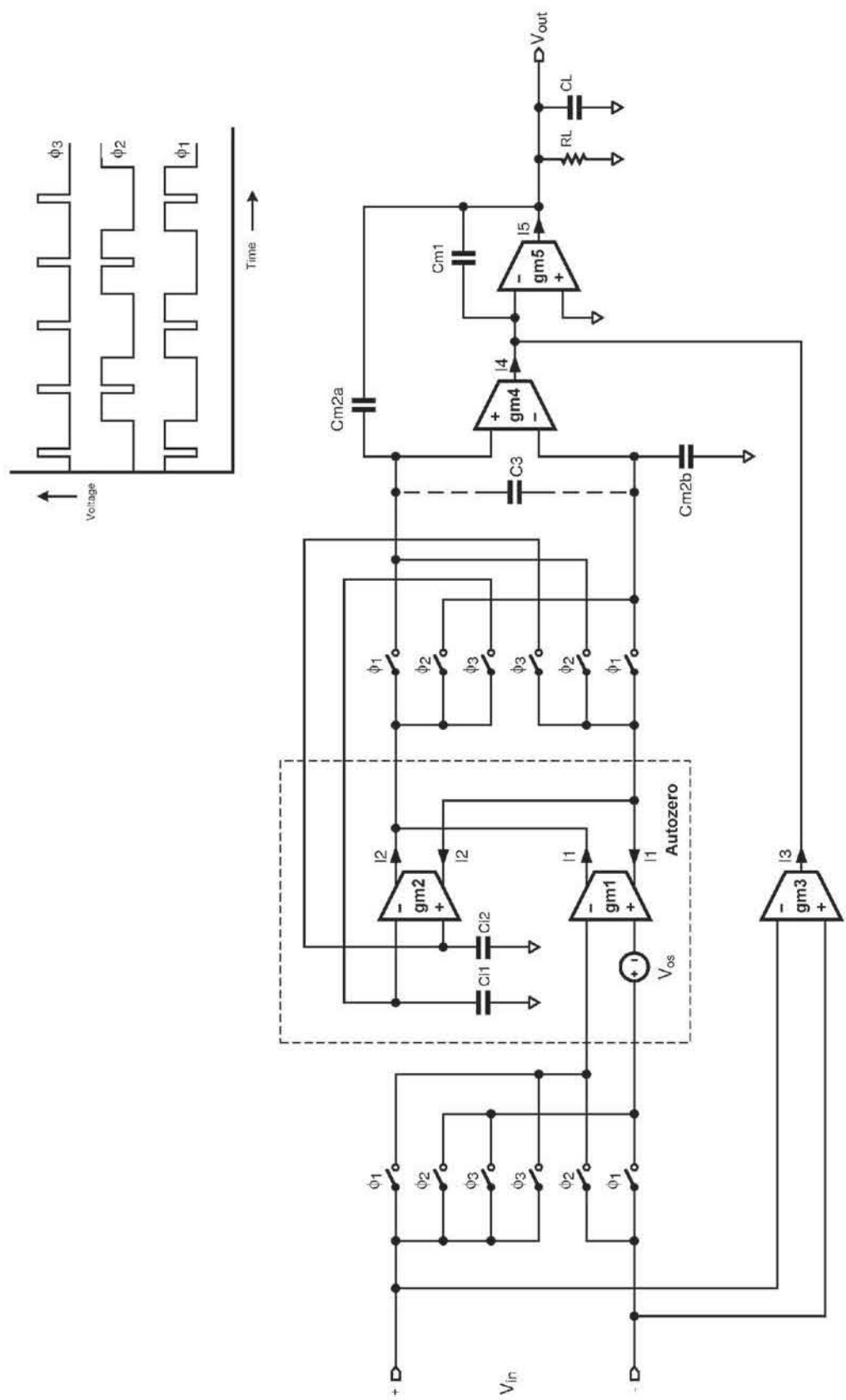


Fig. 11

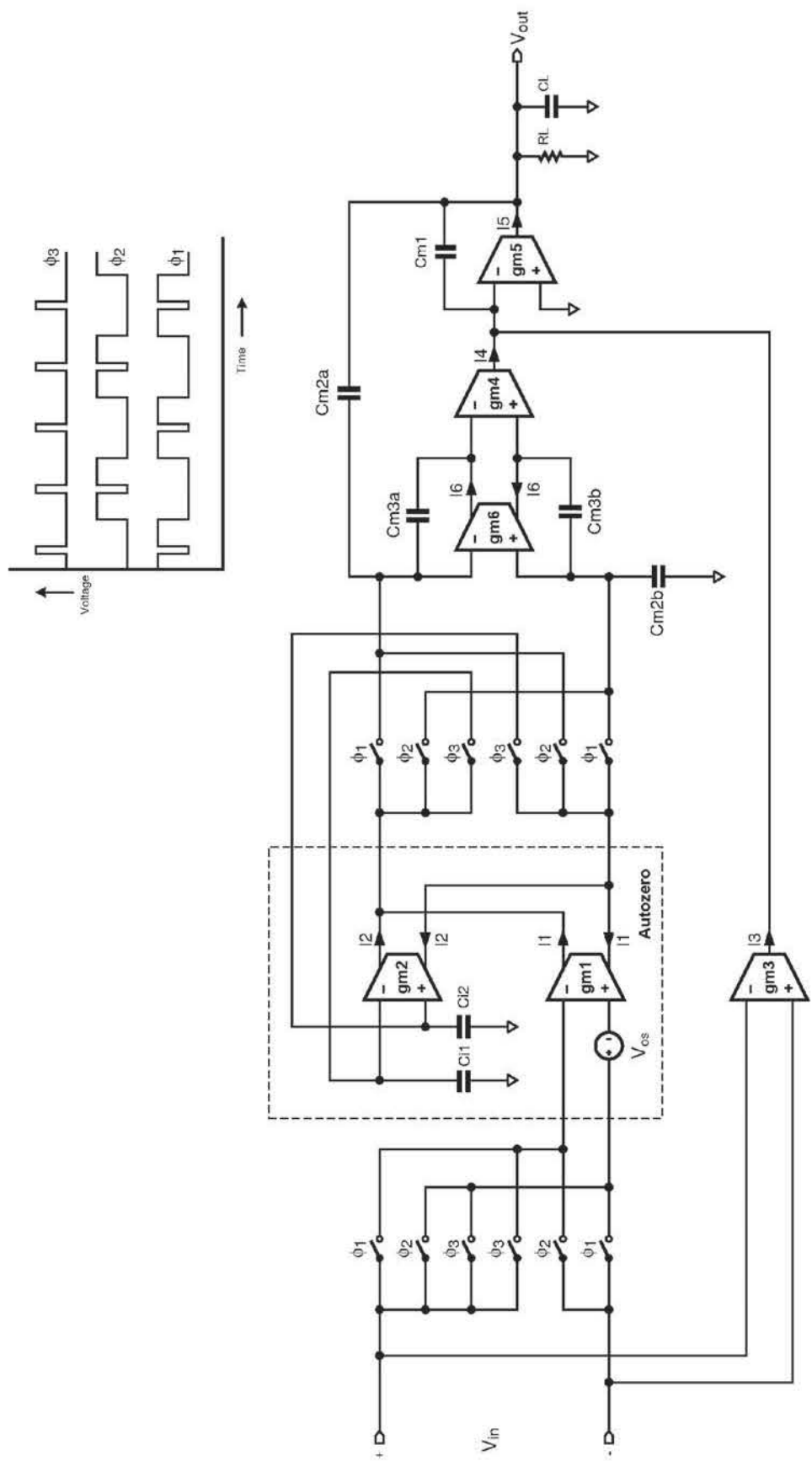
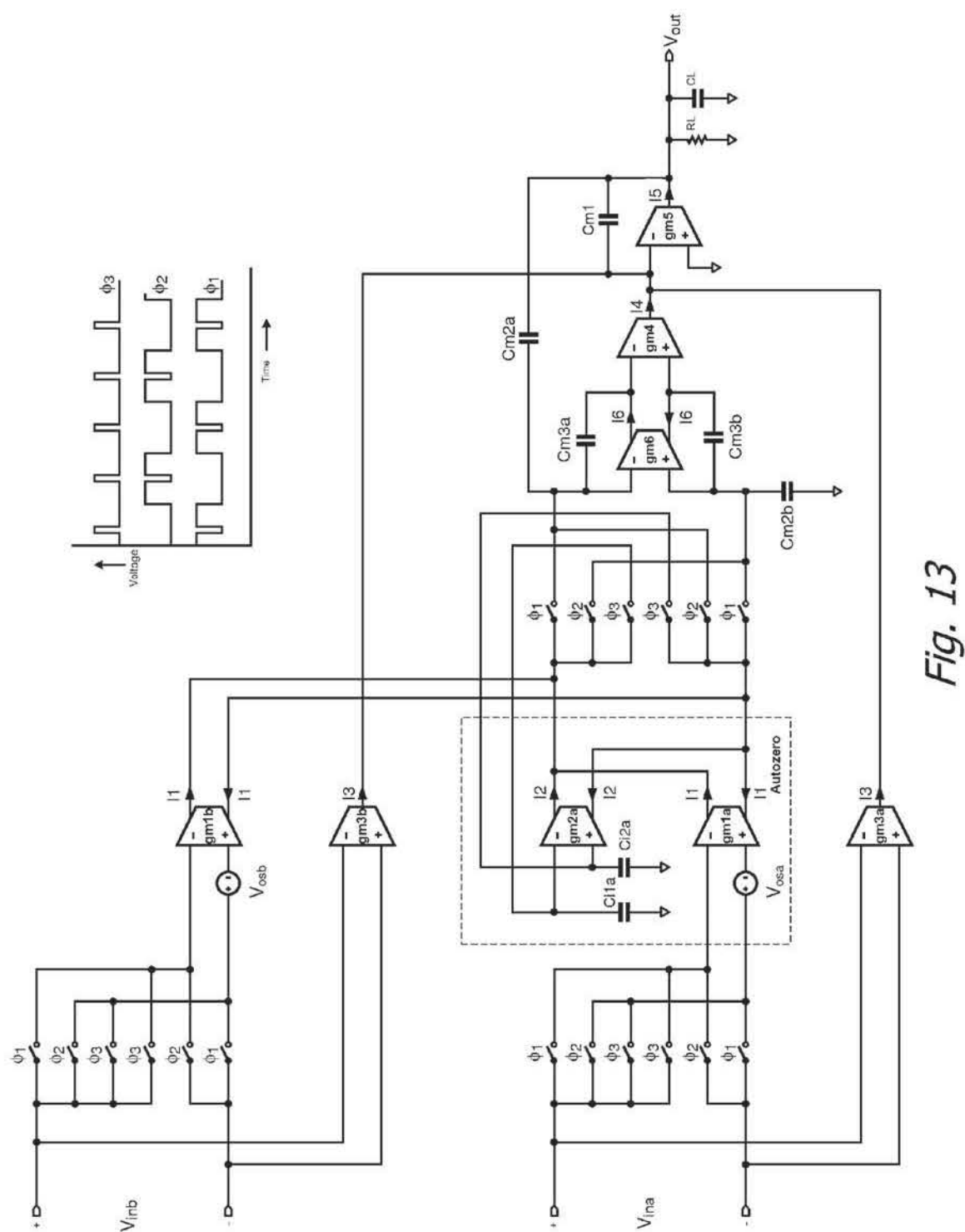


Fig. 12



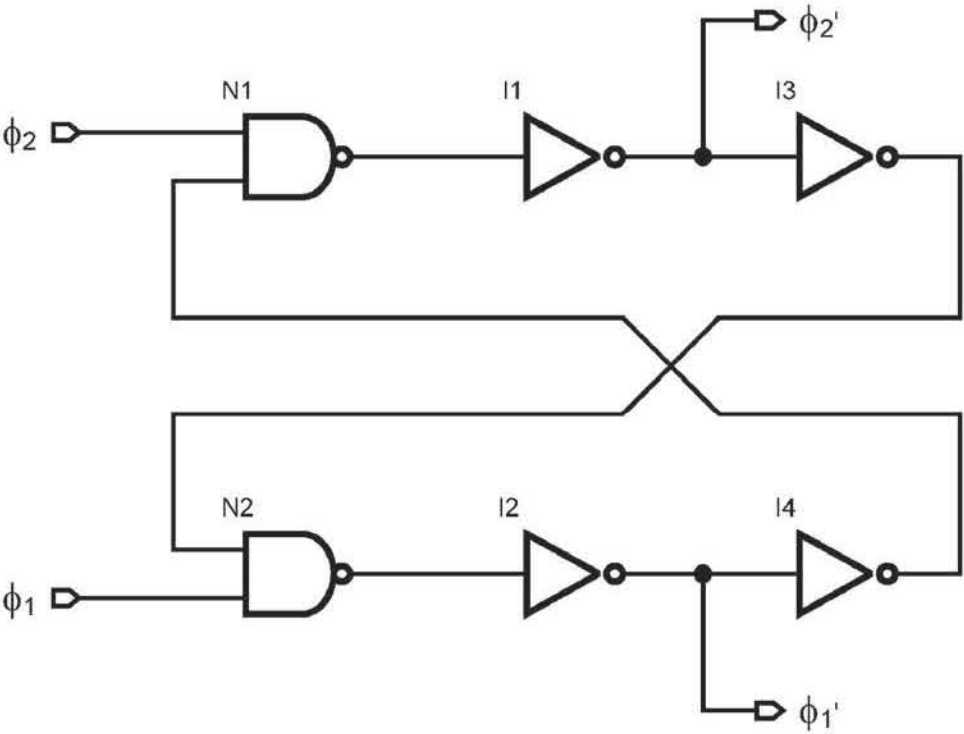


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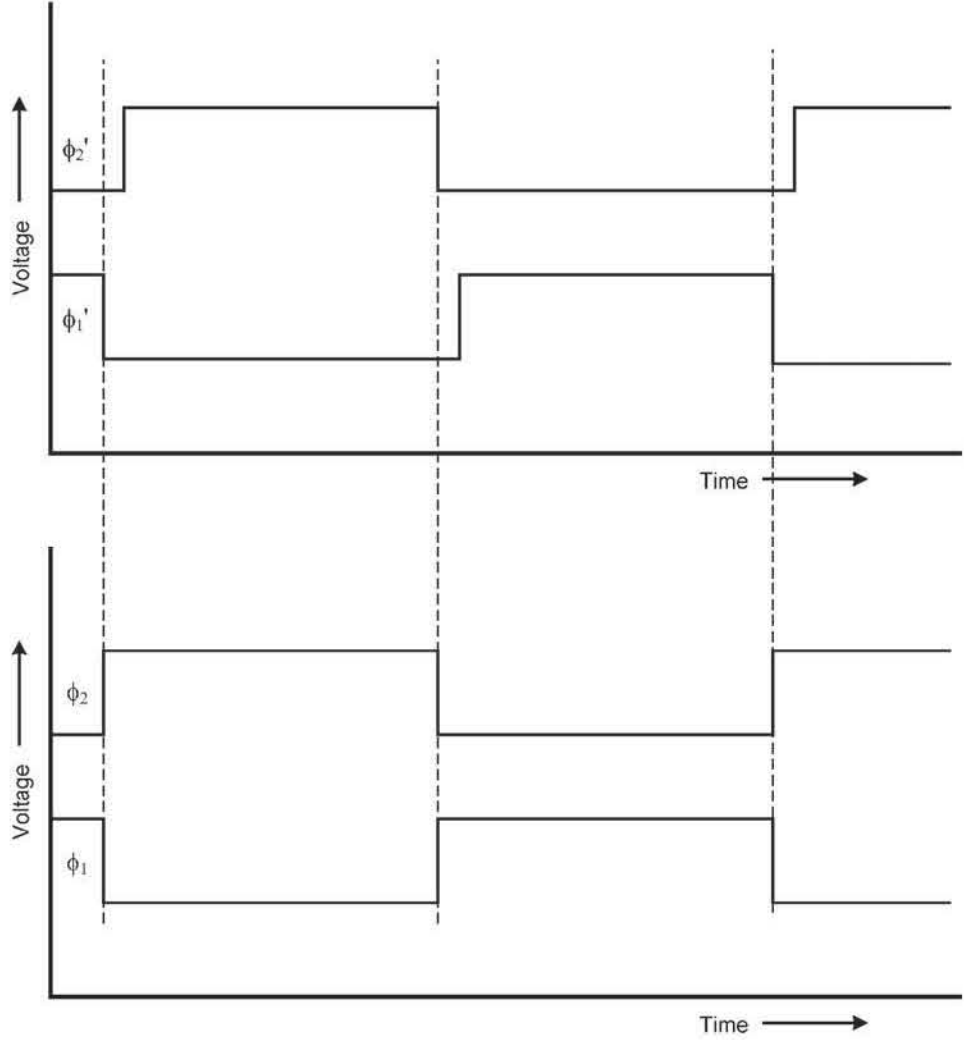


Fig. 16 (Prior Art)

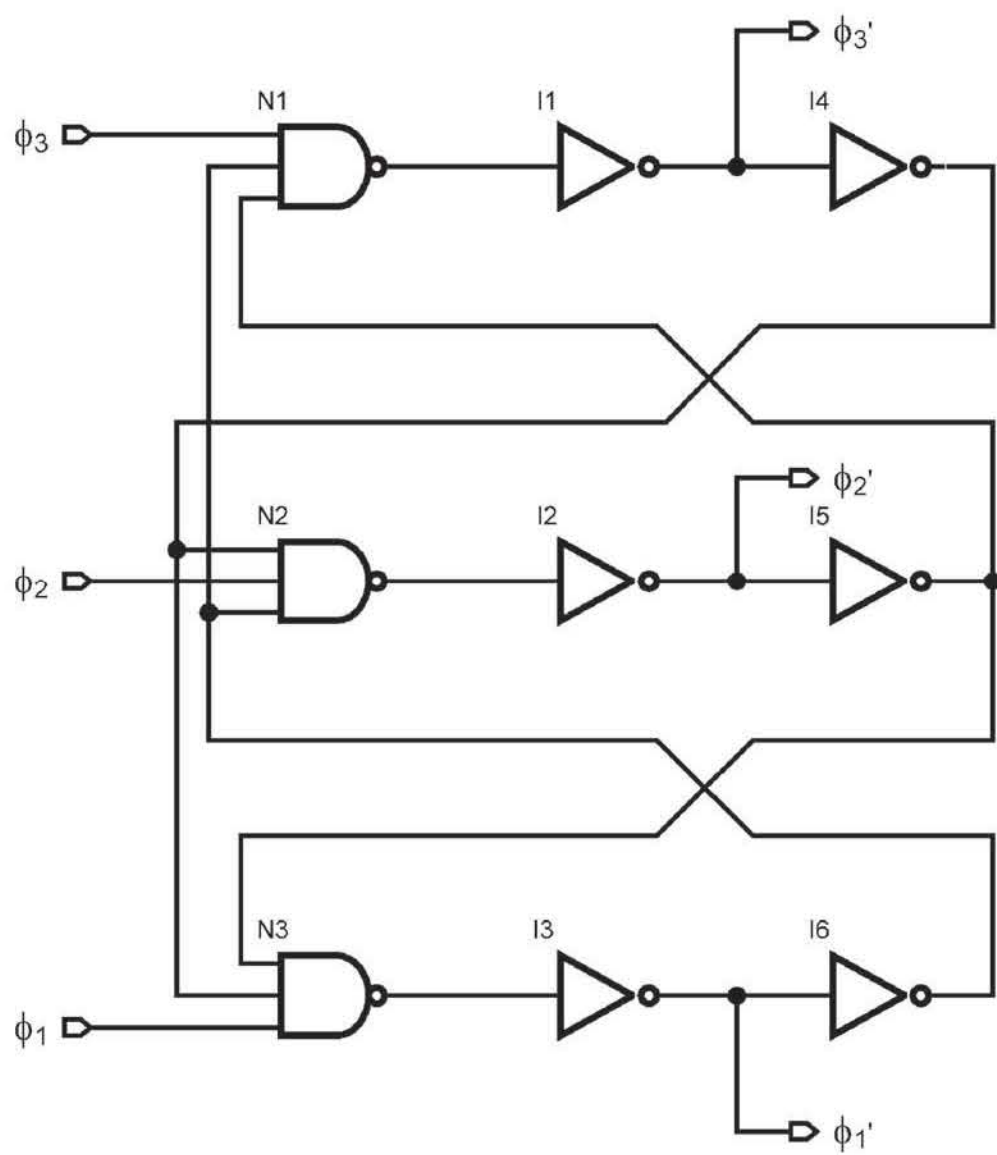


Fig. 17

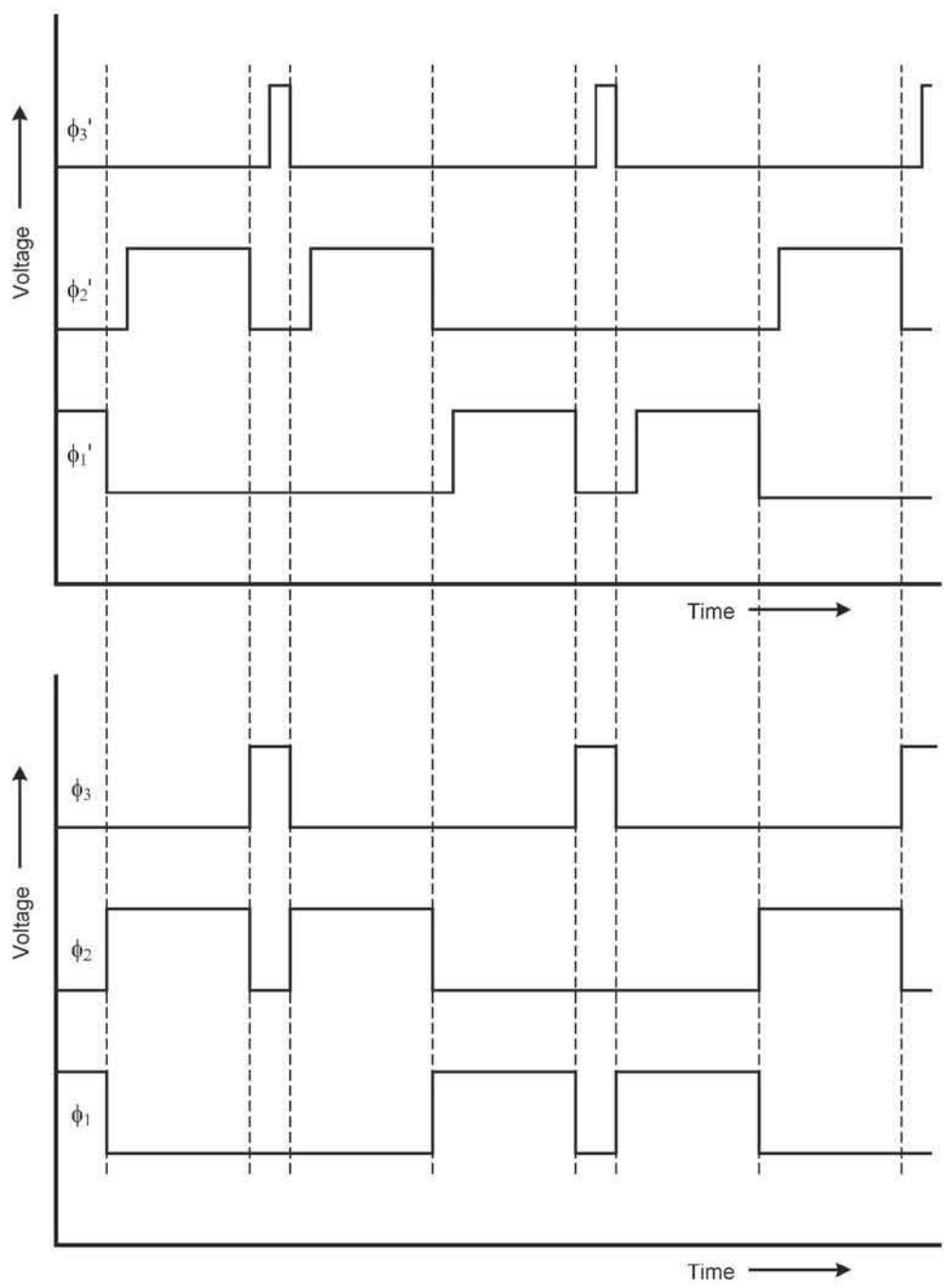


Fig. 18

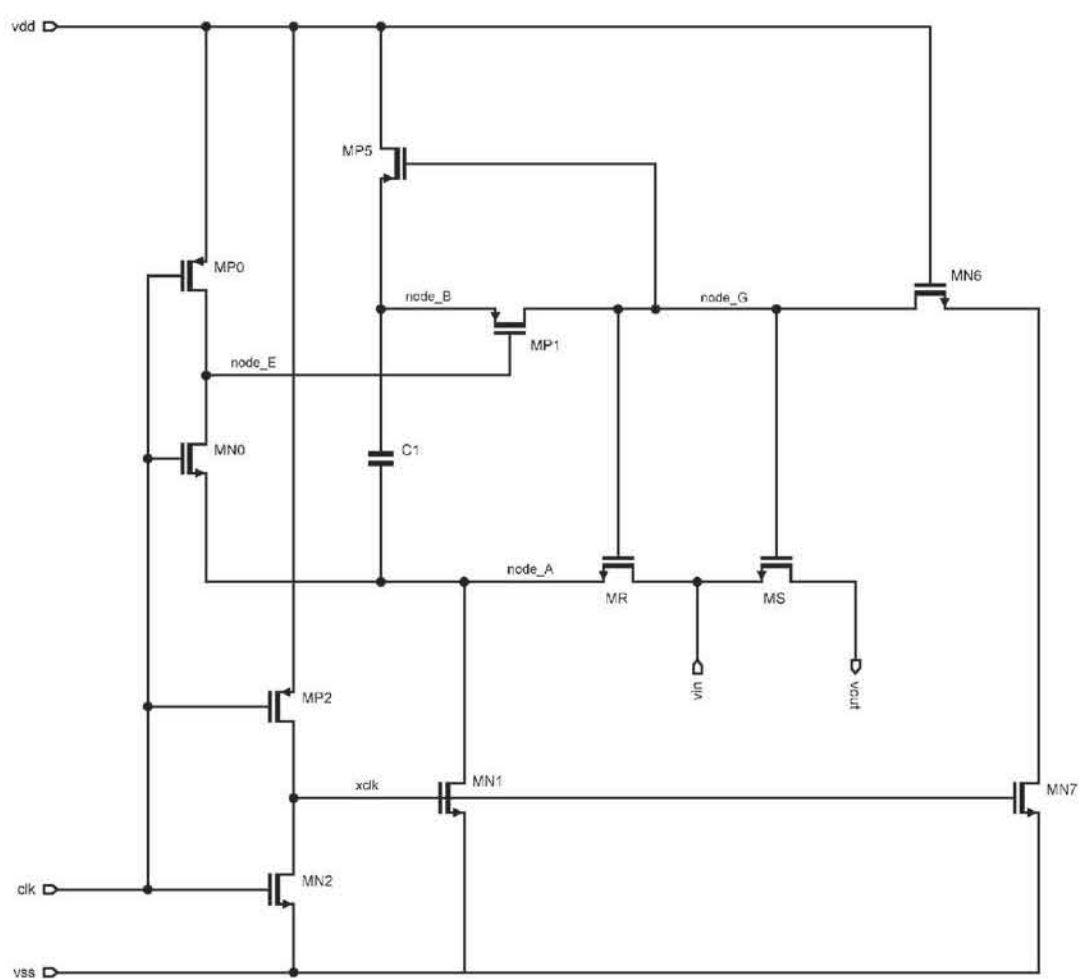


Fig. 19 (Prior Art)

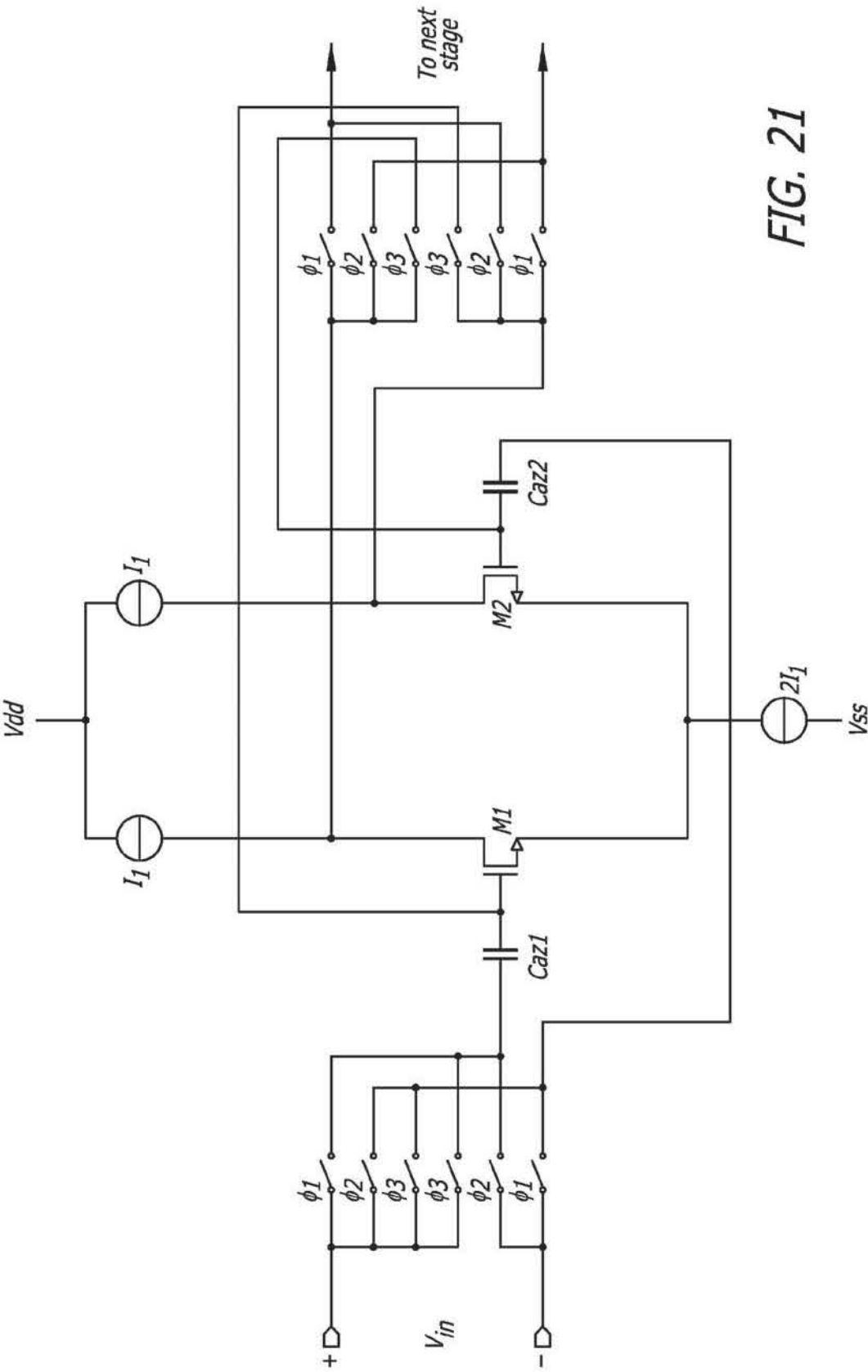


FIG. 21

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LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of operational and instrumentation amplifiers.

2. Prior Art

One of the key performance specifications of an operational amplifier is its DC error or offset voltage. The offset voltage limits the ability of the amplifier to resolve small DC input voltages. The total offset voltage is usually specified assuming a single source of error at the input terminals. The value of this imaginary voltage source represents the input referred offset voltage of the amplifier. The significance of this parameter lies in the fact that the amplifier will not be able to resolve any DC voltages at its input that are smaller than the input referred offset voltage.

In monolithically integrated operational amplifiers, the input referred offset voltage (also called input offset, offset voltage or just offset for short) is mostly due to statistical mismatch between critical components in the circuit. Commonly, these critical components include the input stage transistors, but other devices may contribute significantly to the offset as well. Typical offset voltages due to component mismatch lie in the order of several millivolts.

In the past, many techniques have been proposed and implemented to limit the effect of statistical mismatch on the input referred offset voltage. These techniques fall into one of two categories (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", C. C. Enz and G. C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, November 1996, pp. 1584-1614).

1. Chopper Stabilization

2. Autozeroing

The following will address each of these techniques, along with their respective advantages and disadvantages.

Chopper Stabilization

Chopper stabilization relies on periodically swapping the signal paths for the negative and positive input terminals of the amplifier. On average, this causes the offset between the two terminals to even out (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", C. C. Enz and G. C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, November 1996, pp. 1584-1614). FIG. 1 shows the block diagram of a chopper stabilized amplifier.

The input referred offset voltage of the input stage g_{m1} is represented by voltage source V_{os} . The behavior of the choppers is to multiply their input signal by +1 or -1, depending on the state of clock phase ϕ_2 . In the case of a differential signal (e.g. chopper chop₁), multiplying by -1 simply means swapping the input signals. Multiplying by +1 indicates direct connections between inputs and outputs.

Note how for one clock phase the input offset source V_{os} will cause a negative error voltage at the output, while for the other phase the effect will be a positive voltage. The net output error voltage, averaged over time, will be zero.

For the input signal the situation is different. In this case the signal passes to both choppers chop₁ and chop₂, and the polarity of the output signal will not change. Therefore, the output signal will consist of the unmodified input signal, and a ripple voltage caused by chopping by chopper chop₂ of the input offset voltage V_{os} .

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Alternatively, in the frequency domain the choppers chop₁ and chop₂ can be regarded as multipliers or mixers, shifting the input frequencies by the chopper frequency f_{chop} . From this point of view, chopper chop₁ will convert up a DC input signal to the chopper frequency f_{chop} . Input stage g_{m1} will then amplify the resulting signal at f_{chop} , while chopper chop₂ converts the signal back to DC. Note that the DC input signal reappears as a DC signal at the output of chopper chop₂. This is because at this point the signal has passed through two choppers, implementing up and down conversion of the input signal.

The situation for the offset source V_{os} is different, however. Since there is only one chopper between the offset source V_{os} and the output, the DC offset voltage V_{os} will get up converted to the chopper frequency f_{chop} at the output. By low pass filtering (or averaging) the output the effect of the offset source V_{os} can then be eliminated.

Besides to the DC offset, the same frequency up conversion applies to any 1/f or low frequency noise of input stage g_{m1} . Therefore, the 1/f noise is shifted out of the signal band in the same way the DC offset is.

The gain stages g_{m1} , g_{m4} and g_{m5} comprise the chopped signal path. Since DC offset is—by definition—a low-frequency phenomenon, the chopped signal path does not require a very high bandwidth. Instead, the parallel input stage g_{m3} is added to the circuit to deal with high frequency signals. Together, input stages g_{m1} and g_{m3} handle the entire spectrum from DC up to the bandwidth of the amplifier. Capacitors C_{m1} and C_{m2} implement frequency compensation to ensure stability when applying feedback to the amplifier, as well as a smooth transition between the high and low frequency portions of the amplifier gain. This frequency compensation setup is based on Multipath Nested Miller Compensation (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.1, Boston, Mass.: Kluwer, 1995, section 6.1, Boston, Mass.: Kluwer, 1995).

A significant benefit of the chopping technique, besides its effectiveness in reducing offset and 1/f noise, is that the noise power density spectrum (PSD) at low frequencies approaches the thermal noise limit of the amplifier without choppers.

The main disadvantage of chopping is that the output spectrum of the chopper stabilized amplifier will show a sharp peak around the chopper frequency f_{chop} (FIG. 2).

This noise peak is caused by the up conversion of the offset voltage and 1/f noise of the input stage g_{m1} , and corresponds to the ripple voltage at the output of the amplifier in the time domain.

Autozeroing

Autozeroing includes techniques that calibrate out the input offset by measuring the offset, storing it into some kind of internal memory, and then compensating for the error during normal operation. This process is very similar to zeroing a weighing scale for example. The moment of calibration can be during manufacturing, in which case the measured offset needs to be stored onto a non-volatile memory, to ensure that the measured offset value does not disappear after the part is powered down. Alternatively, the autozeroing can be performed during normal operation, by periodically interrupting the signal path for a brief calibration. In this case, the measured voltage needs to be retained for a short amount of time only, allowing the use of volatile memory, or even a capacitor to store the value. The advantage of autozeroing during normal operation is that as the offset of the amplifier shifts, e.g. due to temperature changes or aging, the autozeroing will track the changes and continue to compensate for it.

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Autozeroing during manufacturing does not compensate for varying conditions, and is therefore susceptible to offset drift.

FIG. 3 shows the simplified block diagram of an amplifier using autozeroing to reduce its offset.

It comprises of input stage g_{m1} with its associated input referred offset voltage source V_{os} . The switches S_1 and S_2 , transconductor g_{m2} and capacitor C_i implement the autozero function. When clock phase ϕ_1 is high (autozero), switch S_1 shorts the input terminals of input stage g_{m1} . Switch S_2 closes a feedback loop around stage g_{m2} , which forces the output voltage of input stage g_{m1} to zero. After the feedback loop settles, the voltage on autozero capacitor C_i counteracts the input referred offset voltage V_{os} .

The moment clock phase ϕ_1 goes low (normal operation), switch S_2 opens the feedback loop around transconductor g_{m2} . Because of the high input impedance of transconductor g_{m2} , the voltage across the autozero capacitor C_i remains constant (sample-and-hold), and continues to compensate for the offset voltage V_{os} .

With clock phase ϕ_1 low, input switch S_1 goes from shorting out the input stage g_{m1} to directly connecting the input terminals of the amplifier to the input stage g_{m1} . Input stage g_{m1} now operates as a normal input stage, connected between the input terminals of the amplifier and the subsequent gain stages g_{m4} and g_{m5} . As a result of the calibration in the previous clock phase, the small current I_2 that transconductor g_{m2} adds to the output current of input stage g_{m1} exactly compensates for the error current at the output of g_{m1} due to offset voltage V_{os} . In other words, the autozero current I_2 effectively eliminates the input referred offset voltage V_{os} of the amplifier.

Besides eliminating DC offset, the autozero process is also very effective against low-frequency or $1/f$ noise. This noise component can be regarded as a slowly varying offset voltage, and as long as the amplifier is autozeroed with short enough intervals, any $1/f$ noise will be removed in the same fashion DC offset is.

The autozeroed amplifier in FIG. 3 separates high and low frequency signals and processes them through two parallel signal paths, as was the case with the chopper stabilized amplifier of FIG. 1. The gain stages g_{m1} , g_{m4} and g_{m5} comprise the low-frequency autozeroed signal path, while the parallel input stage g_{m3} deals with high frequency signals. Capacitors C_{m1} and C_{m2} again implement Multipath Nested Miller Compensation (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.1, Boston, Mass.: Kluwer, 1995., section 6.1, Boston, Mass.: Kluwer, 1995), ensuring stability and a smooth frequency response.

Although autozeroing according to FIG. 3 is a simple and effective method to reduce the input offset, it greatly deteriorates the noise properties of the amplifier due to a process called wide-band noise sampling (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", C. C. Enz and G. C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, November 1996, pp. 1584-1614).

Wide-band noise sampling, which is inherent to any sample-and-hold action, is caused by the fact that the instantaneous noise value at the output of input stage g_{m1} (and also autozero stage g_{m2}) is sampled by autozero capacitor C_i and held for the entire period that ϕ_1 is low (normal operation). The sampling of the noise takes place by switch S_2 and capacitor C_i , which are both components with a bandwidth that far exceeds the bandwidth of the amplifier. Therefore, the noise is sampled with a very high bandwidth, which results in a corresponding high rms value (or standard deviation σ) of

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the sampled noise voltage in the time domain. As a result, the sampled voltage on autozero capacitor C_i at the end of each autozero period shows a significant random variation. This variation causes a random input referred offset voltage that changes at the end of each autozero interval, and is then kept constant throughout an entire period of normal operation.

In the frequency domain, this wide-band noise sampling causes an increase in the noise floor for low frequencies (see FIG. 4).

The corner frequency ω_c of this elevated noise band is set by the bandwidth of the autozero loop through transconductor g_{m2} , switch S_2 and autozero capacitor C_i and equals g_{m2}/C_i .

In the circuit of FIG. 3, there is also another, second, source of wide-band noise sampling. This is due to the sample-and-hold action of switch S_2 and the integrating capacitor C_{m2} during the autozero period. As a result, the noise floor beyond the corner frequency of the autozero loop will also be higher compared to the thermal noise limit of the amplifier without autozeroing. The bandwidth of this sampled noise spectrum is approximately equal to the frequency at which the amplifier is autozeroed (and lies beyond the maximum frequency on the X-axis of FIG. 4).

The noise power spectral density (or PSD) of the overall amplifier is shown in FIG. 4. Due to the multiple sample-and-hold actions in the circuit, the overall noise density is significantly higher than the thermal noise limit of the circuit without autozeroing. For low frequencies, the noise increase is especially noticeable, and in practice can be a factor 10 or more. Note that compensating for this elevated noise level by lowering the thermal noise of g_{m1} (and g_{m2}), would mean that the currents in these stages will have to go up by the same factor 10. In many cases such a large supply current increase will turn out to be an unacceptable impact to the total power budget of the amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a Prior Art chopper stabilized amplifier.

FIG. 2 illustrates the Noise Power Spectral Density (PSD) of a Prior Art chopper stabilized amplifier.

FIG. 3 is a block diagram of a Prior Art autozeroed amplifier.

FIG. 4 illustrates the Noise PSD of a Prior Art autozeroed amplifier.

FIG. 5 is a block diagram of one circuit combining the advantages of chopping and autozeroing in a single amplifier.

FIG. 6 illustrates the Noise PSD of the amplifier of FIG. 5 with both chopping and autozeroing.

FIG. 7 is a block diagram of an Amplifier combining chopping and autozeroing with a ping-pong autozeroed input stage.

FIG. 8 illustrates the Noise PSD of the amplifier with ping-pong autozeroing.

FIG. 9 is a block diagram of an Amplifier combining chopping and autozeroing with reduced wide-band noise sampling.

FIG. 10 illustrates the Noise PSD of the chopped and autozeroed amplifier with improved clocking scheme of FIG. 9.

FIG. 11 is a block diagram of a Simplified chopped and autozeroed amplifier.

FIG. 12 is a block diagram of a Chopped and autozeroed amplifier using Multipath Hybrid Nested Miller Compensation.

FIG. 13 is a block diagram of an Instrumentation amplifier with chopping and autozeroing.

FIG. 14 illustrates the Clock phases of the chopped and autozeroed amplifier of FIG. 13.

FIG. 15 presents a Prior Art Circuit for generating two-phase non-overlapping clock signals.

FIG. 16 illustrates the two-phase non-overlapping clock signals of the Prior Art circuit of FIG. 15.

FIG. 17 presents a circuit for a three-phase non-overlapping clock generator.

FIG. 18 illustrates the three-phase non-overlapping clock signals for the circuit of FIG. 17.

FIG. 19 presents a Prior Art circuit for a Bootstrapped input switch circuit.

FIG. 20 presents a circuit for an improved bootstrapped switch with reduced switching glitch and die area.

FIG. 21 illustrates an alternative form of autozero circuit using a single differential amplifier.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the attached drawings, for reference, in instances where it matters, all switches are shown in states for a respective low control signal. In that regard, the word switch is used herein and in the following claims in both the singular and the plural sense, and in the sense to include an on/off switch or switches, and switches that alternately connect one line to either of two other lines. However when used in the plural sense, each such switch is responsive to the same control signal. Also the word amplifier as used herein means an amplifier of one or more stages, and may include frequency compensation.

Table 1 summarizes the properties of the chopping and autozeroing techniques for reducing the DC offset and 1/f noise of an amplifier.

TABLE 1

Properties of chopping and autozeroing.		
	Advantage	Disadvantage
Chopping	Low-noise	Output ripple
Autozeroing	No output ripple	Wide-band noise sampling

Clearly, each of the techniques has its own set of advantages and disadvantages. Chopping results in low noise, but causes a significant output ripple, while autozeroing suffers from wide-band noise sampling, and hence high noise, but does not generate a ripple at the output.

Ideally, we would like to find an alternative approach that combines the advantages of chopping and autozeroing, i.e. low noise and small output ripple. FIG. 5 shows a first attempt at such a technique.

The circuit consists of autozeroed input stage g_{m1} that is "embedded" between the two choppers $chop_1$ and $chop_2$. The order of operation of the various parts is as follows. When clock phase ϕ_1 is high, input stage g_{m1} is being autozeroed by switch S_2 , transconductor g_{m2} and autozero capacitor C_f . When clock phase ϕ_1 goes low, input stage g_{m1} enters normal operation, while the output current of transconductor g_{m2} compensates for its input referred offset V_{os} . During this half cycle of normal operation, the two choppers $chop_1$ and $chop_2$ will go through a full clock cycle ϕ_2 , averaging out any remaining offset of autozeroed input stage g_{m1} . The cycle repeats by clock phase ϕ_1 going high again, entering the amplifier into autozero.

At first sight, the circuit of FIG. 5 seems to have many advantages over only chopping or only autozeroing. Because

the offset V_{os} of g_{m1} is already autozeroed, chopping by $chop_2$ does not introduce any output ripple. Also, because the choppers shift any low-frequency noise of the autozeroed input stage g_{m1} to the chopper frequency f_{chop} , the effect of the wide-band noise sampling by autozero capacitor C_f is greatly eliminated. This can be seen in the noise it is shifted to the PSD of FIG. 6.

Clearly, the low frequency noise resulting from the wide band noise sampling by autozero capacitor C_f is shifted to the chopper frequency f_{chop} . Finally, since both the autozeroing and chopping contribute to reducing the offset, the resulting input referred offset can be much lower than by using chopping or autozeroing alone.

The noise PSD of FIG. 6 also shows the main disadvantage of the combined autozeroed and chopped circuit of FIG. 5. Notice how the overall noise floor is raised significantly above the thermal noise limit of the amplifier. This elevated noise floor is entirely due to the sample-and-hold action of switch S_2 and Miller capacitor C_{m2} . While the input stage is being autozeroed (clock phase ϕ_1 is high), the normal signal path is being interrupted. During this time, the voltage across Miller capacitor C_{m2} , holding the value at the time switch S_2 opened, will determine the output voltage of the amplifier. The sample-and-hold effect of switch S_2 and Miller capacitor C_{m2} again gives rise to wide-band noise sampling. It can raise the overall noise floor by a factor 10 or more, all the way up to the autozero frequency f_{az} (which is beyond the range on the x-axis of FIG. 6).

A simple way to avoid the wide-band noise sampling in the circuit of FIG. 5 is shown in FIG. 7.

Here, the input stage of the amplifier is implemented using two independent transconductors g_{m1a} and g_{m1b} in a so-called ping-pong setup. The two input transconductors are alternately being autozeroed. While one transconductor is in its autozero mode, the other will provide a signal path between the input terminals and the intermediate stage g_{m4} , and vice versa. As a result, the normal signal path will never be interrupted, and no wide-band noise sampling takes place on the Miller capacitor C_{m2} . This is apparent from the noise PSD in FIG. 8.

For low frequencies, the noise of the ping-pong circuit is identical to the thermal noise of the amplifier without chopping and autozeroing. The noise bump due to the autozeroing of g_{m1a} and g_{m1b} is shifted to the chopper frequency f_{chop} by the two choppers $chop_1$ and $chop_2$, as was the case in the circuit of FIG. 5.

Although the noise PSD of FIG. 8 approaches the ideal of low-noise and low output voltage ripple, this performance comes at a considerable price in terms of die area and power consumption. Because of the ping-pong structure, the input stage almost doubles in size and supply current. Since both area and supply current of the input stage are key in obtaining a low thermal noise floor, the die size and power penalty of doubling the input stage will be unacceptable in many practical cases.

An alternative approach to combining the advantages of chopping and autozeroing, without the die size and power penalty of a ping-pong autozeroed input stage, is shown in FIG. 9.

This circuit is similar to the circuit of FIG. 5, but employs a modified clocking scheme. Instead of the autozero clock phase ϕ_1 running at half the chopping frequency f_{chop} , it now operates at twice the chopping frequency f_{chop} . Also, the duty cycle is such, that the autozero time is substantially shorter than the time the input stage provides a normal signal path. Thus the duty cycle of ϕ_1 is preferably less than 50%, and is more preferably not more than 25%. The result is that each

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half cycle of the choppers is interrupted by the auto-zeroing, though for less than one half of each half cycle of the chopping. This is also preferred for the embodiments of FIGS. 11, 12 and 13.

By placing the autozero pulse in the middle of each half cycle of the chopper clock phase ϕ_2 , chopper C_{hop2} will average out any residual offset after autozeroing in the time between two autozero pulses. This residual offset averaging stems from the fact that during a period between two autozero pulses, the signal is passed through chopper $chop_2$ directly and with reversed polarity with the same duration.

The modified clocking scheme substantially reduces the wide-band noise sampling by switch S_2 and Miller capacitor C_{m2} . Even though the hold voltage on Miller capacitor C_{m2} after opening S_2 still has the same large random variation as was the case in the circuit of FIG. 5, limiting the time this random voltage affects the signal path, greatly reduces its overall effect. This is shown in FIG. 10.

By choosing a suitably small autozero duty cycle, the overall noise increase due to the wide-band noise sampling can become arbitrarily small. In practice, by choosing a duty cycle less than 10% the noise floor of the circuit will be within several percent of the theoretical thermal noise floor limit.

FIG. 11 shows a simplification of the circuit in FIG. 9.

Notice how in the previous circuit of FIG. 9 the autozero switches and internal chopper switches are connected in series, each with their own clocking phases. The circuit of FIG. 11 combines these series connections of switches into one switch where possible, and provides the proper clocking phases to drive them.

Operation is as follows. The first state of the circuit is when clock phase ϕ_3 is high; the circuit is in autozero mode, with the switches labeled ϕ_3 closed. As a result, the inputs of transconductor g_{m1} are both tied to the positive input terminal. Hence, the input differential voltage of g_{m1} is zero, while the voltage at the positive input sets the common-mode voltage. The output terminals of input transconductor g_{m1} are connected to the autozero capacitors C_{i1} and C_{i2} , closing the autozero loop.

The second state occurs after clock phase ϕ_3 goes low again. Now there are two possible situations: either clock phase ϕ_1 goes high, while phase ϕ_2 remains low, or vice versa. Assuming the first case, ϕ_1 high and ϕ_2 low, input stage g_{m1} is connected directly between the input terminals and the intermediate stage g_{m4} . Offset voltage source V_{os} will cause a positive error voltage at the output of the amplifier. The two autozero capacitors C_{i1} and C_{i2} are disconnected from the signal path and hold their voltage to cancel out any offset of input stage g_{m1} .

The circuit enters its third and final state when ϕ_1 and ϕ_2 reverse polarities (ϕ_1 low and ϕ_2 high). In this situation, input stage g_{m1} is effectively turned upside down, swapping both the input and output terminals. The polarity of the signal path remains the same, but the effect of input offset voltage V_{os} at the output changes sign: it will cause a negative excursion of the output voltage.

Since states two and three have the same duration, the average effect of the offset source V_{os} will be zero. State 1 is effectively operating at twice the frequency of states 2 and 3, though states 2 and 3 are each interrupted by state 1, with each half cycle of the chopping being temporarily interrupted by the auto-zeroing process.

The order of states two and three after each autozero pulse ϕ_3 alternates. This results in the following overall order of the circuit states: 2-1-2, 3-1-3, 2-1-2 etc. The average (residual) offset across one autozero cycle, whether it is the 2-1-2 or the 3-1-3 cycle, will be zero.

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Input stage g_{m3} again implements a separate signal path for high frequencies. Together with capacitors C_{m1} , C_{m2a} and C_{m2b} , this parallel input stage g_{m3} implements Multipath Nested Miller Compensation (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.1, Boston, Mass.: Kluwer, 1995). This frequency compensation technique ensures stability when applying feedback to the overall amplifier, while enabling a smooth frequency response without artifacts in the cross-over region between the high and low frequency signal paths. Capacitor C_3 is an optional component that can help the gain of the low-frequency signal path (g_{m1} , g_{m4} and g_{m5}) to drop off steeply enough at high frequencies not to interfere with the high-frequency signal path through parallel input stage g_{m3} .

A final refinement of the circuit in FIG. 11 is shown in FIG. 12.

This circuit is identical to the circuit of FIG. 11, except for the additional gain stage g_{m6} . The purpose of this additional stage is to increase the gain of the low-frequency signal path through input stage g_{m1} . This additional gain will help to suppress any DC offset of the overall amplifier due to mismatches in the parallel input stage g_{m3} . A DC offset in the parallel input stage g_{m3} will cause an input referred offset voltage of the overall amplifier. The resulting input referred offset can be very small, however, as its effect is reduced by the ratio of the gains of the low frequency signal path and high frequency signal path. By introducing the additional gain stage g_{m6} , the circuit of FIG. 12 will offer gain ratios on the order of 10,000x or more in typical situations. Therefore, a DC offset of the parallel input stage g_{m3} of 10 mV for example, will be reduced to less than a microvolt. At these low levels, the effect of a DC mismatch in the parallel input stage g_{m3} is sufficiently small not to significantly affect the overall performance of the amplifier.

Because of the additional gain stage g_{m6} , the circuit of FIG. 12 now requires Multipath Hybrid Nested Miller compensation to guarantee stability with overall feedback applied (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.3, Boston, Mass.: Kluwer, 1995). This frequency compensation technique is similar to Multipath Nested Miller Compensation used in FIG. 11, except that it uses an active integrator with Miller capacitors C_{m3a} and C_{m3b} , as opposed to the passive filter capacitor C_3 in FIG. 11.

Instrumentation Amplifiers

By adding an additional input stage to any of the circuits in FIG. 5, FIG. 7, FIG. 9, FIG. 11 and FIG. 12, these can easily be transformed into so-called instrumentation amplifiers (see "Operational Amplifiers, Theory and Design", J. Huijsing, pp. 52-53, Boston, Kluwer Academic Publishers, 2001). Instrumentation amplifiers have two sets of differential input terminals and are capable of sensing small differential signals in the presence of a large common-mode disturbance.

In order for the chopping and autozeroing to work properly in the modified circuit, only the input stage devices (including the parallel devices for Multipath frequency compensation) and input switches need to be repeated from the original opamp. The autozeroing can be done across both input stages combined, and therefore does not require additional autozero capacitors, nor autozero feedback switches.

FIG. 13 shows the chopped and autozeroed instrumentation amplifier that results from modifying the opamp depicted in FIG. 12. The components added to the circuit are the two input stages g_{m1b} and g_{m3b} , along with the corresponding input switches.

FIGS. 5, 7 and 9 implement one form of autozero circuit, also effectively incorporated in FIGS. 11, 12 and 13, though it should be understood that other forms of autozero circuits may be used. By way of example, FIG. 21 illustrates an alternative form of autozero circuit using a single differential amplifier rather than the two of the previous embodiment. In FIG. 21, a differential transistor pair M1 and M2 each have a drain current I_1 and a common source connection having a tail current of $2I_1$. Either the drain currents or the tail current can be controlled by a common mode voltage controlled current source to achieve the desired common mode input to the gates of the transistors M1 and M2. Note that this common mode voltage is unrelated to, and can be fixed and very different from, the common mode input to the amplifier system, the difference being the voltages across capacitors Caz1 and Caz2.

Clock phases ϕ_1 and ϕ_2 are the chopper clock phases. During autozeroing, clock phases ϕ_1 and ϕ_2 are low and the clock phase ϕ_3 is high. Note that if the two drain currents I_1 are not perfectly matched, that mismatch, itself, will also cause an offset in the differential pair of transistors M1 and M2. However that offset is also autozeroed by the foregoing process so that a perfect match of the two drain current sources I_1 is not required.

In any autozero circuit, the input to the input stage is periodically disconnected and then shorted, with the offset then being stored on one or more capacitors for subtraction from the signal path between autozeroing operations. In the embodiments of FIGS. 5, 7, 9 and 11-13, a second amplifier is used, with the net input offset of both amplifiers gm1 and gm2 being stored on the capacitors on the input to the second amplifier. The offsets are cancelled by the second amplifier having a current output opposite the current output of the differential input stage when the input of the differential input stage is shorted. In the embodiment of FIG. 21, only one differential amplifier is used for the autozero operation, with the autozeroing being done by appropriately charging capacitors in series with the differential amplifier input.

Clock Generation

The clock phase ϕ_3 can be thought of as the autozero phase, while the clock phase ϕ_1 and ϕ_2 can be (broadly) thought of as the two chopper phases. One complication that arises in the circuits of FIG. 11 and FIG. 12 is that only one of the sets of switches corresponding to a particular clock phase (ϕ_1 , ϕ_2 or ϕ_3) is allowed to be closed at any particular time. Closing two or more sets of switches will cause short circuits between the various nodes of the circuit. In order to guarantee this break-before-make behavior, the switches need to be driven by non-overlapping clock phases.

A prior art circuit for generating two-phase non-overlapping clock signals is shown in FIG. 15 (see "Principles of CMOS Design", N. H. E. Weste and K. Eshraghian, section 5.5.10, Addison-Wesley, 1993).

It generates the two non-overlapping clock phases ϕ_1' and ϕ_2' from the potentially overlapping input clock phases ϕ_1 and ϕ_2 . This process is illustrated in FIG. 16.

Operation of the circuit is as follows (assuming for simplicity that all gates are delay free, except for the inverters I3 and I4). With clock phase ϕ_1 low and clock phase ϕ_2 high, the output clock phases ϕ_1' and ϕ_2' will also be low and high respectively. When the two input clock phases ϕ_1 and ϕ_2 change states (ϕ_1 transitioning to high and ϕ_2 to low), output ϕ_2' will change almost instantaneously (see FIG. 16). This direct output response occurs because when the input ϕ_2 to nand gate N1 goes low, its output will go high, regardless of the state of the other input to the nand gate. During the same transition (ϕ_1 to high and ϕ_2 to low), output ϕ_1' will respond

with a delay. One input of the nand gate N2 is held low by inverter I3. With one input low, the output of nand gate N2 will not change its output, independently of the state of the other input that is connected to input clock phase ϕ_1 . Only when the output of I3 changes, will the output of nand N2 change, and hence output ϕ_1' . Note that inverters I3 and I4 are assumed to exhibit noticeable delay, whereas all other gates are delay-free. The resulting output clock phases ϕ_1' and ϕ_2' are shown in FIG. 16. As indicated before, output ϕ_2' responds directly to the falling edge of ϕ_2 , while clock phase ϕ_1' tracks the rising edge of input ϕ_1 with a slight delay. Note how the resulting output phases ϕ_1' and ϕ_2' are never on at the same time (break before make).

The next change of input state, input clock phase ϕ_1 will go low again, and input clock phase ϕ_2 high. The process reverses, and in this case the output ϕ_1' responds directly to the falling edge of ϕ_2 , while clock phase ϕ_1' tracks the rising edge of input ϕ_1 with a slight delay. This timing again avoids overlap of the two output clock signals ϕ_1' and ϕ_2' . Note in FIG. 16 how the output clock phases always respond directly to a falling edge of the corresponding input clock phase, whereas rising edges are tracked with a slight delay. This timing property is fundamental to producing the two non-overlapping clock signals ϕ_1' and ϕ_2' .

FIG. 17 extends the operation of the non-overlapping clock generator of FIG. 15 to the three specific clock phases of FIG. 14. In the preferred embodiment, the three timing signals input to the circuit of FIG. 17 are generated by a simple state machine, and may be overlapping.

In this case, the circuit needs to make sure that none of the three output clock phases ϕ_1' , ϕ_2' and ϕ_3' will ever be high at the same time. Operation is similar to that of the circuit in FIG. 15 and illustrated in FIG. 18.

For simplicity, all components are assumed to be delay-free again, except for the inverters I4, I5 and I6.

When the input clock phase ϕ_3 is low, the output of inverter I4 is high, and the circuit part consisting of the nand gates N2 and N3, and inverters I2, I3, I5 and I6 behave identically to the prior art circuit in FIG. 15. These six components create non-overlapping clock phases ϕ_1' and ϕ_2' from the two input clock phases ϕ_1 and ϕ_2 . Since clock phase ϕ_3 was low to begin with, the result is that only one output clock phase ϕ_1' , ϕ_2' or ϕ_3' will be high at a given time.

When input clock phase ϕ_3 transitions high, the output clock phase ϕ_3' will wait for both other inputs to the nand gate N1 to become high as well, before it follows input clock phase ϕ_3 in going high. The other two inputs of the nand gate N1 will go high—albeit with some delay—because both input clock phase ϕ_1 and ϕ_2 will be low once input clock phase ϕ_3 has gone high. The delay is caused by one of the two inverters I5 and I6, depending on the state of the input clock phase ϕ_1 and ϕ_2 . If input clock phase ϕ_1 was low before the input clock transition, it will remain low, while input clock phase ϕ_2 goes from high to low. In this case the delay is caused by inverter I5. Inverter I6 becomes responsible for the delay in the situation where input clock phase ϕ_2 starts off and remains low, while input clock phase ϕ_1 makes the high-to-low transition. The delay before the output clock phase ϕ_3' goes high, results in the non-overlap time for this clock phase.

A high-to-low transition of input clock phase ϕ_3 affects output clock phase ϕ_3' almost immediately, as it causes one input to the nand gate N1 (the one connected to input ϕ_3) to go low. One low input to the nand gate is sufficient to make the output clock phase ϕ_3' go low as well, regardless of the other inputs to the nand gate N1.

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Since the circuit of FIG. 17 is symmetrical around all of its input-output pairs ϕ_1/ϕ_1' , ϕ_2/ϕ_2' and ϕ_3/ϕ_3' , the same reasoning that applies to the pair ϕ_3/ϕ_3' holds equally for the other two pairs.

The overall result of the timing in the circuit of FIG. 17, is that the clock phase outputs ϕ_1' , ϕ_2' and ϕ_3' will follow any high-to-low transition of their respective input clock phases ϕ_1 , ϕ_2 and ϕ_3 directly, while a low-to-high transition is propagated with a certain delay. FIG. 18 clearly shows how this delayed response to the rising edges creates the required three phase non-overlapping clock signals. Of course the circuit of FIG. 17 may in effect be realized using logical permutations accordingly to Boolean geometry to achieve the delay of each signal going to a first state until the both the other signals are in the second state.

Rail-to-Rail Input Switches

When operating any of the circuits FIG. 5, FIG. 7, FIG. 9, FIG. 11 or FIG. 12 at a low supply voltage while requiring a rail-to-rail input common-mode voltage range, the need arises for bootstrapped input switches. This need is especially felt when the supply voltage of the amplifier is lower than the sum of the threshold voltages of an NMOS and a PMOS device in the manufacturing process technology. Under these circumstances, we are not able to operate traditional complementary transmission gates at the inputs.

A transmission gate consists of the parallel connection of a PMOS and NMOS switch, each of which is operated by an opposite phase signal at its gate. To turn the transmission gate on, the gate of the NMOS device is pulled high, while the gate of the PMOS device is pulled low. At supply voltages below the sum of the threshold voltages of the NMOS and PMOS device, an area in the middle of the common-mode voltage range of the switch will occur where neither of the two devices can develop enough voltage across its gate-source terminals to be turned on.

The alternative to a transmission gate is to use a single NMOS or PMOS device, with a gate drive voltage that can rise above (NMOS) or drop below (PMOS) the supply voltage of the circuit. FIG. 19 shows an example of a prior art bootstrapped NMOS switch that uses a capacitor to increase the control voltage at the gate of the switching device (see "Very low-voltage digital-audio $\Sigma\Delta$ modulator with 88-dB dynamic range using local switch bootstrapping", M. Dessouky and A. Kaiser, IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 349-355, March 2001).

Operation of the bootstrapped switch is as follows. While the input terminal clk is held low (switch turned off), device M_{N7} pulls down node G (gates of the switching transistor) through cascode device M_{N6} . Switch devices MR and MS are in their off states, while capacitor C_1 is being charged to the supply voltage by devices M_{P5} and M_{N1} . Devices M_{P0} and M_{P1} are off. Stepping the control voltage clk high (turning the switch on), device M_{N0} pulls down node E, and device M_{P1} will start to conduct current. Device M_{P1} on its turn will connect the pre-charged capacitor C_1 between the gate and source of device M_R , which will also turn on. With devices M_{P1} and M_R in their on states, the gate-source voltage of the switching device M_S equals the voltage V_{dd} stored on the capacitor C_1 . With its gate-source voltage V_{gs} above the threshold voltage, the switch devices M_S will turn on.

Even though the voltages at node G and node B can rise significantly above the supply voltage (maximally twice V_{dd}), safe operation of all devices is guaranteed.

There are two apparent drawbacks of the prior art circuit in FIG. 19. The first is that the circuit requires a capacitor for each input switch. Since the disclosed circuits will be operating a total of six input switches, the six capacitors will

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represent a considerable die area penalty. Secondly, operating the switch will cause a major switching glitch in the signal path. This glitch is especially apparent while turning the switch on. In that case, device M_R is closed, while node A is still at the ground potential V_{ss} . With device M_R closed, node A needs to be lifted all the way up to the common-mode voltage level at the input terminal V_{in} . The charge needed for this voltage jump is pulled from the input terminal V_{in} , leading to the switching glitch.

The circuit of FIG. 20 alleviates the die size penalty and switching glitches associated with the prior art circuit of FIG. 19.

The circuit of FIG. 20 uses only one gate-drive capacitor C_1 to drive the two input switch devices M_{S1} and M_{S2} . Since all six input switches in FIG. 11 and FIG. 12 come in three pairs that are driven by the same clock phase, this reduces the total number of capacitors from six to three. This is not needed between stages, as the common mode voltage may be controlled (limited) so a rail to rail switching voltage may be used for these switches.

The key modification to allow driving multiple switch devices with one bootstrap circuit is the use of voltage v_{cm} as a reference to lift gate-control capacitor C_1 , instead of the source of the switch device M_S in the prior art circuit of FIG. 19. Disconnecting the sources of the switches M_{S1} and M_{S2} from the bootstrap circuit has the added benefit of avoiding the switching glitch that arose in the prior art circuit of FIG. 19.

The key to successfully operating the switch devices M_{S1} and M_{S2} in FIG. 20 lies in generating the proper common-mode voltage v_{cm} . This voltage v_{cm} is derived through source follower M_{N8} from the voltage at the sources of the input transistors M_{P6} and M_{P7} of the overall amplifier circuit, M_{P6} and M_{P7} being the differential transistor pair in a differential input stage for the amplifier system. Because of this connection, the common mode voltage v_{cm} has two important properties:

1. The voltage v_{cm} will track the minimum of the two voltages at the gates of input transistors M_{P6} and M_{P7} . This is due to the fact that the input device with the lowest gate voltage, e.g. M_{P6} , will start acting as a source follower, tracking the voltage at its gate with the source, while the other device (M_{P7} in this example) will be turned off by lack of a sufficiently high gate-source voltage V_{gs} . In a typical amplifier application, the differential input will be minimal, so that the voltage v_{cm} will accurately reflect the common mode voltage of the differential input. Note also, that only one source follower M_{N8} need be used for all switches coupled to that differential input.

2. Because of source follower M_{N8} , the common mode voltage v_{cm} can never exceed the positive rail V_{dd} , even if the tail current source of the input pair M_{P6} and M_{P7} is connected to a voltage higher than the supply voltage V_{dd} . A common situation where the input stage tail current source is tied to a higher supply voltage than the remainder of the amplifier is in amplifiers that employ a charge-pump to obtain a rail-to-rail input common-mode range. The charge pump generates a boosted supply voltage for the input stage, extending its common mode input voltage range.

Because of these two points, the circuit continues to guarantee safe operation of all devices in the circuit. The gate of the switching devices M_{S1} and M_{S2} will never be pulled higher than one supply voltage V_{dd} above the minimum of the two input voltages V_{inp} and V_{inm} . Consequently, the gate-source voltages V_{gs} of switching devices M_{S1} and M_{S2} cannot exceed the supply voltage V_{dd} . Also, node E, which is connected to v_{cm} when switch devices M_{N0} and M_R are closed,

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cannot exceed the supply voltage V_{dd} . This is critical to avoid forward biasing of the backgate diode of M_{P3} .

Operation of the circuit is similar to that of the prior art circuit in FIG. 19: when input terminal clk is low (switch turned off), device M_{N7} pulls down node G (gates of the switching transistors) through cascode M_{N6} . Switch devices M_{S1} and M_{S2} are in their off states, while capacitor C_1 is being charged to the supply voltage by devices M_{P5} and M_{N1} . Devices M_{P0} and M_{P1} are off. When the control voltage clk goes high (turning the switch on), device M_{N0} pulls down node E, and device M_{P1} will start to conduct current. Device M_{P1} in turn will connect the pre-charged capacitor C_1 between the gate and source of device M_R , which will also turn on. With devices M_{P1} and M_R in their on states, the voltage at node G will be the common-mode voltage V_{cm} plus the voltage V_{dd} stored on the capacitor. The result is that the gate-source voltages V_{gs} of the switch devices M_{S1} and M_{S2} will rise above their threshold voltages and turn the two devices on.

The embodiments shown and described herein use differential amplifiers. It should be noted that a single ended amplifier is functionally a differential amplifier with one input and/or one output connected to a circuit ground. Similarly, a chopper alternately reverses two inputs, independent of whether one is a circuit ground or not. Accordingly references herein and in the following claims to differential amplifiers is a reference that includes amplifiers with one input and/or one output connected to a circuit ground, i.e., commonly referred to as single ended amplifiers. Also the embodiments shown and described herein are shown and described with respect to MOS transistors, though other active devices may be used, such as, by way of example, bipolar transistors.

Thus the present invention has a number of aspects, which aspects may be practiced alone or in various combinations or sub-combinations, as desired. While certain preferred embodiments of the present invention have been disclosed and described herein for purposes of illustration and not for purposes of limitation, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the full breadth of the following claims.

What is claimed is:

1. In an amplifier system, a circuit comprising:
 - a first differential amplifier;
 - first and second choppers for chopping the input and the output of the first differential amplifier, respectively;
 - autozero circuitry coupled to the first differential amplifier for autozeroing the first differential amplifier;
 - the autozero circuitry operating at a first frequency and the choppers operating at a second frequency, the first frequency being twice the second frequency, the second frequency having a 50% duty cycle;
 - the first frequency having a duty cycle of less than 50%;
 - each half cycle of the choppers being interrupted while the first differential amplifier is auto-zeroed.
2. The circuit of claim 1 further comprising an amplifier having differential inputs coupled to the first and second differential inputs of the amplifier system and an output coupled to the output amplifier.
3. The circuit of claim 1 wherein the first frequency has a duty cycle of not more than 25%.
4. In an amplifier system, a circuit comprising:
 - a first differential amplifier;
 - first and second choppers for chopping the input and the output of the first differential amplifier, respectively;

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the first chopper being coupled to the first and second differential inputs of the amplifier system;

a first-switch having a first first-switch state coupling the differential inputs of the first differential amplifier to differential outputs of the first chopper, and a second first-switch state connecting the differential inputs of the first differential amplifier together;

a second differential amplifier, the second differential amplifier having differential inputs, each connected to a circuit ground through a respective capacitance;

differential outputs of the first and second differential amplifiers being coupled in common;

an output amplifier having an input coupled to an output of the second chopper;

a second-switch having a first second-switch state coupling the common outputs of the first and second differential amplifiers to an input of the second chopper, and a second second-switch state coupling the common outputs of the first and second differential amplifiers to the differential inputs of the second differential amplifier;

the first and second switches operating at a first frequency and the choppers operating at a second frequency unequal to the first frequency.

5. The circuit of claim 4 wherein the second frequency is twice the first frequency, and the first and second frequencies each have a 50% duty cycle.

6. The circuit of claim 4 wherein the first frequency is twice the second frequency, the second frequency having 50% duty cycle.

7. The circuit of claim 6 wherein the first frequency has a duty cycle of less than 50%, whereby each half cycle of the choppers is interrupted while the first differential amplifier is auto-zeroed.

8. The circuit of claim 6 wherein the first frequency has a duty cycle of not more than 25%, whereby each half cycle of the choppers is interrupted while the first differential amplifier is auto-zeroed.

9. The circuit of claim 6 further comprising:

third and fourth differential amplifiers, the fourth differential amplifier having differential inputs, each connected to a circuit ground through a respective capacitance, differential outputs of the third and fourth differential amplifiers being coupled in common;

the first-switch when in the first first-switch state also coupling the differential inputs of the third differential amplifier together and coupling the common outputs of the third and fourth differential amplifiers to the differential inputs to the fourth differential amplifier;

the first-switch when in the second first-switch state coupling the differential outputs of the first chopper to the differential inputs of the third differential amplifier and coupling the common differential outputs of the third and fourth differential amplifiers to the differential inputs of the second chopper.

10. The circuit of claim 9 further comprising an amplifier having differential inputs coupled to the first and second differential inputs of the amplifier system and an output coupled to the output amplifier.

11. The circuit of claim 6 wherein:

the first and second switches and the first and second choppers comprise third, fourth and fifth switches, each having an open and a closed state;

the first differential input of the amplifier system being connectable to a first differential input of the first differential amplifier by third and fifth switches, and to a second differential input of the first differential amplifier by the fourth and fifth switches;

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the second differential input of the amplifier system being connectable to the first differential input of the first differential amplifier by the fourth switch, and to the second differential input of the first differential amplifier by the third switch;

a first common connection of the outputs of the first and third differential amplifiers being connectable to a first differential input of the differential output amplifier through the third switch and to a second differential input to the differential output amplifier through the fourth switch;

a second common connection of the outputs of the first and second differential amplifiers being connectable to a first input of the differential output amplifier through the fourth switch and to a second input to the differential output amplifier through the third switch;

the common connection of the differential outputs of the first and second differential amplifiers being connectable to the differential inputs of the second differential amplifier by the fifth switch.

12. The amplifier of claim 11 wherein the output amplifier is a multiple stage amplifier.

13. The circuit of claim 11 further comprising a third amplifier having differential inputs coupled to the differential inputs of the amplifier system and an output coupled to the output amplifier.

14. The circuit of claim 11 wherein the third switches are all closed at the same time, but not when the fourth and fifth switches are closed, the fourth switches are all closed at the same time, but not when any of the third and fifth switches are closed, and the fifth switches are all closed at the same time, but not when any of the third or fourth switches are closed, whereby the switch operation is nonoverlapping, the fifth switches being closed at the first frequency with a duty cycle of less than 50%, the third switches being closed at a second frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the fifth switches, and the fourth switches being closed at the second frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the fifth switches.

15. The amplifier of claim 14 wherein the fifth switches are closed with a duty cycle of not more than 25%.

16. The amplifier of claim 14 wherein the output amplifier is a multiple stage amplifier.

17. The circuit of claim 14 further having third and fourth differential inputs of the amplifier system forming a second differential input port, and further comprising:

a third differential amplifier having first and second differential inputs;

the third differential input of the amplifier system being connectable to the first differential input of the third differential amplifier by third and fifth switches, and to the second differential input of the third differential amplifier by the fourth and fifth switches;

the fourth differential input of the amplifier system being connectable to the first differential input of the third differential amplifier by the fourth switch and to the second differential input of the third differential amplifier by the third switch;

differential outputs of the third differential amplifier being coupled in common with the differential outputs of the first and second differential amplifiers.

18. The circuit of claim 17 further comprising fourth and fifth differential amplifiers, the fourth differential amplifier having differential inputs coupled to the first and second differential inputs of the amplifier system and an output coupled to the output amplifier, and the fifth differential

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amplifier having differential inputs coupled to the third and fourth differential inputs of the amplifier system and an output coupled to the output amplifier.

19. The circuit of claim 14 further comprising:

a timing circuit for providing three output timing signals for controlling the timing of the third, fourth and fifth switches respectively, the output timing signals having first and second states and being nonoverlapping in the second state, the three output timing signals being provided from three input signals of first and second states, any of which input signals may overlap in the second state, comprising:

logic coupled to delay the change of a first output timing signal to the second state response to a change of the first input signal to the second state until after both second and third output signals are in the first state;

logic coupled to delay the change of a second output timing signal to the second state response to a change of the second input signal to the second state until after both first and third output signals are in the first state; and,

logic coupled to delay the change of a third output timing signal to the second state response to a change of the third input signal to the second state until after both first and second output signals are in the first state.

20. The circuit of claim 19 further comprising:

switch drive circuits for driving the third, fourth and fifth switches on the first and second differential inputs to the amplifier system to control their on and off states, respectively, each drive circuit being responsive to a respective output timing signal of the timing circuit, to control the on and off states of the third, fourth and fifth switches, respectively;

circuitry for connecting a first lead of a capacitor to a power supply voltage, a second capacitor lead to a circuit ground and holding the respective switch in the off state when the respective output timing signal is its first state; and,

circuitry for connecting the second lead of the capacitor to a voltage responsive to a common mode voltage of the first and second differential inputs of the amplifier system and connecting the first capacitor lead to a control voltage for the respective switch when the circuit is clocked by a respective output timing signal;

whereby the control voltage for turning on the switches is approximately one power supply voltage above the common mode voltage of the first and second differential inputs of the amplifier system, independent of what the common mode voltage is.

21. A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

operating the chopper stabilization at a first frequency; and,

operating the auto-zeroing at a second frequency;

the ratio of the frequencies being two to one;

the second frequency being twice the first frequency and having a duty cycle of less than one half.

22. A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

operating the chopper stabilization at a first frequency; and,

operating the auto-zeroing at a second frequency;

the ratio of the frequencies being two to one;

the second frequency having a duty cycle of not more than one-quarter.

23. A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

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operating the chopper stabilization at a first frequency; and, operating the auto-zeroing at a second frequency; the ratio of the frequencies being two to one; after each cycle of the chopper stabilization of the first amplifier, chopper stabilizing a second amplifier using the same choppers; auto-zeroing the second amplifier while the first amplifier is being chopper stabilized; and, auto-zeroing the first amplifier while the second amplifier is being chopper stabilized; the outputs of the first and second amplifiers being connected in common.

24. A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability wherein the chopper stabilized first amplifier has first, second and third pluralities of open and closed switches, the first and second switches being coupled as input and output chopper switches and the third switches being coupled as auto-zero switches, wherein the first switches are all closed at the same time, but not when the second and third switches are closed, the second switches are all closed at the same time, but not when any of the first and third switches are closed, and the third switches are all closed at the same time, but not when the first or second switches are closed, whereby the switch operation is nonoverlapping, the third switches being closed at a first frequency with a duty cycle of less than 50%, the first switches being closed at a second frequency equal to one half the first frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the third switches, and the second switches being closed at the second frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the third switches; operating the first and second switches at a first frequency; and, operating the third switches at a second frequency; the ratio of the frequencies being two to one.

25. The method of claim 24 wherein the third switches are closed with a duty cycle of not more 25%.

26. The method of claim 25 wherein the output amplifier is a multiple stage amplifier.

27. The method of claim 24 wherein the first amplifier has first and second differential inputs and further comprising:

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controlling, responsive to a clocking signal, the on and off states of switches controlling the connection of the first and second differential inputs to differential amplifier system inputs and to themselves, the differential amplifier system inputs having a common mode voltage, comprising, for each pair of switches: connecting a first lead of a capacitor to a power supply voltage, a second capacitor lead to a circuit ground and holding the switches in the off state when the switch control circuit is not being clocked by one of a first, second or third timing signal; and, connecting the second lead of the capacitor to a voltage responsive to the common mode voltage and connecting the first capacitor lead to a control voltage when the circuit is clocked by the respective first, second or third timing signal; whereby the control voltage for turning on the switches is approximately one power supply voltage above the common mode voltage, independent of what the common mode voltage is.

28. The method of claim 27 further comprising: providing the first, second and third timing signals, each having first and second states corresponding to switch on and off states, the three timing signals being nonoverlapping in the first state from three input signals of first and second states, any two of which may overlap in the first state by; delaying the change of the first timing signal to the first state response to a change of the first input signal to the first state until after both the second and the third timing signals are in the second state; delaying the change of the second timing signal to the first state response to a change of the second input signal to the first state until after both the first and the third output signals are in the second state; and, delaying the change of the third timing signal to the first state response to a change of the third input signal to the first state until after both the first and the second output signals are in the second state.

* * * * *



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BIB DATA SHEET

CONFIRMATION NO. 1854

SERIAL NUMBER 12/464,572	FILING or 371(c) DATE 05/12/2009 RULE	CLASS 330	GROUP ART UNIT 2817	ATTORNEY DOCKET NO. 55123P376		
APPLICANTS Rudy G. H. Eschauzier, Bergschenhoek, NETHERLANDS; Nico van Rijn, Katwijk, NETHERLANDS; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/20/2009						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /KHIEM D NGUYEN/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY NETHERLANDS	SHEETS DRAWINGS 17	TOTAL CLAIMS 36	INDEPENDENT CLAIMS 4
ADDRESS MAXIM/BSTZ Blakely Sokoloff Taylor & Zafman LLP 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085-4040 UNITED STATES						
TITLE Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers						
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Electronic Acknowledgement Receipt	
EFS ID:	5321399
Application Number:	12464572
International Application Number:	
Confirmation Number:	1854
Title of Invention:	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers
First Named Inventor/Applicant Name:	Rudy G.H. Eschauzier
Customer Number:	79124
Filer:	Roger W. Blakely/Jessica Clark
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Attorney Docket Number:	55123P376
Receipt Date:	12-MAY-2009
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Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	55123P376_20090512_ADS.pdf	836525	no	4
			50df97211322d016f363364d49be31617e8a3e23		
Warnings:					
Information:					
2		55123P376_20090512_App.pdf	130562	yes	55
			1188b4202ab6e1d956f12ba96b4562990cf810e2		
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	Document Description		Start	End	
	Specification		1	39	
	Claims		40	54	
	Abstract		55	55	
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3	Drawings-only black and white line drawings	55123P376_20090512_Figs.pdf	313307	no	16
			16487ddd22825d002912c77aae6a8851f9d7439e		
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4	Oath or Declaration filed	55123P376_20090512_Decl_POA.pdf	141183	no	4
			cfa7b971856a657398035403d5a77a8862ead0f1		
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5	Fee Worksheet (PTO-875)	fee-info.pdf	38114	no	2
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	55123P376
		Application Number	
Title of Invention	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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For further information see 37 CFR 1.33(a).

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	55123P376
		Application Number	
Title of Invention	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers		

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Customer Number	79124		
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Application Information:

Title of the Invention	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers		
Attorney Docket Number	55123P376	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	16	Suggested Figure for Publication (if any)	

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☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	55123P376
		Application Number	
Title of Invention	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers		

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This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
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Signature	/RWB/			Date (YYYY-MM-DD)	2009-05-12
First Name	Roger	Last Name	Blakely	Registration Number	25831

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Atty Docket No. 55123P376

UNITED STATES PATENT APPLICATION

FOR

**LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION
IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS**

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**LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION
IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS**

BACKGROUND OF THE INVENTION

1. Field of the Invention

5 The present invention relates to the field of
operational and instrumentation amplifiers.

2. Prior Art

One of the key performance specifications of an
operational amplifier is its DC error or offset voltage. The
10 offset voltage limits the ability of the amplifier to resolve
small DC input voltages. The total offset voltage is usually
specified assuming a single source of error at the input
terminals. The value of this imaginary voltage source
represents the input referred offset voltage of the
15 amplifier. The significance of this parameter lies in the
fact that the amplifier will not be able to resolve any DC
voltages at its input that are smaller than the input
referred offset voltage.

In monolithically integrated operational amplifiers, the
20 input referred offset voltage (also called input offset,
offset voltage or just offset for short) is mostly due to
statistical mismatch between critical components in the
circuit. Commonly, these critical components include the

input stage transistors, but other devices may contribute significantly to the offset as well. Typical offset voltages due to component mismatch lie in the order of several millivolts.

5 In the past, many techniques have been proposed and implemented to limit the effect of statistical mismatch on the input referred offset voltage. These techniques fall into one of two categories (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, 10 Correlated Double Sampling, and Chopper Stabilization", C.C. Enz and G.C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, Nov. 1996, pp. 1584-1614).

1. Chopper Stabilization
2. Autozeroing

15 The following will address each of these techniques, along with their respective advantages and disadvantages.

Chopper Stabilization

Chopper stabilization relies on periodically swapping the signal paths for the negative and positive input 20 terminals of the amplifier. On average, this causes the offset between the two terminals to even out (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper

Stabilization", C.C. Enz and G.C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, Nov. 1996, pp. 1584-1614). Figure 1 shows the block diagram of a chopper stabilized amplifier.

The input referred offset voltage of the input stage g_{m1} is represented by voltage source V_{os} . The behavior of the choppers is to multiply their input signal by +1 or -1, depending on the state of clock phase ϕ_2 . In the case of a differential signal (e.g. chopper $chop_1$), multiplying by -1 simply means swapping the input signals. Multiplying by +1 indicates direct connections between inputs and outputs.

Note how for one clock phase the input offset source V_{os} will cause a negative error voltage at the output, while for the other phase the effect will be a positive voltage. The net output error voltage, averaged over time, will be zero.

For the input signal the situation is different. In this case the signal passes to both choppers $chop_1$ and $chop_2$, and the polarity of the output signal will not change. Therefore, the output signal will consist of the unmodified input signal, and a ripple voltage caused by chopping by chopper $chop_2$ of the input offset voltage V_{os} .

Alternatively, in the frequency domain the choppers $chop_1$ and $chop_2$ can be regarded as multipliers or mixers, shifting the input frequencies by the chopper frequency f_{chop} . From

this point of view, chopper $chop_1$ will convert up a DC input signal to the chopper frequency f_{chop} . Input stage g_{m1} will then amplify the resulting signal at f_{chop} , while chopper $chop_2$ converts the signal back to DC. Note that the DC input
5 signal reappears as a DC signal at the output of chopper $chop_2$. This is because at this point the signal has passed through two choppers, implementing up and down conversion of the input signal.

The situation for the offset source V_{os} is different,
10 however. Since there is only one chopper between the offset source V_{os} and the output, the DC offset voltage V_{os} will get up converted to the chopper frequency f_{chop} at the output. By low pass filtering (or averaging) the output the effect of the offset source V_{os} can then be eliminated.

15 Besides to the DC offset, the same frequency up conversion applies to any $1/f$ or low frequency noise of input stage g_{m1} . Therefore, the $1/f$ noise is shifted out of the signal band in the same way the DC offset is.

The gain stages g_{m1} , g_{m4} and g_{m5} comprise the chopped
20 signal path. Since DC offset is - by definition - a low-frequency phenomenon, the chopped signal path does not require a very high bandwidth. Instead, the parallel input stage g_{m3} is added to the circuit to deal with high frequency signals. Together, input stages g_{m1} and g_{m3} handle the entire

spectrum from DC up to the bandwidth of the amplifier. Capacitors C_{m1} and C_{m2} implement frequency compensation to ensure stability when applying feedback to the amplifier, as well as a smooth transition between the high and low

5 frequency portions of the amplifier gain. This frequency compensation setup is based on Multipath Nested Miller Compensation (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.1, Boston, MA: Kluwer, 1995., section 6.1, Boston,

10 MA: Kluwer, 1995).

A significant benefit of the chopping technique, besides its effectiveness in reducing offset and $1/f$ noise, is that the noise power density spectrum (PSD) at low frequencies approaches the thermal noise limit of the amplifier without

15 choppers.

The main disadvantage of chopping is that the output spectrum of the chopper stabilized amplifier will show a sharp peak around the chopper frequency f_{chop} (Figure 2).

This noise peak is caused by the up conversion of the

20 offset voltage and $1/f$ noise of the input stage g_{m1} , and corresponds to the ripple voltage at the output of the amplifier in the time domain.

Autozeroing

Autozeroing includes techniques that calibrate out the input offset by measuring the offset, storing it into some kind of internal memory, and then compensating for the error during normal operation. This process is very similar to zeroing a weighing scale for example. The moment of calibration can be during manufacturing, in which case the measured offset needs to be stored onto a non-volatile memory, to ensure that the measured offset value does not disappear after the part is powered down. Alternatively, the autozeroing can be performed during normal operation, by periodically interrupting the signal path for a brief calibration. In this case, the measured voltage needs to be retained for a short amount of time only, allowing the use of volatile memory, or even a capacitor to store the value. The advantage of autozeroing during normal operation is that as the offset of the amplifier shifts, e.g. due to temperature changes or aging, the autozeroing will track the changes and continue to compensate for it. Autozeroing during manufacturing does not compensate for varying conditions, and is therefore susceptible to offset drift.

Figure 3 shows the simplified block diagram of an amplifier using autozeroing to reduce its offset.

It comprises of input stage g_{m1} with its associated input referred offset voltage source V_{os} . The switches S_1 and S_2 , transconductor g_{m2} and capacitor C_i implement the autozero function. When clock phase ϕ_1 is high (autozero), switch S_1
5 shorts the input terminals of input stage g_{m1} . Switch S_2 closes a feedback loop around stage g_{m2} , which forces the output voltage of input stage g_{m1} to zero. After the feedback loop settles, the voltage on autozero capacitor C_i counteracts the input referred offset voltage V_{os} .

10 The moment clock phase ϕ_1 goes low (normal operation), switch S_2 opens the feedback loop around transconductor g_{m2} . Because of the high input impedance of transconductor g_{m2} , the voltage across the autozero capacitor C_i remains constant (sample-and-hold), and continues to compensate for the offset
15 voltage V_{os} .

With clock phase ϕ_1 low, input switch S_1 goes from shorting out the input stage g_{m1} to directly connecting the input terminals of the amplifier to the input stage g_{m1} . Input stage g_{m1} now operates as a normal input stage,
20 connected between the input terminals of the amplifier and the subsequent gain stages g_{m4} and g_{m5} . As a result of the calibration in the previous clock phase, the small current I_2 that transconductor g_{m2} adds to the output current of input stage g_{m1} exactly compensates for the error current at the

output of g_{m1} due to offset voltage V_{os} . In other words, the autozero current I_2 effectively eliminates the input referred offset voltage V_{os} of the amplifier.

Besides eliminating DC offset, the autozero process is also very effective against low-frequency or $1/f$ noise. This noise component can be regarded as a slowly varying offset voltage, and as long as the amplifier is autozeroed with short enough intervals, any $1/f$ noise will be removed in the same fashion DC offset is.

The autozeroed amplifier in Figure 3 separates high and low frequency signals and processes them through two parallel signal paths, as was the case with the chopper stabilized amplifier of Figure 1. The gain stages g_{m1} , g_{m4} and g_{m5} comprise the low-frequency autozeroed signal path, while the parallel input stage g_{m3} deals with high frequency signals. Capacitors C_{m1} and C_{m2} again implement Multipath Nested Miller Compensation (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.1, Boston, MA: Kluwer, 1995., section 6.1, Boston, MA: Kluwer, 1995), ensuring stability and a smooth frequency response.

Although autozeroing according to Figure 3 is a simple and effective method to reduce the input offset, it greatly deteriorates the noise properties of the amplifier due to a

process called wide-band noise sampling (see "Circuit
Techniques for Reducing the Effects of Op-Amp Imperfections:
Autozeroing, Correlated Double Sampling, and Chopper
Stabilization", C.C. Enz and G.C. Temes, *IEEE J. Solid-State*
5 *Circuits*, vol. 84, Nov. 1996, pp. 1584-1614).

Wide-band noise sampling, which is inherent to any
sample-and-hold action, is caused by the fact that the
instantaneous noise value at the output of input stage g_{m1}
(and also autozero stage g_{m2}) is sampled by autozero capacitor
10 C_i and held for the entire period that ϕ_1 is low (normal
operation). The sampling of the noise takes place by switch
 S_2 and capacitor C_i , which are both components with a
bandwidth that far exceeds the bandwidth of the amplifier.
Therefore, the noise is sampled with a very high bandwidth,
15 which results in a corresponding high rms value (or standard
deviation σ) of the sampled noise voltage in the time domain.
As a result, the sampled voltage on autozero capacitor C_i at
the end of each autozero period shows a significant random
variation. This variation causes a random input referred
20 offset voltage that changes at the end of each autozero
interval, and is then kept constant throughout an entire
period of normal operation.

In the frequency domain, this wide-band noise sampling causes an increase in the noise floor for low frequencies (see Figure 4).

The corner frequency ω_c of this elevated noise band is
5 set by the bandwidth of the autozero loop through
transconductor g_{m2} , switch S_2 and autozero capacitor C_i and
equals g_{m2}/C_i .

In the circuit of Figure 3, there is also another,
second, source of wide-band noise sampling. This is due to
10 the sample-and-hold action of switch S_2 and the integrating
capacitor C_{m2} during the autozero period. As a result, the
noise floor beyond the corner frequency of the autozero loop
will also be higher compared to the thermal noise limit of
the amplifier without autozeroing. The bandwidth of this
15 sampled noise spectrum is approximately equal to the
frequency at which the amplifier is autozeroed (and lies
beyond the maximum frequency on the X-axis of Figure 4.)

The noise power spectral density (or PSD) of the overall
amplifier is shown in Figure 4. Due to the multiple sample-
20 and-hold actions in the circuit, the overall noise density is
significantly higher than the thermal noise limit of the
circuit without autozeroing. For low frequencies, the noise
increase is especially noticeable, and in practice can be a
factor 10 or more. Note that compensating for this elevated

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noise level by lowering the thermal noise of g_{m1} (and g_{m2}),
would mean that the currents in these stages will have to go
up by the same factor 10. In many cases such a large supply
current increase will turn out to be an unacceptable impact
5 to the total power budget of the amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of a Prior Art chopper stabilized amplifier.

Figure 2 illustrates the Noise Power Spectral Density (PSD) of a Prior Art chopper stabilized amplifier.

Figure 3 is a block diagram of a Prior Art autozeroed amplifier.

Figure 4 illustrates the Noise PSD of a Prior Art autozeroed amplifier.

Figure 5 is a block diagram of one circuit combining the advantages of chopping and autozeroing in a single amplifier.

Figure 6 illustrates the Noise PSD of the amplifier of Figure 5 with both chopping and autozeroing.

Figure 7 is a block diagram of an Amplifier combining chopping and autozeroing with a ping-pong autozeroed input stage.

Figure 8 illustrates the Noise PSD of the amplifier with ping-pong autozeroing.

Figure 9 is a block diagram of an Amplifier combining chopping and autozeroing with reduced wide-band noise sampling.

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Figure 10 illustrates the Noise PSD of the chopped and autozeroed amplifier with improved clocking scheme of Figure 9.

Figure 11 is a block diagram of a Simplified chopped and autozeroed amplifier.

Figure 12 is a block diagram of a Chopped and autozeroed amplifier using Multipath Hybrid Nested Miller Compensation.

Figure 13 is a block diagram of an Instrumentation amplifier with chopping and autozeroing.

Figure 14 illustrates the Clock phases of the chopped and autozeroed amplifier of Figure 13.

Figure 15 presents a Prior Art Circuit for generating two-phase non-overlapping clock signals.

Figure 16 illustrates the two-phase non-overlapping clock signals of the Prior Art circuit of Figure 15.

Figure 17 presents a circuit for a three-phase non-overlapping clock generator.

Figure 18 illustrates the three-phase non-overlapping clock signals for the circuit of Figure 17.

Figure 19 presents a Prior Art circuit for a Bootstrapped input switch circuit.

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Figure 20 presents a circuit for an improved bootstrapped switch with reduced switching glitch and die area.

Figure 21 illustrates an alternative form of autozero
5 circuit using a single differential amplifier.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the attached drawings, for reference, in instances where it matters, all switches are shown in states for a respective low control signal. In that regard, the word
5 switch is used herein and in the following claims in both the singular and the plural sense, and in the sense to include an on/off switch or switches, and switches that alternately connect one line to either of two other lines. However when used in the plural sense, each such switch is responsive to
10 the same control signal. Also the word amplifier as used herein means an amplifier of one or more stages, and may include frequency compensation.

Table 1 summarizes the properties of the chopping and autozeroing techniques for reducing the DC offset and $1/f$
15 noise of an amplifier.

	Advantage	Disadvantage
Chopping	Low-noise	Output ripple
Autozeroing	No output ripple	Wide-band noise sampling

Table 1. Properties of chopping and autozeroing.

Clearly, each of the techniques has its own set of advantages and disadvantages. Chopping results in low noise, but causes a significant output ripple, while autozeroing
20 suffers from wide-band noise sampling, and hence high noise, but does not generate a ripple at the output.

Ideally, we would like to find an alternative approach that combines the advantages of chopping and autozeroing, i.e. low noise and small output ripple. Figure 5 shows a first attempt at such a technique.

5 The circuit consists of autozeroed input stage g_{m1} that is "embedded" between the two choppers $chop_1$ and $chop_2$. The order of operation of the various parts is as follows. When clock phase ϕ_1 is high, input stage g_{m1} is being autozeroed by switch S_2 , transconductor g_{m2} and autozero capacitor C_i . When
 10 clock phase ϕ_1 goes low, input stage g_{m1} enters normal operation, while the output current of transconductor g_{m2} compensates for its input referred offset V_{os} . During this half cycle of normal operation, the two choppers $chop_1$ and $chop_2$ will go through a full clock cycle ϕ_2 , averaging out any
 15 remaining offset of autozeroed input stage g_{m1} . The cycle repeats by clock phase ϕ_1 going high again, entering the amplifier into autozero.

At first sight, the circuit of Figure 5 seems to have many advantages over only chopping or only autozeroing.
 20 Because the offset V_{os} of g_{m1} is already autozeroed, chopping by chopper $chop_2$ does not introduce any output ripple. Also, because the choppers shift any low-frequency noise of the autozeroed input stage g_{m1} to the chopper frequency f_{chop} , the effect of the wide-band noise sampling by autozero capacitor

C_i , is greatly eliminated. This can be seen in the noise it is shifted to the PSD of Figure 6.

Clearly, the low frequency noise resulting from the wide band noise sampling by autozero capacitor C_i , is shifted to the chopper frequency f_{chop} . Finally, since both the autozeroing and chopping contribute to reducing the offset, the resulting input referred offset can be much lower than by using chopping or autozeroing alone.

The noise PSD of Figure 6 also shows the main disadvantage of the combined autozeroed and chopped circuit of Figure 5. Notice how the overall noise floor is raised significantly above the thermal noise limit of the amplifier. This elevated noise floor is entirely due to the sample-and-hold action of switch S_2 and Miller capacitor C_{m2} . While the input stage is being autozeroed (clock phase ϕ_1 is high), the normal signal path is being interrupted. During this time, the voltage across Miller capacitor C_{m2} , holding the value at the time switch S_2 opened, will determine the output voltage of the amplifier. The sample-and-hold effect of switch S_2 and Miller capacitor C_{m2} again gives rise to wide-band noise sampling. It can raise the overall noise floor by a factor 10 or more, all the way up to the autozero frequency f_{az} (which is beyond the range on the x-axis of Figure 6).

A simple way to avoid the wide-band noise sampling in the circuit of Figure 5 is shown in Figure 7.

Here, the input stage of the amplifier is implemented using two independent transconductors g_{m1a} and g_{m1b} in a so-called *ping-pong* setup. The two input transconductors are alternately being autozeroed. While one transconductor is in its autozero mode, the other will provide a signal path between the input terminals and the intermediate stage g_{m4} , and vice versa. As a result, the normal signal path will never be interrupted, and no wide-band noise sampling takes place on the Miller capacitor C_{m2} . This is apparent from the noise PSD in Figure 8.

For low frequencies, the noise of the ping-pong circuit is identical to the thermal noise of the amplifier without chopping and autozeroing. The noise bump due to the autozeroing of g_{m1a} and g_{m1b} is shifted to the chopper frequency f_{chop} by the two choppers $chop_1$ and $chop_2$, as was the case in the circuit of Figure 5.

Although the noise PSD of Figure 8 approaches the ideal of low-noise and low output voltage ripple, this performance comes at a considerable price in terms of die area and power consumption. Because of the ping-pong structure, the input stage almost doubles in size and supply current. Since both area and supply current of the input stage are key in

obtaining a low thermal noise floor, the die size and power penalty of doubling the input stage will be unacceptable in many practical cases.

An alternative approach to combining the advantages of chopping and autozeroing, without the die size and power penalty of a ping-pong autozeroed input stage, is shown in Figure 9.

This circuit is similar to the circuit of Figure 5, but employs a modified clocking scheme. Instead of the autozero clock phase ϕ_1 running at half the chopping frequency f_{chop} , it now operates at twice the chopping frequency f_{chop} . Also, the duty cycle is such, that the autozero time is substantially shorter than the time the input stage provides a normal signal path. Thus the duty cycle of ϕ_1 is preferably less than 50%, and is more preferably not more than 25%. The result is that each half cycle of the choppers is interrupted by the auto-zeroing, though for less than one half of each half cycle of the chopping. This is also preferred for the embodiments of Figures 11, 12 and 13.

By placing the autozero pulse in the middle of each half cycle of the chopper clock phase ϕ_2 , chopper c_{hop2} will average out any residual offset after autozeroing in the time between two autozero pulses. This residual offset averaging stems

from the fact that during a period between two autozero pulses, the signal is passed through chopper $chop_2$ directly and with reversed polarity with the same duration.

The modified clocking scheme substantially reduces the wide-band noise sampling by switch S_2 and Miller capacitor C_{m2} . Even though the hold voltage on Miller capacitor C_{m2} after opening S_2 still has the same large random variation as was the case in the circuit of Figure 5, limiting the time this random voltage affects the signal path, greatly reduces its overall effect. This is shown in Figure 10.

By choosing a suitably small autozero duty cycle, the overall noise increase due to the wide-band noise sampling can become arbitrarily small. In practice, by choosing a duty cycle less than 10% the noise floor of the circuit will be within several percent of the theoretical thermal noise floor limit.

Figure 11 shows a simplification of the circuit in Figure 9.

Notice how in the previous circuit of Figure 9 the autozero switches and internal chopper switches are connected in series, each with their own clocking phases. The circuit of Figure 11 combines these series connections of switches

into one switch where possible, and provides the proper clocking phases to drive them.

Operation is as follows. The first state of the circuit is when clock phase ϕ_3 is high; the circuit is in autozero mode, with the switches labeled ϕ_3 closed. As a result, the inputs of transconductor g_{m1} are both tied to the positive input terminal. Hence, the input differential voltage of g_{m1} is zero, while the voltage at the positive input sets the common-mode voltage. The output terminals of input transconductor g_{m1} are connected to the autozero capacitors C_{i1} and C_{i2} , closing the autozero loop.

The second state occurs after clock phase ϕ_3 goes low again. Now there are two possible situations: either clock phase ϕ_1 goes high, while phase ϕ_2 remains low, or vice versa. Assuming the first case, ϕ_1 high and ϕ_2 low, input stage g_{m1} is connected directly between the input terminals and the intermediate stage g_{m4} . Offset voltage source V_{cs} will cause a positive error voltage at the output of the amplifier. The two autozero capacitors C_{i1} and C_{i2} are disconnected from the signal path and hold their voltage to cancel out any offset of input stage g_{m1} .

The circuit enters its third and final state when ϕ_1 and ϕ_2 reverse polarities (ϕ_1 low and ϕ_2 high). In this situation,

input stage g_{m1} is effectively turned upside down, swapping both the input and output terminals. The polarity of the signal path remains the same, but the effect of input offset voltage V_{os} at the output changes sign: it will cause a
5 negative excursion of the output voltage.

Since states two and three have the same duration, the average effect of the offset source V_{os} will be zero. State 1 is effectively operating at twice the frequency of states 2 and 3, though states 2 and 3 are each interrupted by state 1,
10 with each half cycle of the chopping being temporarily interrupted by the auto-zeroing process.

The order of states two and three after each autozero pulse ϕ_3 alternates. This results in the following overall order of the circuit states: 2-1-2, 3-1-3, 2-1-2 etc. The
15 average (residual) offset across one autozero cycle, whether it is the 2-1-2 or the 3-1-3 cycle, will be zero.

Input stage g_{m3} again implements a separate signal path for high frequencies. Together with capacitors C_{m1} , C_{m2a} and C_{m2b} , this parallel input stage g_{m3} implements Multipath Nested
20 Miller Compensation (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.1, Boston, MA: Kluwer, 1995). This frequency compensation technique ensures stability when applying feedback to the overall amplifier, while enabling a

smooth frequency response without artifacts in the cross-over region between the high and low frequency signal paths.

Capacitor C_3 is an optional component that can help the gain of the low-frequency signal path (g_{m1} , g_{m4} and g_{m5}) to drop off steeply enough at high frequencies not to interfere with the high-frequency signal path through parallel input stage g_{m3} .

A final refinement of the circuit in Figure 11 is shown in Figure 12.

This circuit is identical to the circuit of Figure 11, except for the additional gain stage g_{m6} . The purpose of this additional stage is to increase the gain of the low-frequency signal path through input stage g_{m1} . This additional gain will help to suppress any DC offset of the overall amplifier due to mismatches in the parallel input stage g_{m3} . A DC offset in the parallel input stage g_{m3} will cause an input referred offset voltage of the overall amplifier. The resulting input referred offset can be very small, however, as its effect is reduced by the ratio of the gains of the low frequency signal path and high frequency signal path. By introducing the additional gain stage g_{m6} , the circuit of Figure 12 will offer gain ratios on the order of 10,000x or more in typical situations. Therefore, a DC offset of the parallel input stage g_{m3} of 10mV for example, will be reduced to less than a microvolt. At these low levels, the effect of

a DC mismatch in the parallel input stage g_{m3} is sufficiently small not to significantly affect the overall performance of the amplifier.

Because of the additional gain stage g_{m6} , the circuit of Figure 12 now requires Multipath Hybrid Nested Miller compensation to guarantee stability with overall feedback applied (see "Frequency Compensation Techniques for Low-Power Operational Amplifiers", R. Eschauzier and J. Huijsing, section 6.3, Boston, MA: Kluwer, 1995). This frequency compensation technique is similar to Multipath Nested Miller Compensation used in Figure 11, except that it uses an active integrator with Miller capacitors C_{m3a} and C_{m3b} , as opposed to the passive filter capacitor C_3 in Figure 11.

Instrumentation Amplifiers

By adding an additional input stage to any of the circuits in Figure 5, Figure 7, Figure 9, Figure 11 and Figure 12, these can easily be transformed into so-called instrumentation amplifiers (see "Operational Amplifiers, Theory and Design", J. Huijsing, pp. 52-53, Boston, Kluwer Academic Publishers, 2001). Instrumentation amplifiers have two sets of differential input terminals and are capable of sensing small differential signals in the presence of a large common-mode disturbance.

In order for the chopping and autozeroing to work properly in the modified circuit, only the input stage devices (including the parallel devices for Multipath frequency compensation) and input switches need to be repeated from the original opamp. The autozeroing can be done across both input stages combined, and therefore does not require additional autozero capacitors, nor autozero feedback switches.

Figure 13 shows the chopped and autozeroed instrumentation amplifier that results from modifying the opamp depicted in Figure 12. The components added to the circuit are the two input stages g_{m1b} and g_{m3b} , along with the corresponding input switches.

Figures 5, 7 and 9 implement one form of autozero circuit, also effectively incorporated in Figures 11, 12 and 13, though it should be understood that other forms of autozero circuits may be used. By way of example, Figure 21 illustrates an alternative form of autozero circuit using a single differential amplifier rather than the two of the previous embodiment. In Figure 21, a differential transistor pair M1 and M2 each have a drain current I_1 and a common source connection having a tail current of $2I_1$. Either the drain currents or the tail current can be controlled by a common mode voltage controlled current source to achieve the

desired common mode input to the gates of the transistors M1 and M2. Note that this common mode voltage is unrelated to, and can be fixed and very different from, the common mode input to the amplifier system, the difference being the
5 voltages across capacitors Caz1 and Caz2.

Clock phases ϕ_1 and ϕ_2 are the chopper clock phases. During autozeroing, clock phases ϕ_1 and ϕ_2 are low and the clock phase ϕ_3 is high. Note that if the two drain currents I_1 are not perfectly matched, that mismatch, itself, will also
10 cause an offset in the differential pair of transistors M1 and M2. However that offset is also autozeroed by the foregoing process so that a perfect match of the two drain current sources I_1 is not required.

In any autozero circuit, the input to the input stage is
15 periodically disconnected and then shorted, with the offset then being stored on one or more capacitors for subtraction from the signal path between autozeroing operations. In the embodiments of Figures 5, 7, 9 and 11-13, a second amplifier is used, with the net input offset of both amplifiers gm_1 and
20 gm_2 being stored on the capacitors on the input to the second amplifier. The offsets are cancelled by the second amplifier having a current output opposite the current output of the differential input stage when the input of the differential input stage is shorted. In the embodiment of Figure 21, only

one differential amplifier is used for the autozero operation, with the autozeroing being done by appropriately charging capacitors in series with the differential amplifier input.

5 Clock Generation

The clock phase ϕ_3 can be thought of as the autozero phase, while the clock phase ϕ_1 and ϕ_2 can be (broadly) thought of as the two chopper phases. One complication that arises in the circuits of Figure 11 and Figure 12 is that
10 only one of the sets of switches corresponding to a particular clock phase (ϕ_1 , ϕ_2 or ϕ_3) is allowed to be closed at any particular time. Closing two or more sets of switches will cause short circuits between the various nodes of the circuit. In order to guarantee this break-before-make
15 behavior, the switches need to be driven by *non-overlapping* clock phases.

A prior art circuit for generating two-phase non-overlapping clock signals is shown in Figure 15 (see "Principles of CMOS Design", N.H.E. Weste and K. Eshraghian,
20 section 5.5.10, Addison-Wesley, 1993).

It generates the two non-overlapping clock phases ϕ_1' and ϕ_2' from the potentially overlapping input clock phases ϕ_1 and ϕ_2 . This process is illustrated in Figure 16.

Operation of the circuit is as follows (assuming for simplicity that all gates are delay free, except for the inverters I3 and I4). With clock phase ϕ_1 low and clock phase ϕ_2 high, the output clock phases ϕ_1' and ϕ_2' will also be low and high respectively. When the two input clock phases ϕ_1 and ϕ_2 change states (ϕ_1 transitioning to high and ϕ_2 to low), output ϕ_2' will change almost instantaneously (see Figure 16). This direct output response occurs because when the input ϕ_2 to nand gate N1 goes low, its output will go high, regardless of the state of the other input to the nand gate. During the same transition (ϕ_1 to high and ϕ_2 to low), output ϕ_1' will respond with a delay. One input of the nand gate N2 is held low by inverter I3. With one input low, the output of nand gate N2 will not change its output, independently of the state of the other input that is connected to input clock phase ϕ_1 . Only when the output of I3 changes, will the output of nand N2 change, and hence output ϕ_1' . Note that inverters I3 and I4 are assumed to exhibit noticeable delay, whereas all other gates are delay-free. The resulting output clock phases ϕ_1' and ϕ_2' are shown in Figure 16. As indicated before, output ϕ_2' responds directly to the falling edge of ϕ_2 , while clock phase ϕ_1' , tracks the rising edge of input ϕ_1 with a slight delay. Note how the resulting output phases ϕ_1' and ϕ_2' are never on at the same time (break before make).

The next change of input state, input clock phase ϕ_1 will go low again, and input clock phase ϕ_2 high. The process reverses, and in this case the output ϕ_1' responds directly to the falling edge of ϕ_2 , while clock phase ϕ_1' tracks the rising edge of input ϕ_1 with a slight delay. This timing again avoids overlap of the two output clock signals ϕ_1' and ϕ_2' . Note in Figure 16 how the output clock phases always respond directly to a falling edge of the corresponding input clock phase, whereas rising edges are tracked with a slight delay. This timing property is fundamental to producing the two non-overlapping clock signals ϕ_1' and ϕ_2' .

Figure 17 extends the operation of the non-overlapping clock generator of Figure 15 to the three specific clock phases of Figure 14. In the preferred embodiment, the three timing signals input to the circuit of Figure 17 are generated by a simple state machine, and may be overlapping.

In this case, the circuit needs to make sure that none of the three output clock phases ϕ_1' , ϕ_2' and ϕ_3' will ever be high at the same time. Operation is similar to that of the circuit in Figure 15 and illustrated in Figure 18.

For simplicity, all components are assumed to be delay-free again, except for the inverters I4, I5 and I6.

When the input clock phase ϕ_3 is low, the output of inverter I4 is high, and the circuit part consisting of the nand gates N2 and N3, and inverters I2, I3, I5 and I6 behave identically to the prior art circuit in Figure 15. These six
5 components create non-overlapping clock phases ϕ_1' and ϕ_2' from the two input clock phases ϕ_1 and ϕ_2 . Since clock phase ϕ_3 was low to begin with, the result is that only one output clock phase ϕ_1' , ϕ_2' or ϕ_3' will be high at a given time.

When input clock phase ϕ_3 transitions high, the output
10 clock phase ϕ_3' will wait for both other inputs to the nand gate N1 to become high as well, before it follows input clock phase ϕ_3 in going high. The other two inputs of the nand gate N1 will go high -albeit with some delay- because both input clock phase ϕ_1 and ϕ_2 will be low once input clock phase ϕ_3 has
15 gone high. The delay is caused by one of the two inverters I5 and I6, depending on the state of the input clock phase ϕ_1 and ϕ_2 . If input clock phase ϕ_1 was low before the input clock transition, it will remain low, while input clock phase ϕ_2 goes from high to low. In this case the delay is caused by
20 inverter I5. Inverter I6 becomes responsible for the delay in the situation where input clock phase ϕ_2 starts off and remains low, while input clock phase ϕ_1 makes the high-to-low

transition. The delay before the output clock phase ϕ_3' goes high, results in the non-overlap time for this clock phase.

A high-to-low transition of input clock phase ϕ_3 affects output clock phase ϕ_3' almost immediately, as it causes one
5 input to the nand gate N1 (the one connected to input ϕ_3) to go low. One low input to the nand gate is sufficient to make the output clock phase ϕ_3' go low as well, regardless of the other inputs to the nand gate N1.

Since the circuit of Figure 17 is symmetrical around all
10 of its input-output pairs ϕ_1/ϕ_1' , ϕ_2/ϕ_2' and ϕ_3/ϕ_3' , the same reasoning that applies to the pair ϕ_3/ϕ_3' holds equally for the other two pairs.

The overall result of the timing in the circuit of Figure 17, is that the clock phase outputs ϕ_1' , ϕ_2' and ϕ_3' will
15 follow any high-to-low transition of their respective input clock phases ϕ_1 , ϕ_2 and ϕ_3 directly, while a low-to-high transition is propagated with a certain delay. Figure 18 clearly shows how this delayed response to the rising edges creates the required three phase non-overlapping clock
20 signals. Of course the circuit of Figure 17 may in effect be realized using logical permutations accordingly to Boolean geometry to achieve the delay of each signal going to a first

state until the both the other signals are in the second state.

Rail-to-Rail Input Switches

When operating any of the circuits Figure 5, Figure 7,
5 Figure 9, Figure 11 or Figure 12 at a low supply voltage while requiring a rail-to-rail input common-mode voltage range, the need arises for bootstrapped input switches. This need is especially felt when the supply voltage of the amplifier is lower than the sum of the threshold voltages of
10 an NMOS and a PMOS device in the manufacturing process technology. Under these circumstances, we are not able to operate traditional complementary transmission gates at the inputs.

A transmission gate consists of the parallel connection
15 of a PMOS and NMOS switch, each of which is operated by an opposite phase signal at its gate. To turn the transmission gate on, the gate of the NMOS device is pulled high, while the gate of the PMOS device is pulled low. At supply voltages below the sum of the threshold voltages of the NMOS
20 and PMOS device, an area in the middle of the common-mode voltage range of the switch will occur where neither of the two devices can develop enough voltage across its gate-source terminals to be turned on.

The alternative to a transmission gate is to use a single NMOS or PMOS device, with a gate drive voltage that can rise above (NMOS) or drop below (PMOS) the supply voltage of the circuit. Figure 19 shows an example of a prior art

5 bootstrapped NMOS switch that uses a capacitor to increase the control voltage at the gate of the switching device (see "Very low-voltage digital-audio $\Sigma\Delta$ modulator with 88-dB dynamic range using local switch bootstrapping", M. Dessouky and A. Kaiser, IEEE J. Solid-State Circuits, vol. 36, no. 3,

10 pp. 349-355, Mar. 2001).

Operation of the bootstrapped switch is as follows. While the input terminal *clk* is held low (switch turned off), device M_{N7} pulls down node G (gates of the switching transistor) through cascode device M_{N6} . Switch devices M_R and

15 M_S are in their off states, while capacitor C_1 is being charged to the supply voltage by devices M_{P5} and M_{N1} . Devices M_{P0} and M_{P1} are off. Stepping the control voltage *clk* high (turning the switch on), device M_{N0} pulls down node E, and device M_{P1} will start to conduct current. Device M_{P1} on its

20 turn will connect the pre-charged capacitor C_1 between the gate and source of device M_R , which will also turn on. With devices M_{P1} and M_R in their on states, the gate-source voltage of the switching device M_S equals the voltage V_{dd} stored on the capacitor C_1 . With its gate-source voltage V_{gs} above the

25 threshold voltage, the switch devices M_S will turn on.

Even though the voltages at node G and node B can rise significantly above the supply voltage (maximally twice V_{dd}), safe operation of all devices is guaranteed.

There are two apparent drawbacks of the prior art circuit in Figure 19. The first is that the circuit requires a capacitor for each input switch. Since the disclosed circuits will be operating a total of six input switches, the six capacitors will represent a considerable die area penalty. Secondly, operating the switch will cause a major switching glitch in the signal path. This glitch is especially apparent while turning the switch on. In that case, device M_R is closed, while node A is still at the ground potential V_{ss} . With device M_R closed, node A needs to be lifted all the way up to the common-mode voltage level at the input terminal V_{in} . The charge needed for this voltage jump is pulled from the input terminal V_{in} , leading to the switching glitch.

The circuit of Figure 20 alleviates the die size penalty and switching glitches associated with the prior art circuit of Figure 19.

The circuit of Figure 20 uses only one gate-drive capacitor C_1 to drive the two input switch devices M_{S1} and M_{S2} . Since all six input switches in Figure 11 and Figure 12 come in three pairs that are driven by the same clock phase, this

reduces the total number of capacitors from six to three. This is not needed between stages, as the common mode voltage may be controlled (limited) so a rail to rail switching voltage may be used for these switches.

5 The key modification to allow driving multiple switch devices with one bootstrap circuit is the use of voltage v_{cm} as a reference to lift gate-control capacitor C_1 , instead of the source of the switch device M_S in the prior art circuit of Figure 19. Disconnecting the sources of the switches $MS1$ and
10 $MS2$ from the bootstrap circuit has the added benefit of avoiding the switching glitch that arose in the prior art circuit of Figure 19.

 The key to successfully operating the switch devices M_{S1} and M_{S2} in Figure 20 lies in generating the proper common-mode
15 voltage v_{cm} . This voltage v_{cm} is derived through source follower M_{N8} from the voltage at the sources of the input transistors M_{P6} and M_{P7} of the overall amplifier circuit, M_{P6} and M_{P7} being the differential transistor pair in a differential input stage for the amplifier system. Because
20 of this connection, the common mode voltage v_{cm} has two important properties:

1. The voltage v_{cm} will track the *minimum* of the two voltages at the gates of input transistors M_{P6} and M_{P7} . This is due to the fact that the input device with the lowest gate

voltage, e.g. M_{P6} , will start acting as a source follower, tracking the voltage at its gate with the source, while the other device (M_{P7} in this example) will be turned off by lack of a sufficiently high gate-source voltage V_{gs} . In a typical
 5 amplifier application, the differential input will be minimal, so that the voltage v_{cm} will accurately reflect the common mode voltage of the differential input. Note also, that only one source follower M_{N8} need be used for all switches coupled to that differential input.

10 2. Because of source follower M_{N8} , the common mode voltage v_{cm} can never exceed the positive rail V_{dd} , even if the tail current source of the input pair M_{P6} and M_{P7} is connected to a voltage higher than the supply voltage V_{dd} . A common situation where the input stage tail current source is tied
 15 to a higher supply voltage than the remainder of the amplifier is in amplifiers that employ a charge-pump to obtain a rail-to-rail input common-mode range. The charge pump generates a boosted supply voltage for the input stage, extending its common mode input voltage range.

20 Because of these two points, the circuit continues to guarantee safe operation of all devices in the circuit. The gate of the switching devices M_{S1} and M_{S2} will never be pulled higher than one supply voltage V_{dd} above the minimum of the two input voltages V_{inp} and V_{inm} . Consequently, the gate-source

voltages V_{gs} of switching devices M_{S1} and M_{S2} cannot exceed the supply voltage V_{dd} . Also, node E, which is connected to v_{cm} when switch devices M_{N0} and M_R are closed, cannot exceed the supply voltage V_{dd} . This is critical to avoid forward biasing
 5 of the backgate diode of M_{P0} .

Operation of the circuit is similar to that of the prior art circuit in Figure 19: when input terminal clk is low (switch turned off), device M_{N7} pulls down node G (gates of the switching transistors) through cascode M_{N6} . Switch
 10 devices M_{S1} and M_{S2} are in their off states, while capacitor C_1 is being charged to the supply voltage by devices M_{P5} and M_{N1} . Devices M_{P0} and M_{P1} are off. When the control voltage clk goes high (turning the switch on), device M_{N0} pulls down node E, and device M_{P1} will start to conduct current. Device M_{P1} in
 15 turn will connect the pre-charged capacitor C_1 between the gate and source of device M_R , which will also turn on. With devices M_{P1} and M_R in their on states, the voltage at node G will be the common-mode voltage v_{cm} plus the voltage V_{dd} stored on the capacitor. The result is that the gate-source
 20 voltages V_{gs} of the switch devices M_{S1} and M_{S2} will rise above their threshold voltages and turn the two devices on.

The embodiments shown and described herein use differential amplifiers. It should be noted that a single ended amplifier is functionally a differential amplifier with

one input and/or one output connected to a circuit ground.

Similarly, a chopper alternately reverses two inputs,
independent of whether one is a circuit ground or not.

Accordingly references herein and in the following claims to

5 differential amplifiers is a reference that includes
amplifiers with one input and/or one output connected to a
circuit ground, i.e., commonly referred to as single ended
amplifiers. Also the embodiments shown and described herein
are shown and described with respect to MOS transistors,
10 though other active devices may be used, such as, by way of
example, bipolar transistors.

Thus the present invention has a number of aspects,
which aspects may be practiced alone or in various
combinations or sub-combinations, as desired. While certain
15 preferred embodiments of the present invention have been
disclosed and described herein for purposes of illustration
and not for purposes of limitation, it will be understood by
those skilled in the art that various changes in form and
detail may be made therein without departing from the spirit
20 and scope of the invention as defined by the full breadth of
the following claims.

CLAIMS

What is claimed is:

1 1. In an amplifier system, a circuit comprising:
2 a first differential amplifier;
3 first and second choppers for chopping the input and the
4 output of the first differential amplifier, respectively;
5 autozero circuitry coupled to the first differential
6 amplifier for autozeroing the first differential amplifier;
7 the autozero circuitry operating at a first frequency
8 and the choppers operating at a second frequency unequal to
9 the first frequency.

1 2. The circuit of claim 1 wherein the second frequency
2 is twice the first frequency, and the first and second
3 frequencies each have a 50% duty cycle.

1 3. The circuit of claim 1 further comprising an
2 amplifier having differential inputs coupled to the first and
3 second differential inputs of the amplifier system and an
4 output coupled to the output amplifier.

1 4. The circuit of claim 1 wherein the first frequency
2 is twice the second frequency, the second frequency having a
3 50% duty cycle.

1 5. The circuit of claim 4 wherein the first frequency
2 has a duty cycle of less than 50%, whereby each half cycle of
3 the choppers is interrupted while the first differential
4 amplifier is auto-zeroed.

1 6. The circuit of claim 4 wherein the first frequency
2 has a duty cycle of not more than 25%, whereby each half
3 cycle of the choppers is interrupted while the first
4 differential amplifier is auto-zeroed.

1 7. The circuit of claim 1 wherein the first chopper is
2 coupled to the first and second differential inputs of the
3 amplifier system, and further comprising:

4 a first-switch having a first first-switch state
5 coupling the differential inputs of the first differential
6 amplifier to differential outputs of the first chopper, and a
7 second first-switch state connecting the differential inputs
8 of the first differential amplifier together;

9 a second differential amplifier, the second differential
10 amplifier having differential inputs, each connected to a
11 circuit ground through a respective capacitance;

12 differential outputs of the first and second
13 differential amplifiers being coupled in common;

14 an output amplifier having an input coupled to an output
15 of the second chopper;

16 a second-switch having a first second-switch state
17 coupling the common outputs of the first and second
18 differential amplifiers to an input of the second chopper,
19 and a second second-switch state coupling the common outputs
20 of the first and second differential amplifiers to the
21 differential inputs of the second differential amplifier.

1 8. The circuit of claim 7 wherein the second frequency
2 is twice the first frequency, and the first and second
3 frequencies each have a 50% duty cycle.

1 9. The circuit of claim 7 wherein the first frequency
2 is twice the second frequency, the second frequency having a
3 50% duty cycle.

1 10. The circuit of claim 9 wherein the first frequency
2 has a duty cycle of less than 50%, whereby each half cycle of
3 the choppers is interrupted while the first differential
4 amplifier is auto-zeroed.

1 11. The circuit of claim 9 wherein the first frequency
2 has a duty cycle of not more than 25%, whereby each half
3 cycle of the choppers is interrupted while the first
4 differential amplifier is auto-zeroed.

1 12. The circuit of claim 9 further comprising:

2 third and fourth differential amplifiers, the fourth
3 differential amplifier having differential inputs, each
4 connected to a circuit ground through a respective
5 capacitance, differential outputs of the third and fourth
6 differential amplifiers being coupled in common;

7 the first-switch when in the first first-switch state
8 also coupling the differential inputs of the third
9 differential amplifier together and coupling the common
10 outputs of the third and fourth differential amplifiers to
11 the differential inputs to the fourth differential amplifier;

12 the first-switch when in the second first-switch state
13 coupling the differential outputs of the first chopper to the
14 differential inputs of the third differential amplifier and
15 coupling the common differential outputs of the third and
16 fourth differential amplifiers to the differential inputs of
17 the second chopper.

1 13. The circuit of claim 12 further comprising an
2 amplifier having differential inputs coupled to the first and
3 second differential inputs of the amplifier system and an
4 output coupled to the output amplifier.

1 14. The circuit of claim 9 wherein:

2 the first and second switches and the first and second
3 choppers comprise third, fourth and fifth switches, each
4 having an open and a closed state;

5 the first differential input of the amplifier system
6 being connectable to a first differential input of the first
7 differential amplifier by third and fifth switches, and to a
8 second differential input of the first differential amplifier
9 by the fourth and fifth switches;

10 the second differential input of the amplifier system
11 being connectable to the first differential input of the
12 first differential amplifier by the fourth switch, and to the
13 second differential input of the first differential amplifier
14 by the third switch;

15 a first common connection of the outputs of the first
16 and third differential amplifiers being connectable to a
17 first differential input of the differential output amplifier
18 through the third switch and to a second differential input
19 to the differential output amplifier through the fourth
20 switch;

21 a second common connection of the outputs of the first
22 and second differential amplifiers being connectable to a
23 first input of the differential output amplifier through the

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24 fourth switch and to a second input to the differential
25 output amplifier through the third switch;

26 the common connection of the differential outputs of the
27 first and second differential amplifiers being connectable to
28 the differential inputs of the second differential amplifier
29 by the fifth switch.

1 15. The amplifier of claim 14 wherein the output
2 amplifier is a multiple stage amplifier.

1 16. The circuit of claim 14 further comprising a third
2 amplifier having differential inputs coupled to the
3 differential inputs of the amplifier system and an output
4 coupled to the output amplifier.

1 17. The circuit of claim 14 wherein the third switches
2 are all closed at the same time, but not when the fourth and
3 fifth switches are closed, the fourth switches are all closed
4 at the same time, but not when any of the third and fifth
5 switches are closed, and the fifth switches are all closed at
6 the same time, but not when any of the third or fourth
7 switches are closed, whereby the switch operation is
8 nonoverlapping, the fifth switches being closed at the first
9 frequency with a duty cycle of less than 50%, the third
10 switches being closed at a second frequency with a duty cycle
11 of approximately 50%, except as interrupted for the closure

12 of the fifth switches, and the fourth switches being closed
13 at the second frequency with a duty cycle of approximately
14 50%, except as interrupted for the closure of the fifth
15 switches.

1 18. The amplifier of claim 17 wherein the fifth
2 switches are closed with a duty cycle of not more 25%.

1 19. The amplifier of claim 17 wherein the output
2 amplifier is a multiple stage amplifier.

1 20. The circuit of claim 17 further having third and
2 fourth differential inputs of the amplifier system forming a
3 second differential input port, and further comprising:
4 a third differential amplifier having first and second
5 differential inputs;
6 the third differential input of the amplifier system
7 being connectable to the first differential input of the
8 third differential amplifier by third and fifth switches, and
9 to the second differential input of the third differential
10 amplifier by the fourth and fifth switches;
11 the fourth differential input of the amplifier system
12 being connectable to the first differential input of the
13 third differential amplifier by the fourth switch and to the
14 second differential input of the third differential amplifier
15 by the third switch;

16 differential outputs of the third differential amplifier
17 being coupled in common with the differential outputs of the
18 first and second differential amplifiers.

1 21. The circuit of claim 20 further comprising fourth
2 and fifth differential amplifiers, the fourth differential
3 amplifier having differential inputs coupled to the first and
4 second differential inputs of the amplifier system and an
5 output coupled to the output amplifier, and the fifth
6 differential amplifier having differential inputs coupled to
7 the third and fourth differential inputs of the amplifier
8 system and an output coupled to the output amplifier.

1 22. The circuit of claim 17 further comprising:
2 a timing circuit for providing three output timing
3 signals for controlling the timing of the third, fourth and
4 fifth switches respectively, the output timing signals having
5 first and second states and being nonoverlapping in the
6 second state, the three output timing signals being provided
7 from three input signals of first and second states, any of
8 which input signals may overlap in the second state,
9 comprising:
10 logic coupled to delay the change of a first output
11 timing signal to the second state response to a change of the
12 first input signal to the second state until after both
13 second and third output signals are in the first state;

14 logic coupled to delay the change of a second output
15 timing signal to the second state response to a change of the
16 second input signal to the second state until after both
17 first and third output signals are in the first state; and,
18 logic coupled to delay the change of a third output
19 timing signal to the second state response to a change of the
20 third input signal to the second state until after both first
21 and second output signals are in the first state.

1 23. The circuit of claim 22 further comprising:
2 switch drive circuits for driving the third, fourth and
3 fifth switches on the first and second differential inputs to
4 the amplifier system to control their on and off states,
5 respectively, each drive circuit being responsive to a
6 respective output timing signal of the timing circuit, to
7 control the on and off states of the third, fourth and fifth
8 switches, respectively;
9 circuitry for connecting a first lead of a capacitor to
10 a power supply voltage, a second capacitor lead to a circuit
11 ground and holding the respective switch in the off state
12 when the respective output timing signal is its first state;
13 and,
14 circuitry for connecting the second lead of the
15 capacitor to a voltage responsive to a common mode voltage of
16 the first and second differential inputs of the amplifier

17 system and connecting the first capacitor lead to a control
18 voltage for the respective switch when the circuit is clocked
19 by a respective output timing signal;

20 whereby the control voltage for turning on the switches
21 is approximately one power supply voltage above the common
22 mode voltage of the first and second differential inputs of
23 the amplifier system, independent of what the common mode
24 voltage is.

1 24. A method of operating a chopper stabilized first
2 amplifier, the chopper stabilized first amplifier having an
3 auto-zeroing capability comprising:

4 operating the chopper stabilization at a first
5 frequency; and,

6 operating the auto-zeroing at a second frequency;

7 the ratio of the frequencies being two to one.

1 25. The method of claim 24 wherein the first frequency
2 is twice the second frequency, and each having a duty cycle
3 of 50%.

1 26. The method of claim 24 wherein the second frequency
2 is twice the first frequency and has duty cycle of less than
3 one half.

1 27. The method of claim 26 wherein the second frequency
2 has a duty cycle of not more than one-quarter.

1 28. The method of claim 24 further comprising:
2 after each cycle of the chopper stabilization of the
3 first amplifier, chopper stabilizing a second amplifier using
4 the same choppers;
5 auto-zeroing the second amplifier while the first
6 amplifier is being chopper stabilized; and,
7 auto-zeroing the first amplifier while the second
8 amplifier is being chopper stabilized;
9 the outputs of the first and second amplifiers being
10 connected in common.

1 29. The method of claim 24 wherein the chopper
2 stabilized first amplifier has first, second and third
3 pluralities of open and closed switches, the first and second
4 switches being coupled as input and output chopper switches
5 and the third switches being coupled as auto-zero switches,
6 wherein the first switches are all closed at the same time,
7 but not when the second and third switches are closed, the
8 second switches are all closed at the same time, but not when
9 any of the first and third switches are closed, and the third
10 switches are all closed at the same time, but not when the
11 first or second switches are closed, whereby the switch

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12 operation is nonoverlapping, the third switches being closed
13 at a first frequency with a duty cycle of less than 50%, the
14 first switches being closed at a second frequency equal to
15 one half the first frequency with a duty cycle of
16 approximately 50%, except as interrupted for the closure of
17 the third switches, and the second switches being closed at
18 the second frequency with a duty cycle of approximately 50%,
19 except as interrupted for the closure of the third switches.

1 30. The method of claim 29 wherein the third switches
2 are closed with a duty cycle of not more 25%.

1 31. The method of claim 30 wherein the output amplifier
2 is a multiple stage amplifier.

1 32. The method of claim 29 wherein the first amplifier
2 has first and second differential inputs and further
3 comprising:

4 controlling, responsive to a clocking signal, the on and
5 off states of switches controlling the connection of the
6 first and second differential inputs to differential
7 amplifier system inputs and to themselves, the differential
8 amplifier system inputs having a common mode voltage,
9 comprising, for each pair of switches:

10 connecting a first lead of a capacitor to a power supply
11 voltage, a second capacitor lead to a circuit ground and

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12 holding the switches in the off state when the switch control
13 circuit is not being clocked by one of a first, second or
14 third timing signal; and,

15 connecting the second lead of the capacitor to a voltage
16 responsive to the common mode voltage and connecting the
17 first capacitor lead to a control voltage when the circuit is
18 clocked by the respective first, second or third timing
19 signal;

20 whereby the control voltage for turning on the switches
21 is approximately one power supply voltage above the common
22 mode voltage, independent of what the common mode voltage is.

1 33. The method of claim 32 further comprising:

2 providing the first, second and third timing signals,
3 each having first and second states corresponding to switch
4 on and off states, the three timing signals being
5 nonoverlapping in the first state from three input signals of
6 first and second states, any two of which may overlap in the
7 first state by;

8 delaying the change of the first timing signal to the
9 first state response to a change of the first input signal to
10 the first state until after both the second and the third
11 timing signals are in the second state;

12 delaying the change of the second timing signal to the
13 first state response to a change of the second input signal

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14 to the first state until after both the first and the third
15 output signals are in the second state; and,
16 delaying the change of the third timing signal to the
17 first state response to a change of the third input signal to
18 the first state until after both the first and the second
19 output signals are in the second state.

1 34. A circuit for providing three output timing signals
2 having first and second states and being nonoverlapping in
3 the first state from three input signals of first and second
4 states, any two of which may overlap in the first state,
5 comprising:

6 logic coupled to delay the change of a first output
7 timing signal to the first state response to a change of the
8 first input signal to the first state until after both second
9 and third output signals are in the second state;

10 logic coupled to delay the change of a second output
11 timing signal to the first state response to a change of the
12 second input signal to the first state until after both first
13 and third output signals are in the second state; and,

14 logic coupled to delay the change of a third output
15 timing signal to the first state response to a change of the
16 third input signal to the first state until after both first
17 and second output signals are in the second state.

1 35. A switch control circuit for controlling,
2 responsive to a clocking signal, the on and off states of
3 switches controlling the connection of first and second
4 differential input signals, the first and second differential
5 input signals having a common mode voltage, comprising:

6 circuitry for connecting a first lead of a capacitor to
7 a power supply voltage, a second capacitor lead to a circuit
8 ground and holding the switches in the off state when the
9 switch control circuit is not being clocked; and,

10 circuitry for connecting the second lead of the
11 capacitor to a voltage responsive to the common mode voltage
12 and connecting the first capacitor lead to a switch control
13 voltage when the circuit is clocked;

14 whereby the switch control voltage for turning on the
15 switches is approximately one power supply voltage above the
16 common mode voltage, independent of what the common mode
17 voltage is.

1 36. The switch control circuit of claim 35 wherein the
2 first and second differential input signals are coupled to an
3 input pair of transistors having a common connection to a
4 current source, and wherein the common mode voltage is
5 provided by a third transistor coupled to the common
6 connection.

ABSTRACT

Low-noise, low-power, low drift offset correction in operational and instrumentation amplifiers and amplifiers using the same are disclosed. The amplifiers disclosed use different combinations of chopping and auto-zero techniques. Also disclosed are amplifiers using on-off switches to affect the chopping and auto-zeroing, with unique circuits for driving the switches on the differential input to provide boot-strapped switch controls. Other features are disclosed.

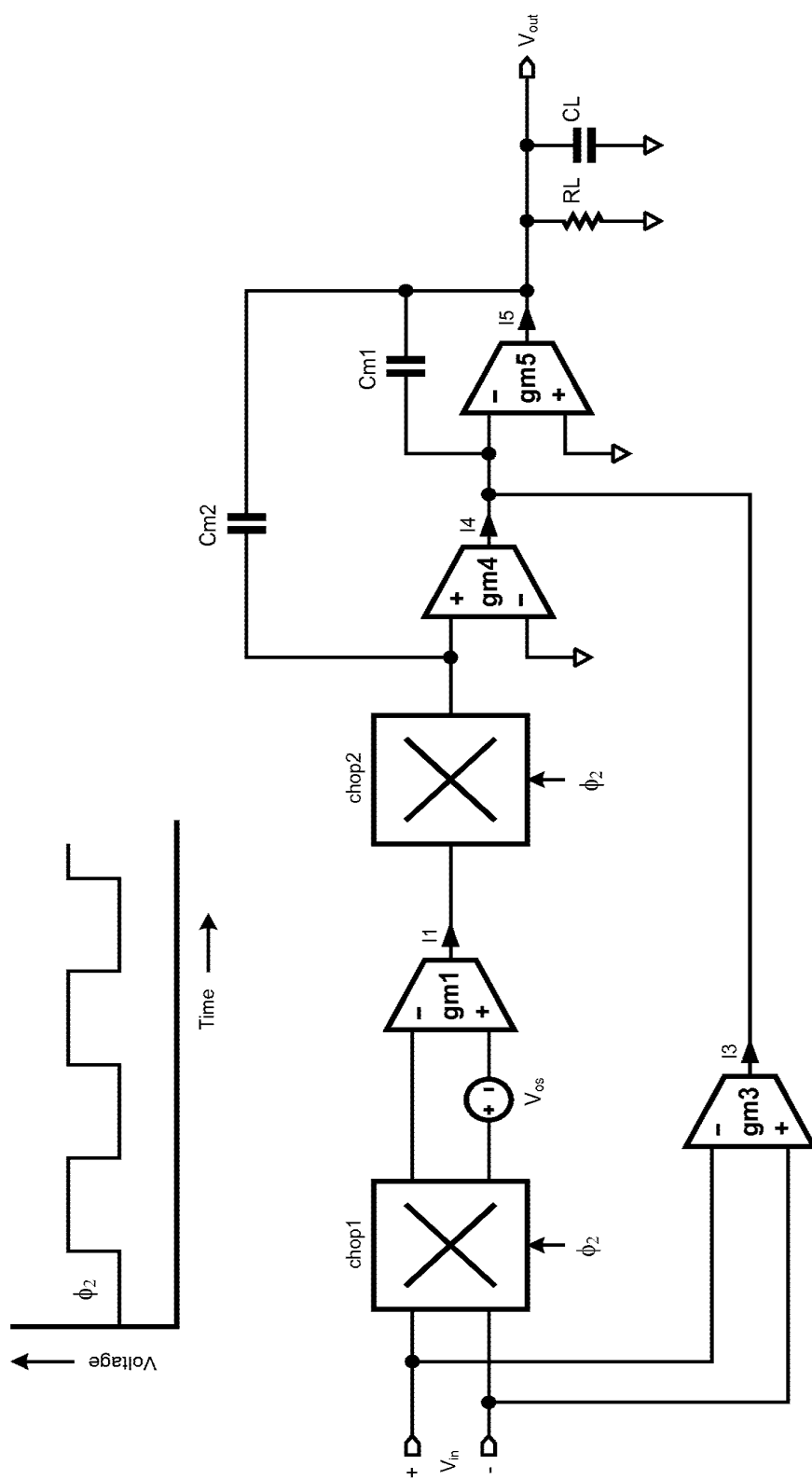


Fig. 1 (Prior Art)

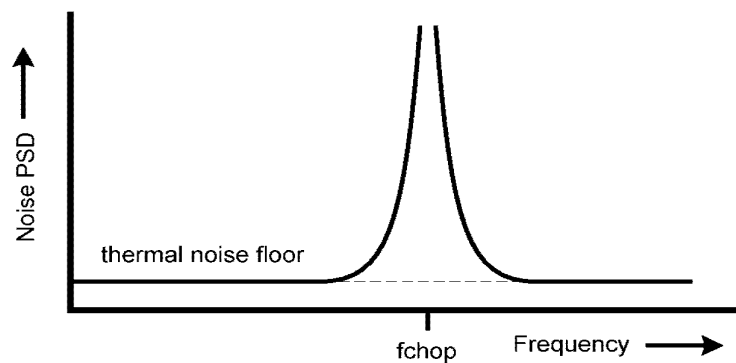


Fig. 2 (Prior Art)

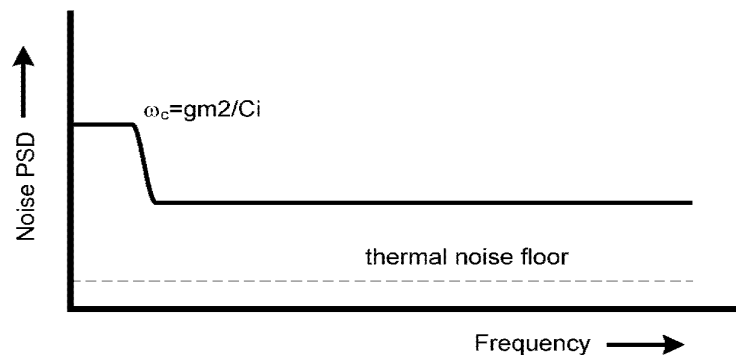


Fig. 4 (Prior Art)

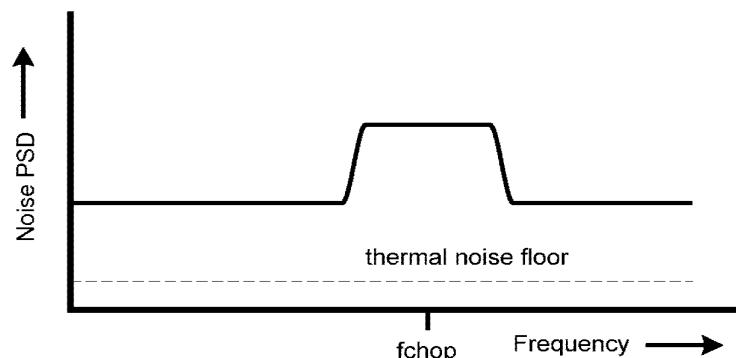


Fig. 6

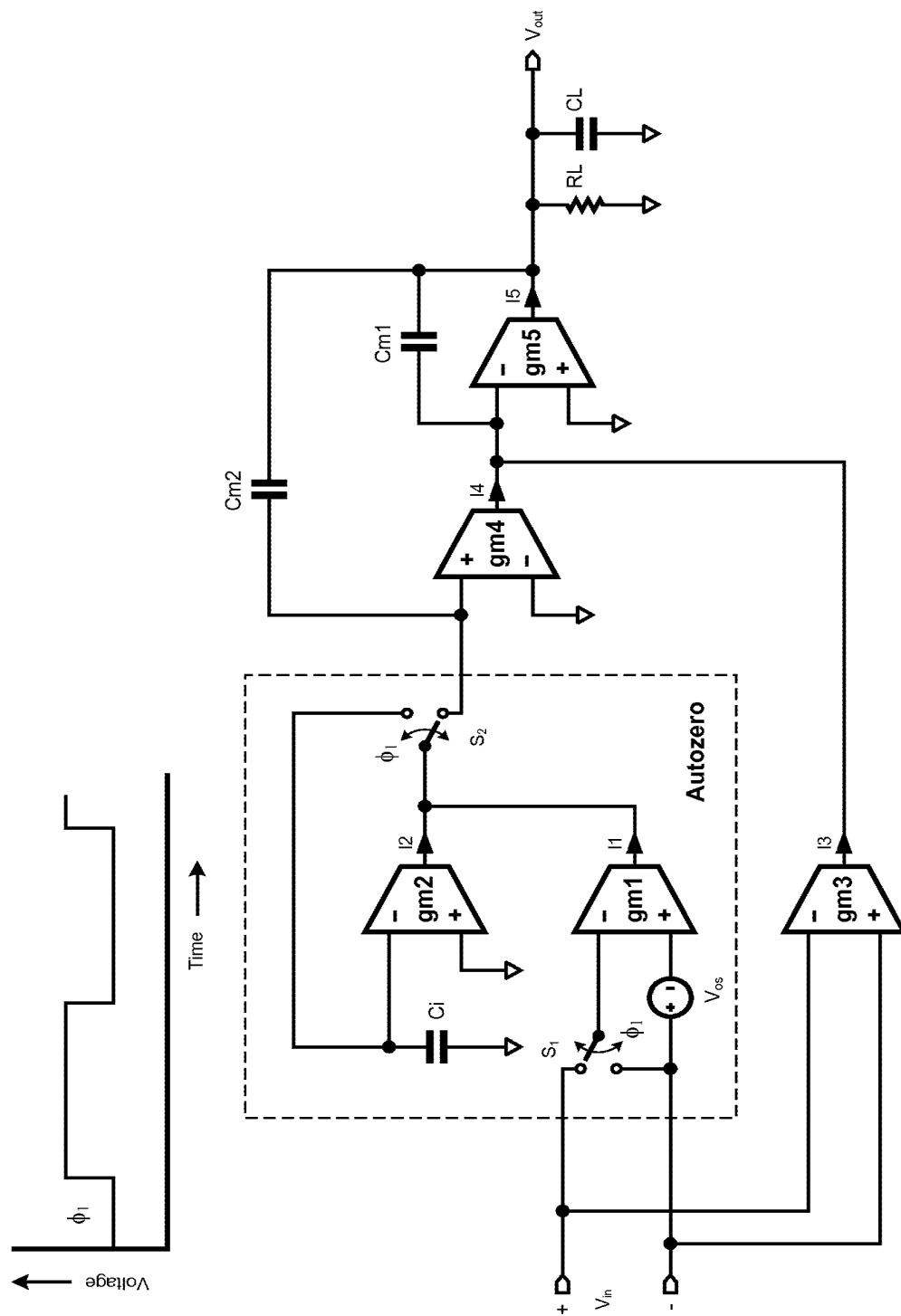


Fig. 3 (Prior Art)

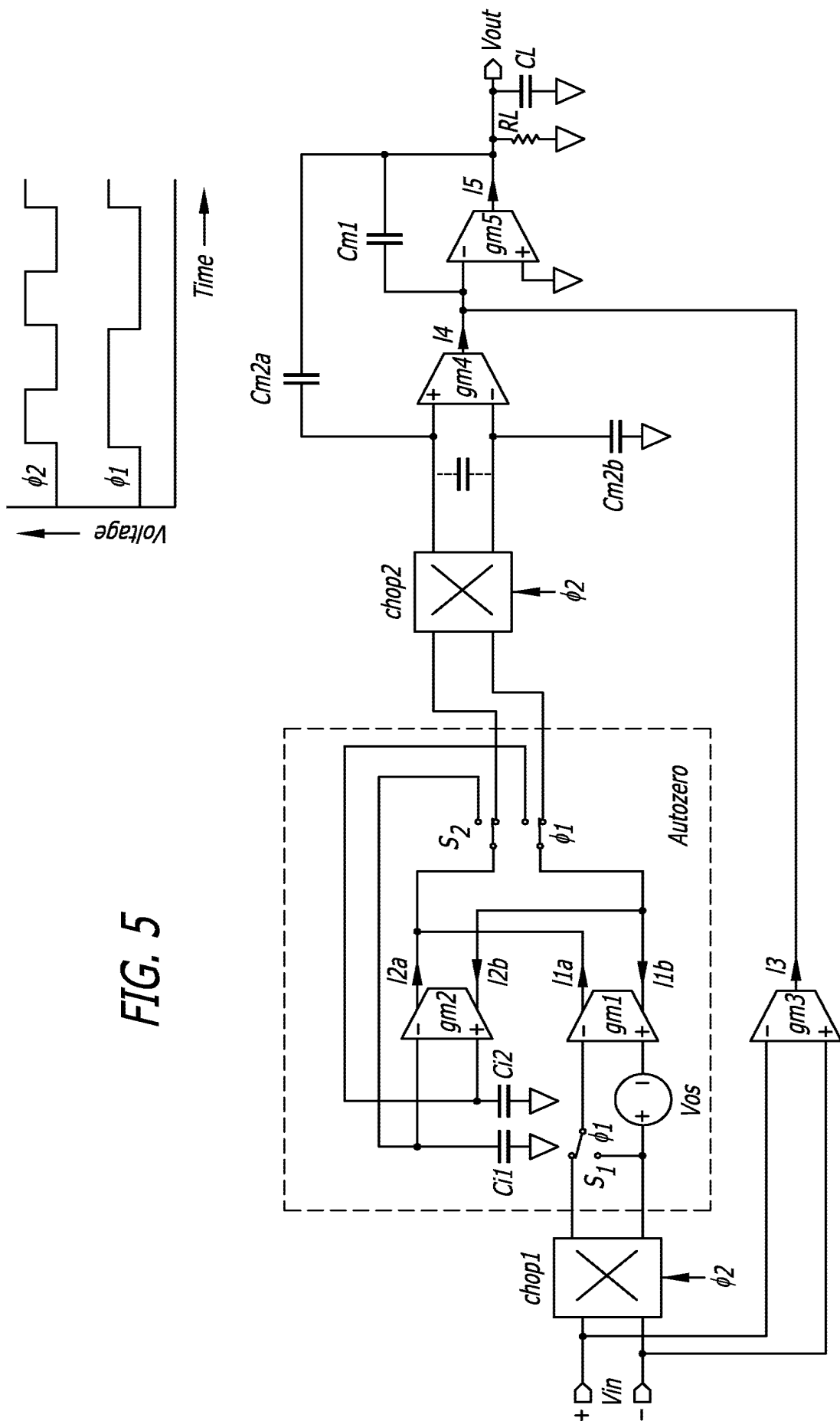


FIG. 5

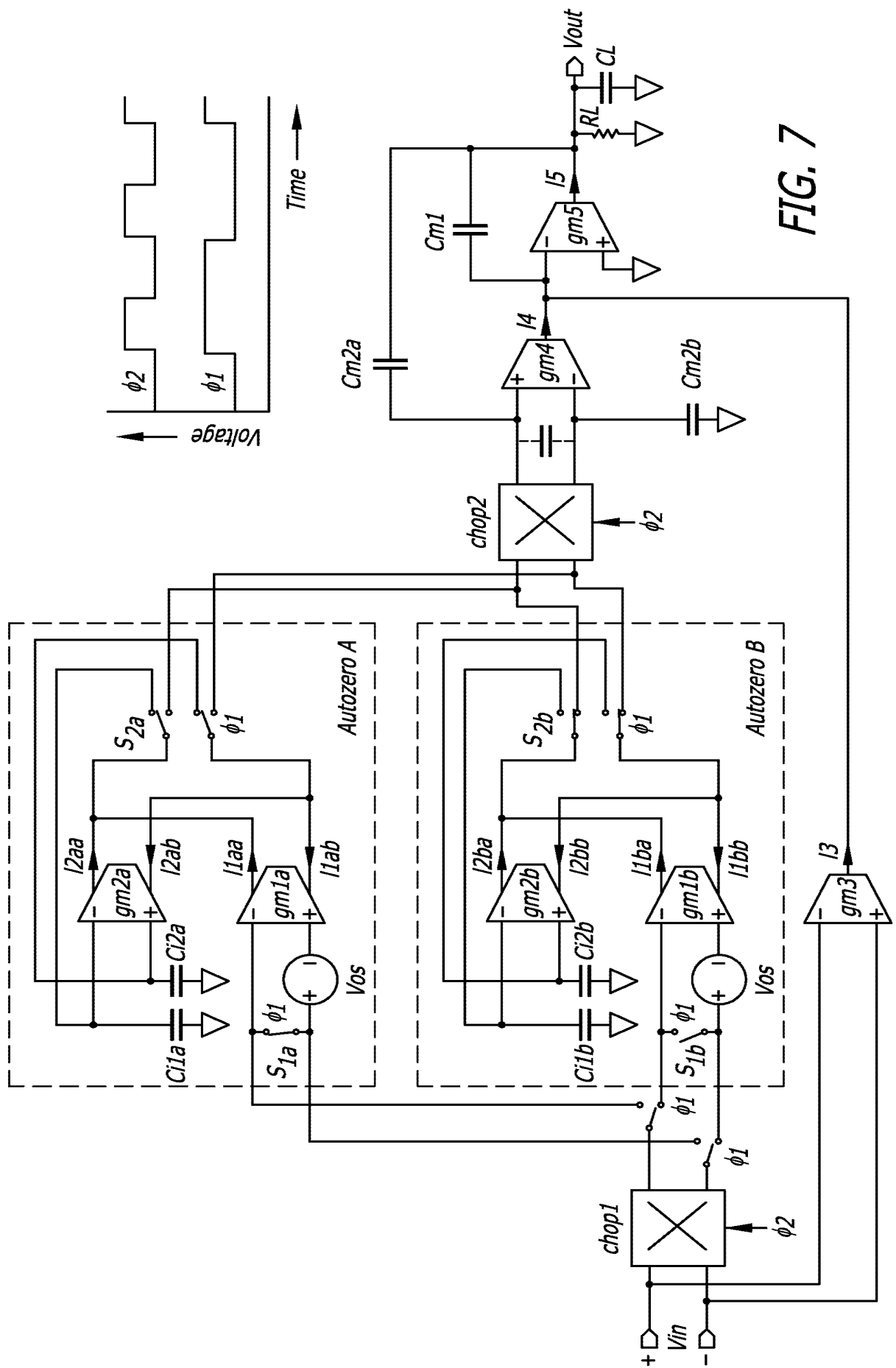


FIG. 7

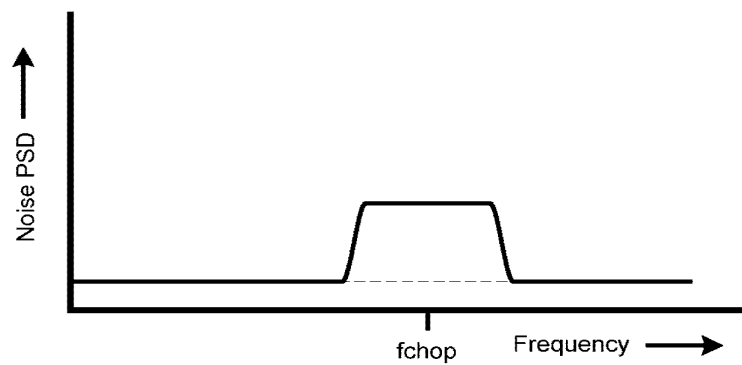


Fig. 8

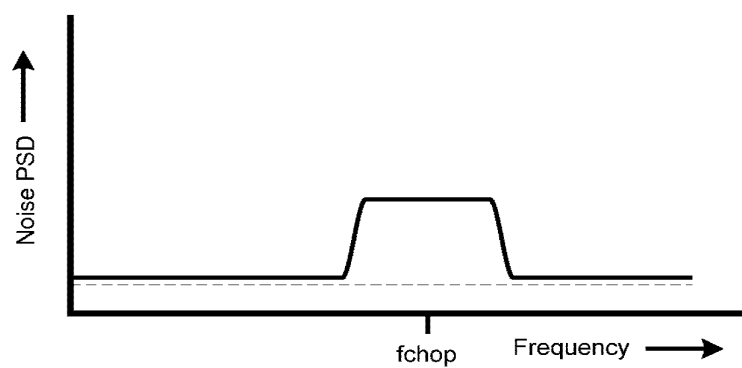


Fig. 10

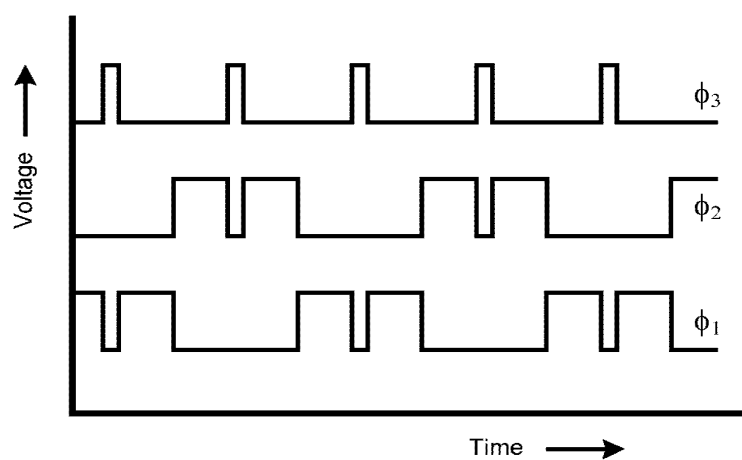


Fig. 14

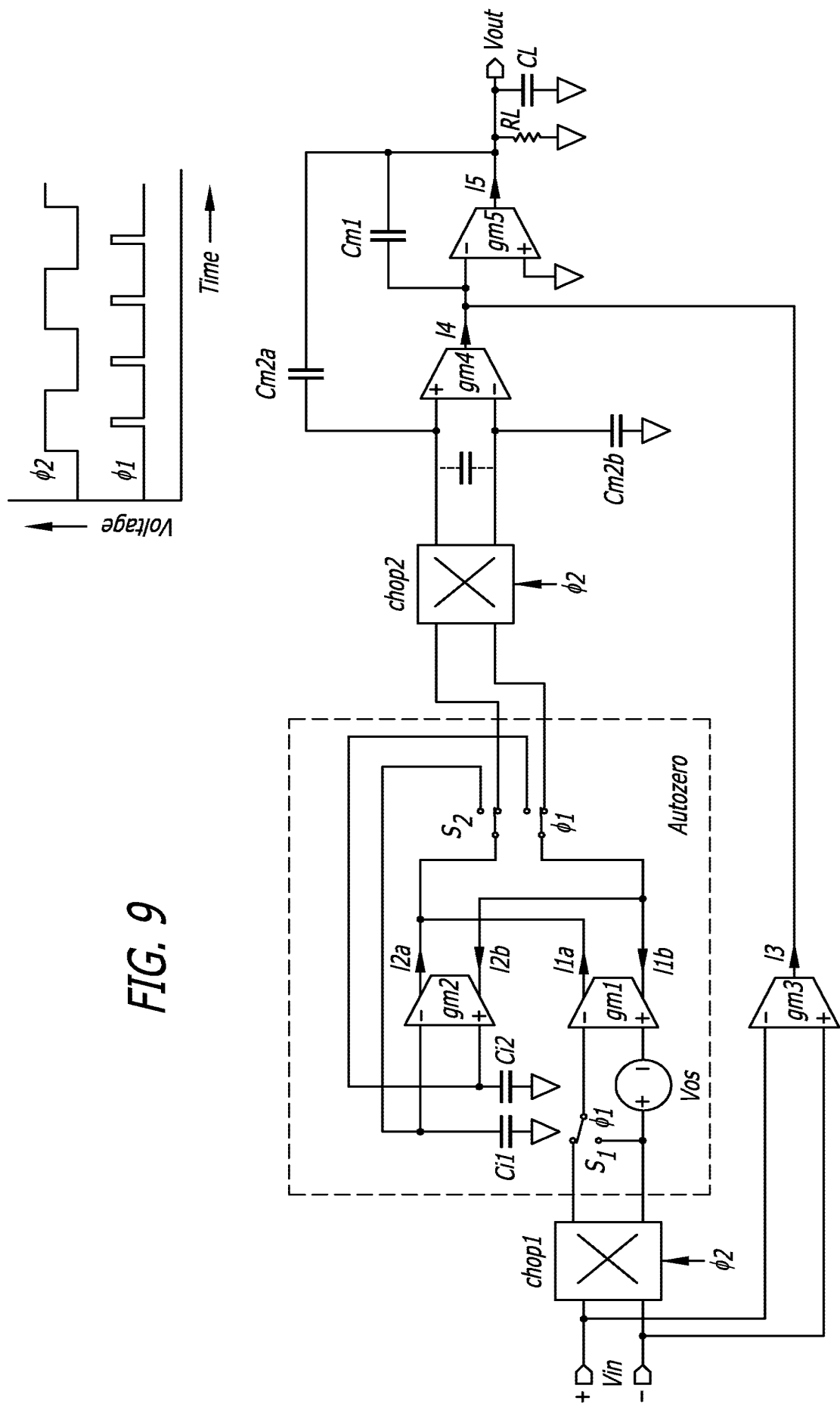


FIG. 9

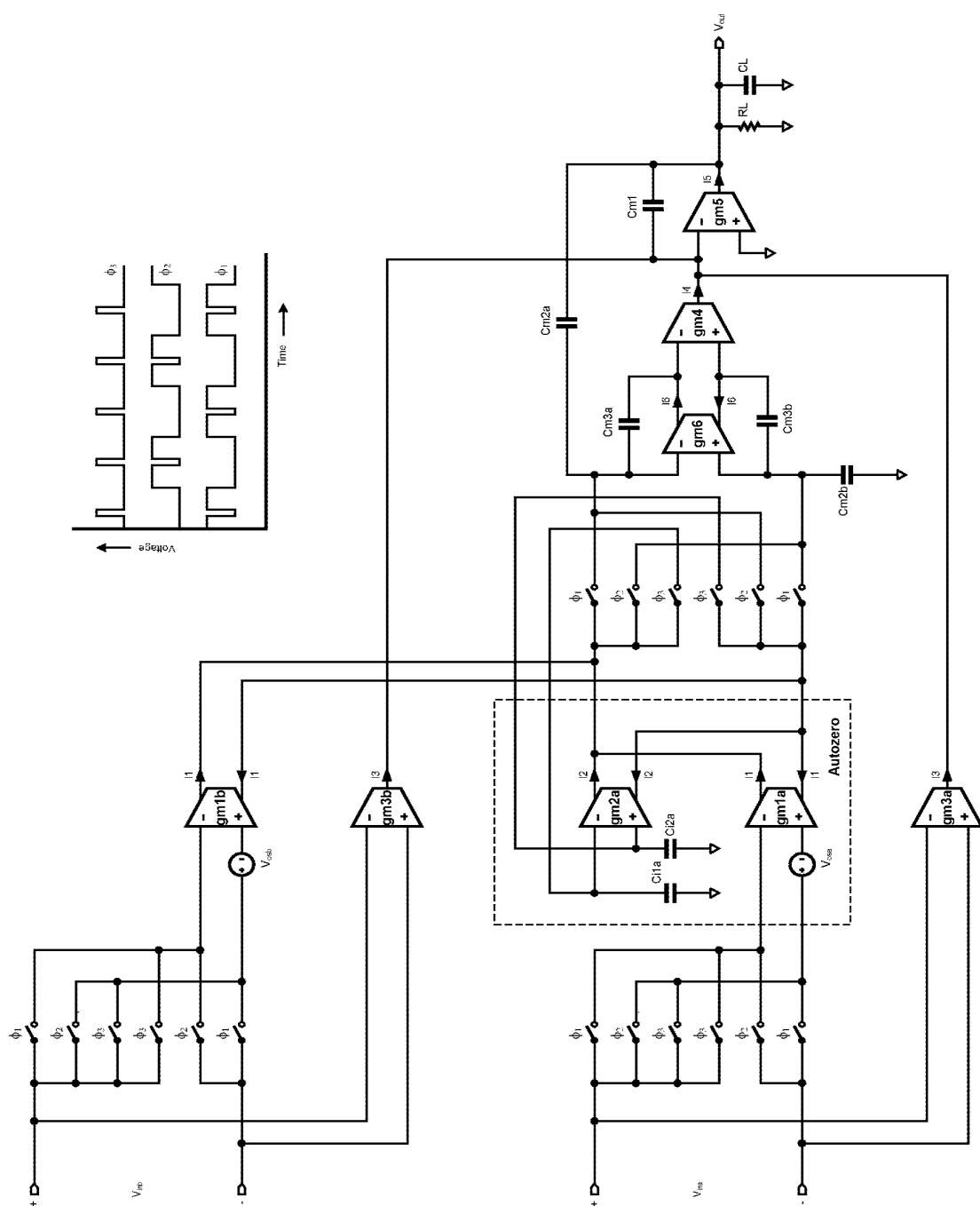


Fig. 13

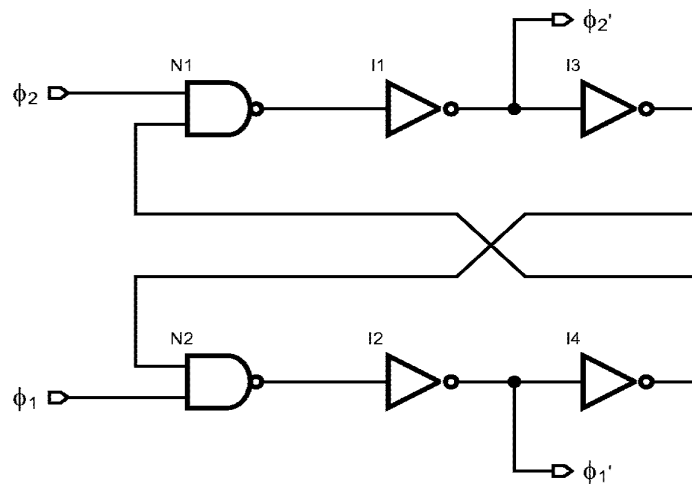


Fig. 15 (Prior Art)

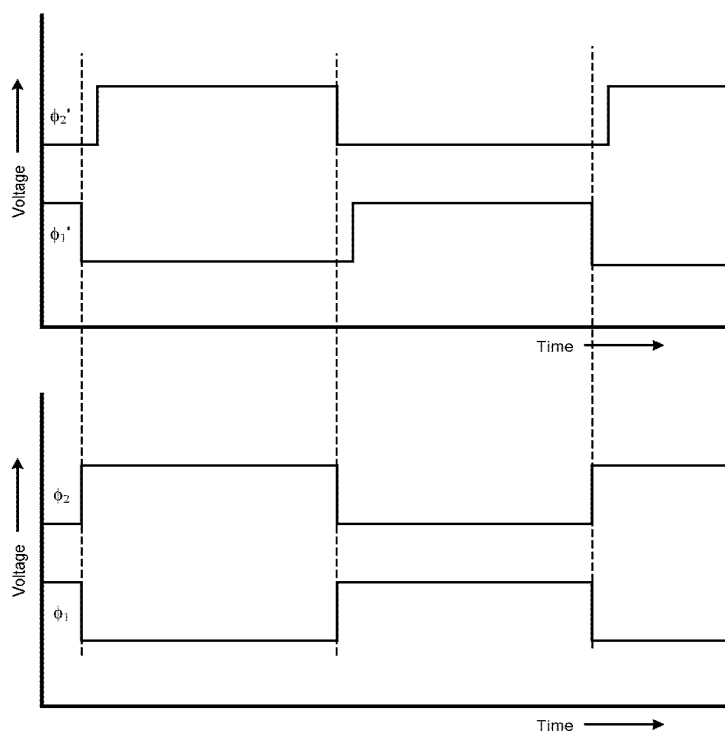


Fig. 16 (Prior Art)

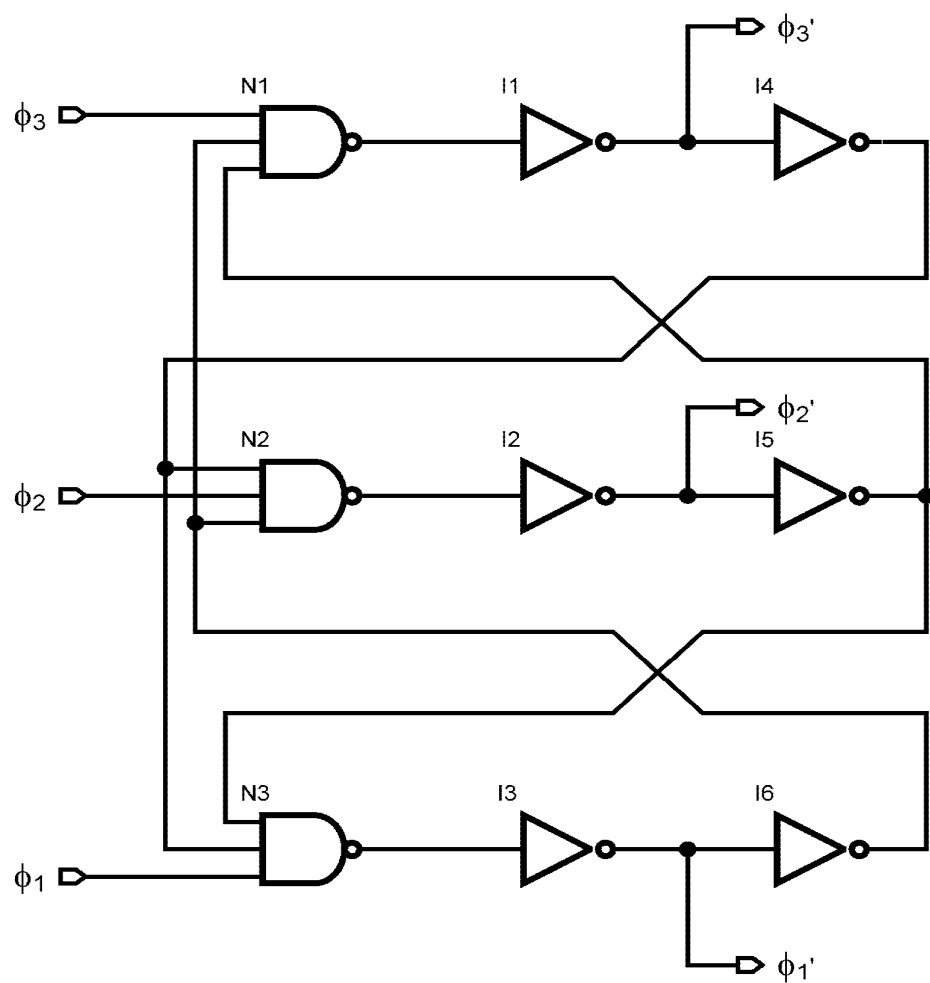


Fig. 17

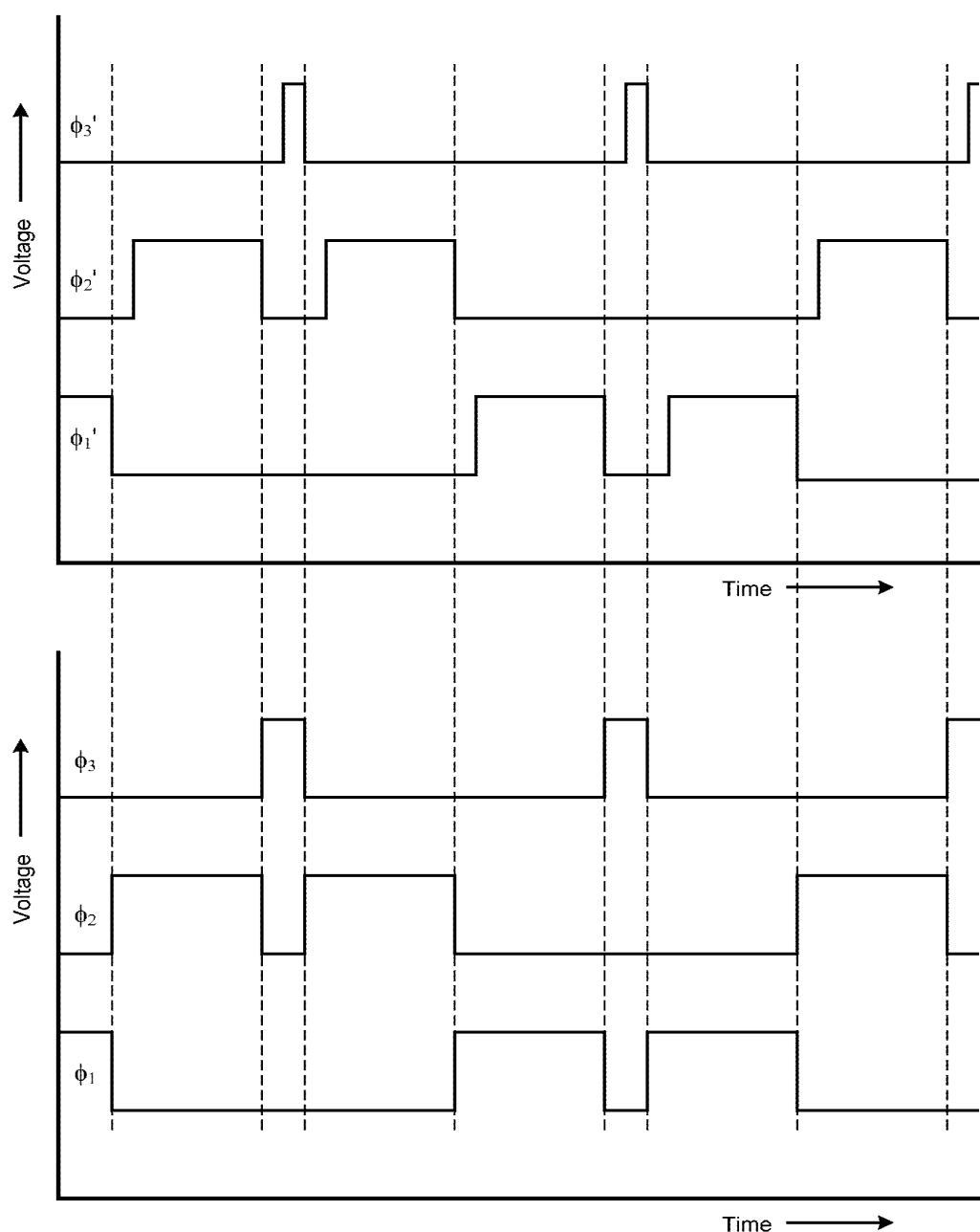


Fig. 18

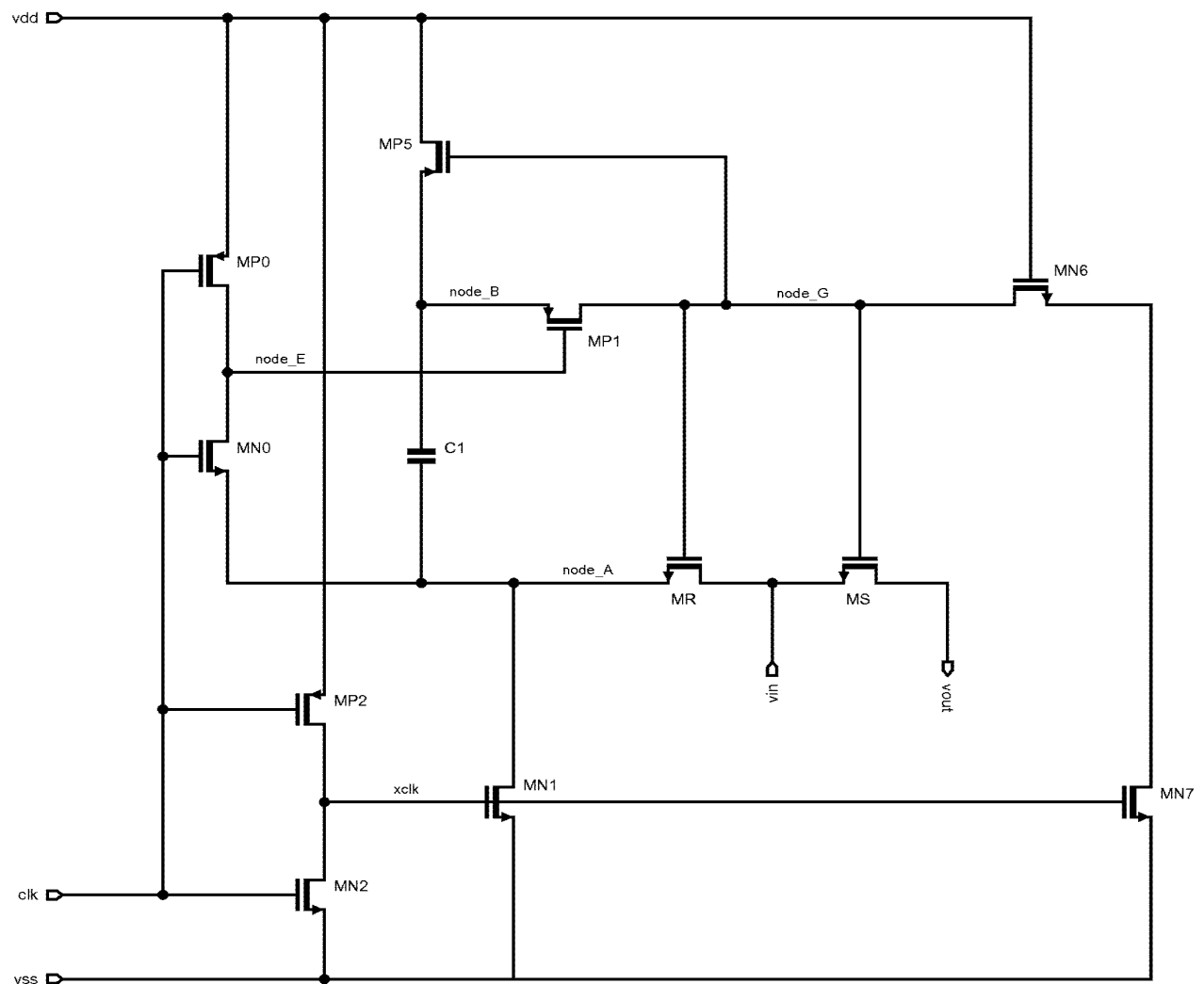


Fig. 19 (Prior Art)

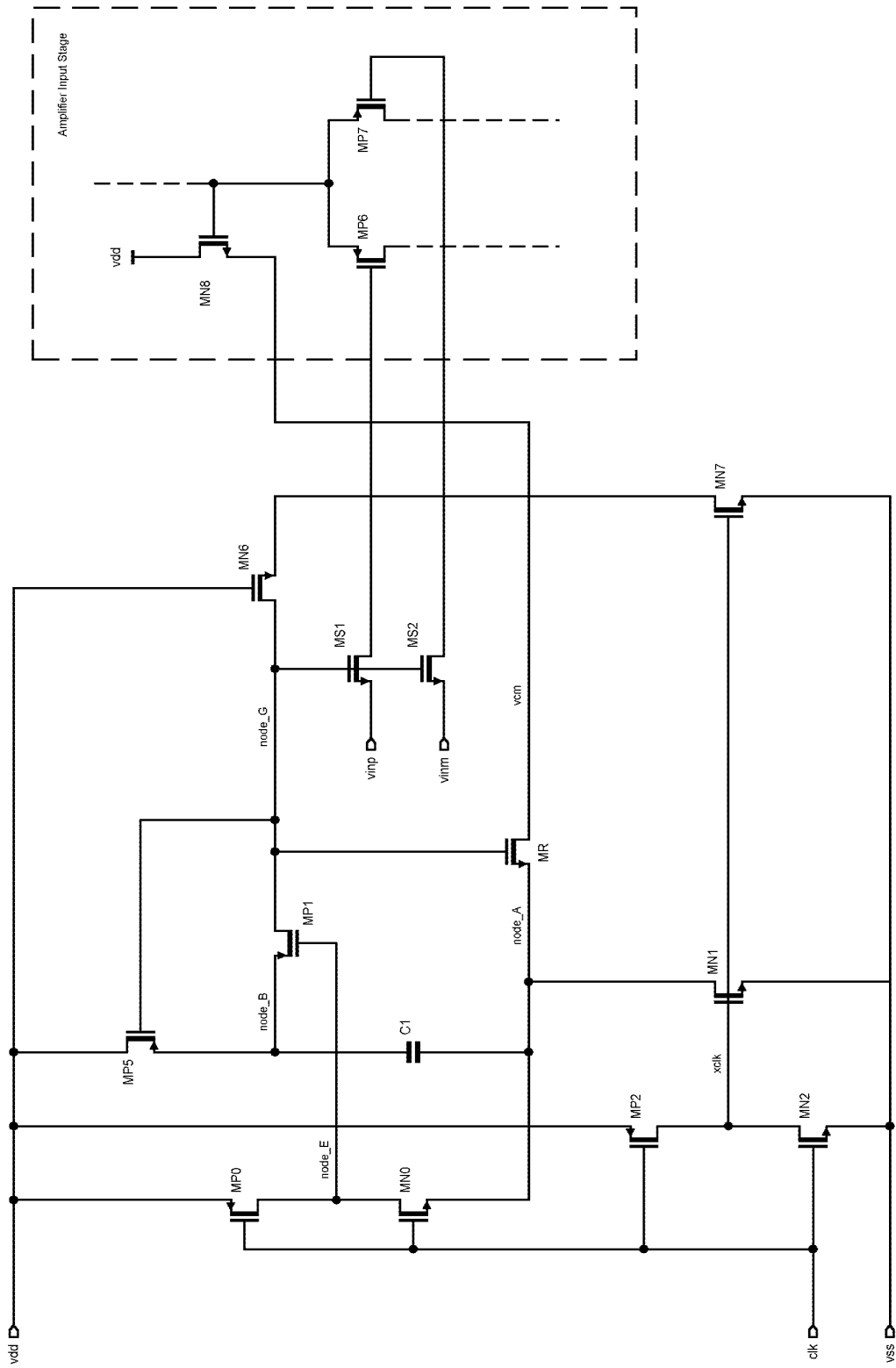
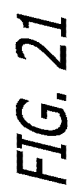


Fig. 20



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Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached?
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NAME OF SOLE OR FIRST INVENTOR: ☐ A petition has been filed for this undersigned inventor

Full Name: Rudy G. H. Eschauzier
(First, Middle [if any], Family Name (or Surname), and Suffix [if any])
Inventor's Signature  Date 5/12/09
Residence Bergschenhoek, Netherlands Citizenship Netherlands
(City, State, Country) (Country)
Mailing Address Roland Holstlaan 10
Bergschenhoek, 2662 AM Netherlands

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers		
First Named Inventor/Applicant Name:		Rudy G.H. Eschauzier		
Filer:		Roger W. Blakely/Jessica Clark		
Attorney Docket Number:		55123P376		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	16	52	832
Independent claims in excess of 3	1201	1	220	220
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2142

Electronic Acknowledgement Receipt	
EFS ID:	5370887
Application Number:	12464572
International Application Number:	
Confirmation Number:	1854
Title of Invention:	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers
First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Customer Number:	79124
Filer:	Roger W. Blakely/Jessica Clark
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Attorney Docket Number:	55123P376
Receipt Date:	20-MAY-2009
Filing Date:	12-MAY-2009
Time Stamp:	16:48:39
Application Type:	Utility under 35 USC 111(a)

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	55123P376_20090520_IDS_Letter.PDF	69470	no	1
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2	Information Disclosure Statement (IDS) Filed (SB/08)	55123P376_20090520_IDS.pdf	37641	no	1
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application No.	12/464,572
	Filing Date	May 12, 2009
	First Inventor	Rudy G. H. Eschauzier, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket No.	55123P376

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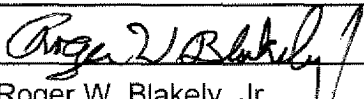
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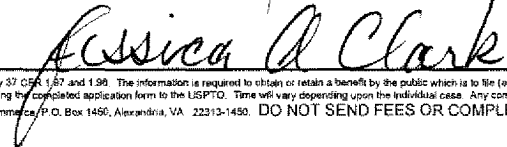
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Name/Print	Roger W. Blakely, Jr.	Registration Number	25,831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark		Date	05-20-09
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	12/464,572
	Filing Date	05/12/2009
	First Named Inventor	Rudy G.H. Eschauzier
	Group Art Unit	
	Examiner Name	
Sheet 1 of 1		Attorney Docket No: 55123P376

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		DESSOUKY, MOHAMED , et al., "Very Low-Voltage Digital-Audio $\Delta\Sigma$ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 36, No. 3, (March 2001), Pgs. 349-355	
		ENZ, CHRISTIAN C., et al., "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", <u>Proceedings of the IEEE</u> , Vol. 84, No. 11, (November 1996), Pgs. 1584-1614	
		ESCHAUZIER, RUDY G., et al., "Frequency Compensation Techniques for Low-Power Operational Amplifiers", Section 6.1, Springer, (1995)	
		ESCHAUZIER, RUDY G., et al., "Frequency Compensation Techniques for Low-Power Operational Amplifiers", Section 6.3, Springer, (1995)	
		HUIJSING, JOHAN H., "Operational Amplifiers, Theory and Design", Kluwer Academic Publishers, (2001), Pgs. 52-53	
		WESTE, NEIL H., et al., "Principles of CMOS VLSI Design, A Systems Perspective, Second Edition", Section 5.5.10, Addison-Wesley Publishing Company, (1993), Pgs. 346-350	

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Very Low-Voltage Digital-Audio $\Delta\Sigma$ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping

Mohamed Dessouky, *Student Member, IEEE*, and Andreas Kaiser, *Member, IEEE*

Abstract—A 1-V 1-mW 14-bit $\Delta\Sigma$ modulator in a standard CMOS 0.35- μm technology is presented. Special attention has been given to device reliability and power consumption in a switched-capacitor implementation. A locally bootstrapped symmetrical switch that avoids gate dielectric overstress is used in order to allow rail-to-rail signal switching. The switch constant overdrive also enhances considerably circuit linearity. Modulator coefficients of a single-loop third-order topology have been optimized for low power. Further reduction in the power consumption is obtained through a modified two-stage opamp. Measurement results show that for an oversampling ratio of 100, the modulator achieves a dynamic range of 88 dB, a peak signal-to-noise ratio of 87 dB and a peak signal-to-noise-plus-distortion ratio of 85 dB in a signal bandwidth of 25 kHz.

Index Terms—Analog circuits, bootstrapped switch, delta-sigma modulators, switched-capacitor circuits, very low voltage.

I. INTRODUCTION

FUTURE systems-on-chip will require integration of logic, analog, and memory on the same chip at low power-supply voltages. The need for the development of low-voltage and low-power analog circuit techniques is, thus, twofold. First, the demand on low-voltage low-power mixed-signal circuits is significantly increasing in order to cope with modern advances in portable and battery-operated systems. In these systems, the operating voltage and the total power consumption have a direct impact on the battery weight and lifetime. On the other side, advances in CMOS technology are driven by the digital system need to enhance the circuit speed performance and increase the integration density by continuously reducing the channel length. Lower channel lengths lead to lower supply voltages. The supply voltage is expected to drop down to around 0.6 V for a channel length of 0.05 μm by 2011 [1]. The threshold voltage, however, must remain relatively constant to keep the off transistor leakage within tolerable limits.

Analog-to-digital converters (ADCs) are one of the performance limiting blocks in any mixed-signal circuit. Robust switched-capacitor (SC) circuits are still good candidates even under very low voltage. However, in contrast to digital circuits, the power consumption of analog circuits increases as the supply voltage decreases [2]. In addition, the widely

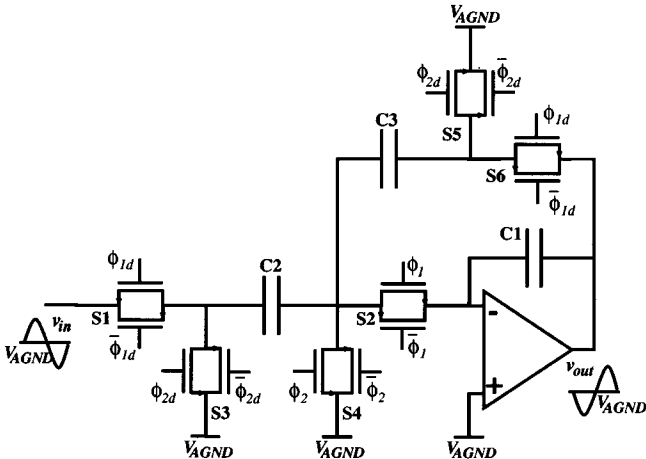


Fig. 1. SC first-order low-pass filter.

used clock voltage multiplication technique [3] cannot be employed anymore for critical switches in the circuit due to the gate dielectric reliability limitation [4]. New circuit techniques are thus needed to allow SC circuit operation under these challenging conditions and maintain, at least, the same signal-to-noise ratio (SNR).

After a brief introduction to low-voltage SC techniques, this paper describes the design of a 1-V 14-bit digital-audio $\Delta\Sigma$ modulator in a standard CMOS technology using a dedicated low-voltage switch. Special attention has been paid to device reliability and power consumption.

II. LOW-VOLTAGE SWITCHED-CAPACITOR OPERATION

Fig. 1 shows a typical first-order low-pass SC section. The analog ground potential V_{AGND} is usually set to $V_{DD}/2$ to maximize signal excursions. The CMOS switch is fully operational for supply voltages higher than the sum of the threshold voltages of both transistors $V_{thn} + V_{thp}$. For lower supply voltages, a conductance gap begins to appear around the middle of the supply range, as will be shown later on. This means that under low-voltage operation, this configuration no longer works.

Some solutions to this problem can be found in the open literature. Special fabrication processes have been modified to have, besides standard transistors, low-threshold transistors. These processes, however, are more expensive since processing steps must be added during circuit fabrication. Since the clock voltage multiplication technique [3] is not compatible with very advanced low-voltage CMOS processes where gate-oxide

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A. Kaiser is with the Institut d'Electronique et de Microelectronique du Nord (IEMN), F-59046 Lille cedex, France (e-mail: Andreas.Kaiser@isen.fr).
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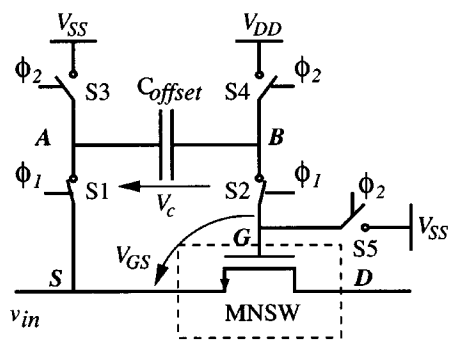


Fig. 2. Basic switch bootstrapping circuit.

breakdown becomes an issue, the switched-opamp technique [5], [6] has been proposed to get around this problem. Reference voltages are set to V_{DD} and V_{SS} ; the remaining critical switches at the outputs of each opamp, e.g., switch S6 in Fig. 1, are then eliminated by switching the opamp itself. However, the switch S1 connected to the input of the circuit remains, and it severely restricts the maximum allowable amplitude of the input signal. The switching of the opamp may also affect the speed of the circuit.

In this paper, very low-voltage SC operation has been achieved using a special low-voltage *bootstrapped* switch [7]. The basic idea of this switch is demonstrated in Fig. 2. The signal switch is transistor MNSW while the five additional switches S1-S5 and the capacitor C_{offset} constitute the bootstrap circuit. During ϕ_2 , switches S3 and S4 charge the capacitor to V_{DD} while switch S5 fixes the gate voltage of MNSW to V_{SS} to make sure that the transistor is in the off state. During ϕ_1 , switches S1 and S2 connect the precharged capacitor between the gate and the source of MNSW such that its gate-source voltage V_{GS} is equal to the voltage V_c ($\approx V_{DD}$) across the capacitor. This switch configuration allows rail-to-rail signal switching since the gate-source voltage is always constant during ϕ_1 independently of the input signal. A transistor-level implementation of the bootstrapped switch, which is fully compatible with modern low-voltage CMOS processes, is given in Section IV.A.

Fig. 3 shows a low-voltage first-order low-pass SC filter based on bootstrapped switches [8]. In order to minimize the number of bootstrapped switches, two analog reference voltages are used: V_{SS} at the opamp input where a normal n-switch can be used to switch the ground voltage, and a $V_{DD}/2$ analog reference voltage at the opamp output and at the circuit input to maximize the signal swing. The bootstrapped switch is used to switch signals at this voltage level. Using V_{SS} at the opamp input eases the biasing of the input transistors of the low-voltage opamp, however, it may cause charge leakage due to negative transient spikes [6]. Reversed biased diodes corresponding to drain/source-bulk junctions exist on all nodes of the SC circuit. Large negative voltage spikes could then forward bias these diodes, causing bulk current spikes leading to charge loss. These current spikes may also cause noise coupling to other parts of the circuit. Nodes N and I in Fig. 3 are subjected to those spikes. The associated drain/source diodes are also shown. Since the SCs C_2 and C_3 are not reset

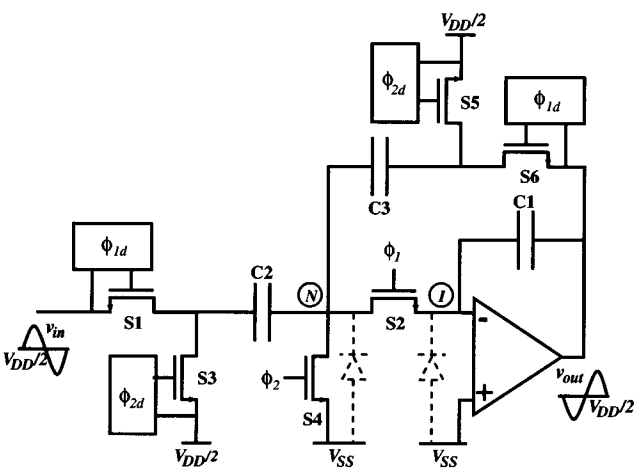


Fig. 3. Low-voltage SC first-order low-pass filter using bootstrapped switches.

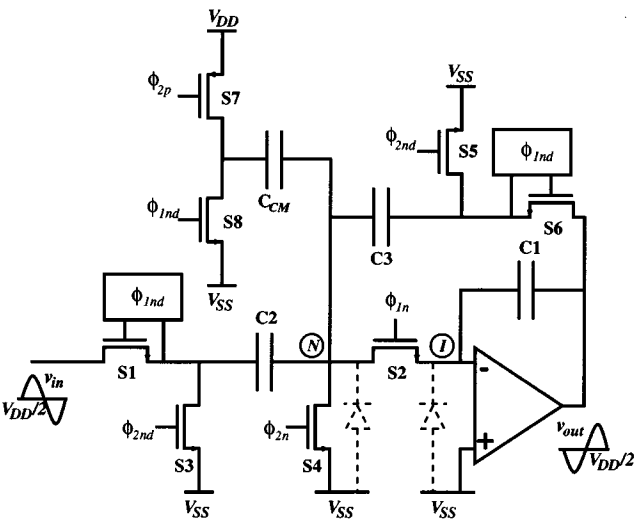


Fig. 4. Low-voltage SC first-order low-pass filter using charge cancellation.

to zero but to $V_{DD}/2$ which is also the input reference voltage, the maximum voltage step is limited to $V_{DD}/2$. For supply voltages at 1 V, the maximum spike value is thus limited to around 0.5 V. This represents the maximum spike height for an open circuit at the nodes under investigation. In spite of the opamp finite bandwidth, in practice, the spike height is much lower than this value due to the finite switching time and the fact that these nodes are already connected to the virtual ground opamp input. In addition, using delayed clock phases, as shown in Fig. 3, also reduces the amplitude of these spikes by first connecting these nodes to V_{SS} before the application of the voltage step. As a result, this spike is usually not sufficient to forward bias the drain/source-bulk diode.

Another technique to further reduce the number of bootstrapped switches is presented in [9] where a single analog reference voltage at V_{SS} is used, as shown in Fig. 4. However, the signal still varies around $V_{DD}/2$ at the circuit input as well as at the opamp output to preserve the maximum swing. The difference between the two reference voltages is compensated by injecting a fixed amount of charge at the opamp input using an extra capacitor C_{CM} [6]. This extra capacitor, however, increases the switching noise. It also decreases the opamp

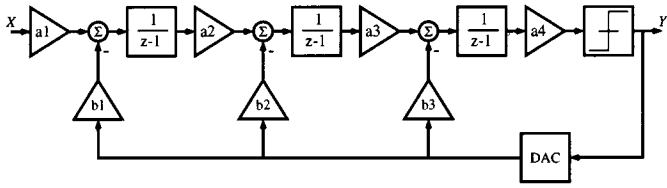


Fig. 5. Modulator topology.

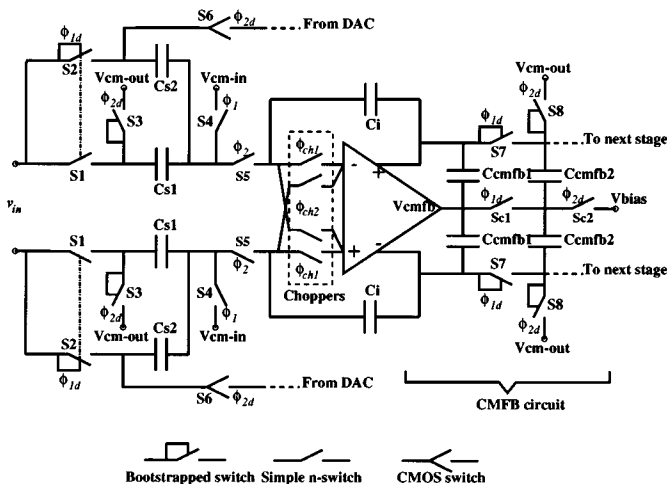


Fig. 6. Fully differential low-voltage integrator.

feedback factor β leading to an increase of the amplifier closed-loop settling time.

III. MODULATOR ARCHITECTURE

For low-voltage low-power applications, a single-loop $\Delta\Sigma$ modulator topology is preferable over a cascaded one because it has more relaxed requirements on linear amplifier nonidealities, such as the dc gain and the gain-bandwidth product. Also, since noise injected at the internal nodes is reduced so much by the large gain of the preceding integrators, integrators inside the feedback loop can be scaled down resulting in a lower power dissipation [10]. However, in order to keep the oversampling ratio relatively low to reduce power consumption, the loop order must be increased. A third-order feedback topology based on delayed integrators, shown in Fig. 5, is thus used. Fig. 6 shows the SC circuit implementation of a fully differential integrator cell used in the modulator, based on the low-voltage technique shown in Fig. 3. The supply voltage is set to 1 V. The amplifier output common-mode (CM) voltage V_{cm-out} is set to the mid-supply 0.5 V, while its input CM voltage V_{cm-in} is set to V_{SS} . CMOS switches are only used to switch the digital-to-analog converter (DAC) levels, namely V_{SS} and V_{DD} . The same bootstrap circuit can be used to drive parallel switches. This can be seen for switches S1 and S2 in Fig. 6. Delayed clocks are used for the input switches S1, S2, and S3, as well as the feedback switch S6 to reduce charge injection.

Modulator coefficients have been determined with the help of the *Delta-Sigma Toolbox* [11] for MATLAB [12], according to the design procedure described in [13]. Table I shows the corresponding scaled modulator coefficients.

TABLE I
MODULATOR COEFFICIENTS.

	Interstage Coeff.	Feedback Coeff.
1 st Integrator	$a_1 = 0.10$	$b_1 = 0.10$
2 nd Integrator	$a_2 = 0.27$	$b_2 = 0.18$
3 rd Integrator	$a_3 = 0.31$	$b_3 = 0.17$
Comparator	$a_4 = 4.35$	

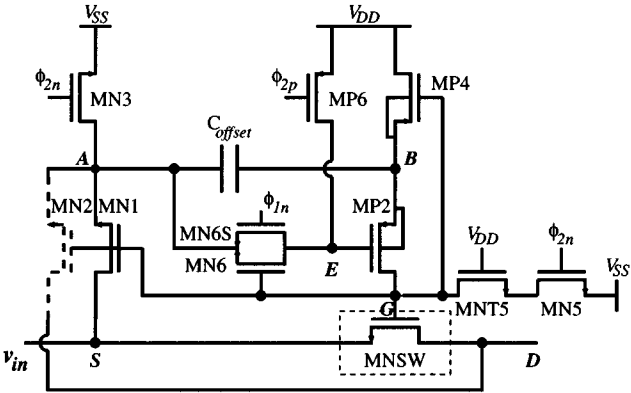


Fig. 7. Transistor-level implementation of the bootstrapped switch.

IV. LOW-VOLTAGE BUILDING BLOCKS

In this section, the low-voltage circuit building blocks used in the modulator are discussed.

A. Symmetrical Bootstrapped Switch

Fig. 7 shows the transistor-level implementation of the switch bootstrapping circuit shown in Fig. 2 [14]. Transistors MN1, MP2, MN3, MP4, and MN5 correspond to the five ideal switches S1-S5 respectively. Additional transistors and modified connectivity shown in Fig. 7 were introduced to extend all switch operation from rail-to-rail while limiting all gate-source voltages to V_{DD} . Gate connections of MP4 and MP2 prevent their overstress as the voltage on node B rises above V_{DD} . Transistor MN6S triggers MP2 on at the beginning of ϕ_1 while transistor MN6 keeps it on as the voltage on node A rises to the input voltage v_{in} . Gate connections of transistors MN1 and MN6 allow them to be turned on similar to the main switch MNSW. Furthermore, transistor MNT5 has been added to prevent the gate-drain voltage of MN5 from exceeding V_{DD} during ϕ_1 while it is off. During ϕ_1 when MNT5 is off, its drain-bulk diode junction voltage reaches a reverse bias voltage of $2V_{DD}$. This must be compatible with the technology limits. It should be also noted that the bulk of transistors MP2 and MP4 must be tied to the highest potential, i.e., node B, and not to V_{DD} .

However, in the circuit presented in [14], the voltage at the drain side of the main switch MNSW must be always higher than that at the source side at the switching moment to prevent the drain-gate voltage from exceeding V_{DD} during the turn-on transient. While this is not a problem for the SC charge cancellation scheme shown in Fig. 4, since the source terminal of the bootstrapped switch is always discharged to V_{SS} , in the corresponding SC configuration shown in Fig. 3, the drain side could have lower voltages before switching on. In order to overcome

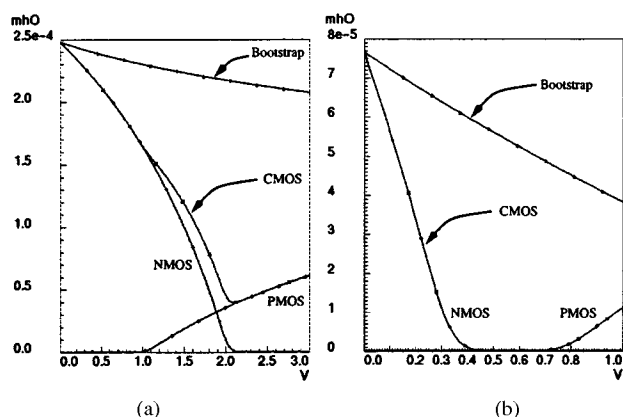


Fig. 8. Comparison of the bootstrapped and the CMOS switch conductance using minimal size transistors $W/L = 0.5\mu/0.35\mu$. (a) $V_{DD} = 3$ V. (b) $V_{DD} = 1$ V.

this limitation, an additional transistor MN2 has been added on the drain side, shown dashed in Fig. 7, such that the switch MNSW becomes completely symmetrical. The gate voltage is thus clamped at a voltage V_{DD} higher than the terminal of the lowest terminal voltage.

This bootstrapping circuit thus allows switch operation (transistor MNSW) from rail-to-rail while limiting all gate-source/drain voltages to V_{DD} avoiding any oxide overstress. Fig. 8 shows the conductance of a minimal size bootstrapped switch versus the source potential for two different supply voltages. Also shown is the conductance of a CMOS switch. For the 3-V case, shown in Fig. 8(a), the bootstrapped switch conductance has less variations than that of the CMOS case. This means that using this switch would reduce significantly harmonic distortion effects, such as charge injection related to switch operation. For the 1-V case, shown in Fig. 8(b), while the CMOS switch fails due to the conductance gap for signal voltages in the mid-supply range, the bootstrapped switch allows rail-to-rail operation. In spite of the fact that the gate-source potential of the bootstrapped switch is held constant, the conductance drops with the source voltage due to the source-bulk potential which increases the threshold voltage. In [15], a solution to this bulk effect is proposed through the use of a separate well p-transistor as the main switch and controlling its bulk potential.

It is to be mentioned that other bootstrapped switch implementations have been proposed. In [16], a MOS-only implementation was presented, however, no attention has been paid to reliability problems. In [4], reliability problems have been addressed, however, the bootstrap implementation [14] used in this work has the merit of being much simpler and addressing the transient reliability problem.

B. Opamp

In very low-voltage SC circuits, stacked transistors cannot be used to achieve the required DC gain. Thus, usually a two-stage amplifier is needed. Fig. 9 shows the used opamp [8]. It is based on a fully differential folded-cascode p-type two-stage Miller-compensated configuration. The second stage is a common-source amplifier with active load which also allows a large output swing.

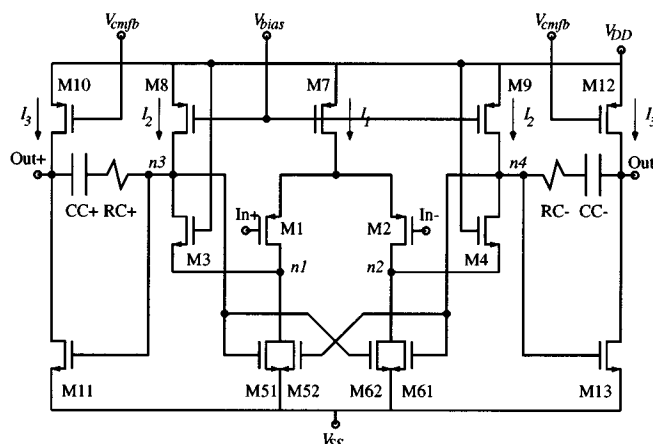


Fig. 9. Two-stage amplifier with inherent first-stage CMFB.

Due to the differential structure, the CM output voltage of both stages needs to be regulated using common-mode feedback (CMFB). Biasing of class-A amplifiers is typically accomplished with a CMFB circuit that senses the output CM voltage in order to control the tail current source in the first stage. However, owing to stability considerations, the gain and bandwidth of the CMFB loop are limited to, at most, those of the differential mode signal path. Moreover, since the gain from the first stage to the output is positive, an additional inverting amplifier is needed to achieve a stable CMFB, thus increasing the overall power consumption. This CMFB amplifier also limits the output swing of the original differential amplifier.

In order to avoid this extra CM amplifier, the CMFB circuit for the first stage has been replaced by the cross-coupled connection of transistors M51, M52, M61, and M62, similar to [17]. The differential output conductance seen at the output of the first stage (nodes $n3$ and $n4$) is given by

$$g_{ds_{out1}} = g_{ds8} + (gm_{51} - gm_{52}) + \frac{g_{ds3}(g_{ds1} + 2g_{ds51})}{g_{ds3} + g_{ds1} + 2g_{ds51} + gm_3 + gmb_3}. \quad (1)$$

With $gm_{51} = gm_{52}$, the transconductance gm_{51} seen at the gate of transistors M51 and M61 is thus canceled by the opposite action of the parallel transistors M52 and M62, respectively. This negative feedback connection causes the differential signal at the output of the first stage to see a high load impedance limited by $1/g_{ds8}$. On the other hand, for the common mode signal, the output conductance is still given by (1) with the negative sign turned positive. The conductance is thus limited by $gm_{51} + gm_{52}$. This is a low impedance and consequently the first stage does not require an additional CMFB circuit.

For the second stage, a simple passive SC CMFB circuit, shown in Fig. 6, is used. Since the output CM of the amplifier is set to $V_{DD}/2$, bootstrapped switches must be used in the CMFB circuit for those switches connected to the amplifier output. Those bootstrapped switches, however, can be shared with the sampling network connecting the integrator output to the subsequent stage, as shown in Fig. 6.

The amplifier has a minimum supply voltage, determined by the cross-coupled connection, of $V_{GS1} + V_{DSsat8}$ which is around 1 V. This low supply voltage allows biasing the cascode

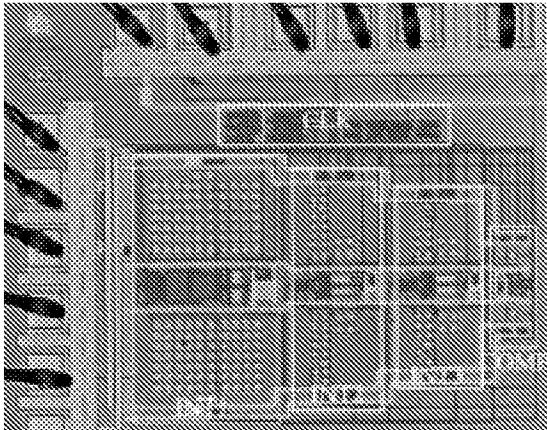


Fig. 12. Chip die photo.

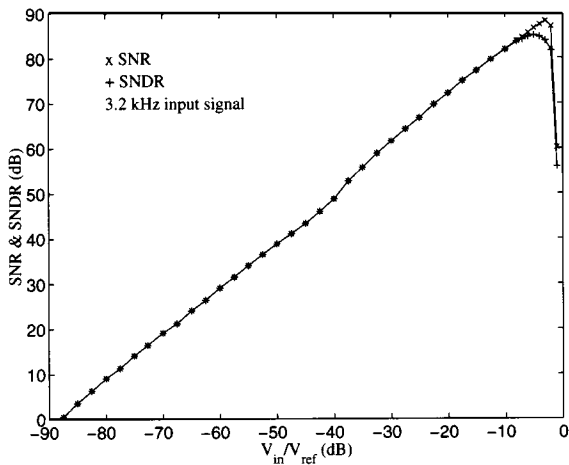


Fig. 13. Measured SNR and SNDR.

VI. EXPERIMENTAL RESULTS

The modulator has been implemented in a 0.35-μm standard CMOS process with double-poly and triple-metal levels. The threshold voltages for the n- and p-transistors are 580 and 600 mV, respectively. Fig. 12 shows the chip photograph. Capacitors have been implemented using the two poly layers. The core area excluding bonding pads is 0.9 × 0.7 mm². A single clock at 5 MHz is used to drive the modulator. The nonoverlapping delayed clock phases as well as the overlapping clock phases at half the clock frequency needed for the chopper stabilization circuit are all generated on chip.

On the test board, the input signal is converted from single-ended to differential using a transformer and shifted to a CM level equal to $V_{DD}/2$. The digital output of the modulator is captured with a data analyzer through optocouplers to isolate ground noise of the digital measurement equipment. The data are then transferred to a PC, which performs fast Fourier transform (FFT), windowing, and graphical representation.

The modulator operates at a V_{DD} of 1 V and dissipates 950 μW including the digital circuitry. 60% of the total power is consumed by the first integrator. The reference voltage is set to 1 V and is brought on chip on a separate pad. With an oversampling ratio of 100, the signal bandwidth is 25 kHz. Fig. 13 shows the measured SNR and signal-to-noise-plus-distortion

TABLE II
CONVERTER PERFORMANCE SUMMARY.

Supply Voltage	1 V
Reference Voltage	1 V
DR	88 dB
Peak SNR / SNDR	87 dB / 85 dB
Oversampling Ratio	100
Sampling Rate	5 MHz
Signal Bandwidth	25 kHz
Power Consumption	950 μW
Figure of Merit ×10 ⁶	275
Die Area	0.9 mm × 0.7 mm
Technology	0.35 μm CMOS TMDP

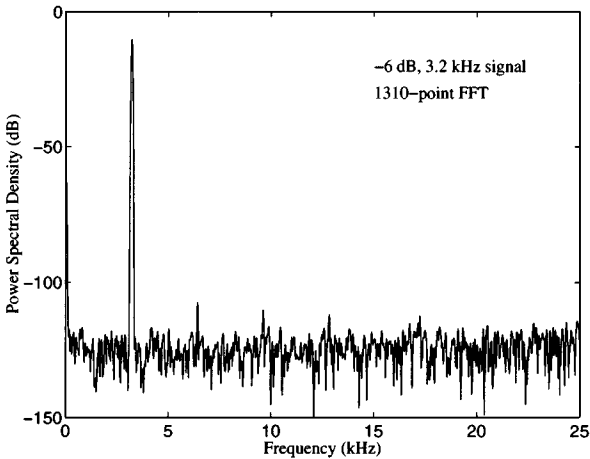


Fig. 14. Measured baseband output spectrum.

ratio (SNDR) versus the relative input amplitude (V_{in}/V_{ref}). An input sinusoidal signal at 3.2 kHz was used to produce these plots. It is apparent that the modulator achieves a dynamic range (DR) of 88 dB, and a peak SNR and peak SNDR of 87 and 85 dB, respectively. The measured performance is summarized in Table II. Fig. 14 shows the output baseband spectrum for a 3.2-kHz input signal at -6 dB relative input level. The frequency independence of the noise floor indicates that the modulator’s performance is thermal-noise limited rather than quantization-noise limited.

Various ADC implementations are often compared using the following figure of merit [3]:

$$FM = \frac{4kT \times DR \times f_N}{P} \tag{2}$$

where f_N is the Nyquist sampling frequency and P is the total power dissipation. Compared to another very low-voltage ΔΣ implementation presented in [10], the current design achieves practically the same figure of merit, whereas the SNDR is about 25 dB higher. Further improvement in the dynamic range may be obtained by reducing the opamp thermal noise.

VII. CONCLUSION

A 1-V ΔΣ modulator has been implemented using the local switch bootstrapping technique. Rail-to-rail operation of bootstrapped switches allows very low-voltage robust SC implementations in standard CMOS technologies while avoiding tran-

sistor gate oxide overstress. Contrary to clock boosting circuits, the bootstrapping circuit presented in this work is thus fully compatible with future low-voltage technologies. Furthermore, switch charge injection and linearity is improved due to the constant gate-source overdrive. An additional transistor renders the switch completely symmetrical and eliminates transient reliability problems.

Modifications introduced to the two-stage folded cascode opamp allow very low-voltage operation and permit the use of a passive CMFB SC circuit.

Obtained results show the feasibility of very low-voltage high performance circuits using common SC techniques.

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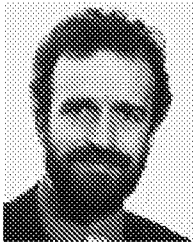


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Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization

CHRISTIAN C. ENZ, MEMBER, IEEE, AND GABOR C. TEMES, FELLOW, IEEE

Invited Paper

In linear IC's fabricated in a low-voltage CMOS technology, the reduction of the dynamic range due to the dc offset and low-frequency noise of the amplifiers becomes increasingly significant. Also, the achievable amplifier gain is often quite low in such a technology, since cascoding may not be a practical circuit option due to the resulting reduction of the output signal swing. In this paper, some old and some new circuit techniques will be described for the compensation of the amplifier most important nonideal effects including the noise (mainly thermal and $1/f$ noise), the input-referred dc offset voltage, as well as the finite gain resulting in a nonideal virtual ground at the input.

I. INTRODUCTION¹

In linear active circuits, the active element most often used is the operational amplifier (op-amp), whose main function in the circuit is to create a virtual ground, i.e., a node with a zero (or constant) voltage at its input terminal without sinking any current. Using op-amps with MOS input transistors, the op-amp input current at low frequencies can indeed be made extremely small; however, the input voltage of a practical op-amp is usually significantly large (typically of the order of 1–10 mV), since it is affected by several nonideal effects. These include noise (most importantly, $1/f$ and thermal noise), the input-referred dc offset voltage, as well as the signal voltage needed to generate the desired output voltage of the op-amp. Normally, the thermal noise occupies a wide frequency band, while the $1/f$ noise, offset and input signal are narrowband low-frequency signals.

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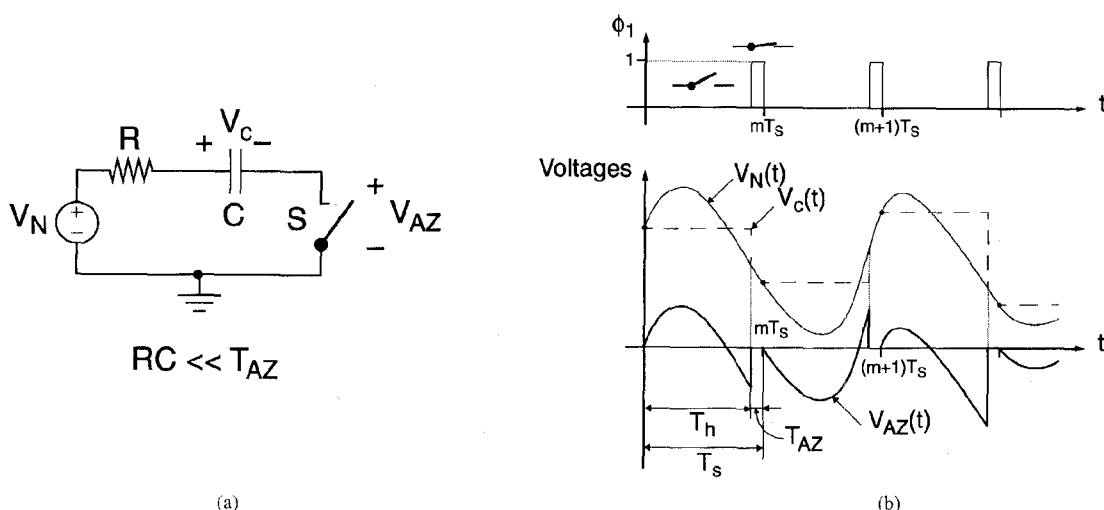
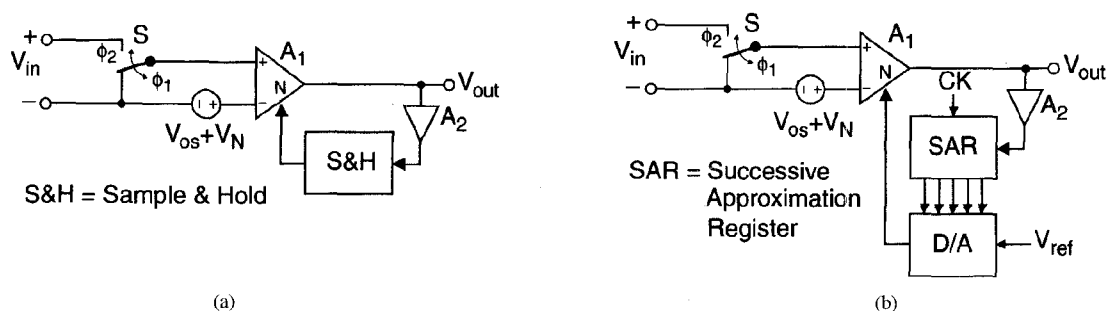
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¹ This work is dedicated to Prof. Karoly Simonyi on his 80th birthday.

The purpose of the circuit techniques discussed in this paper is to reduce the effects of the narrow-band noise sources at the virtual ground of an op-amp stage. By reducing the low-frequency noise and offset at the op-amp input, hence the dynamic range of the circuit is improved; by reducing the signal voltage at the virtual ground terminal, the effect of the finite low-frequency gain of the op-amp on the signal-processing characteristics of the stage is decreased. Both improvements are especially significant for low-supply voltage circuits, which have limited signal swings and where the op-amp gain may be low since headroom for cascoding may not be available. The proposed techniques are applicable to such important building blocks as voltage amplifiers, ADC and DAC stages, integrators and filters, sample-and-hold (S/H) circuits, analog delay stages, and comparators.

Sections II and III present the two basic techniques that are used to reduce the offset and low-frequency noise of op-amps, namely the autozero (AZ) and chopper stabilization (CHS) techniques. A clear distinction is made between autozeroing, which is a sampling technique, and CHS, which is a modulation technique, mainly with respect to their effect on the amplifier broadband noise. The correlated double sampling (CDS) technique is described in Section II as a particular case of AZ where, as its name indicates, the amplifier noise and offset are sampled twice in each clock period. Then, Section IV treats the most important practical issues at the transistor and circuit level that are faced when implementing the offset and noise reduction techniques discussed previously. Section V presents fundamental building blocks that are used for sampled-data analog signal processing. They are all realized as switched-capacitor (SC) circuits and therefore exploit the CDS technique not only for reducing the offset and the $1/f$ noise, but also to lower the sensitivity of the circuit performance to the finite amplifier gain. Examples of SC S/H stages, voltage amplifiers, integrators, and filters are

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presented. An example of the use of the CHS technique to realize a low-noise and low-offset micropower amplifier for instrumentation applications is presented in Section VI. Finally, a summary is given in Section VII, where the two techniques discussed in this paper are compared.

II. AUTOZEROING AND CORRELATED DOUBLE SAMPLING TECHNIQUES

In this section, the principle of AZ and CDS techniques will be introduced and their effect on offset and noise analyzed.

A. Basic Principle

The basic idea of AZ is sampling the unwanted quantity (noise and offset) and then subtracting it from the instantaneous value of the contaminated signal either at the input or the output of the op-amp. This cancellation can also be done at some intermediate node between the input and the output of the op-amp, using an additional input port defined as the nulling input and identified with the letter N in the schematics of Fig. 1.

If the noise is constant over time (like a dc offset) it will be cancelled, as needed in a high-precision amplifier or high-resolution comparator. If the unwanted disturbance

is low-frequency random noise (for example, $1/f$ noise), it will be high-pass filtered and thus strongly reduced at low frequencies but at the cost of an increased noise floor due to aliasing of the wideband noise inherent to the sampling process. The general principle of the AZ process will first be described considering only the input referred dc offset voltage V_{os} and will then be extended to the input referred random noise voltage V_N .

The AZ process requires at least two phases: a sampling phase (ϕ_1) during which the offset voltage V_{os} and the noise voltage V_N are sampled and stored, and a signal-processing phase (ϕ_2) during which the offset-free stage is available for operation. The two major categories of AZ are shown in Fig. 1. During the sampling phase (shown in Fig. 1), the amplifier is disconnected from the signal path, its inputs are short-circuited and set to an appropriate common-mode voltage. The offset is nulled using an auxiliary nulling input port N by means of an appropriate feedback configuration and/or a dedicated algorithm. The control quantity x_c is next sampled and stored, either in an analog form as a voltage using a S/H stage [Fig. 1(a)] or in a digital form, using for example a register [Fig. 1(b)]. The output V_{out} is forced to a small value in these particular configurations. The input terminals of the amplifier can afterwards be connected back to the signal source for amplification. If

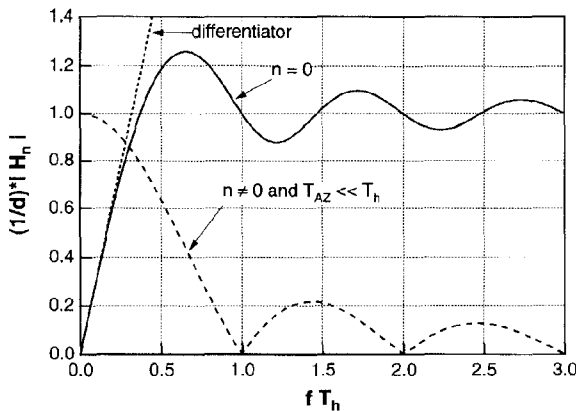


Fig. 3. Autozero baseband and foldover bands transfer functions.

it is used under the same conditions as during sampling, the amplifier will ideally be free from any unwanted offset.

B. The Effect of AZ on the Noise

The autozero principle can be used not only to cancel the amplifier offset but also to reduce its low-frequency noise, for example $1/f$ noise. But unlike the offset voltage, which can be considered constant, the amplifier's noise and particularly its wideband thermal noise component is time-varying and random. The efficiency of the AZ process for the low-frequency noise reduction will thus strongly depend on the correlation between the noise sample and the instantaneous noise value from which this sample is subtracted. The autocorrelation between two samples of $1/f$ noise separated by a time interval τ decreases much slower with increasing τ than it does for white noise, assuming they have the same bandwidth. The AZ process is thus efficient for reducing the $1/f$ noise but not the broadband white noise.

Another way of looking at the effect of AZ is to note that it is equivalent to subtracting from the time-varying noise a recent sample of the same noise. For dc or very low-frequency noise this results in a cancellation. This indicates that AZ effectively high-pass filters the noise.

In addition to this basic high-pass filtering process, since AZ is a sampling technique, the wideband noise is aliased down to the baseband, increasing the resulting in-band power spectral density (PSD) unless the system is already a sampled-data one.

The effects of AZ on the amplifier's noise can be better understood by analyzing the simple circuit shown in Fig. 2, where source V_N may represent the noise at the output of the amplifier in the autozero phase [see, i.e., Fig. 21(a)]. Each time switch S is closed, the output voltage V_{AZ} is

reset to zero and the noise source voltage V_N appears across resistor R and capacitor C . Assuming $RC \ll T_{AZ}$, at the end of the sampling phase (when switch S opens) the noise voltage V_N is sampled onto capacitor C . The output voltage becomes equal to the difference between the instantaneous voltage V_N and the voltage V_c stored on capacitor C . This eliminates the dc component of V_N , but not its time-varying part. It can be shown [8] that if source voltage $V_N(t)$ corresponds to a stationary random noise with a PSD $S_N(f)$, the PSD of the autozero voltage across the switch can be decomposed into two components: one caused by the baseband noise (which is reduced by the AZ process) and the other by the foldover components introduced by aliasing. Thus

$$S_{AZ}(f) = \underbrace{|H_0(f)|^2 S_N(f)}_{\text{baseband}} + \underbrace{S_{fold}(f)}_{\text{foldover}} \quad (1)$$

where

$$S_{fold}(f) \equiv \sum_{\substack{n=-\infty \\ n \neq 0}}^{+\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right). \quad (2)$$

The foldover component results from the replicas of the original spectrum shifted by the integer multiples of the sampling frequency. The baseband transfer function $|H_0(f)|^2$ is given by (see (3) at the bottom of the page) where $d \equiv T_h/T_s$ is the duty cycle of the clock signal [Fig. 2(b)]. The magnitude of $H_0(f)$ normalized to the duty cycle d is plotted as a function of $f T_h$ in Fig. 3, which shows its high-pass characteristic. Note that for $\pi f T_h \ll 1$, $H_0(f)$ acts like a differentiator

$$|H_0(f)| \cong \pi f T_h. \quad (4)$$

It imposes a zero at the origin of frequency axis that cancels out any dc component present in $V_N(t)$. The other transfer functions $|H_n(f)|^2$ for $n \neq 0$ are derived in the Appendix. Their shape depends on the duty cycle d , but they all merge to a common function in the case the AZ time T_{AZ} can be considered much smaller than the hold time ($T_{AZ} \ll T_h$)

$$|H_n(f)|^2 \cong [d \cdot \text{sinc}(\pi f T_h)]^2 \quad \text{for } n \neq 0 \text{ and } T_{AZ} \ll T_h \quad (5)$$

where $\text{sinc}(x) \equiv \sin(x)/x$. $|H_n(f)|$ is plotted in Fig. 3.

The PSD at the output of the AZ circuit clearly depends on the PSD of the source which is autozeroed. The low-frequency input-referred noise PSD of an amplifier generally contains both a white and a $1/f$ noise component. It can be written in the following convenient form:

$$S_N(f) = S_0 \left(1 + \frac{f_k}{|f|}\right) \quad (6)$$

$$|H_0(f)|^2 = d^2 \left\{ \left[1 - \frac{\sin(2\pi f T_h)}{2\pi f T_h}\right]^2 + \left[\frac{1 - \cos(2\pi f T_h)}{2\pi f T_h}\right]^2 \right\} \quad (3)$$

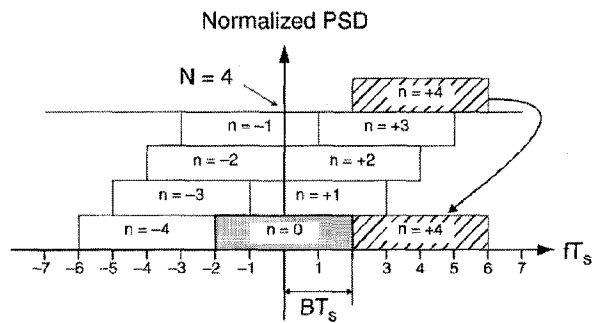


Fig. 4. Aliasing of an ideally low-pass filtered white noise having a bandwidth equal to twice the sampling frequency.

where S_0 represents the white noise PSD and f_k is the corner frequency, defined as the frequency for which the $1/f$ noise PSD becomes equal to the white noise S_0 . The corner frequency of amplifiers having MOS input devices can be relatively high (typically ranging from 1 kHz to as high as 100 kHz), which means that in the absence of aliasing the input noise is often dominated by the $1/f$ noise component in the frequency range of interest. The effect of AZ will be examined separately for each of these PSD components, starting with the white noise.

The foldover component defined by (2) can easily be calculated if the amplifier's broadband white noise is considered as an ideally low-pass filtered white noise having a bandwidth equal to B . The aliasing effect introduced by the sampling process in this case is illustrated in Fig. 4 for $BT_s = 2$ (i.e., for a noise bandwidth $B =$ four times the Nyquist frequency). Fig. 4 clearly shows the effect of undersampling the broadband white noise: the original noise power spectrum is shifted by multiples n of the sampling frequency and summed, resulting in a white noise of PSD value approximately equal to NS_0 , where N is the integer closest to the undersampling factor defined by $2BT_s$. Thus

$$\sum_{n=-\infty}^{+\infty} S_N \left(f - \frac{n}{T_s} \right) \cong 2BT_s S_0. \quad (7)$$

The signal corresponding to (7) has no physical reality since its power is infinite. The power is actually bounded by the $\text{sinc}^2(\pi f T_s)$ function introduced by the hold operation. The foldover component in the Nyquist range is then simply derived from (7) by subtracting the original band ($n = 0$) and multiplying the remainder by the $\text{sinc}^2(\pi f T_s)$ function:

$$S_{\text{fold-white}}(f) = (2BT_s - 1)S_0 \text{sinc}^2(\pi f T_s). \quad (8)$$

This result can be extended to the case of a first-order low-pass filtered white noise with a PSD

$$S_{N\text{-white}}(f) = \frac{S_0}{1 + \left(\frac{f}{f_c} \right)^2} \quad (9)$$

where f_c is the 3-dB noise bandwidth, which typically corresponds to the amplifier gain-bandwidth product when the noise is sampled with the op-amp in a unity-gain configuration. Therefore, f_c is generally much larger than

the sampling frequency $f_s \equiv 1/T_s$. The detailed analysis given in [8] shows that (8) also holds for the foldover component of a first-order low-pass filtered white noise if B is replaced by the equivalent noise bandwidth defined by

$$B \equiv \frac{1}{S_0} \int_{-\infty}^{+\infty} S_{N\text{-white}}(f) df = \frac{\pi}{2} f_c. \quad (10)$$

If the undersampling factor $2BT_s = \pi f_c T_s$ is much larger than unity, the foldover component dominates, since the baseband term $|H_0(f)|^2$ is bounded by 1.6. The autozeroed white noise is thus dominated by the aliased broadband noise component and can be approximated by

$$S_{AZ\text{-white}}(f) \cong S_{\text{fold-white}}(f) \cong (\pi f_c T_s - 1)S_0 \text{sinc}^2(\pi f T_s). \quad (11)$$

The PSD of a first-order low-pass filtered white noise having a bandwidth five times larger than the sampling frequency² ($f_c T_s = 5$) and the different PSD components resulting from the AZ process are plotted in Fig. 5. It clearly shows that the autozeroed noise PSD is dominated by the foldover component in the Nyquist band ($|f T_s| \leq 0.5$).

A similar analysis can be carried out for a first-order low-pass filtered $1/f$ noise having a PSD given by

$$S_{N\text{-}1/f}(f) = \frac{S_0 f_k}{|f| \left[1 + \left(\frac{f}{f_c} \right)^2 \right]}. \quad (12)$$

As shown in Fig. 6, the input $1/f$ noise is zeroed, removing the original divergence of the $1/f$ noise occurring at the origin of frequency. Although $1/f$ noise has a narrow bandwidth, it still has a foldover component due to the aliasing of all the tails of the $1/f$ noise. This foldover component and the original baseband PSD are plotted in Fig. 6 for $f_c T_s = 5$ and for a corner frequency equal to the sampling frequency ($f_k T_s = 1$).

The foldover component for the $1/f$ noise can be approximated [8] in the Nyquist range by

$$S_{\text{fold-}1/f} \cong 2S_0 f_k T_s [1 + \ln(\frac{2}{3} f_c T_s)] \text{sinc}^2(\pi f T_s). \quad (13)$$

Comparing $S_{\text{fold-}1/f}$ to the corresponding term obtained for the white noise (8), it can be seen that it increases proportionally to $f_c T_s$ for the white noise, but only logarithmically for the $1/f$ noise. The effect of aliasing on the $1/f$ noise is thus not as dramatic as on the broadband white noise.

The PSD at the output of the AZ circuit at low frequencies, considering both the white and the $1/f$ component given by (6) and assuming $\pi f_c T_s \gg 1$, can simply be obtained from (11) and (13):

$$S_{AZ}(f) = |H_0(f)|^2 S_N(f) + S_{\text{fold}} \quad (14)$$

²This selection reflects the requirement $f_c T_s \geq 5$ needed for the full settling of an SC stage [10].

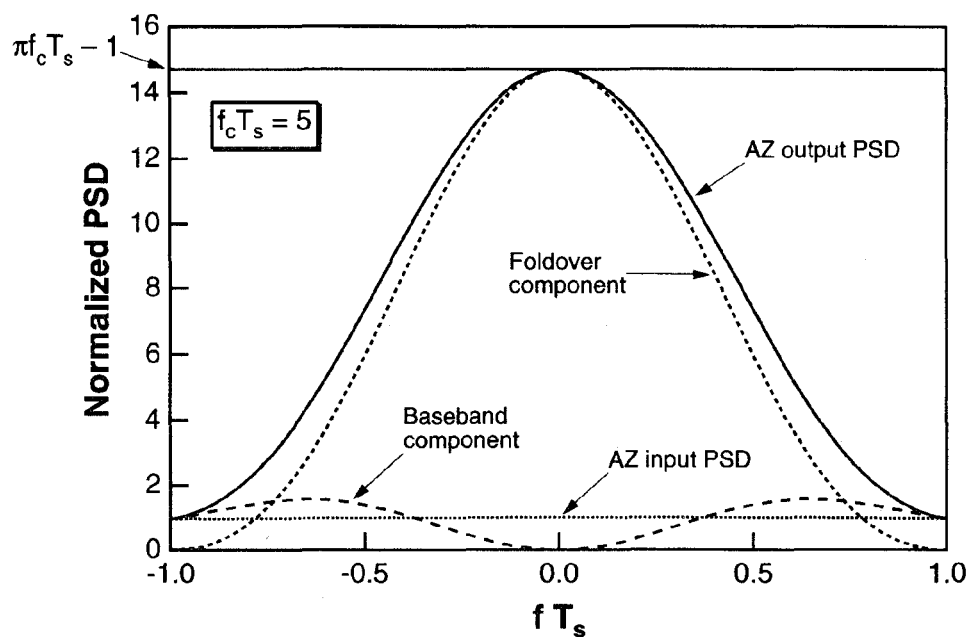


Fig. 5. Effect of the AZ process on a first-order low-pass filtered white noise with a bandwidth five times larger than the sampling frequency.

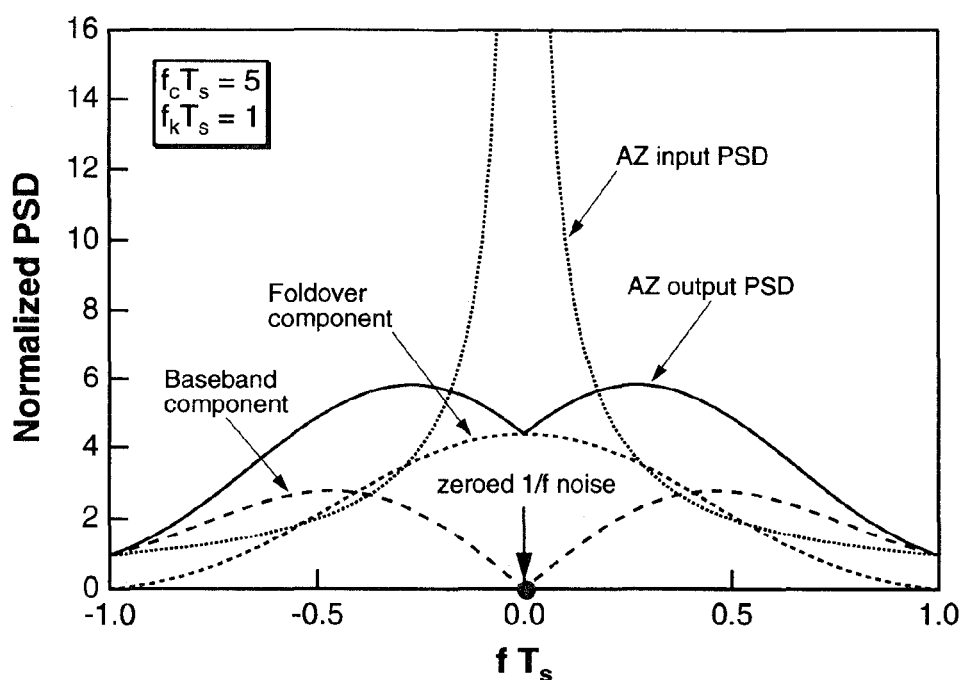


Fig. 6. Effect of the AZ process on a first-order low-pass filtered $1/f$ noise having a bandwidth five times larger than the sampling frequency.

where the total foldover component is given by

$$S_{\text{fold}} = S_0 \left\{ (\pi f_c T_s - 1) + 2 f_k T_s \left[1 + \ln \left(\frac{2}{3} f_c T_s \right) \right] \right\} \cdot \text{sinc}^2(\pi f T_s). \quad (15)$$

The corner frequency for which the $1/f$ noise foldover component [given by (13)] is equal to the foldover component coming from the white noise [as given by (8)] is plotted against the normalized white-noise bandwidth in Fig. 7. The

total foldover term given by (15) is thus dominated by the $1/f$ noise contribution for parameter values $(f_k T_s, f_c T_s)$ falling in the region above this curve, while it is dominated by the broadband white noise contribution below the curve. For example, an amplifier autozeroed at 100 kHz and having a gain-bandwidth product equal to $7 \times f_s = 700$ kHz should have a corner frequency larger than $4.13 \times f_s = 413$ kHz for the $1/f$ noise foldover to dominate.

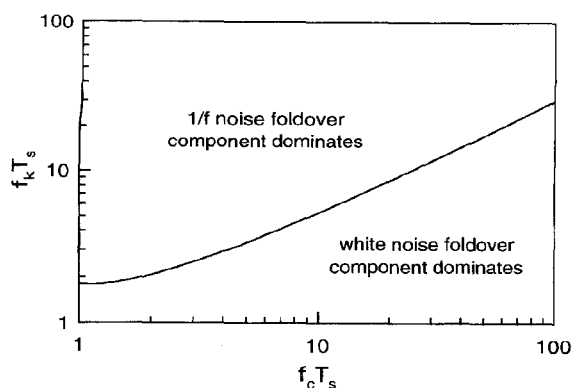


Fig. 7. Comparison between the $1/f$ and white noise contribution to the total foldover component as a function of the white-noise bandwidth.

This demonstrates that in most practical cases the foldover component is dominated by the broadband white noise.

In conclusion, it was shown in this section that the AZ process not only cancels the amplifier's offset, but it also strongly reduces the amplifier $1/f$ noise thanks to the double zero introduced by the AZ baseband power transfer function. This improvement is obtained at the cost of an increased white noise foldover component due to the aliasing of the amplifier's thermal and as well as $1/f$ noise. In most practical cases, this foldover term is dominated by the aliased thermal noise component, which is approximately equal to the amplifier's original broadband thermal noise multiplied by the ratio of the equivalent noise bandwidth to the Nyquist frequency.

C. Residual Offset

Next, the effectiveness of the stages of Fig. 1 in eliminating the effects of V_{os} will be discussed. Since the additional input used in the amplifiers of Fig. 1 for nulling the offset can either be a voltage or a current, it will generally be denoted as a control variable x_c . Changing this input when the amplifier is in the sampling phase, as shown in Fig. 1, allows the zeroing of the output voltage for a particular value of the control variable.

Let the input-referred offset V_{ios} be defined as the output voltage during the offset sampling phase divided by the differential gain of the amplifier in the amplification mode. The relation between this input-referred offset and the control variable is schematically plotted in Fig. 8, and is first assumed to be linear (see the continuous straight line in Fig. 8). Assume that the amplifier has an initial offset as shown in Fig. 8(a). The appropriate feedback configuration or the dedicated algorithm will have to bring this offset very close to zero. When the loop has settled or the algorithm is completed, the control information is stored. During the storage process, there might be some error Δx_c introduced into the control variable, due for example to charge injection by the sampling switch, or to the quantization error of the A/D converter, that leads to a residual offset $V_{ios-lin}$ or V_{ios-nl} depending if the compensation characteristic is linear or not. It is important to notice that the characteristics

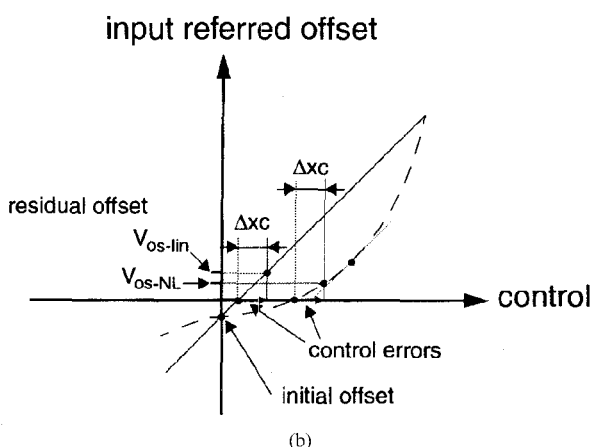
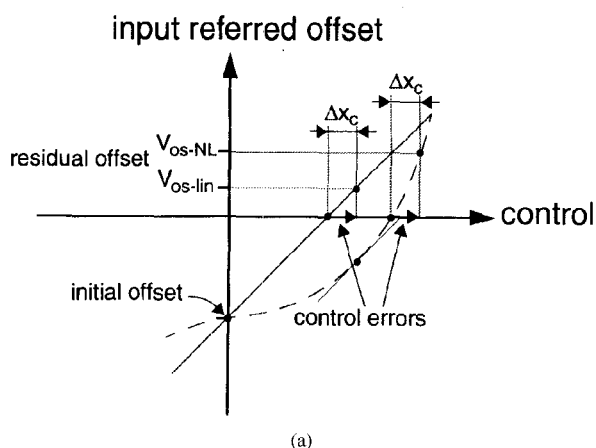


Fig. 8. Input-referred offset versus nulling control variable: (a) large initial offset and (b) small initial offset.

between the control variable and the input-referred offset voltage is not required to be linear. An example of a nonlinear characteristic is illustrated in broken lines in Fig. 8(a) and (b). Let ΔV be defined as the difference between the initial offset and the offset corresponding to the point where the incremental gain on the nonlinear characteristic equals the slope of the linear characteristic. The resulting residual offsets of the linear ($V_{ios-lin}$) and the nonlinear (V_{ios-nl}) characteristics resulting from equal control errors Δx_c are compared in Fig. 8(a) for an initial offset larger than ΔV . The residual error of the nonlinear characteristic is obviously larger. On the other hand, if the initial offset is already small compared to ΔV [Fig. 8(b)], the residual offset of the nonlinear characteristic becomes smaller. A nonlinear offset-nulling characteristic can thus potentially reduce the sensitivity to control errors and hence reduce the residual offset. But this only happens if the initial offset is already small. The choice between a linear or a nonlinear control characteristic depends on the anticipated initial offset reduction strategy and the test methodology.

D. Correlated Double Sampling

In the AZ principle described in Fig. 1, the amplifier has to be disconnected from the signal path during phase ϕ_1 in

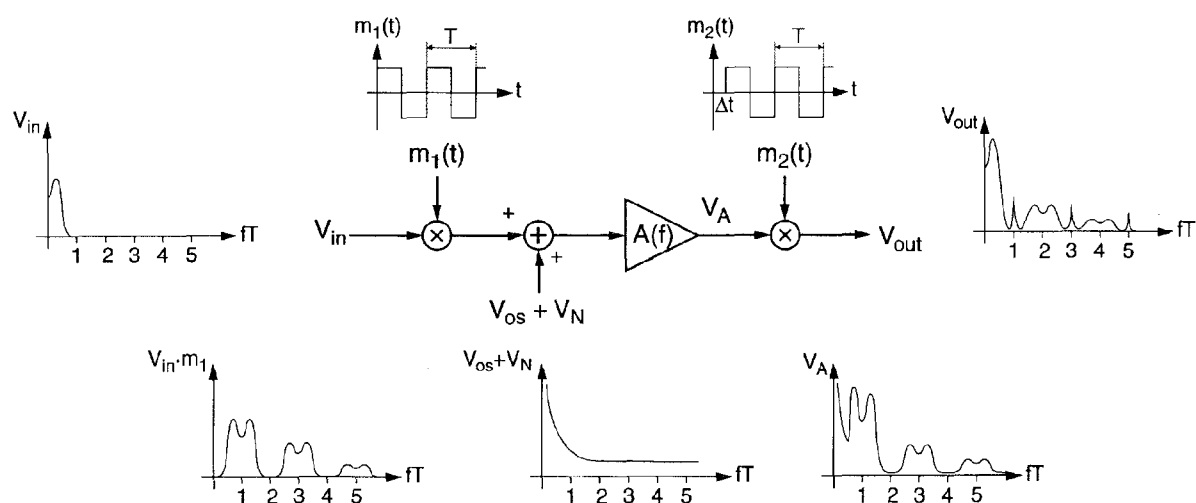


Fig. 9. The chopper amplification principle [19].

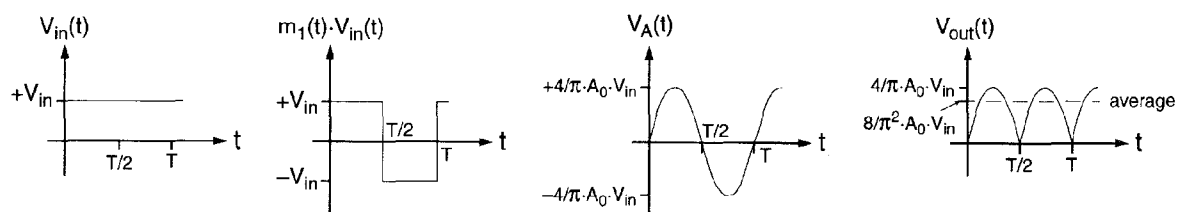


Fig. 10. Waveforms appearing along the chopper amplifier for a dc input and an amplifier bandwidth limited to twice the chopper frequency.

order to S/H its own offset and noise. It is therefore only available for amplification during phase ϕ_2 . Although this may be incompatible with continuous-time applications, it is well suited to sampled-data systems such as SC circuits where all the signals are sampled at the end of a phase and held during the complementary time interval. The amplifier can then be autozeroed while the voltages are held and connected back for amplification when needed [20]. After the AZ phase, the output of the amplifier is then sampled again by the next stage (SC integrator or SC amplifier). There are thus two sampling operations: a first one to sample the amplifier noise and offset (AZ) followed by a second sampling of the signal and the instantaneous (or direct) noise of the amplifier in hold mode. Note that the AZ phase may require one additional phase [20].

The CDS technique which has originally been introduced to reduce the noise produced in charged-coupled devices (CCD's) [13], [14] can be described as an AZ operation followed by a S/H. It is widely used in sampled-data systems and particularly in SC circuits (see Section V).

Although the signal at the output of a circuit using CDS is now S/H, the effect of CDS on the amplifier offset and noise is very similar to that of the AZ process. The baseband transfer function $H_0(fT_s)$ still imposes a zero at the origin of frequency that cancels any offset and strongly reduces the $1/f$ noise in the same way the AZ technique does. On the other hand, although the transfer functions for $n \neq 0$ are different from those obtained for the AZ process, the

foldover component due to aliasing is comparable since the wideband noise has already been sampled once.

III. THE CHOPPER STABILIZATION TECHNIQUE

In this section, an alternative technique for the suppression of the low-frequency noise, called (for historic reasons) chopper stabilization (CHS), will be introduced. Its properties will be analyzed and compared with those of the AZ and CDS schemes.

A. Basic Principle

The CHS technique was introduced about 50 years ago to realize high-precision dc gains with ac-coupled amplifiers. These were originally constructed using vacuum tubes and mechanical relay choppers. When solid-state components became available, they were then made with modular and hybrid techniques. Now they can easily be realized on-chip by taking advantage of integrated switches.

Unlike the AZ process, the CHS technique does not use sampling, but rather applies modulation to transpose the signal to a higher frequency where there is no $1/f$ noise, and then demodulates it back to the baseband after amplification. The chopper amplification principle is illustrated in Fig. 9.

Suppose that the input signal has a spectrum limited to half of the chopper frequency so no signal aliasing occurs, and that the amplifier is ideal, with no noise or offset. This

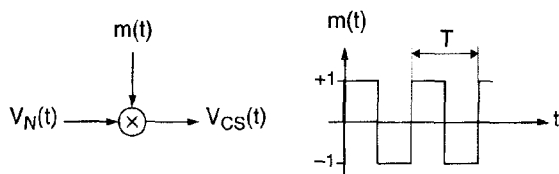


Fig. 11. Chopper modulation.

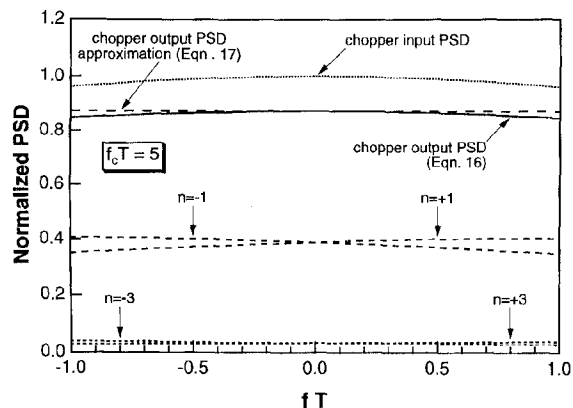


Fig. 12. Chopper output PSD for a first-order low-pass filtered white noise.

input signal is multiplied by the square-wave carrier signal $m_1(t)$ with period $T = 1/f_{\text{chop}}$. After this modulation, the signal is transposed to the odd harmonic frequencies of the modulation signal. It is then amplified and demodulated back to the original band. Assuming that the input of the chopper amplifier is a dc signal V_{in} , the signal at the output of the first chopper modulator is a square wave of period T and amplitude V_{in} . If the amplifier has a gain A_0 , an infinite bandwidth and does not introduce any delay, the signal at its output is simply the same square wave with an amplitude $A_0 \cdot V_{in}$ and the signal after demodulation is again a dc signal of value $A_0 \cdot V_{in}$. To illustrate a less ideal solution, assume now that the amplifier has a constant gain A_0 up to twice the chopper frequency and is zero otherwise (ideal low-pass). As shown in Fig. 10, the amplifier output signal $V_A(t)$ is now a sinewave corresponding to the fundamental component of the chopped dc signal with an amplitude $(4/\pi)(A_0 \cdot V_{in})$. The output of the second modulator is then a rectified sinewave containing even-order harmonic frequencies components. The dc value after low-pass filtering is $(8/\pi^2)(A_0 \cdot V_{in})$, corresponding to an equivalent dc gain of $(8/\pi^2) \cdot A_0 \cong 0.8 \cdot A_0$. This example shows that the finite bandwidth of the amplifier introduces some spectral components around the even harmonics of the chopper frequency which have to be low-pass filtered to recover the amplified signal. The gain of the chopper amplifier is also sensitive to the delay introduced by the main amplifier. Assume again that the input is a dc signal V_{in} and that the amplifier has an infinite bandwidth but introduces a constant delay, say of a quarter of a period $T/4$. If the input and output modulators are in phase, the output signal is a chopped cosine wave, without a dc

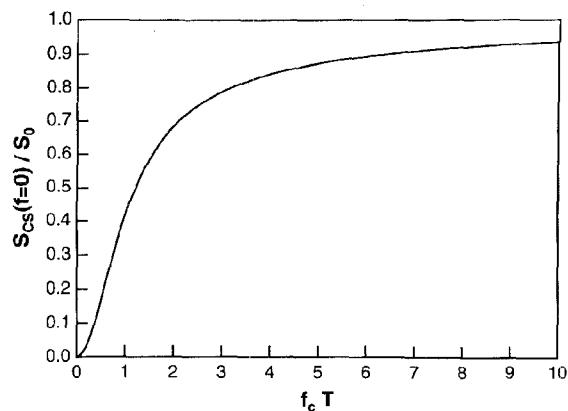


Fig. 13. Chopper modulated white noise at zero frequency as a function of the original white noise bandwidth.

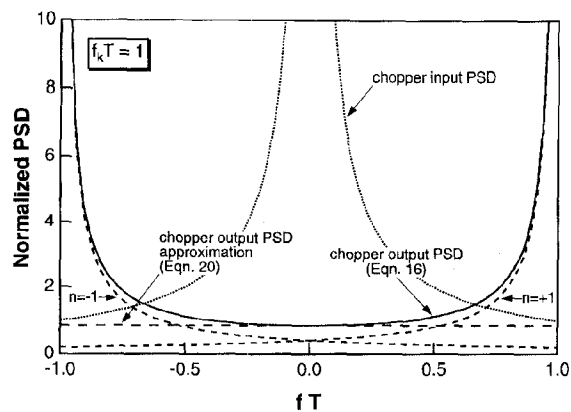


Fig. 14. Chopper output PSD for a $1/f$ noise.

component and containing only odd harmonics. This means that the dc gain of the overall chopper amplifier is zero. If the same constant delay is introduced between the input and the output modulators, the output signal is again a rectified sine wave. This shows that in order to maintain a maximum dc gain, the phase shift between the input and the output modulators has to match precisely the phase shift introduced by the amplifier.

Since the noise and offset are modulated only once, they are transposed to the odd harmonics of the output chopping square wave, leaving the amplifier ideally without any offset and low-frequency noise.

B. The Effect of Chopping on the Amplifier Noise

The effect of the chopper modulation on the amplifier noise can be analyzed from Fig. 11 where $V_N(t)$ is the noise and $m(t)$ the carrier signal.

The bilateral PSD of the chopped output signal $V_{CS}(t)$ is given by

$$S_{CS}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n \text{ odd}}}^{+\infty} \frac{1}{n^2} S_N\left(f - \frac{n}{T}\right). \quad (16)$$

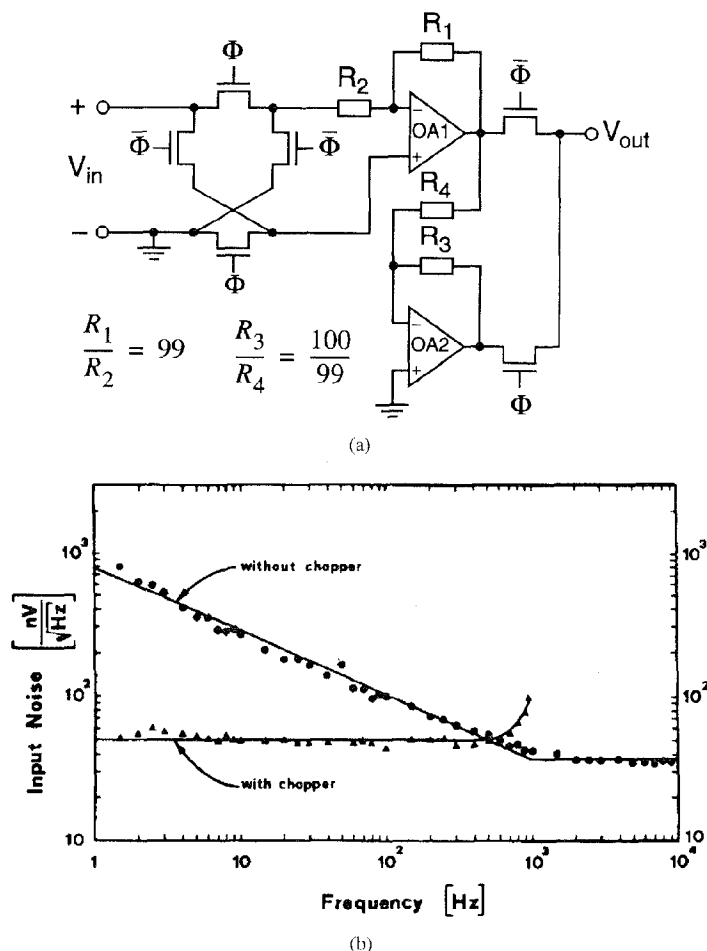


Fig. 15. Experimental chopper amplifier. (a) Experimental chopper amplifier schematic. The chopper frequency has been set to the amplifier corner frequency $f_{chop} = f_k = 1$ kHz. (OA1 and OA2 are, respectively, a CA3420 and μ A 741 and the switches are MC14016.) (b) Measured input referred PSD without and with the chopper.

The output PSD, resulting from the summation of the replicas of the original spectrum shifted to the odd harmonics of the chopper frequency, is plotted in Fig. 12 for $n = 1, -1, 3, -3$ and for an amplifier cut-off frequency f_c equal to five times the chopper frequency $1/T$. It can be approximated in the baseband ($|fT| \leq 0.5$) by a white noise PSD

$$S_{CS-white}(f) \cong S_{CS-white}(f = 0) = S_0 \left[1 - \frac{\tanh\left(\frac{\pi}{2} f_c T\right)}{\frac{\pi}{2} f_c T} \right] \quad (17)$$

which for $f_c T \gg 1$ which can further be approximated by

$$S_{CS-white}(f) \cong S_0 \quad \text{for } |fT| \leq 0.5 \text{ and } f_c T \gg 1. \quad (18)$$

Unlike the AZ technique, the chopper modulation does not introduce aliasing of the broadband noise, which for AZ

causes the PSD in the baseband to increase proportionally with the ratio of the noise bandwidth and the sampling frequency. As shown by (17), the baseband PSD resulting from the chopper modulation is nearly constant (white noise), and it tends to the value of the input white noise S_0 for a large $f_c T$. This is due to the fact that the noise is not sampled nor held, just periodically inverted without changing the general properties of the noise in the time domain. Although the chopper modulator output PSD results from a summation as for the S/H process, in the chopper modulation the replicas are multiplied by $1/n^2$, making their contribution to the baseband decrease very rapidly.

The PSD given in (17) is plotted in Fig. 13 against the white-noise bandwidth normalized to the chopper frequency. It shows that the chopper-modulated PSD is always smaller than the PSD of the original white noise, and tends asymptotically to it for very large cutoff to chopper frequency ratios. It becomes equal to 90% of the original spectrum for $f_c T$ slightly larger than six.

The effect of the chopper modulation on the $1/f$ noise can also be analyzed using (16), assuming a cutoff fre-

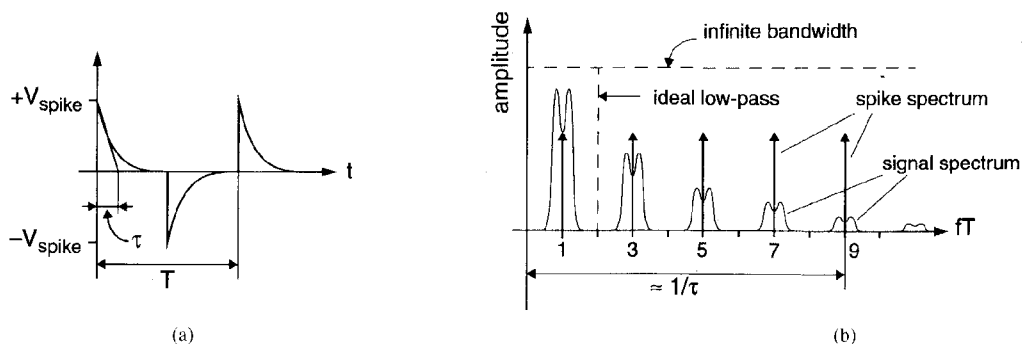


Fig. 16. Spike signal appearing at the input of the amplifier and causing residual offset. (a) Spike signal at the amplifier input and (b) spike signal and chopper modulated signal spectra with amplifier bandwidth characteristics.

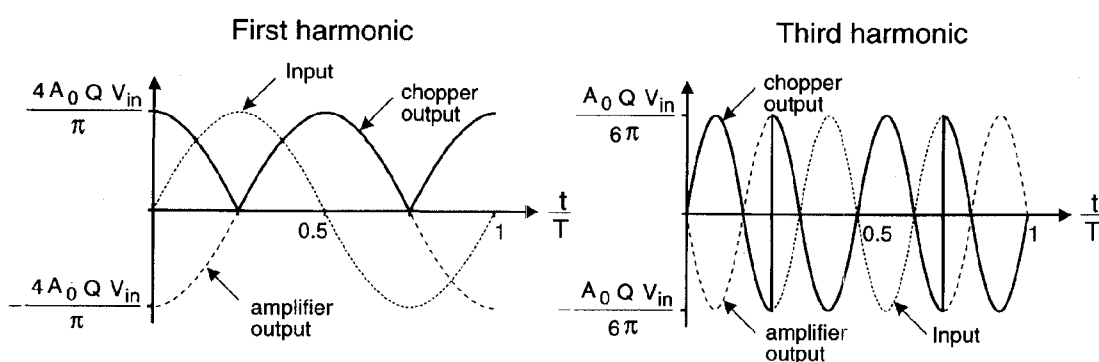


Fig. 17. Effect of the phase shift introduced by a second-order low-pass selective amplifier on the first and third harmonics.

quency much larger than the chopper frequency and an input PSD given by

$$S_{N-1/f}(f) = S_0 \frac{f_k}{|f|} = S_0 \frac{f_k T}{|fT|}. \quad (19)$$

The result of the summation is plotted in Fig. 14, which clearly shows that the $1/f$ noise pole has disappeared from the baseband since it has been transposed to $\pm 1/T$ and to the odd harmonics of the chopper frequency. It also shows that the chopped $1/f$ noise PSD can be approximated in the baseband by a white noise component

$$S_{CS-1/f}(f) \cong 0.8525 S_0 f_k T. \quad (20)$$

The total residual noise in the baseband for a typical amplifier input referred noise given by (6) can be obtained by adding (18) and (20), resulting in

$$S_{CS}(f) \cong S_0(1 + 0.8525 f_k T) \quad \text{for } |fT| \leq 0.5 \text{ and } f_c T \gg 1. \quad (21)$$

According to (21), a good compromise is obtained by choosing the chopper frequency equal to the amplifier corner frequency. The resulting white noise PSD increase is then less than 6 dB. Equation (21) has been verified experimentally on a breadboard circuit. The schematic is presented in Fig. 15(a), and the measured input referred noise PSD with and without the chopper is shown in Fig. 15(b). The chopper frequency was set equal to the

amplifier corner frequency at $1/T = f_k = 1$ kHz. The white noise component of the amplifier without the chopper was estimated to be $37 \text{ nV}/\sqrt{\text{Hz}}$, and the theoretical white noise of the amplifier with the chopper active as calculated from (21) was $50.4 \text{ nV}/\sqrt{\text{Hz}}$ which is very close to the measured result shown in Fig. 15(b).

C. Residual Offset

Residual offset is mainly due to the nonidealities of the chopper modulators and more specifically of the input modulator. If the modulators are realized with simple MOS switches, these nonidealities will include clock feedthrough and charge injection (see Section IV-A for a discussion of these and other nonideal effects). More generally, any spikes caused by the modulator nonidealities and appearing at the amplifier input will be amplified and demodulated by the output modulator, giving rise to a residual dc component. Since only the odd harmonics of the chopper frequency will contribute to the residual offset, the positive and negative spikes will have an odd symmetry (Fig. 16).

Since the time constant τ of these parasitic spikes is generally much smaller than the half chopper period $T/2$, most of the spike energy appears at frequencies higher than the chopper frequency. The spectra of the signal resulting from such spikes and of a chopper-modulated signal at the amplifier input are shown in Fig. 16(b). Since the spectral envelope is inversely proportional to frequency, the output

signal after amplification and demodulation is essentially reconstructed by the fundamental component. Using an amplifier with a bandwidth much larger than the chopper frequency results in a maximum gain approximately equal to the dc gain of the amplifier A_0 , but also leads to a maximum output offset voltage, since almost all the spectral component of the spike signal will contribute. The input referred offset can be calculated assuming that $\tau \ll T/2$ [8], [12]:

$$V_{os} \cong \frac{2\tau}{T} V_{\text{spike}} \quad (22)$$

where V_{spike} is the amplitude of the spikes at the chopper amplifier input as shown in Fig. 16(a). Keeping the same gain A_0 in the passband, but limiting the bandwidth to twice the chopper frequency slightly lowers the overall dc gain to $(8/\pi^2)A_0 = 0.81A_0$, but greatly reduces the offset voltage referred to the input. The new value is

$$V_{os} \cong \left(\frac{2\tau}{T}\right)^2 V_{\text{spike}} \quad (23)$$

which is much smaller than that given by (22), since τ has been assumed to be much smaller than $T/2$. Therefore, the offset can be reduced drastically, without losing too much signal gain, by limiting the amplifier bandwidth to twice the chopper frequency. It can be shown that (23) also holds for a second-order low-pass or band-pass selective amplifier with its resonance frequency locked to the chopper frequency. This is essentially due to the phase characteristic of the selective amplifier. As illustrated in Fig. 17, for a constant input signal V_{in} and a low-pass selective amplifier, the fundamental component is delayed by a quarter of a period while all the harmonics are delayed by half a period, making their mean values equal to zero after demodulation. Since the offset is not further reduced by using higher-order selective filtering characteristics, the second-order selective amplifier is the best trade-off between circuit complexity and residual offset. Note that the band-pass selective amplifier is the simplest since it does not require any delay between the input and output chopper signals.

IV. PRACTICAL IMPLEMENTATION ISSUES

A. Nonideal Effects in Switches

The S/H circuit as well as the chopper modulator are most often realized using MOS switches. The MOS switch nonidealities include a nonzero and nonlinear on-resistance. However, the most important factors affecting residual offset are the following:

- clock feedthrough;
- channel charge injection;
- sampled noise;
- leakage current.

Clock feedthrough and channel-charge injection will be considered first.

Each time a switch is turned off, the charges in its conducting channel are released and removed through the

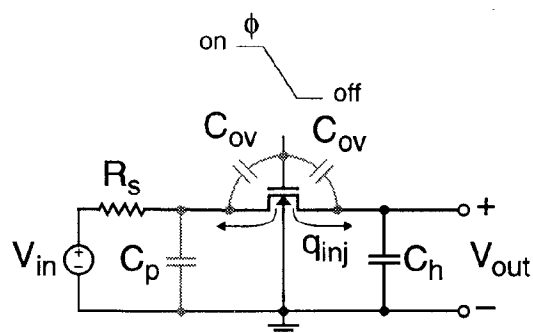


Fig. 18. Basic S/H circuit.

MOS source and drain terminals (the fraction of charges that flows to the substrate can generally be neglected). The partitioning of these charges between the source and drain depends mainly on the ratio of the total capacitance C_h at the switch drain (the hold capacitor) and at the source (C_p , corresponding to the total parasitic capacitance) and on the so called “switching parameter” [2] determined mainly by the transistor’s “on” resistance R_{on} and the slope of the clock signal applied to the gate. The channel charge is split equally between source and drain only if either the capacitances C_p and C_h are equal (independent of the switching time), or if the switching transition time is much less than the $R_{on}C$ time constant (independent of C_p/C_h). In general, for slowly falling clock signals, the channel charge is divided unequally between source and drain, going mostly to the terminal showing the lower impedance. In the case where the source or drain capacitance is much larger than the other, most of the charge flows to the larger capacitance. The charge q_{inj} injected into the hold capacitor is thus difficult to predict accurately. There are, however, circuit techniques which can reduce the effect of charge injection. The simplest one uses complementary switches in such a way that the charges released by one switch are absorbed by the complementary device building its channel. This technique is rather inefficient, since the matching between the channel charges of the n-MOS and the p-MOS devices is poor and signal dependent. This charge mismatch is further degraded by phase jitter between the two complementary clocks. Other more efficient strategies include:

- 1) making capacitance C_p much larger than C_h (by adding an extra capacitor) and choosing a switching parameter much smaller than one (by choosing a slow clock transition) in order to attract most of the channel charge to C_p , reducing q_{inj} almost to zero [Fig. 19(a)]. This technique of course sets a limit on the maximum clock frequency. Furthermore, the charge flow due to the overlap capacitance C_{ov} is still present;
- 2) making C_p equal to C_h to force the channel charge to split equally between source and drain, and then compensating the injected charge by adding half-size dummy switches [Fig. 19(b)];

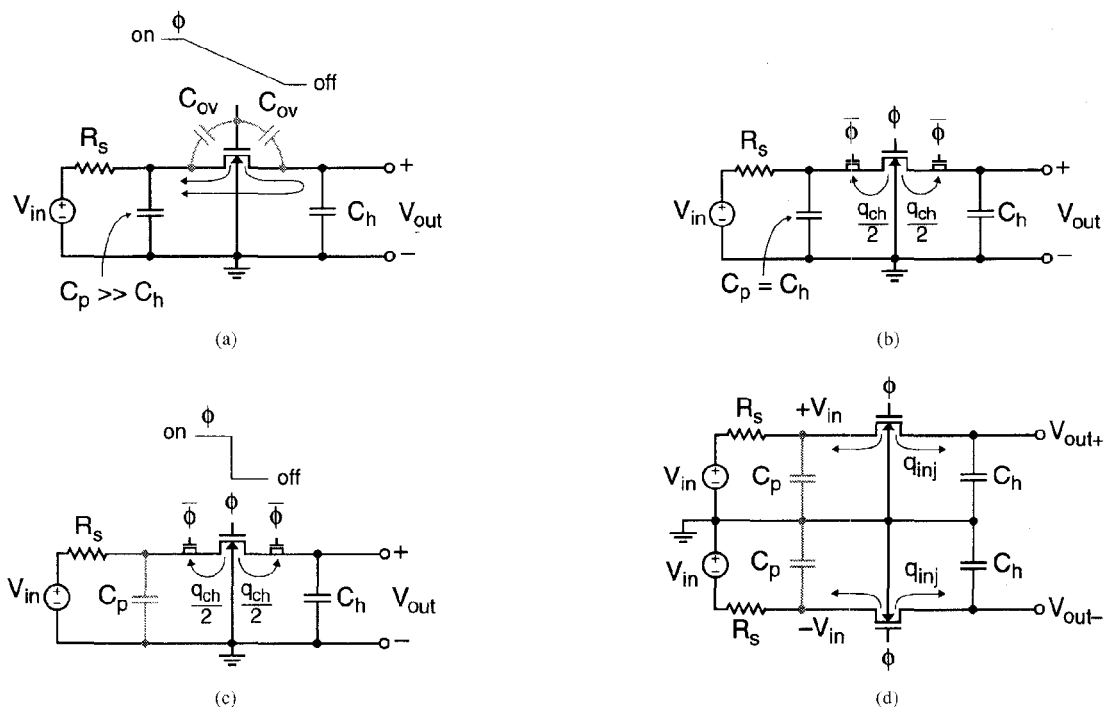


Fig. 19. First-order charge injection cancellation techniques: (a) large shunt capacitor and slow clock transition time, (b) symmetrical capacitances ($C_p = C_h$) with half-sized dummy switches, (c) short clock transition time with half-sized dummy switches, and (d) fully differential structure.

- 3) using a very short transition time to force the channel charge to split equally between source and drain and then compensating the injected charge by half-sized dummy switches [Fig. 19(c)];
- 4) using a fully differential structure. If the injected charges to the differential capacitors are matched, the resulting voltage appears as a common-mode voltage and is therefore rejected [Fig. 19(d)]. This usually requires the generation of delayed-cutoff clock phases.

It should be noted that none of the previous described techniques offers a perfect charge-injection cancellation. Furthermore, the efficiency of the half-sized dummy transistor technique depends on a proper layout in order to insure a good matching and a first-order insensitivity to doping gradient. The technique which usually offers the best results is a combination of a fully differential structure and the half-sized dummy transistor technique described in 3) and 4).

It is also important to notice that the simulation of the charge injection effect at the transistor level using a circuit simulator such as SPICE often does not yield accurate results. This is mainly due to the problem of inaccurate charge conservation inherent to such simulators, combined with an incorrect modeling of the MOS transistor's intrinsic charges and of the partitioning of the channel charge between source and drain [37]–[43]. A clear discussion of charge conservation in MOSFET models and SPICE is given in [43].

Each time the switch of Fig. 18 is opened, an additional error charge due to the thermal noise of the switch channel

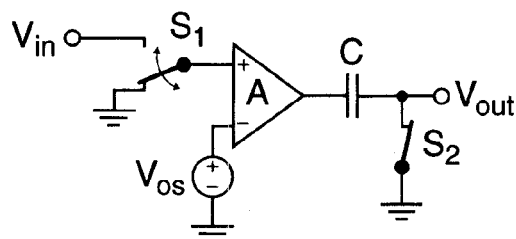


Fig. 20. Open-loop offset cancellation technique.

will be sampled on the hold capacitor C_h . The variance of this noise charge is equal to kTC_h [1], [2], corresponding to a sampled noise voltage variance equal to kT/C_h .

For very long hold time and/or for high-temperature operation [35], the leakage current I_{leak} associated with the drain-to-bulk junctions also has to be taken into account, since it will discharge the hold capacitor and thus introduce an additional error into the sampled voltage.

The total error ΔV in the sampled voltage across the hold capacitor due to clock feedthrough, charge injection, sampled noise and leakage current is given by

$$\Delta V = \alpha \frac{C_{ov}}{C_{ov} + C_h} V_{swing} + \frac{q_{inj}}{C_h} + \sqrt{\frac{kT}{C_h}} + \frac{I_{leak} T_h}{C_h} \quad (24)$$

where V_{swing} is the swing of the clock signal and I_{leak} the leakage current of the drain-to-bulk diodes at the operating temperature. The attenuation factor $\alpha < 1$ accounts for the part of the total charge $C_{ov} V_{swing}$ coming from the overlap capacitor and flowing to ground instead of the hold

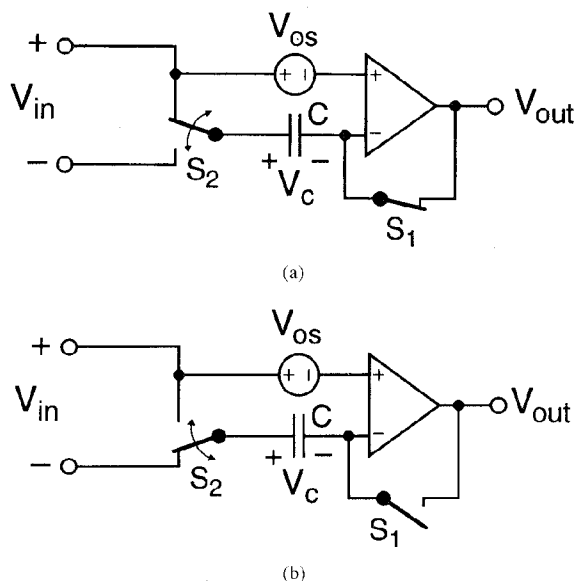


Fig. 21. Closed-loop-amplifier offset cancellation principle: (a) offset sampling phase (AZ) and (b) amplification phase.

capacitor. It is important to notice that all contributions appearing in (24) decrease if a larger hold capacitor is used. Since in most practical cases the second term of (24) dominates, the voltage change ΔV will be replaced by q_{inj}/C_h in the following discussions.

B. The Open-Loop Offset Cancellation Principle

The simplest way to implement offset cancellation is to sample the offset at the output of the amplifier as shown in Fig. 20. This technique is sometimes called output offset storage (OOS) [2], [6], [33]. During the AZ phase, the input switch S_1 and the output switch S_2 are both connected to ground. Switch S_2 is then opened and the offset voltage V_{os} multiplied by the amplifier gain A remains stored on capacitor C . This stored output voltage is altered by an error voltage q_{inj}/C caused by the charge injection occurring at the opening of switch S_2 . After the AZ phase, the input terminal of the amplifier is connected back to the signal by switch S_1 . The input-referred residual offset is thus limited by the charge injection q_{inj} (or charge injection mismatch Δq_{inj} in the case of a differential implementation)

$$V_{os-res} = \frac{1}{A} \frac{q_{inj}}{C}. \quad (25)$$

This technique is obviously effective only if the amplifier does not saturate during the offset-sampling phase. This requires that the output-referred offset remain smaller than the minimum saturation voltage. This is possible only if the amplifier gain is relatively small (typically, less than ten), or if C and S_2 follow the first stage of the amplifier.

C. The Closed-Loop Offset Cancellation Principle

The open-loop offset cancellation principle is not well suited to high-gain amplifiers. It is usually preferable there

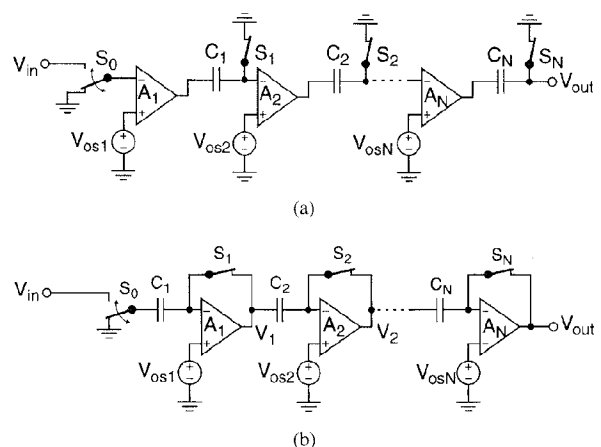


Fig. 22. Multistage offset cancellation principles.

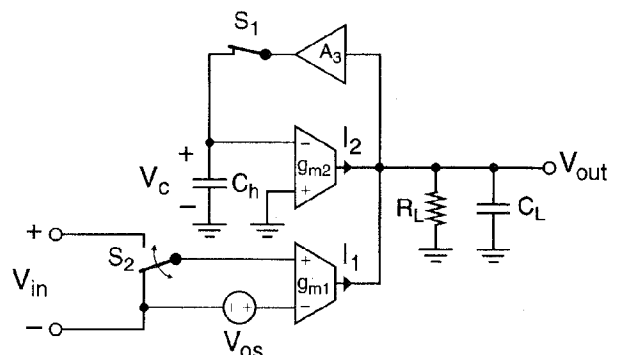


Fig. 23. Offset compensation using an additional offset nulling input.

to sense the amplifier's offset in a closed-loop configuration as shown in Fig. 21.

During the sampling phase, the amplifier is disconnected from the signal path and connected in a unity-gain configuration as shown in Fig. 21(a). Assuming that the open-loop gain A of the amplifier is much larger than one, the voltage V_c obtained across the storage capacitor C after the amplifier has settled is almost equal to its offset voltage V_{os}

$$V_c - \frac{A}{1+A} V_{os} \cong V_{os}. \quad (26)$$

This voltage (plus an additional error q_{inj}/C caused by the charge injection occurring when switch S_1 opens) is stored across capacitor C . The charge will remain trapped on capacitor C since the input current of the amplifier is zero for a MOS input stage, and hence capacitor C behaves like a floating voltage source equal to V_{os} plus the charge-injection error. After this sampling phase, the offset-compensated stage is available for amplification and is connected again to the signal path. The residual offset can then be found

$$V_{os-res} = V_{os} - V_c \cong \frac{V_{os}}{A} + \frac{q_{inj}}{C}. \quad (27)$$

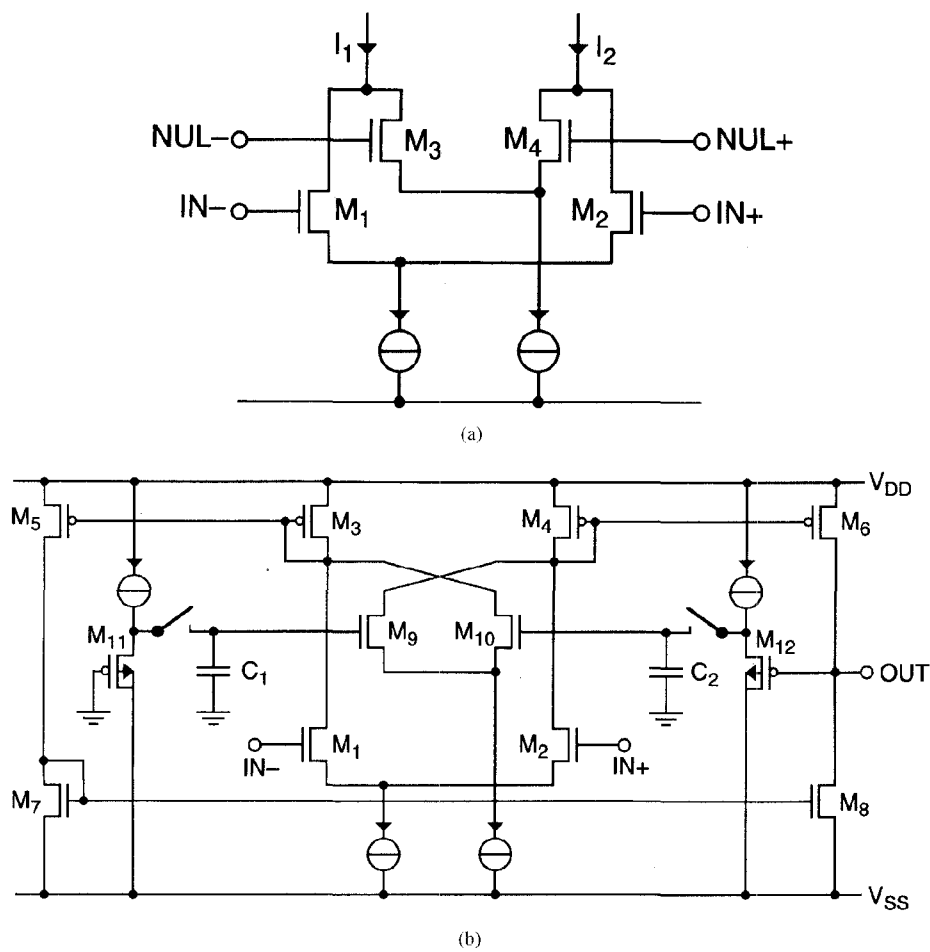


Fig. 24. Realization of the nulling input port using an additional differential pair connected in parallel with the main pair: (a) principle and (b) complete AZ scheme.

It is thus nearly equal to the original offset divided by the amplifier dc gain, and is ultimately limited by the charge-injection term q_{inj}/C . The latter could be reduced to a mismatch error of charge injections if a fully differential configuration is used.

The amplifier is in general connected in a closed-loop configuration for amplification, and in an open-loop configuration when it is used as a comparator.

In the scheme described above, the amplifier is not available to the external circuitry during the offset sampling phase. This is not a major drawback for most applications. In case continuous-time amplification is required, the offset-free amplifier can be duplicated and used in a time-shared ("ping-pong") operation [25], [26], or the continuous-time feedforward technique discussed below in Section IV-F may be used [22], [35], [36].

D. Multistage Offset Storage

If high gain and speed is required, several single-stage amplifiers can be cascaded as shown in Fig. 22 [33], [50]. The circuit of Fig. 22(a) operates as follows. In the offset sampling phase (shown in Fig. 22), the negative inputs of all the amplifiers are connected to ground. Switch S_1 is

then opened first, causing some charge to be injected into capacitor C_1 , which results in an error voltage appearing at the negative input of the second amplifier. This error voltage can be viewed as a change in the input-referred offset voltage of the second amplifier and will thus be cancelled along with V_{os2} . Subsequently, switches $S_2, S_3, \dots, S_N$ are opened successively, so that the only offset voltage affecting the output is due to the charge injection of switch S_N into capacitor C_N . Since the total gain is equal to the product of the individual gains, the equivalent input-referred offset is

$$V_{os-rcs} = \frac{1}{A_1 A_2 \cdots A_N} \cdot \frac{q_{inj-N}}{C_N} \quad (28)$$

which is obviously much lower than that obtained for a single-stage low-gain amplifier.

The circuit of Fig. 22(b) operates in a similar way. When switch S_1 opens, charge is injected onto capacitor C_1 resulting in an output voltage V_1 for the first amplifier equal to $V_{os1} + A_1 q_{inj1}/C_1$ for $A_1 \gg 1$. When switch S_2 opens, the sum of V_1 , the offset voltage of the second amplifier V_{os2} and the charge injection voltage q_{inj2}/C_2 of switch S_2 is stored on capacitor C_2 . The output voltage

of the second amplifier when both switches S_1 and S_2 are opened sequentially is thus independent of the voltage V_1 and is simply equal to for $V_{os2} + A_2 q_{inj2}/C_2$ for $A_2 \gg 1$. This means that neither the offset nor the charge-injection errors propagate along the amplifier chain. The output offset is therefore affected only by the last stage, and equals $V_{osN} + A_N q_{injN}/C_N$. Hence, the equivalent input-referred offset is given by

$$V_{os-res} \cong \frac{V_{osN} + A_N \cdot \frac{q_{injN}}{C_N}}{A_1 A_2 \cdots A_N} \quad (29)$$

which is again much lower than the offset obtained for a single-stage low-gain amplifier.

High-gain and high-precision amplifiers or comparators can thus be realized simply by cascading low-gain stages and performing an input or output offset cancellation. If the switches are opened sequentially, the output offset is only determined by the last stage. The equivalent input-referred offset can thus be made extremely small. It should be noticed that this is true only if the delay between the edges of the clock pulses controlling switches S_1 to S_N is long enough to allow complete offset storage on the capacitors [6]. Note also that using a cascade of low-gain stages in a feedback amplifier may lead to stability problems.

E. Closed-Loop Offset Compensation Using an Auxiliary Input Port

The charge injection term appearing in (27) can be drastically reduced by storing the offset voltage at some intermediate node instead of at the amplifier input. The basic principle is that the gain A_1 from the signal input to the output is now higher than the gain A_2 from the nulling input to the output. The voltage change at the nulling input due to charge injection is therefore divided by the ratio A_1/A_2 which can be set much larger than one. The compensation is often realized using transconductance stages as shown in Fig. 23. Amplifier A_3 has been added to avoid loading the main amplifier with the hold capacitor C_h and therefore slowing down the AZ process. This allows the reduction of the effects of charge injected by switch S_1 and of the kT/C_h sampled noise by using a large hold capacitor C_h . It can also increase the compensation loop gain and therefore reduce the residual offset, as will be shown hereafter. In the case a compensation loop gain $g_{m2}R_L$ is sufficient, amplifier A_3 can be a simple voltage follower.

Assume that the input terminals of the main amplifier are short-circuited and that the compensation loop is still inactive (switch S_1 is open). The output voltage is zeroed if the current $I_2 = -g_{m2}V_c$ is equal to the current $-I_1 = g_{m1}V_{os}$, i.e., if the control voltage V_c is equal to $-(g_{m1}/g_{m2})V_{os}$. The ratio g_{m1}/g_{m2} should be chosen such that the control voltage V_c is much larger than the offset at the input of g_{m2} introduced by the nonidealities of the compensation loop containing transconductor g_{m2} and amplifier A_3 . On the other hand, the maximum value V_{c-max} of the control voltage before transconductor g_{m2} saturates should be

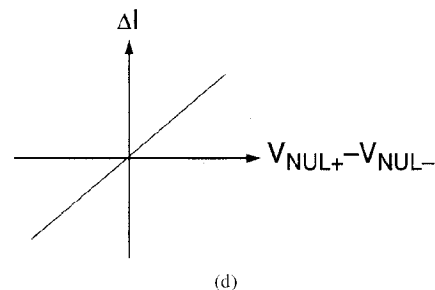
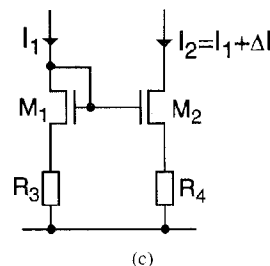
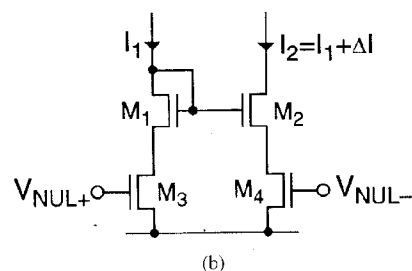
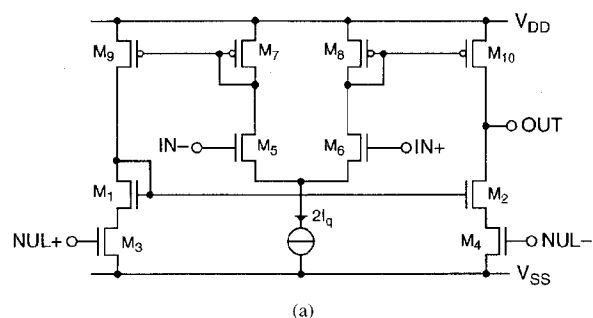


Fig. 25. Realization of the nulling input port using a degenerated current mirror: (a) principle, (b) adjustable current mirror, (c) equivalent schematic of (b), and (d) nulling current transfer characteristic.

chosen such that the maximum input offset voltage V_{os-max} can still be compensated. This sets the maximum value for the ratio g_{m1}/g_{m2} equal to $|V_{c-max}/V_{os-max}|$.

The control voltage V_c is developed during the AZ phase by sensing the output voltage in a closed-loop configuration (with switch S_1 closed). Defining $A_1 \equiv g_{m1}R_L$, the resulting output voltage is then equal to the initial offset $-A_1V_{os}$ at the output divided by the compensation loop gain (which is assumed to be much larger than one). The corresponding input-referred residual offset is given by

$$V_{os-res} \cong -\frac{V_{os}}{A_2 A_3} \quad (30)$$

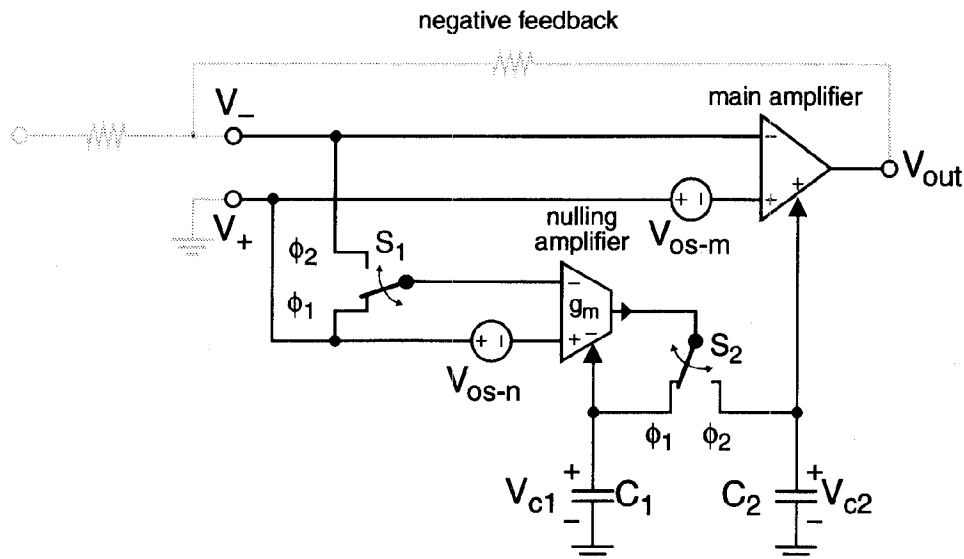


Fig. 26. Continuous-time AZ amplifier using feedforward technique.

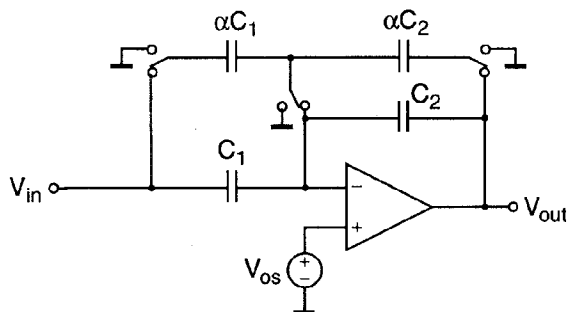


Fig. 27. Uncompensated SC voltage amplifier.

where $A_2 \equiv g_{m2}R_L$. The residual input-referred offset can thus be made small by choosing the loop gain A_2A_3 sufficiently large. Equation (30) ignores the charge injection occurring at the end of the AZ phase when switch S_1 opens. The input-referred residual offset voltage including charge injection of switch S_1 is given by

$$\begin{aligned} V_{os-res} &\cong -\frac{V_{os}}{A_2A_3} - \frac{A_2}{A_1} \frac{q_{inj}}{C_h} \\ &= -\frac{V_{os}}{A_2A_3} - \frac{g_{m2}}{g_{m1}} \frac{q_{inj}}{C_h}. \end{aligned} \quad (31)$$

As already mentioned, the first term of (31) can be made small by choosing a sufficiently large loop gain A_2A_3 , whereas the effect of charge injection is essentially determined by the ratio of the transconductances g_{m2}/g_{m1} . Assuming that the first term of (31) can be made negligible, the minimum value of ratio g_{m1}/g_{m2} should then be chosen such that the current at the output of transconductor g_{m2} due to charge injection remains smaller than the output current of transconductor g_{m1} produced by the maximum tolerated residual offset voltage:

$$g_{m2} \frac{q_{inj}}{C_h} < g_{m1} V_{os-res-max}. \quad (32)$$

The ratio g_{m1}/g_{m2} is thus limited by a lower bound set by the ratio of the voltage due to charge injection on C_h to the maximum acceptable residual offset. Its upper bound is determined by the ratio of the maximum admissible control voltage before the g_{m2} transconductor reaches saturation to the maximum initial offset to be compensated. Therefore, it must satisfy

$$\frac{\frac{q_{inj}}{C_h}}{V_{os-res-max}} < \frac{g_{m1}}{g_{m2}} < \frac{V_{c-max}}{V_{os-max}}. \quad (33)$$

The minimum value of A_2A_3 should be such that the maximum residual offset due to finite gain remains smaller than the charge injection contribution:

$$\frac{V_{os-max}}{A_2A_3} < \frac{A_2}{A_1} \frac{q_{inj}}{C_h} \quad (34)$$

leading to a condition on the gain A_2 :

$$A_2 > \sqrt{\frac{A_1 V_{os-max}}{A_3 \frac{q_{inj}}{C_h}}}. \quad (35)$$

There are several ways of realizing the additional nulling input port. Fig. 24(a) shows a possible implementation where an additional differential pair M_3-M_4 (corresponding to transconductor g_{m2} in Fig. 23) is connected in parallel with the main input pair M_1-M_2 (corresponding to transconductor g_{m1} in Fig. 23) [1], [2], [4], [24]. Connecting both main inputs together to the common-mode voltage (to ground), the offset voltage of the main differential pair M_1-M_2 will produce a difference in the drain currents of M_1 and M_2 . This offset current can then be cancelled by imposing the appropriate differential voltage on the nulling input, making the currents I_1 and I_2 equal. The complete AZ schematic is shown in Fig. 24(b), where two source followers $M_{11}-M_{12}$, two sampling switches and two hold

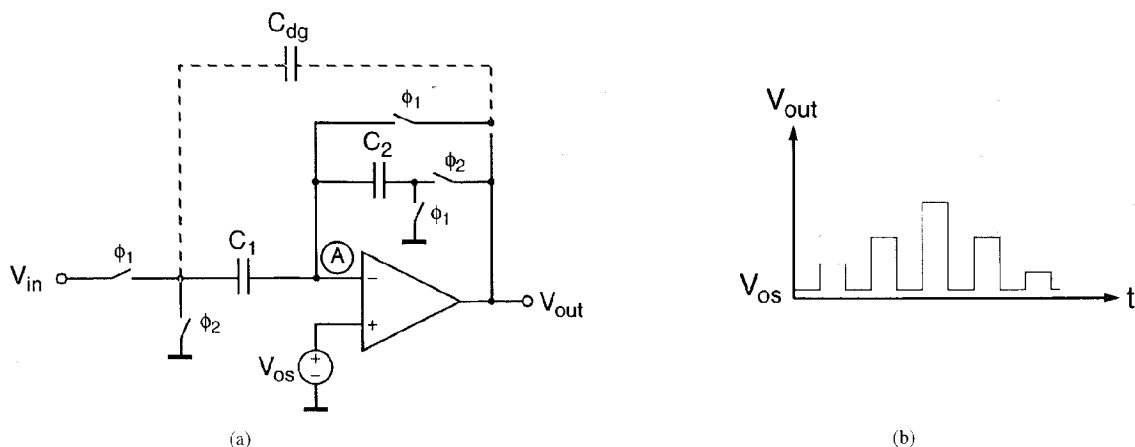


Fig. 28. Offset-compensated SC amplifier: (a) schematic and (b) output signal.

capacitors C_1 , C_2 have been added to perform the AZ operation [1], [2].

Another way of realizing the nulling input port is presented in Fig. 25. The adjustable current mirror M_1 – M_2 is degenerated by two transistors M_3 – M_4 operating in their linear regions and behaving as two resistors R_3 and R_4 controlled by voltages V_{NUL+} and V_{NUL-} , respectively [Fig. 25(b) and (c)]. Setting V_{NUL+} higher than V_{NUL-} implies that resistance R_4 becomes smaller than R_3 . For a given input current I_1 , the source voltage of M_2 is then smaller than that of M_1 resulting in an increase ΔI of the drain current of M_2 with respect to I_1 . The current increase ΔI is almost a linear function of the differential nulling voltage V_{NUL+} and V_{NUL-} as shown in Fig. 25(d). This simple scheme has been used in several applications [1]–[4], and [26]. Residual offset voltages as small as 200 μ V at a 3 V supply voltage have been reported [4].

F. Continuous-Time AZ Amplifiers

Some applications require continuous-time amplification and therefore the amplifier cannot be disconnected from the signal path in order to perform the AZ. This problem can be circumvented by duplicating the autozeroed amplifier and using one amplifier in its amplification mode while the other is being autozeroed. This time-sharing (“ping-pong”) technique has been successfully used and described in [25], [26]. Nevertheless, switching the two amplifiers can result in spikes appearing at the output. This can be avoided by using another technique originally presented in [22] and recently used [35]. This scheme also uses two amplifiers as shown in Fig. 26: a main amplifier which is never disconnected from the signal path and an autozeroed amplifier (nulling amplifier) controlling the nulling input of the main amplifier. The basic idea behind this circuit is to use a low-offset amplifier to sense the main amplifier’s offset and generate a correction voltage that is applied to the nulling input of the main amplifier to cancel its own offset. The nulling amplifier is autozeroed during phase ϕ_1 and its nulling voltage V_{c1} is stored on capacitor C_1 at the end of phase ϕ_1 and held during phase ϕ_2 . The

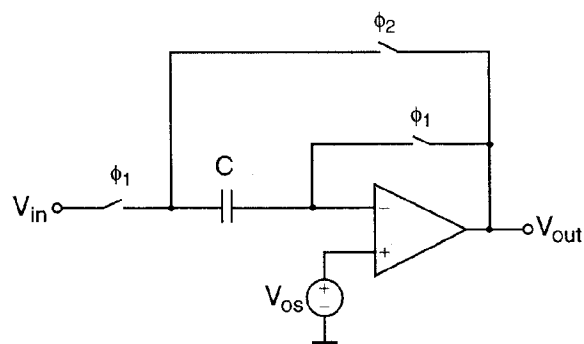


Fig. 29. A SC S/H stage.

nulling amplifier can therefore be considered as an almost offset-free amplifier that senses and zeroes the offset of the main amplifier during phase ϕ_2 . The main amplifier nulling information V_{c2} is then sampled and held on capacitor C_2 during phase ϕ_1 , while the nulling amplifier is zeroing its own offset. As shown in Fig. 26, this principle can only work if the overall amplifier is used with negative feedback in such a way that the voltage V_+ – V_- appearing between the positive and negative input terminals is almost equal to the main amplifier offset V_{os-m} . This principle has been used in the commercially available op-amp ICL7650S [36] (which has been misnamed Super Chopper-Stabilized Operational Amplifier although it does not use CHS but rather AZ). This op-amp features a typical offset as low as $\pm 0.7 \mu$ V at room temperature [36]. Note that C_1 and C_2 are very large (typically 100 nF) off-chip capacitors in this application.

We shall next discuss the operation of the circuit in detail. During phase ϕ_1 , corresponding to the state represented in Fig. 26, the nulling amplifier is disconnected from the signal path and is autozeroed. Its autocorrection voltage is then sampled on capacitor C_1 resulting in a control voltage V_{c1} across C_1 that is given by

$$\begin{aligned} V_{c1} &= -\frac{A_n}{1 + A'_n} V_{os-n} + \Delta V_{c1} \\ &\cong -\alpha_n V_{os-n} + \Delta V_{c1} \end{aligned} \quad (36)$$

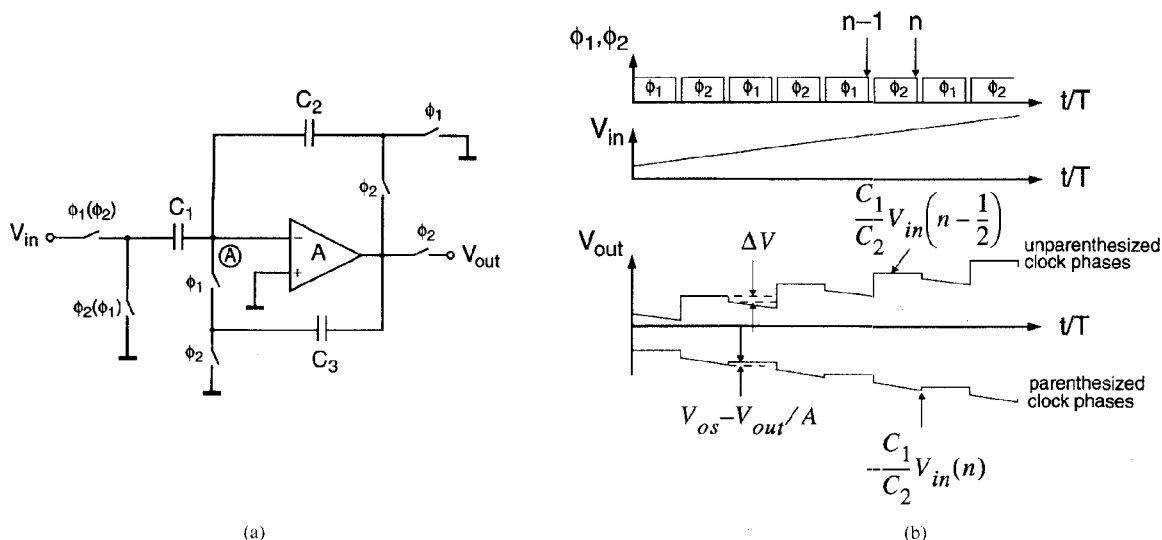


Fig. 30. Offset- and finite-gain compensated SC amplifier: (a) an offset and finite-gain compensated SC amplifier and (b) clock and signal waveforms.

where A_n is the gain of the nulling amplifier from its signal input, A'_n is its gain from the nulling input, and $\alpha_n = A_n/A'_n$. Voltage ΔV_{c1} corresponds to the voltage change due to charge injection, sampled noise, and leakage current. It is given by (24), where C_h is replaced by C_1 .

In the next phase ϕ_2 , the inverting input of the nulling amplifier is connected back to the signal and its output is switched to the nulling input of the main amplifier. The output voltage of the main amplifier is given by

$$V_{out} = A_m(V_+ - V_- - V_{os-m}) + A'_m V_{c2} \quad (37)$$

where A_m is the gain of the main amplifier from its signal input and $A'_m = A_m/\alpha_m$ is the gain from the nulling input. V_{c2} is the correction voltage applied to the nulling input which during phase ϕ_2 is given by

$$V_{c2} = A_n(V_+ - V_- - V_{os-n}) - A'_n V_{c1} \quad (38)$$

where it has been assumed that $A'_n \gg 1$. By definition of the residual offset voltage $V_{os(2)}$, imposing $V_+ - V_- = -V_{os(2)}$ during phase ϕ_2 will bring the output voltage to zero. Hence, the offset voltage $V_{os(2)}$ of the main amplifier during phase ϕ_2 is obtained by introducing the expression of V_{c2} given by (38) into (37), setting the output voltage to zero and solving for $V_+ - V_- = V_{os(2)}$ which results in

$$V_{os(2)} \cong \frac{\alpha_m V_{os-m} + \alpha_n V_{os-n}}{A_n} + \frac{\Delta V_{c1}}{\alpha_n}. \quad (39)$$

Here it was assumed that the gain $A_n A'_m$ from the input $(V_+ - V_-)$ through the nulling amplifier to the output (V_{out}) is much larger than the gain A_m of the main amplifier alone. When switch S_2 opens at the end of phase ϕ_2 , the output voltage will change by an amount $\Delta V_{out} = A'_m \Delta V_{c2}$, where the control voltage change ΔV_{c2} is due to charge injection, sampled noise and leakage current on capacitor C_2 , and is given by (24) with C_h replaced by C_2 . The

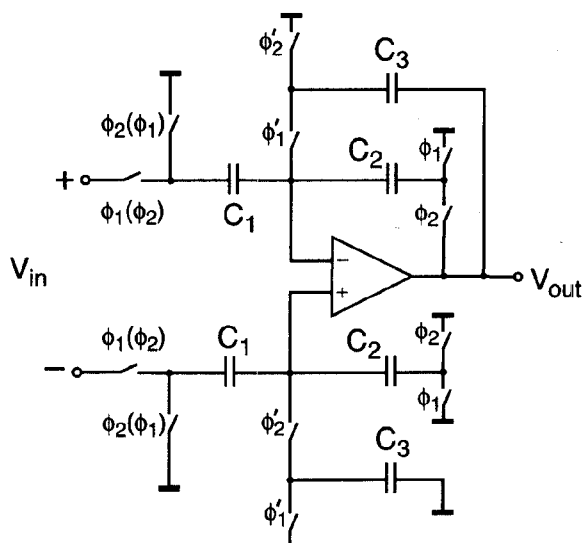


Fig. 31. An implementation of the scheme of Fig. 30. The primed clock phases cut off earlier than the unprimed ones.

initial input voltage equal to $V_{os(2)}$ should thus be reduced by an amount $\Delta V_{out}/A_m = \Delta V_{c2}/\alpha_m$ in order to bring the output voltage back to zero again. The resulting residual input-referred offset voltage $V_{os(1)}$ valid for phase ϕ_1 is therefore slightly different than for phase ϕ_2 due to charge injection onto C_2 and is given by

$$V_{os(1)} = V_{os(2)} - \frac{\Delta V_{c2}}{\alpha_m} \quad (40)$$

$$\cong \frac{\alpha_m V_{os-m} + \alpha_n V_{os-n}}{A_n} + \frac{\Delta V_{c1}}{\alpha_n} - \frac{\Delta V_{c2}}{\alpha_m}.$$

In the case the gains of the main and nulling amplifiers from their signal inputs are equal to their nulling inputs (corresponding to $\alpha_n = \alpha_m = 1$), (39) and (40) show that the residual offset is basically equal to the

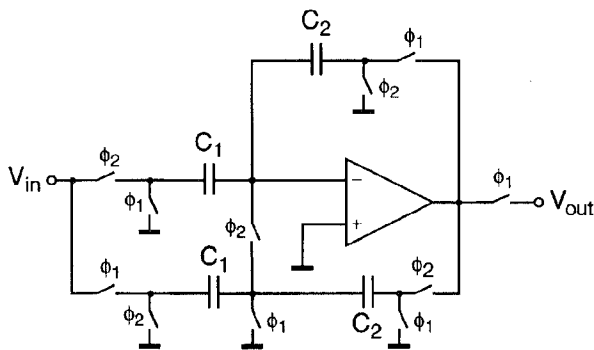


Fig. 32. A wideband compensated SC amplifier.

sum of the main and nulling amplifiers offsets, divided by the gain of the nulling amplifier A_n , plus the charge injection terms. The latter contribution can be reduced by decreasing the gains from the nulling input relative to the gains from the main inputs for both amplifiers. (This corresponds to setting both α_n and α_m larger than one.) The design criteria are very similar to those discussed in Section IV-E for the AZ scheme using an auxiliary input port.

As was suggested in [35], the injection terms contained in ΔV_{c1} and ΔV_{c2} can be reduced to a mismatch of injection by using a differential nulling input as shown in Fig. 24(a) or Fig. 25(a).

It should be noticed that during phase ϕ_2 the autozeroed amplifier has two forward signal paths: one directly through the main amplifier and the other through the nulling amplifier and the nulling input of the main amplifier. The dc gain is therefore equal to $A_m + A_n A'_m$, but generally reduces to $A_n A'_m$ corresponding to the gain from the input through the nulling amplifier and the main amplifier's nulling input.

The frequency responses of the main and nulling amplifiers must be designed so as to ensure that the autozeroed amplifier is stable during both phases. Stability during phase ϕ_1 requires that the main amplifier's primary input signal path and the nulling amplifier's auxiliary input signal path be unity-gain stable. The stability conditions during phase ϕ_2 depend on how the auxiliary inputs are realized. A detailed discussion of the stability of a particular implementation can be found in [35].

It should be noticed that since voltages V_{c1} and V_{c2} are generally not equal, a transient spike may appear at the amplifier output at the beginning of phase ϕ_2 when switch S_2 is connected to capacitor C_2 . Assuming that no signal is present at the amplifier input, the instantaneous value of the amplifier output voltage during ϕ_2 after the transient has vanished might be slightly negative in order to compensate for a positive spike and maintain a zero mean value. Another potential problem is caused by signals that are near or equal to an integer multiple of the clock frequency and that appear at the virtual ground of the amplifier. Such signals are sampled on C_2 at the end of phase ϕ_2 and may be aliased down to dc [35]. This will result in an apparent offset which is different than the

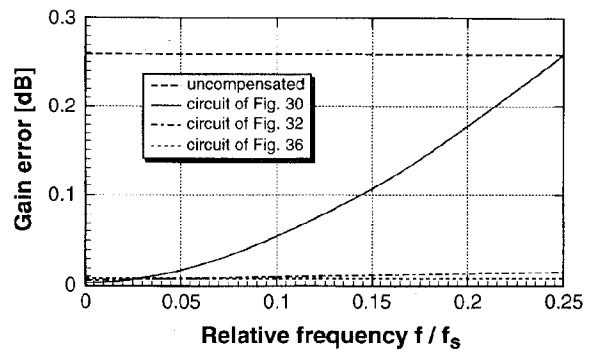


Fig. 33. Gain error versus frequency curves for compensated SC amplifier.

real main amplifier offset voltage V_{os-m} which is to be compensated. To circumvent this problem, the voltage V_{c2} should be proportional to the mean value of the voltage at the virtual ground node. This can be achieved by low-pass filtering the signal when sensing the main amplifier input voltage during phase ϕ_2 . A way to implement this low-pass filter is to use an operational transconductance amplifier (OTA) instead of an op-amp for the nulling amplifier [35] as shown in Fig. 26. The OTA is loaded by capacitor C_2 which is generally an external capacitor and can therefore be chosen rather large, setting the cut-off frequency at a very low frequency. The linear range of the OTA should be chosen sufficiently large in order to avoid any saturation due the sum of the dc offset to be compensated and the parasitic signal to be filtered.

V. PRECISION BUILDING BLOCKS USING THE CORRELATED DOUBLE SAMPLING TECHNIQUE

This section presents some examples of basic building blocks such as S/H stages, voltage amplifiers, integrators, and filters, that use the CDS technique to reduce the amplifier's offset and noise as well as to lower the effect of the finite amplifier gain.

A. SC S/H and Voltage Amplifiers

The CDS technique described earlier in Section IV-C for AZ comparators can readily be applied to SC voltage amplifiers. Fig. 27 illustrates a conventional SC amplifier [50]. The nominal output is $V_{out} = -(C_1/C_2)V_{in}$, but finite op-amp gain changes the ideal voltage gain to

$$\hat{A}_v = \frac{A_v}{1 + \frac{1 + A_v}{A}} \quad (41)$$

where $A_v = -C_1/C_2$ is the ideal gain, and A is the dc gain of the op-amp. Thus for typical values of A and A_v , a gain error of 1% or more may occur. In some high-precision applications, e.g., if the amplifier is part of a DAC or ADC, this may be unacceptable.

Also, a nonzero input-referred dc op-amp offset V_{os} will introduce an output offset voltage $V_{os-out} = (1 + |A_v|)V_{os}$. Since V_{os} is typically 1–10 mV, and $|A_v|$ can have a value

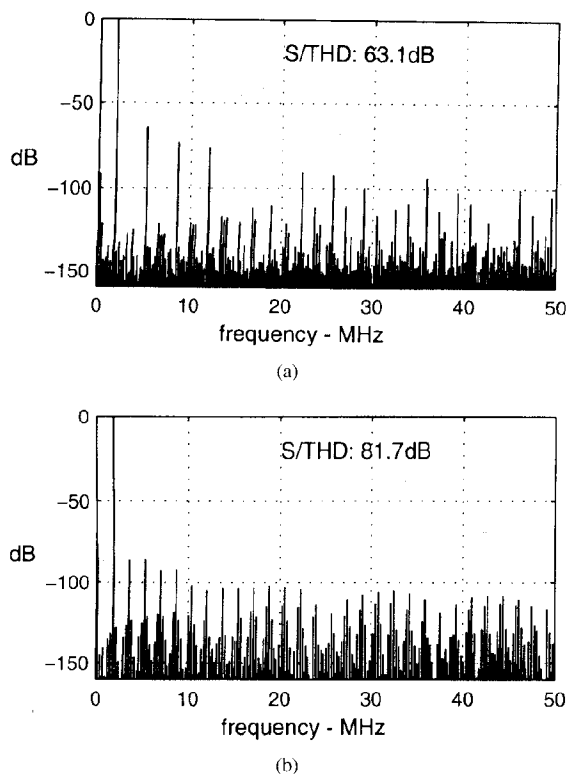


Fig. 34. Output spectra of SC amplifiers using nonlinear op-amps. The op-amp offset assumed was 5 mV, and the SC amplifier voltage gain was -2 : (a) offset-compensated SC amplifier (Fig. 28) and (b) wideband compensated SC amplifier (Fig. 32).

of 10 or more, the output offset may become a significant limitation on the permissible signal swing, especially in a low-voltage technology. It also may introduce ADC or DAC offset which needs to be calibrated.

If only the offset needs to be eliminated, the simple amplifier stage introduced by Gregorian [51] may be used [Fig. 28(a)]. Here, during the $\phi_1 = 1$ period, C_1 charges to $V_{in} - V_{os}$, and C_2 to V_{os} . V_{out} is developed during the $\phi_2 = 1$ interval. In this circuit, capacitors C_1 and C_2 are always connected to the virtual ground node (A), so if the input-referred offset voltage is constant, then when the switches driven by ϕ_2 close, the total charge entering node A is $C_1 V_{in} + C_2 V_{out} = 0$, which leads to the desired relation between V_{in} and V_{out} independent of V_{os} . However, as Fig. 28(b) illustrates, during the $\phi_1 = 1$ intervals the output is pulled to V_{os} , and the op-amp must have a high slew rate and fast settling time to enable V_{out} to slew back and forth at each clock transition. Also, the closed-loop gain of the stage is still affected by the dc gain of the op-amp the same way as in the circuit of Fig. 27.

Note that the small “degitching” capacitor C_{dg} does not play a role in the signal charge redistribution. Its sole purpose is to prevent glitches in the op-amp output by providing negative feedback during the brief intervals when the nonoverlapping clock phases are both low, and the feedback path of the op-amp is otherwise open-circuited [52].

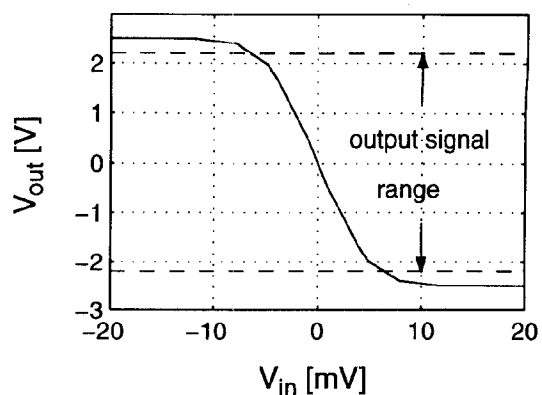


Fig. 35. The nonlinear op-amp transfer characteristics.

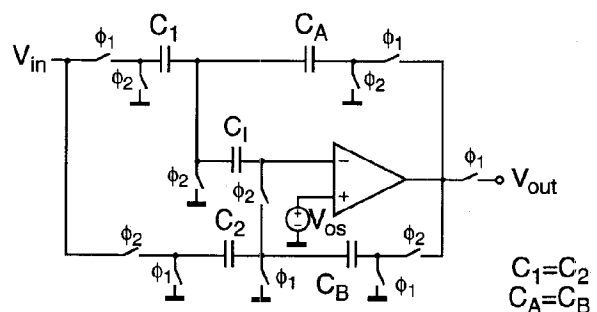


Fig. 36. SC amplifier with offset storage capacitor.

A unity-gain buffer stage, which can be used as a simple S/H circuit, or as an analog memory, or as an analog delay stage, and which also utilizes CDS to reduce dc offset effects, is shown in Fig. 29 [53]. Here, C charges to $V_{in} - V_{os}$ during $\phi_1 = 1$ period, and is connected as a feedback branch during $\phi_2 = 1$, causing $V_{out}(n) = V_{in}(n - 1/2)$. As in the previous circuit, the op-amp output voltage is reset to V_{os} in every clock period, and hence the slew-rate and settling-time requirements are difficult to meet for high clock rates. Also, the op-amp gain affects V_{out} . Note that the operation of this circuit does not depend on the exact value of its single capacitor.

An SC amplifier which does not require a resetting of the output in each clock period and also reduces the effect of the op-amp gain, and hence allows more relaxed op-amp specifications for low-frequency inputs, is shown in Fig. 30(a) [54]. In this circuit, the feedback reset switch is replaced by the elementary S/H branch consisting of C_3 and its two associated switches. Assume that the circuit is used as a noninverting amplifier, and hence the clock phases shown outside of the parentheses in Fig. 30(a) are valid. Then, when $\phi_2 \rightarrow 1$, C_1 discharges into C_2 , and the valid output voltage is generated. This voltage is stored in C_3 . When $\phi_1 \rightarrow 1$ next, C_3 becomes the feedback capacitor, while C_1 samples the difference between the input and the voltage at node (A) and C_2 discharges. If the signal bandwidth is much smaller than $f_s/2$, i.e., if the signal is significantly oversampled, then V_{out} does not vary much from one clock phase to the next. Thus for a finite dc

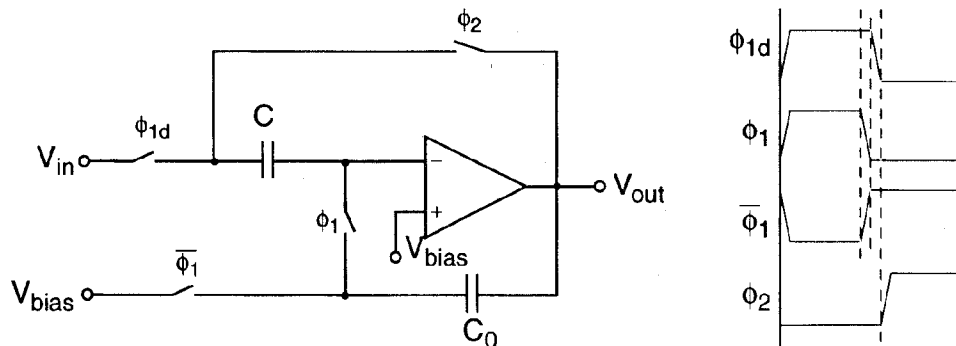


Fig. 37. Offset- and gain-compensated SC buffer.

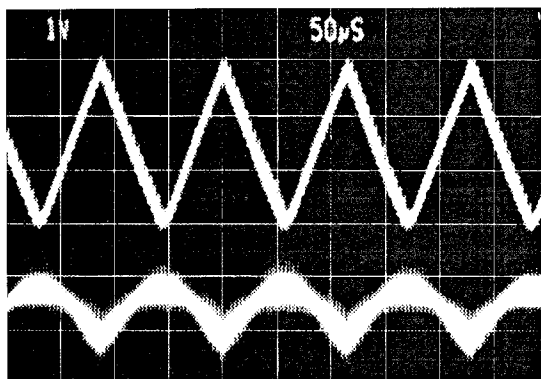


Fig. 38. Experimentally observed output voltages for offset-compensated SC buffers with a triangle-wave input at high clock rates. Top curve: buffer of Fig. 37; bottom curve: buffer of Fig. 29.

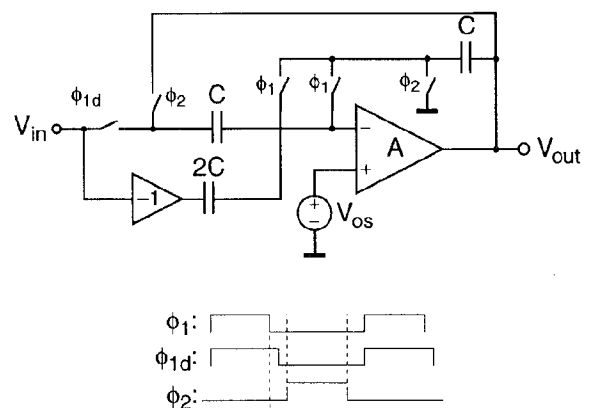


Fig. 39. A wide-band T/H stage.

op-amp gain A , the signal voltage $-V_{out}/A$ at the virtual ground is a slowly varying signal which is therefore nearly cancelled by the CDS switching of C_1 and C_2 . This reduces the effect of finite A on the voltage gain of the stage.

Fig. 30(b) illustrates the clock phases and waveforms of the amplifier. When $\phi_1 \rightarrow 1$ and the reset phase begins, there is a small step $\Delta V = V_{os} - V_{out}/A - (C_1/C_3)\Delta V_{in}$ in the output voltage, where ΔV_{in} is the change in V_{in} during the $\phi_2 = 1$ interval (The ΔV_{in} term enters only for noninverting operation.) This step occurs because, as $\phi_2 \rightarrow 1$, C_3 is disconnected from ground and reconnected to the virtual ground. As ΔV is of the order of a few mVs, this does not require a fast settling time or a high slew rate from the op-amp. The dc output offset voltage is $(1 - C_1/C_2)(V_{os}/A)$, which is much smaller than V_{os} .

Detailed analysis [54] shows that the gain is now weakly frequency dependent due to the high-pass CDS effect on the virtual ground voltage, with the dc gain given by

$$H(z)|_{z=1} = \frac{-\frac{C_1}{C_2}}{1 + \frac{\left(1 + \frac{C_1}{C_2}\right)}{A^2}}. \quad (42)$$

As (42) demonstrates, the error term in the denominator of the transfer function is now proportional to A^{-2} , rather

than A^{-1} . Thus the effective value of the op-amp gain as far as the dc gain is concerned is the square of the true value. Circuits with this property are called *gain-enhanced* or *gain-squaring* stages.

Fig. 31 shows a differential-input/single-ended-output SC amplifier incorporating the described principle [55]. Its CMOS implementation exhibited an accurate stage gain and a total of about 10 mV output offset, a 0.1–0.2% signal distortion and a 50 dB CMRR, in addition to a very low op-amp gain sensitivity.

The circuit of Fig. 30 was also successfully used in an GaAs SC amplifier, where the op-amp gain was restricted by the technology used [60].

The frequency dependence of the voltage gain of the compensated amplifier can be reduced, and thus the operation of the circuit extended to higher signal frequencies, by using the anticipatory compensation (prediction/correction) principle illustrated by the circuit shown in Fig. 32 [56]. Here, the precharging of the signal-processing capacitors is performed using the virtual-ground signal voltage that is expected to be present during the next amplification phase. This is achieved by essentially duplicating the SC branches used in the amplifier, and performing an anticipatory amplification step during the $\phi_2 = 1$ phase. If V_{in} changes only when $\phi_1 \rightarrow 1$, the operation will be independent of the rate of change of V_{in} , and hence of the signal frequency.

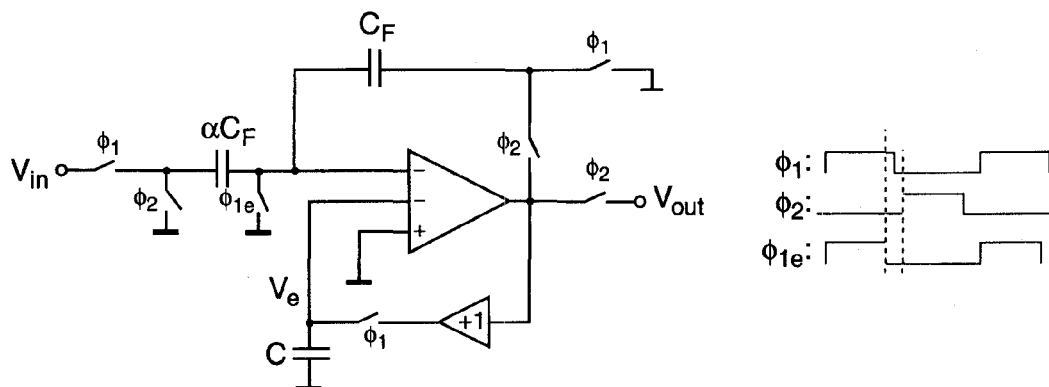


Fig. 40. Offset-compensated SC voltage amplifier using a low-sensitivity auxiliary input.

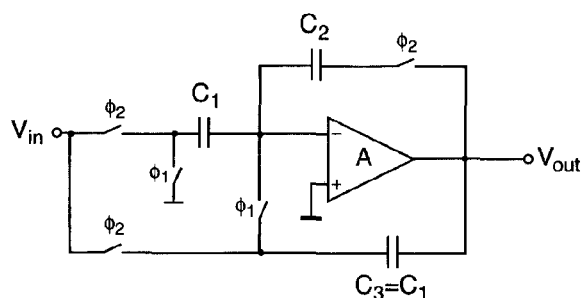


Fig. 41. Offset- and gain-compensated SC integrator.

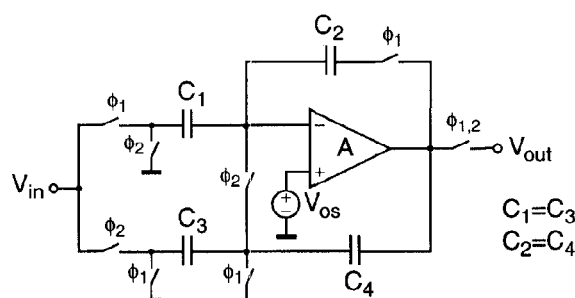


Fig. 42. Wideband compensated SC integrator.

The effectiveness of this principle is illustrated in Fig. 33, which compares the gain error versus frequency responses of an uncompensated SC amplifier with that of the stage of Fig. 30, and of the circuits of Figs. 32 and 36. The ratio of the dc op-amp gain to the desired stage gain was about 30. As the curves illustrate, the dc gain error is higher for the anticipating stage (because the error term is now $(1 + C_1/C_2)^2/A^2$, rather than $(1 + C_1/C_2)/A^2$ as for the circuit of Fig. 30, but the error remains essentially constant all the way up to $f_s/4$. The output voltage step for a constant input due to offset and finite gain is $\Delta V = (1 + C_1/C_2)(V_{os} - V_{out}/A)$. This is again typically of the order of 10 mV, not putting much strain on the op-amp.

The gain-enhancing property of CDS also helps to reduce the harmonic distortion caused by the nonlinear op-amp gain characteristics [74]. This is illustrated in Fig. 34, which compares the output spectra of the amplifiers of Figs. 28 and 32 for a 4.4 V output sine-wave signal. The assumed op-amp gain characteristic is shown in Fig. 35.

A different implementation of the anticipatory compensation principle, which uses an offset-storage capacitor C_I playing a somewhat similar role to that of C in the autozeroed amplifier of Fig. 21, is shown in Fig. 36 [57]. Its frequency response is very similar to that of the circuit of Fig. 32, and is also included in Fig. 33 (bottom curve).

The gain-compensating techniques described above can also be extended to the design of unity-gain buffers, T/H stages and memory or delay stages. Fig. 37 shows an improved version of the offset-compensated buffer of Fig. 29,

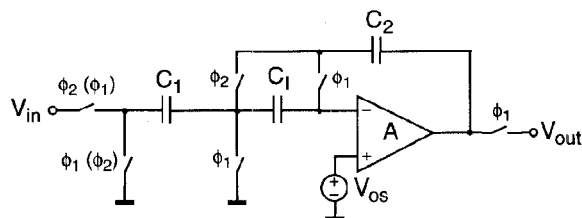


Fig. 43. SC integrator with offset-storing capacitor.

which does not require the resetting of the output voltage to V_{os} in every clock period [58]. Here, the reset switch is replaced by the S/H capacitor C_0 which holds the output voltage close to its previous value during the reset period. This also reduces the effects of the finite op-amp gain.

Fig. 38 shows some experimental results demonstrating the speed improvements achieved by this scheme over that of Fig. 29 [58].

An even faster version of the circuit, which relies on anticipating rather than storing the output voltage, is shown in Fig. 39 [59]. It is only practical to implement in fully differential form. In this circuit, the output signal tracks the input during the $\phi_1 = 1$ interval without inverting it. Hence, the virtual ground voltage at the instant when $\phi_2 \rightarrow 1$ will have the required value, independent of the signal frequency.

An alternative approach to offset compensation, which can also include the compensation of clock-feedthrough effects, but which does not enhance the effective value of

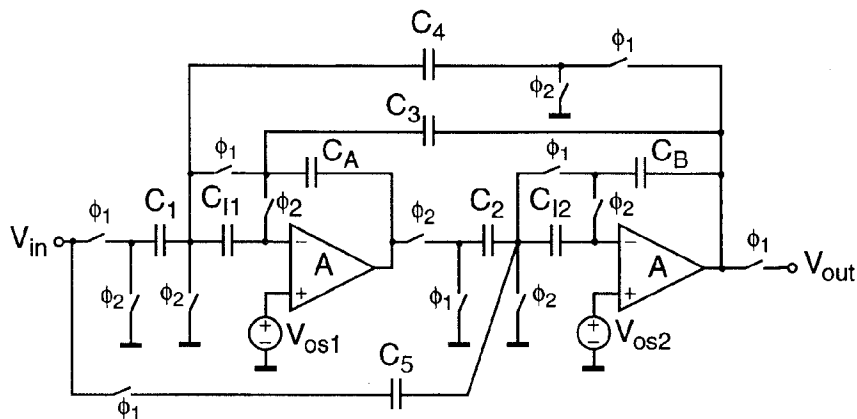


Fig. 44. Gain- and offset-compensated high-Q biquad.

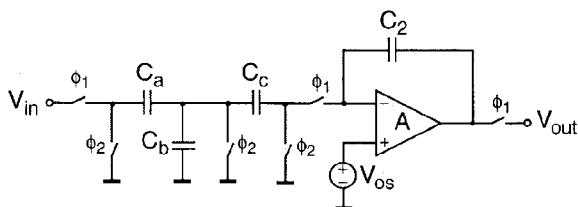


Fig. 45. Basic very-large-time-constant (VLT) integrator.

the dc op-amp gain, was discussed in Section IV-E earlier. It is shown schematically in Fig. 40. In this circuit, during the compensation phase ($\phi_1 = 1$), an error correction voltage V_e is developed across C . To reduce the effect of charge injection occurring when C is disconnected from the buffer as $\phi_2 \rightarrow 0$, the gain $|V_{out}/V_e|$ should be much lower than the signal gain of the op-amp. (See Section IV-E for a discussion of the optimization of this circuit.)

B. SC Integrators and Filters

The compensation schemes described in Section V-A are, with minor modifications, applicable also to SC integrators. As an overview of Section V-A reveals, these schemes fall into the following categories:

- 1) output is reset to V_{os} ; input capacitor stores and then subtracts V_{os} (Figs. 28 and 29);
- 2) output is held during reset; input and feedback capacitors are referenced to the previous value of virtual-ground voltage V_A (Figs. 30, 31, and 37);
- 3) output during reset anticipates the next signal output; signal-path capacitors are referenced to the anticipated value of V_A with (Fig. 36) or without (Figs. 32 and 39) the use of an extra offset-storage capacitor C_I ;
- 4) auxiliary input signal is established during reset; then it compensates for slowly varying noise effects (offset, $1/f$ noise, clock feedthrough); see Fig. 40.

As discussed above, the circuits using techniques 1) and 4) are relatively simple, but they cannot provide finite-gain compensation. Those using scheme 2) are more complex,

but they perform also gain squaring at or near dc. Finally, the circuits using the anticipatory compensation scheme 3) tend to be even more elaborate, but they provide gain compensation over a wide signal-frequency range. This improves the linearity of the stage. The use of more switches may, however, increase the sampled wideband noise in the output signal of these circuits.

Next, we shall briefly discuss how these CDS techniques can be used in SC integrators. In Fig. 28(a), by eliminating the switch grounding the right-side terminal of C_2 during reset, an offset- (but not gain-) compensated integrator results [51]. Similarly, it is possible to leave out the grounding switch of C_2 in the circuit of Fig. 30(a) to obtain an offset- and gain-compensated SC integrator [61]. However, the charge flow into node A from C_1 as $\phi_1 \rightarrow 1$ is now not balanced by an equal and opposite charge from C_2 as in Fig. 30(a), and hence, the gain compensation becomes inaccurate. This problem can be solved for an inverting integrator by a slight change in the switching arrangement for C_3 [54], as shown in Fig. 41. For noninverting integration, a slightly more elaborate circuit is needed [54].

Similarly, the wideband amplifier of Fig. 32 can be transformed into a gain- and offset-compensated integrator [56] by eliminating the switches discharging the feedback capacitor C_2 (Fig. 42).

Efficient gain- and offset-compensated integrators can also be obtained by using an offset-storage capacitor C_I . Fig. 43 illustrates a noninverting integrator [57] based on this principle. The circuit can also be used as an inverting integrator with a full clock period delay, if the clock phases of the input switches are interchanged. It was later independently recognized by several researchers [62], [63] that the integrator of Fig. 43 can also be used as a delay-free inverting integrator, by changing its switching scheme and choosing the value of C_I equal to that of the feedback capacitor C_2 .

It is also possible to apply scheme 4) (i.e., auxiliary input compensation) to SC integrators [64]. As before, the correction reduces the low-frequency noise (including that due to charge injection), but it does not compensate for

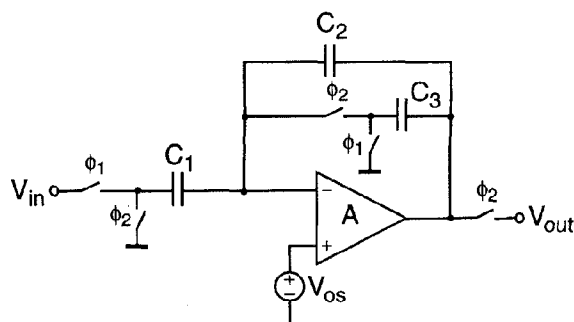


Fig. 46. Improved VLT integrator.

finite op-amp gain effects. It was used successfully in a high-accuracy low-voltage CMOS A/D converter [66].

Using the compensated integrators as building blocks, SC filters can thus be made insensitive to offset, $1/f$ noise and finite-gain effects. As an illustration, Fig. 44 shows a gain- and offset-compensated high-Q biquad [67] based on the modified version of the integrator of Fig. 43.

An important application of offset- and gain-compensated integrators is in delta-sigma A/D converters. Low-frequency noise and offset in the input integrator of the converter enters the output signal unfiltered, and hence should be suppressed. Also, in the cascade (MASH) architecture, the finite gain of the op-amp of the input stage allows the leakage of large unfiltered 1-b quantization noise into the output signal. Both problems can be remedied by using a compensated integrator in the input stage. Successful implementations of delta-sigma converters using offset- and gain-compensated front ends have been reported in [68]–[70].

C. SC Filters with Very Large Time Constants

In some applications, the magnitudes $|p_i|$ of the poles realized by SC filters are much smaller than the clock frequency $f_s = 1/T$. Since the time constants TC_2/C_1 of the integrators used in the filter are around $1/|p_i|$, now $C_2/C_1 \approx 1/(|p_i| \cdot T) \gg 1$ is required. This results in large chip area requirements. To remedy this situation, several ingenious schemes have been proposed. One option [72] is to use a T-cell attenuator at the input (Fig. 45). As a result of the charge redistribution in the T-cell, the capacitance spread $S = C_{\max}/C_{\min}$ can be reduced approximately to $\sqrt{S}$, and the chip area will be correspondingly smaller.

The T-cell integrator is sensitive to the stray capacitance in parallel with C_b , and it requires two large capacitors (normally, $C_b = C_2 \approx \sqrt{S} \cdot C_a = \sqrt{S} \cdot C_c$ are chosen). An improved very-large-time-constant (VLT) integrator [73] is shown in Fig. 46. Analysis shows that the circuit is equivalent to an integrator with a capacitance ratio $C_2/C_1 > 1$, followed by a voltage division by $1 + C_2/C_3$. If $C_1 = C_3 \approx C_2/\sqrt{S}$ are chosen, the ideal performance of the circuit will be the same as that of the T-cell integrator; however, it is stray-insensitive, and it needs only one large capacitor, C_2 .

A major flaw of both VLT circuits is their extreme sensitivity to offset, noise and charge-injection effects. To illustrate this point, consider the dc offset performance

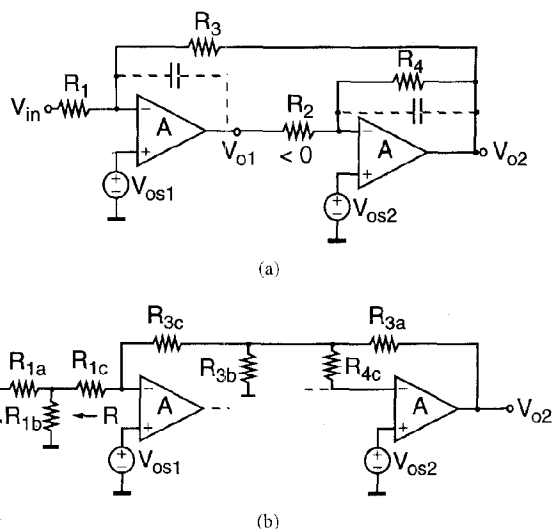


Fig. 47. The dc equivalent circuits: (a) dc equivalent circuit of a low-Q biquad and (b) dc equivalent circuit of a VLT biquad using T-cells.

of a conventional two-integrator loop where the familiar $SC \leftrightarrow R$ equivalence [50] was used [Fig. 47(a)]. Since V_{o2} has to generate V_{os1} at the virtual ground of the first op-amp by voltage division, we obtain $V_{o2} = (1 + R_3/R_1)V_{os1}$. For a VLT biquad, R_3 and R_1 are both large, and $V_{o2} \approx 2V_{os}$ to $10V_{os}$ results. By contrast, for a T-cell biquad, as the dc equivalent circuit of Fig. 47(b) illustrates, V_{o2} is divided twice before producing V_{os1} . This requires a much larger output offset voltage V_{o2} , often as large as $100V_{os1}$ to $200V_{os1}$. A similar argument shows that charge injection will also cause a large output offset. While the explanation is not so obvious for the VLT integrator of Fig. 46, it leads to a similar result: small dc offsets become amplified 100 times or more in the output signal of filters containing such stages.

To reduce this sensitivity, the VLT integrators should be compensated for their low-frequency noise, offset, and (if possible) charge injection. Figs. 48 and 49 illustrate the use of offset-storing capacitors in the circuits of Figs. 45 and 46, respectively [71]. These circuits reduce the low-frequency noise, and also the finite-gain effect on the frequency response. They do not, however, compensate for charge feedthrough; hence, the VLT filters should make full use of the well-known techniques (fully differential circuitry, delayed-cutoff clock signals, dummy switches, etc.) for reducing clock-feedthrough effects.

The improvement in finite-gain performance afforded by the compensated integrators is illustrated in Fig. 50. This shows the simulated gain responses of an eighth-order SC low-pass filter with Bessel–Chebyshev characteristics, a clock rate $f_s = 9.766$ kHz and a cutoff frequency of 2.5 Hz. The circuit of Fig. 46 was used, with (top curve) and without (bottom curve) gain- and offset-compensation. An op-amp gain of only 40 dB was assumed. The phase response is also distorted by the finite op-amp gain and restored by using CDS.

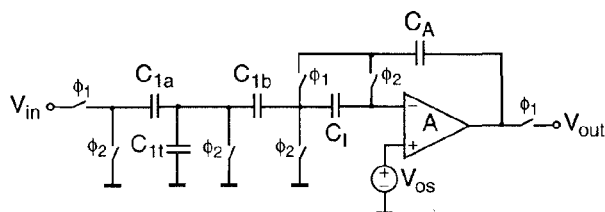


Fig. 48. T-cell integrator with offset compensation.

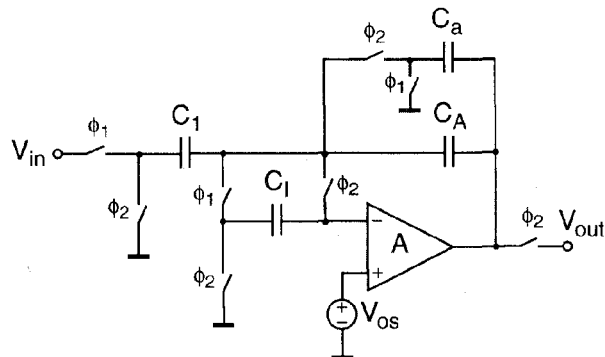


Fig. 49. The VLT integrator of Fig. 46 with offset compensation.

VI. A MICROPOWER LOW-NOISE CHOPPER AMPLIFIER USING THE CHOPPER STABILIZATION TECHNIQUE

This section presents a practical example of the use of the CHS technique in an amplifier to reduce its offset and $1/f$ noise without degrading the wideband noise. Unlike the many examples of the use of CDS in SC circuits, some of which were presented in Section V, there are very few examples of circuits that use CHS. The latter are generally low-noise continuous-time amplifiers, mainly used for instrumentation applications such as biomedical electronics.

Some applications such as electronic sensor interfaces require not only a very small offset and offset drift, but also very low noise. Often, the CHS technique is best suited to such applications. The electronics containing the front-end low-noise amplifier and the signal conditioning circuits, combined with the sensor, forms a microsystem which often has to be portable or stand alone, and is therefore battery powered. Hence, the power consumption of the electronics has to be small. It is therefore even more crucial to eliminate the $1/f$ noise and to reduce the noise down to the fundamental thermal noise which is mainly determined by the allowable current consumption of the input stage.

Examples of low-noise chopper amplifiers with a very low power consumption have been presented in [8], [12]. The design objective was to reach the microvolt level for both offset and noise, with a bandwidth limited to a few hundred Hz, while maintaining the power consumption below $100 \mu\text{W}$. This chopper amplifier used a selective stage with its center frequency locked to the chopper frequency in order to minimize the residual offset, as explained in Section III. The chopper amplifier presented in Fig. 9 where the amplifier is replaced by a selective amplifier and the

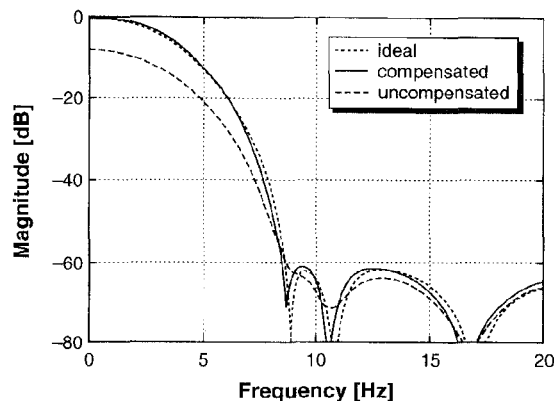


Fig. 50. Frequency responses of VLT filters.

output is low-pass filtered at half the chopper frequency, has an overall low-pass transfer function given by

$$G_0(s) \cong \frac{8}{\pi^2} \frac{A_{\max}}{1 + s/\omega_c} \quad (43)$$

where $\omega_c = \omega_0/(2Q)$ is the chopper amplifier's cutoff frequency, determined by the selective amplifier's resonant frequency ω_0 and quality factor Q . $A_{\max}$ corresponds to the gain of the selective amplifier at the resonant frequency. Equation (43) has been obtained assuming that $Q \gg 1$ and is valid for $|s| \ll \omega_0$. It shows that the chopper amplifier's dc gain is only $\pi^2/8 = 1.234$ (or approximately 2 dB less than the gain of the selective amplifier at the resonant frequency).

The selective amplifier can be realized using either a low-pass [12] or a band-pass second-order $g_m - C$ continuous-time filter [44]–[49]. The advantage of choosing the band-pass circuit is that the input and output chopper modulation signals can be identical, since there is no phase shift at the resonant frequency. The filter's resonant frequency can be locked to the chopper frequency by means of a PLL using either a voltage-controlled reference filter [44], [48] or a voltage-controlled oscillator built using the same resonator as the selective amplifier [44], [47], and [49].

An example of such a band-pass filter is presented in Fig. 51. The gain $A_{\max}$ at the resonant frequency is given by the ratio g_{m1}/g_{m4} , where g_{m1} and g_{m4} are the transconductances of the input and output stages, respectively. This ratio has to be large in order to have a sufficient dc gain for the chopper amplifier. Typically, for a dc gain of 500, the g_{m1}/g_{m4} ratio has to be 617! This large gain imposes the use of linearized transconductors for realizing the integrators and the output load [47], in order to limit the distortion and intermodulation. Another problem arising from this large gain is the mistuning effect resulting from the difference between the bias currents of the integrators. This is due to the fact that the offset of the input differential pair $T_1-T'_1$ appears at the low-pass output multiplied by the corresponding dc gain, while the band-pass output offset stays at zero. This offset voltage is fed to the input of differential pair $T_3-T'_3$ and compensates the offset current due to the input differential pair, forcing the band-pass

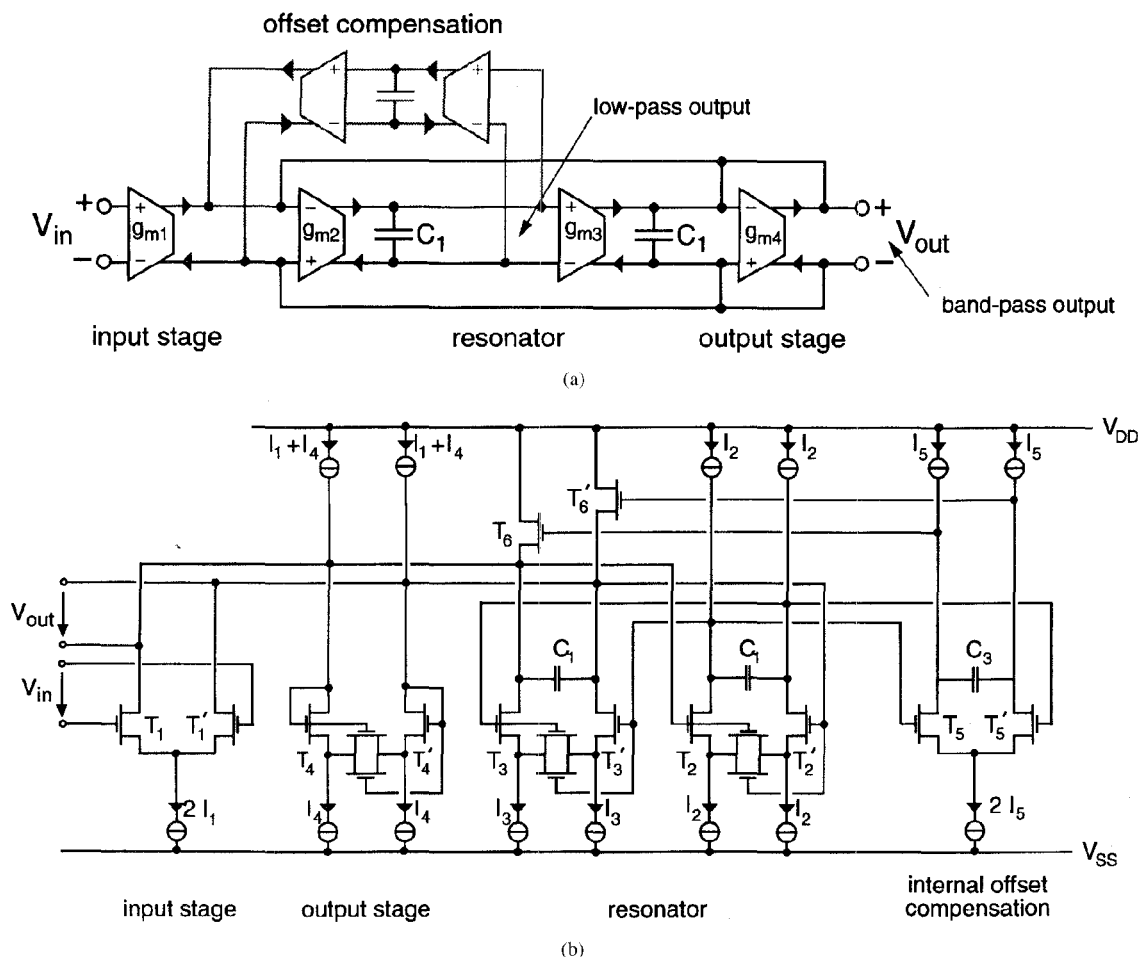


Fig. 51. Second-order $g_m - C$ continuous-time band-pass filter used to realize the selective amplifier: (a) principle and (b) implementation.

output to stay at zero. The resulting mismatch between the biasing points of the two integrators gives rise to a nonzero phase shift at the chopper frequency, which is unacceptable for the chopper amplifier. Fortunately, since the signal is modulated and amplified at high frequency, the current offset ΔI_1 produced by the mismatch of input differential pair T_1-T_1' can be compensated without changing the signal transfer function. This offset compensation can be realized as shown in Fig. 51, by sensing the offset voltage with differential pair T_5-T_5' at the low-pass output (i.e., at the input of differential pair T_3-T_3' and injecting the current necessary to compensate the offset current ΔI_1 using transistors T_6-T_6' . This compensation does not require any S/H action since the signal is mainly centered around the resonant frequency. The feedback loop can therefore be held closed continuously if a compensation capacitance C_3 is added at the output of differential pair T_5-T_5' to ensure stability.

The measured frequency responses of the selective amplifier and the chopper amplifier are shown in Fig. 52(a) and (b), respectively. The gain measured at the filter's 4 kHz resonance frequency is equal to 56.8 dB, corresponding to

a 54.8 dB dc gain for the chopper amplifier. The quality factor is 5.4 which sets the -3 dB cut-off frequency of the chopper amplifier to 367 Hz.

Using (21), the chopper amplifier's input-referred noise can be found from

$$S_{Nin} = \frac{\pi^2}{8} 4\gamma kT R_{Nin} \left(1 + 0.8525 \frac{f_k}{f_{chop}} \right) \quad (44)$$

where R_{Nin} is the equivalent input thermal noise resistance of the selective amplifier, which is inversely proportional to the transconductance g_{m1} of the input differential pair. Noise factor γ is defined as the product $g_{m1} R_{Nin}$ and accounts for the excess thermal noise coming from sources other than the input stage.

The low-frequency output noise of the chopper amplifier has been measured and is shown in Fig. 53. As expected, the $1/f$ noise has disappeared, leaving a white noise PSD corresponding to an equivalent input-referred white noise of 43 nV/ $\sqrt{\text{Hz}}$, which can still be made lower at the expense of an increase of the input differential pair bias current and thus of the total power consumption.

The input and output chopper modulators are simply realized by four switches controlled by complementary phases,

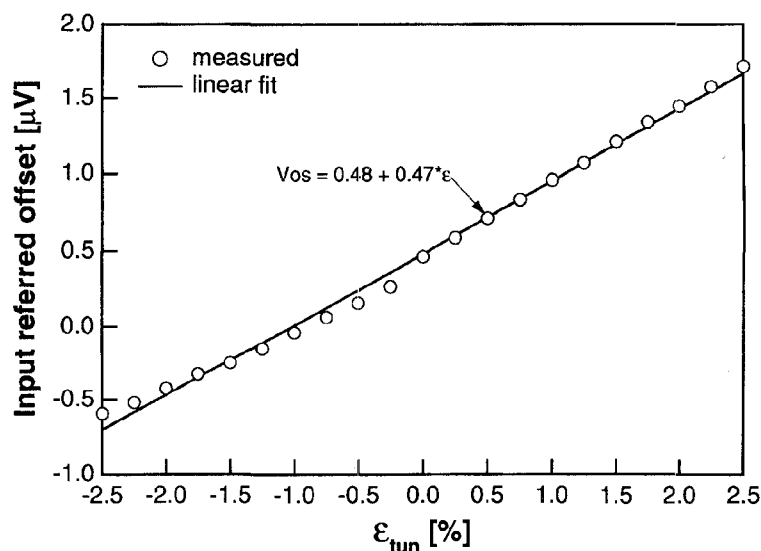


Fig. 55. Measured input referred offset versus tuning error.

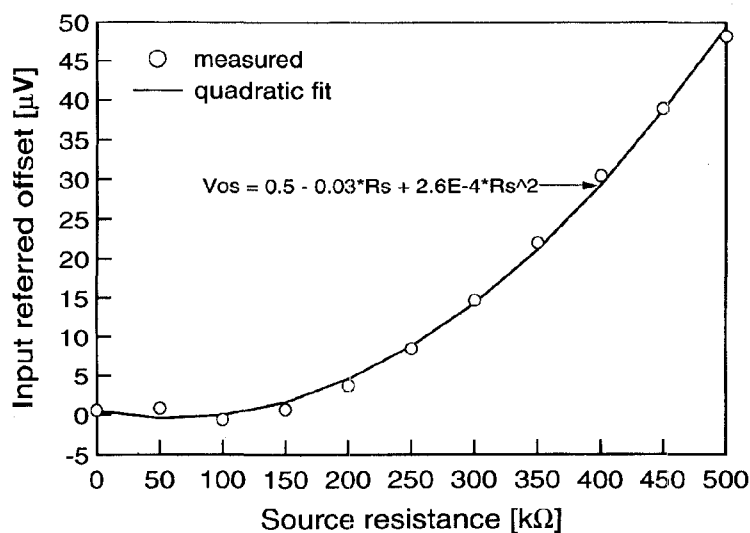


Fig. 56. Measured input referred offset versus source resistance.

VII. CONCLUSIONS

A detailed comparison of the relative advantages and disadvantages of the CHS technique versus CDS was given earlier [7], [8]. These are the main points.

- 1) CDS is inherently a sampled-data method; CHS is based on modulation rather than sampling, and hence can be used for continuous-time signals.
- 2) CDS reduces the low-frequency noise by highpass filtering; CHS translates it to some out-of-band frequency.
- 3) The output noise of a CDS stage is normally dominated by the undersampled wideband noise; in a continuous-time CHS stage the noise spectrum is not folded, and hence $1/f$ noise remains dominant in the baseband before the second modulation. After demodulation, white noise is folded into the baseband

and replaces the $1/f$ noise. If the chopping frequency is much larger than the noise corner frequency, then the baseband white noise in the output is only very slightly larger than it was without CHS.

- 4) As shown earlier, CDS can also be used to enhance the effective gain of the op-amps used in the signal processing. A continuous-time CHS system, by contrast, causes the op-amp to amplify a higher-frequency signal, and hence its effective gain is usually reduced.

In conclusion, CDS is preferable in applications which inherently use sampled-data circuits (such as SC stages), so that the baseband noise behavior is not made worse by noise aliasing. Also, the dc offsets are eliminated, not just modulated to higher frequency, by CDS, which may improve the allowable signal swing. Finally, the gain-

$$|H_n(f)|^2 = d^2 \left\{ \left[\frac{\sin \alpha}{\alpha} - \frac{\sin \beta}{\beta} \right]^2 + \left[\frac{1 - \cos \alpha}{\alpha} - \frac{1 - \cos \beta}{\beta} \right]^2 \right\} \quad (50)$$

enhancing ability of CDS may be an important advantage in some applications. On the other hand, CHS is the method of choice if the system is a continuous-time one to start with, and if low baseband noise is an important requirement.

APPENDIX

AUTOZEROED NOISE ANALYSIS

The autozeroed voltage $v_{AZ}(t)$ shown in Fig. 2 can be approximated by

$$v_{AZ}(t) = \sum_{m=-\infty}^{+\infty} h(t - mT_s)[v_N(t) - v_N(mT_s)] \quad (46)$$

where it has been assumed that the RC time constant in the track mode is much smaller than the duration T_{AZ} of the AZ phase, i.e., that voltage $v_{AZ}(t)$ instantaneously goes down to zero at the beginning of the AZ phase. Here $h(t)$ is a window function corresponding to the hold phase:

$$h(t) \equiv \begin{cases} 1, & \text{for } 0 \leq t < T_h, \\ 0, & \text{otherwise.} \end{cases} \quad (47)$$

If $v_N(t)$ is assumed to be a stationary random process having a PSD $S_N(f)$, the PSD of the autozeroed voltage is given by

$$S_{AZ}(f) \equiv \sum_{n=-\infty}^{+\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right) \quad (48)$$

which consists of replicas of the original spectrum shifted by multiples of the sampling frequency and multiplied by the squared magnitude of the corresponding band transfer function. These transfer functions can be evaluated by calculating the Fourier transform of $v_{AZ}(t)$

$$H_n(f) = d[e^{-j\pi nd} \text{sinc}(\pi nd) - e^{-j\pi dfT_s} \text{sinc}(\pi dfT_s)] \quad (49)$$

where $d \equiv T_h/T_s$ is the duty cycle. The $|H_n(f)|^2$ functions are then readily obtained from (49) (see (50) at the top of the page) with $\alpha \equiv 2\pi dn$, $\beta \equiv 2\pi dfT_s$.

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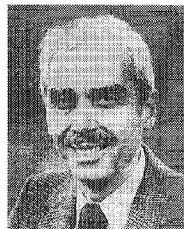
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6 Multipath Compensation Techniques

In many of the compensation techniques described in the previous chapter, the addition of stages to the circuit leads to a reduction of the obtainable bandwidth. Going from simple two-stage Miller compensation to Nested Miller compensation with three gain stages, for instance, results in a fifty percent smaller bandwidth. Also Hybrid Nested Miller compensation suffers from this drawback. Although the bandwidth reduction effect is absent in Reversed Nested Miller compensation, the dependency of this compensation technique on the load capacitance makes it fundamentally unsuited for general purpose applications. Therefore we would like to eliminate the bandwidth reduction in Nested and Hybrid Nested Miller compensation, while retaining the high level of robustness inherent to these methods.

This chapter presents the Multipath technique to avoid the step back in bandwidth of certain nested compensation schemes. The technique is based on a parallel signal path that bypasses one or more transistors of the main path. This bypass realizes a short high-frequency signal path, while the circuit maintains the gain advantage for low frequencies of a longer path with more amplifier stages. A key aspect of the Multipath technique is that we can configure the parallel signal path independently from the main path. This avoids the appearance of pole-zero doublets in the passband. Earlier feedforward circuits [18] mostly base themselves on the insertion of capacitors to create a high frequency bypass for critical components, such as lateral PNPs. These bypass capacitors result in strong

6. Multipath Compensation Techniques

and inevitable pole-zero doublets, however, disqualifying the circuits for a large number of applications where fast settling is of importance. Pole-zero doublets are pairs of a closely spaced pole and zero. Their presence deteriorates the settling performance of an amplifier by introducing signal components into the step response with a time constant much larger than the one associated with the bandwidth of the circuit. Section 6.2 will address the relation between the occurrence of pole-zero doublets and these so-called slow-settling components.

6.1. Multipath Nested Miller compensation

The first candidate for bandwidth improvement is the Nested Miller compensation technique described in Section 5.2. This section showed that three-stage Nested Miller compensation has a factor two bandwidth penalty as compared to ordinary, two-stage, Miller compensation. This is related to the down shift of the bandwidth limiting pole p_1' caused by the outer Miller loop. The root locus of Fig. 5-9b, which is repeated in Fig. 6-1, illustrated the down shift. Closing of the outer Miller loop shifts down the bandwidth limiting pole p_1' , until it collides with pole p_3 . The collision occurs at approximately half the frequency of p_1' . The addition of more stages, and consequently more Miller capacitor nests, even further reduces the obtainable bandwidth.

We can overcome the bandwidth reduction caused by the nested Miller loops by adding a Multipath input stage that provides an independent path directly driving the output stage [20]. The result is the Multipath Nested Miller compensation topology depicted in Fig. 6-2. In this figure, transistors T_1 through T_3 , together with the two capacitors C_{m1} and C_{m2} , build up the conventional Nested Miller compensation structure. The Multipath input stage is transistor pair T_4 . This differential pair directly drives the output transistor, bypassing T_2 for high frequencies.

In Figure 6-3 the Bode plot of the Multipath Nested Miller compensated amplifier is shown. The gray line represents the high-gain, low-frequency part established by the three-stage Nested Miller compensated amplifier. The black line shows the high frequency part created by the two transistors T_4 and T_1 and Miller capacitor C_{m1} . Adding the two plots yields a straight 20dB/dec frequency response of which only the low frequency part is provided by the three-stage amplifier. The high frequency

6.1. Multipath Nested Miller compensation

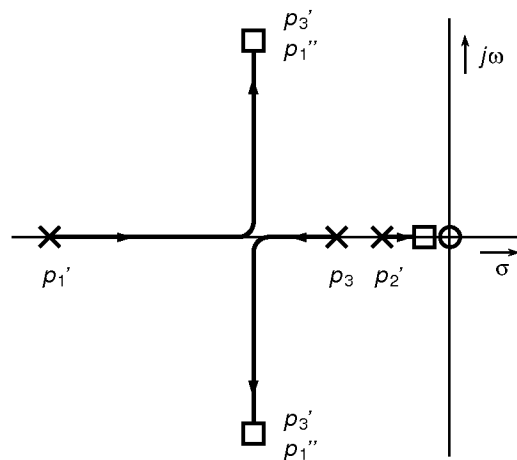


Fig. 6-1. Root locus showing the bandwidth reduction caused by the closing of the outer Miller loop of Nested Miller compensation.

portion is determined by two stages. Therefore, the obtainable bandwidth approaches the theoretical maximum of a two-stage amplifier with single Miller compensation. A major advantage of the Multipath technique is that the matching of the high and low frequency part of the total frequency response is duly controllable. This is important, since even a slight mismatch can deteriorate the settling behavior of the amplifier, as demonstrated in Section 6.2. The following analysis confirms the accurate matching properties.

The Multipath input stage has no effect on the position of the poles of the original circuit. This is caused by the fact that the current generated by the input stage only depends on the input voltage. Therefore, we can regard this current as coming from an independent input signal source. We can use this observation fruitfully in Eq. 2-11, which expresses the transfer between any two nodes of a network as the ratio Δ_{ij}/Δ . Since any input source enters the cofactor in the numerator of this equation, the addition of a branch that carries a current proportional to the input signal only affects

6. Multipath Compensation Techniques

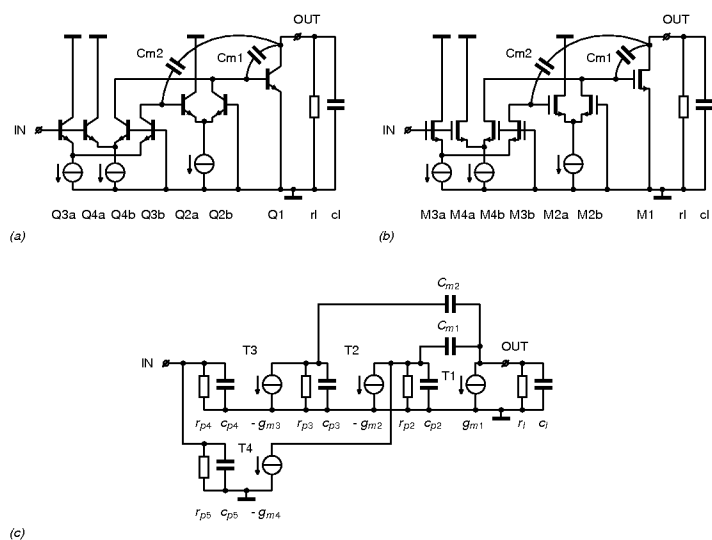


Fig. 6-2. Three-stage amplifier with Multipath Nested Miller compensation.

the number and position of the zeros. The poles, on the other hand, remain fixed at their original locations.

In the case of Multipath Nested Miller compensation the pole locations are identical to those of the Nested Miller compensation technique. These follow from solving the denominator of Eq. 5-19 and are given by

$$p_1'' = p_1' \left(\frac{1}{2} + \frac{1}{2} \sqrt{1 - \frac{4g_{m2}}{p_1' C_{m1}}} \right) \tag{6-1}$$

$$p_3' = p_1' \left(\frac{1}{2} - \frac{1}{2} \sqrt{1 - \frac{4g_{m2}}{p_1' C_{m1}}} \right) \tag{6-2}$$

6.1. Multipath Nested Miller compensation

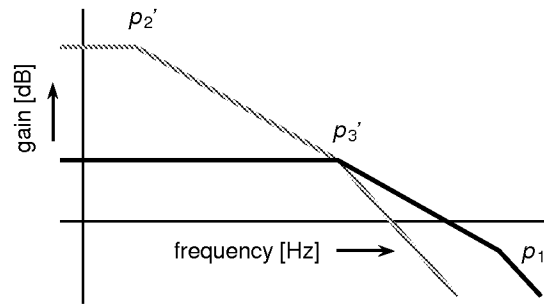


Fig. 6-3. Bode plot of the Multipath Nested Miller compensated amplifier.

under the condition that $p_2'' \ll p_1''$. Nodal analysis reveals that the Multipath input stage adds a single zero to the transfer function of the Nested Miller circuit. The position of this zero z_m is given by

$$z_m = -\frac{g_{m2}g_{m3}}{g_{m4}C_{m2}} \quad (6-3)$$

To obtain a straight 20dB/dec frequency response, the zero z_m must exactly cancel out the pole p_3' . This leads to the condition

$$\frac{g_{m4}}{C_{m1}} = \frac{p_1''}{p_1'} \frac{g_{m3}}{C_{m2}} \quad (6-4)$$

The ratio p_1''/p_1' denotes the relative movement of the bandwidth limiting pole p_1' . We can derive the ratio from Eq. 6-1. It equals

$$\frac{p_1''}{p_1'} = \frac{1}{2} + \frac{1}{2} \sqrt{1 - \frac{4g_{m2}}{p_1' C_{m1}}} \quad (6-5)$$

6. Multipath Compensation Techniques

To realize the maximum bandwidth, the down shift of the pole p_1 must be as small as possible, which corresponds to maximizing Eq. 6-5. The optimum value is attained when the transconductance of the middle stage g_{m2} is set to zero. In that case no bandwidth reduction takes place, since in the absence of T_2 the circuit of Fig. 6-2 reduces to a two-stage amplifier consisting of the Multipath input stage T_4 and the output stage T_1 . Although under these conditions the bandwidth is at its theoretical maximum, clearly this situation is not preferable from the gain point of view. Fortunately a compromise is possible with high gain and only a fractional reduced bandwidth. The compromise is given by

$$\frac{g_{m2}}{C_{m1}} \approx \frac{p_1'}{10} \quad (6-6)$$

With this ratio, the bandwidth reduction following from Eq. 6-5 only amounts to about 10%, and still three stages contribute to the low frequency gain. Since the relative bandwidth reduction is close to unity, we can simplify Eq. 6-4, giving the condition for pole-zero cancellation, into

$$\frac{g_{m4}}{C_{m1}} = \frac{g_{m3}}{C_{m2}} \quad (6-7)$$

In other words, to obtain a straight first-order frequency response, the unity-gain frequency determined by the original input stage T_3 and the outer Miller capacitor C_{m2} must equal the unity-gain frequency of the Multipath input stage T_4 and the inner Miller capacitor C_{m1} . One can also understand this condition intuitively. The left-hand part of Eq. 6-7 defines the slope of the frequency response of the two-stage single Miller compensated amplifier comprising T_1 and T_4 , while the part on the right gives the slope of the three-stage Nested Miller compensated amplifier T_1 , T_3 and T_4 . Matching of the two slopes results in an unbroken curve.

Since the dimensioning of Multipath Nested Miller compensation depends on the ratios of capacitors and transconductances only —both being among the best controlled parameters of an I.C. process— matching can be very close. In a typical bipolar process the mismatch can be as low as 0.1%. CMOS technology yields slightly less controllable ratios, resulting in a mismatch of about 5%. We can find the position of the pole-zero doublet as

6.1. Multipath Nested Miller compensation

$$\omega_d = \frac{g_{m2}}{C_{m1}} \quad (6-8)$$

or, with Eq. 6-6

$$\omega_d \approx \frac{p_1'}{10} \approx \frac{\omega_t}{5} \quad (6-9)$$

The second approximation of this equation is based on the fact that, for a phase margin of 60° , the unity-gain frequency ω_t of the opamp should be half p_1'' ($\approx p_1'$). The unity-gain frequency is therefore given by

$$\omega_t = \frac{g_{m4}}{C_{m1}} = \frac{g_{m3}}{C_{m2}} = \frac{1}{2}p_1' \quad (6-10)$$

which is indeed a factor of two higher than the unity-gain frequency of Nested Miller compensation given by Eq. 5-23. Equation 6-6, Eq. 6-7 and Eq. 6-10 are the dimensioning expressions for Multipath Nested Miller compensation. The pole p_1' is given as before by $p_1' = g_{m1}/c_l$.

The introduction of the factor $1/10$ in Eq. 6-6 indicates that the bias currents of the Multipath Nested Miller compensated circuit can be considerably lower than those of its Nested Miller compensated counterpart. In practical situations this will about balance the extra current required for the Multipath input stage. Therefore, the bandwidth improvement of the Multipath technique goes without a current penalty and the bandwidth-to-power ratio is improved. Also the die area of the chip does not increase when using Multipath Hybrid Nested Miller compensation, since the higher bandwidth allows for smaller compensation capacitors.

The root locus in Fig. 6-4 shows the movement of the poles in the Multipath Nested Miller compensation structure as a result of the introduction of capacitor C_{m2} . In contrast to Nested Miller compensation, closing the outer Miller loop only moves the poles slightly because of the low value g_{m2}/C_{m1} . Pole p_3' is eliminated by the Multipath zero z_m . Since pole p_1' remains virtually motionless, no bandwidth reduction occurs as compared to the single Miller compensation technique.

6. Multipath Compensation Techniques

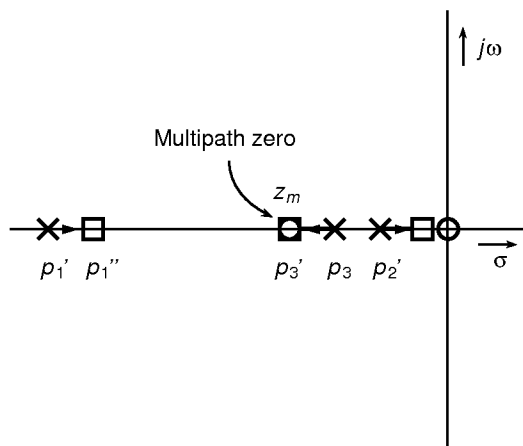


Fig. 6-4. Multipath Nested Miller compensation’s root locus showing the effect of the outer Miller capacitor C_{m2} .

6.1.1. Multipath Darlington

The low transconductance of the intermediate stage of Multipath Nested Miller compensation makes a special type of circuit possible where the intermediate inverting amplifier stage is substituted by a voltage follower. The resulting circuit presents a wide bandwidth alternative to the Darlington configuration.

The Multipath Darlington is shown in Fig. 6-5. It consists of the output stage Q_1 and the emitter follower intermediate stage Q_2 . The signal current sources on the left model the normal input stage Q_3 and the Multipath input stage Q_4 . The current of each of the sources equals the input voltage of the amplifier times the respective transconductance g_{m3} and g_{m4} . The current that the Multipath input stage directly provides to the output transistor results in a bandwidth improvement over the normal Darlington composite. In the traditional configuration the output impedance of

6.3. Multipath Hybrid Nested Miller compensation

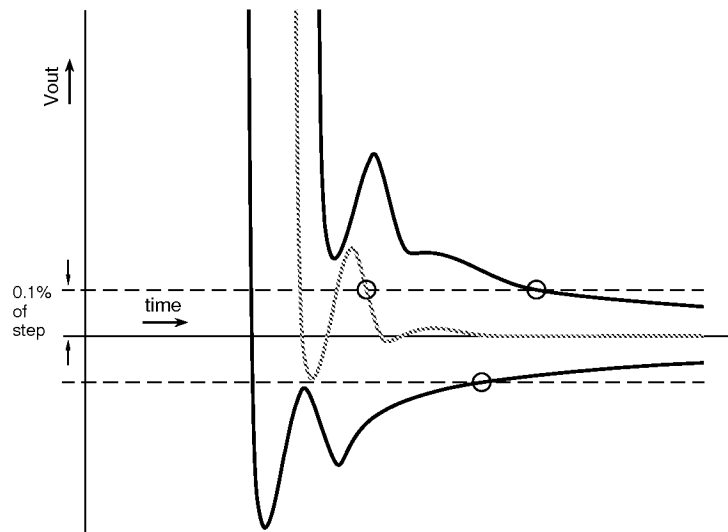


Fig. 6-9. Typical step response showing the effect of slow-settling components on the step response. The gray curve is the response without slow-settling effects, the black curves give the slow-settling step responses for various pole-zero positions.

6.3. Multipath Hybrid Nested Miller compensation

Although the bandwidth reduction of Hybrid Nested Miller compensation is small compared to Nested Miller compensation, in some cases even this small reduction is not acceptable. In this situation the Multipath technique is an attractive option resulting in Multipath Hybrid Nested Miller Compensation [15] [16]. Figure 6-10 shows a Multipath Hybrid Nested Miller compensated amplifier. The Multipath input stage T_5 that directly drives the output transistor T_1 is added to the Hybrid Nested Miller compensated circuit of Fig. 5-21. As with Nested Miller compensation, the extra input stage and the output stage together constitute a two-stage amplifier with

6. Multipath Compensation Techniques

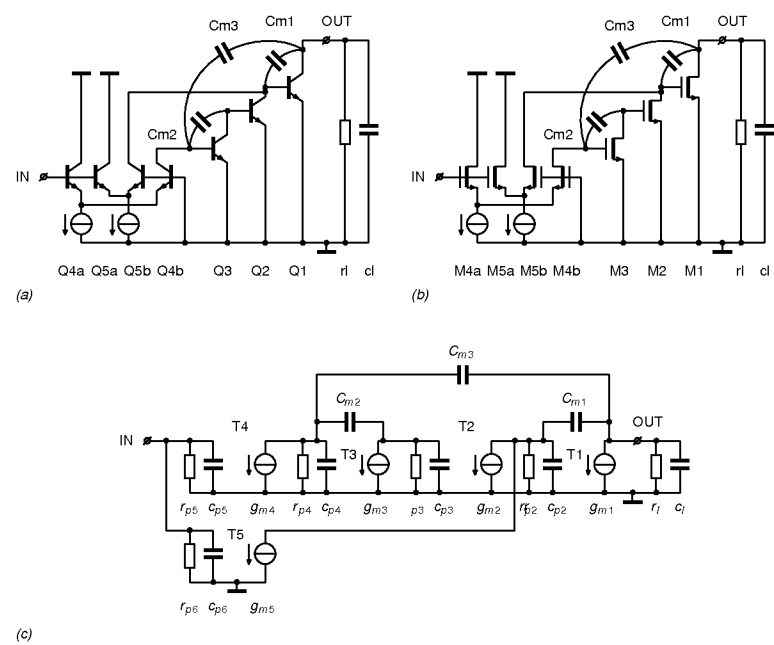


Fig. 6-10. Amplifier with Multipath Hybrid Nested Miller compensation.

relatively low gain, but a high bandwidth. The remainder of the circuit, a four-stage amplifier with Hybrid Nested Miller compensation, pairs a low bandwidth and a high gain. When the two circuit parts properly match, the result is a 20dB/dec roll-off with both a high unity-gain frequency and a high gain.

The analysis of Multipath Hybrid Nested Miller compensation is almost identical to that of Multipath Nested Miller compensation when the voltage gain around the second stage is taken into account according to the scheme of Fig. 5-23. Equation 6-6 therefore becomes

6.3. Multipath Hybrid Nested Miller compensation

$$\frac{g_{m2}C_{m3}}{C_{m1}C_{m2}} \approx \frac{p_1'}{10} \quad (6-18)$$

Equation 6-7, which denotes the condition for pole-zero matching, for Multipath Hybrid Nested Miller compensation changes into

$$\frac{g_{m5}}{C_{m1}} = \frac{g_{m4}}{C_{m3}} \quad (6-19)$$

For the frequency of the pole-zero doublet, Eq. 6-9 remains valid:

$$\omega_d \approx \frac{p_1'}{10} \approx \frac{\omega_t}{5} \quad (6-20)$$

The unity-gain frequency of the Multipath Hybrid Nested Miller compensated circuit equals

$$\omega_t = \frac{g_{m5}}{C_{m1}} = \frac{g_{m4}}{C_{m3}} = \frac{1}{2}p_1' \quad (6-21)$$

To assure that the limited bandwidth of the voltage amplifier around T_3 does not deteriorate the overall performance of the circuit, Multipath Hybrid Nested Miller compensation puts an additional demand on the dimensioning. This condition is comparable to the condition found in Eq. 5-52 for Hybrid Nested Miller compensation without the Multipath input stage. Due to the easing of the bandwidth requirement of the four-stage amplifier part (it merely has to supply the gain) the condition for Multipath Hybrid Nested Miller compensation relaxes into

$$\frac{g_{m3}}{C_{m3}} > \frac{p_1'}{10} \quad (6-22)$$

A complete instrumentation voltage amplifier arises if we include the current-to-voltage conversion function of the load impedances Z_{L1} and Z_{L2} . In that case the reciprocal nominal overall voltage gain $1/A_{vm}$ and the overall CMCR $1/H_i$ are given by Eq.3.4.4.

$$\begin{aligned} 1/A_{vm} &= -1/Y_2 Z_{Ld} \\ 1/H_i &\approx 1/H_e + 1/F_e H_{iL} \end{aligned} \quad (3.4.4)$$

with: $Z_{Ld} = Z_{L1} + Z_{L2}$, $1/H_{iL} = \Delta Z_{L1}/Z_{Ld}$, $\Delta Z_{L1} = Z_{L1} - Z_{L2}$.

The reciprocal value of the discrimination factor is defined as: $1/F_e = (I_{2c}/V_{ic})/(I_{2d}/V_{id}) = 1/Z_{ice} Y_{in}$.

From the above expression we see that a low overall CMCR $1/H_i$ can only be obtained if the amplifier has a low CMCR $1/H_e$ as well as a low reciprocal discrimination factor $1/F_e$. The effect of the latter term is further reduced by a low CMCR $1/H_{iL}$ of the load circuit.

Instrumentation Voltage Amplifier

An instrumentation voltage amplifier with a voltage-source character between the output terminals arises if we insert a balanced floating impedance amplifier with an OFA and two impedances Z_{11} and Z_{12} between the preceding example's instrumentation transadmittance amplifier and its load circuit [3.3, 3.4].

The complete instrumentation voltage amplifier circuit is drawn in Fig. 3.4.4 together with the source and load circuits.

The reciprocal nominal overall differential voltage gain and the CMCR of the complete amplifier are described by Eq.3.4.5.

$$\begin{aligned} 1/A_{vm} &= -1/Y_2 Z_{1s} \\ 1/H_i &\approx 1/H_e + 1/F_e H_i \end{aligned} \quad (3.4.5)$$

with: $Z_{1s} = Z_{11} + Z_{12}$, $1/H_i = \Delta Z_1/Z_{1s}$, $\Delta Z_1 = Z_{11} - Z_{12}$

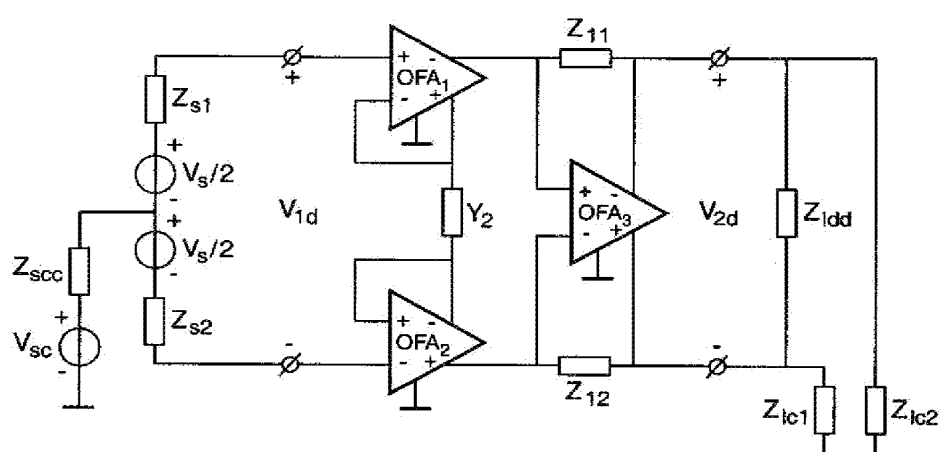


Fig. 3.4.4: Instrumentation voltage amplifier with source and load circuits

The instrumentation amplifier has a floating entrance port and an independently floating exit port. It measures the differential entrance voltage at nominal zero entrance currents. The differential exit port has a voltage source character.

Instrumentation Current Amplifier

If we change the sequence of the transadmittance and transimpedance amplifiers of the preceding example we obtain an instrumentation current amplifier. This circuit is drawn in Fig. 3.4.5 together with the source and load circuits.

The overall reciprocal nominal current gain is given by Eq.3.4.6.

$$I/A_{vn} = -1/Y_2 Z_{ls} \quad (3.4.6)$$

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A Systems Perspective

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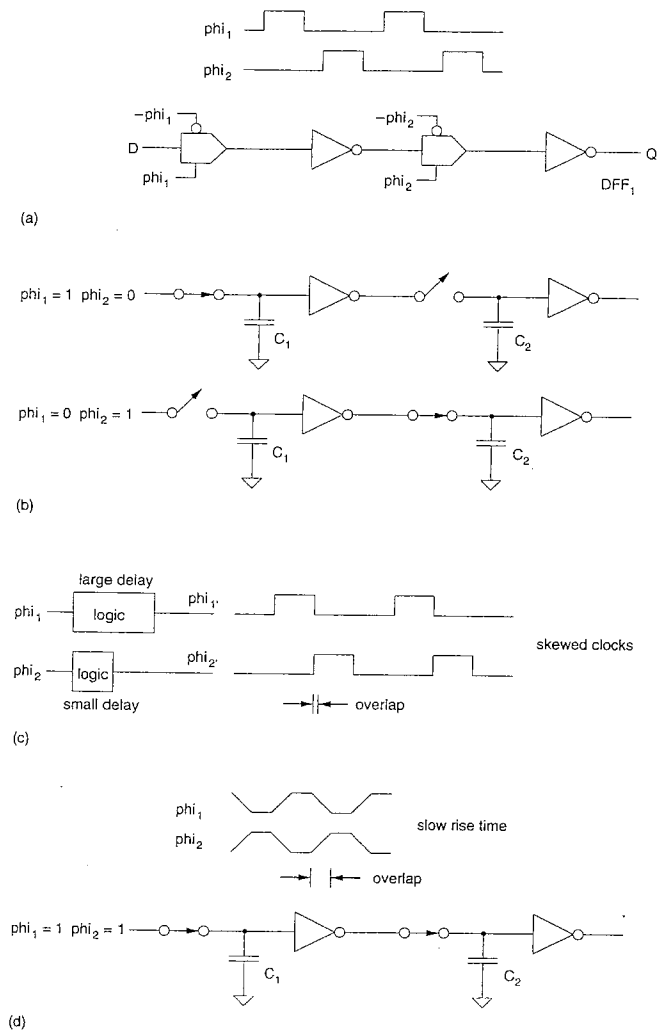


FIGURE 5.69 Two-phase clocking: (a) dynamic register and clock waveforms; (b) operation; (c) failure due to clock skew; (d) failure due to slow-rise-time clocks

5.5.10 Two-phase Memory Structures

Two-phase registers are usually replications of single-phase structures with ϕ_1 feeding the master and ϕ_2 feeding the slave of the register. Examples are shown in Fig. 5.70.

Considering DFF1, two representative layouts are shown in Fig. 5.71(a) and Fig. 5.71(e). A layout representing the DFF2 configuration are shown in

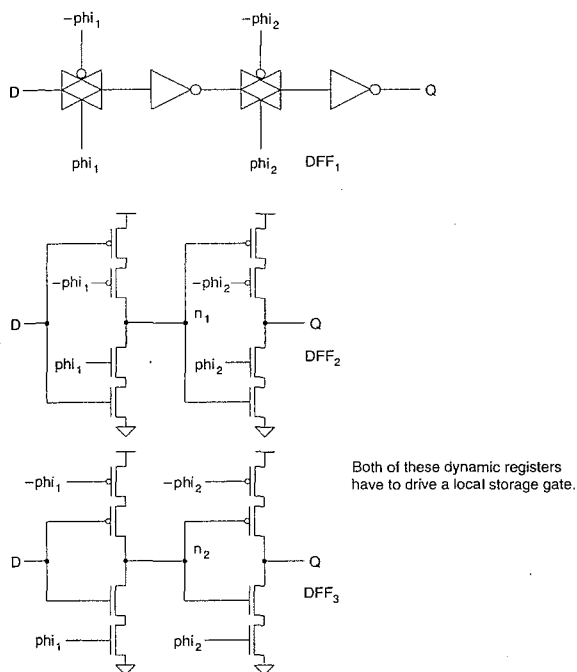


FIGURE 5.70 Two-phase dynamic registers

Fig. 5.71(b), Fig. 5.71(c) and Fig. 5.71(d). Note that routing clocks in polysilicon may lead to clock-delay problems if long unbuffered clock lines are used. An example of DFF2 may be found in Fig. 8.70.

A reduction in the number of clock lines can be accommodated if only n-transistors are used in the transmission gate, as would be the case in an n-MOS design (Fig. 5.72a). Two effects occur in this configuration. First, the '1' level transferred to the input of the inverter is degraded to approximately $V_{DD} - V_{tn}$. This has the effect of slowing down the low transition of the inverter. Furthermore, the high-noise margin (N_{MH}) of the inverter is degraded. It also has the possible effect of causing static power dissipation. For instance, if $V_{tp} < V_{DD} - V_{tn}$, then the p-transistor in the inverter will be turned on when the inverter output is in the low state, thus causing current to flow through the inverter. This is consistent with the reduced N_{MH} . Although this is not catastrophic, it must be taken into account when calculating total power dissipation. Figure 5.72(b) shows the addition of p feedback transistors to provide fully restored logic levels. Figure 5.72(c) shows a single clock version of this register that uses p and n pass transistors. The rising transition at the output of the inverter in Fig. 5.72(a) and 5.72(b) is faster

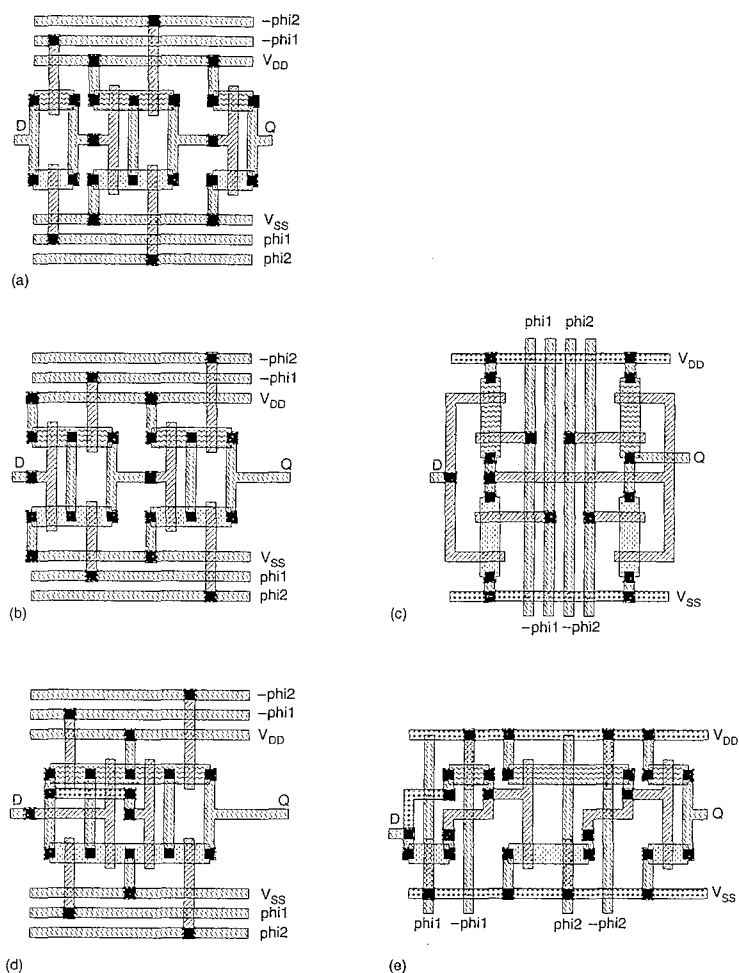


FIGURE 5.71 Various layouts for two-phase dynamic registers

because the capacitance at the output is reduced due to the absence of the p-transistor. There is no hard and fast rule for when the various flip-flop configurations should be used. Of course, if density is crucial the last mentioned flip-flop could be used, provided that the speed was suitable and that static power dissipation was not a problem. This can only be reconciled by worst-case simulation and power-dissipation calculations.

Clock distribution techniques for two-phase clocks may differ depending on the design. One technique is to globally distribute the two clocks with

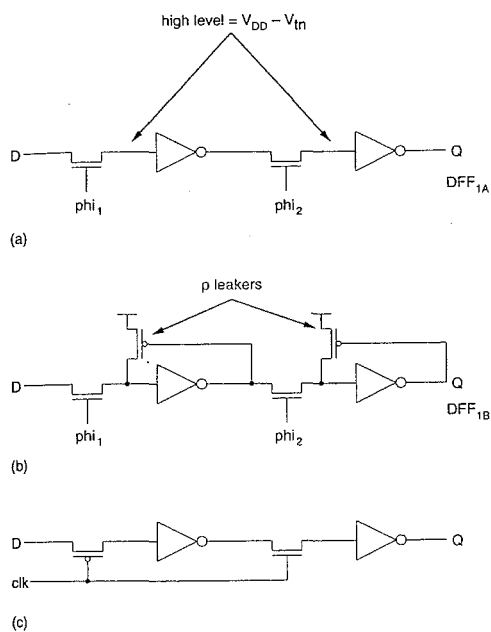


FIGURE 5.72 Two-phase registers with single-polarity clocks: (a) nMOS pass transistors; (b) adding p leakers; (c) a single clock version; (c) pass gate

or without their complements. Alternatively, a single clock can be distributed and local two-phase clocks generated in individual modules. Regardless of the technique, somewhere a two-phase clock generator is required. Figure 5.73 shows the basic circuit that is normally used; it is based on a cross-coupled RS flip-flop. This basic design is modified to meet drive considerations and overlap requirements. Methods for conditionally loading two-phase registers are shown in Fig. 5.74. Figure 5.74(a) uses a multiplexer on the front of a two-phase register. Alternatively, the clocks to the master may be gated, as shown in Fig. 5.74(b). Gating the clock can lead to delayed clocks, which in turn can lead to clock-skew problems in registers that are susceptible to skew. Another clock qualification method is shown in Fig. 5.74(c). This uses

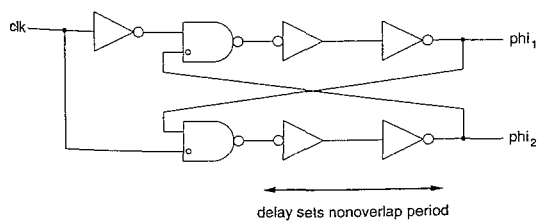


FIGURE 5.73 Two-phase clock generator

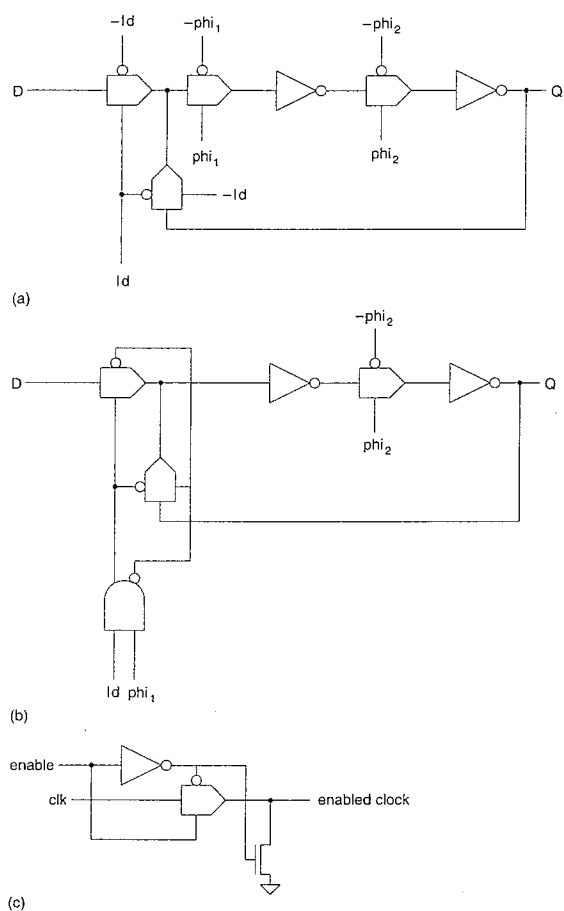


FIGURE 5.74 Clock-enable circuits: (a) mux; (b) clock gating; (c) pass gate

a transmission gate as an AND function. The n-pulldown transistor ensures that the falling edge of the enabled clock is fast.

5.5.11 Two-phase Logic Structures

For two-phase systems, conventional static logic may be used in conjunction with the memory elements that have been described in the last section. If dynamic logic is required, the two-phase logic scheme outlined in Fig. 5.75 may be used. In this scheme, the first stage is precharged during ϕ_{i1} and evaluated during ϕ_{i2} . While the first stage is evaluated, the second stage is precharged and the first-stage outputs are stored on the second-stage inputs.



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330

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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Electronic Acknowledgement Receipt	
EFS ID:	5759233
Application Number:	12464572
International Application Number:	
Confirmation Number:	1854
Title of Invention:	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers
First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Customer Number:	79124
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	55123P376
Receipt Date:	23-JUL-2009
Filing Date:	12-MAY-2009
Time Stamp:	16:32:31
Application Type:	Utility under 35 USC 111(a)

Payment information:					
Submitted with Payment			no		
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	55123P376_20090723_Resp_Corr_App_Pprs.PDF	23942	no	1
			2068ea635d3f918fa5489c1696b1d147f0182ebc		
Warnings:					
Information:					

2	Drawings-only black and white line drawings	55123P376_20090723_Rplcmnt_Figs.pdf	357196 0176a2714336c03bbe09a9a73c5cc840b794378c	no	17
Warnings:					
Information:					
Total Files Size (in bytes):			381138		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

RUDY G. H. ESCHAUZIER, ET AL.

Application No.: 12/464,572

Filed: May 12, 2009

For: **Low-Noise, Low-Power, Low Drift Offset Correction in
Operational and Instrumentation Amplifiers**

Art Group:

Examiner:

Confirmation No.: 1854

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Sir:

In response to the Notice to File Corrected Application Papers mailed May 28, 2009, please find enclosed:

- substitute drawing(s) in compliance with 37 CFR § 1.84;

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: July 23, 2009

1279 Oakmead Parkway
Sunnyvale, CA 94085-4040
Telephone: (714) 557-3800



Roger W. Blakely, Jr., Reg. No. 25,831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.



Jessica A. Clark

07/23/09

Date

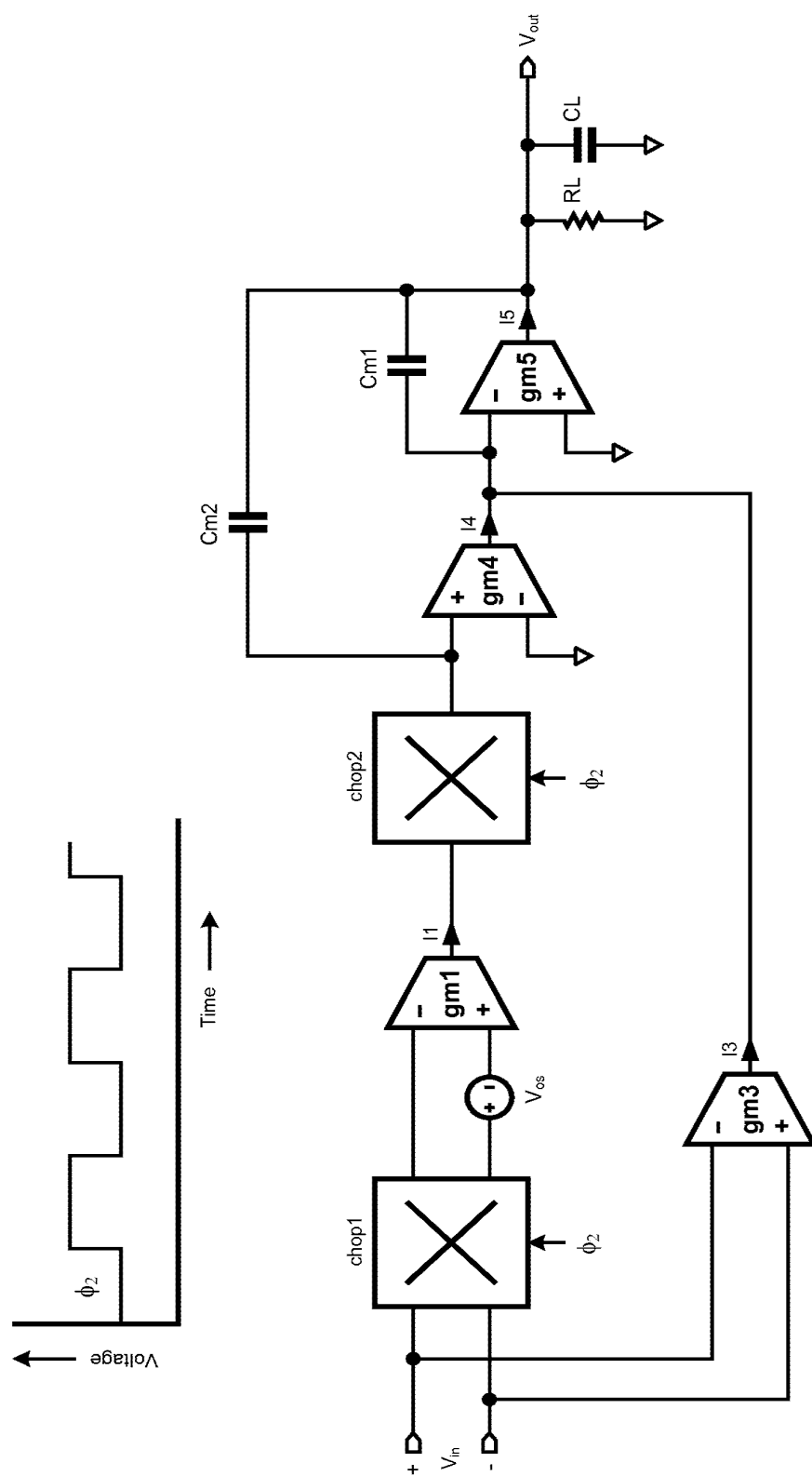


Fig. 1 (Prior Art)

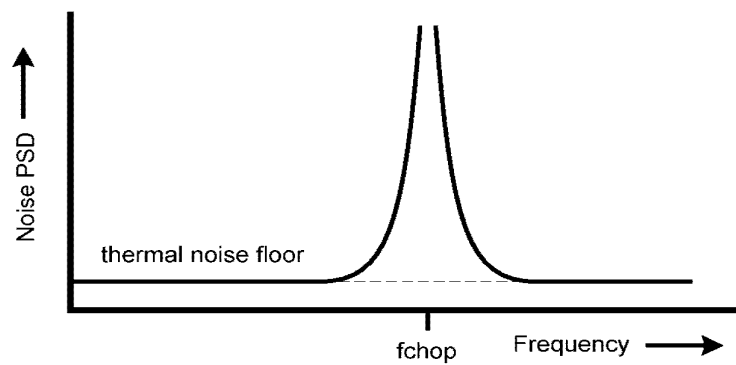


Fig. 2 (Prior Art)

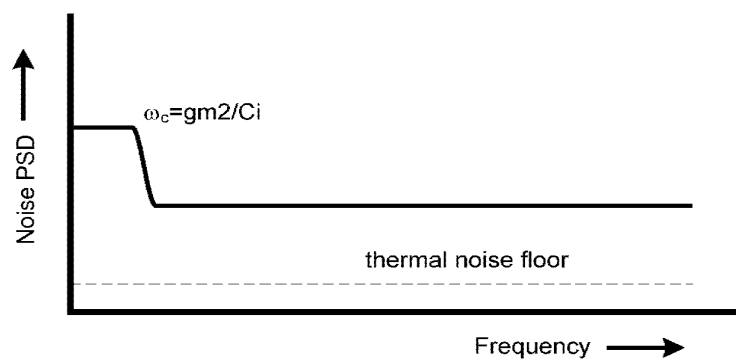


Fig. 4 (Prior Art)

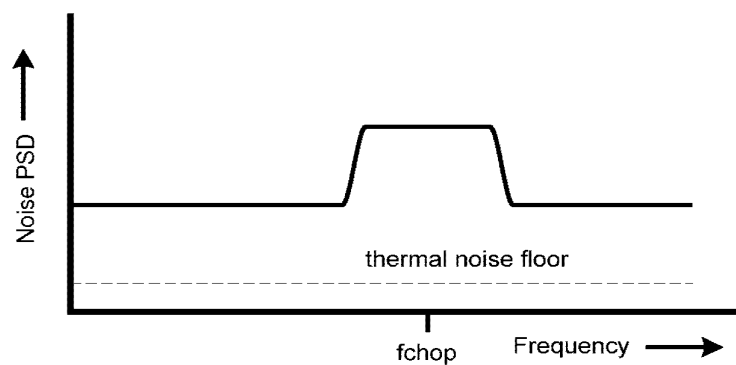


Fig. 6

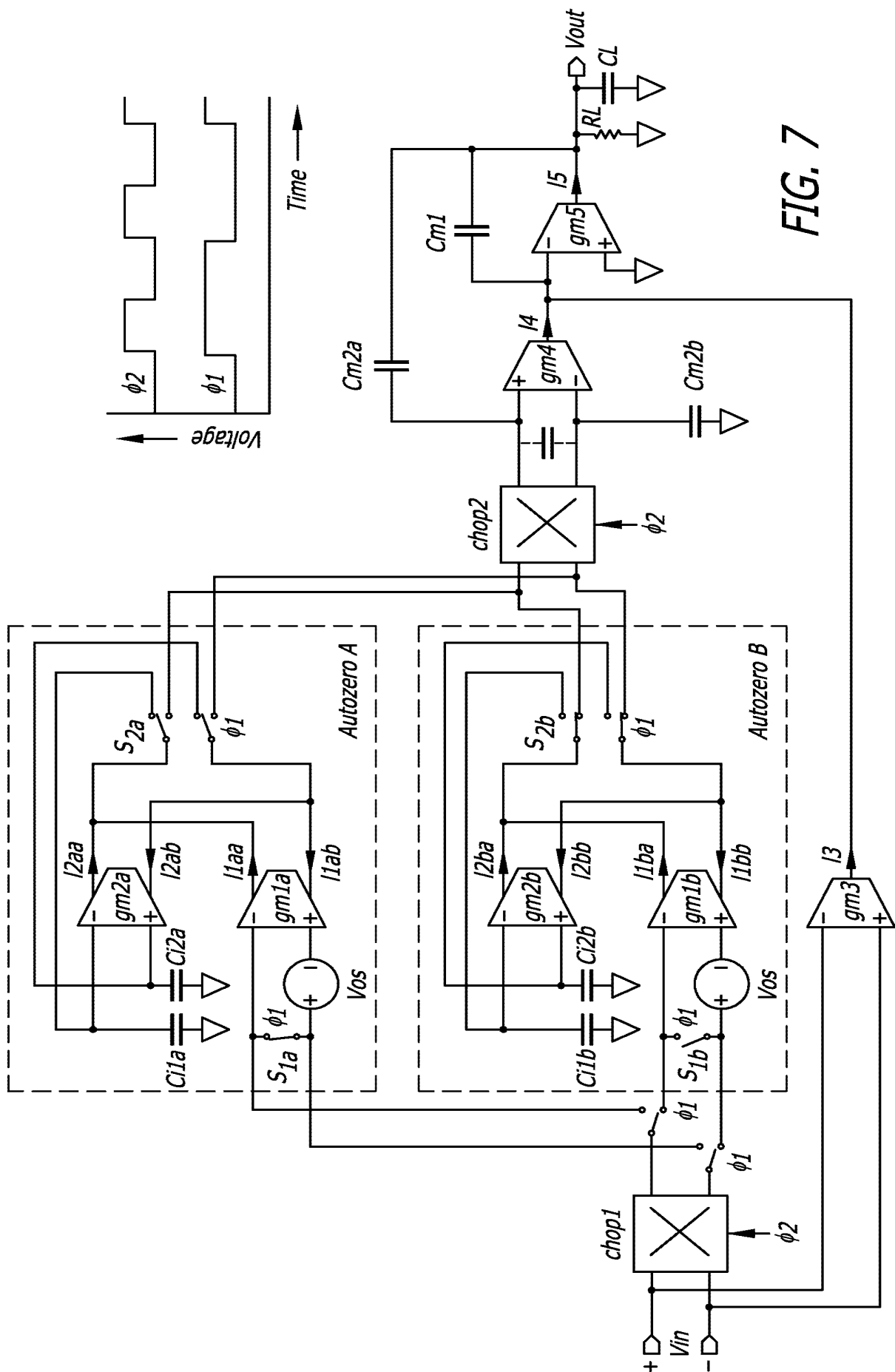


FIG. 7

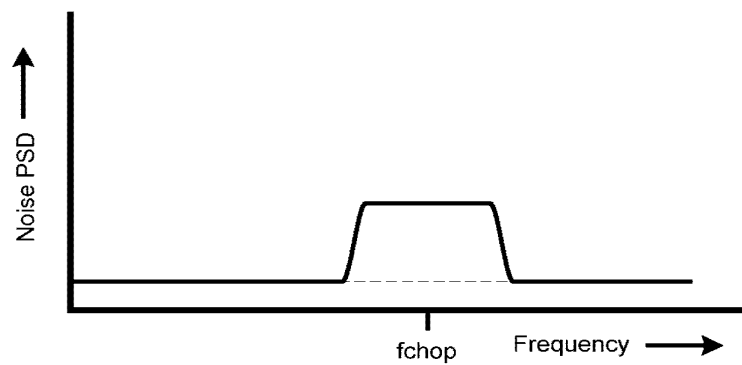


Fig. 8

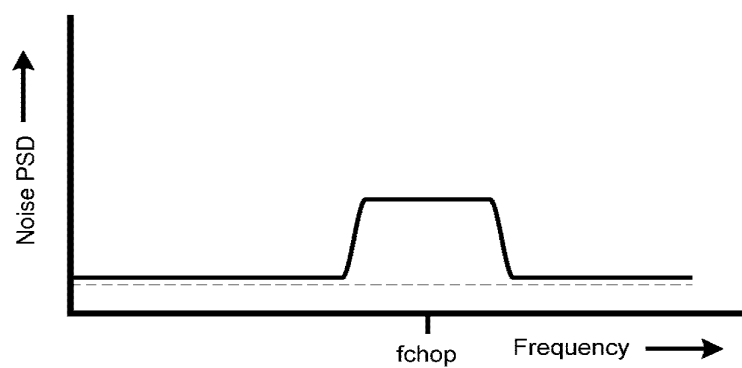


Fig. 10

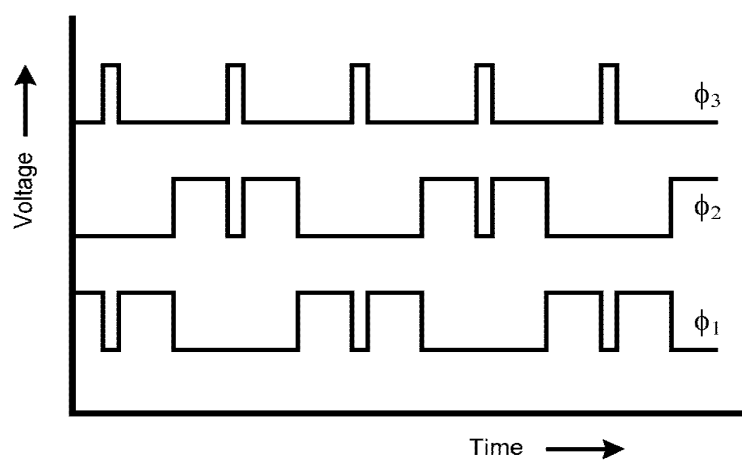


Fig. 14

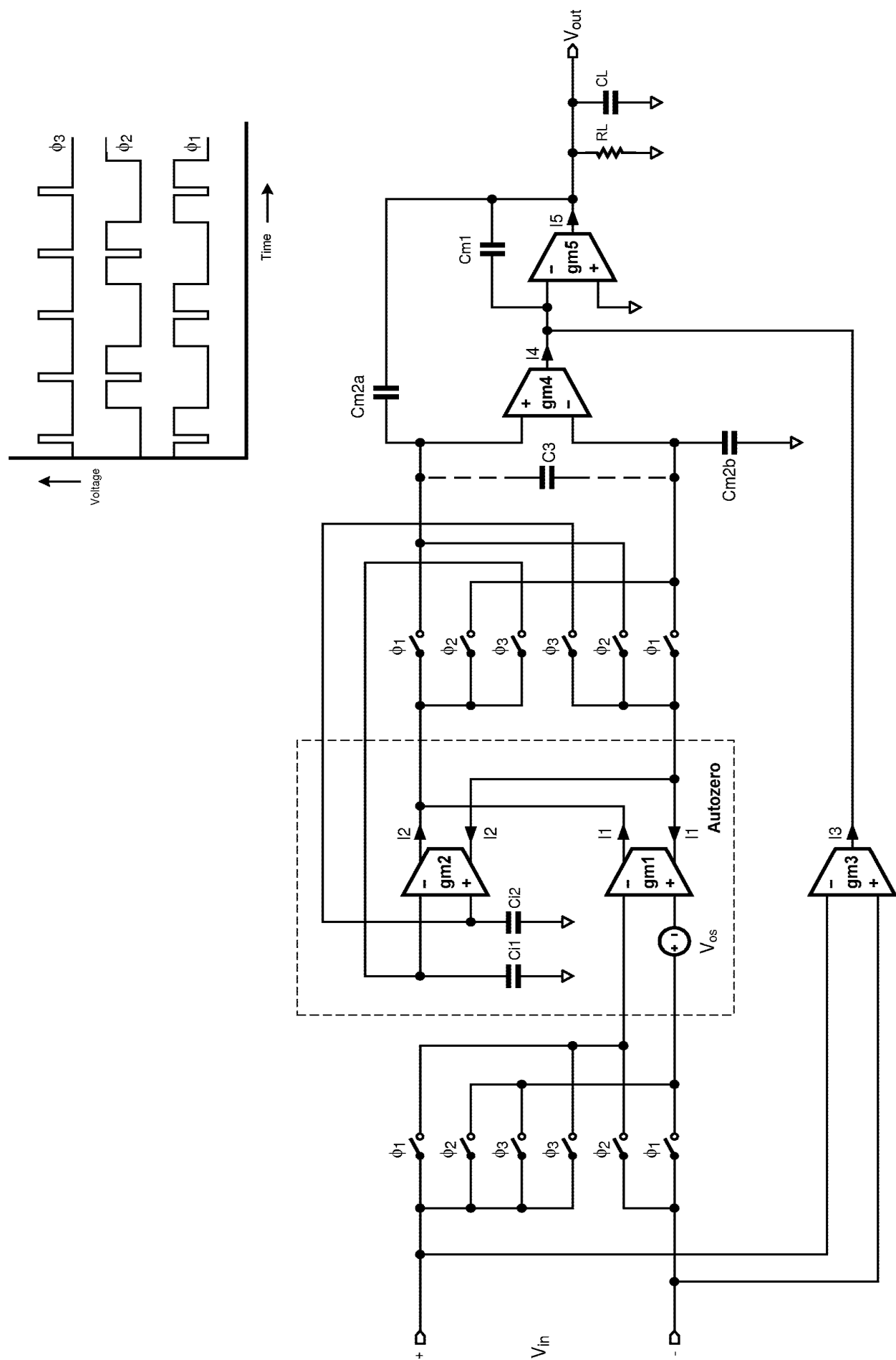


Fig. 11

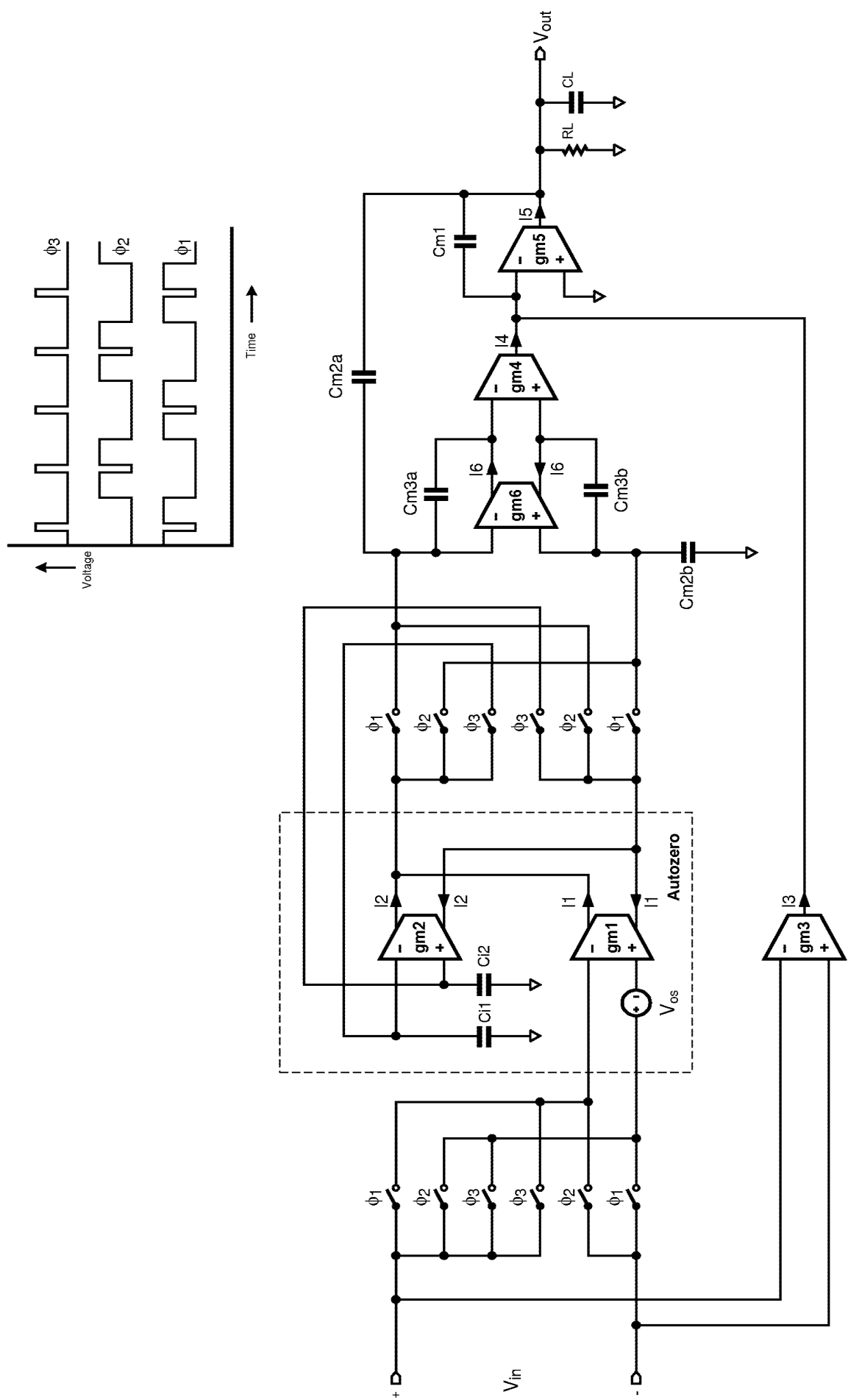


Fig. 12

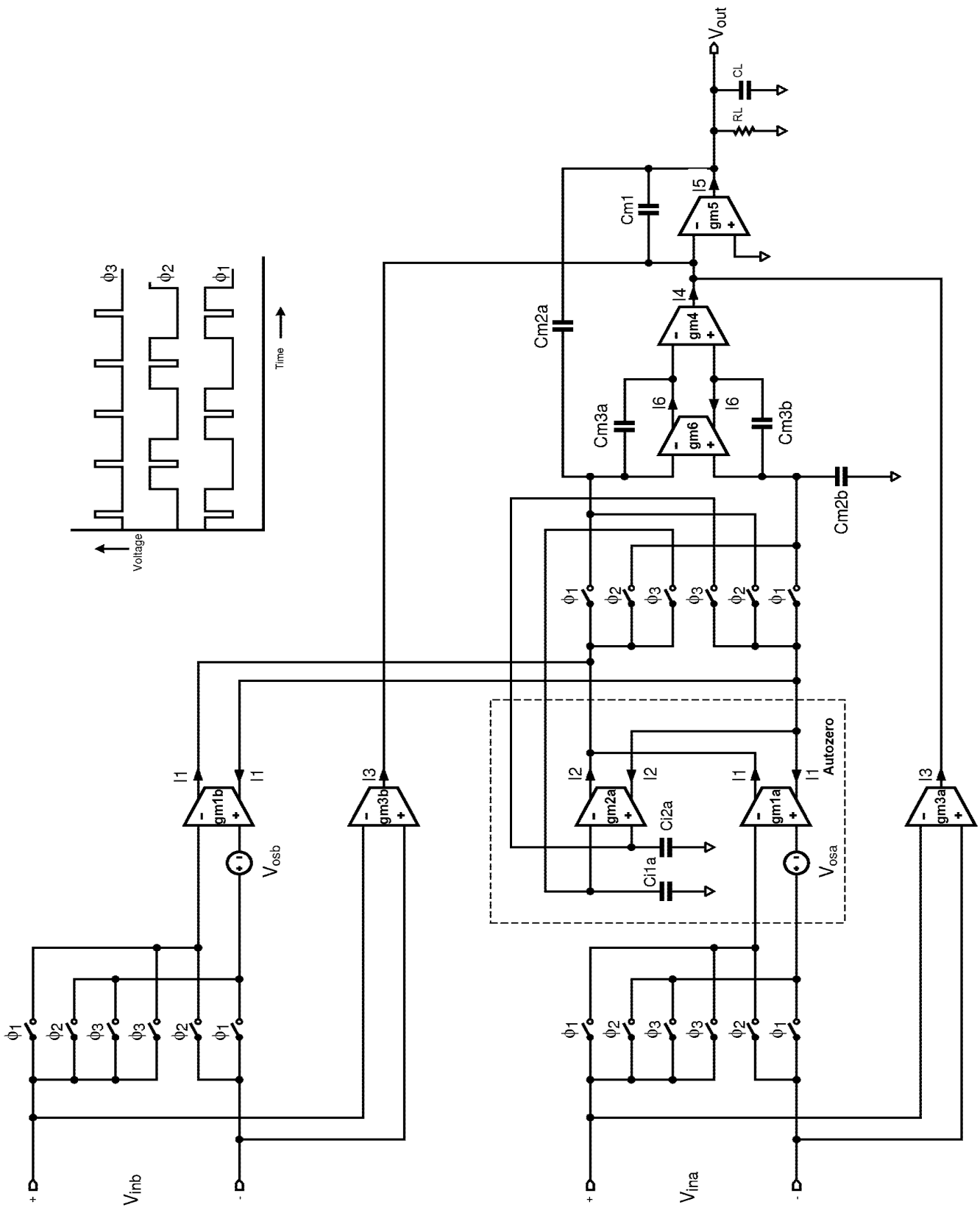


Fig. 13

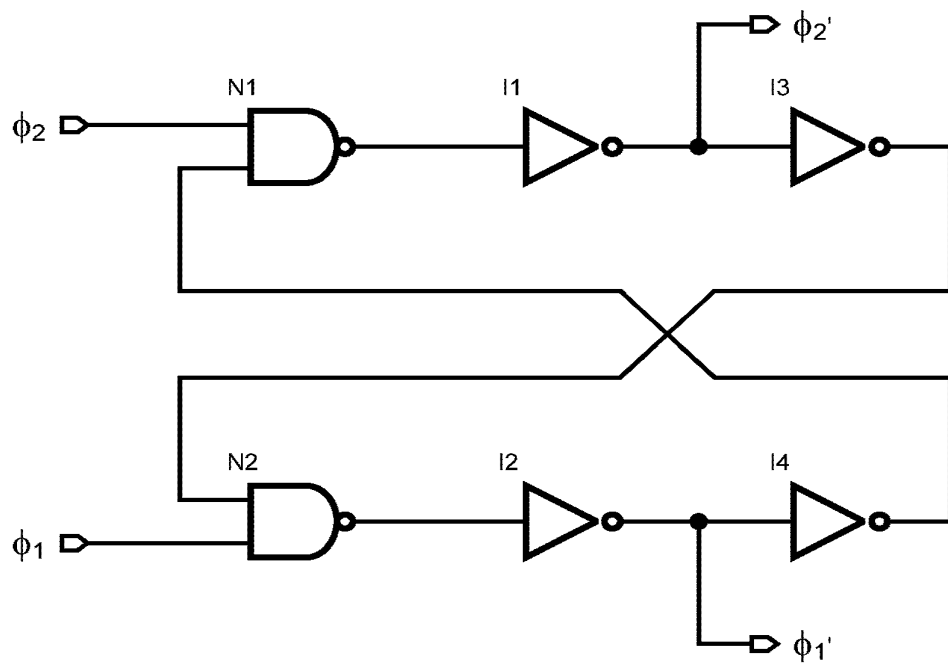


Fig. 15 (Prior Art)

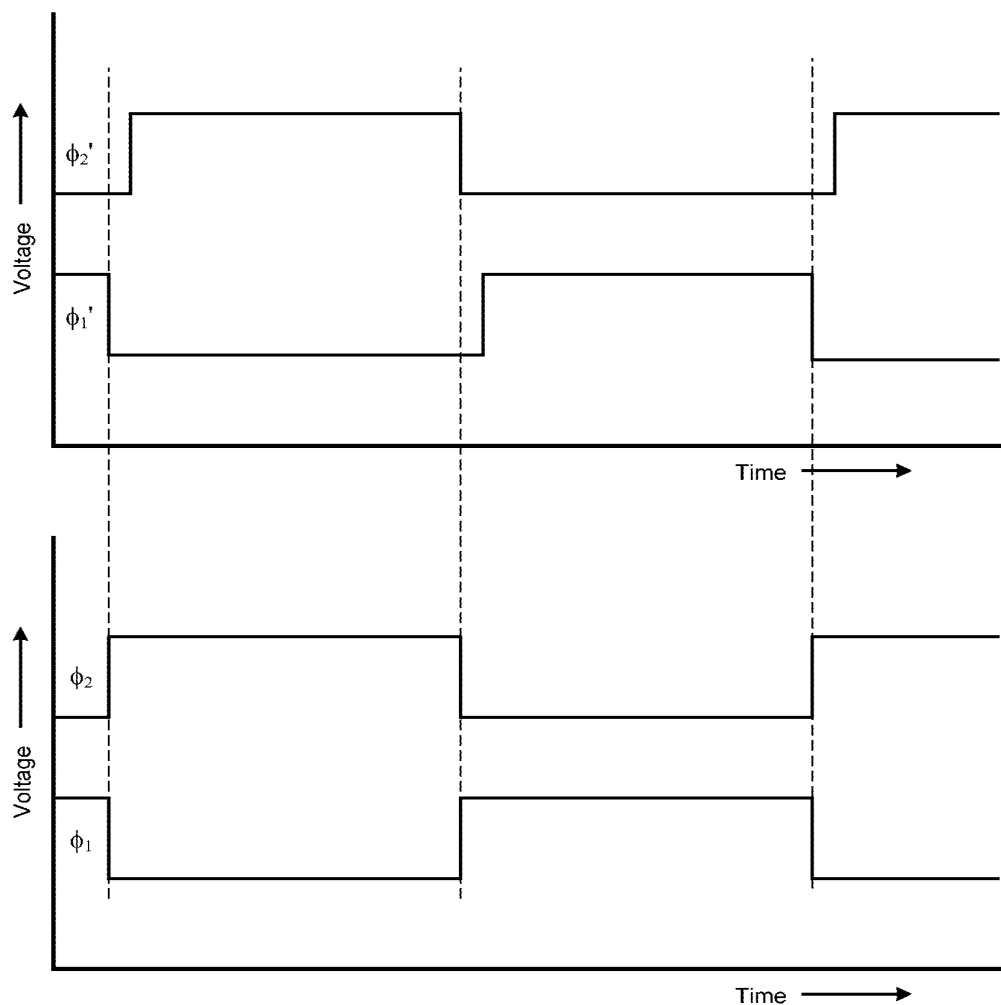


Fig. 16 (Prior Art)

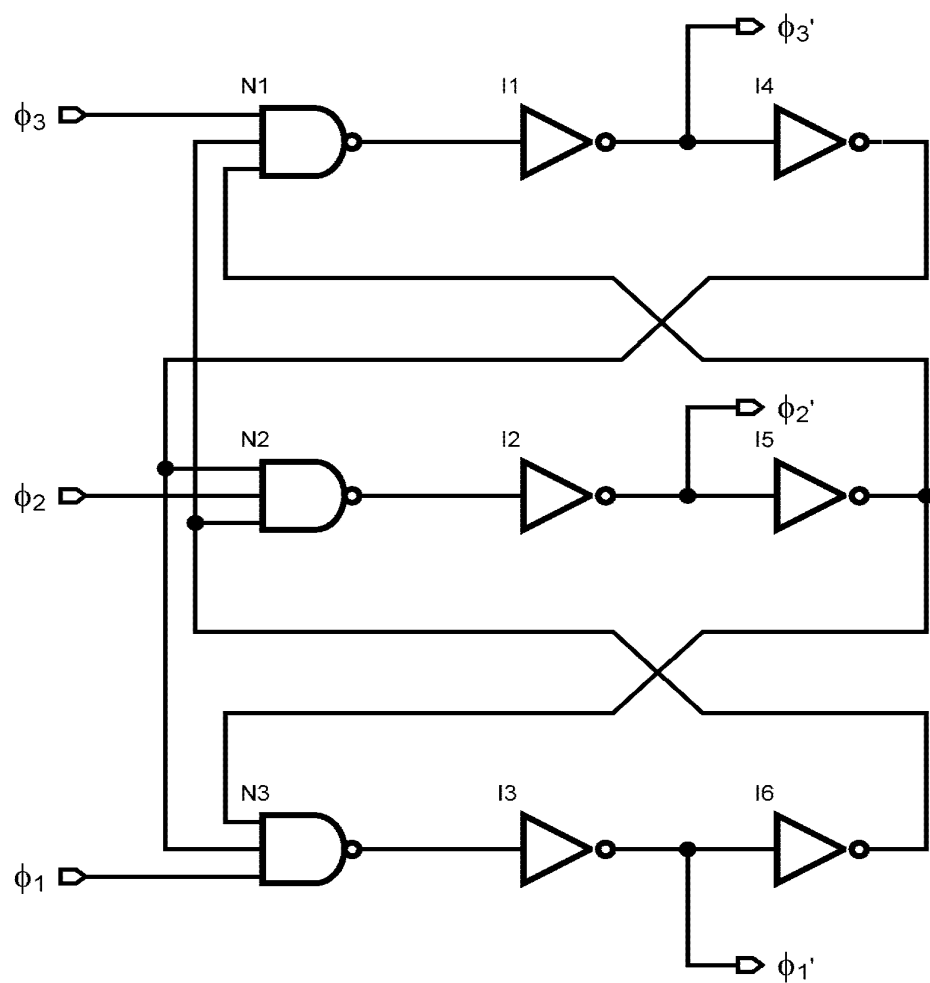


Fig. 17

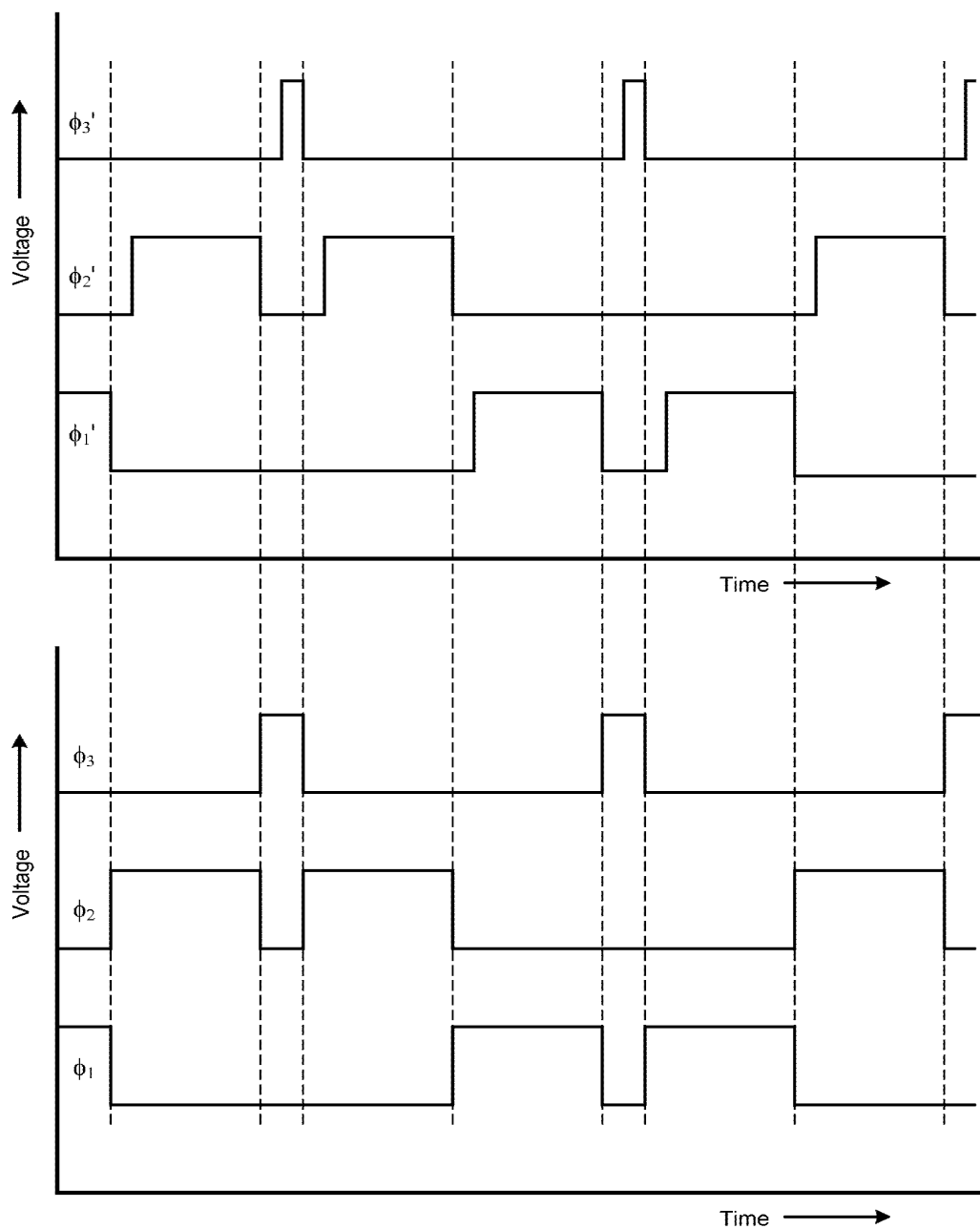


Fig. 18

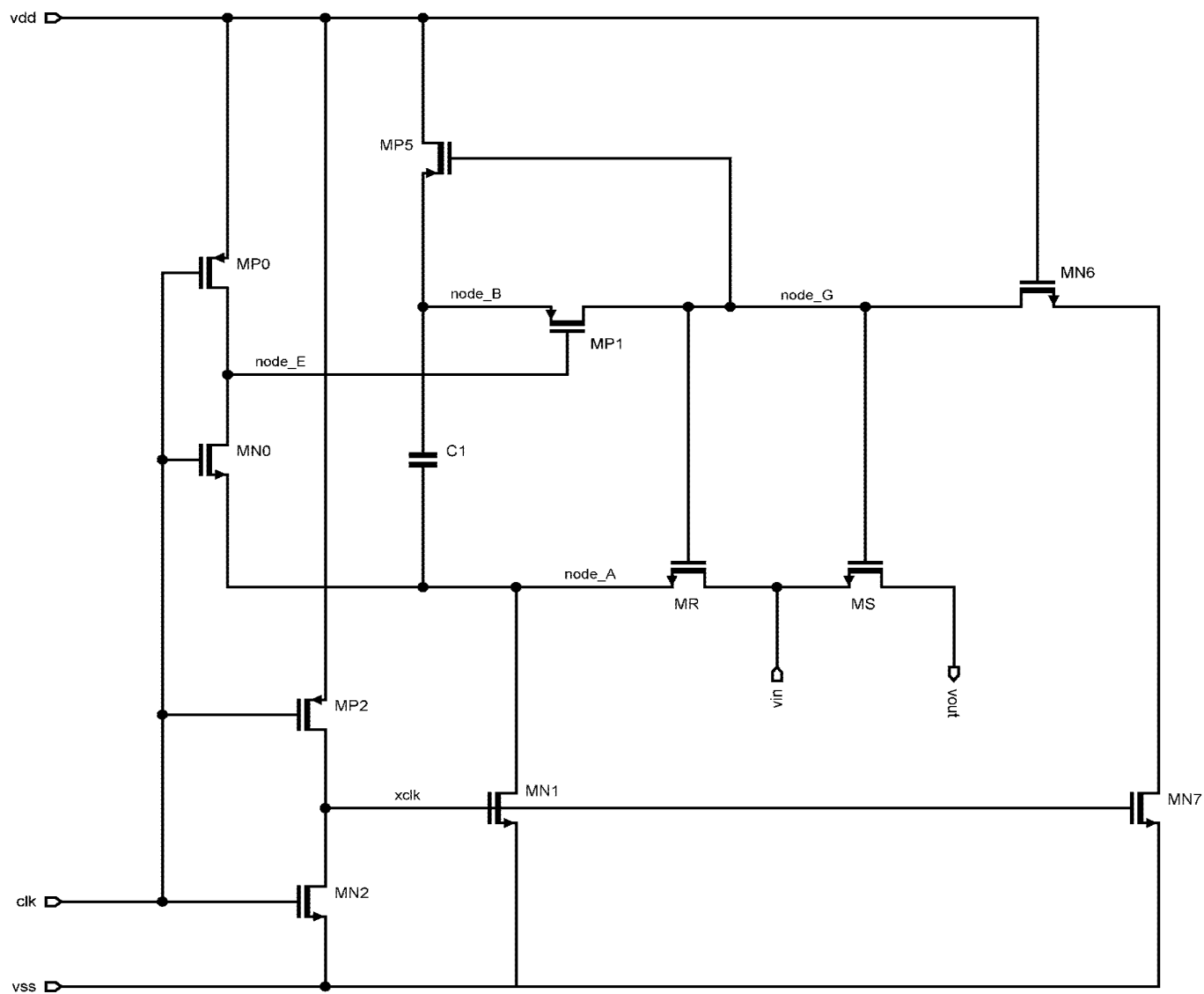
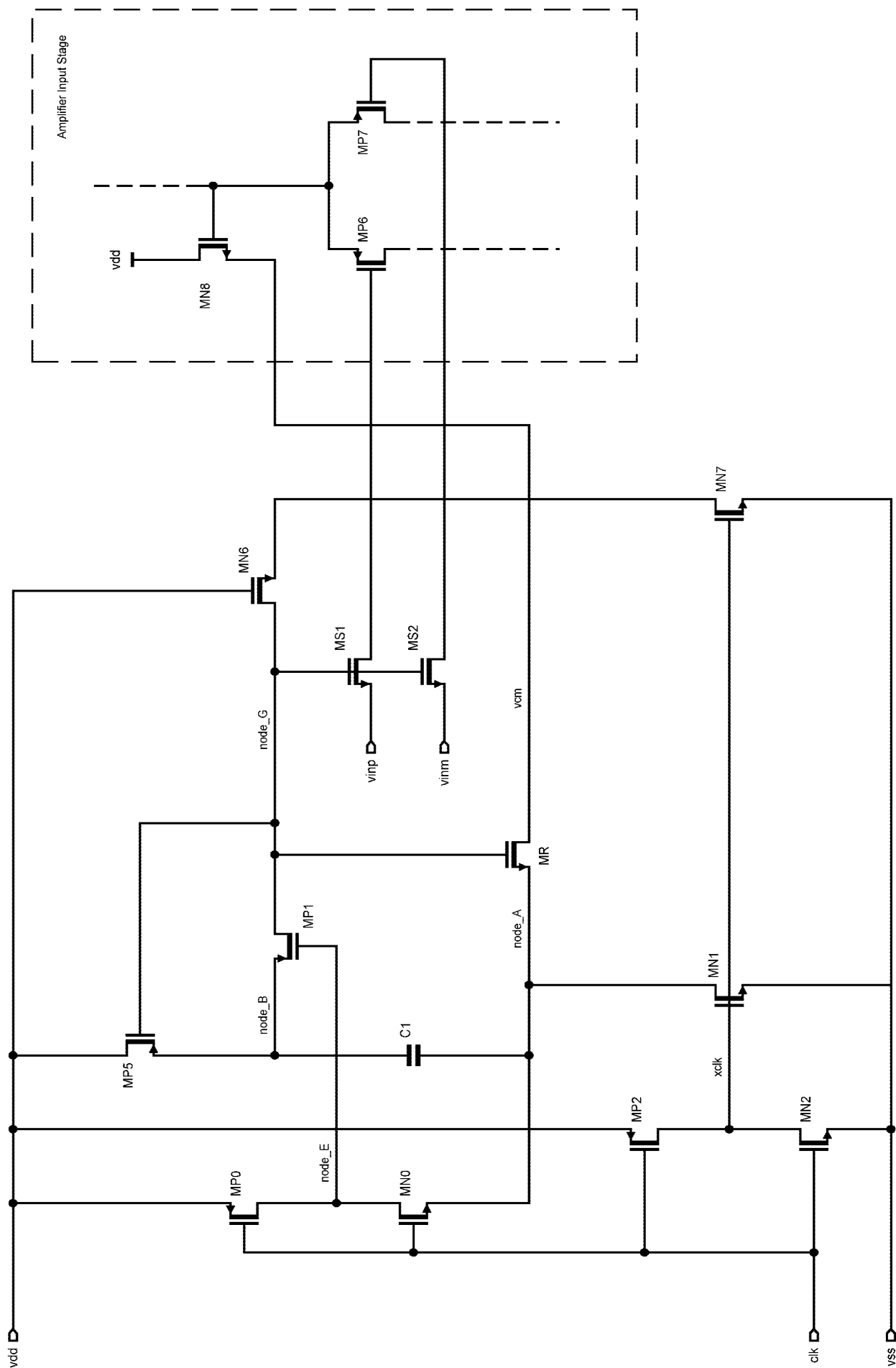


Fig. 19 (Prior Art)



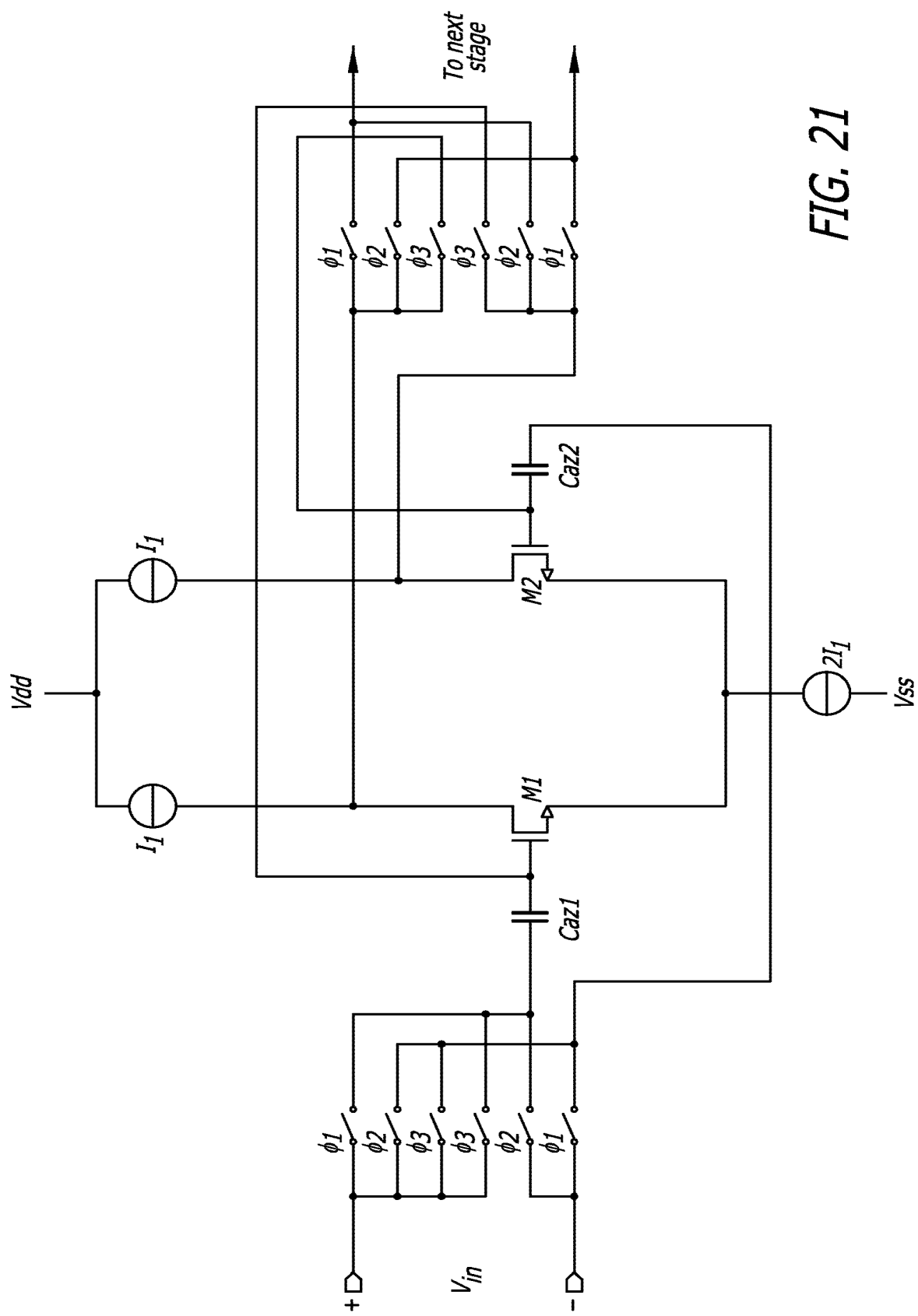


FIG. 21

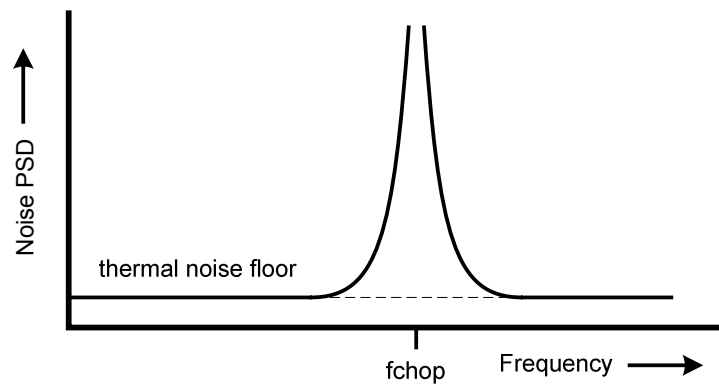


Fig. 2 (Prior Art)

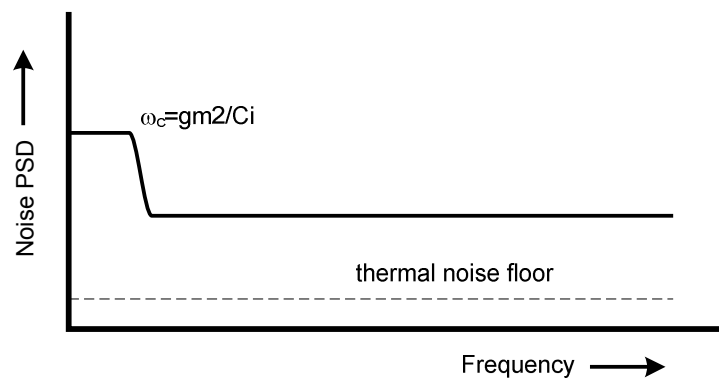


Fig. 4 (Prior Art)

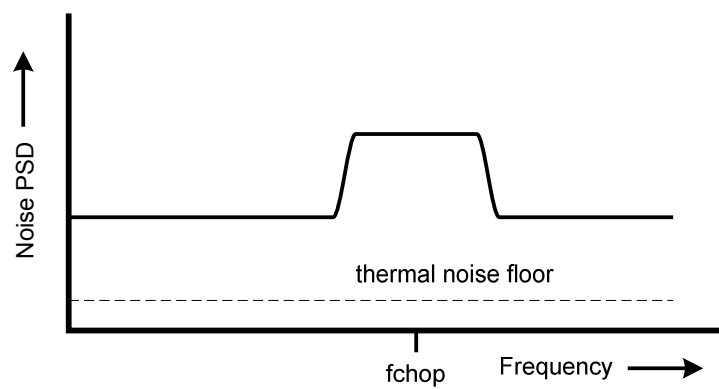


Fig. 6

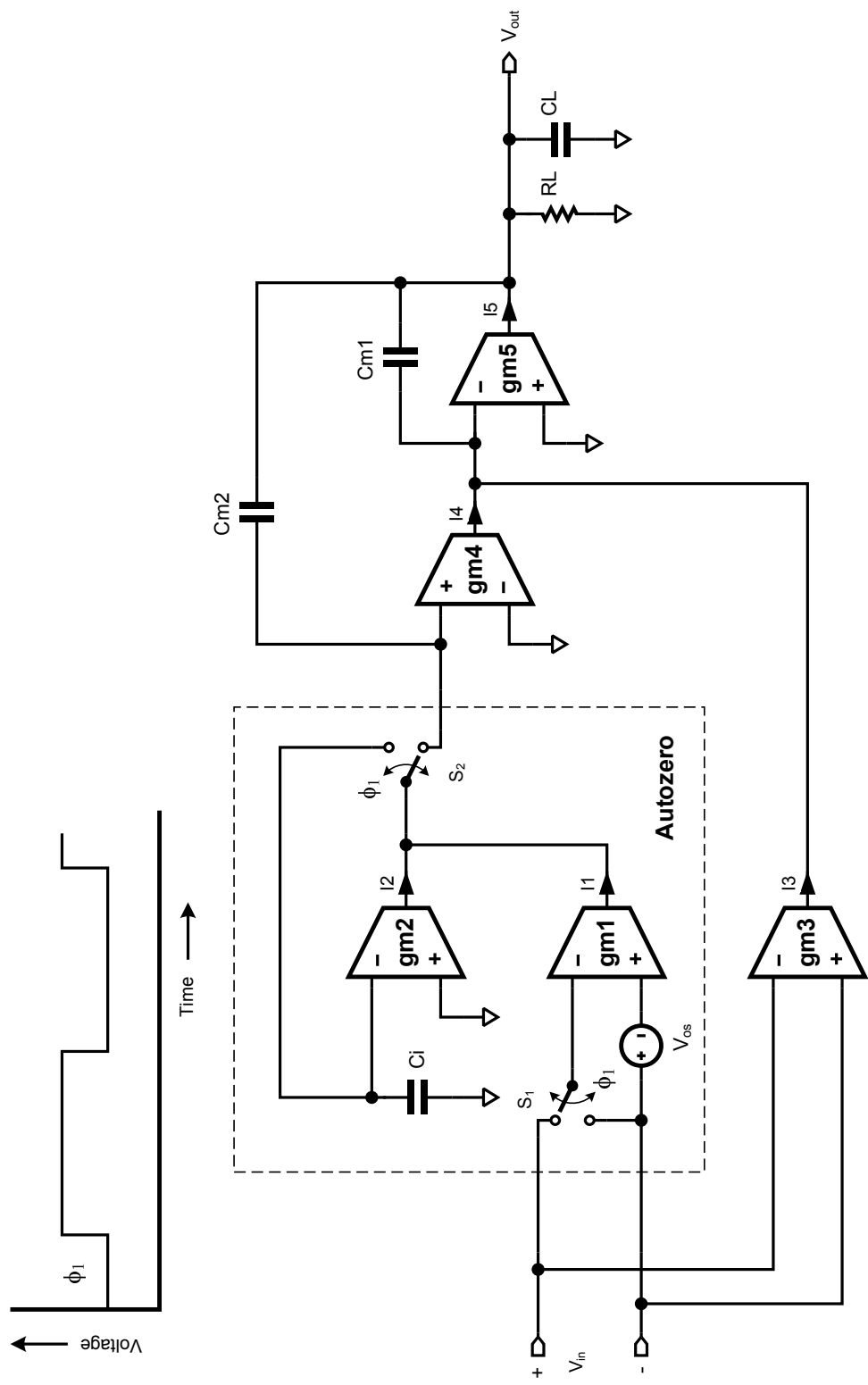


Fig. 3 (Prior Art)

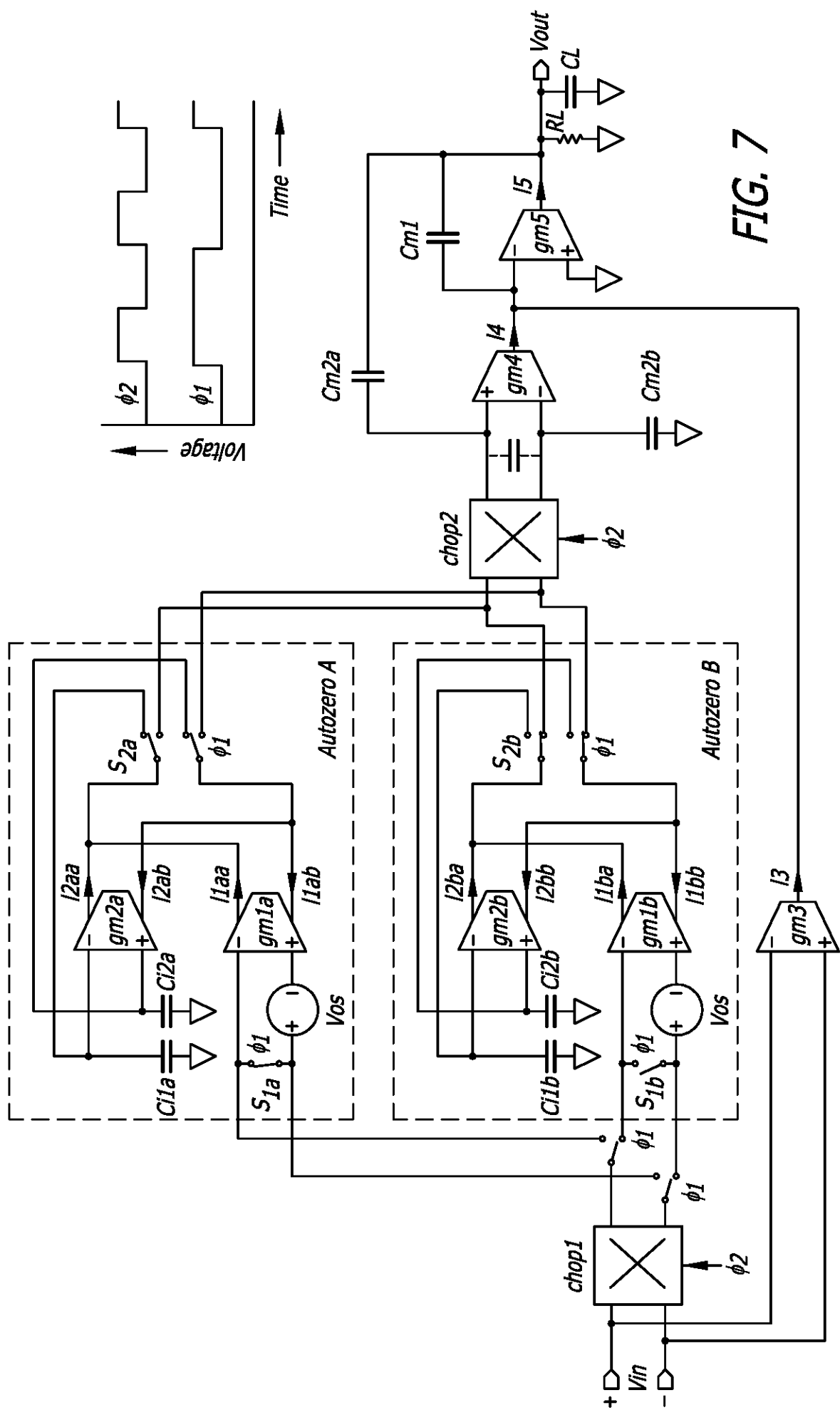


FIG. 7

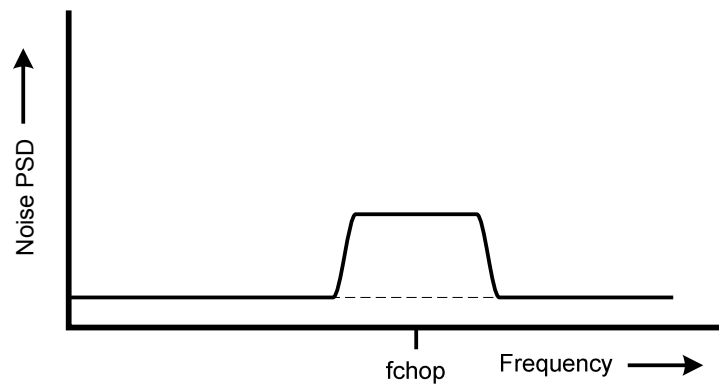


Fig. 8

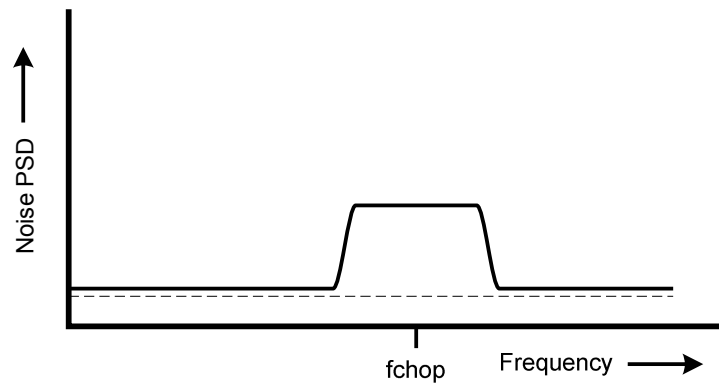


Fig. 10

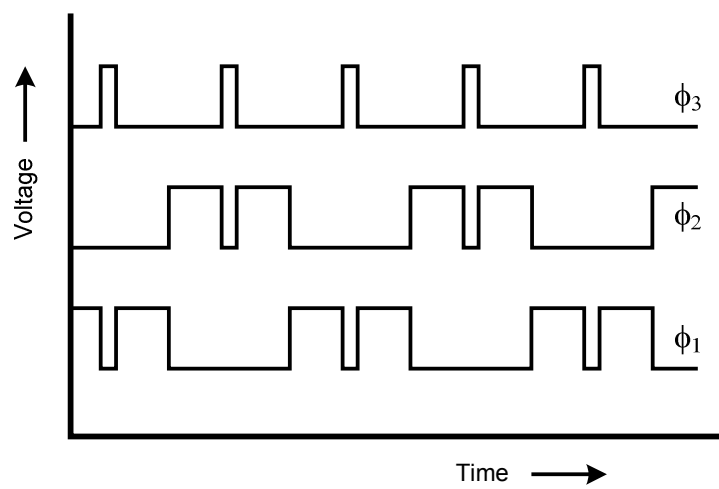


Fig. 14

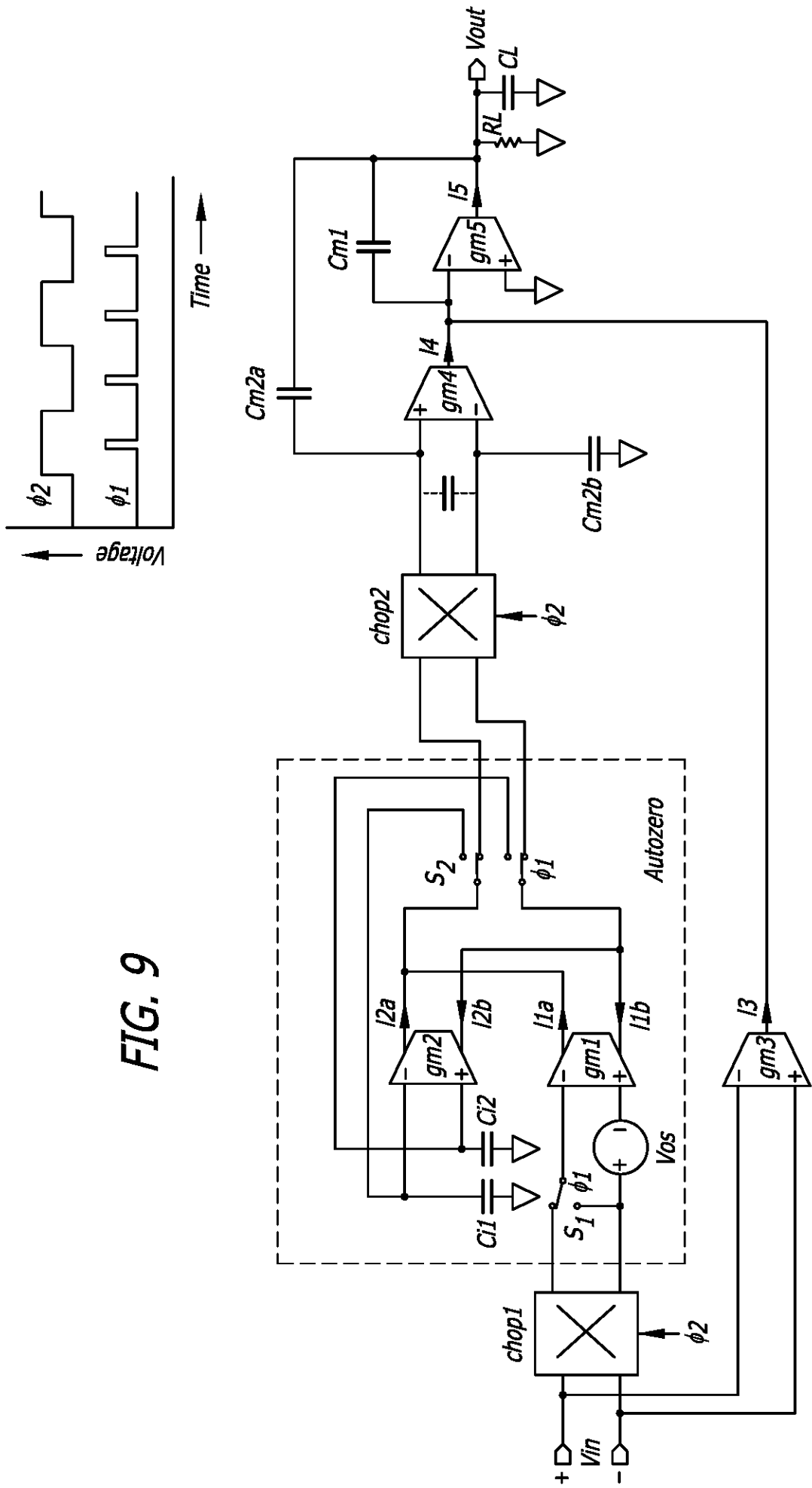


FIG. 9

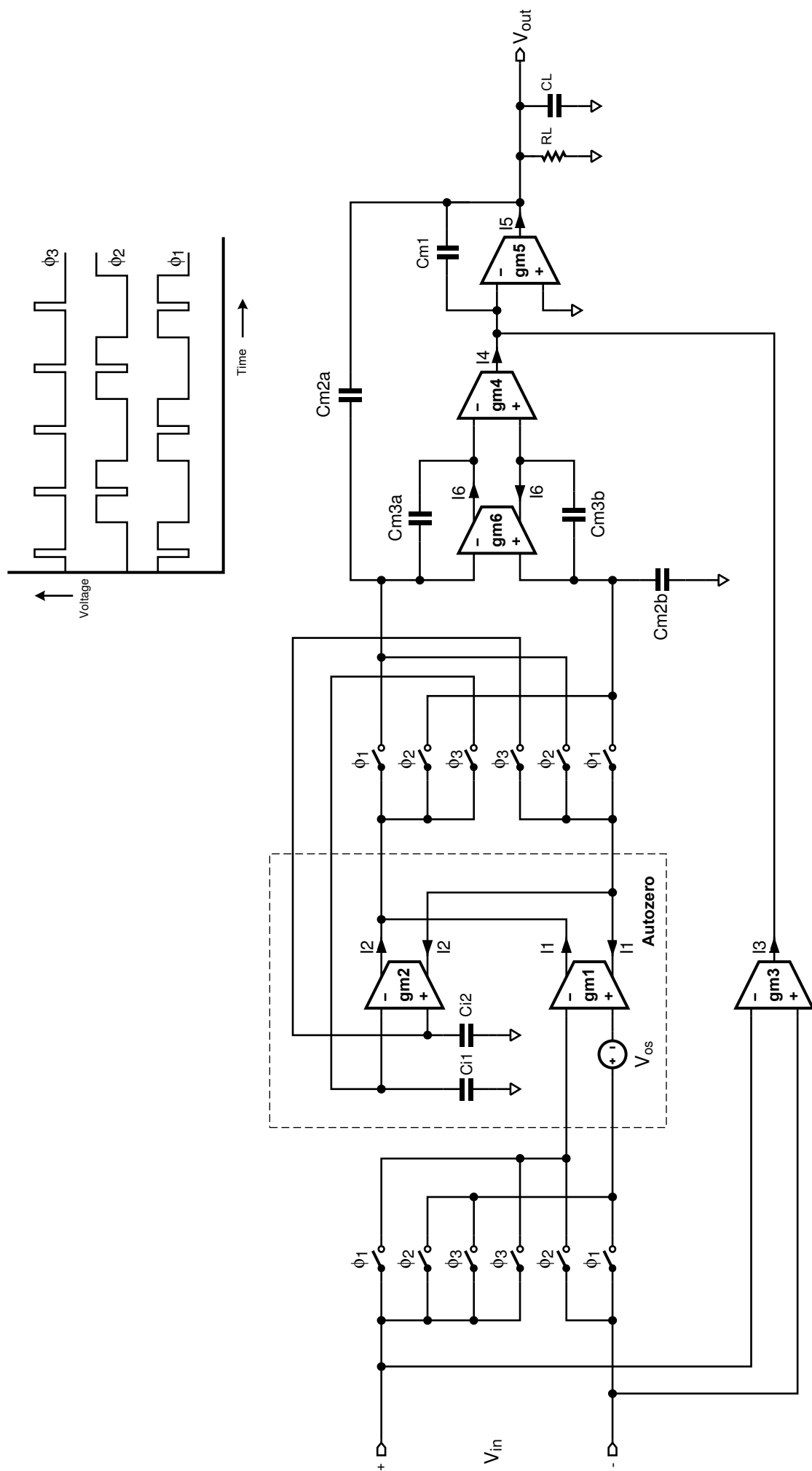


Fig. 12

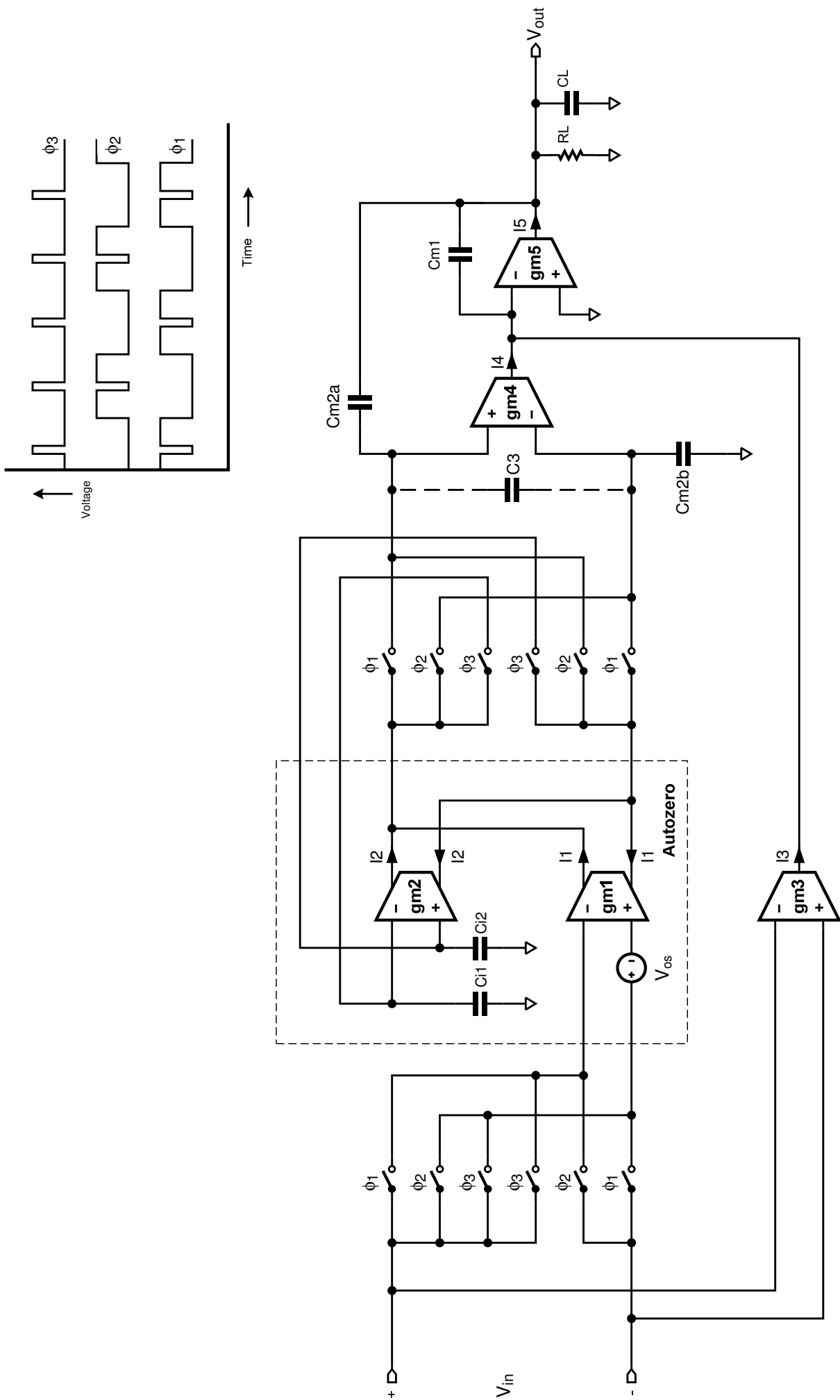


Fig. 11

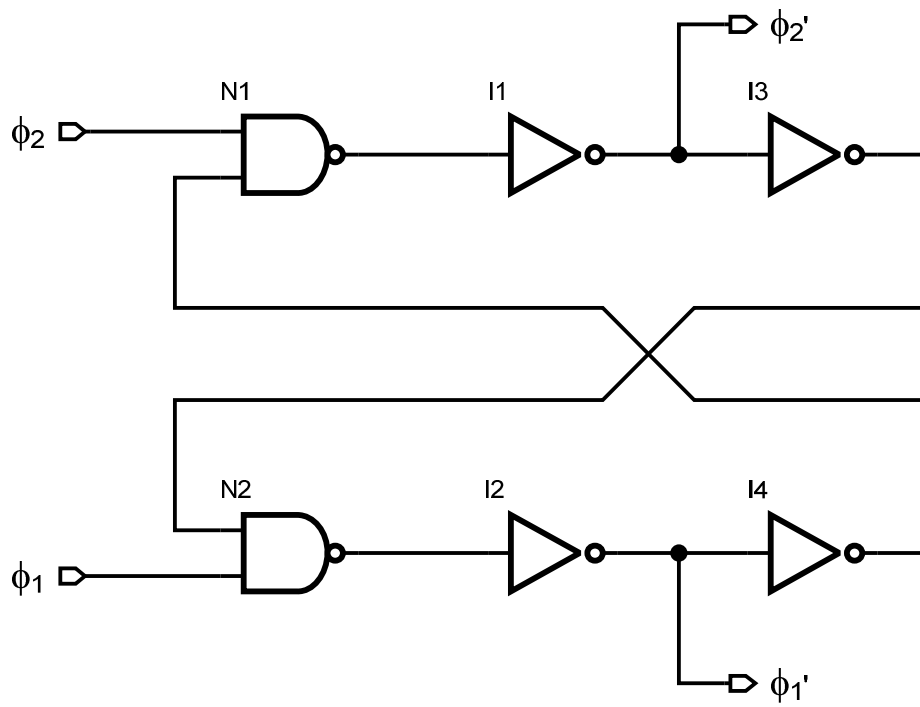


Fig. 15 (Prior Art)

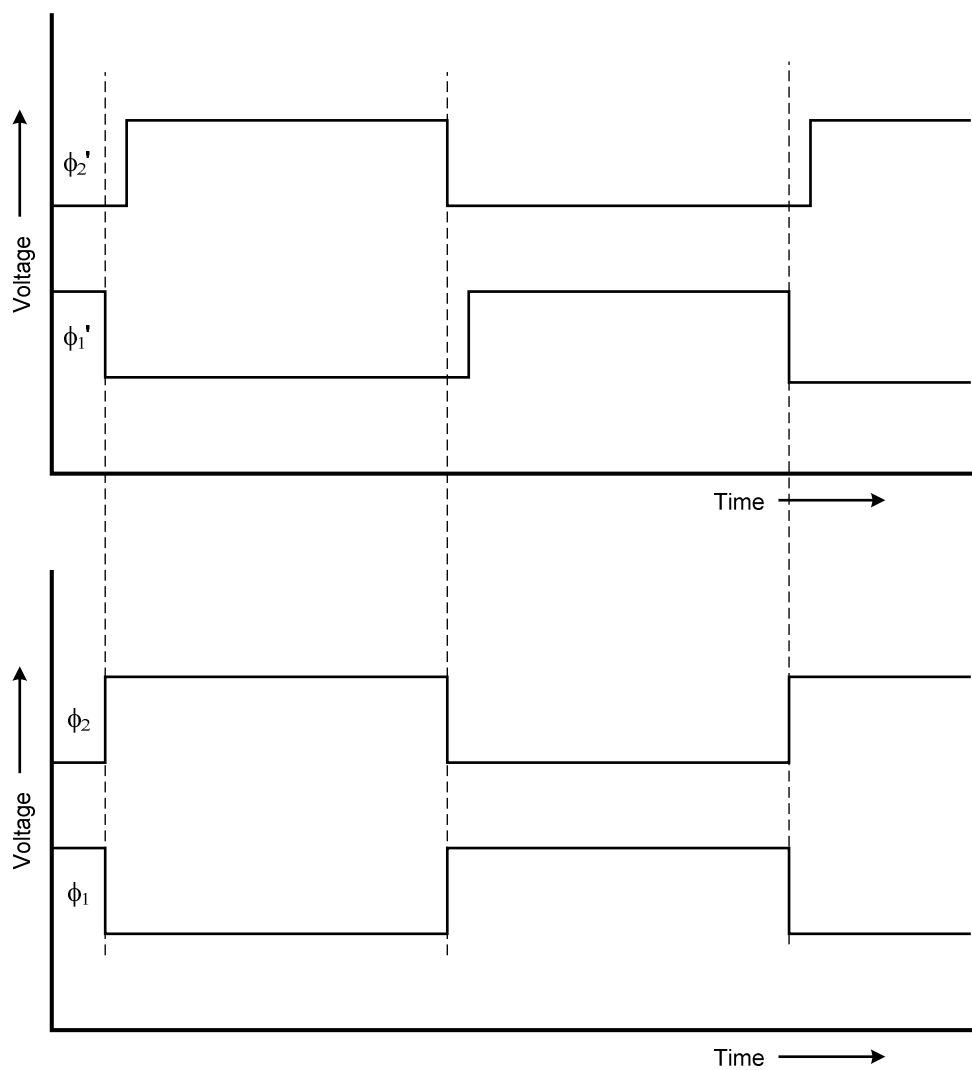


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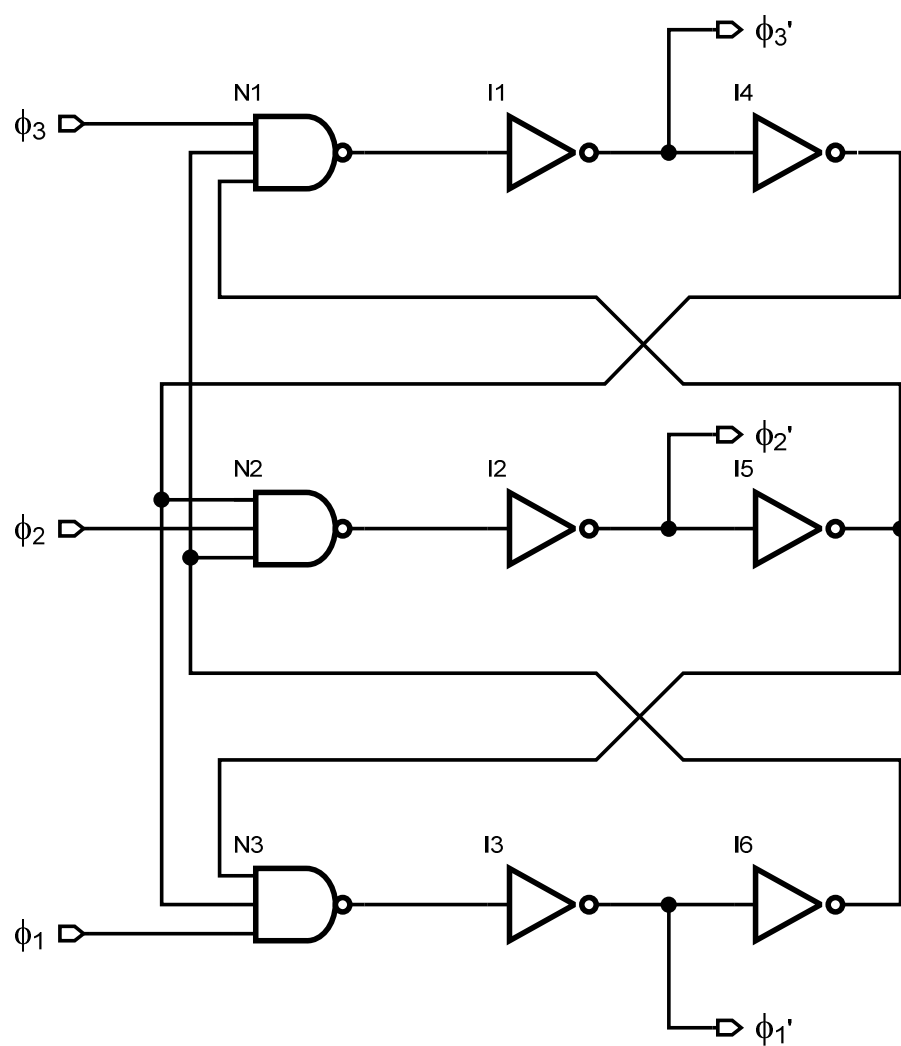


Fig. 17

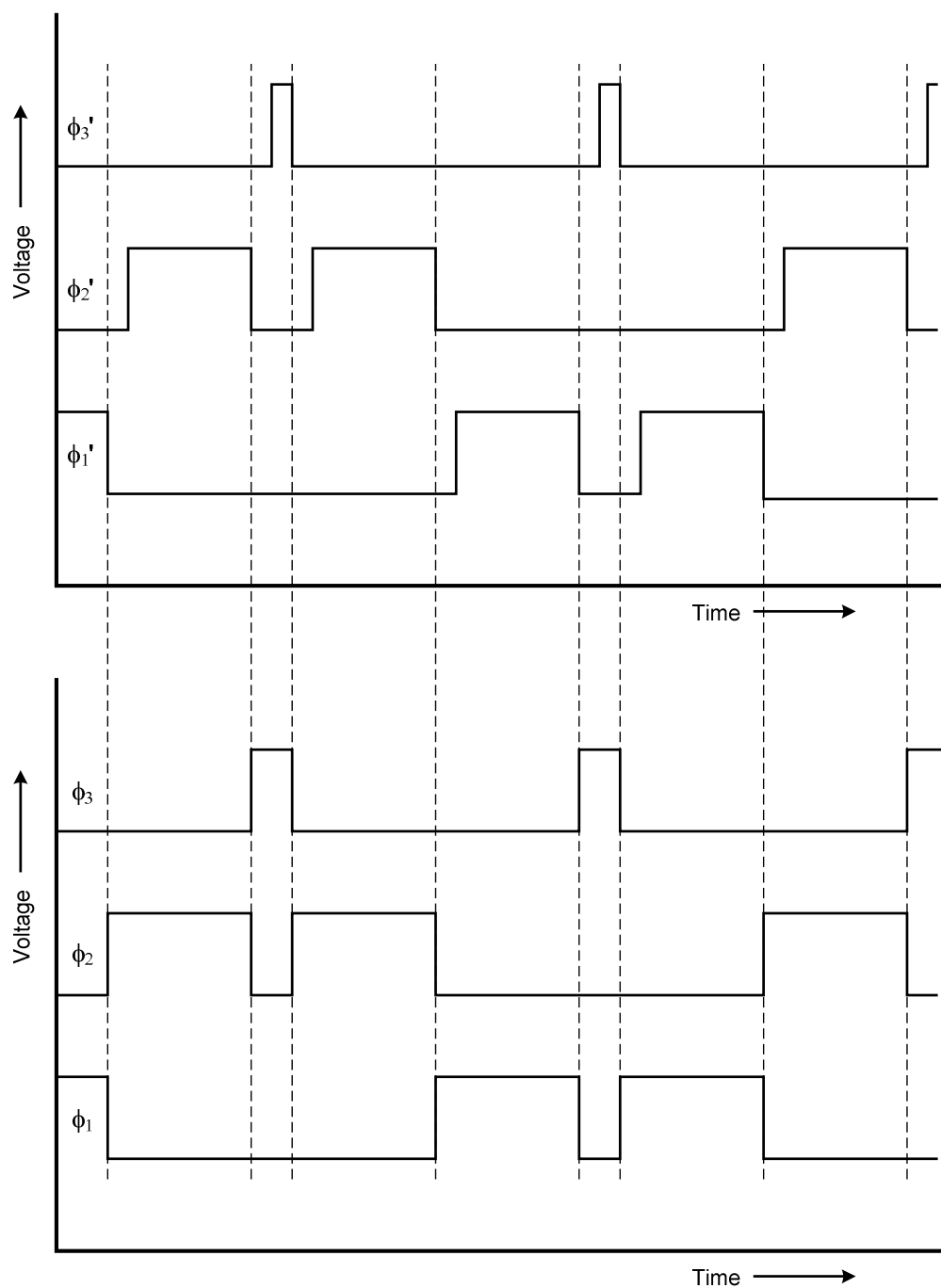


Fig. 18

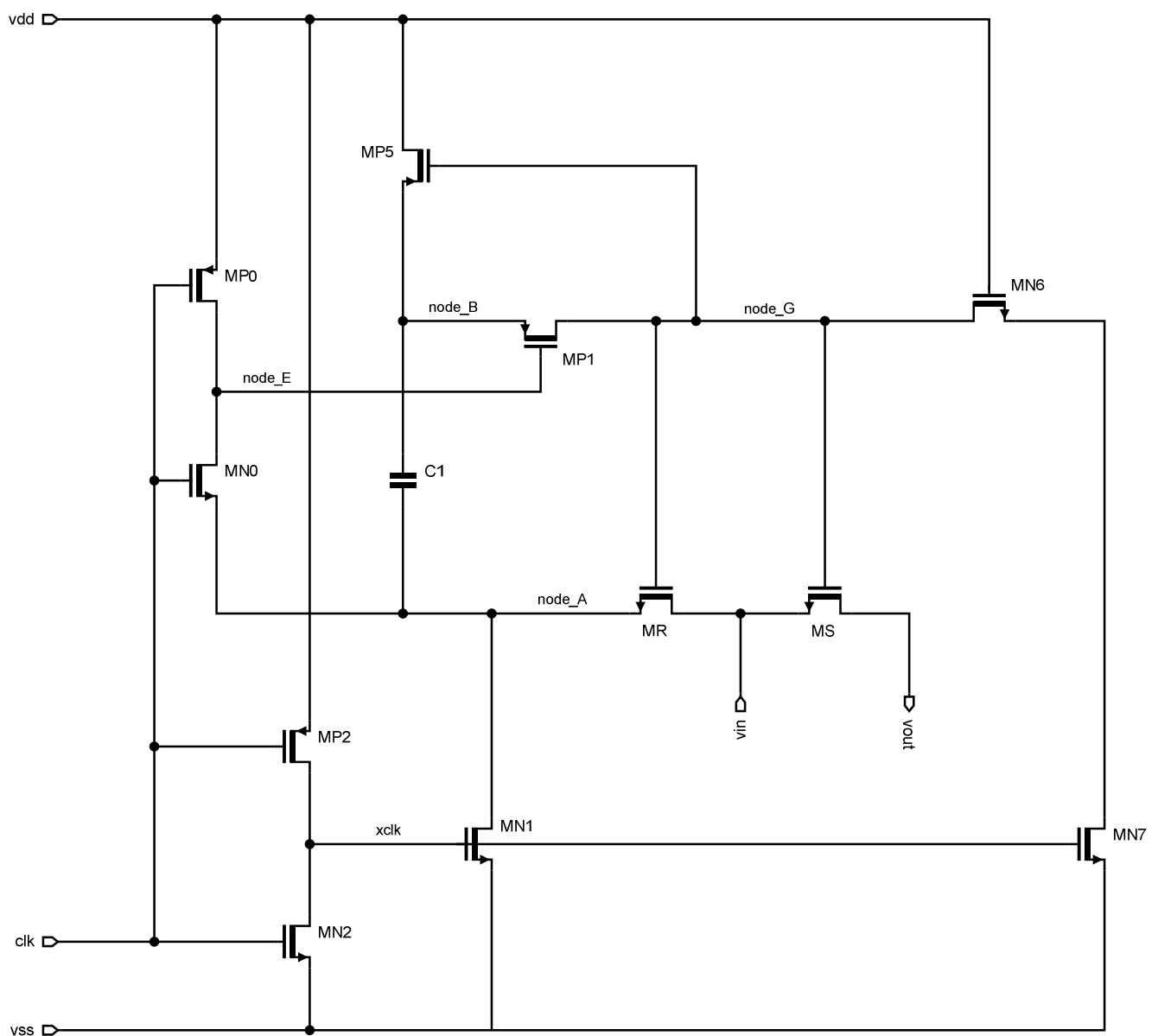
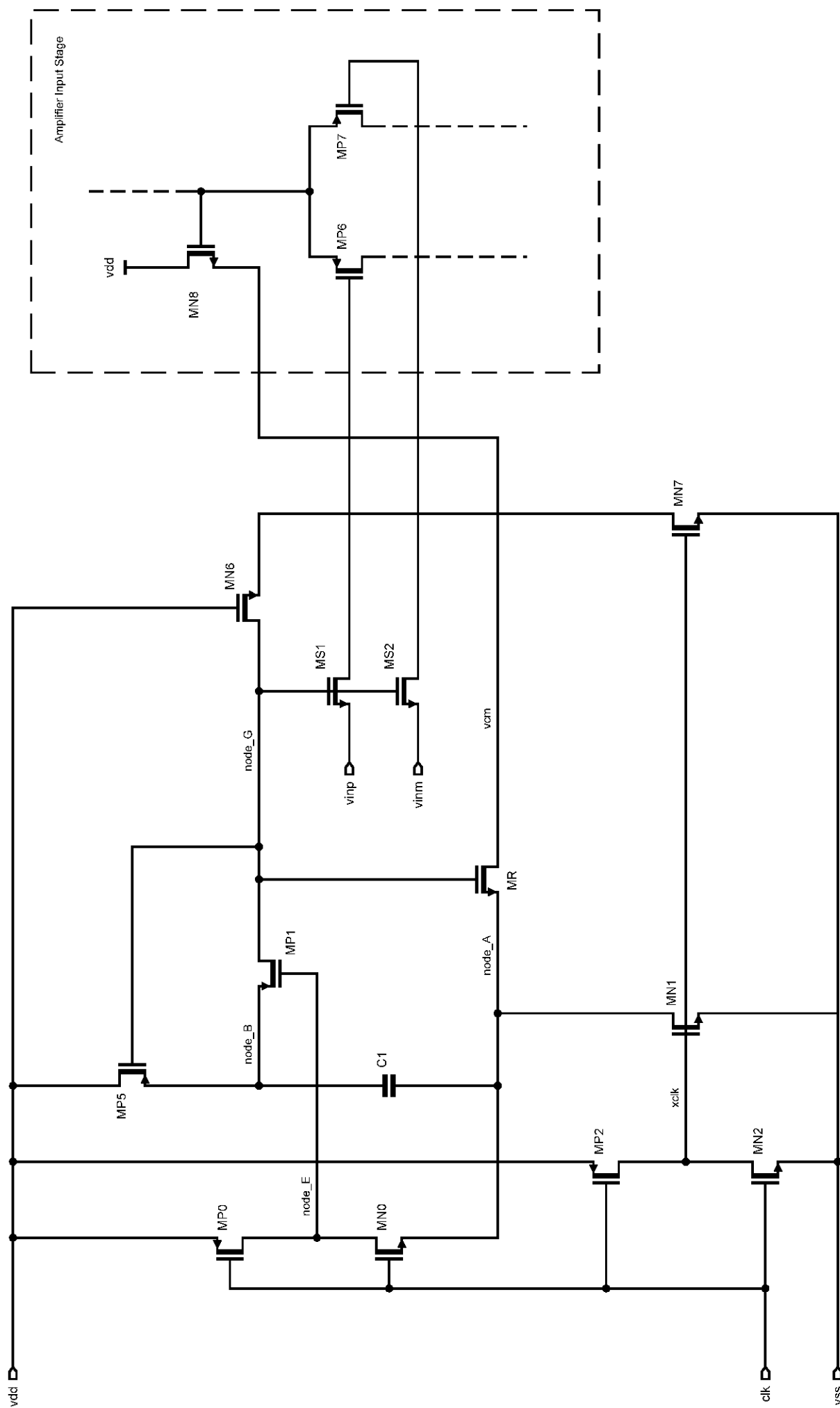
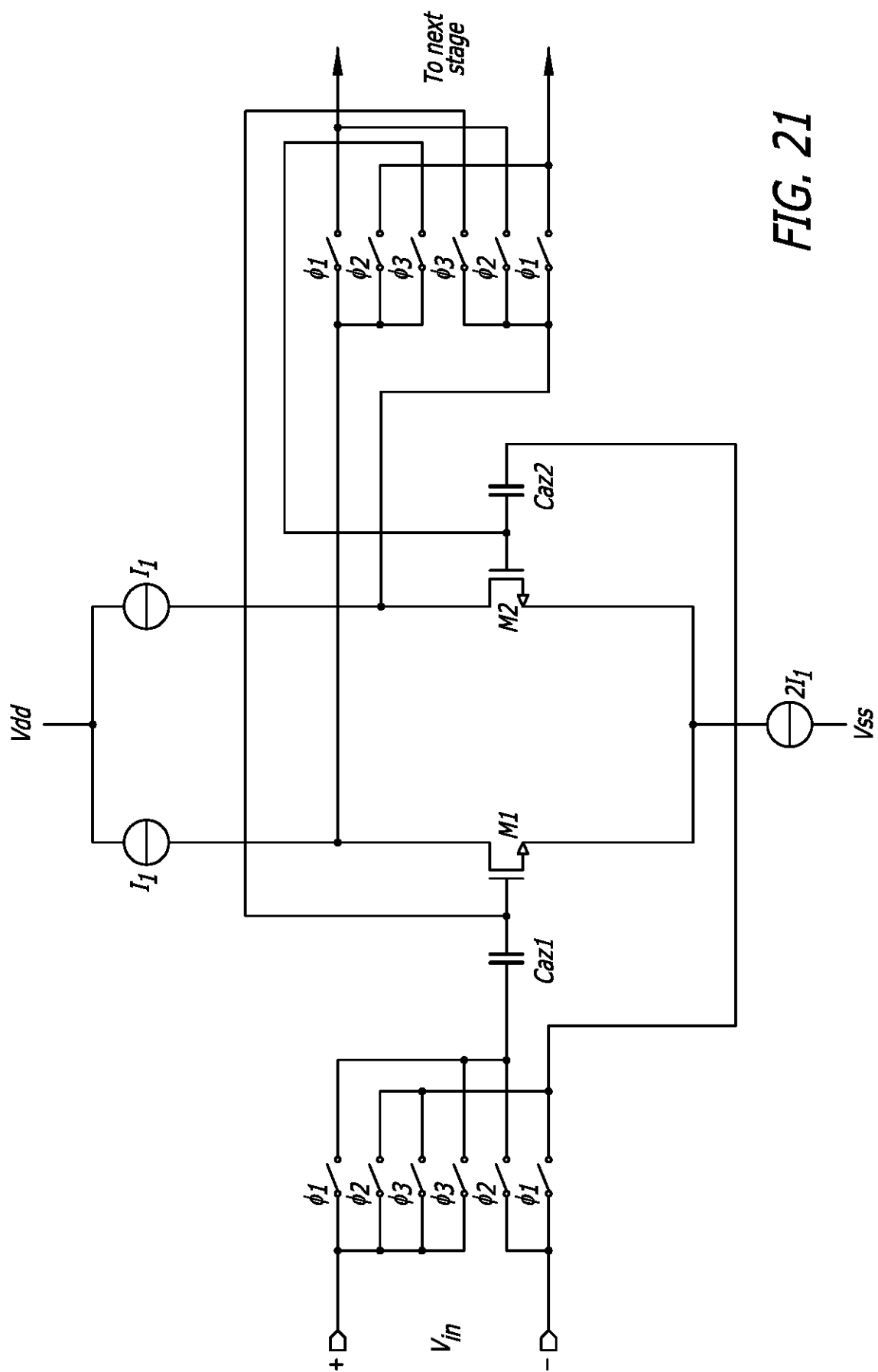


Fig. 19 (Prior Art)





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Application Number: 12464572 Document Date: 7/23/2009

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/464,572	05/12/2009	2817	2142	55123P376	36	4

CONFIRMATION NO. 1854

79124
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

UPDATED FILING RECEIPT



Date Mailed: 08/04/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Rudy G. H. Eschauzier, Bergschenhoek, NETHERLANDS;
Nico van Rijn, Katwijk, NETHERLANDS;

Assignment For Published Patent Application

NUMBER 14 B.V., Bergschenhoek, NETHERLANDS

Power of Attorney: The patent practitioners associated with Customer Number 79124

Domestic Priority data as claimed by applicant

Foreign Applications

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 05/20/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/464,572**

Projected Publication Date: 11/18/2010

Non-Publication Request: No

Early Publication Request: No

Title

Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers

Preliminary Class

330

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,572	05/12/2009	Rudy G. H. Eschauzier	55123P376	1854
79124	7590	09/21/2010		
MAXIM/BSTZ Blakely Sokoloff Taylor & Zafman LLP 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085-4040			EXAMINER NGUYEN, KHIEM D	
			ART UNIT	PAPER NUMBER
			2817	
			MAIL DATE	DELIVERY MODE
			09/21/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/464,572	ESCHAUZIER ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☐ Responsive to communication(s) filed on _____.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-36 is/are pending in the application.
4a) Of the above claim(s) 34-36 is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-6 and 24-28 is/are rejected.
7) ☒ Claim(s) 7-23 and 29-33 is/are objected to.
8) ☒ Claim(s) 34-36 are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 23 July 2009 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)	4) ☐ Interview Summary (PTO-413)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) ☒ Information Disclosure Statement(s) (PTO/SB/08)	5) ☐ Notice of Informal Patent Application
Paper No(s)/Mail Date <u>05/20/2009</u> .	6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. During a telephone conversation with Roger Blakely on 8-27-2010 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-33. Affirmation of this election must be made by applicant in replying to this Office action. Claims 34-36 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.
2. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-33, drawn to a chopper amplifier and auto-zero circuitry, classified in class 330, subclass 9.
 - II. Claims, 34, 35, 36, drawn to logic circuit and switches and clock signal, classified in class 326, subclass 99.
3. Inventions Group I and Group II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because Group I discloses an amplifier system comprising differential amplifier and chopper and auto-zero circuitry. The subcombination has separate utility such as Group II discloses a circuit comprising logic and switches circuit.

Because of these inventions are distinct for the reason given above and the search for Group II is not required for Group I, restriction for examination purpose as indicated is proper

The examiner has required restriction between combination and subcombination inventions. Where applicant elects a subcombination, and claims thereto are subsequently found allowable, any claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

4. Restriction for examination purposes as indicated is proper because all these inventions listed in this action are independent or distinct for the reasons given above and there would be a serious search and/or examination burden if restriction were not required because at least the following reason(s) apply:

- (a) the inventions have acquired a separate status in the art in view of their different classification;
- (b) the inventions have acquired a separate status in the art due to their recognized divergent subject matter;

- (c) the inventions require a different field of search (for example, searching different classes/subclasses or electronic resources, or employing different search queries);
- (d) the prior art applicable to one invention would not likely be applicable to another invention;
- (e) the inventions are likely to raise different non-prior art issues under 35 U.S.C. 101 and/or 35 U.S.C. 112, first paragraph.

Applicant is advised that the reply to this requirement to be complete must include (i) an election of a invention to be examined even though the requirement may be traversed (37 CFR 1.143) and (ii) identification of the claims encompassing the elected invention.

The election of an invention may be made with or without traverse. To reserve a right to petition, the election must be made with traverse. If the reply does not distinctly and specifically point out supposed errors in the restriction requirement, the election shall be treated as an election without traverse. Traversal must be presented at the time of election in order to be considered timely. Failure to timely traverse the requirement will result in the loss of right to petition under 37 CFR 1.144. If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

If claims are added after the election, applicant must indicate which of these claims are readable upon the elected invention.

Should applicant traverse on the ground that the inventions are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the inventions to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1 & 3 are rejected under 35 U.S.C. 102(b) as being anticipated by Huijsing et al. (USP 6,734,723 B2).

Huijsing et al. disclose (e.g. fig. 3) having operational amplifier system, a circuit comprising an amplifier A1 (i.e. a first differential amplifier); Choppers S1 and S2 (i.e. first and second choppers) for chopping the input and the output of the first differential amplifier A1, respectively; Autozero amplifier Gm3 and choppers S3, S4, and integrator

Gm4 form an autozero circuitry coupled to the first differential amplifier for autozeroing the first differential amplifier; and wherein the autozero circuitry operating at a first frequency and the choppers operating at a second frequency unequal to the first frequency (see column 5, second paragraph, frequency f2 and f1 could be identical but does not have to be) and an amplifier Gm3 having differential inputs coupled to the first and second differential inputs of the amplifier system and an output coupled to the output amplifier.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claims 2, 4-6 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huijsing et al.

Huijsing et al. teach all of the limitations as discussed above except for the second frequency being twice the first frequency, and the first and second frequencies each have a 50% duty cycle or the first frequency is twice the second frequency, the second frequency having a 50% duty cycle and the first frequency has a duty cycle of less than 50% or the first frequency has a duty cycle of not more than 25% or the ratio of the frequencies being two to one or duty cycle of less than one half or duty cycle of not more than one-quarter . However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the circuit wherein the second frequency being twice the first frequency and the first and second frequencies each have a 50% duty cycle or the first frequency is twice the second frequency, since this could be achieved through routine experimentation and the effective of the value on the circuit would have known it would be obvious to optimize such as a circuit to achieve the claimed invention.

Allowable Subject Matter

11. Claims 7-23 & 29-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

An output amplifier having an input coupled to an output of the second chopper and third switch pluralities of open and closed switches are do not disclosed by Huijsing et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571)270-3941. The examiner can normally be reached on Mon-Fri 8:00AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KDN

/Robert Pascal/
Supervisory Patent Examiner, Art Unit 2817

Notice of References Cited	Application/Control No. 12/464,572		Applicant(s)/Patent Under Reexamination ESCHAUZIER ET AL.	
	Examiner Khiem D. Nguyen		Art Unit 2817	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,734,723 B2	05-2004	Huijsing et al.	330/9
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Complete if Known	
	Application Number	12/464,572
	Filing Date	05/12/2009
	First Named Inventor	Rudy G.H. Eschauzier
	Group Art Unit	
	Examiner Name	
Sheet 1 of 1		Attorney Docket No: 55123P376

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
/K.N./		DESSOUKY, MOHAMED , et al., "Very Low-Voltage Digital-Audio ΔΣ Modulator with 88-dB Dynamic Range Using Local Switch Bootstrapping", <u>IEEE Journal of Solid-State Circuits</u> , Vol. 36, No. 3, (March 2001), Pgs. 349-355	
/K.N./		ENZ, CHRISTIAN C., et al., "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", <u>Proceedings of the IEEE</u> , Vol. 84, No. 11, (November 1996), Pgs. 1584-1614	
/K.N./		ESCHAUZIER, RUDY G., et al., "Frequency Compensation Techniques for Low-Power Operational Amplifiers", Section 6.1, Springer, (1995)	
/K.N./		ESCHAUZIER, RUDY G., et al., "Frequency Compensation Techniques for Low-Power Operational Amplifiers", Section 6.3, Springer, (1995)	
/K.N./		HUIJSING, JOHAN H., "Operational Amplifiers, Theory and Design", Kluwer Academic Publishers, (2001), Pgs. 52-53	
/K.N./		WESTE, NEIL H., et al., "Principles of CMOS VLSI Design, A Systems Perspective, Second Edition", Section 5.5.10, Addison-Wesley Publishing Company, (1993), Pgs. 346-350	

EXAMINER	/Khiem Nguyen/	DATE CONSIDERED	08/30/2010
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Based on PTO/SB/08A(09-05) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,572	05/12/2009	Rudy G. H. Eschauzier	55123P376

CONFIRMATION NO. 1854

PUBLICATION NOTICE



OC000000044555224

79124
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

Title:Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers

Publication No.US-2010-0289568-A1

Publication Date:11/18/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,572	05/12/2009	Rudy G. H. Eschauzier	55123P376	1854
79124	7590	11/30/2010	EXAMINER	
MAXIM/BSTZ			NGUYEN, KHIEM D	
Blakely Sokoloff Taylor & Zafinan LLP			ART UNIT	PAPER NUMBER
1279 OAKMEAD PARKWAY			2817	
SUNNYVALE, CA 94085-4040			MAIL DATE	DELIVERY MODE
			11/30/2010	PAPER

Notice of Erroneous Early Release of Patent Application Information
on November 11, 2010

On November 11, 2010, the United States Patent and Trademark Office (USPTO), unintentionally and as a result of a processing error, made available to subscribers of patent application data the patent application publications that were not scheduled to publish under 35 U.S.C. 122(b) until November 18, 2010. The USPTO's subscription service allows a member of the public to obtain copies of all patents or application publications from the USPTO on the date of grant or publication for a fee. One subscriber who had access to the early-published data made these premature patent application publications available on its free Web service, known as Free Patents Online, on November 11, 2010 - one week prior to the scheduled publication date. At the USPTO's request, the subscriber removed access to the patent application publications dated November 18, 2010 on November 15, 2010 until November 18, 2010. While the premature release of application information on November 11, 2010, is not considered a publication of such applications under 35 U.S.C. 122(b), the USPTO acknowledges that there are potential international ramifications in certain very limited circumstances such as where an applicant whose application information was released early did not file a foreign application within the Paris Convention priority period but did file in a foreign country between November 11, 2010 and November 18, 2010.

The USPTO did not post the publications on its Web site until November 18, 2010, and it did not provide access to the public Patent Application Information Retrieval (PAIR) System based on the early release of the publication data. Moreover, the USPTO did not record in its records that a publication occurred until November 18, 2010. Copies of, and access to, any of the affected applications described in this document were not provided by the USPTO under 37 CFR 1.14 based on the error described in this document. The USPTO regrets this error and is instituting controls to prevent similar processing errors in the future.

Inquiries regarding this matter may be directed to Mark Polutta, Senior Legal Advisor, Office of Patent Legal Administration at (571) 272-7709 or via email addressed to mark.polutta@uspto.gov.

Electronic Acknowledgement Receipt	
EFS ID:	9089201
Application Number:	12464572
International Application Number:	
Confirmation Number:	1854
Title of Invention:	Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers
First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Customer Number:	79124
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	55123P376
Receipt Date:	21-DEC-2010
Filing Date:	12-MAY-2009
Time Stamp:	16:53:51
Application Type:	Utility under 35 USC 111(a)

Payment information:	
Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$880
RAM confirmation Number	4357
Deposit Account	022666
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		55123P376_20101221_Amd. PDF	428296	yes	14
			a2a9da52c5b6dfd5467a67bc525cff38022f4696		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	11	
	Applicant Arguments/Remarks Made in an Amendment		12	13	
	Authorization for Extension of Time all replies		14	14	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	30718	no	2
			401bf98209d66198e078da58525a21ca00518de6		
Warnings:					
Information:					
Total Files Size (in bytes):			459014		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Appl. No. 12/464,572
Amdt. Dated 12/21/2010
Reply to Office Action of September 21, 2010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No. :	12/464,572	Confirmation No. 1854
Applicant :	Rudy G. H. Eschauzier et al.	
Filed :	05/12/2009	
TC/A.U. :	2817	
Examiner :	Nguyen, Khiem D	
Docket No. :	55123P376	
Customer No. :	79124	

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AMENDMENT

Sir:

In response to the Office Action of September 21, 2010, please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 12 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) In an amplifier system, a circuit comprising:
a first differential amplifier;
first and second choppers for chopping the input and the output of the first differential amplifier, respectively;
autozero circuitry coupled to the first differential amplifier for autozeroing the first differential amplifier;
the autozero circuitry operating at a first frequency and the choppers operating at a second frequency, ~~unequal to the first frequency~~ being twice the second frequency, the second frequency having a 50% duty cycle;
the first frequency having a duty cycle of less than 50%;
each half cycle of the choppers being interrupted while the first differential amplifier is auto-zeroed.
2. (cancelled)
3. (original) The circuit of claim 1 further comprising an amplifier having differential inputs coupled to the first and second differential inputs of the amplifier system and an output coupled to the output amplifier.
4. (cancelled)
5. (cancelled)

6. (currently amended) The circuit of claim 4 wherein the first frequency has a duty cycle of not more than 25%, ~~whereby each half cycle of the choppers is interrupted while the first differential amplifier is auto-zeroed.~~

7. (currently amended) In an amplifier system, a circuit comprising:
a first differential amplifier;
first and second choppers for chopping the input and the output of the first differential amplifier, respectively;

~~The circuit of claim 1 wherein the first chopper is being coupled to the first and second differential inputs of the amplifier system;~~ and further comprising:

a first-switch having a first first-switch state coupling the differential inputs of the first differential amplifier to differential outputs of the first chopper, and a second first-switch state connecting the differential inputs of the first differential amplifier together;

a second differential amplifier, the second differential amplifier having differential inputs, each connected to a circuit ground through a respective capacitance;

differential outputs of the first and second differential amplifiers being coupled in common;

an output amplifier having an input coupled to an output of the second chopper;

a second-switch having a first second-switch state coupling the common outputs of the first and second differential amplifiers to an input of the second chopper, and a second second-switch state coupling the common outputs of the first and second differential amplifiers to the differential inputs of the second differential amplifier;

the first and second switches operating at a first frequency and the choppers operating at a second frequency unequal to the first frequency.

8. (original) The circuit of claim 7 wherein the second frequency is twice the first frequency, and the first and second frequencies each have a 50% duty cycle.

9. (original) The circuit of claim 7 wherein the first frequency is twice the second frequency, the second frequency having a 50% duty cycle.

10. (original) The circuit of claim 9 wherein the first frequency has a duty cycle of less than 50%, whereby each half cycle of the choppers is interrupted while the first differential amplifier is auto-zeroed.

11. (original) The circuit of claim 9 wherein the first frequency has a duty cycle of not more than 25%, whereby each half cycle of the choppers is interrupted while the first differential amplifier is auto-zeroed.

12. (original) The circuit of claim 9 further comprising:
third and fourth differential amplifiers, the fourth differential amplifier having differential inputs, each connected to a circuit ground through a respective capacitance, differential outputs of the third and fourth differential amplifiers being coupled in common;
the first-switch when in the first first-switch state also coupling the differential inputs of the third differential amplifier together and coupling the common outputs of the third and fourth differential amplifiers to the differential inputs to the fourth differential amplifier;
the first-switch when in the second first-switch state coupling the differential outputs of the first chopper to the differential inputs of the third differential amplifier and coupling the common differential outputs of the third and fourth differential amplifiers to the differential inputs of the second chopper.

13. (original) The circuit of claim 12 further comprising an amplifier having differential inputs coupled to the first and second differential inputs of the amplifier system and an output coupled to the output amplifier.

14. (original) The circuit of claim 9 wherein:
the first and second switches and the first and second choppers comprise third, fourth and fifth switches, each having an open and a closed state;
the first differential input of the amplifier system being connectable to a first differential input of the first differential amplifier by third and fifth switches, and to a second differential input of the first differential amplifier by the fourth and fifth switches;

the second differential input of the amplifier system being connectable to the first differential input of the first differential amplifier by the fourth switch, and to the second differential input of the first differential amplifier by the third switch;

a first common connection of the outputs of the first and third differential amplifiers being connectable to a first differential input of the differential output amplifier through the third switch and to a second differential input to the differential output amplifier through the fourth switch;

a second common connection of the outputs of the first and second differential amplifiers being connectable to a first input of the differential output amplifier through the fourth switch and to a second input to the differential output amplifier through the third switch;

the common connection of the differential outputs of the first and second differential amplifiers being connectable to the differential inputs of the second differential amplifier by the fifth switch.

15. (original) The amplifier of claim 14 wherein the output amplifier is a multiple stage amplifier.

16. (original) The circuit of claim 14 further comprising a third amplifier having differential inputs coupled to the differential inputs of the amplifier system and an output coupled to the output amplifier.

17. (original) The circuit of claim 14 wherein the third switches are all closed at the same time, but not when the fourth and fifth switches are closed, the fourth switches are all closed at the same time, but not when any of the third and fifth switches are closed, and the fifth switches are all closed at the same time, but not when any of the third or fourth switches are closed, whereby the switch operation is nonoverlapping, the fifth switches being closed at the first frequency with a duty cycle of less than 50%, the third switches being closed at a second frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the fifth switches, and the fourth switches being closed at the second frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the fifth switches.

18. (original) The amplifier of claim 17 wherein the fifth switches are closed with a duty cycle of not more than 25%.

19. (original) The amplifier of claim 17 wherein the output amplifier is a multiple stage amplifier.

20. (original) The circuit of claim 17 further having third and fourth differential inputs of the amplifier system forming a second differential input port, and further comprising:
a third differential amplifier having first and second differential inputs;
the third differential input of the amplifier system being connectable to the first differential input of the third differential amplifier by third and fifth switches, and to the second differential input of the third differential amplifier by the fourth and fifth switches;
the fourth differential input of the amplifier system being connectable to the first differential input of the third differential amplifier by the fourth switch and to the second differential input of the third differential amplifier by the third switch;
differential outputs of the third differential amplifier being coupled in common with the differential outputs of the first and second differential amplifiers.

21. (original) The circuit of claim 20 further comprising fourth and fifth differential amplifiers, the fourth differential amplifier having differential inputs coupled to the first and second differential inputs of the amplifier system and an output coupled to the output amplifier, and the fifth differential amplifier having differential inputs coupled to the third and fourth differential inputs of the amplifier system and an output coupled to the output amplifier.

22. (original) The circuit of claim 17 further comprising:
a timing circuit for providing three output timing signals for controlling the timing of the third, fourth and fifth switches respectively, the output timing signals having first and second states and being nonoverlapping in the second state, the three output timing signals being provided from three input signals of first and second states, any of which input signals may overlap in the second state, comprising:

logic coupled to delay the change of a first output timing signal to the second state response to a change of the first input signal to the second state until after both second and third output signals are in the first state;

logic coupled to delay the change of a second output timing signal to the second state response to a change of the second input signal to the second state until after both first and third output signals are in the first state; and,

logic coupled to delay the change of a third output timing signal to the second state response to a change of the third input signal to the second state until after both first and second output signals are in the first state.

23. (original) The circuit of claim 22 further comprising:

switch drive circuits for driving the third, fourth and fifth switches on the first and second differential inputs to the amplifier system to control their on and off states, respectively, each drive circuit being responsive to a respective output timing signal of the timing circuit, to control the on and off states of the third, fourth and fifth switches, respectively;

circuitry for connecting a first lead of a capacitor to a power supply voltage, a second capacitor lead to a circuit ground and holding the respective switch in the off state when the respective output timing signal is its first state; and,

circuitry for connecting the second lead of the capacitor to a voltage responsive to a common mode voltage of the first and second differential inputs of the amplifier system and connecting the first capacitor lead to a control voltage for the respective switch when the circuit is clocked by a respective output timing signal;

whereby the control voltage for turning on the switches is approximately one power supply voltage above the common mode voltage of the first and second differential inputs of the amplifier system, independent of what the common mode voltage is.

24. (cancelled)

25. (cancelled)

26. (currently amended) ~~The method of claim 24 wherein~~ A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

operating the chopper stabilization at a first frequency; and,

operating the auto-zeroing at a second frequency;

the ratio of the frequencies being two to one.

the second frequency is being twice the first frequency and ~~has~~ having a duty cycle of less than one half.

27. (currently amended) ~~The method of claim 26 wherein~~ A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

operating the chopper stabilization at a first frequency; and,

operating the auto-zeroing at a second frequency;

the ratio of the frequencies being two to one.

the second frequency ~~has~~ having a duty cycle of not more than one-quarter.

28. (currently amended) ~~The method of claim 24 further comprising~~ A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

operating the chopper stabilization at a first frequency; and,

operating the auto-zeroing at a second frequency;

the ratio of the frequencies being two to one.

after each cycle of the chopper stabilization of the first amplifier, chopper stabilizing a second amplifier using the same choppers;

auto-zeroing the second amplifier while the first amplifier is being chopper stabilized;
and,

auto-zeroing the first amplifier while the second amplifier is being chopper stabilized;
the outputs of the first and second amplifiers being connected in common.

29. (currently amended) ~~The method of claim 24~~ A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability wherein the chopper stabilized first amplifier has first, second and third pluralities of open and closed switches, the first and second switches being coupled as input and output chopper switches and the third switches being coupled as auto-zero switches, wherein the first switches are all closed at the same time, but not when the second and third switches are closed, the second switches are all closed at the same time, but not when any of the first and third switches are closed, and the third switches are all closed at the same time, but not when the first or second switches are closed, whereby the switch operation is nonoverlapping, the third switches being closed at a first frequency with a duty cycle of less than 50%, the first switches being closed at a second frequency equal to one half the first frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the third switches, and the second switches being closed at the second frequency with a duty cycle of approximately 50%, except as interrupted for the closure of the third switches;

operating the first and second switches at a first frequency; and,

operating the third switches at a second frequency;

the ratio of the frequencies being two to one.

30. (original) The method of claim 29 wherein the third switches are closed with a duty cycle of not more 25%.

31. (original) The method of claim 30 wherein the output amplifier is a multiple stage amplifier.

32. (original) The method of claim 29 wherein the first amplifier has first and second differential inputs and further comprising:

controlling, responsive to a clocking signal, the on and off states of switches controlling the connection of the first and second differential inputs to differential amplifier system inputs and to themselves, the differential amplifier system inputs having a common mode voltage, comprising, for each pair of switches:

connecting a first lead of a capacitor to a power supply voltage, a second capacitor lead to a circuit ground and holding the switches in the off state when the switch control circuit is not being clocked by one of a first, second or third timing signal; and,

connecting the second lead of the capacitor to a voltage responsive to the common mode voltage and connecting the first capacitor lead to a control voltage when the circuit is clocked by the respective first, second or third timing signal;

whereby the control voltage for turning on the switches is approximately one power supply voltage above the common mode voltage, independent of what the common mode voltage is.

33. (original) The method of claim 32 further comprising:

providing the first, second and third timing signals, each having first and second states corresponding to switch on and off states, the three timing signals being nonoverlapping in the first state from three input signals of first and second states, any two of which may overlap in the first state by;

delaying the change of the first timing signal to the first state response to a change of the first input signal to the first state until after both the second and the third timing signals are in the second state;

delaying the change of the second timing signal to the first state response to a change of the second input signal to the first state until after both the first and the third output signals are in the second state; and,

delaying the change of the third timing signal to the first state response to a change of the third input signal to the first state until after both the first and the second output signals are in the second state.

34. (withdrawn) A circuit for providing three output timing signals having first and second states and being nonoverlapping in the first state from three input signals of first and second states, any two of which may overlap in the first state, comprising:

logic coupled to delay the change of a first output timing signal to the first state response to a change of the first input signal to the first state until after both second and third output signals are in the second state;

logic coupled to delay the change of a second output timing signal to the first state response to a change of the second input signal to the first state until after both first and third output signals are in the second state; and,

logic coupled to delay the change of a third output timing signal to the first state response to a change of the third input signal to the first state until after both first and second output signals are in the second state.

35. (withdrawn) A switch control circuit for controlling, responsive to a clocking signal, the on and off states of switches controlling the connection of first and second differential input signals, the first and second differential input signals having a common mode voltage, comprising:

circuitry for connecting a first lead of a capacitor to a power supply voltage, a second capacitor lead to a circuit ground and holding the switches in the off state when the switch control circuit is not being clocked; and,

circuitry for connecting the second lead of the capacitor to a voltage responsive to the common mode voltage and connecting the first capacitor lead to a switch control voltage when the circuit is clocked;

whereby the switch control voltage for turning on the switches is approximately one power supply voltage above the common mode voltage, independent of what the common mode voltage is.

36. (withdrawn) The switch control circuit of claim 35 wherein the first and second differential input signals are coupled to an input pair of transistors having a common connection to a current source, and wherein the common mode voltage is provided by a third transistor coupled to the common connection.

REMARKS/ARGUMENTS

Applicant hereby affirms election of claims 1-33 (Group 1) without traverse.

In the outstanding office action claims 7-23 and 29-33 were merely objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, claim 7 has been amended to now be in independent form and to include the limitations of claim 1 on which it previously depended. In that regard, claim 1 included the phrase "autozero circuitry coupled to the first differential amplifier for autozeroing the first differential amplifier". That phrase has been deleted as being redundant, the autozero circuitry itself being spelled out in original claim 7 (see Figure 5 of the present application). Also, claim 29 has been amended to now be in independent form and include all of the limitations of original claim 24 on which it originally depended. Accordingly, since claims 8-23 depend directly or indirectly on claim 7 and claims 30-33 depend directly or indirectly on claim 29, claims 7-23 and 29-33 should now be in condition for allowance.

Claim 1 has now been amended to include the limitations of claims 4 and 5. It is believed that this claim is now allowable, both because of the limitation that the first frequency have a duty cycle less than 50% and further that each half cycle of the choppers is interrupted while the first differential amplifier is autozeroed. The art cited by the examiner does not disclose either limitation, and certainly does not disclose that each half cycle of the choppers is interrupted while the first differential amplifier is autozeroed. Accordingly it is believed that claim 1 is now in condition for allowance. Claims 2, 4 and 5 have now been cancelled. Since it is believed that claim 1 is now in condition for allowance, claim 3, which depends on claim 1, should also be in condition for allowance, as should claim 6 which has now been amended to now depend on claim 1 and to eliminate a now redundant portion thereof.

Claims 24 and 25 have been cancelled, though the limitations of original claim 24 have now been included in claims 26, 27 and 28. Claim 26 includes the limitation that the second frequency is twice the first frequency and has a duty cycle of less than one half, whereas claim 27 is similar, though requires that the second frequency have a duty cycle of not more than one quarter, neither of which limitations is disclosed or rendered obvious by the cited art. Claim 28 also provides for chopper stabilizing a second amplifier using the same choppers, autozeroing the second amplifier while the first amplifier is being chopper stabilized and autozeroing the first amplifier while the second amplifier is being chopper stabilized, with the outputs of the first and second amplifiers being connected in common. This, too, is neither disclosed nor rendered obvious by the prior art cited by the examiner.

Accordingly, for the reasons set forth herein, it is believed that all claims in the case are now in condition for allowance.

Appl. No. 12/464,572
Amdt. Dated 12/21/2010
Reply to Office Action of September 21, 2010

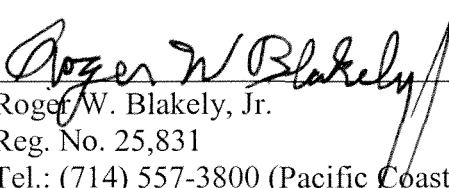
CONCLUSION

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 12/21/2010

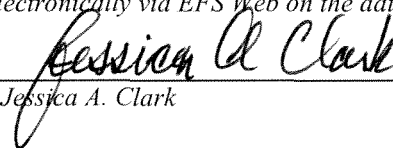
By 
Roger W. Blakely, Jr.
Reg. No. 25,831
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1279 Oakmead Parkway
Sunnyvale, California 94085

CERTIFICATE OF TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Date: 12/21/2010

 12/21/2010
Jessica A. Clark Date

Appl. No. 12/464,572
Extension of Time, All Replies Dated 12/21/2010
Accompanying Reply to Office Action of September 21, 2010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No.	:	12/464,572	Confirmation No. 1854
Applicant	:	Rudy G. H. Eschauzier et al.	
Filed	:	05/12/2009	
TC/A.U.	:	2817	
Examiner	:	Nguyen, Khiem D	
Docket No.	:	55123P376	
Customer No.	:	79124	

Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

AUTHORIZATION FOR EXTENSION OF TIME, ALL REPLIES

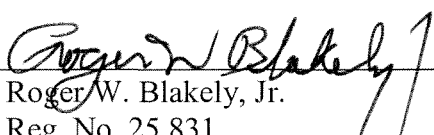
Sir:

Authorization is given to treat any concurrent or future reply requiring a petition for an extension of time under 37 CFR §1.136(a) for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. If any other petition is necessary for consideration of this paper, it is hereby so petitioned. Please charge any shortage in fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such deposit account.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 12/21/2010

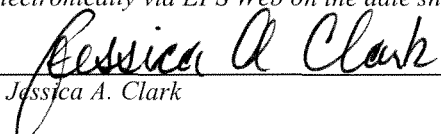
By 
Roger W. Blakely, Jr.
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Sunnyvale, California 94085

CERTIFICATE OF TRANSMISSION (37 CFR 1.84)

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Date: 12/21/2010


Jessica A. Clark
Date 12/21/2010

Docket No: 55123P376

Page 14 of 14

RWB/jc

Electronic Patent Application Fee Transmittal				
Application Number:		12464572		
Filing Date:		12-May-2009		
Title of Invention:		Low-Noise, Low-Power, Low Drift Offset Correction in Operational and Instrumentation Amplifiers		
First Named Inventor/Applicant Name:		Rudy G. H. Eschauzier		
Filer:		Roger W. Blakely/Jessica Clark		
Attorney Docket Number:		55123P376		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Independent claims in excess of 3	1201	4	220	880
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				880

Examiner-Initiated Interview Summary	Application No. 12/464,572	Applicant(s) ESCHAUZIER ET AL.	
	Examiner Khiem D. Nguyen	Art Unit 2817	

All Participants:

(1) Khiem D. Nguyen.

(2) BLAKELY, ROGER, 25831 (ATTNY).

Date of Interview: 22 February 2011

Status of Application: _____

(3) _____.

(4) _____.

Time: _____

Type of Interview:
☒ Telephonic
☐ Video Conference
☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description: _____

Part I.

Rejection(s) discussed:

Claims discussed:
Claim 6

Prior art documents discussed:

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
Discussed claim 6, applicant agreed to change term "claim 4" in line 1, to read as --claim 1--. Please see detailed Examiner's amendment.

Part III.
☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.
☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

/Khiem D Nguyen/
Examiner, Art Unit 2817

(Applicant/Applicant's Representative Signature – if appropriate)

Notice of Allowability	Application No.	Applicant(s)	
	12/464,572	ESCHAUZIER ET AL.	
	Examiner	Art Unit	
	Khiem D. Nguyen	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amend as filed on 12/21/2010.

2. ☒ The allowed claim(s) is/are 1, 3, 6-23 and 26-33.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.

(a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached

1) ☐ hereto or 2) ☐ to Paper No./Mail Date ____.

(b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)

2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date ____

4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material

5. ☐ Notice of Informal Patent Application

6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date 2-22-2011 .

7. ☒ Examiner's Amendment/Comment

8. ☐ Examiner's Statement of Reasons for Allowance

9. ☐ Other ____.

DETAILED ACTION

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with BLAKELY, ROGER on 2-22-2011.

The application has been amended as follows:

Claims 34, 35, 36 have been cancelled.

In Claim 6:

Claim 6 recites "claim 4" in lin1, has been changed to read as –claim 1--.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571)270-3941. The examiner can normally be reached on Mon-Fri 8:00AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Application/Control Number: 12/464,572
Art Unit: 2817

Page 3

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KDN (2-22-2011)

/Robert Pascal/
Supervisory Patent Examiner, Art Unit 2817



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NOTICE OF ALLOWANCE AND FEE(S) DUE

79124 7590 02/25/2011
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER

NGUYEN, KHIEM D

ART UNIT PAPER NUMBER

2817

DATE MAILED: 02/25/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/464,572 05/12/2009 Rudy G. H. Eschauzier 55123P376 1854

TITLE OF INVENTION: LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional NO \$1510 \$300 \$0 \$1810 05/25/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

79124 7590 02/25/2011
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

	(Depositor's name)
	(Signature)
	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

12/464,572 05/12/2009 Rudy G. H. Eschauzier 55123P376 1854

TITLE OF INVENTION: LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/25/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, KHIEM D	2817	330-009000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____ (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____
--	--

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted: ☐ Issue Fee ☐ Publication Fee (No small entity discount permitted) ☐ Advance Order - # of Copies _____	4b. Payment of Fee(s); (Please first reapply any previously paid issue fee shown above) ☐ A check is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).
--	---

5. Change in Entity Status (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____	Date _____
Typed or printed name _____	Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,572	05/12/2009	Rudy G. H. Eschauzier	55123P376	1854
79124	7590	02/25/2011	EXAMINER	
MAXIM/BSTZ			NGUYEN, KHIEM D	
Blakely Sokoloff Taylor & Zafman LLP			ART UNIT	
1279 OAKMEAD PARKWAY			PAPER NUMBER	
SUNNYVALE, CA 94085-4040			2817	
DATE MAILED: 02/25/2011				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 71 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 71 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	10168833
Application Number:	12464572
International Application Number:	
Confirmation Number:	1854
Title of Invention:	LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS
First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Customer Number:	79124
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	55123P376
Receipt Date:	25-MAY-2011
Filing Date:	12-MAY-2009
Time Stamp:	17:43:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1810
RAM confirmation Number	2285
Deposit Account	022666
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	55123P376_20110525_IssueFeeTrans_FeeAddr.PDF	70786 61e1f88c48b9a92fc7c1d7a25af7e9c5654aff5b1	no	2

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	32222 aac0f5dad9e9af3025d1ad42696f5bd350d6fcac	no	2
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Warnings:

Information:

Total Files Size (in bytes):	103008
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

79124 7590 02/25/2011
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

Certificate of Transmission

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark	(Depositor's name)
<i>Jessica A. Clark</i>	(Signature)
May 25, 2011	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,572	05/12/2009	Rudy G. H. Eschauzier	55123P376	1854

TITLE OF INVENTION: LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/25/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, KHIEM D	2817	330-009000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 Blakely Sokoloff
2 Taylor & Zafman LLP
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)
PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.
(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)
Number 14 B.V. Bergschenhoek, Netherlands

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____
4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)
☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature *Roger W. Blakely* Date May 25, 2011
Typed or printed name Roger W. Blakely, Jr. Registration No. 25,831

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☒ Customer Number: **38062**

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	12/464,572

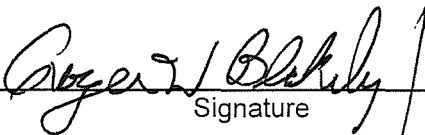
Completed by (check one):

☐ Applicant/Inventor

☒ Attorney or Agent of record 25,831
(Reg. No.)

☐ Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☐ Assignee recorded at Reel _____ Frame _____


Signature

Roger W. Blakely, Jr.
Typed or printed name

(714) 557-3800

Requester's telephone number

May 25, 2011

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ * Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS. SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:		12464572		
Filing Date:		12-May-2009		
Title of Invention:		LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN OPERATIONAL AND INSTRUMENTATION AMPLIFIERS		
First Named Inventor/Applicant Name:		Rudy G. H. Eschauzier		
Filer:		Roger W. Blakely/Jessica Clark		
Attorney Docket Number:		55123P376		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,572	07/05/2011	7973596	55123P376	1854

79124 7590 06/15/2011
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 71 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Rudy G. H. Eschauzier, Bergschenhoek, NETHERLANDS;
Nico van Rijn, Katwijk, NETHERLANDS;

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2019-01-07

Document Title - Applicant Communication Re: Payment of Maintenance Fee,
8th Year, Large Entity

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2022-12-20

Document Title - Applicant Communication Re: Payment of Maintenance Fee,
12th Year, Large Entity

8553733



THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

December 13, 2024

**THIS IS TO CERTIFY THAT ANNEXED IS A TRUE COPY FROM THE
RECORDS OF THIS OFFICE OF THE FILE WRAPPER AND CONTENTS
OF:**

APPLICATION NUMBER: 12/464,572

FILING DATE: *May 12, 2009*

PATENT NUMBER: 7973596

ISSUE DATE: *July 05, 2011*



Certified by

Katherine Kelly Vidal

Performing the Functions and Duties of the
Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

Filing Date: 05/12/09

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD						Application or Docket Number					
Substitute for Form PTO-875						12/464,572					
APPLICATION AS FILED – PART I						SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)	FEE (\$)		RATE (\$)	FEE (\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A			N/A	330		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A			N/A	540		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A			N/A	220		
TOTAL CLAIMS (37 CFR 1.16(i))		36	minus 20 =	16	x\$26			x\$52	832		
INDEPENDENT CLAIMS (37 CFR 1.16(h))		4	minus 3 =	1	x\$110			x\$220	220		
APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR									
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						195		390			
						TOTAL		TOTAL	2142		
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II						SMALL ENTITY		OR		OTHER THAN SMALL ENTITY	
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=	
	Application Size Fee (37 CFR 1.16(s))										
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A			N/A		
						TOTAL ADD'T FEE		TOTAL ADD'T FEE			
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=	
	Application Size Fee (37 CFR 1.16(s))										
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A			N/A		
						TOTAL ADD'T FEE		TOTAL ADD'T FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.											
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".											
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/464,572		Filing Date 05/12/2009		☐ To be Mailed						
APPLICATION AS FILED – PART I															
(Column 1)			(Column 2)		SMALL ENTITY ☐		OR		OTHER THAN SMALL ENTITY						
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)		OR		RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A				OR		N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A				OR		N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A				OR		N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =		*		X \$ =				OR		X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =		*		X \$ =				OR		X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).													
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										TOTAL		TOTAL			
* If the difference in column 1 is less than zero, enter "0" in column 2.															
APPLICATION AS AMENDED – PART II															
(Column 1)			(Column 2)		(Column 3)		SMALL ENTITY		OR		OTHER THAN SMALL ENTITY				
AMENDMENT	12/21/2010	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)					
	Total (37 CFR 1.16(i))	* 31	Minus	** 36	= 0	X \$ =		OR	X \$52=	0					
	Independent (37 CFR 1.16(h))	* 8	Minus	*** 4	= 4	X \$ =		OR	X \$220=	880					
	☐ Application Size Fee (37 CFR 1.16(s))														
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR							
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	880					
(Column 1)			(Column 2)		(Column 3)										
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)		RATE (\$)	ADDITIONAL FEE (\$)					
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =						
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =						
	☐ Application Size Fee (37 CFR 1.16(s))														
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR							
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE						
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.										Legal Instrument Examiner: /NINA RATANAVONG/					
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".															
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".															
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.															

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Search results for: PNS=(US7973596);

Collections searched: DWPI; ARIPO grant; Argentina UM; Argentina app; Armenia grant; Australia UM; Australia app; Australia grant; Austria UM; Austria app; Austria grant; Belarus UM; Belarus grant; Belgium app; Belgium grant; Brazil UM; Brazil app; Brazil grant; Bulgaria UM; Bulgaria app; Bulgaria grant; Canada app; Canada grant; China, Mainland UM; China, Mainland app; China, Mainland grant; Colombia app; Costa Rica UM; Costa Rica app; Croatia UM; Croatia app; Croatia grant; Cuba app; Cuba grant; Czech Republic UM; Czech Republic app; Czech Republic grant; Czechoslovakia grant; Denmark UM; Denmark app; Denmark grant; Estonia UM; Estonia app; Estonia grant; Eurasian (EAPO) grant; Europe (EP) app; Europe (EP) grant; Finland app; Finland grant; France app; France grant; Georgia grant; German Democratic Republic app; German Democratic Republic grant; Germany UM; Germany app; Germany grant; Greece app; Greece grant; Gulf Cooperation Council grant; Hong Kong UM; Hong Kong app; Hong Kong grant; Hungary grant; Iceland grant; India app; India grant; Indonesia UM; Indonesia app; Ireland UM; Ireland app; Ireland grant; Israel grant; Italy grant; Italy grant; Italy grant; Italy grant; Japan UM; Japan app; Japan grant; Korea UM; Korea app; Korea grant; Latvia grant; Lithuania grant; Luxembourg app; Luxembourg grant; Malaysia app; Malaysia grant; Mexico app; Mexico grant; Moldova UM; Moldova grant; Monaco grant; Mongolia UM; Mongolia grant; Morocco app; Morocco grant; Netherlands app; Netherlands grant; New Zealand grant; Norway app; Norway grant; OAPI grant; PCT (WO) app; Philippines UM; Philippines app; Philippines grant; Poland UM; Poland grant; Portugal UM; Portugal app; Portugal grant; Romania UM; Romania app; Romania granted; Russia UM; Russia app; Russia grant; Saudi Arabia app; Saudi Arabia grant; Serbia UM; Serbia app; Serbia grant; Singapore app; Singapore grant; Slovakia UM; Slovakia app; Slovakia grant; Slovenia UM; Slovenia grant; South Africa app; Spain UM; Spain app; Spain grant; Sweden app; Sweden grant; Switzerland app; Switzerland grant; Taiwan UM; Taiwan appl; Taiwan grant; Thailand UM; Thailand app; Thailand grant; Tunisia app; Turkey UM; Turkey app; UK app; UK grant; USSR grant; Ukraine UM; Ukraine grant; United States app; United States grant; Uruguay app; Vietnam UM; Vietnam app; Vietnam grant; Other

Table of Contents

-
1. US7973596B2 Low-noise, low-power, low drift offset correction in operational and instrumentation amplifiers
-

Family 1/1
1 record(s) per family

Record 1/1 US7973596B2 Low-noise, low-power, low drift offset correction in operational and instrumentation amplifiers

Title: Low-noise, low-power, low drift offset correction in operational and instrumentation amplifiers

Title - DWPI: Amplifier circuit such as operational amplifier, has auto-zero circuitry operating at frequency different from chopper, that is coupled to differential amplifier for auto-zeroing differential amplifier

Priority Number: US2009464572A

Priority Date: 2009-05-12

Application Number: US2009464572A

Application Date: 2009-05-12

Publication Date: 2011-07-05

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H03F000102	H	H03	H03F	H03F0001	H03F000102

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H03F000100	H	H03	H03F	H03F0001	H03F000100
H03F000102	H	H03	H03F	H03F0001	H03F000102
H03F000126	H	H03	H03F	H03F0001	H03F000126
H03F000320	H	H03	H03F	H03F0003	H03F000320
H03F0003347	H	H03	H03F	H03F0003	H03F0003347
H03F000345	H	H03	H03F	H03F0003	H03F000345

Assignee/Applicant: Number 14 B.V.,Bergschenhoek,NL

JP F Terms:

JP FI Codes:

Assignee - Original: Number 14 B.V.

Any CPC Table:

Type	CPC - Current - Invention	CPC - Current - Additional	Version	Office
Current	H03F 3/45475	H03F 2200/261	20130101	EP; US
Current	H03F 3/347	H03F 2203/45138	20130101	EP; US
Current	H03F 3/45968	H03F 2203/45212	20130101	EP; US
Original	H03F 3/45475	H03F 2200/261	20130101	US
Original	H03F 3/347	H03F 2203/45138	20130101	US
Original	H03F 3/45968	H03F 2203/45212	20130101	US

ECLA: H03F000345S1K | H03F0003347 | H03F000345S3K3 | T03F0200261 | T03F020345138 | T03F020345212

Abstract:

Low-noise, low-power, low drift offset correction in operational and instrumentation amplifiers and amplifiers using the same are disclosed. The amplifiers disclosed use different combinations of chopping and auto-zero techniques. Also disclosed are amplifiers using on-off switches to affect the chopping and auto-zeroing, with unique circuits for driving the switches on the differential input to provide boot-strapped switch controls. Other features are disclosed.

Language of Publication: EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2022-12-20	MAFP	+
Description: MAINTENANCE FEE PAYMENT FEE PAYMENT YEAR 12 PAYMENT OF MAINTENANCE FEE, 12TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1553); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY		
2019-01-07	MAFP	+
Description: MAINTENANCE FEE PAYMENT FEE PAYMENT YEAR 8 PAYMENT OF MAINTENANCE FEE, 8TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1552); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY		
2015-01-05	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 4		
2011-06-15	STCF	-
Description: INFORMATION ON STATUS: PATENT GRANT PATENTED CASE		

2010-12-06	FEPP	-
Description: FEE PAYMENT PROCEDURE PAYOR NUMBER ASSIGNED (ORIGINAL EVENT CODE: ASPN); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY		
2009-07-23	AS	-
Description: ASSIGNMENT NUMBER 14 B.V., NETHERLANDS ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNORS:ESCHAUZIER, RUDY G. H.; VAN RIJN, NICO; REEL/FRAME:022999/0283 2009-05-12		

Post-Issuance (US):

Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
NUMBER 14 B.V.,BERGSCHENHOEK,NL	ESCHAUZIER, RUDY G. H.	2009-05-12	022999/0283	2009-07-23
	VAN RIJN, NICO	2009-05-12	-	-
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085				

Maintenance Status (US):

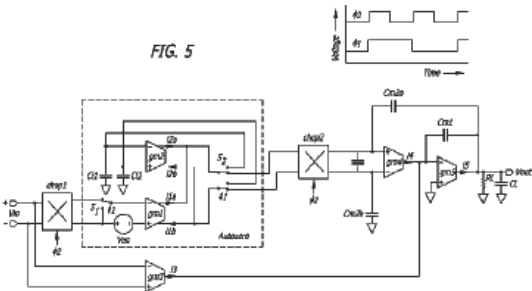
Litigation (US):

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Priority Number - DWPI: US2009464572A

Priority Date - DWPI: 2009-05-12

Assignee - Current US: NUMBER 14 B.V.



United States Patent and Trademark Office

Office of the Commissioner for Patents

LOW-NOISE, LOW-POWER, LOW DRIFT OFFSET CORRECTION IN
OPERATIONAL AND INSTRUMENTATION AMPLIFIERS

PATENT #

7973596

APPLICATION #

12464572

FILING DATE

05/12/2009

ISSUE DATE

07/05/2011

Payment Window Status

WINDOW

11.5 Year

STATUS

Closed

FEES

Paid

No maintenance fees are due.

Window	First Day to Pay	Surcharge Starts	Last Day to Pay	Status	Fees
3.5 Year	07/05/2014	01/06/2015	07/06/2015	Closed	Paid
7.5 Year	07/05/2018	01/08/2019	07/05/2019	Closed	Paid
11.5 Year	07/05/2022	01/06/2023	07/05/2023	Closed	Paid

Patent Holder Information

Customer #

38062

Entity Status

UNDISCOUNTED

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