

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANALOG DEVICES, INC.,
Petitioner,

v.

NUMBER 14 B.V.,
Patent Owner.

IPR2025-00550
U.S. Patent 7,973,596

DECLARATION OF DR. ION OPRIS (Ex. 1003)

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I, Dr. Ion Opris declare as follows:

1. I am over eighteen years of age, and I am competent to testify regarding the matters set forth in this declaration if called upon to do so.

2. I have been retained in this matter on behalf of Petitioner Analog Devices, Inc., (“ADI”).

3. I submit this declaration at the request of K&L Gates, counsel for ADI in this proceeding.

4. I have been asked to provide an opinion on U.S. Patent No. 7,973,596 (the ’596 Patent). In preparing this declaration, I have studied the ’596 Patent (Ex. 1001 [’596 Patent]), its file history (Ex. 1002 [File History]), U.S. Patent No. 6,476,671 (“*Tang*”) (Ex. 1008 [Tang]) and U.S. Patent No. 1011 (“*Pertijs*”) (Ex. 1011 [Pertijs]). I have also considered the other documents or references cited in this declaration.

5. In forming the opinions, I expressed below, I have considered the documents listed above, the relevant legal standards as provided to me by counsel, and my own knowledge and experience, as well as any other document referenced in this declaration.

6. I reserve the right to supplement my opinions in the future to respond to any arguments raised by the opposition and to take into account new information that becomes available to me.

I. BACKGROUND AND QUALIFICATIONS

7. This section briefly summarizes my career history education, publications, and other relevant qualification. My full *curriculum vitae* (“CV”) is included as Ex. 1004.

8. I received a Ph.D. in Electrical Engineering from Stanford University, Stanford, CA in 1996. I also hold an M.S. in Electrical Engineering from Stanford University, Stanford, CA in 1991 and a Diploma of Engineering Electronics and Telecommunications with highest honors from Bucharest Polytechnic Institute, Romania in 1986.

9. Since June 1996, I have been employed as an independent consultant at Opris Consulting designing analog, mixed-mode and ASIC IC devices, specializing in high performance analog circuits, such as analog to digital converters, digital to analog converters, communications circuits, and sensor interfaces.

10. I have completed over 200 design projects for extremely low power sensors read-out circuitry, ultrasonic imaging, audio/video interface products, CCD and CMOS light sensors, wired and RF data communications (DSL, Ethernet, RFID, Wi-Fi), MEMS accelerometers, gyroscopes, and MEMS based displays.

11. From April 2010 to October 2010, I was the Vice President of Product Design at MCube Inc. and from September 2009 to April 2010 I was also the

Senior Director of IC Design responsible for the CMOS and MEMS design of MEMS base accelerometers and magnetic sensors.

12. From June 1994 to October 1997, I was a Principal Design Engineer at National Semiconductor Corp. responsible for system architecture and analog/digital circuit design for high speed/high resolution A/D converters, mixed-mode analog/digital ASICs, and complex behavioral simulations. I released to production a family of high performance 12-bit A/D converters.

13. From September 1990 to December 1995, I have also worked as a research assistant at Stanford University enrolled as a PhD candidate in Electrical Engineering conducting research in the areas of analog to digital converters, analog nonlinear circuits and nonlinear control as well as low power/low noise amplifiers and continuous time filters for biological data acquisition.

14. From April 1989 to August 1990, I was a Design Engineer at Core International, Boca Raton, FL designing DMA adapters for tape drives and hard disk drives.

15. From 1991 to present, I have had various consulting jobs in hardware design/firmware with applications in RF data communication and spread spectrum technology.

16. Almost all analog circuits that I have worked on include design of operational amplifiers. Several projects with relevant experience in operational amplifiers design include as follows:

- several families of high speed, high resolution A/D converters, including the operational amplifiers embedded in these designs;
- several families of MEMS based sensors for accelerometer, gyroscopes and microphone application, including the operational amplifiers embedded in these designs;
- several sensor interfaces design for chemical or mechanical sensors based on resistive bridge sensors, including the operational amplifiers embedded in these designs.

17. I was ranked 2nd at the PhD Qualification Examination at Stanford University in January 1991 and awarded a School of Engineering Fellowship at Stanford University in 1990-1991.

18. I was ranked 1st in 1983, 1984, 1985, and 2nd in 1986 at the Romanian National Electronic Engineering contest. This is a highly competitive contest that is open to all undergraduate students in the country which tests both theoretical and practical skills.

19. I have been awarded over 85 US and international patents and I have authored over 30 technical papers.

20. Some of the relevant patents are:

- US Patent No. 9,444,404, (issued Sept. 13, 2016) (“MEMS device front-end charge amplifier”);
- US Patent No. 8,754,694 (issued June 17, 2014) (“Accurate ninety-degree phase shifter”);
- US Patent No. 8,743,082 (issued June 3, 2014) (“Controller architecture for combination touch, handwriting, and fingerprint sensor”);
- US Patent No. 8,742,964 (issued June 3, 2014) (“Noise reduction method with chopping for merged MEMS accelerometer sensor”)
- US Patent No. 8,064,622 (issued Nov. 22, 2011) (“Self-biased Amplifier Device for an Electret Microphone”);
- US Patent No. 6,642,778 (issued November 4, 2003) (“Low-voltage bandgap reference circuit”);
- US Patent No. 6,549,065 (issued Apr. 15, 2003) (“Low-voltage bandgap reference circuit”);
- US Patent No. 6,426,669 (issued July 30, 2002) (“Low voltage bandgap reference circuit”);
- US Patent No. 6,407,622 (issued May 1, 2001) (“Low-voltage bandgap reference circuit”);

- US Patent No. 6,225,850 (issued May 2001) (“Series resistance compensation in translinear circuits”)
- US Patent No. 6,121,824 (issued Sept. 19, 2000) (“Series resistance compensation in translinear circuits”);
- US Patent No. 5,847,607 (issued Dec. 8, 1998) (“High speed fully differential operational amplifier with fast settling time for switched capacitor applications”)

21. I am being compensated for my work associated with this case at my consulting rate of \$400.00 per hour. My compensation is not contingent on my opinions or the outcome of this case, and I have no other interest in the case or the parties thereto.

II. LEGAL STANDARDS

22. Although I am not a lawyer, I have been advised of the relevant legal principles by ADI’s counsel and have used them as a basis for my opinions. These are consistent with my understanding of the legal principles based on my prior experience with patent litigation matters.

A. Level of skill in the art

23. I understand that the person of ordinary skill in the art (POSITA) is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I further understand that the factors that may be considered in

determining the ordinary skill in the art include the following: the type of problems encountered in the art, prior art solutions to those problems, rapidity with which innovations are made, sophistication of the technology, and the educational level of workers in the field.

B. Claim Construction

24. I understand that the claims within a patent set forth what the inventors have presented as their inventions. I understand that claims can be independent or in dependent form, meaning that they depend from the identified independent claim and add requirements to those claims.

25. I understand that claim construction is a matter of law for the arbiter of law to decide. I further understand that claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, i.e., the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention in light of what the patent teaches.

26. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered

“intrinsic” evidence), and “extrinsic” evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.

27. I understand that a person of ordinary skill in the art is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. For this reason, the words of the claim must be interpreted in view of the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification.

28. I understand that claim terms must be construed in a manner consistent with the context of the intrinsic record. In addition to consulting the specification, one should also consider the patent’s prosecution history.

29. I understand that in addition to the intrinsic record, courts may also look to extrinsic evidence to construe claim terms. I understand that extrinsic evidence can be helpful in many ways, including to explain scientific principles, the meaning of technical terms, and terms of art that appear in the patent and prosecution history. However, any extrinsic evidence should be afforded less weight than the intrinsic evidence, as the intrinsic evidence is a better indicator of how the applicants understood their invention.

30. I understand that commonly, determining the ordinary and customary meaning of the claim requires examination of terms that have a particular meaning in a field of art. I understand that extrinsic evidence can educate the court regarding the field of the invention and can help the court determine what a person of ordinary skill in the art would understand claim terms to mean.

C. Invalidity

31. I understand that, unlike at the district court, patents subject to *inter partes* review, such as this proceeding, are not presumed to be valid, such that a lower burden of proof is used to judge the patentability of challenged claims. Unlike the district court's "clear and convincing" burden, here a "preponderance of the evidence" burden exists, meaning that to establish invalidity, the decision maker must simply find their factual findings "more likely than not."

1. Anticipation

32. I understand that a patent claim is invalid as "anticipated" by a single "prior art" reference if the reference discloses every single element of the claim with sufficient precision and detail to establish that the subject matter of the claim existed in the prior art. In particular, I understand that it is not sufficient to establish that all of the elements are collectively disclosed within the four corners of a particular document. Instead, the operative question is whether a person of ordinary skill would have understood the elements as being arranged as in the

claim itself. I also understand that a prior art reference cannot “anticipate” a patent claim unless that reference enables one of ordinary skill in the art to make and use what is disclosed without undue experimentation. Thus, if the reference does not enable one of ordinary skill to make or use each and every claim limitation, then the claim cannot be “anticipated” by the reference.

33. I understand that a prior art reference can disclose a given claim element actually or inherently.

34. In the case of actual disclosure, I understand that a person of ordinary skill would need to have understood that the disclosure corresponds to the claim element in question. I also understand that such disclosure may be implicit rather than explicit. For example, prior art need not use the same words as the claimed invention. However, I understand that ambiguous references do not anticipate.

35. In the case of alleged “inherent” anticipation, I understand that the claim element in question must necessarily be present when practicing the described technology even though the prior art reference itself contains no express description of the element in question. In particular, I understand that “possibilities or probabilities” are not sufficient to establish inherency. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, the essence of inherency is that one of ordinary skill in the art would recognize that a reference unavoidably teaches the property in question.

2. Obviousness

36. I understand that a patent claim may describe an invention that was new (i.e., not anticipated by any prior art reference), but nevertheless be invalid for “obviousness” if the differences between the patented subject matter and the prior art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention was made.

37. I understand that an invention is not rendered obvious simply on the basis of two or more different disclosures that collectively disclose all of the claimed elements. In other words, an invention is not obvious just because all of the elements that comprise the invention may have been independently known in the prior art. Instead, a person of ordinary skill in the art must have had a reason or basis to make any alleged modification or combination as well as a reasonable expectation of success in pursuing the possibility that turns out to succeed and is claimed. In particular, I understand that knowledge of a goal does not itself render achievement of that goal obvious.

38. I also understand that determining whether or not a claimed invention would have been obvious requires assessing facts related to (1) the scope and content of the prior art, (2) the differences between the prior art and the claimed invention, (3) the level of ordinary skill in the art, and (4) any objective evidence

(“secondary considerations”) of non-obviousness. I understand that this is known as consideration of the “Graham Factors.”

39. I further understand that an invention is not obvious just by demonstrating that each of its elements was, independently, known in the prior art. To prove that an invention is obvious, I understand that it can be important to point to a reason or reasons, such as a teaching, suggestion, or motivation (although such a reason need not be found in the references themselves), that would have prompted a person of ordinary skill in the relevant field to combine or modify the elements in the way the claimed invention does. I understand that this is because inventions in most (if not all) instances rely upon building blocks already known, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known, therefore it can be important to point to such a reason or reasons. I understand that in identifying such a reason, the analysis need not require precise teachings in the prior art directed to the specific subject matter of the challenged claim.

40. I understand that it will often be necessary for a court to look to interrelated teachings of multiple patents and the background knowledge possessed by a person having ordinary skill in the art in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. I understand that any need or problem known in the field of

endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. I understand that the combination of familiar elements according to known methods may be obvious when it does no more than yield predictable results.

41. I also understand that a claim is not invalid as obvious if it is more than the predictable use of prior art elements according to their established functions.

42. Further, I understand that while predictability is a touchstone of obviousness, the concept of a “predictable result” under the law refers not only to the expectation that prior art elements are capable of being physically combined, but also that the combination would have worked for its intended purpose.

43. I also understand that if the prior art teaches away from combining known elements in the manner claimed by the invention at issue, discovering a successful way to combine them is less likely to be obvious. In particular, I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant, or would understand based on the reference that the line of

development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. Likewise, I understand that similar subject matter may not be sufficient motivation for a person of skill in the art to combine references if the references have conflicting elements.

44. Further, I understand that even if a reference does not necessarily "teach away," its statements regarding preferences are relevant to a finding whether a person of ordinary skill would have had reason to combine that reference with another reference.

45. I also understand that one must be cautious and resist the temptation to rely on hindsight reasoning when attempting to combine references to suggest that a claim may be obvious. It is important to analyze validity based on the perspective of one at the time of the invention, which I understand is at least as early as the effective filing date. I understand that objective indicia (or "secondary considerations") of non-obviousness or obviousness may be particularly probative and helpful in avoiding hindsight.

46. I also understand that the burden of persuasion concerning unpatentability (in other words, the ultimate burden to prove the relevant facts to the specified degree of certainty—here, preponderance of the evidence) remains at all times on the party challenging patentability. If the Board is left uncertain as to validity issues, Petitioner has thus failed to meet its burden.

III. LEVEL OF ORDINARY SKILL IN THE ART

47. I understand from counsel that the '596 Patent is analyzed from the viewpoint of a person of ordinary skill in the art ("POSITA") in and around May, 2009. My analysis and opinions below are given from the perspective of a POSITA in the technological field in the relevant time frame, unless stated otherwise.

48. I satisfied the definition of a POSITA long before the filing date of the application leading to the '596 Patent. I now consider myself an expert in the relevant field of technology for the '596 Patent.

49. It is my opinion that a POSITA of the '596 Patent would have a bachelor's degree in electrical engineering or a related field (or equivalent understanding through actual work experience) and had at least two or three years of experience relating to the design or implementation of analog integrated circuits. Additionally, additional professional experience could substitute for formal education and additional formal education could substitute for professional experience.

IV. TECHNICAL BACKGROUND

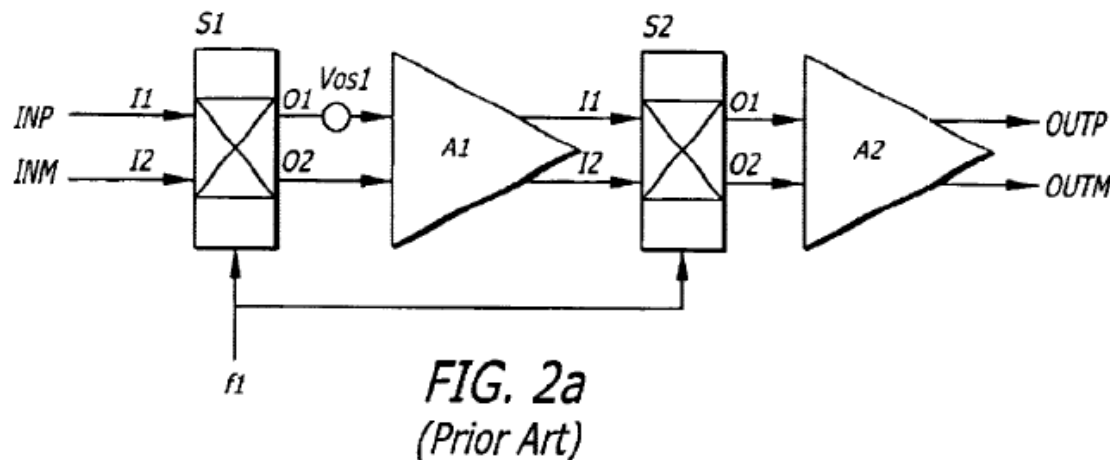
50. An operational amplifier, or opamp, is an integrated circuits which amplifies the difference in voltage between two inputs, outputting the result. Ex. 1005 [Huijsing] 1:11-13. In theory, an opamps will have zero output when the

differential input is zero. Ex. 1005 [Huijsing] 1:18-21. However, “a real op amp will not have a zero output for a zero differential input, but rather will have a zero output at some finite differential input.” Ex. 1005 [Huijsing] 1:25-27. This finite differential input will be equal to what “is commonly referred to as the input offset[.]” Ex. 1005 [Huijsing] 1:28-35. The offset voltage (also called offset voltage, input offset, or offset) “will cause an error in the output of the system equal to the input offset times the gain between the input and system output.” Ex. 1005 [Huijsing] 1:28-35.

51. Imperfect component matching, including in the input stage of an optical amplifier, contribute to input offsets. Ex. 1005 [Huijsing] 1:38-46. Input offsets may be modeled as a voltage source in series with the input terminals of an opamp. Ex. 1005 [Huijsing] 1:38-46.

52. One common method used to compensate for or reduce offset voltages is chopper stabilization. Chopper stabilization involves synchronously inverting the polarity of both the input and output of an amplifier on a periodic basis. Ex. 1005 [Huijsing] 1:53-60; Ex.1006 [Tang] 1:54-58; Ex. 1011 [Pertijs] 4:46-51. In one phase of the chopping period, the signal is uninverted or inverted twice, while the offset voltage effect is either uninverted or inverted. Thus, over a period of the chopping clock, the output signal is mostly not affected, whereas the effects of the input offset are averaged to zero. Ex. 1005 [Huijsing] 1:60-2:1. An example

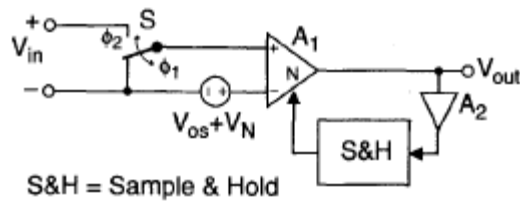
chopper stabilization system is provided by *Huijsing*, where amplifier A1 is stabilized by S1 and S2:



Ex. 1005 [Huijsing] Fig. 2a.

53. Choppers can be constructed with switches having two positions. Ex. 1005 [Huijsing] 1:56-57; *see e.g.*, Ex. 1006 [Tang] Fig. 1; Ex. 1011 [Pertijs] Fig. 1. While choppers aid in reducing the effects of offset voltages, they often produce spurious signals at the amplifier output. Ex. 1011 [Pertijs] 1:45-48.

54. Another method for reducing offset voltage is auto-zeroing. Auto-zeroing systems periodically sample some internal signals when the differential inputs of the amplifier are shorted out and use these sampled signals to compensate for the input offset voltage. Ex. 1011 [Pertijs] 4:5-7. Example auto-zeroing circuitry is provided is provided below:



Ex. 1010 [Enz] Fig. 1(a). In various structures, the auto-zeroing circuitry may couple to the auto-zeroing stage with one or more switches rather than the comparator A_2 . Ex. 1006 [Tang] Fig. 2a; Ex. 1011 [Pertijs] Fig. 1.

55. Often, the auto-zeroing stage (S&H Block) includes one or more capacitors and transconductance stage. Ex. 1010 [Enz] Fig. 2a; Ex. 1006 [Tang] Fig. 2a; Ex. 1011 [Pertijs] 4:12-20. As the amplifier inputs are shorted, the capacitor will store a certain internal value in order to compensate for the input offset voltage, and the transconductance stage will be coupled to the amplifier to compensate or counteract for this offset voltage.

56. Prior to the filing of the '596 Patent, systems had been used which employed both chopping stabilization and auto-zeroing techniques to improve amplifier performance. *See generally*, Ex. 1006 [Tang]; Ex. 1011 [Pertijs].

A. Pertijs

57. *Pertijs* was filed October 15, 2008, and issued on November 16, 2010. Ex. 1011 [Pertijs] Title Page. *Pertijs* provides a ping-pong amplifier structure where both amplifier stages are auto-zeroed and chopper stabilized. Ex. 1011 [Pertijs] Abstract, 2:32-35. For example, Fig. 1 depicts the ping-pong amplifier:

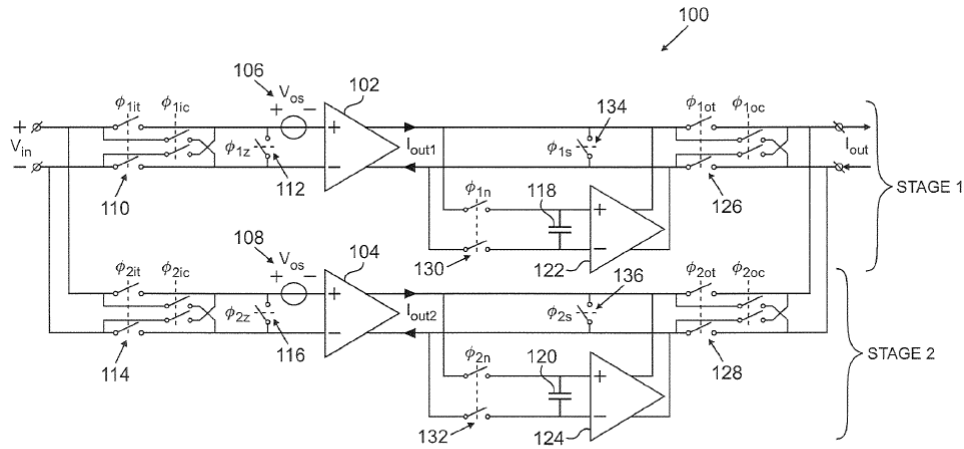


FIG. 1

Ex. 1011 [Pertijs] Fig. 1.

58. Chopper stabilization is performed in this ping-pong amplifier. Ex. 1011 [Pertijs] 2:54-65, 3:1-3, 3:43-48. The first transconductance amplifier 102 has its input chopped by switches 110 and output chopped by switches 126, and the second transconductance amplifier 104 has its input chopped by switches 114 and output chopped by switches 126. Ex. 1011 [Pertijs] Fig. 1, 4:44-51. These switches 110, 114, 126, 128 all act as choppers because they can invert the polarities of the signal inputs. Ex. 1011 [Pertijs] 2:56-58, 3:1-3. Accordingly, they perform chopper stabilization on transconductance amplifiers 102 and 104.

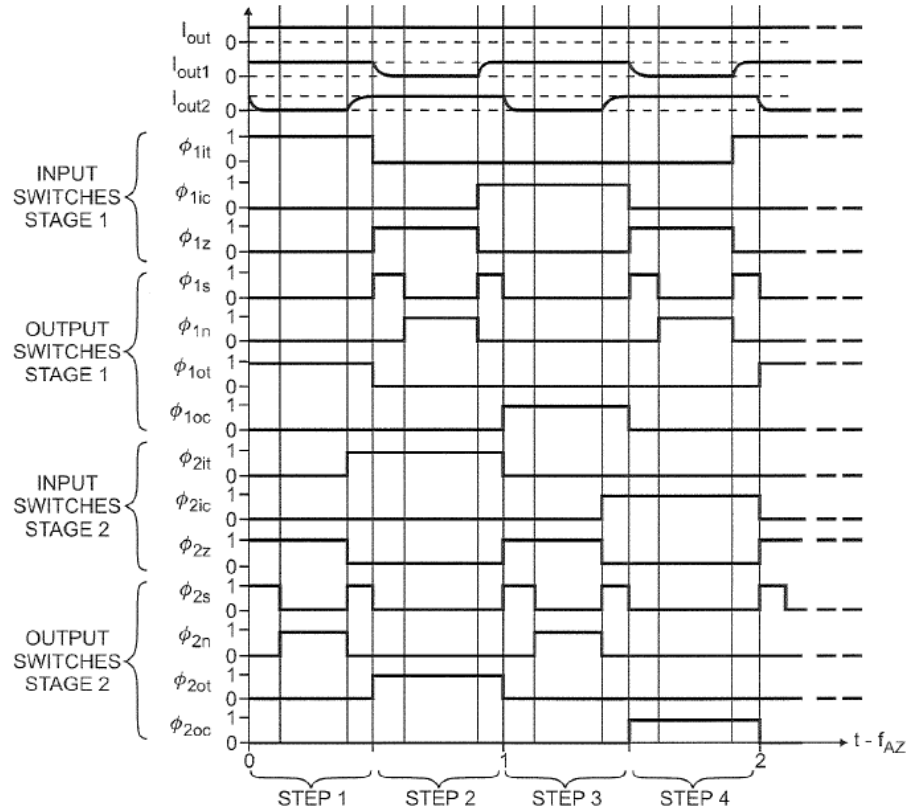
59. The ping-pong amplifier also includes switches 112, 116, 130, 132, differential capacitors 118, 120, and additional transconductance stages 122, 124 which are used to auto-zero the first and second transconductance amplifier 102, 104. Ex. 1011 [Pertijs] 4:5-30. Switches 112, 116 are used to short the inputs of

the amplifiers 102, 104, respectively. Ex. 1011 [Pertijs] 2:65-3:3. Switches 130, 132 couple the transconductance amplifiers 102, 104, to the capacitors 118, 120 and additional transconductance stages 122, 124. Ex. 1011 [Pertijs] 4:12-14. Because the transconductance amplifier 102, 104 inputs are shorted, the differential output current of each amplifier 102, 104 represents the input offset voltage of the transconductance stage. Ex. 1011 [Pertijs] 4:14-20. The transconductance stages 112, 124 compensate for this input offset voltage. Ex. 1011 [Pertijs] 4:17-20.

60. Accordingly, *Pertijs* performs auto-zeroing and chopper stabilization on the same amplifier.

61. *Pertijs* provides the following clock signals to control the various switches in its ping-pong amplifier:

FIG. 2



Ex. 1011 [Pertijs] Fig. 2, 3:51-52.

62. Based on these clock signals, transconductance stage 102 provides an un-inverted output at Step 1, is auto-zeroed at Step 2, provides a twice-inverted output at Step 3, and is auto-zeroed again at Step 4. Ex. 1011 [Pertijs] 4:54-65.

63. Transconductance stage 104 is auto-zeroed at Step 1, provides an un-inverted output at Step 2, is auto-zeroed again at Step 3, and provides a twice inverted output at Step 4. Ex. 1011 [Pertijs] 4:54-65.

B. Tang

64. *Tang* was filed on September 4, 2001, and issued on November 5, 2002. Ex. 1006 [Tang] Cover. *Tang* provides a ping-pong amplifier with both auto-zeroing and chopping capabilities as shown in Fig. 2a:

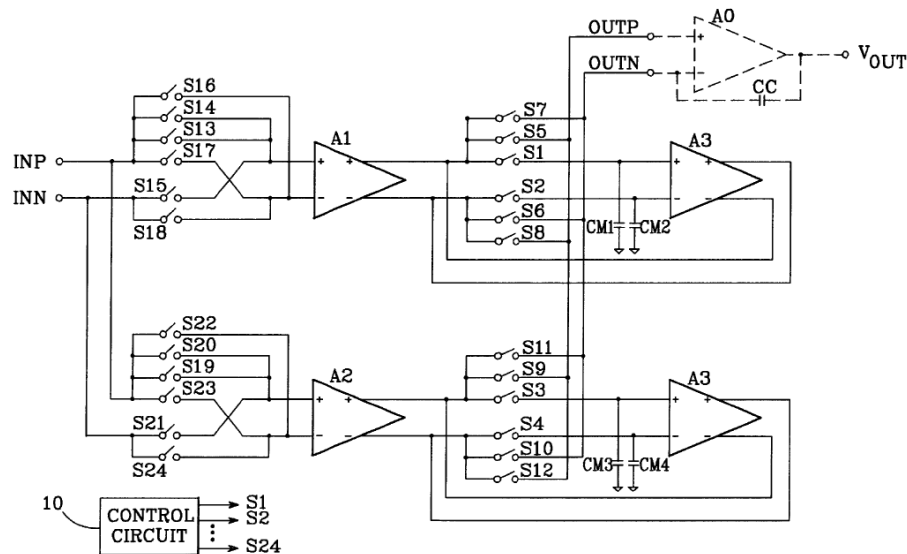


FIG. 2a

Ex. 1006 [Tang] 3:48-50, Fig. 2a. The specification makes reference to a nulling amplifier A4, which I interpret to be the bottom right differential nulling amplifier mistakenly labeled as A3.

65. In a companion paper (*TangPaper*, (Ex. 1008 [TangPaper])) referring to *Tang*, provides more constructive details on his circuit. Ex. 1008 [TangPaper] 1. In particular, *TangPaper* teaches that the ping-pong architecture used “is based on a ping-pong auto-zeroing op-amp such as that of Reference [5]” (Ex. 1008 [TangPaper] 1 citing Ex. 1007 (“Reference [5]”). I am a co-author of Ex. 1007.

66. *Tang's* circuit includes differential gain amplifiers A1 and A2 which receive and communicate signals through a plurality of switches S1-S24. Ex. 1006 [Tang] 3:9-11. Through these switches, the outputs of amplifiers A1 and A2 may be communicated to nulling amplifiers A3, A4 and memory capacitors CM1-CM4. Ex. 1006 [Tang] 3:11-24.

67. To perform auto-zeroing on amplifier A1, S1 and S2 are closed to connect amplifier A1's outputs to the inputs of the nulling amplifier A3 and S14 and S16 are closed together to short A1's inputs. Ex. 1006 [Tang] 3:54-58. The memory capacitors CM1 and CM2 store an offset voltage, which is applied to the inputs of A3 to compensate for the offset voltage. Ex. 1006 [Tang] 3:58-62.

68. To perform auto-zeroing on amplifier A2, switches S3, S4, S20, and S22 are closed to store the corresponding error voltage in memory capacitors CM3 and CM4. Ex. 1006 [Tang] 4:14-18.

69. Amplifier A1 is also chopper stabilized by switches S5-S8, S13, S15, S17, and S18. Ex. 1006 [Tang] 4:23-37. When closed, switches S5, S6, S13, and S18 do not invert the input and output of amplifier A1, while S7, S8, S15, S17 do invert the input and output of amplifier A1 when closed. Ex. 1006 [Tang] 4:23-37. This has the effect of chopping amplifier A1. Ex. 1006 [Tang] 4:35-37.

70. Similarly, amplifier A2 is chopper stabilized by switches S9-12, S19, S21, S23, and S24. When closed, S9, S10, S19, and S24, the inputs and outputs of

amplifier A2 do not get inverted. When switches S11, S12, S21, and S23 are closed, the inputs and outputs of amplifier A2 are inverted. Ex. 1006 [Tang] 4:1-14. This has the effect of chopping amplifier A2. Ex. 1006 [Tang] 4:12-14.

71. The switches S1-S24 form what *Tang* describes as a switching network which is controlled by the control circuit 10 which uses a four-phase timing cycle. Ex. 1006 [Tang] 3:50-54. One example timing cycle is provided in Fig. 4d:

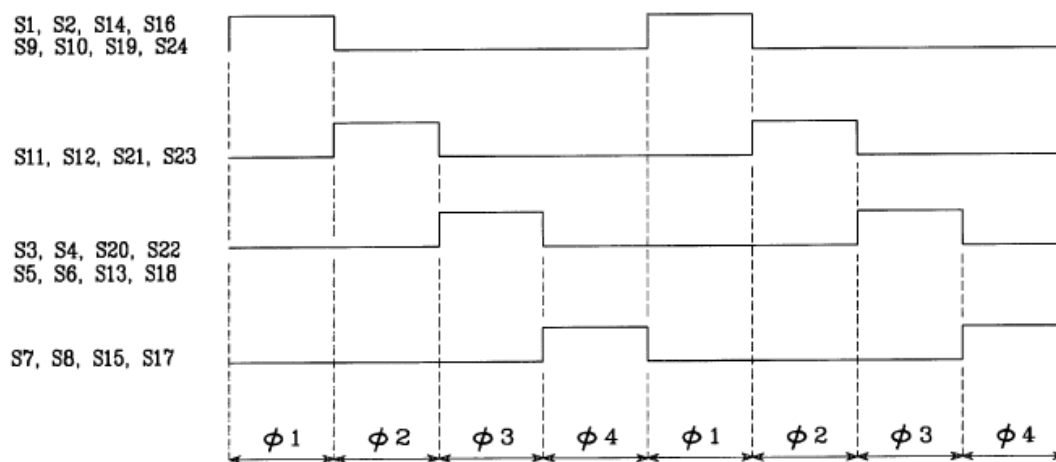


FIG.4d

Ex. 1006 [Tang] Fig. 4d.

72. Based on the timing cycle described in Fig. 4d, amplifier A1 is auto-zeroed during $\Phi 1$, and is chopper stabilized over $\Phi 3$ and $\Phi 4$. During $\Phi 2$, none of the corresponding switches are closed to provide amplifier A1 any inputs.

73. Amplifier A2 is chopper stabilized over $\Phi 1$ and $\Phi 2$, and amplifier A1 is auto-zeroed over $\Phi 3$. During $\Phi 4$, none of the corresponding switches are closed to provide amplifier A2 any inputs.

74. Alternative timing arrangements are also taught by *Tang*. For example, Fig. 4e depicts a timing cycle with eight separate phases $\Phi 1$ - $\Phi 8$:

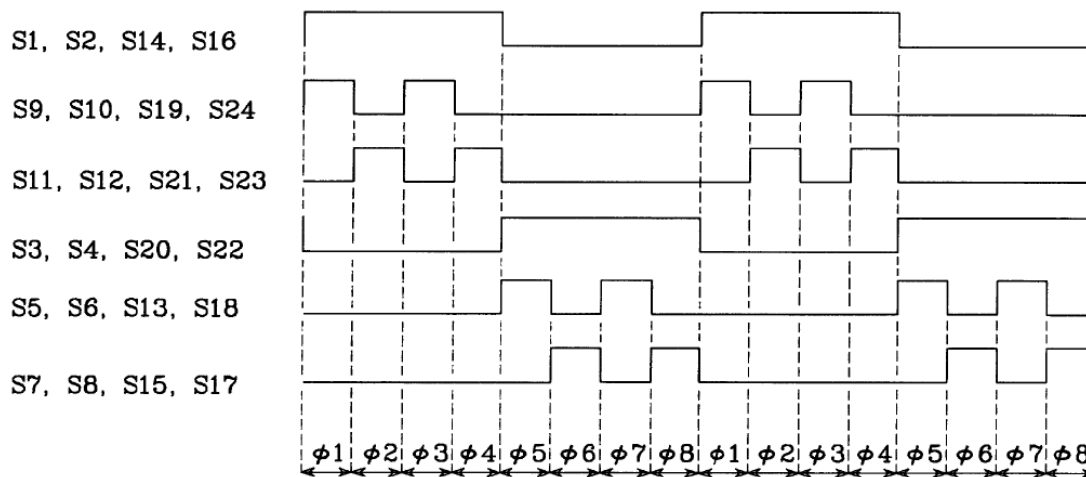
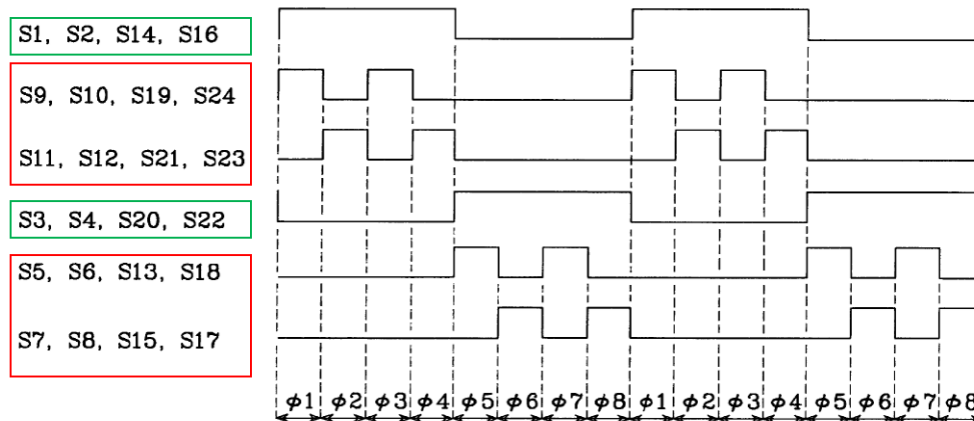


FIG.4e

Ex. 1006 [Tang] Fig. 4e. For clarity, Fig. 4e is annotated below with the switches used in auto-zeroing (in green) and the switches used in chopper stabilization (in red) for both amplifiers A1 and A2:

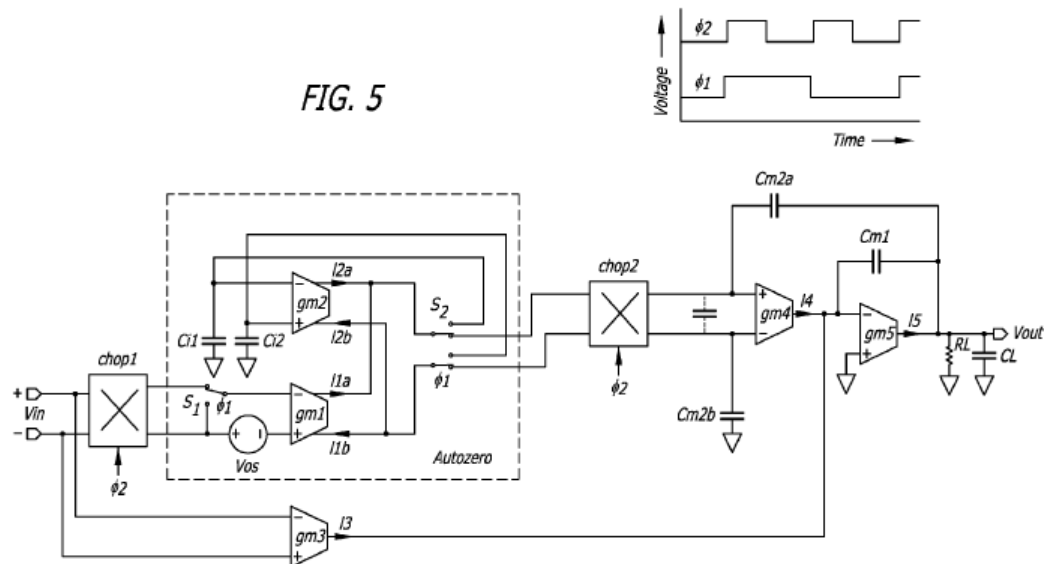


Ex. 1006, Fig. 4e.

75. In Fig. 4e, multiple chopping cycles are performed during each auto-zero period. Ex. 1006 [Tang] 4:59-62. For example, in $\Phi 1$ - $\Phi 4$, a single auto-zeroing cycle is performed on the first amplifier A1 (through switches S1, S2, S14, and S16) while two chopping cycles are performed on the second amplifier A2 (through switches S9-S12, S19, S21, S23, and S24). Likewise, during $\Phi 5$ - $\Phi 8$ a single auto-zeroing cycle is performed on the second amplifier A2 (through switches S3, S4, S20, and S22) and two chopping cycles are performed on the first amplifier A1 (through switches S5-S8, S13, S15, S17, and S18).

V. THE '596 PATENT

76. Much like *Tang* and *Pertijs*, the '596 Patent is directed towards opamp systems which use both chopper stabilization and auto-zeroing. Ex. 1001 ['596 Patent] Abstract, Cls. 21-22, 5:49-52. For example, Fig. 5 of the '596 Patent provides a circuit which auto-zeroes an amplifier between two choppers.



Ex. 1001 [’596 Patent] Fig. 5. Fig. 5 is constructed so that the choppers (chop₁ and chop₂) invert the input polarity based on one clock phase ($\Phi2$) while the autozeroing cycle is performed based on the timing of another clock phase ($\Phi1$). Various timing arrangements may be assigned to these systems. *See e.g.*, Ex. 1001 [’596 Patent] Fig. 9.

77. During prosecution, the Examiner rejected Claims 21 and 22 (originally Claims 26 and 27 during prosecution) based on *Huijsing* (Ex. 1005). Ex. 1002 [File History] 247-249. To overcome the Examiner’s rejection, Applicant argued that “[c]laim 26 includes the limitation that the second frequency is twice the first frequency and has a duty cycle of less than one half, whereas claim 27 is similar, though requires that the second frequency have a duty cycle of not more than one quarter, neither of which limitations is disclosed or rendered

obvious by the cited art.” Ex. 1002 [File History] 268. However, the prior art references *Pertijs* (Ex. 1011) and *Tang* (Ex. 1006) disclose these limitations.

VI. CLAIM CONSTRUCTION

78. I have been informed by counsel that claim terms must receive their ordinary and customary meaning as would have been understood by a POSITA based on the specification, prosecution history, and extrinsic evidence.

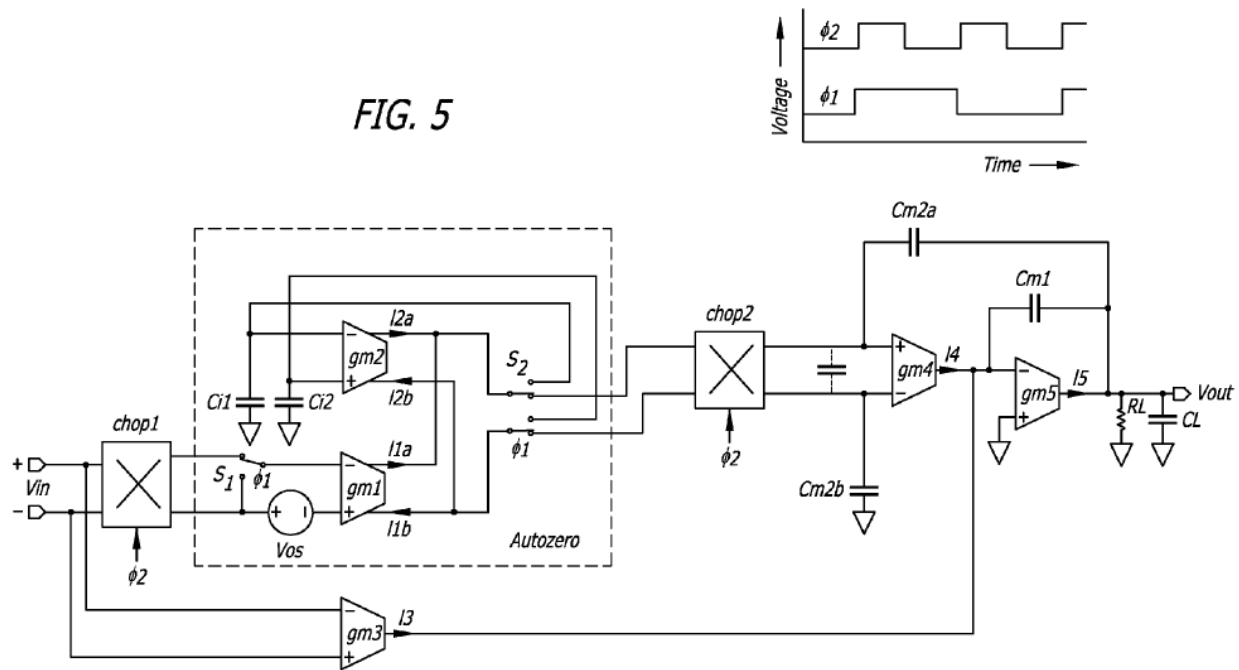
A. “operating the chopper stabilization at a first frequency” and “operating the auto-zeroing at a second frequency”

79. The ’596 Patent does not explicitly define the “the first frequency” or “the second frequency[.]” Instead, both terms are explained by embodiments relating the frequencies of operation of the chopper stabilization and auto-zeroing systems.

80. I interpret the first frequency in the term “operating the chopper stabilization at a first frequency” to mean “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle.”

81. I interpret the second frequency in the term “operating the auto-zeroing at a second frequency” to mean “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle.”

82. Fig. 5 of the '596 Patent provides two different clocks (Φ_1 and Φ_2) used to operate the auto-zeroing and chopper stabilization circuit elements respectively. Ex. 1001, Fig. 5, 5:58-65. Fig. 5 is depicted below:



Ex. 1001 Fig. 1.

83. When Φ_1 is high, the switch S_1 shorts the inputs of the input stage gm_1 , and the switches S_2 couple the inputs of the gm_2 stage to its outputs. In this state, the amplifier with gm_1 and gm_2 enters auto-zero mode. When Φ_1 is low, the switch S_1 couples the gm_1 input to the $chop_1$ output, the switches S_2 couple the outputs of gm_1 and gm_2 to the inputs of $chop_2$, and the amplifier with gm_1 and gm_2 enters normal operation. The output current of gm_2 compensates for the input referred offset V_{os} . Ex. 1001, 5:55-60.

87. Fig. 9 includes the same circuitry as Fig. 5. Unlike in Fig. 5 where the auto-zeroing frequency is half the chopping frequency, the auto-zeroing operates at twice the chopping frequency. Ex. 1001, 6:60-63. In Fig. 9, the auto-zeroing clock Φ_1 has one active pulse in a full cycle period. Meanwhile, the chopper stabilization clock Φ_2 has also one active pulse in a full cycle period, but the full cycle period of chopper stabilization clock Φ_2 is twice as long as the period of a full cycle period of the auto-zeroing clock Φ_1 (in other words, Φ_1 repeats twice in the time Φ_2 repeats once). In this case, the chopping frequency is half the auto-zeroing frequency.

88. Fig. 11 depicts an alternative embodiment of Fig. 9, where the chopper stabilizers are implemented as an array of switches:

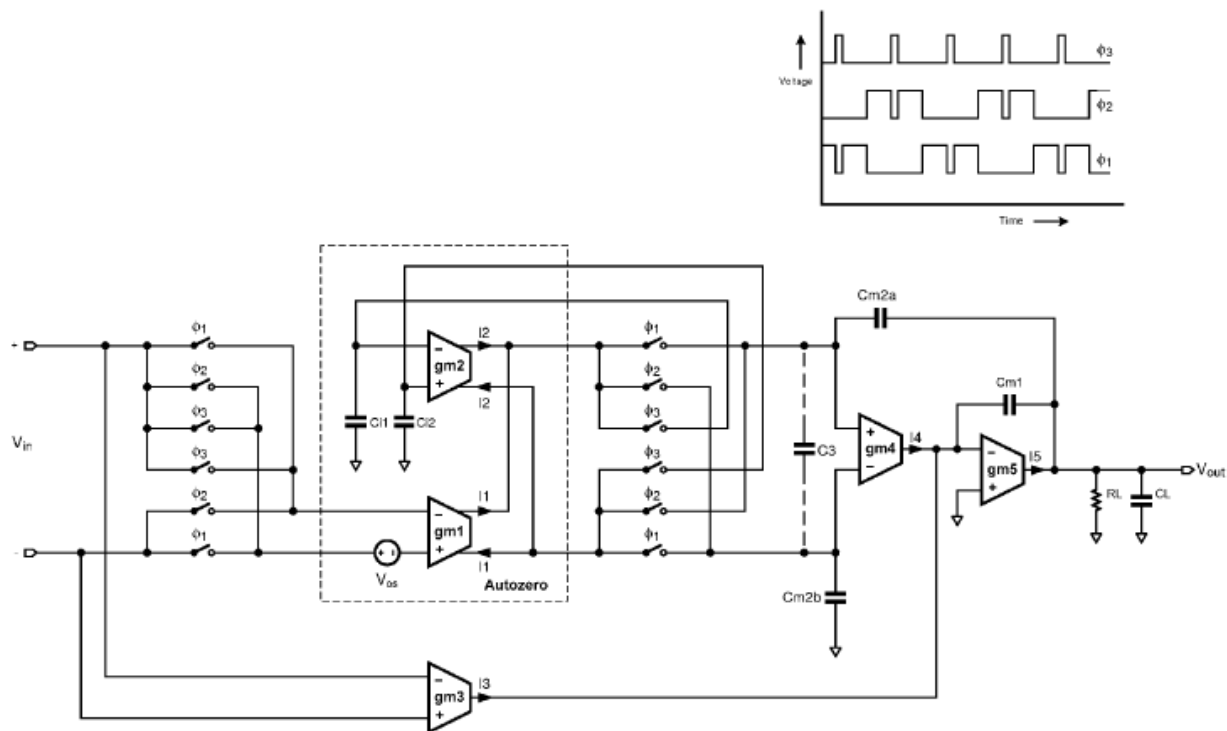
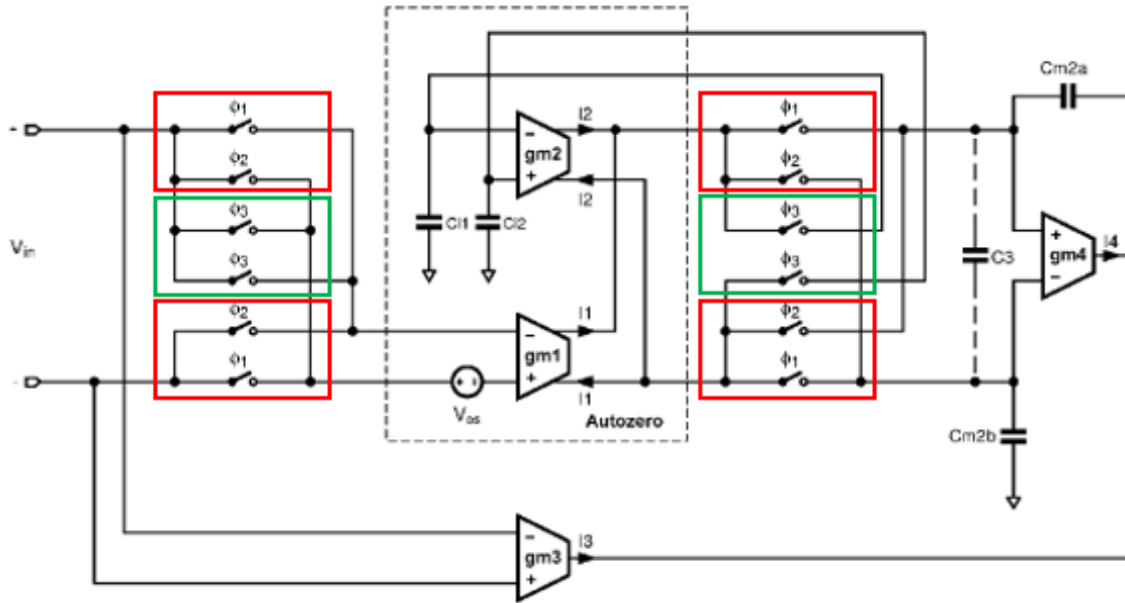


Fig. 11

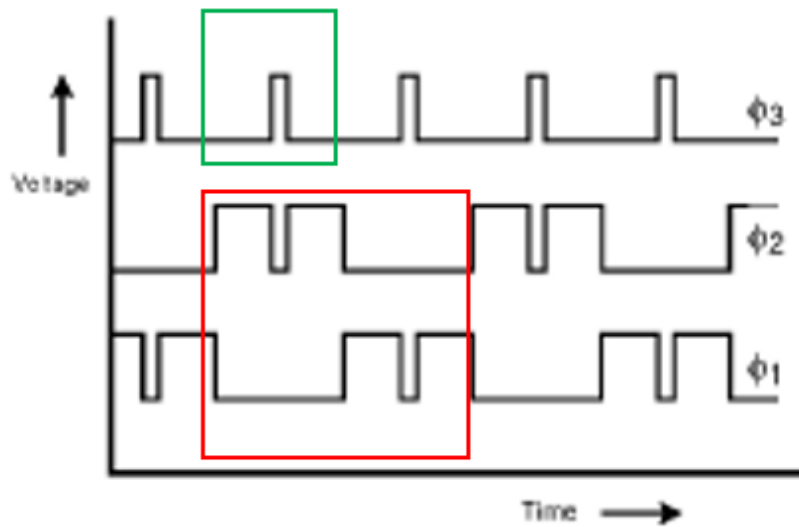
Ex. 1001, Fig. 11, 7:25.

89. The chopper switches are controlled by Φ_1 and Φ_2 . These switches perform chopper stabilization by providing uninverted and inverted polarities at both the inputs and outputs of the amplifier with g_{m1} and g_{m2} . Ex. 1001, 7:40-62. The auto-zeroing switches are controlled by Φ_3 . These switches short the input of the amplifier during the auto-zeroing mode. The chopping switches are shown in red and the auto-zeroing switches are shown in green:



Ex. 1001, Fig. 11.

90. The timing arrangement is also annotated below:



Ex. 1001, Fig. 11.

91. The pulse pattern of the auto-zeroing switch (Φ_3) is annotated in **green**. In this period, Φ_3 has one active pulse and repeats at the end of the **green** box.

92. The pulse pattern of the chopper stabilization switches (Φ_1 and Φ_2) is annotated in **red**. In this period, Φ_1 and Φ_2 each have one active pulse and repeats at the end of the **red** box. Each active pulse is interrupted by the auto-zeroing process, but only one active pulse occurs in the **red** box. There is only one inversion of the input/output signals due to chopping signals Φ_1 and Φ_2 in the red box.

93. As shown, the auto-zeroing cycle in **green** repeats twice for every one chopper cycle period in **red**. Accordingly, the auto-zeroing frequency is twice the chopping frequency as described in the '596 Patent. Ex. 1001, 6:60-63, 7:58-62.

94. As shown through these examples, my interpretation that “first frequency” (the chopper stabilization frequency), means “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle” and, the “second frequency” (the auto-zeroing frequency) means “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle” is supported by the specification and would be understood by a POSITA.

B. “the ratio of the two frequencies being two to one” [claim 22]

95. I interpret “the ratio” in the ’596 Patent as requiring either (1) that the auto-zeroing frequency (the second frequency) is twice the chopping frequency (the first frequency) or (2) that the chopping frequency (the first frequency) is twice the auto-zeroing frequency (the second frequency). Such construction is also supported by disclose in the specification the ’596 Patent. Ex. 1001 [’596 Patent] 6:61-62, Fig. 5, Fig. 9.

96. Note that this construction is not necessary for Claim 21 despite this limitation being included in Claim 21. Claim 21 includes an additional limitation which requires “the second frequency being twice the first frequency[.]” Ex. 1001 [’596 Patent] Cl. 21. So, the chopping frequency (first frequency) being twice the auto-zeroing frequency (the second frequency) would not be permitted in claim 21, despite being permitted for the claimed *ratio*.

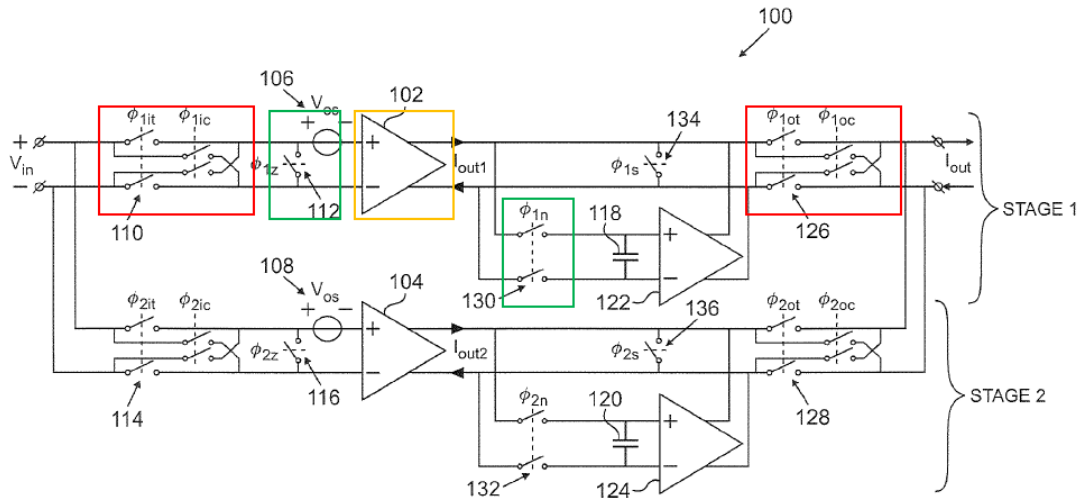
VII. GROUND 1 - PERTIJS

A. Claim 21

- 1. [21pre] A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:**

97. I offer no opinion as to whether the preamble is limiting. To the extent the preamble is limiting, it is obvious in light of *Pertijs*.

98. *Pertijs* discusses a chopper stabilized and auto-zeroed amplifier. Ex. 1011 [Pertijs] 2:32-35, Fig. 1. Indeed, as annotated below, Fig. 1 depicts an amplifier (yellow) and switches used for chopper stabilization (red) and switches used in *Pertijs* auto-zeroing protocol (green):



Ex. 1011 [Pertijs] Fig. 1, 2:32-35.

99. The switches 110, 126 are used to receive a signal and either provide that signal or provide an inverted signal at their outputs. Ex. 1011 [Pertijs] 3:59-61. Meanwhile, the capacitor 118 and additional transconductance stage 122 are used to compensate the offset voltage of the amplifier. Ex 1011, 2:65-3:1, 3:61-63. Stage 2 of *Pertijs* provides the same structure as Stage 1. Ex. 1011 [Pertijs] 2:38-45, 3:1-3, 4:29-30.

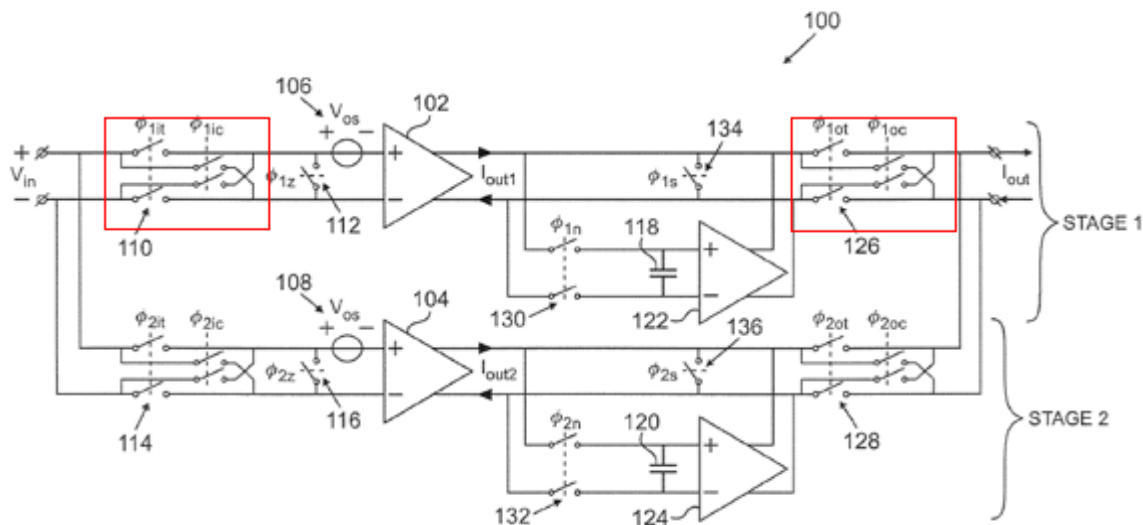
100. So, *Pertijs* also depicts an amplifier with chopper stabilization and auto-zeroing capabilities.

2. [21a] operating the chopper stabilization at a first frequency; and

101. This limitation is obvious in light of *Pertijs*.

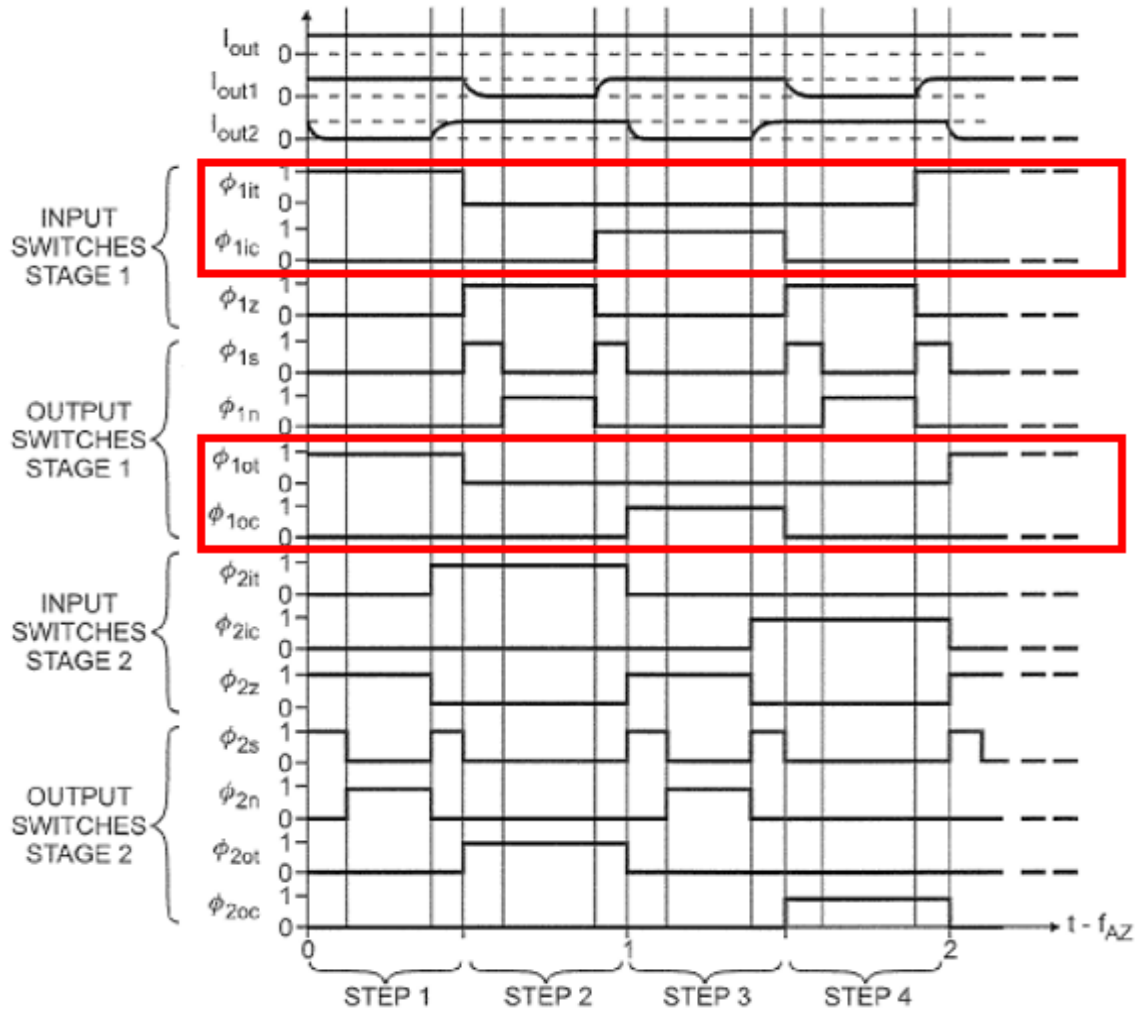
102. The operation frequency of the chopper stabilization, i.e., the “first frequency” is “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle” as described in Section VI.A.

103. The chopper stabilization is performed by switches 110 and 126 (annotated in red) which periodically invert the polarities of their input signal:



Ex. 1011 [Pertijs] 3:59-61.

104. As annotated in red Switches 110 are opened and closed according to clock signals Φ_{1it} and Φ_{1ic} as shown while switches 126 are opened and closed according to the clock signals Φ_{1ot} and Φ_{1oc} :



Ex. 1011 [Pertijs] Fig. 2.

105. During Step 1, switch 110 provides a direct connection between the system inputs and the transconductance amplifier 110 inputs, and switch 126 provides a direct or uninverted connection between the transconductance amplifier 110 output and the system outputs. Ex. 1011 [Pertijs] 4:46-51. During Step 3, switch 110 provides an inverted connection (i.e. cross-connected) between the system inputs and the transconductance amplifier 110 inputs, and switch 126 provides an inverted connection between the transconductance amplifier 110

outputs and the system outputs. Ex. 1011 [Pertijs] 4:46-51. In other words, switches 110, 126 perform chopper stabilization by periodically inverting their output signals. Ex. 1011 [Pertijs] 3:59-61.

106. When the transconductance amplifier 102 has an uninverted connection (or a straight connection) the system is in a first state. When the input and output of amplifier 102 have inverted connections (so the signal is twice inverted), the system is in a second state. Although the output switches 126 closes slightly after the input switches 110, such lag does not change the frequency of the chopping.

107. The input switches 110 and output switches 126 (controlled by clock signals Φ_{lit} , Φ_{lic} , Φ_{lot} , and Φ_{loc}) include one pulse in a complete cycle period which repeats after STEP 4.

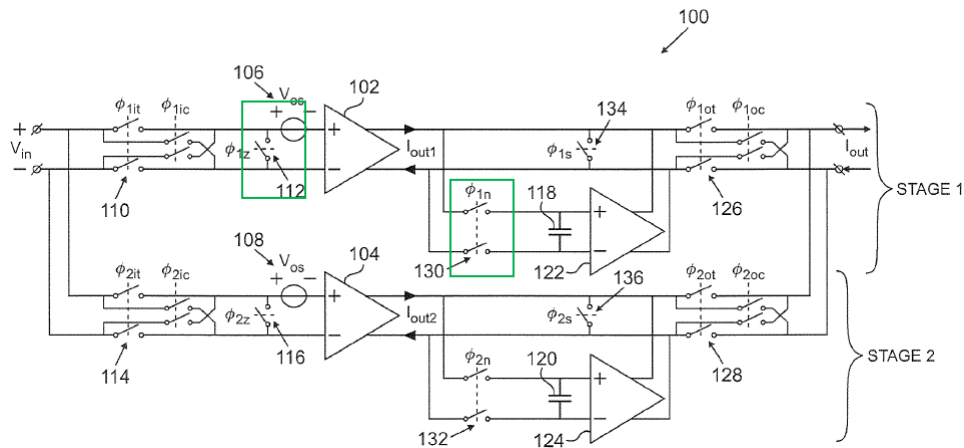
108. So, the first frequency is $1/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$.

3. [21b] operating the auto-zeroing at a second frequency;

109. This limitation is obvious in light of *Pertijs*.

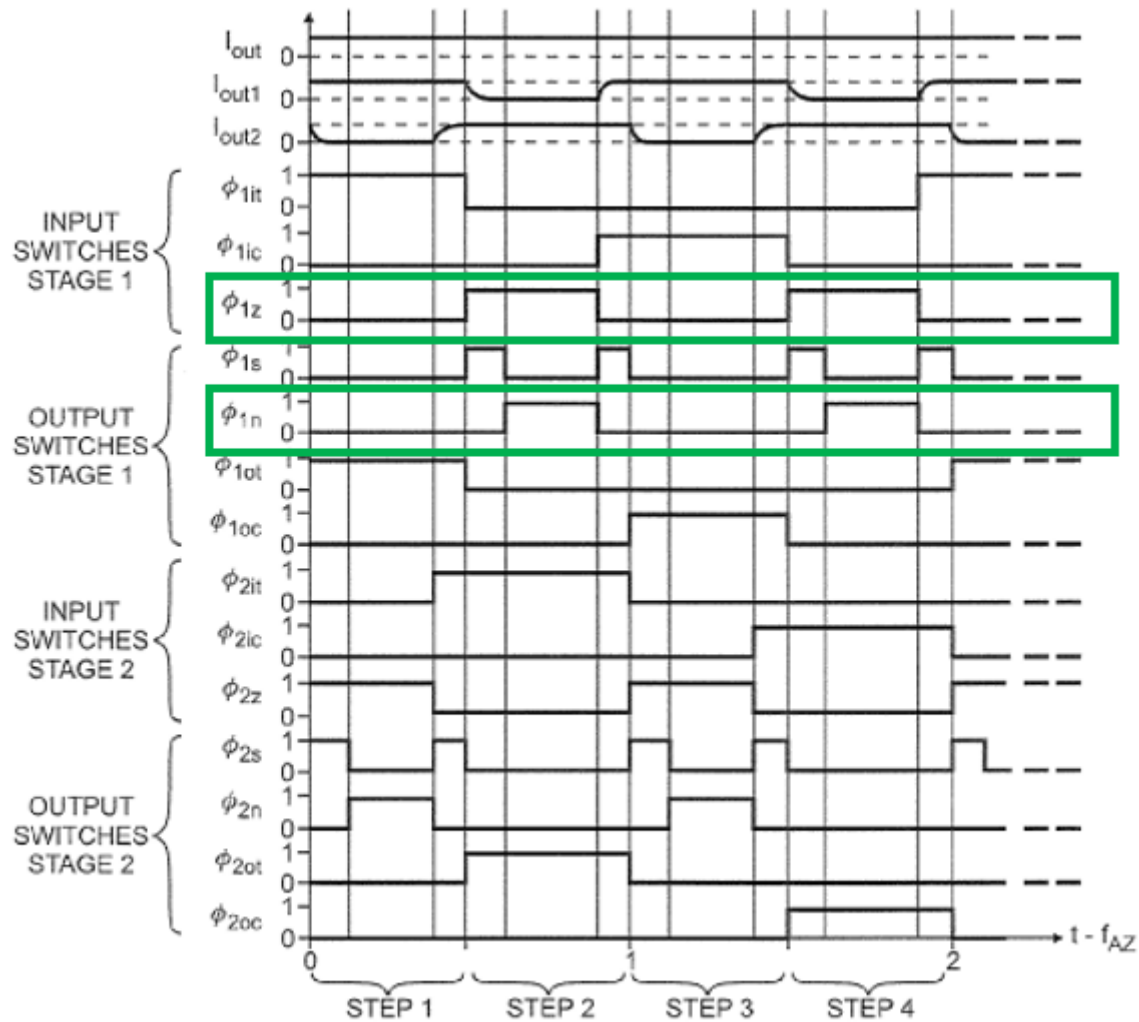
110. The operation frequency of the auto-zeroing, i.e., the “second frequency” is “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle” as described in Section VI.A.

111. In *Pertijs*, the auto-zeroing cycle is performed on transconductance amplifier 102 when switches 106 and 130 (annotated in green) are closed:



Ex. 1011 [Pertijs] Fig. 1. Switch 112 shorts the input of the transconductance amplifier 102. Ex. 1011 [Pertijs] 2:65-3:1. Switch 130 couples the transconductance amplifier 102 to the capacitor 118 and additional transconductance stage 122 which are necessary for the auto-zeroing cycle. Ex. 1011 [Pertijs] 4:12-14.

112. The auto-zeroing cycle is performed on transconductance amplifier 102 at Step 2 and Step 4. Ex. 1011 [Pertijs] 4:57-60, 4:63-65. As annotated in green, the auto-zeroing cycle is performed when switch 112 is closed based on Φ_{1z} and switches 130 is closed based on clock Φ_{1n} :



Ex. 1011 [Pertijs] Fig. 2.

113. Auto-zeroing switches 112 and 139 (controlled by clock signals Φ_{1z} and Φ_{1n}) both have two active pulses in a full cycle period (that repeats after STEP 4).

114. So, the second frequency is $2/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$.

4. [21c] the ratio of the frequencies being two to one;

115. This limitation is obvious in light of *Pertijs*. As described in Sections VII.A.2 and VII.A.3, the first frequency is $1/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$ while the second frequency is $2/(\text{Step 1} + \text{Step 2} + \text{Step 3} + \text{Step 4})$. *Pertijs* itself indicates that “the chopping performed in the amplifier 100 is performed at half the auto-zeroing frequency f_{AZ} .” Ex. 1011 [Pertijs] 4:44-46.

116. Accordingly, the ratio of the frequencies is two to one.

**5. [21d] the second frequency being twice the first frequency
and**

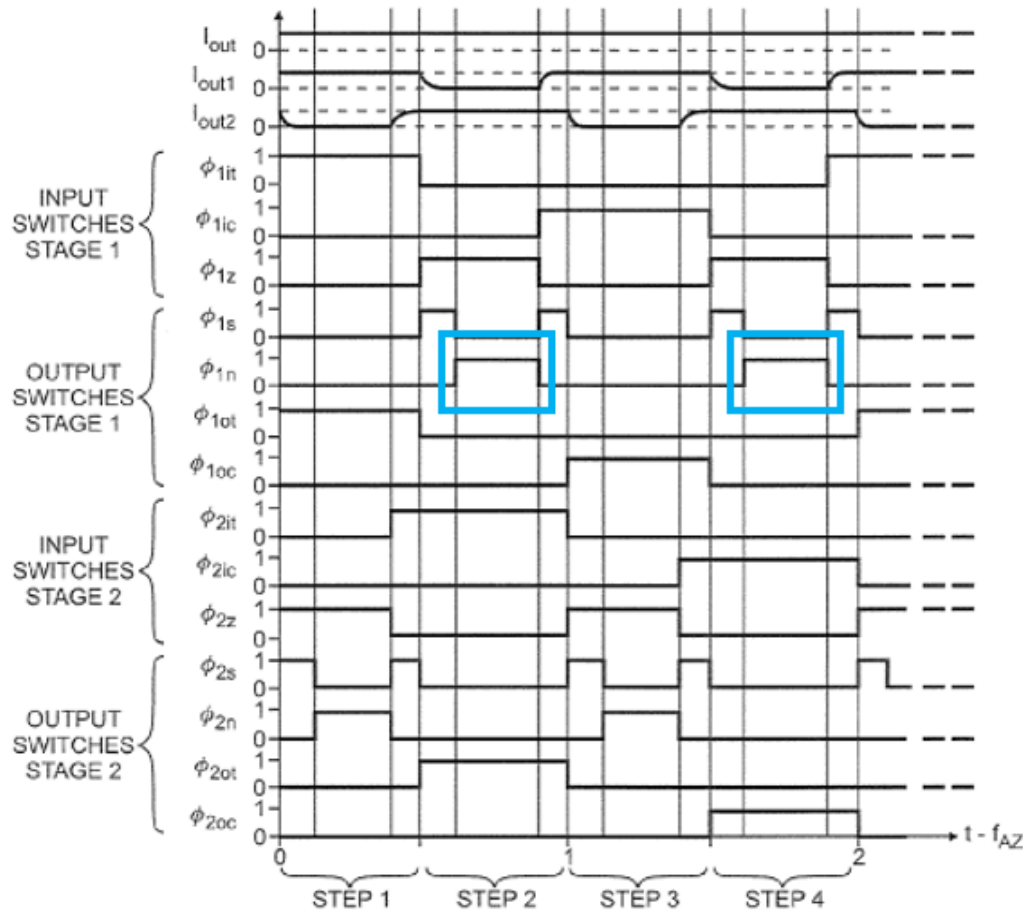
117. This limitation is obvious in light of *Pertijs*. As noted in Section VII.A.4, the auto-zeroing frequency F_{AZ} is twice the chopping frequency. Ex. 1011 [Pertijs] 4:44-46, 4:66-5:5.

**6. [21e] [the second frequency] having a duty cycle of less than
one half.**

118. This limitation is obvious in light of *Pertijs*. *Pertijs* does not explicitly state that Steps 1, 2, 3, and 4, of Fig. 2 are each equal lengths of time. Irrespective of the relative sizes of Steps 1-4, this limitation is obvious.

119. First, if Steps 1, 2, 3, and 4 are equal the duty cycle of the auto-zeroing cycle would be less than one half. As noted in blue, the auto-zeroing cycle

of the transconductance amplifier 102 occurs only during a portion of Step 2 and a portion of Step 4:

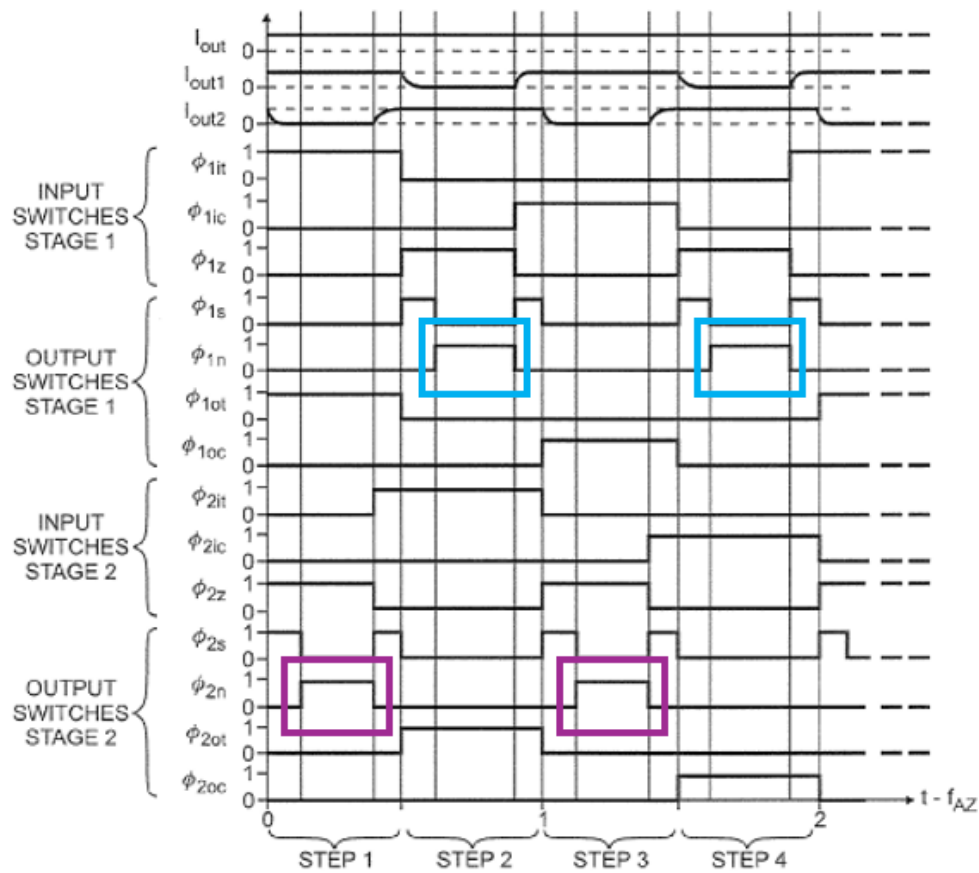


Ex. 1011 [Pertijs] Fig. 2. The auto-zeroing cycles of Step 2 and Step 4 only begins once the first transconductance amplifier 102 is coupled to the capacitor 118 and additional transconductance stage 122 when coupled to them by switches 130. Accordingly, if each step is of the same length, the duty cycle of the auto-zeroing circuitry is less than half.

120. Second, even if Steps 1-4 are unequal, *Pertijs* still renders obvious an auto-zeroing cycle with a duty cycle of less than one half.

121. Ping-pong amplifier systems are configured to have alternating outputs between two similar amplifiers. Stage 2 of *Pertijs* (with transconductance amplifier 104) provides the same structure to Stage 1. Ex. 1011 [Pertijs] 2:38-45, 3:1-3, 4:29-30. My opinion regarding the elements and teachings of Stage 1 (described in elements [21pre] [21a], [21b], [21c], and [21d] are also true for the corresponding elements and time intervals described for Stage 2. Accordingly, the duty cycle for auto-zeroing of either Stage 1 or Stage 2 renders this limitation obvious.

122. In the case of *Pertijs*, transconductance amplifiers 102 and 104 also alternate performance of auto-zeroing cycles during Steps 1-4 as annotated (in blue and purple respectively) below:



Ex. 1011 [Pertijs] Fig. 2.

123. Due to this alternating nature and the symmetric configuration of the system depicted in *Pertijs*, at least one of the transconductance amplifiers 102 or 104 has an auto-zeroing cycle of less than one half over the period of Step 1 to Step 4.

124. For example, if Step 1 (or Step 3) is longer than each of the three remaining steps, then the duty cycle of the auto-zeroing cycle for transconductance amplifier 102 will be less than half. Likewise, if Step 2 (or Step 4) is longer than

each of the three other steps, then the duty cycle of the auto-zeroing cycle for transconductance amplifier 104 will be less than half.

125. As none of the auto-zeroing cycles occupy the entirety of any Step 1-4, no combination of time lengths results in both transconductance amplifiers 102 and 104 both having auto-zeroing cycles with duty cycles greater than one half.

126. Therefore, irrespective of the relative sizes of Steps 1-4, this limitation is obvious.

B. Claim 22

1. **[22pre] A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:**

127. I offer no opinion as to whether the preamble is limiting. To the extent the preamble is limiting, it is obvious in light of *Pertijs*. *See supra* Section VII.A.1.

2. **[22a] operating the chopper stabilization at a first frequency; and**

128. This limitation is obvious in light of *Pertijs*. *See supra* Section VII.A.2.

3. [22b] operating the auto-zeroing at a second frequency;

129. This limitation is obvious in light of *Pertijs*. See *supra* Section VII.A.3.

4. [22c] the ratio of the frequencies being two to one;

130. This limitation is obvious in light of *Pertijs*. See *supra* Section VII.A.4.

5. [22d] the second frequency having a duty cycle of not more than one-quarter.

131. This limitation is obvious in light of *Pertijs*. It would be obvious to implement the auto-zeroing circuitry to have a duty cycle of not more than one-quarter.

132. *Pertijs* teaches a variety of modifications and notes that “this architecture could be extended to an amplifier having an arbitrary number of stages. In some embodiments, one stage is auto-zeroed at any point in time, while the overall output signal I_{out} represents the sum of the outputs of the remaining stages.” Ex. 1011 [Pertijs] 5:63-67. *Pertijs* states that “the overall supply current needed to obtain a given noise performance can be less than that of a two-stage chopped auto-zeroed ping-pong amplifier.” Ex. 1011, [Pertijs] 5:67-6:4.

133. It would be obvious to construct a system, as described in *Pertijs*, to include an auto-zeroing cycle of at least one of the amplifiers having a duty cycle of not more than one-quarter. For example, consider an embodiment of *Pertijs* where there are four separate stages. In the four-stage system, one stage would perform auto-zeroing at a time, while the remaining three amplifiers provide the output signal. Ex. 1011 [*Pertijs*] 5:63-67.

134. One such implementation is provided below:

	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8
Stage 1	AZ	Uninverted			AZ	Twice Inverted		
Stage 2		AZ	Uninverted			AZ	Twice Inverted	
Stage 3	Uninverted		AZ	Twice Inverted			AZ	
Stage 4	Uninverted			AZ	Twice Inverted			AZ

135. The timing arrangement is consistent with *Pertijs* description that the chopper stabilization is performed at half the auto-zeroing frequency. Ex. 1011 [*Pertijs*] 4:44-46.

136. Each stage has stage has 3 steps with uninverted inputs and outputs (in green), 3 steps with twice inverted inputs and outputs (in blue) and 2 steps in auto-zeroing mode (AZ, in white) over an 8-step cycle. The cycle would repeat every 8 steps.

137. This implementation is consistent with the auto-zeroing cycle being performed at twice the chopper stabilization frequency because the auto-zeroing switches have one pulse every 4 steps (so two pulses every 8 steps) while the chopper stabilization switches would have one pulse every eight steps.

138. If each auto-zeroing cycle is performed for an equal amount of time, no auto-zeroing cycle would have a duty cycle of more than one-quarter. *See* Ex. 1011 [Pertijs] Fig. 2 (indicating the auto-zeroing cycle occupy less than a full step).

139. Even if each stage performs the auto-zeroing cycle an unequal amount of time, at least one of the stages will perform auto-zeroing for not more than one quarter.

140. Accordingly, *Pertijs* teaches the auto-zeroing cycle having a duty cycle of less than one-quarter.

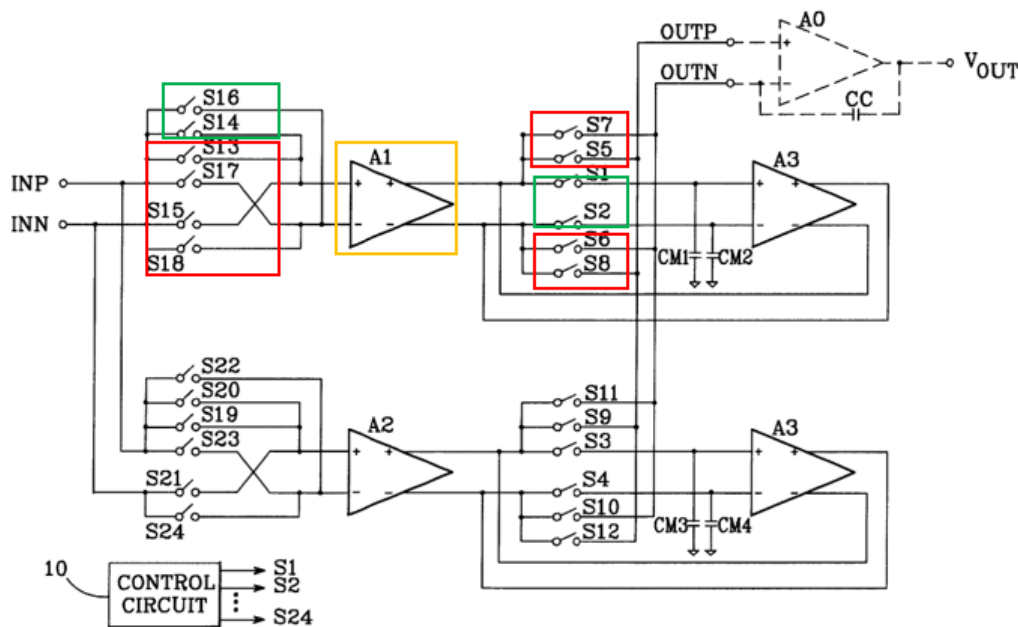
VIII. GROUND 2 - TANG

A. Claim 22

1. [22pre] A method of operating a chopper stabilized first amplifier, the chopper stabilized first amplifier having an auto-zeroing capability comprising:

141. I offer no opinion as to whether the preamble is limiting. To the extent the preamble is limiting, it is obvious in light of *Tang*.

142. *Tang* describes a circuit that employs both auto-zeroing and chopping techniques. Ex. 1006 [Tang] 1:66-2:1. *Tang's* system includes an amplifier A1 (in yellow) and a switch network that includes switches used for chopper stabilization (in red) and auto-zeroing (in green):



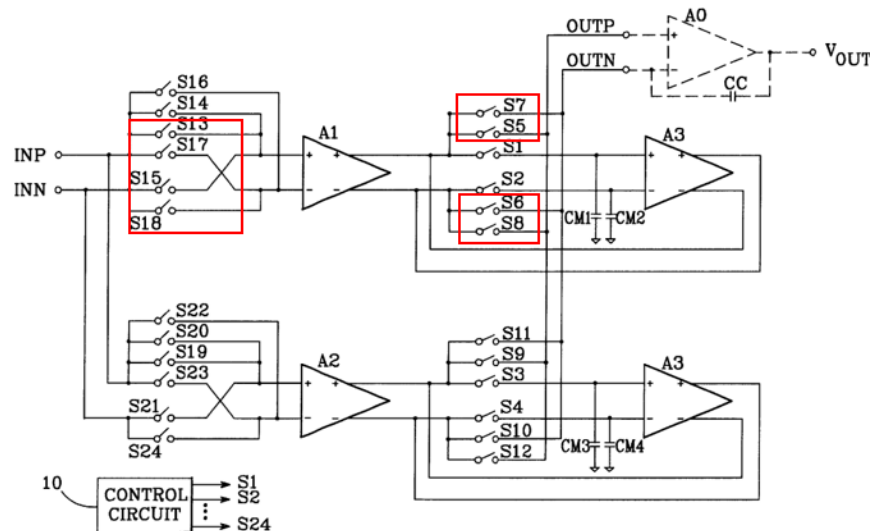
Ex. 1006 [Tang] Fig 2a.

2. [22a] operating the chopper stabilization at a first frequency; and,

143. This limitation is obvious in light of *Tang*.

144. The operation frequency of the chopper stabilization, i.e., the “first frequency” is “the number of active pulses of a chopper switch in a full cycle period divided by the period of the cycle” as described in Section VI.A.

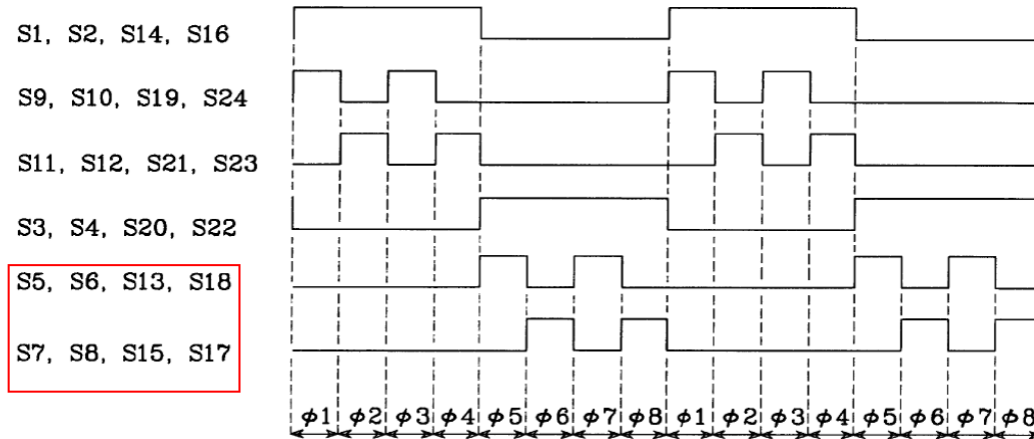
145. Switches S6-8, S13, S15, S17, and S18 open and close to have the effect of chopping the input and output signals of amplifier A1. Ex. 1006 [Tang] 4:23-37. These switches are annotated in red below:



Ex. 1011 [Pertijs] Fig. 2a. The switches in *Tang's* switch network are controlled by the control circuit 10. Ex. 1006, 3:49-51

146. When switches S5, S6, S13, and S16, are closed, the input and output of amplifier A1 are not inverted. When switches S15, S17, S7, and S8 are closed,

the inputs and outputs of the amplifier A1 are inverted. One of the timing arrangements provided in *Tang* illustrates amplifier A1 being chopper stabilized by the switches annotated in red:



Ex. 1006 [Tang] Fig. 4e.

147. As shown, at $\Phi 5$ and $\Phi 7$, switches S5, S6, S13, and S18 are closed, providing uninverted connections for the input and output of amplifier A1. In other words, the positive input voltage INP is coupled to the positive input of amplifier A1 (by S13) and the positive amplifier A1 output is coupled to OUTP (by S5), while the negative input voltage INN is coupled to the negative input of amplifier A1 (by S18) and the negative amplifier A1 output is coupled to OUTN (by S6).

148. At $\Phi 6$ and $\Phi 8$, switches S5, S6, S13, and S18 are opened and switches S7, S8, S15, and S17 are closed. This couples the positive input voltage INP to the negative input of amplifier A1 (by S17) and the positive amplifier A1 output is

coupled to OUTP (by S8). The negative input voltage INN is coupled to the positive input of amplifier A1 (by S15) and the negative amplifier A1 output is coupled to OUTN (by S7).

149. The chopper stabilization switches S5, S6, S7, S8, S13, S15, S17, and S18 each have two pulses in a full cycle period (which repeats every $\Phi 1$ to $\Phi 8$).

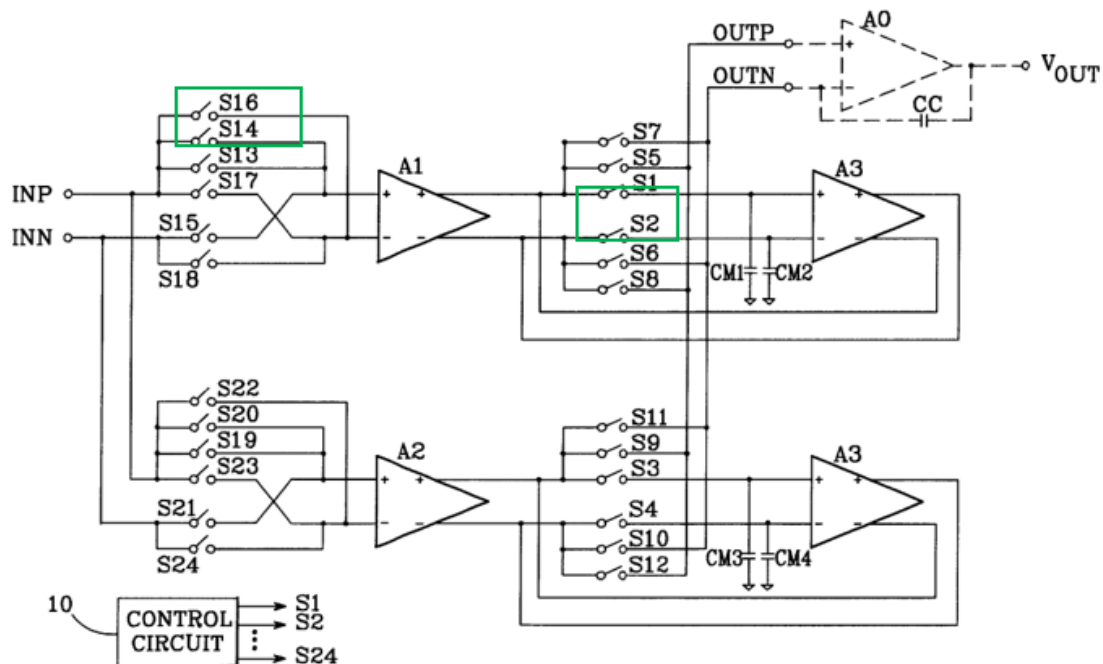
150. Therefore, the first frequency is $2/(\Phi 1 \text{ to } \Phi 8)$.

3. [22b] operating the auto-zeroing at a second frequency;

151. This limitation is obvious in light of *Tang*.

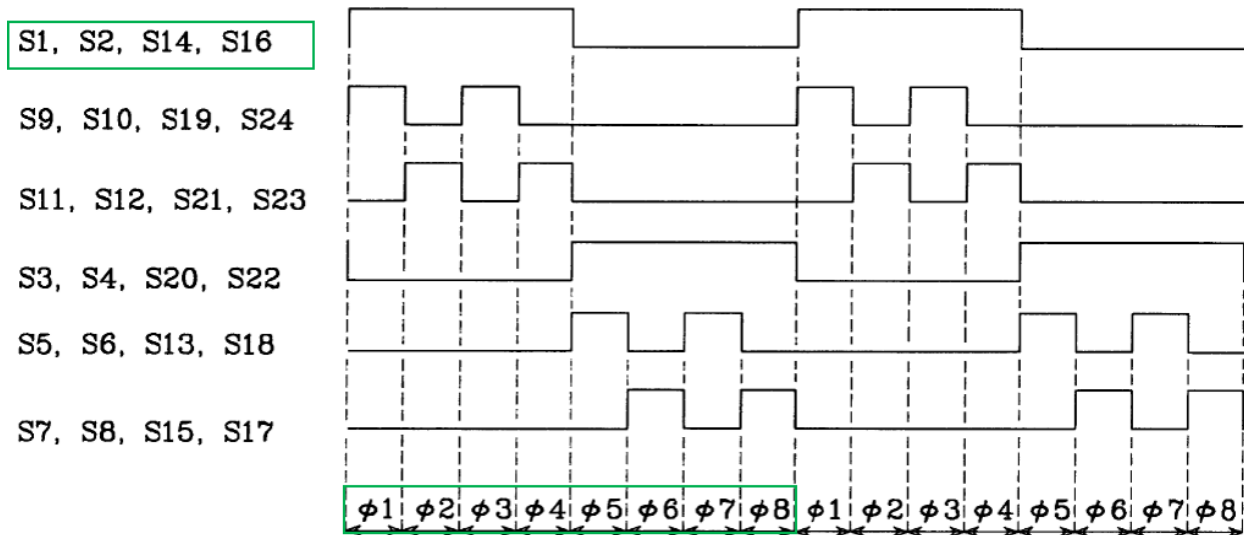
152. The operation frequency of the auto-zeroing, i.e., the “second frequency” is “the number of active pulses of an auto-zeroing switch in a full cycle period divided by the period of the cycle” as described in Section VI.A.

153. The switches S1, S2, S14, and S16 are closed to auto-zero amplifier A1. These switches are annotated in green below:



Ex. 1006 [Tang] Fig. 2a.

154. When switches S16 and S14 are closed, they short the input of amplifier A1, and when switches S1 and S2 are shorted, the output of amplifier A1 is coupled to the nulling amplifier A3 and memory capacitors CM1 and CM2. Ex. 1006 [Tang] 3:54-61. For one of *Tang's* timing arrangements each of these switches are closed once during $\Phi 1$ - $\Phi 4$ (as annotated in green):



Ex. 1006 [Tang] Fig. 4e.

155. Auto-zeroing switches S1, S2, S14, and S16 have one active pulse in a full cycle period (that repeats $\Phi 1$ to $\Phi 8$).

156. So, the second frequency is $1/(\Phi 1 \text{ to } \Phi 8)$.

1. [22c] the ratio of the frequencies being two to one;

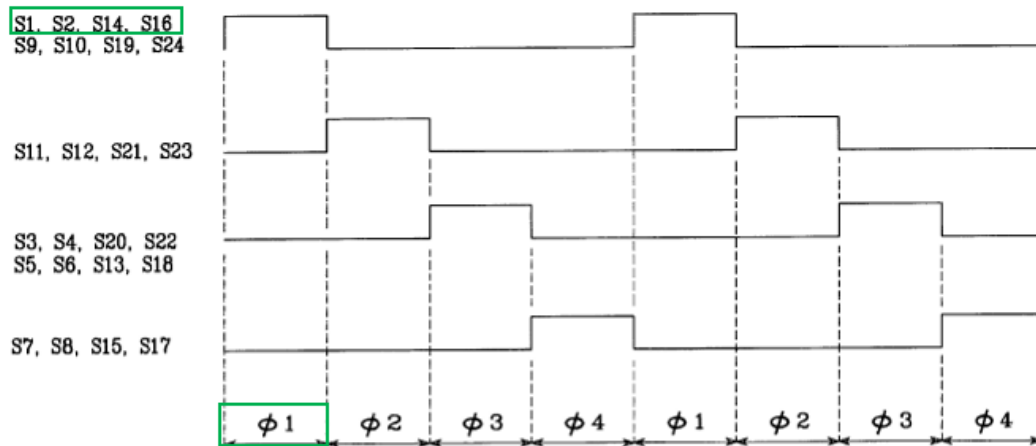
157. This limitation is obvious in light of *Tang*. As described in Section VIII.A.2 and VIII.A.3, the first frequency is $2/(\Phi 1 \text{ to } \Phi 8)$ while the second frequency is $1/(\Phi 1 \text{ to } \Phi 8)$. Further, *Tang* explicitly notes that in Fig. 4e, “multiple chopping cycles are performed during each auto-zero period.” Ex. 1006 [Tang] 4:59-62.

158. Therefore, the ratio between the two frequencies is two to one.

2. [22d] the second frequency having a duty cycle of not more than one-quarter.

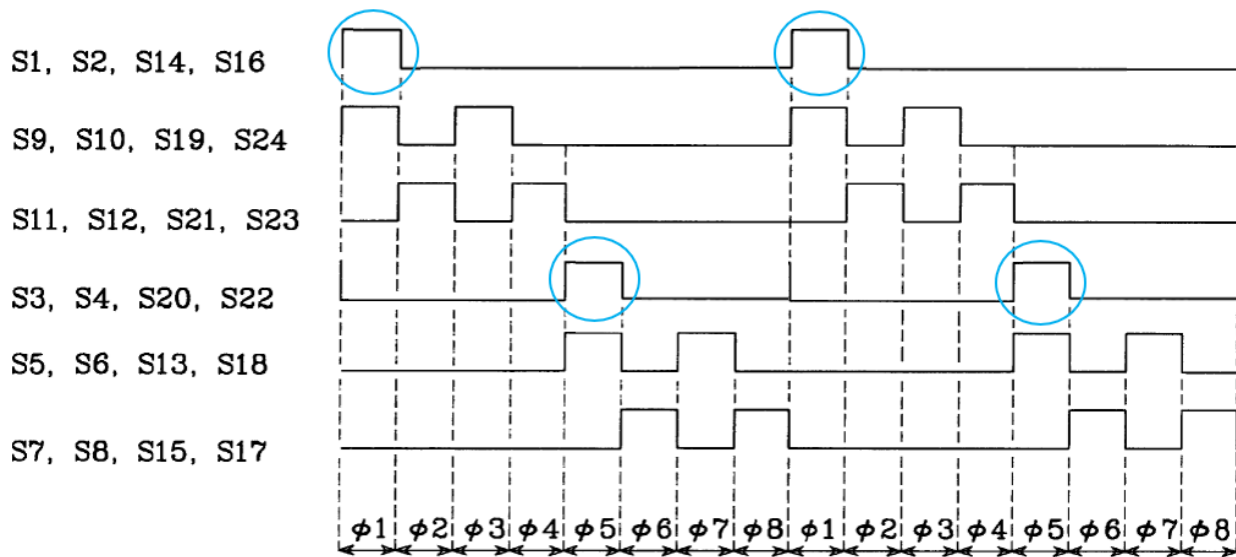
159. This limitation is obvious in light of *Tang*.

160. One of the timing arrangements *Tang* describes includes a timing arrangement where the auto-zeroing function occurs over only during phase $\Phi 1$ (as shown in green):



Ex. 1006 [Tang] Fig. 4d. *Tang* specifically notes that while the auto-zeroing cycle could be performed during $\Phi 1$ and $\Phi 2$, it is also functionally equivalent to have auto-zeroing occur only during $\Phi 1$ or only during $\Phi 2$. Ex. 1006 [Tang] 3:63-67, 4:53-57.

161. It would be obvious to apply this teaching to *Tang*'s other timing arrangements, such as the arrangement provided in Fig. 4e as modified below, where each auto-zeroing cycle occurs for just one phase partition or 1Φ , rather than 4Φ . As noted by the blue dotted lines:



162. Ex. 1006 [Tang] Fig. 4e. Such implementation would be consistent with *Tang's* disclosure and multiple timing arrangements. In this implementation, auto-zeroing would occur on the first amplifier A1 only during $\Phi 1$ over a period of $\Phi 1$ - $\Phi 8$. Similarly, the auto-zeroing cycle on the second amplifier would occur only during $\Phi 5$. While the duty cycle of the auto-zeroing is modified to only occur during $\Phi 1$ or $\Phi 5$, the auto-zeroing and chopping frequencies remain unchanged from Fig. 4e.

163. *Tang* does not specify that each phase is of the same length. However, it would be obvious for a POSITA to apply *Tang's* teachings of pin-pong amplifiers where each step is the same size. It would be obvious to a POSITA to implement *Tang's* timing arrangement so that each Φ is equal to one clock cycle. A clock cycle is the timing unit or period of a master clock in an integrated circuit, and it

would be simplest to implement the switches to be controlled based on equal clock cycles.

164. Therefore, a POSITA would find it obvious to operate the auto-zeroing circuit with a duty cycle of not more than one quarter (here, one of eight phases).

IX. RESERVATION OF RIGHTS

165. I reserve the right to amend or supplement this declaration as this case proceeds and any additional information comes to light.

166. I understand that traditionally no live expert testimony is used at the PTAB, and I presently have no plans to testify, however should I be asked, I reserve my right to use exhibits to summarize or exemplify my opinion (including exhibits I have not yet created) if called to testify.

167. If it would be helpful to the Board, I am willing and able to provide additional background.

168. I further reserve the right to respond to any opinion presented by any of Patent Owner's experts regarding the meaning of any claim term or limitation within the Asserted Claims.

169. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful

false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Dated: *January 9th, 2025*

A handwritten signature in black ink, appearing to read 'Ion Opris', written over a horizontal line.

Ion Opris