

23.4 A 3 μ V-Offset Operational Amplifier with 20nV/ $\sqrt{\text{Hz}}$ Input Noise PSD at DC Employing both Chopping and Autozeroing

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Much progress has been made recently in reducing the offset voltage and noise of instrumentation amplifiers allowing small differential signals to be amplified with greater fidelity [1,2]. Less work, however, has been presented on precision operational amplifiers. Although instrumentation amplifiers offer the convenience of amplifying a differential signal with high impedance inputs, op-amps offer the flexibility of diverse feedback networks, enabling different closed-loop transfer functions such as tailored gains or filters, while allowing use of external transistors for power boosting.

State-of-the-art precision instrumentation amplifiers use chopping to reduce input offset to sub-microvolt levels [1,2,3]. One disadvantage of chopping is that large energy is present at the chopping frequency due to modulation of the amplifier offset up to the chopping frequency (Figure 23.4.1). Manufacturers of precision op-amps, however, are reluctant to use chopping because the large energy arising from chopping restricts the usable bandwidth and requires high-order filtering. To avoid these obstacles, autozeroing is preferred to minimize input offset [3,4].

Unfortunately, the noise power spectral density (PSD) at DC is greater when using autozeroing than when using chopping, since aliasing occurs when the input offset voltage is sampled [3]. For signal bandwidths $>10\text{Hz}$, the peak-to-peak noise from a previous autozeroed op-amp is already larger than the input offset, demonstrating that the noise is more of a limiting factor on fidelity than input offset for many applications [4].

This precision op-amp uses both autozeroing and chopping [6]. Combining these techniques gives low noise PSD at DC, and low energy at the chopping frequency (Figure 23.4.1). The architecture is shown in Figure 23.4.2 and is based on a ping-pong autozeroing op-amp such as that of Reference [5]. INPL and INMI are the non-inverting and inverting op-amp inputs, respectively. Transconductance amplifiers A1 and A2 are the two input gain stages of the ping-pong configuration, transconductance amplifiers A3 and A4 are the nulling amplifiers used to correct the offsets of A1 and A2, and amplifier A0 is the output amplifier. A four-phase cycle ($\phi 1$ to $\phi 4$) controls the switches.

When A1 is autozeroed ($\phi 1$), the inputs of A1 are both connected to INPL. The differential output current from A1 is $\text{VOS1} \cdot \text{gm1}$, where VOS1 is the input offset voltage of A1 and gm1 is the differential transconductance of A1. The outputs of A1 are connected to the inputs and outputs of A3 such that A3 acts as a resistance of $1/\text{gm3}$, where gm3 is the transconductance of A3. A gained up version of $\text{VOS1} \cdot \text{gm1}/\text{gm3}$, is stored between memory capacitors C1 and C2. These capacitors together with A3 continue to null out A1 offset when A1 is later used for signal amplification.

While A1 is being autozeroed, A2 (nulled by A4, C3 and C4) is used for signal amplification. The op-amp departs from prior autozeroing op-amps in that the input gain stage is chopped during signal amplification [7]. During $\phi 1$, no inversion is used at the inputs and outputs of A2. During $\phi 2$ however, both the inputs and outputs of A2 are inverted, thus chopping A2. This has two benefits. The first is that any residual offset VOSAZ2 after the autozeroing process

is reduced since this offset becomes +VOSAZ2 during $\phi 1$ and -VOSAZ2 during $\phi 2$, producing a theoretical average of zero. The second is that the aliased noise PSD is modulated up to the chopping frequency, and the pre-chopped noise PSD at the chopping frequency is modulated down to DC (Figure 23.4.1). This noise transformation is desirable because most precision amplifiers are used to amplify low frequency signals only, and the noise transformation lowers the noise PSD at DC.

During $\phi 3$ and $\phi 4$, the roles of A1 and A2 are reversed: A2 offset is nulled, and the input signal is chopped and amplified using A1.

Another feature of this op-amp is glitch reduction. Prior autozeroing op-amps suffered from glitches at the harmonics of the autozeroing frequency due to switching transients injected into the signal path. Referring to Figure 23.4.2, a difference between the common-mode (CM) output voltages of A1 and A2 (caused by mismatch in the CM feedback circuitry) would cause voltage transients to be injected into the compensation capacitor CC when CC is toggled between A1 and A2.

Figure 23.4.3 illustrates how the op-amp reduces transients injected into CC [8]. During $\phi 2$, A5 adjusts A1 common-mode reference (CMR) input until A1 CM output is equal to VCMR plus the offset voltage of A5 (VOS5). This CMR input is stored onto C5, which continues to set A1 CMR input when A1 is used for signal amplification. Similarly, A5 adjusts A2 CMR input during $\phi 4$ until A2 CM output is equal to VCMR plus VOS5. By ensuring that the CM output voltages of A1 and A2 are equal (and independent of mismatch in the CM feedback circuitry), transients into CC and hence the output are reduced.

The noise spectrum of the op-amp is shown in Figure 23.4.4 and Figure 23.4.5: 20nV/ $\sqrt{\text{Hz}}$ input noise PSD is maintained from DC to 1.5kHz, and rises to 48nV/ $\sqrt{\text{Hz}}$ at 20kHz. The noise at low frequencies is half of that in Reference [4] while consuming similar power. A prior autozeroed op-amp architecture attains this noise level only by quadrupling the input stage transconductance, necessitating increased die area and power consumption. Measurements (not shown in this paper) demonstrate that the noise increase with frequency can be rolled off by a first-order low-pass filter (e.g. using a capacitor across the feedback resistor). Calculations also show that the op-amp exhibits a lower total integrated noise than that in Reference [4] for applications requiring signal bandwidths $<6\text{kHz}$. Other parameters are compared in Figure 23.4.6.

References:

- [1] Q. Huang, C. Menolfi, "A 200nV Offset 6.5nV/ $\sqrt{\text{Hz}}$ Noise PSD 5.6kHz Chopper Instrumentation Amplifier in 1mm Digital CMOS", ISSCC Digest of Technical Papers, pp.362-363, Feb. 2001.
- [2] A. Bakker et al., "A CMOS Nested Chopper Instrumentation Amplifier with 100nV Offset", ISSCC Digest of Technical Papers, pp.156-157, Feb. 2000.
- [3] C.C. Enz, G. C. Temes, "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization". Proceedings of the IEEE, vol. 84, no. 11, pp.1584-1614, Nov 1996.
- [4] Analog Devices Inc., "AD8551 data sheet", 1999.
- [5] I. E. Opris, G. T. A. Kovacs, "A Rail-to-Rail Ping-Pong Op-Amp", IEEE Journal of Solid-State Circuits, vol. 31, no. 9, pp.1320-1324, Sept. 1996.
- [6] Analog Devices Inc., "AD8628 preliminary data sheet", 2001.
- [7] A. T. K. Tang, "Ping-Pong Amplifier Using Both Auto-Zeroing And Chopping", U.S. patent pending.
- [8] A. T. K. Tang, "Auto-Zeroed Ping-Pong Amplifier With Low Transient Switching", U.S. patent pending.

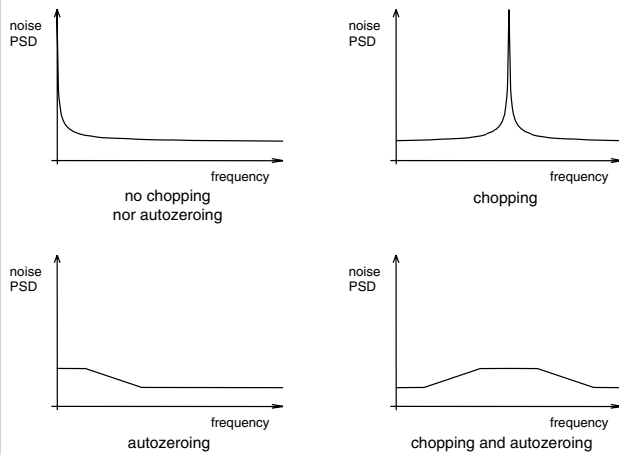


Figure 23.4.1: Noise behavior from different offset reduction schemes.

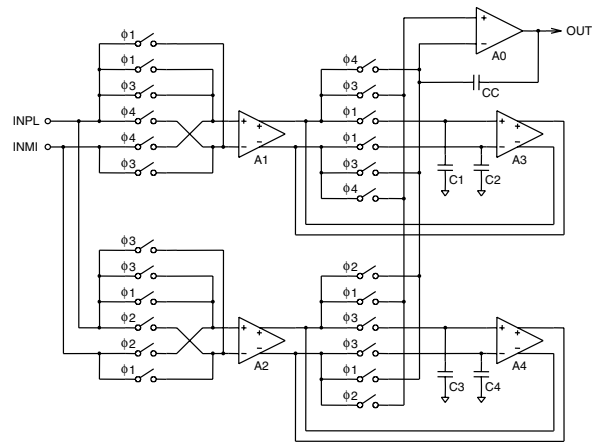


Figure 23.4.2: Simplified schematic of new op-amp showing chopping and autozeroing.

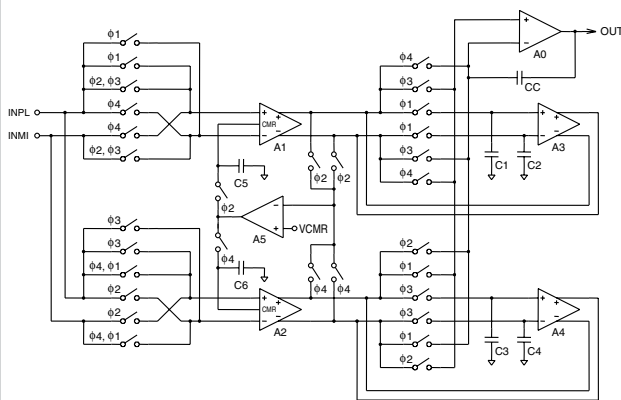


Figure 23.4.3: Simplified schematic of new op-amp showing chopping, autozeroing and glitch reduction.

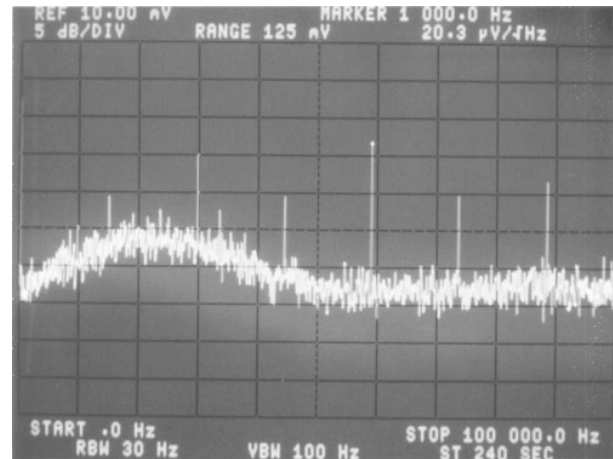


Figure 23.4.4: DC to 100kHz spectrum with 0V input: x10 closed loop gain with x100 post-gain (x1000 total gain).

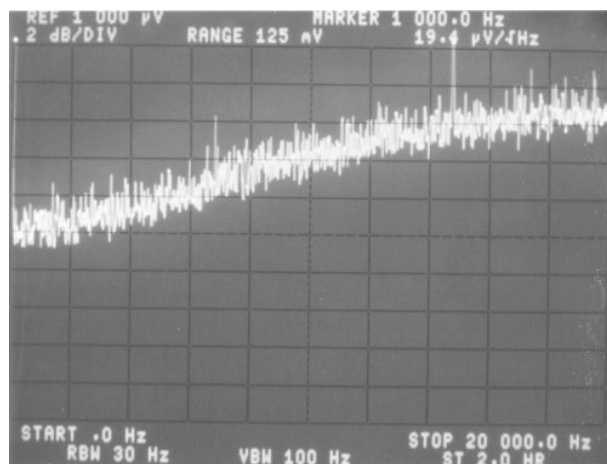


Figure 23.4.5: DC to 20kHz spectrum with 0V input: x10 closed loop gain with x100 post-gain with x100 post-gain (x1000 total gain).

	new op-amp	[4]	[5]
Year of release / publication	2001	1999	1996
Chopping frequency	15kHz	N/A	N/A
Autozeroing frequency	7.5kHz	4kHz	100kHz
Input noise density at DC	20nV/√Hz	48nV/√Hz	225nV/√Hz
Offset voltage	3μV	1μV	100μV
Input bias current	40pA	4pA	
Common-mode input range	0V to 5V	0V to 5V	0V to 5V
Supply current	800μA	800μA	300μA
Unity gain bandwidth	2.5MHz	1.5MHz	5 MHz
Process	0.6μm CMOS	0.6μm CMOS	2μm CMOS
Die area	0.60mm x 1.12mm		0.61mm x 0.42mm

Figure 23.4.6: Comparison of different precision op-amps with 5V supply.