Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization

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Invited Paper

In linear IC's fabricated in a low-voltage CMOS technology, the reduction of the dynamic range due to the dc offset and low-frequency noise of the amplifiers becomes increasingly significant. Also, the achievable amplifier gain is often quite low in such a technology, since cascoding may not be a practical circuit option due to the resulting reduction of the output signal swing. In this paper, some old and some new circuit techniques will be described for the compensation of the amplifier most important nonideal effects including the noise (mainly thermal and $1/f$ noise), the input-referred dc offset voltage, as well as the finite gain resulting in a nonideal virtual ground at the input.

I. INTRODUCTION[1]

In linear active circuits, the active element most often used is the operational amplifier (op-amp), whose main function in the circuit is to create a virtual ground, i.e., a node with a zero (or constant) voltage at its input terminal without sinking any current. Using op-amps with MOS input transistors, the op-amp input current at low frequencies can indeed be made extremely small; however, the input voltage of a practical op-amp is usually significantly large (typically of the order of 1–10 mV), since it is affected by several nonideal effects. These include noise (most importantly, $1/f$ and thermal noise), the input-referred dc offset voltage, as well as the signal voltage needed to generate the desired output voltage of the op-amp. Normally, the thermal noise occupies a wide frequency band, while the $1/f$ noise, offset and input signal are narrowband low-frequency signals.

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[1] This work is dedicated to Prof. Karoly Simonyi on his 80th birthday.

The purpose of the circuit techniques discussed in this paper is to reduce the effects of the narrow-band noise sources at the virtual ground of an op-amp stage. By reducing the low-frequency noise and offset at the op-amp input, hence the dynamic range of the circuit is improved; by reducing the signal voltage at the virtual ground terminal, the effect of the finite low-frequency gain of the op-amp on the signal-processing characteristics of the stage is decreased. Both improvements are especially significant for low-supply voltage circuits, which have limited signal swings and where the op-amp gain may be low since headroom for cascoding may not be available. The proposed techniques are applicable to such important building blocks as voltage amplifiers, ADC and DAC stages, integrators and filters, sample-and-hold (S/H) circuits, analog delay stages, and comparators.

Sections II and III present the two basic techniques that are used to reduce the offset and low-frequency noise of op-amps, namely the autozero (AZ) and chopper stabilization (CHS) techniques. A clear distinction is made between autozeroing, which is a sampling technique, and CHS, which is a modulation technique, mainly with respect to their effect on the amplifier broadband noise. The correlated double sampling (CDS) technique is described in Section II as a particular case of AZ where, as its name indicates, the amplifier noise and offset are sampled twice in each clock period. Then, Section IV treats the most important practical issues at the transistor and circuit level that are faced when implementing the offset and noise reduction techniques discussed previously. Section V presents fundamental building blocks that are used for sampled-data analog signal processing. They are all realized as switched-capacitor (SC) circuits and therefore exploit the CDS technique not only for reducing the offset and the $1/f$ noise, but also to lower the sensitivity of the circuit performance to the finite amplifier gain. Examples of SC S/H stages, voltage amplifiers, integrators, and filters are

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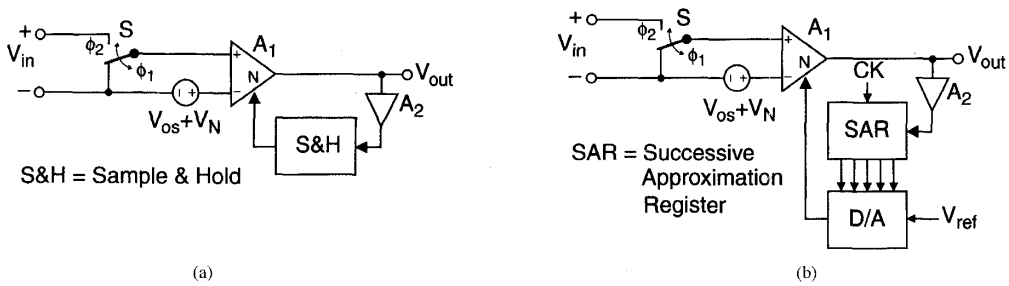
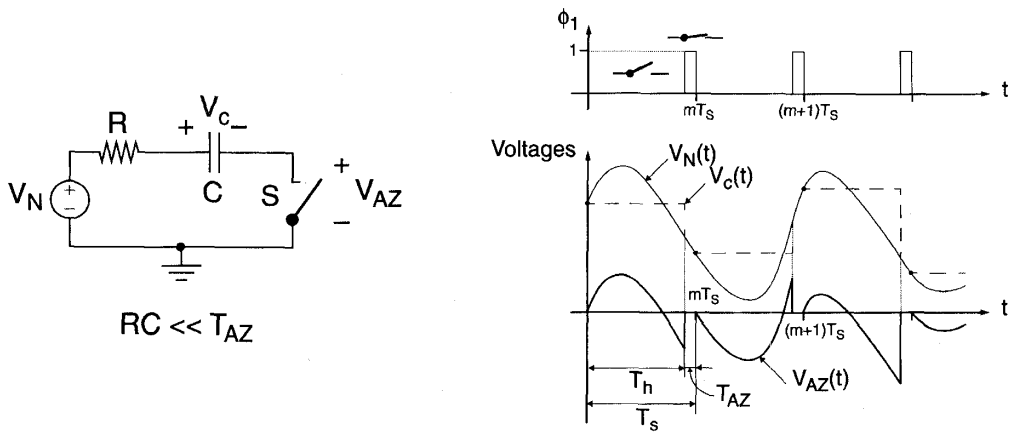


(a) (b)

Fig. 1. Basic autozeroed stages. (a) Analog offset control storage and (b) digital offset control storage.



(a) (b)

Fig. 2. (a) Basic AZ circuit and autozeroed signal: (b) shows voltages in (a).

presented. An example of the use of the CHS technique to realize a low-noise and low-offset micropower amplifier for intrumentation applications is presented in Section VI. Finally, a summary is given in Section VII, where the two techniques discussed in this paper are compared.

II. Autozeroing and Correlated Double Sampling Techniques

In this section, the principle of AZ and CDS techniques will be introduced and their effect on offset and noise analyzed.

A. Basic Principle

The basic idea of AZ is sampling the unwanted quantity (noise and offset) and then subtracting it from the instantaneous value of the contaminated signal either at the input or the output of the op-amp. This cancellation can also be done at some intermediate node between the input and the output of the op-amp, using an additional input port defined as the nulling input and identified with the letter N in the schematics of Fig. 1.

If the noise is constant over time (like a dc offset) it will be cancelled, as needed in a high-precision amplifier or high-resolution comparator. If the unwanted disturbance is low-frequency random noise (for example, $1/f$ noise), it will be high-pass filtered and thus strongly reduced at low frequencies but at the cost of an increased noise floor due to aliasing of the wideband noise inherent to the sampling process. The general principle of the AZ process will first be described considering only the input referred dc offset voltage V_{os} and will then be extended to the input referred random noise voltage V_N.

The AZ process requires at least two phases: a sampling phase (ϕ_1) during which the offset voltage V_{os} and the noise voltage V_N are sampled and stored, and a signal-processing phase (ϕ_2) during which the offset-free stage is available for operation. The two major categories of AZ are shown in Fig. 1. During the sampling phase (shown in Fig. 1), the amplifier is disconnected from the signal path, its inputs are short-circuited and set to an appropriate common-mode voltage. The offset is nulled using an auxiliary nulling input port N by means of an appropriate feedback configuration and/or a dedicated algorithm. The control quantity x_c is next sampled and stored, either in an analog form as a voltage using a S/H stage [Fig. 1(a)] or in a digital form, using for example a register [Fig. 1(b)]. The output V_{out} is forced to a small value in these particular configurations. The input terminals of the amplifier can afterwards be connected back to the signal source for amplification. If

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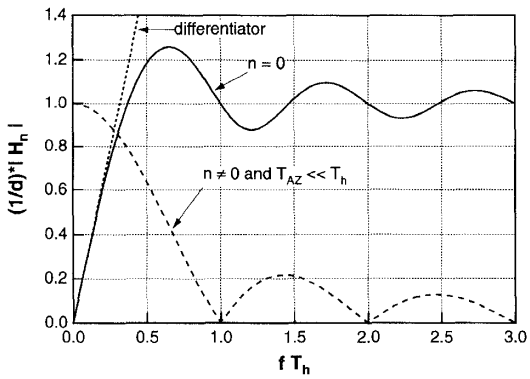

Fig. 3. Autozero baseband and foldover bands transfer functions.

it is used under the same conditions as during sampling, the amplifier will ideally be free from any unwanted offset.

B. The Effect of AZ on the Noise

The autozero principle can be used not only to cancel the amplifier offset but also to reduce its low-frequency noise, for example $1/f$ noise. But unlike the offset voltage, which can be considered constant, the amplifier's noise and particularly its wideband thermal noise component is time-varying and random. The efficiency of the AZ process for the low-frequency noise reduction will thus strongly depend on the correlation between the noise sample and the instantaneous noise value from which this sample is subtracted. The autocorrelation between two samples of $1/f$ noise separated by a time interval τ decreases much slower with increasing τ than it does for white noise, assuming they have the same bandwidth. The AZ process is thus efficient for reducing the $1/f$ noise but not the broadband white noise.

Another way of looking at the effect of AZ is to note that it is equivalent to subtracting from the time-varying noise a recent sample of the same noise. For dc or very low-frequency noise this results in a cancellation. This indicates that AZ effectively high-pass filters the noise.

In addition to this basic high-pass filtering process, since AZ is a sampling technique, the wideband noise is aliased down to the baseband, increasing the resulting in-band power spectral density (PSD) unless the system is already a sampled-data one.

The effects of AZ on the amplifier's noise can be better understood by analyzing the simple circuit shown in Fig. 2, where source V_N may represent the noise at the output of the amplifier in the autozero phase [see, i.e., Fig. 21(a)]. Each time switch S is closed, the output voltage V_{AZ} is reset to zero and the noise source voltage V_N appears across resistor R and capacitor C. Assuming $RC \ll T_{\mathrm{AZ}}$, at the end of the sampling phase (when switch S opens) the noise voltage V_N is sampled onto capacitor C. The output voltage becomes equal to the difference between the instantaneous voltage V_N and the voltage V_c stored on capacitor C. This eliminates the dc component of V_N, but not its time-varying part. It can be shown [8] that if source voltage $V_N(t)$ corresponds to a stationary random noise with a PSD $S_N(f)$, the PSD of the autozero voltage across the switch can be decomposed into two components: one caused by the baseband noise (which is reduced by the AZ process) and the other by the foldover components introduced by aliasing. Thus

$$S_{\mathrm{AZ}}(f) = \underbrace{|H_0(f)|^2 S_N(f)}_{\text{baseband}} + \underbrace{S_{fold}(f)}_{\text{foldover}} \tag{1}$$

where

$$S_{\mathrm{fold}}(f) \equiv \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right). \tag{2}$$

The foldover component results from the replicas of the original spectrum shifted by the integer multiples of the sampling frequency. The baseband transfer function $|H_0(f)|^2$ is given by (see (3) at the bottom of the page) where $d \equiv T_h/T_s$ is the duty cycle of the clock signal [Fig. 2(b)]. The magnitude of $H_0(f)$ normalized to the duty cycle d is plotted as a function of fT_h in Fig. 3, which shows its high-pass characteristic. Note that for $\pi f T_h \ll 1$, $H_0(f)$ acts like a differentiator

$$|H_0(f)| \cong \pi f T_h. \tag{4}$$

It imposes a zero at the origin of frequency axis that cancels out any dc component present in $V_N(t)$. The other transfer functions $|H_n(f)|^2$ for $n \neq 0$ are derived in the Appendix. Their shape depends on the duty cycle d, but they all merge to a common function in the case the AZ time T_{AZ} can be considered much smaller than the hold time ($T_{\mathrm{AZ}} \ll T_h$)

$$|H_n(f)|^2 \cong [d \cdot \mathrm{sinc}\,(\pi f T_h)]^2 \quad \text{for } n \neq 0 \text{ and } T_{\mathrm{AZ}} \ll T_h \tag{5}$$

where $\mathrm{sinc}\,(x) \equiv \sin(x)/x$. $|H_n(f)|$ is plotted in Fig. 3.

The PSD at the output of the AZ circuit clearly depends on the PSD of the source which is autozeroed. The low-frequency input-referred noise PSD of an amplifier generally contains both a white and a $1/f$ noise component. It can be written in the following convenient form:

$$S_N(f) = S_0\left(1 + \frac{f_k}{|f|}\right) \tag{6}$$

$$|H_0(f)|^2 = d^2\left\{\left[1 - \frac{\sin(2\pi f T_h)}{2\pi f T_h}\right]^2 + \left[\frac{1-\cos(2\pi f T_h)}{2\pi f T_h}\right]^2\right\} \tag{3}$$

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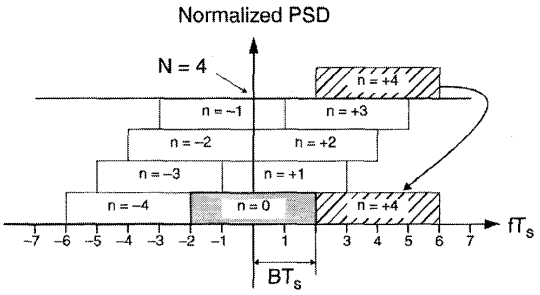

Fig. 4. Aliasing of an ideally low-pass filtered white noise having a bandwidth equal to twice the sampling frequency.

where S_0 represents the white noise PSD and f_k is the corner frequency, defined as the frequency for which the $1/f$ noise PSD becomes equal to the white noise S_0. The corner frequency of amplifiers having MOS input devices can be relatively high (typically ranging from 1 kHz to as high as 100 kHz), which means that in the absence of aliasing the input noise is often dominated by the $1/f$ noise component in the frequency range of interest. The effect of AZ will be examined separately for each of these PSD components, starting with the white noise.

The foldover component defined by (2) can easily be calculated if the amplifier's broadband white noise is considered as an ideally low-pass filtered white noise having a bandwidth equal to B. The aliasing effect introduced by the sampling process in this case is illustrated in Fig. 4 for $BT_s = 2$ (i.e., for a noise bandwidth B = four times the Nyquist frequency). Fig. 4 clearly shows the effect of undersampling the broadband white noise: the original noise power spectrum is shifted by multiples n of the sampling frequency and summed, resulting in a white noise of PSD value approximately equal to NS_0, where N is the integer closest to the *undersampling factor* defined by $2BT_s$. Thus

$$\sum_{n=-\infty}^{+\infty} S_N\left(f - \frac{n}{T_s}\right) \cong 2BT_s S_0. \tag{7}$$

The signal corresponding to (7) has no physical reality since its power is infinite. The power is actually bounded by the $\text{sinc}^2(\pi f T_s)$ function introduced by the hold operation. The foldover component in the Nyquist range is then simply derived from (7) by subtracting the original band ($n = 0$) and multiplying the remainder by the $\text{sinc}^2(\pi f T_s)$ function:

$$S_{\text{fold-white}}(f) = (2BT_s - 1)S_0 \,\text{sinc}^2(\pi f T_s). \tag{8}$$

This result can be extended to the case of a first-order low-pass filtered white noise with a PSD

$$S_{N\text{-white}}(f) = \frac{S_0}{1 + \left(\frac{f}{f_c}\right)^2} \tag{9}$$

where f_c is the 3-dB noise bandwidth, which typically corresponds to the amplifier gain-bandwidth product when the noise is sampled with the op-amp in a unity-gain configuration. Therefore, f_c is generally much larger than the sampling frequency $f_s \equiv 1/T_s$. The detailed analysis given in [8] shows that (8) also holds for the foldover component of a first-order low-pass filtered white noise if B is replaced by the equivalent noise bandwidth defined by

$$\begin{aligned} B &\equiv \frac{1}{S_0}\int_{-\infty}^{+\infty} S_{N\text{-white}}(f)\,df \\ &= \frac{\pi}{2} f_c. \end{aligned} \tag{10}$$

If the undersampling factor $2BT_s = \pi f_c T_s$ is much larger than unity, the foldover component dominates, since the baseband term $|H_0(f)|^2$ is bounded by 1.6. The autozeroed white noise is thus dominated by the aliased broadband noise component and can be approximated by

$$\begin{aligned} S_{\text{AZ}} - \text{white}(f) &\cong S_{\text{fold}} - \text{white}(f) \\ &\cong (pi f_c T_s - 1) S_0 \,\text{sinc}^2(\pi f T_s). \end{aligned} \tag{11}$$

The PSD of a first-order low-pass filtered white noise having a bandwidth five times larger than the sampling frequency[2] ($f_c T_s = 5$) and the different PSD components resulting from the AZ process are plotted in Fig. 5. It clearly shows that the autozeroed noise PSD is dominated by the foldover component in the Nyquist band ($|fT_s| \leq 0.5$).

A similar analysis can be carried out for a first-order low-pass filtered $1/f$ noise having a PSD given by

$$S_{N-1/f}(f) = \frac{S_0 f_k}{|f|\left[1 + \left(\frac{f}{f_c}\right)^2\right]}. \tag{12}$$

As shown in Fig. 6, the input $1/f$ noise is zeroed, removing the original divergence of the $1/f$ noise occurring at the origin of frequency. Although $1/f$ noise has a narrow bandwidth, it still has a foldover component due to the aliasing of all the tails of the $1/f$ noise. This foldover component and the original baseband PSD are plotted in Fig. 6 for $f_c T_s = 5$ and for a corner frequency equal to the sampling frequency ($f_k T_s = 1$).

The foldover component for the $1/f$ noise can be approximated [8] in the Nyquist range by

$$S_{\text{fold-}1/f} \cong 2S_0 f_k T_s[1 + \ln(\tfrac{2}{3} f_c T_s)]\text{sinc}^2(\pi f T_s). \tag{13}$$

Comparing $S_{\text{fold-1/f}}$ to the corresponding term obtained for the white noise (8), it can be seen that it increases proportionally to $f_c T_s$ for the white noise, but only logarithmically for the $1/f$ noise. The effect of aliasing on the $1/f$ noise is thus not as dramatic as on the broadband white noise.

The PSD at the output of the AZ circuit at low frequencies, considering both the white and the $1/f$ component given by (6) and assuming $\pi f_c T_s \gg 1$, can simply be obtained from (11) and (13):

$$S_{\text{AZ}}(f) = |H_0(f)|^2 S_N(f) + S_{\text{fold}} \tag{14}$$

[2]This selection reflects the requirement $f_c T_s \geq 5$ needed for the full settling of an SC stage [10].

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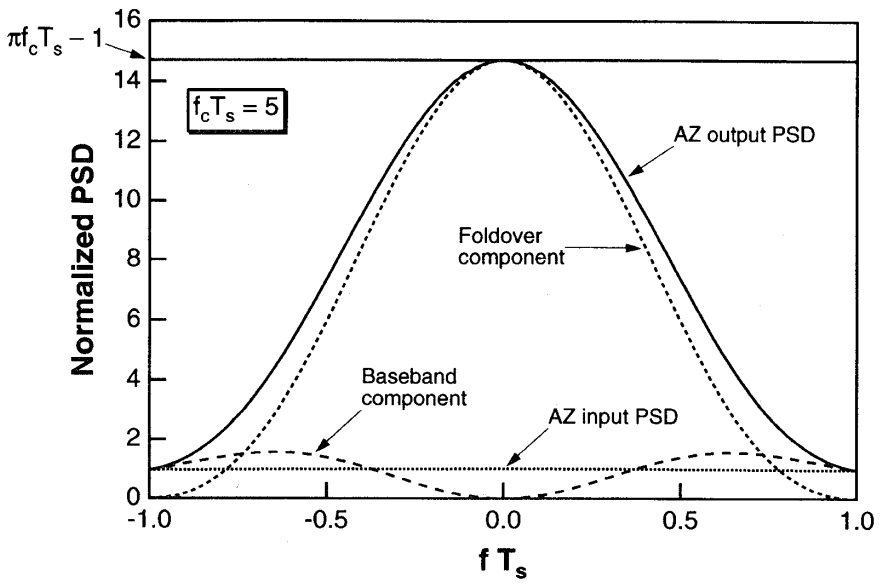

Fig. 5. Effect of the AZ process on a first-order low-pass filtered white noise with a bandwidth five times larger than the sampling frequency.

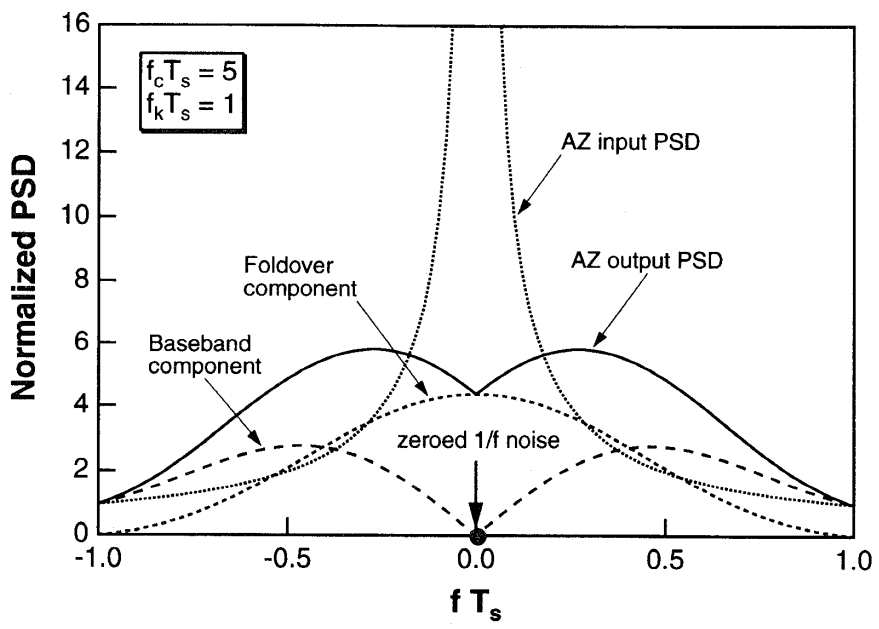

Fig. 6. Effect of the AZ process on a first-order low-pass filtered $1/f$ noise having a bandwidth five times larger than the sampling frequency.

where the total foldover component is given by

$$S_{\text{fold}} = S_0\{(\pi f_c T_s - 1) + 2 f_k T_s[1 + \ln(\tfrac{2}{3} f_c T_s)]\} \cdot \text{sinc}^2(\pi f T_s). \tag{15}$$

The corner frequency for which the $1/f$ noise foldover component [given by (13)] is equal to the foldover component coming from the white noise [as given by (8)] is plotted against the normalized white-noise bandwidth in Fig. 7. The total foldover term given by (15) is thus dominated by the $1/f$ noise contribution for parameter values $(f_k T_s, f_c T_s)$ falling in the region above this curve, while it is dominated by the broadband white noise contribution below the curve. For example, an amplifier autozeroed at 100 kHz and having a gain-bandwith product equal to $7 \times f_s = 700$ kHz should have a corner frequency larger than $4.13 \times f_s = 413$ kHz for the $1/f$ noise foldover to dominate.

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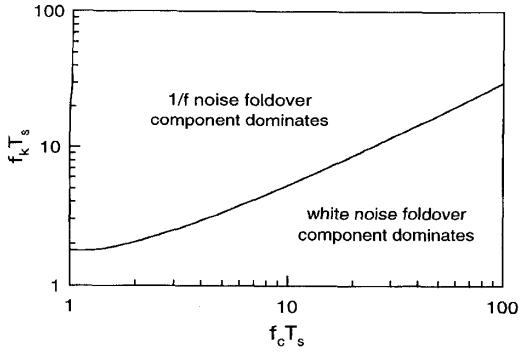

Fig. 7. Comparison between the $1/f$ and white noise contribution to the total foldover component as a function of the white-noise bandwidth.

This demonstrates that in most practical cases the foldover component is dominated by the broadband white noise.

In conclusion, it was shown in this section that the AZ process not only cancels the amplifier's offset, but it also strongly reduces the amplifier $1/f$ noise thanks to the double zero introduced by the AZ baseband power transfer function. This improvement is obtained at the cost of an increased white noise foldover component due to the aliasing of the amplifier's thermal and as well as $1/f$ noise. In most practical cases, this foldover term is dominated by the aliased thermal noise component, which is approximately equal to the amplifier's original broadband thermal noise multiplied by the ratio of the equivalent noise bandwidth to the Nyquist frequency.

C. Residual Offset

Next, the effectiveness of the stages of Fig. 1 in eliminating the effects of V_{os} will be discussed. Since the additional input used in the amplifiers of Fig. 1 for nulling the offset can either be a voltage or a current, it will generally be denoted as a control variable x_c. Changing this input when the amplifier is in the sampling phase, as shown in Fig. 1, allows the zeroing of the output voltage for a particular value of the control variable.

Let the input-referred offset V_{ios} be defined as the output voltage during the offset sampling phase divided by the differential gain of the amplifier in the amplification mode. The relation between this input-referred offset and the control variable is schematically plotted in Fig. 8, and is first assumed to be linear (see the continuous straight line in Fig. 8). Assume that the amplifier has an initial offset as shown in Fig. 8(a). The appropriate feedback configuration or the dedicated algorithm will have to bring this offset very close to zero. When the loop has settled or the algorithm is completed, the control information is stored. During the storage process, there might be some error Δx_c introduced into the control variable, due for example to charge injection by the sampling switch, or to the quantization error of the A/D converter, that leads to a residual offset $V_{\text{ios-lin}}$ or $V_{\text{ios-NL}}$ depending if the compensation characteristic is linear or not. It is important to notice that the characteristics

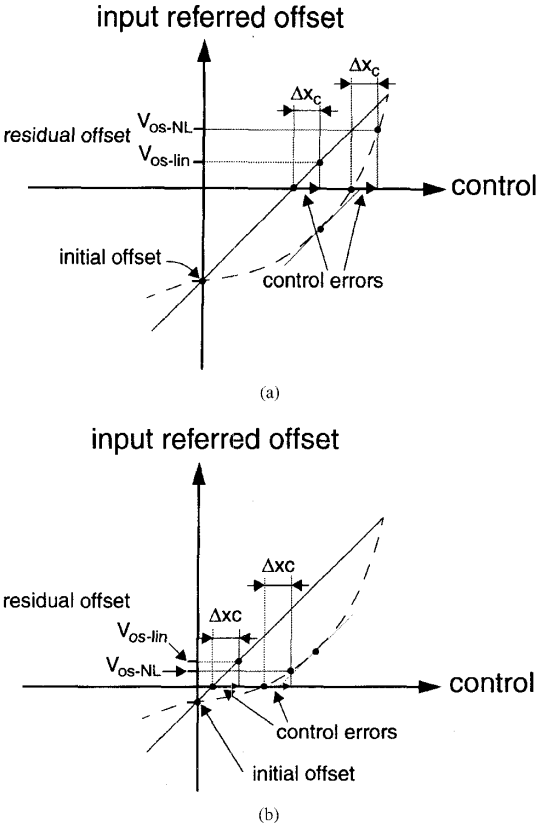

Fig. 8. Input-referred offset versus nulling control variable: (a) large initial offset and (b) small initial offset.

between the control variable and the input-referred offset voltage is not required to be linear. An example of a nonlinear characteristic is illustrated in broken lines in Fig. 8(a) and (b). Let ΔV be defined as the difference between the initial offset and the offset corresponding to the point where the incremental gain on the nonlinear characteristic equals the slope of the linear characteristic. The resulting residual offsets of the linear ($V_{\text{ios-lin}}$) and the nonlinear ($V_{\text{ios-NL}}$) characteristics resulting from equal control errors Δx_c are compared in Fig. 8(a) for an initial offset larger than ΔV. The residual error of the nonlinear characteristic is obviously larger. On the other hand, if the initial offset is already small compared to ΔV [Fig. 8(b)], the residual offset of the nonlinear characteristic becomes smaller. A nonlinear offset-nulling characteristic can thus potentially reduce the sensitivity to control errors and hence reduce the residual offset. But this only happens if the initial offset is already small. The choice between a linear or a nonlinear control characteristic depends on the anticipated initial offset reduction strategy and the test methodology.

D. Correlated Double Sampling

In the AZ principle described in Fig. 1, the amplifier has to be disconnected from the signal path during phase ϕ_1 in

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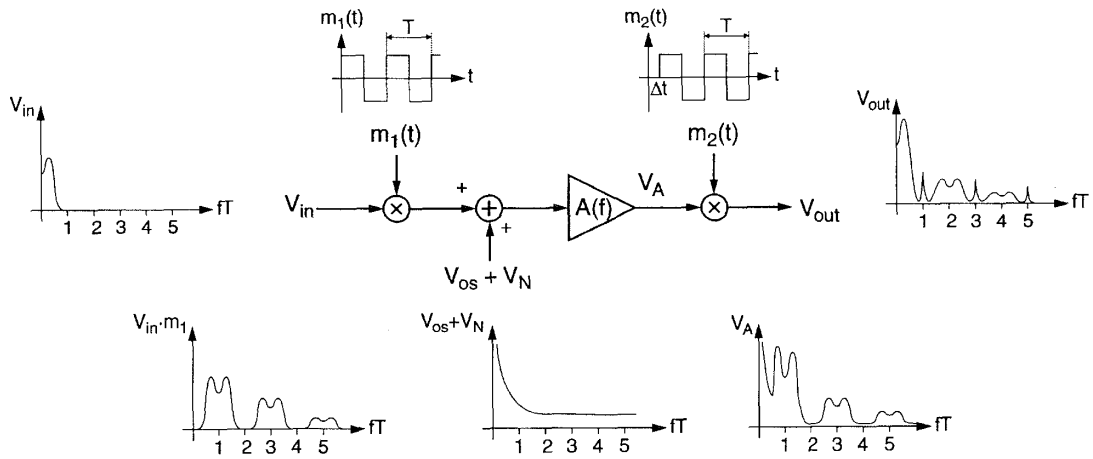

Fig. 9. The chopper amplification principle [19].

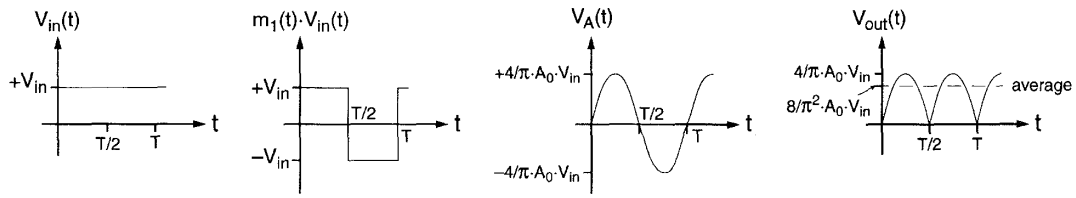

Fig. 10. Waveforms appearing along the chopper amplifier for a dc input and an amplifier bandwidth limited to twice the chopper frequency.

order to S/H its own offset and noise. It is therefore only available for amplification during phase ϕ_2. Although this may be incompatible with continuous-time applications, it is well suited to sampled-data systems such as SC circuits where all the signals are sampled at the end of a phase and held during the complementary time interval. The amplifier can then be autozeroed while the voltages are held and connected back for amplification when needed [20]. After the AZ phase, the output of the amplifier is then sampled again by the next stage (SC integrator or SC amplifier). There are thus two sampling operations: a first one to sample the amplifier noise and offset (AZ) followed by a second sampling of the signal and the instantaneous (or direct) noise of the amplifier in hold mode. Note that the AZ phase may require one additional phase [20].

The CDS technique which has originally been introduced to reduce the noise produced in charged-coupled devices (CCD's) [13], [14] can be described as an AZ operation followed by a S/H. It is widely used in sampled-data systems and particularly in SC circuits (see Section V).

Although the signal at the output of a circuit using CDS is now S/H, the effect of CDS on the amplifier offset and noise is very similar to that of the AZ process. The baseband transfer function $H_0(fT_s)$ still imposes a zero at the origin of frequency that cancels any offset and strongly reduces the $1/f$ noise in the same way the AZ technique does. On the other hand, although the transfer functions for $n \neq 0$ are different from those obtained for the AZ process, the foldover component due to aliasing is comparable since the wideband noise has already been sampled once.

III. The Chopper Stabilization Technique

In this section, an alternative technique for the suppression of the low-frequency noise, called (for historic reasons) chopper stabilization (CHS), will be introduced. Its properties will be analyzed and compared with those of the AZ and CDS schemes.

A. Basic Principle

The CHS technique was introduced about 50 years ago to realize high-precision dc gains with ac-coupled amplifiers. These were originally constructed using vacuum tubes and mechanical relay choppers. When solid-state components became available, they were then made with modular and hybrid techniques. Now they can easily be realized on-chip by taking advantage of integrated switches.

Unlike the AZ process, the CHS technique does not use sampling, but rather applies modulation to transpose the signal to a higher frequency where there is no $1/f$ noise, and then demodulates it back to the baseband after amplification. The chopper amplification principle is illustrated in Fig. 9.

Suppose that the input signal has a spectrum limited to half of the chopper frequency so no signal aliasing occurs, and that the amplifier is ideal, with no noise or offset. This

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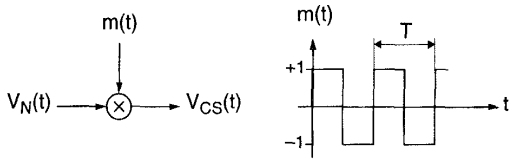

Fig. 11. Chopper modulation.

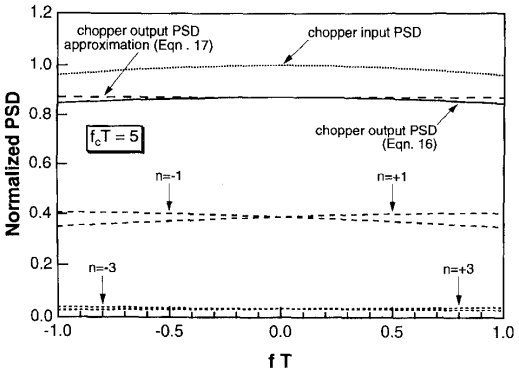

Fig. 12. Chopper output PSD for a first-order low-pass filtered white noise.

input signal is multiplied by the square-wave carrier signal $m_1(t)$ with period $T = 1/f_{\text{chop}}$. After this modulation, the signal is transposed to the odd harmonic frequencies of the modulation signal. It is then amplified and demodulated back to the original band. Assuming that the input of the chopper amplifier is a dc signal V_{in}, the signal at the output of the first chopper modulator is a square wave of period T and amplitude V_{in}. If the amplifier has a gain A_0, an infinite bandwidth and does not introduce any delay, the signal at its output is simply the same square wave with an amplitude $A_0 \cdot V_{in}$ and the signal after demodulation is again a dc signal of value $A_0 \cdot V_{in}$. To illustrate a less ideal solution, assume now that the amplifier has a constant gain A_0 up to twice the chopper frequency and is zero otherwise (ideal low-pass). As shown in Fig. 10, the amplifier output signal $V_A(t)$ is now a sinewave corresponding to the fundamental component of the chopped dc signal with an amplitude $(4/\pi)(A_0 \cdot V_{in})$. The output of the second modulator is then a rectified sinewave containing even-order harmonic frequencies components. The dc value after low-pass filtering is $(8/\pi^2)(A_0 \cdot V_{in})$, corresponding to an equivalent dc gain of $(8/\pi^2) \cdot A_0 \cong 0.8 \cdot A_0$. This example shows that the finite bandwidth of the amplifier introduces some spectral components around the even harmonics of the chopper frequency which have to be low-pass filtered to recover the amplified signal. The gain of the chopper amplifier is also sensitive to the delay introduced by the main amplifier. Assume again that the input is a dc signal V_{in} and that the amplifier has an infinite bandwidth but introduces a constant delay, say of a quarter of a period $T/4$. If the input and output modulators are in phase, the output signal is a chopped cosine wave, without a dc

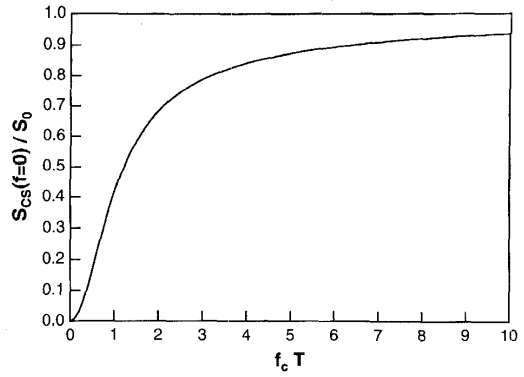

Fig. 13. Chopper modulated white noise at zero frequency as a function of the original white noise bandwidth.

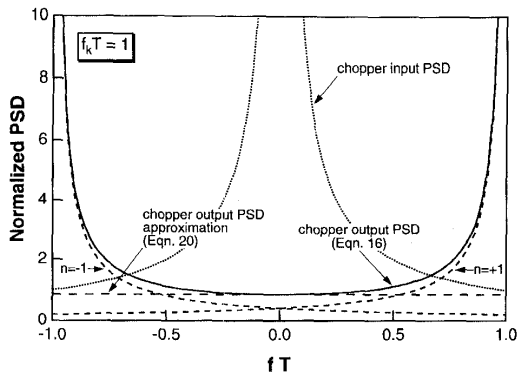

Fig. 14. Chopper output PSD for a $1/f$ noise.

component and containing only odd harmonics. This means that the dc gain of the overall chopper amplifier is zero. If the same constant delay is introduced between the input and the output modulators, the output signal is again a rectified sine wave. This shows that in order to maintain a maximum dc gain, the phase shift between the input and the output modulators has to match precisely the phase shift introduced by the amplifier.

Since the noise and offset are modulated only once, they are transposed to the odd harmonics of the output chopping square wave, leaving the amplifier ideally without any offset and low-frequency noise.

B. The Effect of Chopping on the Amplifier Noise

The effect of the chopper modulation on the amplifier noise can be analyzed from Fig. 11 where $V_N(t)$ is the noise and $m(t)$ the carrier signal.

The bilateral PSD of the chopped output signal $V_{CS}(t)$ is given by

$$S_{CS}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n \text{ odd}}}^{+\infty} \frac{1}{n^2} S_N\left(f - \frac{n}{T}\right). \tag{16}$$

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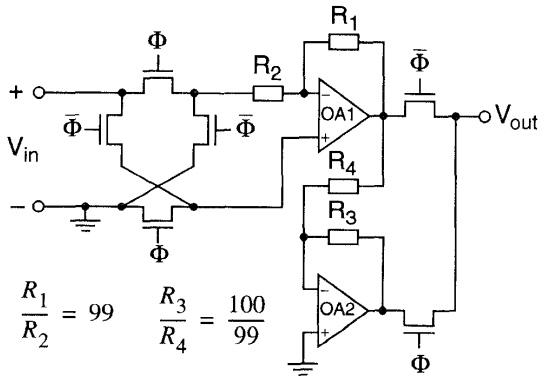
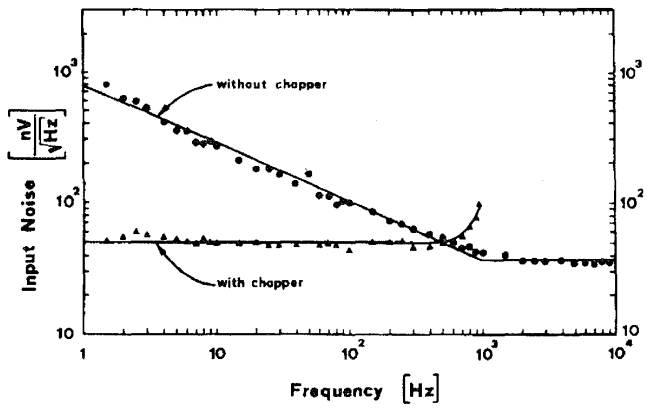


(a)



(b)

Fig. 15. Experimental chopper amplifier. (a) Experimental chopper amplifier schematic. The chopper frequency has been set to the amplifier corner frequency $f_{chop} = f_k = 1$ kHz. (OA1 and OA2 are, respectively, a CA3420 and μ A 741 and the switches are MC14016.) (b) Measured input referred PSD without and with the chopper.

The output PSD, resulting from the summation of the replicas of the original spectrum shifted to the odd harmonics of the chopper frequency, is plotted in Fig. 12 for $n = 1, -1, 3, -3$ and for an amplifier cut-off frequency f_c equal to five times the chopper frequency $1/T$. It can be approximated in the baseband ($|fT| \leq 0.5$) by a white noise PSD

$$S_{CS\text{-white}}(f) \cong S_{CS\text{-white}}(f=0) = S_0 \left[1 - \frac{\tanh\left(\frac{\pi}{2} f_c T\right)}{\frac{\pi}{2} f_c T} \right] \tag{17}$$

which for $f_c T \gg 1$ which can further be approximated by

$$S_{CS\text{-white}}(f) \cong S_0 \quad \text{for} \quad |fT| \leq 0.5 \text{ and } f_c T \gg 1. \tag{18}$$

Unlike the AZ technique, the chopper modulation does not introduce aliasing of the broadband noise, which for AZ causes the PSD in the baseband to increase proportionally with the ratio of the noise bandwidth and the sampling frequency. As shown by (17), the baseband PSD resulting from the chopper modulation is nearly constant (white noise), and it tends to the value of the input white noise S_0 for a large $f_c T$. This is due to the fact that the noise is not sampled nor held, just periodically inverted without changing the general properties of the noise in the time domain. Although the chopper modulator output PSD results from a summation as for the S/H process, in the chopper modulation the replicas are multiplied by $1/n^2$, making their contribution to the baseband decrease very rapidly.

The PSD given in (17) is plotted in Fig. 13 against the white-noise bandwidth normalized to the chopper frequency. It shows that the chopper-modulated PSD is always smaller than the PSD of the original white noise, and tends asymptotically to it for very large cutoff to chopper frequency ratios. It becomes equal to 90% of the original spectrum for $f_c T$ slightly larger than six.

The effect of the chopper modulation on the $1/f$ noise can also be analyzed using (16), assuming a cutoff fre-

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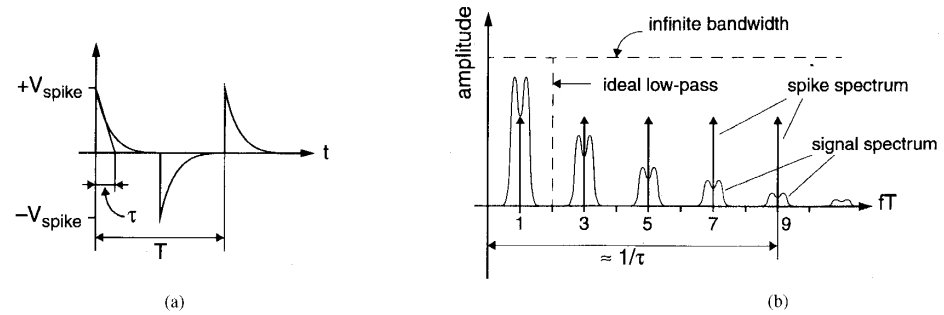

Fig. 16. Spike signal appearing at the input of the amplifier and causing residual offset. (a) Spike signal at the amplifier input and (b) spike signal and chopper-modulated signal spectra with amplifier bandwidth characteristics.

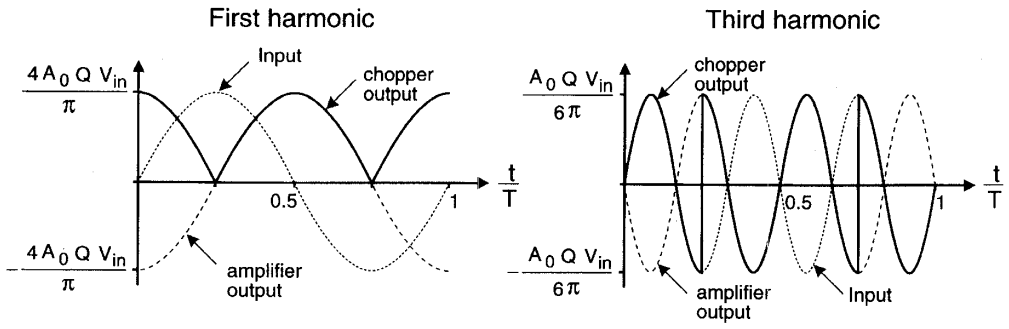

Fig. 17. Effect of the phase shift introduced by a second-order low-pass selective amplifier on the first and third harmonics.

quency much larger than the chopper frequency and an input PSD given by

$$S_{N-1/f}(f) = S_0 \frac{f_k}{|f|} = S_0 \frac{f_k T}{|fT|}. \tag{19}$$

The result of the summation is plotted in Fig. 14, which clearly shows that the $1/f$ noise pole has disappeared from the baseband since it has been transposed to $\pm 1/T$ and to the odd harmonics of the chopper frequency. It also shows that the chopped $1/f$ noise PSD can be approximated in the baseband by a white noise component

$$S_{CS\text{-}1/f}(f) \cong 0.8525 S_0 f_k T. \tag{20}$$

The total residual noise in the baseband for a typical amplifier input referred noise given by (6) can be obtained by adding (18) and (20), resulting in

$$S_{CS}(f) \cong S_0(1 + 0.8525 f_k T) \quad \text{for } |fT| \leq 0.5 \text{ and } f_c T \gg 1. \tag{21}$$

According to (21), a good compromise is obtained by choosing the chopper frequency equal to the amplifier corner frequency. The resulting white noise PSD increase is then less than 6 dB. Equation (21) has been verified experimentally on a breadboard circuit. The schematic is presented in Fig. 15(a), and the measured input referred noise PSD with and without the chopper is shown in Fig. 15(b). The chopper frequency was set equal to the amplifier corner frequency at $1/T = f_k = 1$ kHz. The white noise component of the amplifier without the chopper was estimated to be 37 nV/$\sqrt{\text{Hz}}$, and the theoretical white noise of the amplifier with the chopper active as calculated from (21) was 50.4 nV/$\sqrt{\text{Hz}}$ which is very close to the measured result shown in Fig. 15(b).

C. Residual Offset

Residual offset is mainly due to the nonidealities of the chopper modulators and more specifically of the input modulator. If the modulators are realized with simple MOS switches, these nonidealities will include clock feedthrough and charge injection (see Section IV-A for a discussion of these and other nonideal effects). More generally, any spikes caused by the modulator nonidealities and appearing at the amplifier input will be amplified and demodulated by the output modulator, giving rise to a residual dc component. Since only the odd harmonics of the chopper frequency will contribute to the residual offset, the positive and negative spikes will have an odd symmetry (Fig. 16).

Since the time constant τ of these parasitic spikes is generally much smaller than the half chopper period $T/2$, most of the spike energy appears at frequencies higher than the chopper frequency. The spectra of the signal resulting from such spikes and of a chopper-modulated signal at the amplifier input are shown in Fig. 16(b). Since the spectral envelope is inversely proportional to frequency, the output

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signal after amplification and demodulation is essentially reconstructed by the fundamental component. Using an amplifier with a bandwidth much larger than the chopper frequency results in a maximum gain approximately equal to the dc gain of the amplifier A_0, but also leads to a maximum output offset voltage, since almost all the spectral component of the spike signal will contribute. The input referred offset can be calculated assuming that $\tau \ll T/2$ [8], [12]:

$$V_{os} \cong \frac{2\tau}{T} V_{\text{spike}} \tag{22}$$

where V_{spike} is the amplitude of the spikes at the chopper amplifier input as shown in Fig. 16(a). Keeping the same gain A_0 in the passband, but limiting the bandwidth to twice the chopper frequency slightly lowers the overall dc gain to $(8/\pi_2)A_0 = 0.81A_0$, but greatly reduces the offset voltage referred to the input. The new value is

$$V_{os} \cong \left(\frac{2\tau}{T}\right)^2 V_{\text{spike}} \tag{23}$$

which is much smaller than that given by (22), since τ has been assumed to be much smaller than $T/2$. Therefore, the offset can be reduced drastically, without losing too much signal gain, by limiting the amplifier bandwidth to twice the chopper frequency. It can be shown that (23) also holds for a second-order low-pass or band-pass selective amplifier with its resonance frequency locked to the chopper frequency. This is essentially due to the phase characteristic of the selective amplifier. As illustrated in Fig. 17, for a constant input signal V_{in} and a low-pass selective amplifier, the fundamental component is delayed by a quarter of a period while all the harmonics are delayed by half a period, making their mean values equal to zero after demodulation. Since the offset is not further reduced by using higher-order selective filtering characteristics, the second-order selective amplifier is the best trade-off between circuit complexity and residual offset. Note that the band-pass selective amplifier is the simplest since it does not require any delay between the input and output chopper signals.

IV. Practical Implementation Issues

A. Nonideal Effects in Switches

The S/H circuit as well as the chopper modulator are most often realized using MOS switches. The MOS switch nonidealities include a nonzero and nonlinear on-resistance. However, the most important factors affecting residual offset are the following:

- clock feedthrough;
- channel charge injection;
- sampled noise;
- leakage current.

Clock feedthrough and channel-charge injection will be considered first.

Each time a switch is turned off, the charges in its conducting channel are released and removed through the

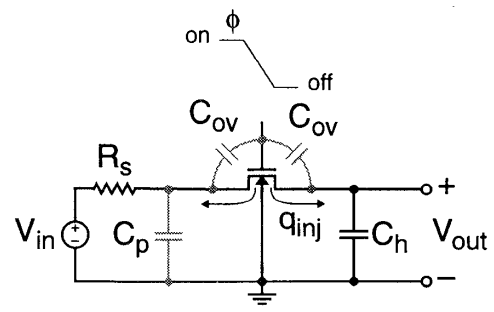

Fig. 18. Basic S/H circuit.

MOS source and drain terminals (the fraction of charges that flows to the substrate can generally be neglected). The partitioning of these charges between the source and drain depends mainly on the ratio of the total capacitance C_h at the switch drain (the hold capacitor) and at the source (C_p, corresponding to the total parasitic capacitance) and on the so called "switching parameter" [2] determined mainly by the transistor's "on" resistance R_{on} and the slope of the clock signal applied to the gate. The channel charge is split equally between source and drain only if either the capacitances C_p and C_h are equal (independent of the switching time), or if the switching transition time is much less than the $R_{on}C$ time constant (independent of C_p/C_h). In general, for slowly falling clock signals, the channel charge is divided unequally between source and drain, going mostly to the terminal showing the lower impedance. In the case where the source or drain capacitance is much larger than the other, most of the charge flows to the larger capacitance. The charge q_{inj} injected into the hold capacitor is thus difficult to predict accurately. There are, however, circuit techniques which can reduce the effect of charge injection. The simplest one uses complementary switches in such a way that the charges released by one switch are absorbed by the complementary device building its channel. This technique is rather inefficient, since the matching between the channel charges of the n-MOS and the p-MOS devices is poor and signal dependent. This charge mismatch is further degraded by phase jitter between the two complementary clocks. Other more efficient strategies include:

1) making capacitance C_p much larger than C_h (by adding an extra capacitor) and choosing a switching parameter much smaller than one (by choosing a slow clock transition) in order to attract most of the channel charge to C_p, reducing q_{inj} almost to zero [Fig. 19(a)]. This technique of course sets a limit on the maximum clock frequency. Furthermore, the charge flow due to the overlap capacitance C_{ov} is still present;
2) making C_p equal to C_h to force the channel charge to split equally between source and drain, and then compensating the injected charge by adding half-size dummy switches [Fig. 19(b)];

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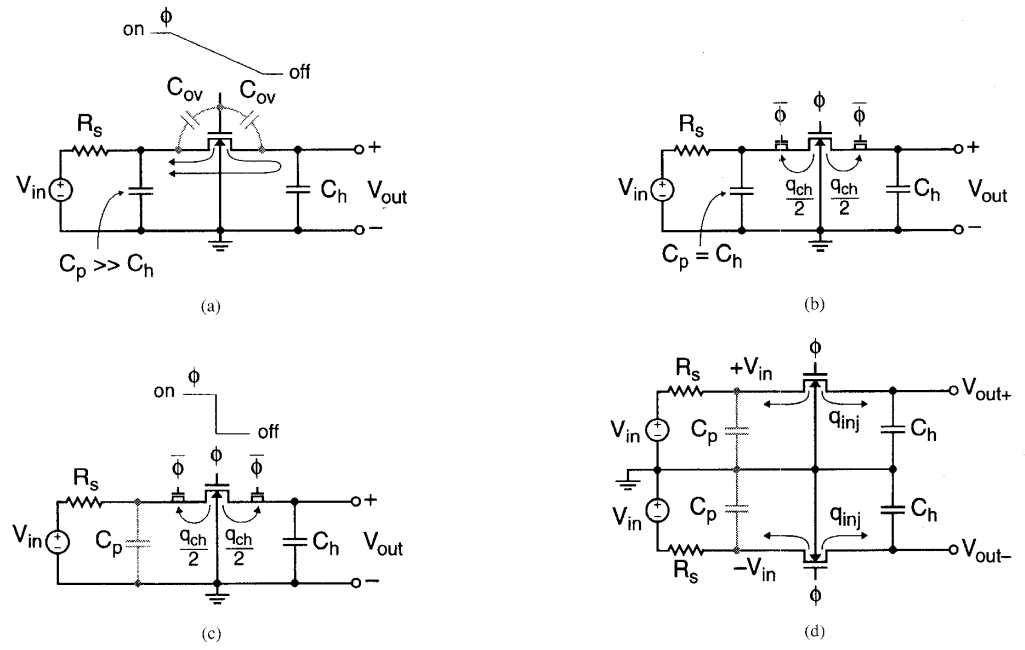

Fig. 19. First-order charge injection cancellation techniques: (a) large shunt capacitor and slow clock transition time, (b) symmetrical capacitances ($C_p = C_h$) with half-sized dummy switches, (c) short clock transition time with half-sized dummy switches, and (d) fully differential structure.

3) using a very short transition time to force the channel charge to split equally between source and drain and then compensating the injected charge by half-sized dummy switches [Fig. 19(c)];
4) using a fully differential structure. If the injected charges to the differential capacitors are matched, the resulting voltage appears as a common-mode voltage and is therefore rejected [Fig. 19(d)]. This usually requires the generation of delayed-cutoff clock phases.

It should be noted that none of the previous described techniques offers a perfect charge-injection cancellation. Furthermore, the efficiency of the half-sized dummy transistor technique depends on a proper layout in order to insure a good matching and a first-order insensitivity to doping gradient. The technique which usually offers the best results is a combination of a fully differential structure and the half-sized dummy transistor technique described in 3) and 4).

It is also important to notice that the simulation of the charge injection effect at the transistor level using a circuit simulator such as SPICE often does not yield accurate results. This is mainly due to the problem of inaccurate charge conservation inherent to such simulators, combined with an incorrect modeling of the MOS transistor's intrinsic charges and of the partitioning of the channel charge between source and drain [37]–[43]. A clear discussion of charge conservation in MOSFET models and SPICE is given in [43].

Each time the switch of Fig. 18 is opened, an additional error charge due to the thermal noise of the switch channel will be sampled on the hold capacitor C_h. The variance of this noise charge is equal to kTC_h [1], [2], corresponding to a sampled noise voltage variance equal to kT/C_h.

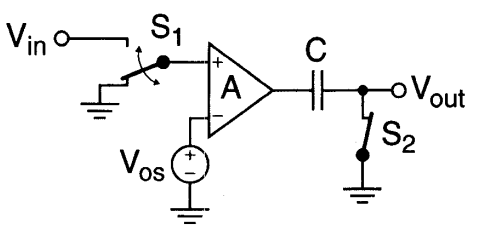

Fig. 20. Open-loop offset cancellation technique.

For very long hold time and/or for high-temperature operation [35], the leakage current I_{leak} associated with the drain-to-bulk junctions also has to be taken into account, since it will discharge the hold capacitor and thus introduce an additional error into the sampled voltage.

The total error ΔV in the sampled voltage across the hold capacitor due to clock feedthrough, charge injection, sampled noise and leakage current is given by

$$\Delta V = \alpha \frac{C_{ov}}{C_{ov} + C_h} V_{\text{swing}} + \frac{q_{inj}}{C_h} + \sqrt{\frac{kT}{C_h}} + \frac{I_{\text{leak}} T_h}{C_h} \tag{24}$$

where V_{swing} is the swing of the clock signal and I_{leak} the leakage current of the drain-to-bulk diodes at the operating temperature. The attenuation factor $\alpha < 1$ accounts for the part of the total charge $C_{ov} V_{\text{swing}}$ coming from the overlap capacitor and flowing to ground instead of the hold

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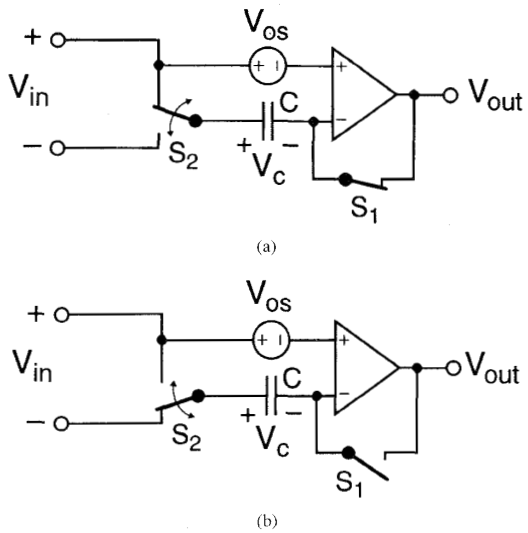

Fig. 21. Closed-loop-amplifier offset cancellation principle: (a) offset sampling phase (AZ) and (b) amplification phase.

capacitor. It is important to notice that all contributions appearing in (24) decrease if a larger hold capacitor is used. Since in most practical cases the second term of (24) dominates, the voltage change ΔV will be replaced by q_{inj}/C_h in the following discussions.

B. The Open-Loop Offset Cancellation Principle

The simplest way to implement offset cancellation is to sample the offset at the output of the amplifier as shown in Fig. 20. This technique is sometimes called output offset storage (OOS) [2], [6], [33]. During the AZ phase, the input switch S_1 and the output switch S_2 are both connected to ground. Switch S_2 is then opened and the offset voltage V_{os} multiplied by the amplifier gain A remains stored on capacitor C. This stored output voltage is altered by an error voltage q_{inj}/C caused by the charge injection occurring at the opening of switch S_2. After the AZ phase, the input terminal of the amplifier is connected back to the signal by switch S_1. The input-referred residual offset is thus limited by the charge injection q_{inj} (or charge injection mismatch Δq_{inj} in the case of a differential implementation)

$$V_{os\text{-}res} = \frac{1}{A}\frac{q_{inj}}{C}. \tag{25}$$

This technique is obviously effective only if the amplifier does not saturate during the offset-sampling phase. This requires that the output-referred offset remain smaller than the minimum saturation voltage. This is possible only if the amplifier gain is relatively small (typically, less than ten), or if C and S_2 follow the first stage of the amplifier.

C. The Closed-Loop Offset Cancellation Principle

The open-loop offset cancellation principle is not well suited to high-gain amplifiers. It is usually preferable there

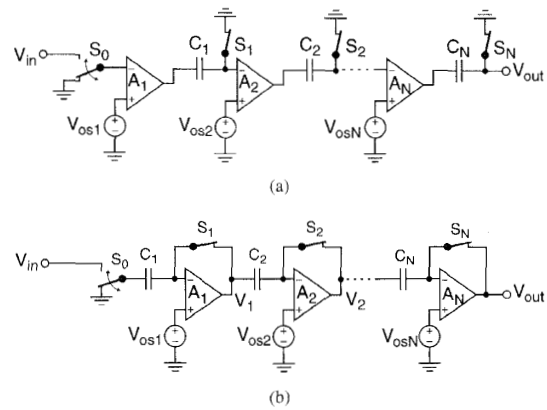

Fig. 22. Multistage offset cancellation principles.

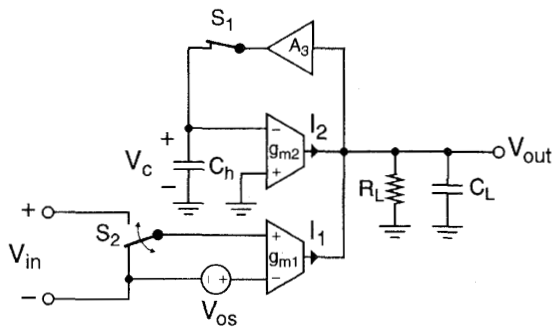

Fig. 23. Offset compensation using an additional offset nulling input.

to sense the amplifier's offset in a closed-loop configuration as shown in Fig. 21.

During the sampling phase, the amplifier is disconnected from the signal path and connected in a unity-gain configuration as shown in Fig. 21(a). Assuming that the open-loop gain A of the amplifier is much larger than one, the voltage V_c obtained across the storage capacitor C after the amplifier has settled is almost equal to its offset voltage V_{os}

$$V_c = \frac{A}{1+A}V_{os} \cong V_{os}. \tag{26}$$

This voltage (plus an additional error q_{inj}/C caused by the charge injection occurring when switch S_1 opens) is stored across capacitor C. The charge will remain trapped on capacitor C since the input current of the amplifier is zero for a MOS input stage, and hence capacitor C behaves like a floating voltage source equal to V_{os} plus the charge-injection error. After this sampling phase, the offset-compensated stage is available for amplification and is connected again to the signal path. The residual offset can then be found

$$\begin{aligned} V_{os\text{-}res} &= V_{os} - V_c \\ &\cong \frac{V_{os}}{A} + \frac{q_{inj}}{C}. \end{aligned} \tag{27}$$

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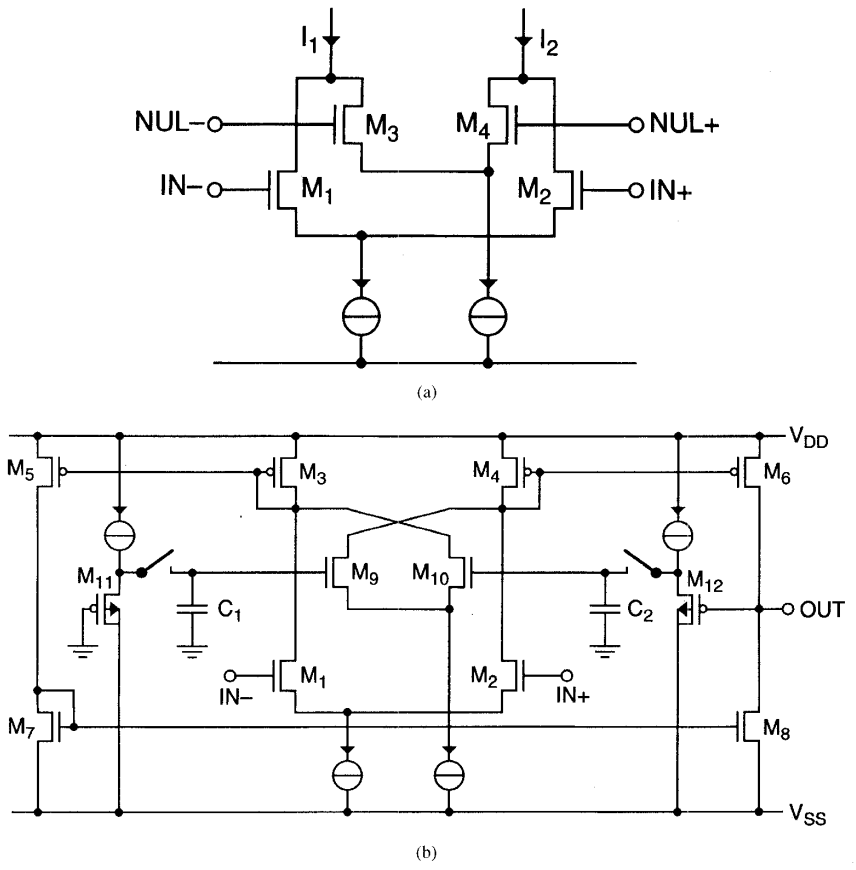

Fig. 24. Realization of the nulling input port using an additional differential pair connected in parallel with the main pair: (a) principle and (b) complete AZ scheme.

It is thus nearly equal to the original offset divided by the amplifier dc gain, and is ultimately limited by the charge-injection term q_{inj}/C. The latter could be reduced to a mismatch error of charge injections if a fully differential configuration is used.

The amplifier is in general connected in a closed-loop configuration for amplification, and in an open-loop configuration when it is used as a comparator.

In the scheme described above, the amplifier is not available to the external circuitry during the offset sampling phase. This is not a major drawback for most applications. In case continuous-time amplification is required, the offset-free amplifier can be duplicated and used in a time-shared ("ping-pong") operation [25], [26], or the continuous-time feedforward technique discussed below in Section IV-F may be used [22], [35], [36].

D. Multistage Offset Storage

If high gain and speed is required, several single-stage amplifiers can be cascaded as shown in Fig. 22 [33], [50]. The circuit of Fig. 22(a) operates as follows. In the offset sampling phase (shown in Fig. 22), the negative inputs of all the amplifiers are connected to ground. Switch S_1 is then opened first, causing some charge to be injected into capacitor C_1, which results in an error voltage appearing at the negative input of the second amplifier. This error voltage can be viewed as a change in the input-referred offset voltage of the second amplifier and will thus be cancelled along with V_{os2}. Subsequently, switches S_2, S_3, $\cdots$, S_N are opened successively, so that the only offset voltage affecting the output is due to the charge injection of switch S_N into capacitor C_N. Since the total gain is equal to the product of the individual gains, the equivalent input-referred offset is

$$V_{os\text{-}res} = \frac{1}{A_1 A_2 \cdots A_N} \cdot \frac{q_{inj-N}}{C_N} \tag{28}$$

which is obviously much lower than that obtained for a single-stage low-gain amplifier.

The circuit of Fig. 22(b) operates in a similar way. When switch S_1 opens, charge is injected onto capacitor C_1 resulting in an output voltage V_1 for the first amplifier equal to $V_{os1} + A_1 q_{inj1}/C_1$ for $A_1 \gg 1$. When switch S_2 opens, the sum of V_1, the offset voltage of the second amplifier V_{os2} and the charge injection voltage q_{inj2}/C_2 of switch S_2 is stored on capacitor C_2. The output voltage

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of the second amplifier when both switches S_1 and S_2 are opened sequentially is thus independent of the voltage V_1 and is simply equal to for $V_{os2} + A_2 q_{inj2}/C_2$ for $A_2 \gg 1$. This means that neither the offset nor the charge-injection errors propagate along the amplifier chain. The output offset is therefore affected only by the last stage, and equals $V_{osN} + A_N q_{injN}/C_N$. Hence, the equivalent input-referred offset is given by

$$V_{os\text{-}res} \cong \frac{V_{osN} + A_N \cdot \dfrac{q_{injN}}{C_N}}{A_1 A_2 \cdots A_N} \tag{29}$$

which is again much lower than the offset obtained for a single-stage low-gain amplifier.

High-gain and high-precision amplifiers or comparators can thus be realized simply by cascading low-gain stages and performing an input or output offset cancellation. If the switches are opened sequentially, the output offset is only determined by the last stage. The equivalent input-referred offset can thus be made extremely small. It should be noticed that this is true only if the delay between the edges of the clock pulses controlling switches S_1 to S_N is long enough to allow complete offset storage on the capacitors [6]. Note also that using a cascade of low-gain stages in a feedback amplifier may lead to stability problems.

E. Closed-Loop Offset Compensation Using an Auxiliary Input Port

The charge injection term appearing in (27) can be drastically reduced by storing the offset voltage at some intermediate node instead of at the amplifier input. The basic principle is that the gain A_1 from the signal input to the output is now higher than the gain A_2 from the nulling input to the output. The voltage change at the nulling input due to charge injection is therefore divided by the ratio A_1/A_2 which can be set much larger than one. The compensation is often realized using transconductance stages as shown in Fig. 23. Amplifier A_3 has been added to avoid loading the main amplifier with the hold capacitor C_h and therefore slowing down the AZ process. This allows the reduction of the effects of charge injected by switch S_1 and of the kT/C_h sampled noise by using a large hold capacitor C_h. It can also increase the compensation loop gain and therefore reduce the residual offset, as will be shown hereafter. In the case a compensation loop gain $g_{m2}R_L$ is sufficient, amplifier A_3 can be a simple voltage follower.

Assume that the input terminals of the main amplifier are short-circuited and that the compensation loop is still inactive (switch S_1 is open). The output voltage is zeroed if the current $I_2 = -g_{m2}V_c$ is equal to the current $-I_1 = g_{m1}V_{os}$, i.e., if the control voltage V_c is equal to $-(g_{m1}/g_{m2})V_{os}$. The ratio g_{m1}/g_{m2} should be chosen such that the control voltage V_c is much larger than the offset at the input of g_{m2} introduced by the nonidealities of the compensation loop containing transconductor g_{m2} and amplifier A_3. On the other hand, the maximum value $V_{c\text{-max}}$ of the control voltage before transconductor g_{m2} saturates should be

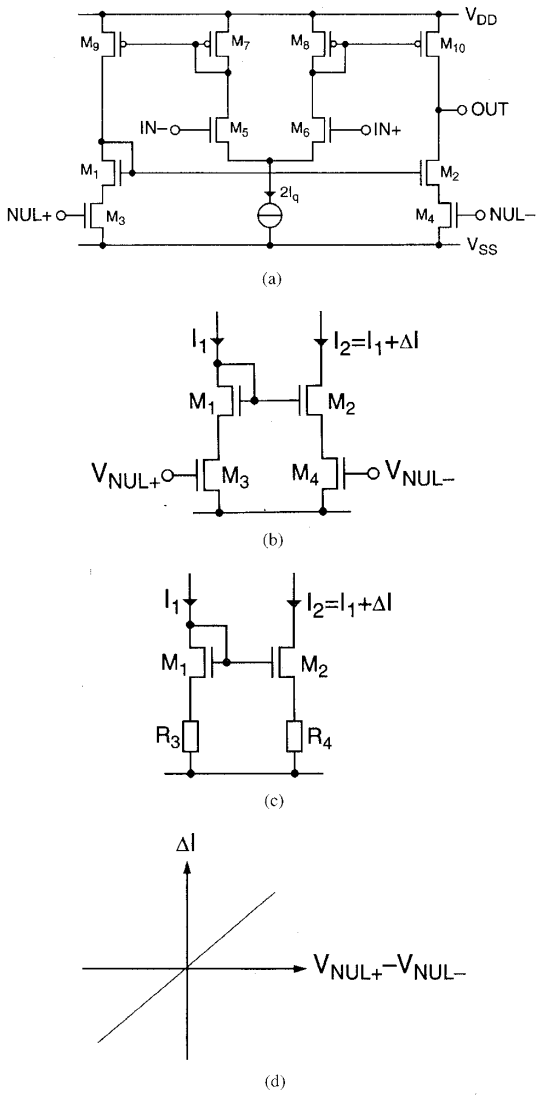

Fig. 25. Realization of the nulling input port using a degenerated current mirror: (a) principle, (b) adjustable current mirror, (c) equivalent schematic of (b), and (d) nulling current transfer characteristic.

chosen such that the maximum input offset voltage $V_{os\text{-max}}$ can still be compensated. This sets the maximum value for the ratio g_{m1}/g_{m2} equal to $|V_{c\text{-max}}/V_{os\text{-max}}|$.

The control voltage V_c is developed during the AZ phase by sensing the output voltage in a closed-loop configuration (with switch S_1 closed). Defining $A_1 \equiv g_{m1}R_L$, the resulting output voltage is then equal to the initial offset $-A_1 V_{os}$ at the output divided by the compensation loop gain (which is assumed to be much larger than one). The corresponding input-referred residual offset is given by

$$V_{os\text{-}res} \cong -\frac{V_{os}}{A_2 A_3} \tag{30}$$

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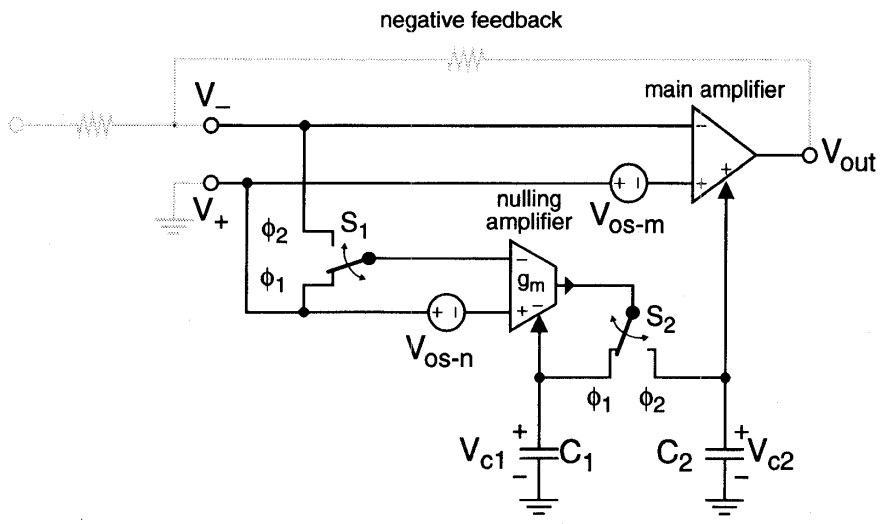

Fig. 26. Continuous-time AZ amplifier using feedforward technique.

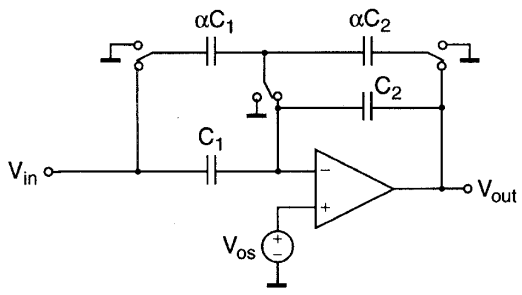

Fig. 27. Uncompensated SC voltage amplifier.

where $A_2 \equiv g_{m2}R_L$. The residual input-referred offset can thus be made small by choosing the loop gain A_2A_3 sufficiently large. Equation (30) ignores the charge injection occurring at the end of the AZ phase when switch S_1 opens. The input-referred residual offset voltage including charge injection of switch S_1 is given by

$$V_{os\text{-}res} \cong -\frac{V_{os}}{A_2A_3} - \frac{A_2}{A_1}\frac{q_{inj}}{C_h} = -\frac{V_{os}}{A_2A_3} - \frac{g_{m2}}{g_{m1}}\frac{q_{inj}}{C_h}. \tag{31}$$

As already mentioned, the first term of (31) can be made small by choosing a sufficiently large loop gain A_2A_3, whereas the effect of charge injection is essentially determined by the ratio of the transconductances g_{m2}/g_{m1}. Assuming that the first term of (31) can be made negligible, the minimum value of ratio g_{m1}/g_{m2} should then be chosen such that the current at the output of transconductor g_{m2} due to charge injection remains smaller than the output current of transconductor g_{m1} produced by the maximum tolerated residual offset voltage:

$$g_{m2}\frac{q_{inj}}{C_h} < g_{m1}V_{os\text{-}res\text{-}\max}. \tag{32}$$

The ratio g_{m1}/g_{m2} is thus limited by a lower bound set by the ratio of the voltage due to charge injection on C_h to the maximum acceptable residual offset. Its upper bound is determined by the ratio of the maximum admissible control voltage before the g_{m2} transconductor reaches saturation to the maximum initial offset to be compensated. Therefore, it must satisfy

$$\frac{\frac{q_{inj}}{C_h}}{V_{os\text{-}res\text{-}\max}} < \frac{g_{m1}}{g_{m2}} < \frac{V_{c\text{-}\max}}{V_{os\text{-}\max}}. \tag{33}$$

The minimum value of A_2A_3 should be such that the maximum residual offset due to finite gain remains smaller than the charge injection contribution:

$$\frac{V_{os\text{-}\max}}{A_2A_3} < \frac{A_2}{A_1}\frac{q_{inj}}{C_h} \tag{34}$$

leading to a condition on the gain A_2:

$$A_2 > \sqrt{\frac{A_1V_{os\text{-}\max}}{A_3\frac{q_{inj}}{C_h}}}. \tag{35}$$

There are several ways of realizing the additional nulling input port. Fig. 24(a) a shows a possible implementation where an additional differential pair M_3–M_4 (corresponding to transconductor g_{m2} in Fig. 23) is connected in parallel with the main input pair M_1–M_2 (corresponding to transconductor g_{m1} in Fig. 23) [1], [2], [4], [24]. Connecting both main inputs together to the common-mode voltage (to ground), the offset voltage of the main differential pair M_1–M_2 will produce a difference in the drain currents of M_1 and M_2. This offset current can then be cancelled by imposing the apropriate differential voltage on the nulling input, making the currents I_1 and I_2 equal. The complete AZ schematic is shown in Fig. 24(b), where two source followers M_{11}–M_{12}, two sampling switches and two hold

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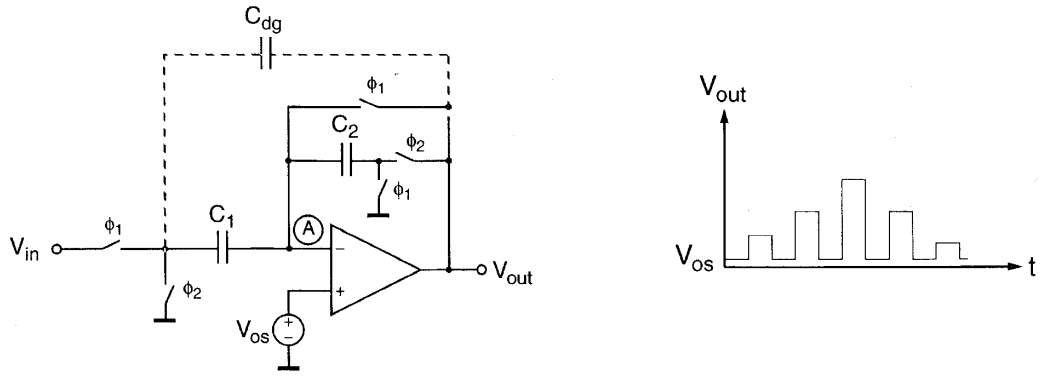

(a) (b)

Fig. 28. Offset-compensated SC amplifier: (a) schematic and (b) output signal.

capacitors C_1, C_2 have been added to perform the AZ operation [1], [2].

Another way of realizing the nulling input port is presented in Fig. 25. The adjustable current mirror M_1–M_2 is degenerated by two transistors M_3–M_4 operating in their linear regions and behaving as two resistors R_3 and R_4 controlled by voltages V_{NUL+} and V_{NUL-}, respectively [Fig. 25(b) and (c)]. Setting V_{NUL+} higher than V_{NUL-} implies that resistance R_4 becomes smaller than R_3. For a given input current I_1, the source voltage of M_2 is then smaller than that of M_1 resulting in an increase ΔI of the drain current of M_2 with respect to I_1. The current increase ΔI is almost a linear function of the differential nulling voltage V_{NUL+} and V_{NUL-} as shown in Fig. 25(d). This simple scheme has been used in several applications [1]–[4], and [26]. Residual offset voltages as small as 200 μV at a 3 V supply voltage have been reported [4].

F. Continuous-Time AZ Amplifiers

Some applications require continuous-time amplification and therefore the amplifier cannot be disconnected from the signal path in order to perform the AZ. This problem can be circumvented by duplicating the autozeroed amplifier and using one amplifier in its amplification mode while the other is being autozeroed. This time-sharing ("ping-pong") technique has been successfully used and described in [25], [26]. Nevertheless, switching the two amplifiers can result in spikes appearing at the output. This can be avoided by using another technique originally presented in [22] and recently used [35]. This scheme also uses two amplifiers as shown in Fig. 26: a main amplifier which is never disconnected from the signal path and an autozeroed amplifier (nulling amplifier) controlling the nulling input of the main amplifier. The basic idea behind this circuit is to use a low-offset amplifier to sense the main amplifier's offset and generate a correction voltage that is applied to the nulling input of the main amplifier to cancel its own offset. The nulling amplifier is autozeroed during phase ϕ_1 and its nulling voltage V_{c1} is stored on capacitor C_1 at the end of phase ϕ_1 and held during phase ϕ_2. The

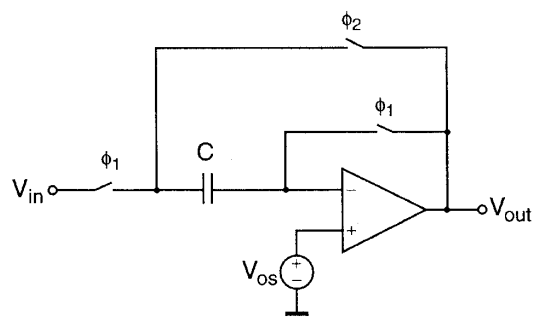

Fig. 29. A SC S/H stage.

nulling amplifier can therefore be considered as an almost offset-free amplifier that senses and zeroes the offset of the main amplifier during phase ϕ_2. The main amplifier nulling information V_{c2} is then sampled and held on capacitor C_2 during phase ϕ_1, while the nulling amplifier is zeroing its own offset. As shown in Fig. 26, this principle can only work if the overall amplifier is used with negative feedback in such a way that the voltage V_+–V_- appearing between the positive and negative input terminals is almost equal to the main amplifier offset $V_{os\text{-}m}$. This principle has been used in the commercially available op-amp ICL7650S [36] (which has been misnamed Super Chopper-Stabilized Operational Amplifier although it does not use CHS but rather AZ). This op-amp features a typical offset as low as $\pm 0.7\,\mu$V at room temperature [36]. Note that C_1 and C_2 are very large (typically 100 nF) off-chip capacitors in this application.

We shall next discuss the operation of the circuit in detail. During phase ϕ_1, corresponding to the state represented in Fig. 26, the nulling amplifier is disconnected from the signal path and is autozeroed. Its autocorrection voltage is then sampled on capacitor C_1 resulting in a control voltage V_{c1} across C_1 that is given by

$$\begin{aligned} V_{c1} &= -\frac{A_n}{1+A_n'}\,V_{os\text{-}n} + \Delta V_{c1} \\ &\cong -\alpha_n V_{os\text{-}n} + \Delta V_{c1} \end{aligned} \tag{36}$$

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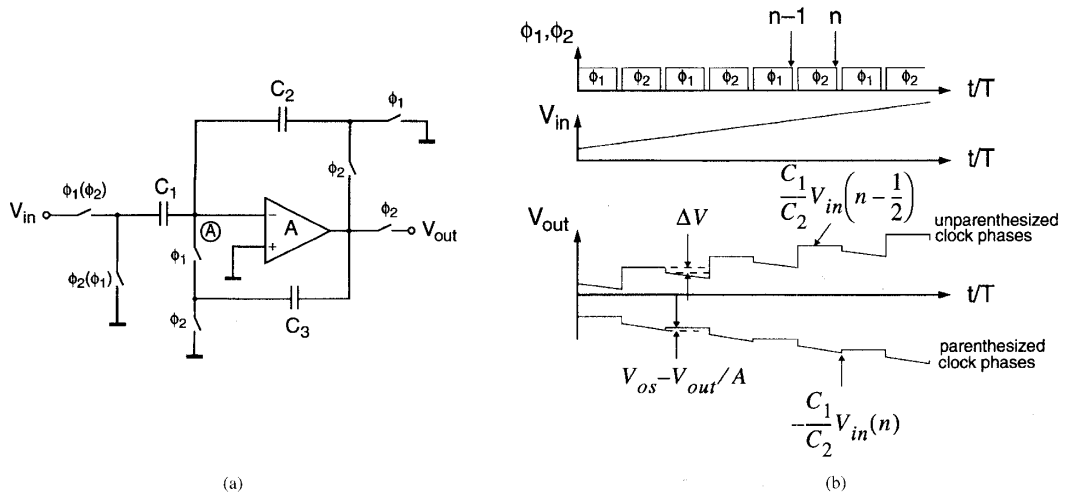

Fig. 30. Offset- and finite-gain compensated SC amplifier: (a) an offset and finite-gain compensated SC amplifier and (b) clock and signal waveforms.

where A_n is the gain of the nulling amplifier from its signal input, $A_n^{'}$ is its gain from the nulling input, and $\alpha_n = A_n/A_n^{'}$. Voltage ΔV_{c1} corresponds to the voltage change due to charge injection, sampled noise, and leakage current. It is given by (24), where C_h is replaced by C_1.

In the next phase ϕ_2, the inverting input of the nulling amplifier is connected back to the signal and its output is switched to the nulling input of the main amplifier. The output voltage of the main amplifier is given by

$$V_{\text{out}} = A_m(V_+ - V_- - V_{os\text{-}m}) + A_m^{'} V_{c2} \tag{37}$$

where A_m is the gain of the main amplifier from its signal input and $A_m^{'} = A_m/\alpha_m$ is the gain from the nulling input. V_{c2} is the correction voltage applied to the nulling input which during phase ϕ_2 is given by

$$\begin{aligned} V_{c2} &= A_n(V_+ - V_- - V_{os\text{-}n}) - A_n^{'} V_{c1} \\ &\cong A_n(V_+ - V_-) - \alpha_n V_{os\text{-}n} - A_n^{'} \Delta V_{c1} \end{aligned} \tag{38}$$

where it has been assumed that $A_n^{'} \gg 1$. By definition of the residual offset voltage $V_{os(2)}$, imposing $V_+ - V_- = -V_{os(2)}$ during phase ϕ_2 will bring the output voltage to zero. Hence, the offset voltage $V_{os(2)}$ of the main amplifier during phase ϕ_2 is obtained by introducing the expression of V_{c2} given by (38) into (37), setting the output voltage to zero and solving for $V_+ - V_- = V_{os(2)}$ which results in

$$V_{os(2)} \cong \frac{\alpha_m V_{os\text{-}m} + \alpha_n V_{os\text{-}n}}{A_n} + \frac{\Delta V_{c1}}{\alpha_n}. \tag{39}$$

Here it was assumed that the gain $A_n A_m^{'}$ from the input $(V_+ - V_-)$ through the nulling amplifier to the output (V_{out}) is much larger than the gain A_m of the main amplifier alone. When switch S_2 opens at the end of phase ϕ_2, the output voltage will change by an amount $\Delta V_{\text{out}} = A_m^{'} \Delta V_{c2}$, where the control voltage change ΔV_{c2} is due to charge injection, sampled noise and leakage current on capacitor C_2, and is given by (24) with C_h replaced by C_2. The

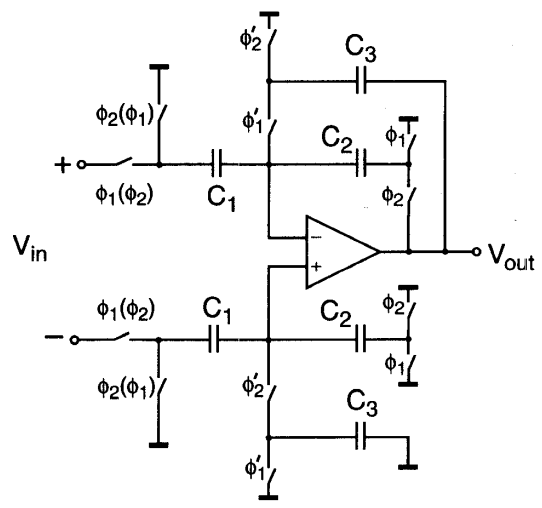

Fig. 31. An implementation of the scheme of Fig. 30. The primed clock phases cut off earlier than the unprimed ones.

initial input voltage equal to $V_{os(2)}$ should thus be reduced by an amount $\Delta V_{\text{out}}/A_m = \Delta V_{c2}/\alpha_m$ in order to bring the output voltage back to zero again. The resulting residual input-referred offset voltage $V_{os(1)}$ valid for phase ϕ_1 is therefore slightly different than for phase ϕ_2 due to charge injection onto C_2 and is given by

$$\begin{aligned} V_{os(1)} &= V_{os(2)} - \frac{\Delta V_{c2}}{\alpha_m} \\ &\cong \frac{\alpha_m V_{os\text{-}m} + \alpha_n V_{os\text{-}n}}{A_n} + \frac{\Delta V_{c1}}{\alpha_n} - \frac{\Delta V_{c2}}{\alpha_m}. \end{aligned} \tag{40}$$

In the case the gains of the main and nulling amplifiers from their signal inputs are equal to their gains from their nulling inputs (corresponding to $\alpha_n = \alpha_m = 1$, (39) and (40) show that the residual offset is basically equal to the

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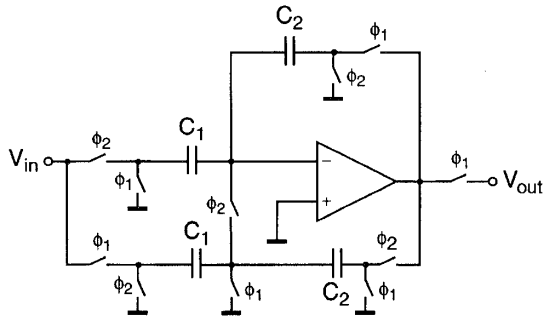

Fig. 32. A wideband compensated SC amplifier.

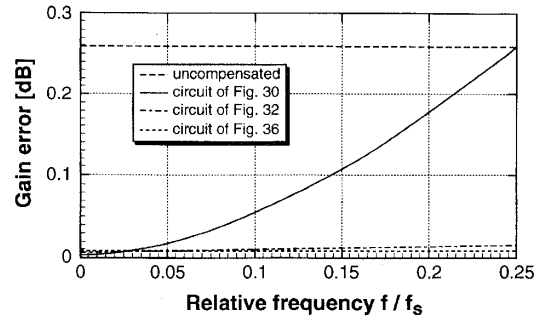

Fig. 33. Gain error versus frequency curves for compensated SC amplifier.

sum of the main and nulling amplifiers offsets, divided by the gain of the nulling amplifier A_n, plus the charge injection terms. The latter contribution can be reduced by decreasing the gains from the nulling input relative to the gains from the main inputs for both amplifiers. (This corresponds to setting both α_n and α_m larger than one.) The design criteria are very similar to those discussed in Section IV-E for the AZ scheme using an auxiliary input port.

As was suggested in [35], the injection terms contained in ΔV_{c1} and ΔV_{c2} can be reduced to a mismatch of injection by using a differential nulling input as shown in Fig. 24(a) or Fig. 25(a).

It should be noticed that during phase ϕ_2 the autozeroed amplifier has two forward signal paths: one directly through the main amplifier and the other through the nulling amplifier and the nulling input of the main amplifier. The dc gain is therefore equal to $A_m + A_n A_m^{'}$, but generally reduces to $A_n A_m^{'}$ corresponding to the gain from the input through the nulling amplifier and the main amplifier's nulling input.

The frequency responses of the main and nulling amplifiers must be designed so as to ensure that the autozeroed amplifier is stable during both phases. Stability during phase ϕ_1 requires that the main amplifier's primary input signal path and the nulling amplifier's auxiliary input signal path be unity-gain stable. The stability conditions during phase ϕ_2 depend on how the auxiliary inputs are realized. A detailed discussion of the stability of a particular implementation can be found in [35].

It should be noticed that since voltages V_{c1} and V_{c2} are generally not equal, a transient spike may appear at the amplifier output at the beginning of phase ϕ_2 when switch S_2 is connected to capacitor C_2. Assuming that no signal is present at the amplifier input, the instantaneous value of the amplifier output voltage during ϕ_2 after the transient has vanished might be slighly negative in order to compensate for a positive spike and maintain a zero mean value. Another potential problem is caused by signals that are near or equal to an integer multiple of the clock frequency and that appear at the virtual ground of the amplifier. Such signals are sampled on C_2 at the end of phase ϕ_2 and may be aliased down to dc [35]. This will result in an apparent offset which is different than the real main amplifier offset voltage $V_{os\text{-}m}$ which is to be compensated. To circumvent this problem, the voltage V_{c2} should be proportional to the mean value of the voltage at the virtual ground node. This can be achieved by low-pass filtering the signal when sensing the main amplifier input voltage during phase ϕ_2. A way to implement this low-pass filter is to use an operational transconductance amplifier (OTA) instead of an op-amp for the nulling amplifier [35] as shown in Fig. 26. The OTA is loaded by capacitor C_2 which is generally an external capacitor and can therefore be chosen rather large, setting the cut-off frequency at a very low frequency. The linear range of the OTA should be chosen sufficiently large in order to avoid any saturation due the sum of the dc offset to be compensated and the parasitic signal to be filtered.

V. Precision Building Blocks Using the Correlated Double Sampling Technique

This section presents some examples of basic building blocks such as S/H stages, voltage amplifiers, integrators, and filters, that use the CDS technique to reduce the amplifier's offset and noise as well as to lower the effect of the finite amplifier gain.

A. SC S/H and Voltage Amplifiers

The CDS technique described earlier in Section IV-C for AZ comparators can readily be applied to SC voltage amplifiers. Fig. 27 illustrates a conventional SC amplifier [50]. The nominal output is $V_{out} = -(C_1/C_2)V_{in}$, but finite op-amp gain changes the ideal voltage gain to

$$\hat{A}_v = \frac{A_v}{1 + \dfrac{1 + A_v}{A}} \tag{41}$$

where $A_v = -C_1/C_2$ is the ideal gain, and A is the dc gain of the op-amp. Thus for typical values of A and A_v, a gain error of 1% or more may occur. In some high-precision applications, e.g., if the amplifier is part of a DAC or ADC, this may be unacceptable.

Also, a nonzero input-referred dc op-amp offset V_{os} will introduce an output offset voltage $V_{os\text{-}out} = (1 + |A_v|)V_{os}$. Since V_{os} is typically 1–10 mV, and $|A_v|$ can have a value

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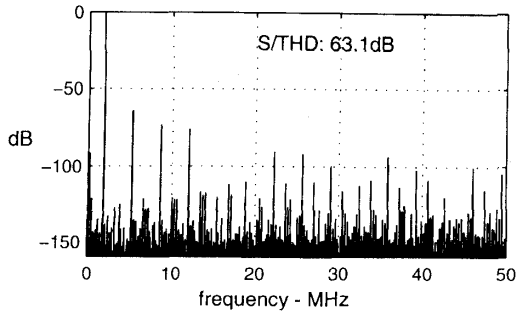
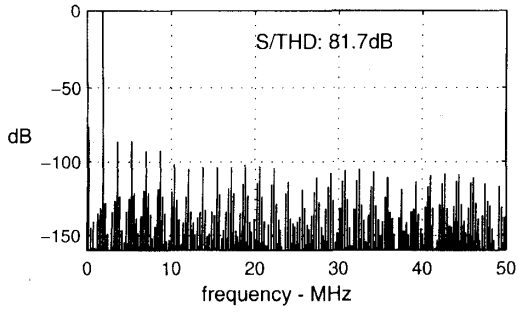


(a)



(b)

Fig. 34. Output spectra of SC amplifiers using nonlinear op-amps. The op-amp offset assumed was 5 mV, and the SC amplifier voltage gain was −2: (a) offset-compensated SC amplifier (Fig. 28) and (b) wideband compensated SC amplifier (Fig. 32).

of 10 or more, the output offset may become a significant limitation on the permissible signal swing, especially in a low-voltage technology. It also may introduce ADC or DAC offset which needs to be calibrated.

If only the offset needs to be eliminated, the simple amplifier stage introduced by Gregorian [51] may be used [Fig. 28(a)]. Here, during the $\phi_1 = 1$ period, C_1 charges to V_{in}–V_{os}, and C_2 to V_{os}. V_{out} is developed during the $\phi_2 = 1$ interval. In this circuit, capacitors C_1 and C_2 are always connected to the virtual ground node Ⓐ, so if the input-referred offset voltage is constant, then when the switches driven by ϕ_2 close, the total charge entering node A is $C_1 V_{in} + C_2 V_{out} = 0$, which leads to the desired relation between V_{in} and V_{out} independent of V_{os}. However, as Fig. 28(b) illustrates, during the $\phi_1 = 1$ intervals the output is pulled to V_{os}, and the op-amp must have a high slew rate and fast settling time to enable V_{out} to slew back and forth at each clock transition. Also, the closed-loop gain of the stage is still affected by the dc gain of the op-amp the same way as in the circuit of Fig. 27.

Note that the small "deglitching" capacitor C_{dg} does not play a role in the signal charge redistribution. Its sole purpose is to prevent glitches in the op-amp output by providing negative feedback during the brief intervals when the nonoverlapping clock phases are both low, and the feedback path of the op-amp is otherwise open-circuited [52].

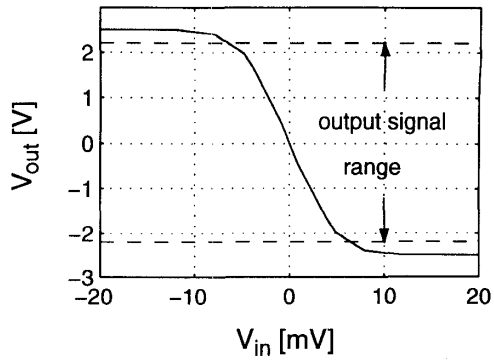


Fig. 35. The nonlinear op-amp transfer characteristics.

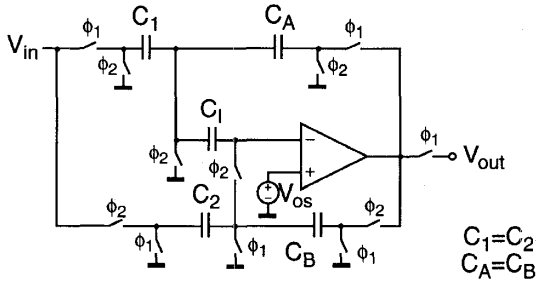


Fig. 36. SC amplifier with offset storage capacitor.

A unity-gain buffer stage, which can be used as a simple S/H circuit, or as an analog memory, or as an analog delay stage, and which also utilizes CDS to reduce dc offset effects, is shown in Fig. 29 [53]. Here, C charges to $V_{in} - V_{os}$ during $\phi_1 = 1$ period, and is connected as a feedback branch during $\phi_2 = 1$, causing $V_{out}(n) = V_{in}(n - 1/2)$. As in the previous circuit, the op-amp output voltage is reset to V_{os} in every clock period, and hence the slew-rate and settling-time requirements are difficult to meet for high clock rates. Also, the op-amp gain affects V_{out}. Note that the operation of this circuit does not depend on the exact value of its single capacitor.

An SC amplifier which does not require a resetting of the output in each clock period and also reduces the effect of the op-amp gain, and hence allows more relaxed op-amp specifications for low-frequency inputs, is shown in Fig. 30(a) [54]. In this circuit, the feedback reset switch is replaced by the elementary S/H branch consisting of C_3 and its two associated switches. Assume that the circuit is used as a noninverting amplifier, and hence the clock phases shown outside of the parentheses in Fig. 30(a) are valid. Then, when $\phi_2 \to 1$, C_1 discharges into C_2, and the valid output voltage is generated. This voltage is stored in C_3. When $\phi_1 \to 1$ next, C_3 becomes the feedback capacitor, while C_1 samples the difference between the input and the voltage at node Ⓐ and C_2 discharges. If the signal bandwidth is much smaller than $f_s/2$, i.e., if the signal is significantly oversampled, then V_{out} does not vary much from one clock phase to the next. Thus for a finite dc

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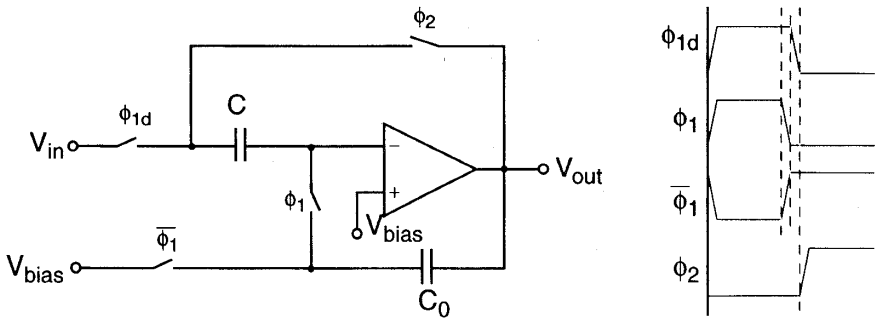

Fig. 37. Offset- and gain-compensated SC buffer.

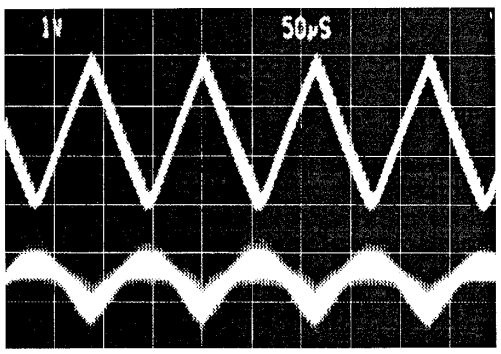

Fig. 38. Experimentally observed output voltages for offset-compensated SC buffers with a triangle-wave input at high clock rates. Top curve: buffer of Fig. 37; bottom curve: buffer of Fig. 29.

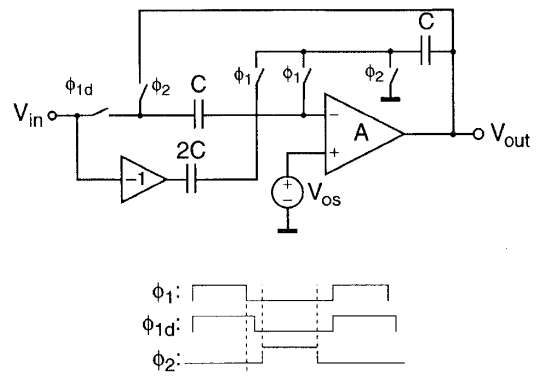

Fig. 39. A wide-band T/H stage.

op-amp gain A, the signal voltage $-V_{out}/A$ at the virtual ground is a slowly varying signal which is therefore nearly cancelled by the CDS switching of C_1 and C_2. This reduces the effect of finite A on the voltage gain of the stage.

Fig. 30(b) illustrates the clock phases and waveforms of the amplifier. When $\phi_1 \to 1$ and the reset phase begins, there is a small step $\Delta V = V_{os} - V_{out}/A - (C_1/C_3)\Delta V_{in}$ in the output voltage, where ΔV_{in} is the change in V_{in} during the $\phi_2 = 1$ interval (The ΔV_{in} term enters only for noninverting operation.) This step occurs because, as $\phi_2 \to 1, C_3$ is disconnected from ground and reconnected to the virtual ground. As ΔV is of the order of a few mVs, this does not require a fast settling time or a high slew rate from the op-amp. The dc output offset voltage is $(1 + C_1/C_2)(V_{os}/A)$, which is much smaller than V_{os}.

Detailed analysis [54] shows that the gain is now weakly frequency dependent due to the high-pass CDS effect on the virtual ground voltage, with the dc gain given by

$$H(z)|_{z=1} = \frac{-\dfrac{C_1}{C_2}}{1 + \dfrac{\left(1 + \dfrac{C_1}{C_2}\right)}{A^2}}. \tag{42}$$

As (42) demonstrates, the error term in the denominator of the transfer function is now proportional to A^{-2}, rather than A^{-1}. Thus the effective value of the op-amp gain as far as the dc gain is concerned is the square of the true value. Circuits with this property are called *gain-enhanced* or *gain-squaring* stages.

Fig. 31 shows a differential-input/single-ended-output SC amplifier incorporating the described principle [55]. Its CMOS implementation exhibited an accurate stage gain and a total of about 10 mV output offset, a 0.1–0.2% signal distortion and a 50 dB CMRR, in addition to a very low op-amp gain sensitivity.

The circuit of Fig. 30 was also successfully used in an GaAs SC amplifier, where the op-amp gain was restricted by the technology used [60].

The frequency dependence of the voltage gain of the compensated amplifier can be reduced, and thus the operation of the circuit extended to higher signal frequencies, by using the anticipatory compensation (prediction/correction) principle illustrated by the circuit shown in Fig. 32 [56]. Here, the precharging of the signal-processing capacitors is performed using the virtual-ground signal voltage that is expected to be present during the next amplification phase. This is achieved by essentially duplicating the SC branches used in the amplifier, and performing an anticipatory amplification step during the $\phi_2 = 1$ phase. If V_{in} changes only when $\phi_1 \to 1$, the operation will be independent of the rate of change of V_{in}, and hence of the signal frequency.

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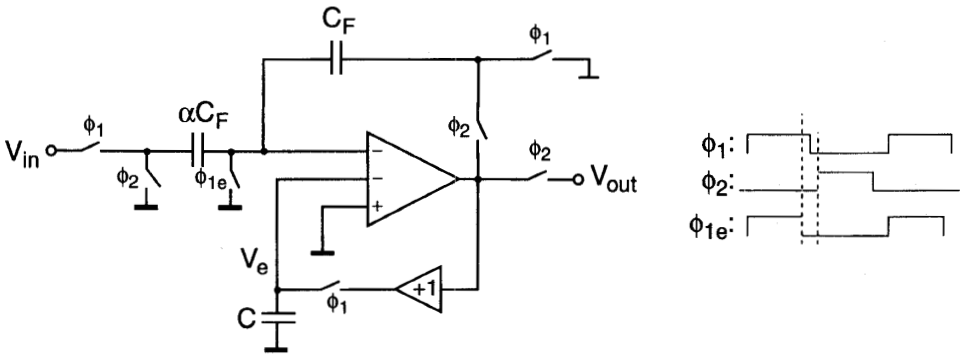

Fig. 40. Offset-compensated SC voltage amplifier using a low-sensitivity auxiliary input.

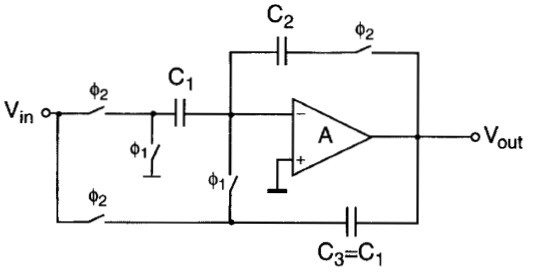

Fig. 41. Offset- and gain-compensated SC integrator.

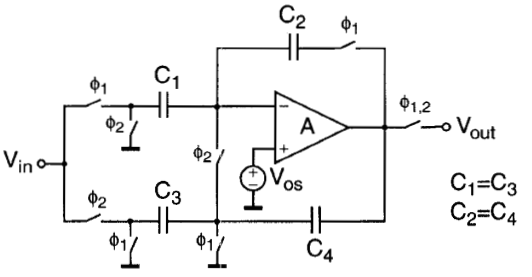

Fig. 42. Wideband compensated SC integrator.

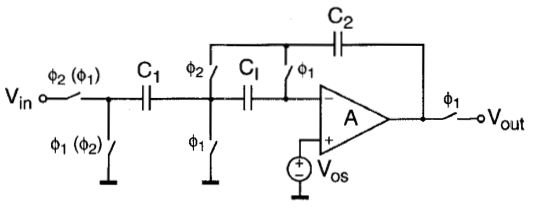

Fig. 43. SC integrator with offset-storing capacitor.

The effectiveness of this principle is illustrated in Fig. 33, which compares the gain error versus frequency responses of an uncompensated SC amplifier with that of the stage of Fig. 30, and of the circuits of Figs. 32 and 36. The ratio of the dc op-amp gain to the desired stage gain was about 30. As the curves illustrate, the dc gain error is higher for the anticipating stage (because the error term is now $(1 + C_1/C_2)^2/A^2$, rather than $(1 + C_1/C_2)/A^2$ as for the circuit of Fig. 30, but the error remains essentially constant all the way up to $f_s/4$. The output voltage step for a constant input due to offset and finite gain is $\Delta V = (1 + C_1/C_2)(V_{os} - V_{out}/A)$. This is again typically of the order of 10 mV, not putting much strain on the op-amp.

The gain-enhancing property of CDS also helps to reduce the harmonic distortion caused by the nonlinear op-amp gain characteristics [74]. This is illustrated in Fig. 34, which compares the output spectra of the amplifiers of Figs. 28 and 32 for a 4.4 V output sine-wave signal. The assumed op-amp gain characteristic is shown in Fig. 35.

A different implementation of the anticipatory compensation principle, which uses an offset-storage capacitor C_I playing a somewhat similar role to that of C in the autozeroed amplifier of Fig. 21, is shown in Fig. 36 [57]. Its frequency response is very similar to that of the circuit of Fig. 32, and is also included in Fig. 33 (bottom curve).

The gain-compensating techniques described above can also be extended to the design of unity-gain buffers, T/H stages and memory or delay stages. Fig. 37 shows an improved version of the offset-compensated buffer of Fig. 29, which does not require the resetting of the output voltage to V_{os} in every clock period [58]. Here, the reset switch is replaced by the S/H capacitor C_0 which holds the output voltage close to its previous value during the reset period. This also reduces the effects of the finite op-amp gain.

Fig. 38 shows some experimental results demonstrating the speed improvements achieved by this scheme over that of Fig. 29 [58].

An even faster version of the circuit, which relies on anticipating rather than storing the output voltage, is shown in Fig. 39 [59]. It is only practical to implement in fully differential form. In this circuit, the output signal tracks the input during the $\phi_1 = 1$ interval without inverting it. Hence, the virtual ground voltage at the instant when $\phi_2 \rightarrow 1$ will have the required value, independent of the signal frequency.

An alternative approach to offset compensation, which can also include the compensation of clock-feedthrough effects, but which does not enhance the effective value of

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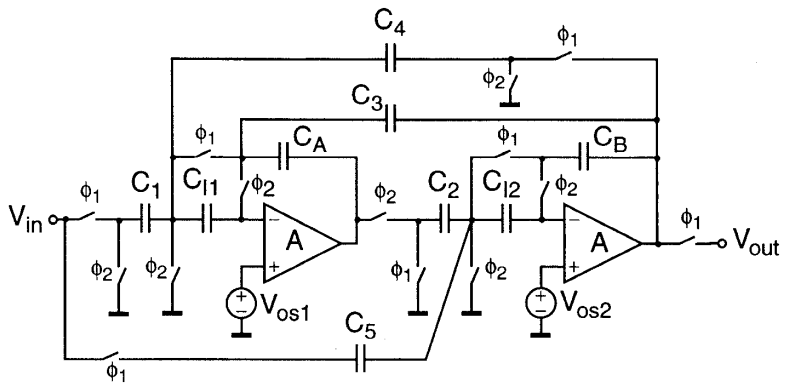

Fig. 44. Gain- and offset-compensated high-Q biquad.

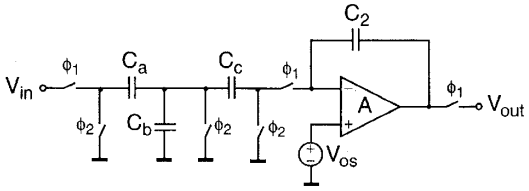

Fig. 45. Basic very-large-time-constant (VLT) integrator.

the dc op-amp gain, was discussed in Section IV-E earlier. It is shown schematically in Fig. 40. In this circuit, during the compensation phase ($\phi_1 = 1$), an error correction voltage V_e is developed across C. To reduce the effect of charge injection occurring when C is disconnected from the buffer as $\phi_2 \to 0$, the gain $|V_{\text{out}}/V_e|$ should be much lower than the signal gain of the op-amp. (See Section IV-E for a discussion of the optimization of this circuit.)

B. SC Integrators and Filters

The compensation schemes described in Section V-A are, with minor modifications, applicable also to SC integrators. As an overview of Section V-A reveals, these schemes fall into the following categories:

1) output is reset to V_{os}; input capacitor stores and then subtracts V_{os} (Figs. 28 and 29);
2) output is held during reset; input and feedback capacitors are referenced to the previous value of virtual-ground voltage V_A (Figs. 30, 31, and 37);
3) output during reset anticipates the next signal output; signal-path capacitors are referenced to the anticipated value of V_A with (Fig. 36) or without (Figs. 32 and 39) the use of an extra offset-storage capacitor C_I;
4) auxiliary input signal is established during reset; then it compensates for slowly varying noise effects (offset, $1/f$ noise, clock feedthrough); see Fig. 40.

As discussed above, the circuits using techniques 1) and 4) are relatively simple, but they cannot provide finite-gain compensation. Those using scheme 2) are more complex, but they perform also gain squaring at or near dc. Finally, the circuits using the anticipatory compensation scheme 3) tend to be even more elaborate, but they provide gain compensation over a wide signal-frequency range. This improves the linearity of the stage. The use of more switches may, however, increase the sampled wideband noise in the output signal of these circuits.

Next, we shall briefly discuss how these CDS techniques can be used in SC integrators. In Fig. 28(a), by eliminating the switch grounding the right-side terminal of C_2 during reset, an offset- (but not gain-) compensated integrator results [51]. Similarly, it is possible to leave out the grounding switch of C_2 in the circuit of Fig. 30(a) to obtain an offset- and gain-compensated SC integrator [61]. However, the charge flow into node A from C_1 as $\phi_1 \to 1$ is now not balanced by an equal and opposite charge from C_2 as in Fig. 30(a), and hence, the gain compensation becomes inaccurate. This problem can be solved for an inverting integrator by a slight change in the switching arrangement for C_3 [54], as shown in Fig. 41. For noninverting integration, a slightly more elaborate circuit is needed [54].

Similarly, the wideband amplifier of Fig. 32 can be transformed into a gain- and offset-compensated integrator [56] by eliminating the switches discharging the feedback capacitor C_2 (Fig. 42).

Efficient gain- and offset-compensated integrators can also be obtained by using an offset-storage capacitor C_I. Fig. 43 illustrates a noninverting integrator [57] based on this principle. The circuit can also be used as an inverting integrator with a full clock period delay, if the clock phases of the input switches are interchanged. It was later independently recognized by several researchers [62], [63] that the integrator of Fig. 43 can also be used as a delay-free inverting integrator, by changing its switching scheme and choosing the value of C_I equal to that of the feedback capacitor C_2.

It is also possible to apply scheme 4) (i.e., auxiliary input compensation) to SC integrators [64]. As before, the correction reduces the low-frequency noise (including that due to charge injection), but it does not compensate for

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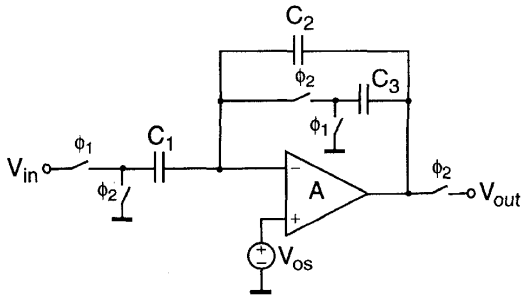

Fig. 46. Improved VLT integrator.

finite op-amp gain effects. It was used successfully in a high-accuracy low-voltage CMOS A/D converter [66].

Using the compensated integrators as building blocks, SC filters can thus be made insensitive to offset, $1/f$ noise and finite-gain effects. As an illustration, Fig. 44 shows a gain- and offset-compensated high-Q biquad [67] based on the modified version of the integrator of Fig. 43.

An important application of offset- and gain-compensated integrators is in delta-sigma A/D converters. Low-frequency noise and offset in the input integrator of the converter enters the output signal unfiltered, and hence should be suppressed. Also, in the cascade (MASH) architecture, the finite gain of the op-amp of the input stage allows the leakage of large unfiltered 1-b quantization noise into the output signal. Both problems can be remedied by using a compensated integrator in the input stage. Successful implementations of delta-sigma converters using offset- and gain-compensated front ends have been reported in [68]–[70].

C. SC Filters with Very Large Time Constants

In some applications, the magnitudes $|p_i|$ of the poles realized by SC filters are much smaller than the clock frequency $f_s = 1/T$. Since the time constants TC_2/C_1 of the integrators used in the filter are around $1/|p_i|$, now $C_2/C_1 \approx 1/(|p_i| \cdot T) \gg 1$ is required. This results in large chip area requirements. To remedy this situation, several ingenious schemes have been proposed. One option [72] is to use a T-cell attenuator at the input (Fig. 45). As a result of the charge redistribution in the T-cell, the capacitance spread $S = C_{\max}/C_{\min}$ can be reduced approximately to $\sqrt{S}$, and the chip area will be correspondingly smaller.

The T-cell integrator is sensitive to the stray capacitance in parallel with C_b, and it requires two large capacitors (normally, $C_b = C_2 \approx \sqrt{S} \cdot C_a = \sqrt{S} \cdot C_c$ are chosen). An improved very-large-time-constant (VLT) integrator [73] is shown in Fig. 46. Analysis shows that the circuit is equivalent to an integrator with a capacitance ratio $C_2/C_1 > 1$, followed by a voltage division by $1+C_2/C_3$. If $C_1 = C_3 \approx C_2/\sqrt{S}$ are chosen, the ideal performance of the circuit will be the same as that of the T-cell integrator; however, it is stray-insensitive, and it needs only one large capacitor, C_2.

A major flaw of both VLT circuits is their extreme sensitivity to offset, noise and charge-injection effects. To illustrate this point, consider the dc offset performance

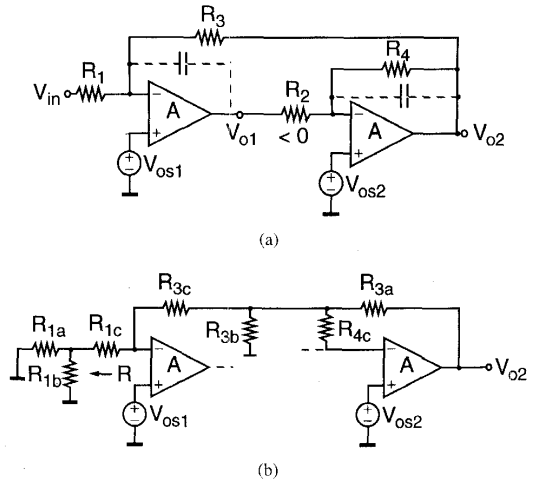

Fig. 47. The dc equivalent circuits: (a) dc equivalent circuit of a low-Q biquad and (b) dc equivalent circuit of a VLT biquad using T-cells.

of a conventional two-integrator loop where the familiar SC $\leftrightarrow R$ equivalence [50] was used [Fig. 47(a)]. Since V_{o2} has to generate V_{os1} at the virtual ground of the first op-amp by voltage division, we obtain $V_{02} = (1+R_3/R_1)V_{os1}$. For a VLT biquad, R_3 and R_1 are both large, and $V_{02} \approx 2V_{os}$ to $10\,V_{os}$ results. By contrast, for a T-cell biquad, as the dc equivalent circuit of Fig. 47(b) illustrates, V_{o2} is divided twice before producing V_{os1}. This requires a much larger output offset voltage V_{o2}, often as large as $100\,V_{os1}$ to $200\,V_{os1}$. A similar argument shows that charge injection will also cause a large output offset. While the explanation is not so obvious for the VLT integrator of Fig. 46, it leads to a similar result: small dc offsets become amplified 100 times or more in the output signal of filters containing such stages.

To reduce this sensitivity, the VLT integrators should be compensated for their low-frequency noise, offset, and (if possible) charge injection. Figs. 48 and 49 illustrate the use of offset-storing capacitors in the circuits of Figs. 45 and 46, respectively [71]. These circuits reduce the low-frequency noise, and also the finite-gain effect on the frequency response. They do not, however, compensate for charge feedthrough; hence, the VLT filters should make full use of the well-known techniques (fully differential circuitry, delayed-cutoff clock signals, dummy switches, etc.) for reducing clock-feedthrough effects.

The improvement in finite-gain performance afforded by the compensated integrators is illustrated in Fig. 50. This shows the simulated gain responses of an eighth-order SC low-pass filter with Bessel–Chebyshev characteristics, a clock rate $f_s = 9.766$ kHz and a cutoff frequency of 2.5 Hz. The circuit of Fig. 46 was used, with (top curve) and without (bottom curve) gain- and offset-compensation. An op-amp gain of only 40 dB was assumed. The phase response is also distorted by the finite op-amp gain and restored by using CDS.

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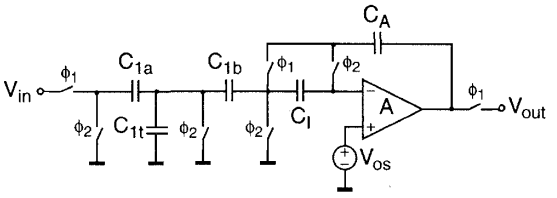

Fig. 48. T-cell integrator with offset compensation.

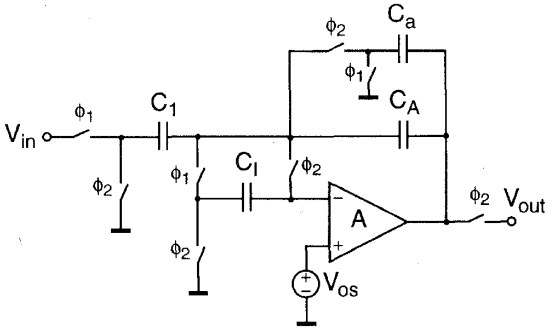

Fig. 49. The VLT integrator of Fig. 46 with offset compensation.

VI. A Micropower Low-Noise Chopper Amplifier Using the Chopper Stabilization Technique

This section presents a practical example of the use of the CHS technique in an amplifier to reduce its offset and $1/f$ noise without degrading the wideband noise. Unlike the many examples of the use of CDS in SC circuits, some of which were presented in Section V, there are very few examples of circuits that use CHS. The latter are generally low-noise continuous-time amplifiers, mainly used for instrumentation applications such as biomedical electronics.

Some applications such as electronic sensor interfaces require not only a very small offset and offset drift, but also very low noise. Often, the CHS technique is best suited to such applications. The electronics containing the front-end low-noise amplifier and the signal conditioning circuits, combined with the sensor, forms a microsystem which often has to be portable or stand alone, and is therefore battery powered. Hence, the power consumption of the electronics has to be small. It is therefore even more crucial to eliminate the $1/f$ noise and to reduce the noise down to the fundamental thermal noise which is mainly determined by the allowable current consumption of the input stage.

Examples of low-noise chopper amplifiers with a very low power consumption have been presented in [8], [12]. The design objective was to reach the microvolt level for both offset and noise, with a bandwidth limited to a few hundred Hz, while maintaining the power consumption below 100 μW. This chopper amplifier used a selective stage with its center frequency locked to the chopper frequency in order to minimize the residual offset, as explained in Section III. The chopper amplifier presented in Fig. 9 where the amplifier is replaced by a selective amplifier and the

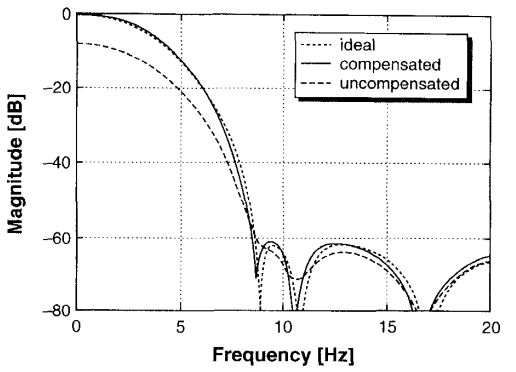

Fig. 50. Frequency responses of VLT filters.

output is low-pass filtered at half the chopper frequency, has an overall low-pass transfer function given by

$$G_0(s) \cong \frac{8}{\pi^2} \frac{A_{\max}}{1 + s/\omega_c} \tag{43}$$

where $\omega_c = \omega_0/(2Q)$ is the chopper amplifier's cutoff frequency, determined by the selective amplifier's resonant frequency ω_0 and quality factor Q. $A_{\max}$ corresponds to the gain of the selective amplifier at the resonant frequency. Equation (43) has been obtained assuming that $Q \gg 1$ and is valid for $|s| \ll \omega_0$. It shows that the chopper amplifier's dc gain is only $\pi^2/8 = 1.234$ (or approximately 2 dB less than the gain of the selective amplifier at the resonant frequency).

The selective amplifier can be realized using either a low-pass [12] or a band-pass second-order $g_m - C$ continuous-time filter [44]–[49]. The advantage of choosing the band-pass circuit is that the input and output chopper modulation signals can be identical, since there is no phase shift at the resonant frequency. The filter's resonant frequency can be locked to the chopper frequency by means of a PLL using either a voltage-controlled reference filter [44], [48] or a voltage-controlled oscillator built using the same resonator as the selective amplifier [44], [47], and [49].

An example of such a band-pass filter is presented in Fig. 51. The gain $A_{\max}$ at the resonant frequency is given by the ratio g_{m1}/g_{m4}, where g_{m1} and g_{m4} are the transconductances of the input and output stages, respectively. This ratio has to be large in order to have a sufficient dc gain for the chopper amplifier. Typically, for a dc gain of 500, the g_{m1}/g_{m4} ratio has to be 617! This large gain imposes the use of linearized transconductors for realizing the integrators and the output load [47], in order to limit the distortion and intermodulation. Another problem arising from this large gain is the mistuning effect resulting from the difference between the bias currents of the integrators. This is due to the fact that the offset of the input differential pair T_1–T_1' appears at the low-pass output multiplied by the corresponding dc gain, while the band-pass output offset stays at zero. This offset voltage is fed to the input of differential pair T_3–T_3' and compensates the offset current due to the input differential pair, forcing the band-pass

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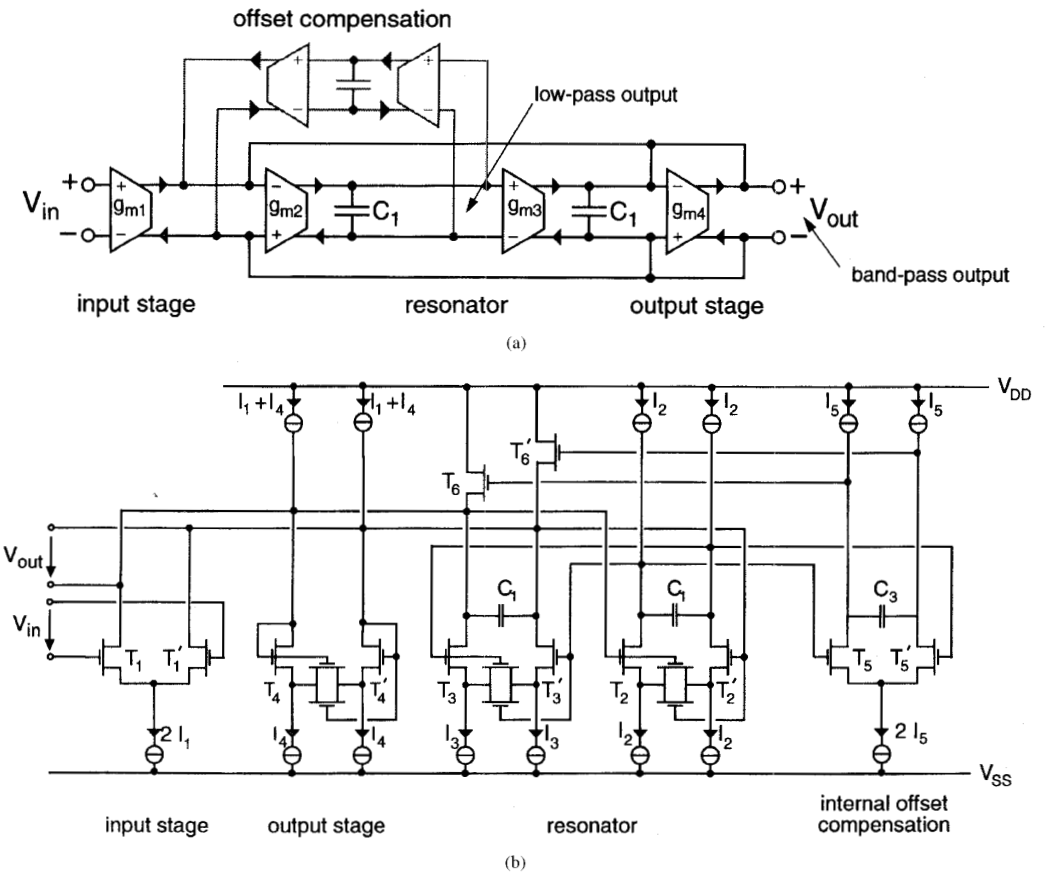

Fig. 51. Second-order $g_m - C$ continuous-time band-pass filter used to realize the selective amplifier: (a) principle and (b) implementation.

output to stay at zero. The resulting mismatch between the biasing points of the two integrators gives rise to a nonzero phase shift at the chopper frequency, which is unacceptable for the chopper amplifier. Fortunately, since the signal is modulated and amplified at high frequency, the current offset ΔI_1 produced by the mismatch of input differential pair T_1–T_1' can be compensated without changing the signal transfer function. This offset compensation can be realized as shown in Fig. 51, by sensing the offset voltage with differential pair T_5–T_5' at the low-pass output (i.e., at the input of differential pair T_3–T_3' and injecting the current necessary to compensate the offset current ΔI_1 using transistors T_6–T_6'. This compensation does not require any S/H action since the signal is mainly centered around the resonant frequency. The feedback loop can therefore be held closed continuously if a compensation capacitance C_3 is added at the output of differential pair T_5–T_5' to ensure stability.

The measured frequency responses of the selective amplifier and the chopper amplifier are shown in Fig. 52(a) and (b), respectively. The gain measured at the filter's 4 kHz resonance frequency is equal to 56.8 dB, corresponding to a 54.8 dB dc gain for the chopper amplifier. The quality factor is 5.4 which sets the −3 dB cut-off frequency of the chopper amplifier to 367 Hz.

Using (21), the chopper amplifier's input-referred noise can be found from

$$S_{Nin} = \frac{\pi^2}{8} 4\gamma kTR_{Nin}\left(1 + 0.8525\frac{f_k}{f_{chop}}\right) \tag{44}$$

where R_{Nin} is the equivalent input thermal noise resistance of the selective amplifier, which is inversely proportional to the transconductance g_{m1} of the input differential pair. Noise factor γ is defined as the product $g_{m1}R_{Nin}$ and accounts for the excess thermal noise coming from sources other than the input stage.

The low-frequency output noise of the chopper amplifier has been measured and is shown in Fig. 53. As expected, the $1/f$ noise has disappeared, leaving a white noise PSD corresponding to an equivalent input-referred white noise of 43 nV/$\sqrt{\text{Hz}}$, which can still be made lower at the expense of an increase of the input differential pair bias current and thus of the total power consumption.

The input and output chopper modulators are simply realized by four switches controlled by complementary phases,

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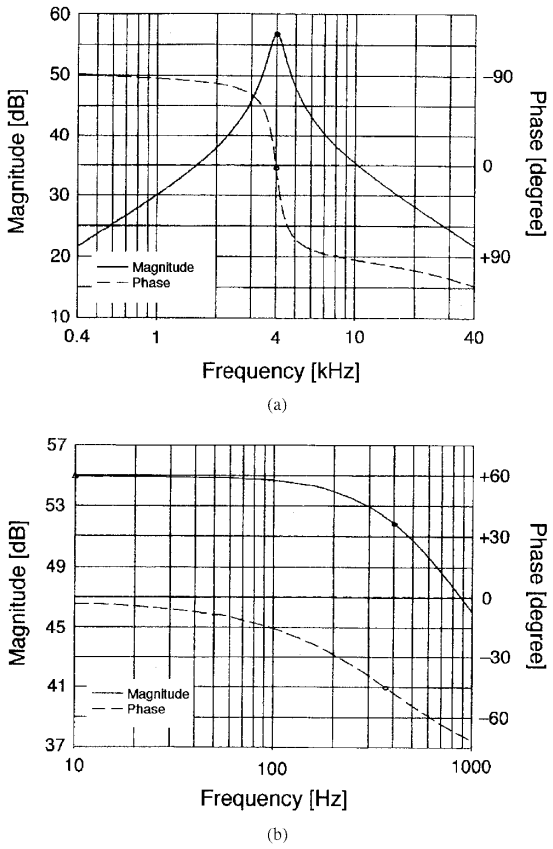

Fig. 52. Measured frequency response of the selective amplifier (a) and the chopper amplifier (b) with a chopper frequency locked to the 4 kHz resonance frequency.

as shown in Fig. 54, where capacitance C_{in} represents the differential input capacitance of the selective amplifier.

At each switching instant, error charges Δq_i $(i = 1, 2, 3)$ result from charge injection and clock-feedthrough mismatches between the different switches. Charges Δq_1 and Δq_3 flow to capacitor C_{in}, while charge Δq_2 flows to ground through the source resistance R_S, producing some spikes at the input of the selective amplifier. An estimation of the residual input-referred offset V_{os} of the chopper amplifier due to the injection of these charges can be derived by assuming that:

1) clock rise and fall times are much smaller than the time constant τ of the spikes;
2) the output modulator is ideal;
3) $\Delta q_1 = \Delta q_2 = -\Delta q_3 = \Delta q$ (representing the worst case);
4) all switches have the same on-resistance R_{on};
5) the source resistance R_S is much smaller than R_{on}.

This leads to [8], [12]

$$V_{os} \cong 4\pi f_{\text{chop}} \Delta q R_{on} (2\pi f_{\text{chop}} R_{on} C_{in} + Q\varepsilon_{tun}) \quad (45)$$

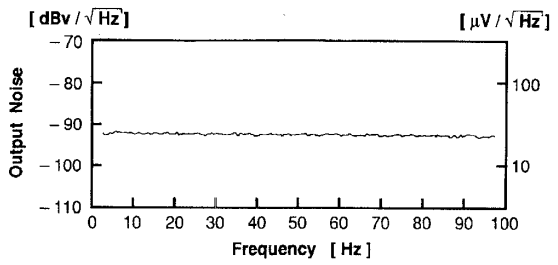

Fig. 53. Measured low-frequency output noise PSD of the complete chopper amplifier.

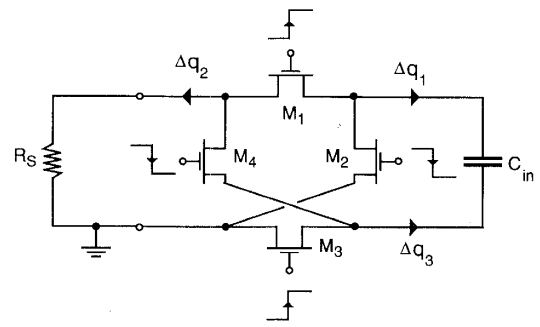

Fig. 54. Implementation of the input chopper modulator.

where $\varepsilon_{tun} \equiv |f_0/f_{\text{chop}} - 1|$ represents the tuning error between the resonance frequency f_0 and the chopper frequency f_{chop}. It can easily be shown that the product $\Delta q R_{on}$ is independent of the switch width W and is minimum for a minimum channel length. Equations (44) and (45) show that there is a trade-off between the noise and the offset with respect to the chopper frequency: according to (45), the chopper frequency should be chosen as small as possible, but nevertheless equal to or larger than the amplifier's corner frequency. In the case where both offset and noise have to be minimized, it is useful to define a total noise power as the sum $V_{os}^2 + V_{Nin}^2$ where V_{Nin} is the total input-referred noise rms voltage. An optimum value of the chopper frequency can be found such that this total noise power is minimum for a given signal bandwidth [8].

The linear dependence of the input-referred offset on small tuning errors as indicated by (45), has been verified experimentally and is presented in Fig. 55. An input-referred offset as small as 0.5 μV and a sensitivity to the tuning error of 0.47 μV per percent of mistuning has been measured.

In case the source resistance R_S is much larger than the switch on-resistance R_{on}, the input offset is still given by (45) but R_{on} has to be replaced by R_S. Hence, the input offset increases quadratically with the source resistance which is in accordance with the experimental results presented in Fig. 56.

The offset voltage drift could not be measured, but other chopper-stabilized amplifier have reported extremely good stability.

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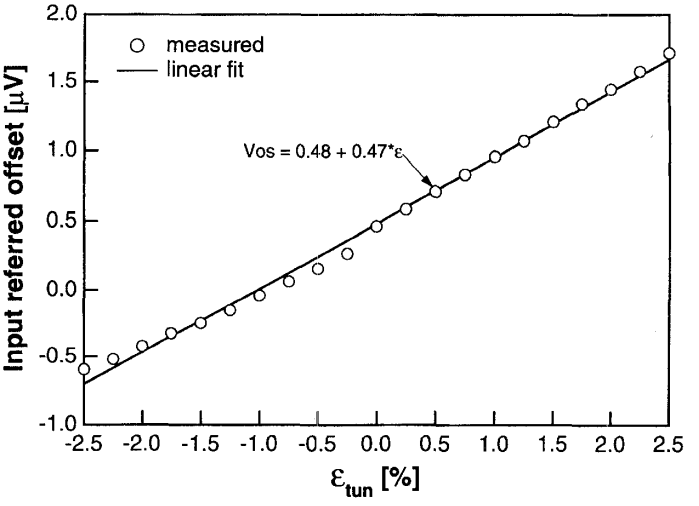

Fig. 55. Measured input referred offset versus tuning error.

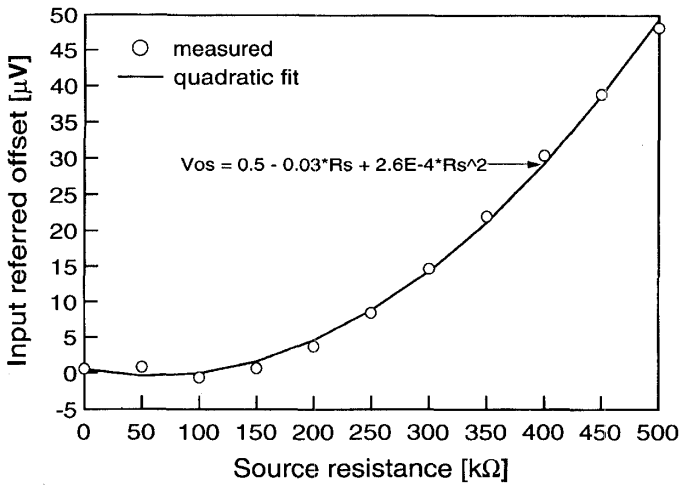

Fig. 56. Measured input referred offset versus source resistance.

VII. Conclusions

A detailed comparison of the relative advantages and disadvantages of the CHS technique versus CDS was given earlier [7], [8]. These are the main points.

1) CDS is inherently a sampled-data method; CHS is based on modulation rather than sampling, and hence can be used for continuous-time signals.
2) CDS reduces the low-frequency noise by highpass filtering; CHS translates it to some out-of-band frequency.
3) The output noise of a CDS stage is normally dominated by the undersampled wideband noise; in a continuous-time CHS stage the noise spectrum is not folded, and hence $1/f$ noise remains dominant in the baseband before the second modulation. After demodulation, white noise is folded into the baseband and replaces the $1/f$ noise. If the chopping frequency is much larger than the noise corner frequency, then the baseband white noise in the output is only very slightly larger than it was without CHS.
4) As shown earlier, CDS can also be used to enhance the effective gain of the op-amps used in the signal processing. A continuous-time CHS system, by contrast, causes the op-amp to amplify a higher-frequency signal, and hence its effective gain is usually reduced.

In conclusion, CDS is preferable in applications which inherently use sampled-data circuits (such as SC stages), so that the baseband noise behavior is not made worse by noise aliasing. Also, the dc offsets are eliminated, not just modulated to higher frequency, by CDS, which may improve the allowable signal swing. Finally, the gain-

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$$|H_n(f)|^2 = d^2\left\{\left[\frac{\sin\alpha}{\alpha} - \frac{\sin\beta}{\beta}\right]^2 + \left[\frac{1-\cos\alpha}{\alpha} - \frac{1-\cos\beta}{\beta}\right]^2\right\} \tag{50}$$

enhancing ability of CDS may be an important advantage in some applications. On the other hand, CHS is the method of choice if the system is a continuous-time one to start with, and if low baseband noise is an important requirement.

Appendix
Autozeroed Noise Analysis

The autozeroed voltage $v_{\mathrm{AZ}}(t)$ shown in Fig. 2 can be approximated by

$$v_{\mathrm{AZ}}(t) = \sum_{m=-\infty}^{+\infty} h(t - mT_s)[v_N(t) - v_N(mT_s)] \tag{46}$$

where it has been assumed that the RC time constant in the track mode is much smaller than the duration T_{AZ} of the AZ phase, i.e., that voltage $v_{\mathrm{AZ}}(t)$ instantaneously goes down to zero at the beginning of the AZ phase. Here $h(t)$ is a window function corresponding to the hold phase:

$$h(t) \equiv \begin{cases} 1, & \text{for } 0 \le t < T_h, \\ 0, & \text{otherwise.} \end{cases} \tag{47}$$

If $v_N(t)$ is assumed to be a stationary random process having a PSD $S_N(f)$, the PSD of the autozeroed voltage is given by

$$S_{\mathrm{AZ}}(f) \equiv \sum_{n=-\infty}^{+\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right) \tag{48}$$

which consists of replicas of the original spectrum shifted by multiples of the sampling frequency and multiplied by the squared magnitude of the corresponding band transfer function. These transfer functions can be evaluated by calculating the Fourier transform of $v_{\mathrm{AZ}}(t)$

$$H_n(f) = d[e^{-j\pi nd}\mathrm{sinc}\,(\pi nd) - e^{-j\pi\, dfT_s}\mathrm{sinc}\,(\pi\, dfT_s)] \tag{49}$$

where $d \equiv T_h/T_s$ is the duty cycle. The $|H_n(f)|^2$ functions are then readily obtained from (49) (see (50) at the top of the page) with $\alpha \equiv 2\pi\, dn$, $\beta \equiv 2\pi\, dfT_s$.

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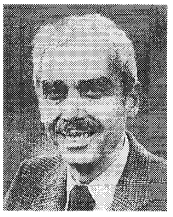

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