

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANALOG DEVICES, INC.,
Petitioner,

v.

NUMBER 14 B.V.,
Patent Owner.

IPR2025-00551
U.S. Patent 7,812,665

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT 7,812,665

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Ex. 1001	U.S. Patent No. 7,812,665 B2 to Eschauzier <i>et al.</i> (“the ’665 patent”)
Ex. 1002	Certified File History of the ’665 patent (“File History”)
Ex. 1003	Declaration of Dr. Ion Opris
Ex. 1004	Curriculum Vitae of Dr. Ion Opris
Ex. 1005	F. Krummenacher <i>et al.</i> , <i>A High-Performance Autozeroed CMOS Opamp with 50pV Offset</i> , 1997 IEEE International Solid-state Circuits Conference, 1997 (“ <i>Krum</i> ”)
Ex. 1006	U.S. Patent No. 6,130,632 to Opris (“ <i>OprisPat</i> ”)
Ex. 1007	U.S. Patent No. 7,642,846 to Yan (“ <i>Yan</i> ”)
Ex. 1008	U.S. Patent No. 6,486,806 to Munoz <i>et al.</i> (“ <i>Munoz</i> ”)
Ex. 1009	U.S. Patent No. 7,265,611 to Wang (“ <i>Wang</i> ”)
Ex. 1010	U.S. Patent No. 5,789,974 to Ferguson <i>et al.</i> (“ <i>Ferguson</i> ”)
Ex. 1011	Reserved
Ex. 1012	Reserved
Ex. 1013	M. Pastre <i>et al.</i> , <i>High-precision DAC Based on a Self-Calibrated Sub-Binary Radix Converter</i> , ISCAS 2004 (“ <i>Pastre</i> ”)
Ex. 1014	U.S. Patent No. 4,336,526 to Weir (“ <i>Weir</i> ”)
Ex. 1015	Reserved
Ex. 1016	Reserved
Ex. 1017	Reserved
Ex. 1018	“Optimal Resistor Ratio in the DAC with Low Precision Resistors – Statistical Approach,” Dragović-Ivanović <i>et al.</i> , Elektrotehnicki fakultet, University of Montenegro, 81000 Podgorica, Montenegro,

Exhibit	Description
	Yugoslavia (“ <i>Drago</i> ”)
Ex. 1019	U.S. Patent No. 4,465,996 (“ <i>Boyacigiller</i> ”)

MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner is a real party-in-interest. Maxim Integrated Products, Inc. is also a real party-in-interest. No other party had access to or control over the filing of this Petition and Petitioner did not file this Petition for the benefit of any other entity.

B. Related Matters (37 C.F.R. §42.8(b)(2))

The '665 Patent is involved in *Number 14 B.V. v. Analog Devices, Inc. and Maxim Integrated Products, Inc.*, 5:24-cv-02435-EJD (Apr. 24, 2024 NDCA). This case is not a patent infringement case.

C. Lead and Back-Up Counsel (37 C.F.R. §42.8(b)(3) and (4))

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Petitioner consents to electronic service at the email addresses listed above.

I. INTRODUCTION

Petitioner requests *inter partes* review and cancellation of claims 1-7, and 9 (the “Challenged Claims”) of U.S. Patent No. 7,812,665 (“the ’665 Patent”) (Ex. 1001).

II. TECHNOLOGY OF THE ’665 PATENT

A. Technological Overview

Amplifiers, and operational amplifiers (“opamp”) in particular, exhibit input offset voltages due to technological imperfections. Ex. 1007 1:35-40; Ex. 1003, ¶51. Input offset voltages (sometimes referred to as input referred offset voltage, input offset, voltage offsets, or offset), are contributed to by the mismatch between different components in a circuit among other factors. Ex. 1009, 1:18-21; Ex. 1003, ¶51. In precise applications, large offsets cannot be tolerated. Ex. 1009, 1:15-18; Ex. 1003, ¶52.

The total offset voltage is commonly conceptualized as a single fictitious voltage source at the input terminal of an amplifier. *E.g.*, Ex. 1009, Fig. 1; Ex. 1003, ¶52. The ’665 Patent itself acknowledges several prior art systems that have been implemented to resolve problems relating to offset voltages. Ex. 1001, 1:28-50, 2:22-55; *See also*, Ex. 1007, 1:40-44; Ex. 1003, ¶¶53-54.

In some instances, offset voltages are reduced by modifying or trimming each opamp during manufacturing to compensate for the then-measured offset voltage.

Ex. 1001, 1:28-36; Ex. 1003, ¶54. Trimming can be done either pre-package or post-package. Ex. 1001, 1:45-50; Ex. 1003, ¶54.

The '665 Patent identifies prior art approaches to post-package trimming that use power-on calibration. Ex. 1001, 2:22-24. One example of this system is *Krum* (Ex. 1005). Ex. 1001, 2:30-34; Ex. 1003, ¶54. This method used to cancel the offset is sometimes called auto-zeroing or offset calibration. Ex. 1005, 1; Ex. 1003, ¶54. Autozeroing may use volatile memory to store an offset compensation value determined each time the power supply is applied to the circuit. Ex. 1001, 2:34-39.

Prior art Figure 1 illustrates an applicant admitted prior art power-on calibration system:

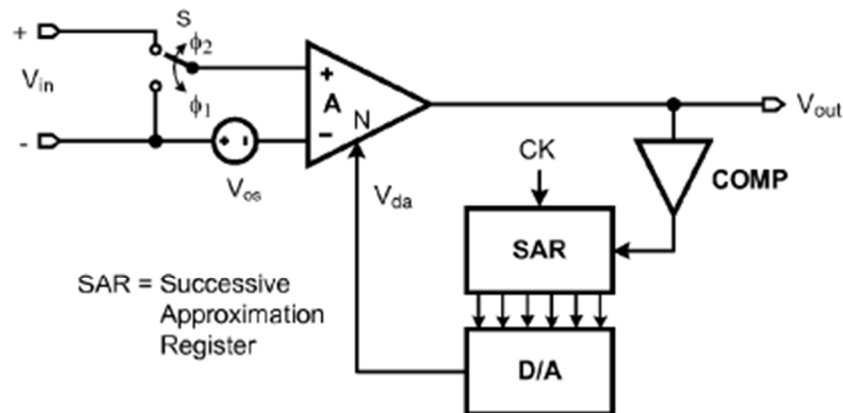


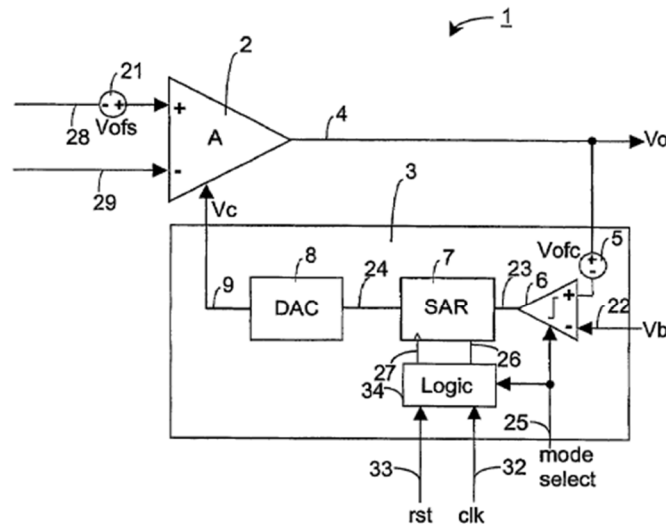
Fig. 1 (Prior Art)

Ex. 1001, Fig. 1, 2:41-42. In this prior art system, the offset voltage V_{os} of opamp A is canceled through use of a successive approximation register (“SAR”), Switch

S, comparator COMP, and digital to analog converter D/A which feeds the offset correction voltage V_{da} to the Opamp A. Ex. 1001, 2:44-48; Ex. 1003, ¶55.

When switch S is closed (shorting the inputs to the amplifier), V_{os} connects to both differential inputs of amplifier A. Ex. 1001, 2:58-60. Since V_{da} drives the offset compensation port N of amplifier A, it can be thought of as directly subtracting from V_{os} at the input of the amplifier, the difference of which resulting in error ϵ . Ex. 1001, 2:60-67; Ex. 1003, ¶56. At start up, the successive approximation register will have all bits set to 0. Ex. 1001, 3:9-10. Based on the error ϵ read at the comparator, the successive approximation register will iteratively select each bit starting at the most significant bit (MSB) and moving to the least significant bit (LSB) until each bit value is stored and until the error ϵ is minimized. Ex. 1001, 2:67-3:6, 3:10-24; Ex. 1003, ¶¶56-57.

Such systems were well-known in the prior art. For example, U.S. Patent No. 7,265,611 (Ex. 1009) (“*Wang*”) relied on in Ground 3, depicts self-zeroing circuitry that includes a comparator 6, a SAR 7, DAC which is used to compensate for the offset voltage of amplifier 2:



Ex. 1009, Fig. 3, 3:8-15; Ex. 1003, ¶78; *see also*, Ex. 1001, 2:22-34 (citing *Krum*).

One common difficulty in SAR systems is the strict matching requirements as slight changes in component values result in errors that can significantly decrease SAR accuracy. Ex. 1008, 2:24-40; Ex. 1014, 2:13-15; Ex. 1003, ¶58. One way to reduce the strict matching requirements is by designing a successive approximation algorithm so the ratio between a bit and the successive bit (e.g., the MSB and next most significant bit) is lower than two. *See generally*, Ex. 1008; Ex. 1014; Ex. 1003, ¶59. This ratio is called a *radix*. Ex. 1003, ¶59.

Employing SARs with a radix of less than two was well known in the art. For example, U.S. Patent No. 6,486,806 (Ex. 1008) (“*Munoz*”) describes “a system for adaptive auto-calibration... [which] includes a plurality of DAC elements having element values ratioed by radix<2[.]” Ex. 1008, 2:45-50. *Munoz* confirms the sole

purported novelty of the '665 Patent (a radix of less than 2) was previously well-known in the opamp field. Ex. 1003, ¶59.

B. The '665 Patent

The '665 Patent describes and claims an apparatus for power calibration (or auto-zeroing) of the input offset voltage of an amplifier. Ex. 1001, 7:30-35; cl. 1; Ex. 1003, ¶91. The sole distinction between claim 1 and the applicant admitted prior art of Figure 1 is the D/A converter having a radix less than two (notwithstanding the trivial “second switch” that connects the amplifier to the comparator during calibration):

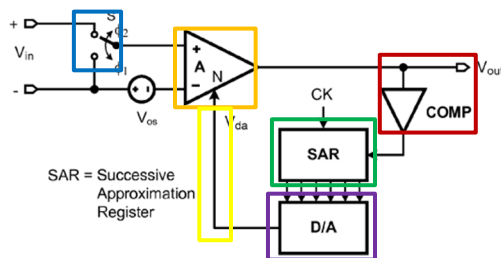


Fig. 1 (Prior Art)

1. An amplifier system having an amplifier system input 35 and an amplifier system output comprising:
 - a first amplifier;
 - a comparator;
 - a successive approximation register having an input coupled to an output of the comparator;
 - a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
 - a second switch for switching an output of the first amplifier from the amplifier system output to an input of the 45 comparator;
 - an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
 - the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;
 - an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

Ex. 1001 Fig. 1, Cl. 1¹; Ex. 1003, ¶91.

C. Prosecution History

The '665 Patent was filed Feb. 23, 2009 as Application No. 12/390,684. Ex.

¹ All color annotations in figures are provided by Petitioner.

1001, Title Page. Claims 1-12 were elected during prosecution and subsequently allowed. Ex. 1002, 212-213. The Examiner stated in the reasons for allowance that “the closest prior art of record, Leung et al (Fig. 1) does not disclose... the functional limitations of the second switch,” confirming the known radix values, as outlined herein. Ex. 1002, 213.

III. GROUNDS FOR STANDING (37 C.F.R. §42.8(B)(1))

Petitioner certifies (1) the '665 Patent is available for IPR; (2) Petitioner is not barred or estopped from requesting an IPR on the Grounds identified herein; and (3) Petitioner has not filed a complaint relating to the '665 Patent. This Petition is filed in accordance with 37 C.F.R. § 42.106(a).

IV. PAYMENT OF FEES (37 C.F.R. §§ 42.15)

Petitioner authorizes the USPTO to charge any required fees to Deposit Account 02-1818.

V. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art (“POSITA”) is a hypothetical person who is presumed to know the relevant prior art. *See Gnosis S.P.A et al. v. S. Ala. Med. Sci. Foundation*, Case IPR2013-00116, Paper 68 at 9, 37 (PTAB June 20, 2014). A POSITA has ordinary creativity, is not an automaton, and is capable of combining teachings of the prior art. *Id.* (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420-421 (2007)).

A POSITA with respect to the '665 patent would have possessed at least a bachelor's degree in electrical engineering or a closely related field and at least two years of experience in the design of analog integrated circuits. Ex. 1003, ¶¶48-50. Additional education could substitute for professional experience and vice versa. Ex. 1003, ¶50.

VI. CLAIM CONSTRUCTION

The Board construes claims using the standard of *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *CUPP Comput. AS v. Trend Micro Inc.*, 53 F.4th 1376, 1380 (Fed. Cir. 2022). According to this standard, claim terms receive their ordinary and customary meaning as would have been understood by one of ordinary skill in the art in light of the specification, prosecution history, and extrinsic evidence. *Phillips*, 415 F.3d at 1314-19. Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

A. “non-binary converter using a radix of less than 2 for at least the most significant bits” [claim 1]

This term should be construed as requiring the element ratio between bit N and bit (N-1), and the element ratio between bit (N-1) and bit (N-2), to each be lower than 2, where the converter has N bits, and where the MSB is bit N and the LSB is bit 1. Ex. 1003, ¶93.

The term *radix* is not defined in the '665 Patent specification. *See generally* Ex. 1001. While the concept of the radix is clear (*i.e.*, the ratio between two elements associated with consecutive bits), the '665 Patent uses the term as referring to one bit, as opposed to two bits. Ex. 1001 Cls. 1, 3; Ex. 1003, ¶94.

While claim 3 recites “the radix for the least significant bit is 2[,]” the radix of claim 1 uses bits (plural), eliminating any potential claim differentiation issues with this construction. Ex. 1003, ¶94.

To be consistent with the patent language, the radix for an arbitrary bit P (not the MSB) is understood to refer to the ratio between the element (P+1) and the element P. Ex. 1003, ¶95.

A. “coupled”, “being coupled” [claims 1, 5, 6, 7, 8]

The '665 Patent uses the term “coupled” only in the claims, and not in the specification. A POSITA would understand that “coupled” or “being coupled” should be understood to mean connecting directly or indirectly through one or more intervening devices. Ex. 1003, ¶96.

VII. STATEMENT OF PRECISE RELIEF REQUESTED

Petitioner requests institution of an IPR and cancellation of the Challenged Claims on the Grounds outlined below.

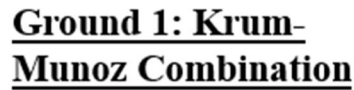
Ground	Challenged Claims	Basis	Prior Art
1	1-4, 9	§ 103	F. Krummenacher <i>et al.</i> , <i>A High-Performance Autozeroed CMOS Opamp with 50pV Offset</i> , 1997 IEEE International Solid-state Circuits Conference, 1997 (“ <i>Krum</i> ”) and U.S. Patent No. 6,486,806 (“ <i>Munoz</i> ”)
2	1, 5-7	§ 103	Krum, Munoz, and U.S. Patent No. 7,642,846 (“ <i>Yan</i> ”)
3	5	§ 103	U.S. Patent No. 7,265,611 (“ <i>Wang</i> ”), U.S. Patent No. 4,336,526 (“ <i>Weir</i> ”), and U.S. Patent No. 5,789,974 (“ <i>Ferguson</i> ”)

Petitioner provides the declaration of Dr. Ion Opris (Ex. 1003), an expert in the field of the '665 Patent and the prior art, in support of these Grounds. Ex. 1003, ¶¶7-21, 48-49; Ex. 1004; *see* Ex. 1006.

VIII. GROUND 1: *KRUM* IN VIEW OF *MUNOZ* RENDERS OBVIOUS CLAIMS 1-4, 9

A. Overview of Ground 1

Ground 1 combines the opamp with offset autozeroing of *Krum*, which itself includes a DAC, with the teachings of *Munoz*. In view of these two references, a POSITA would have been motivated to replace the DAC of *Krum* with the DAC of *Munoz*, which has a radix of less than 2:



Krum discloses a CMOS opamp with offset compensation capabilities. Ex. 1003, ¶98. *Krum*'s system is similar in structure and functionality with the system described in the '665 Patent, although it lacks the specifically claimed radix of claim 1. Ex. 1003, ¶98.

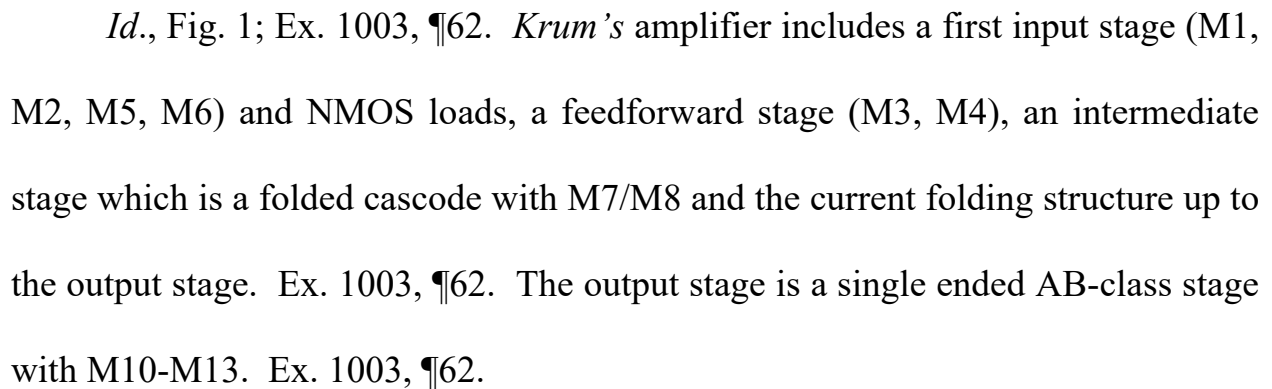
1. Krum

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Patent was filed, confirming it is prior art to the '665 Patent. Ex. 1001, 2:26-33; Ex. 1003, ¶¶60. Indeed, a copy of Ex. 1005 was provided with the IDS submitted on the same day the application leading to the '665 Patent was filed. Ex. 1002, 29, 83, 128-129. This proves that at least the POSITAs at Number 14 B.V. had access to *Krum* as of the filing of the '665 Patent. Moreover, *Krum* itself, as an IEEE article, can serve as prior art as of its copyright date, 1997. *Ericsson Inc. v. Intellectual Ventures I LLC*, IPR2014-00527, Paper 41 (PTAB May 18, 2015) ("IEEE is a well-known, reputable compiler and publisher of scientific and technical publications, and we take Official Notice that members in the scientific and technical communities who both publish and engage in research rely on the information published on the copyright line of IEEE publications.").

Krum is a proceeding condensate of a presentation at the International Solid State Circuits Conference in 1997 and is dated February 8, 1997, suggesting it is publicly available prior art to the '665 Patent. Ex. 1005, 2; Ex. 1003, ¶¶60-61.

Krum describes an opamp with an input offset voltage which needs to be auto-calibrated (or auto-zeroed) with the corresponding autozeroing circuitry. Ex. 1005, 1. The opamp itself has a traditional three-stage structure, including an input stage, feedforward stage, intermediate stage, and an output stage as annotated below:



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is auto-zeroed. Ex. 1005, 1.

In autozeroing, the output stage signal is passed through a comparator (M20-M23), a low-pass filter (a refinement used to reduce the effect of high-frequency noise), and a Schmitt trigger (a comparator with hysteresis which extracts logic signals). Ex. 1005, 1; Ex. 1003, ¶64. Finally, the resulting signal is fed into a SAR, which in turn controls the CALDAC. Ex. 1005, 1. The CALDAC injects the autozeroing signal into the opamp, canceling any input offset and completing the autozeroing. Ex. 1003, ¶65.

2. Munoz

Munoz was filed September 9, 1999 and issued November 26, 2002, so it is prior art under 35 U.S.C. § 102(b). Ex. 1008, Title; Ex. 1003, ¶66. *Munoz* is a patent describing a system to be used during successive approximation for calibrating an analog-digital converter. Ex. 1008, Abstract.

Munoz acknowledges a “binary non-overlap problem[.]” Ex. 1008, 1:66-2:4. This refers to when a most significant bit (MSB) is erroneous due to mismatch, a radix of 2 cannot be compensated for because the MSB has a higher value than the cumulative value of all remaining bits, leading to an issue outputting the proper signal (e.g., occurrence of a gap, or a non-overlap in the output signal). Ex. 1008, 2:24-42; Ex. 1003, ¶67. *Munoz* recognized that, by implementing a radix of less than 2, redundancy is introduced to overcome the binary non-overlap problem. Ex.

1008, 2:45-50.

In Fig. 2, *Munoz* shows a “successive approximation converter”:

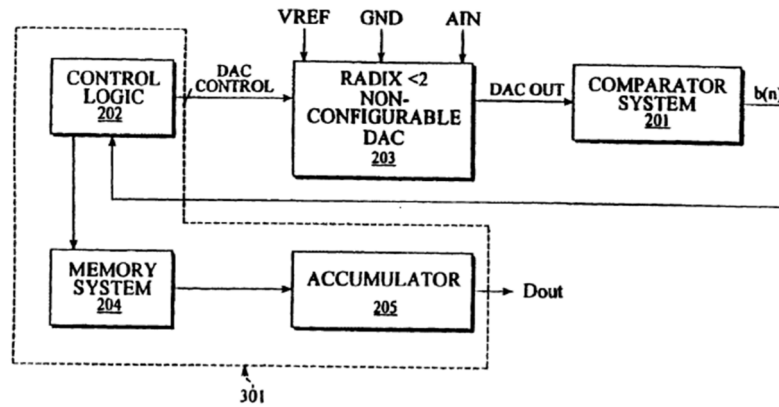
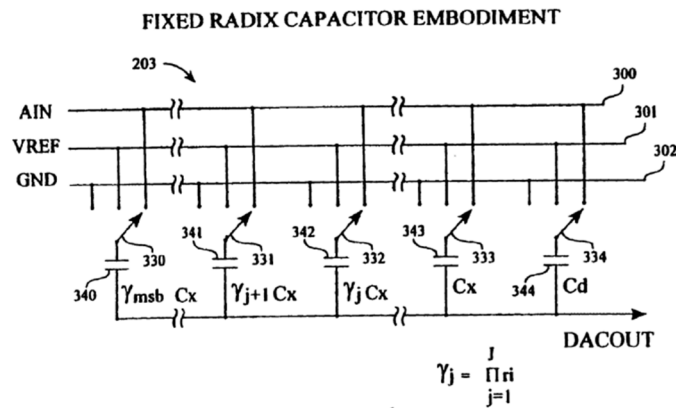


Fig. 2

Ex. 1008, Fig. 2, 6:16-24; Ex. 1003, ¶68.

DAC 203, having a radix of less than 2, is described in more detail in Figs. 3A and 3B. Ex. 1003, ¶¶69-73. Figure 3A depicts a charge redistribution DAC (CRDAC) which includes input voltage (AIN) lead 300, reference voltage (VREF) lead 301, and ground (GND) lead 302, a plurality of switches 330-334 and capacitors 340-344:

*Fig. 3A*

Ex. 1008, Fig. 3A, 6:45-60; Ex. 1003, ¶¶69-70. The capacitors can also be replaced by other charge carrying elements like resistors. Ex. 1008, 6:67-7:3, 9:18-19. Capacitors 340-344 are designed to have a radix of less-than-two. Ex. 1008, 6:58-60, 7:3-13, 17:43-45; Ex. 1003, ¶¶70, 73.

Munoz also teaches that the CRDAC can be implemented with a plurality of switches 330-334 between banks of capacitor sets 420-424 with individual capacitors 431-438, 441-445, 451-453, 461-462, 424 having approximately the same capacitance values, taken in parallel:

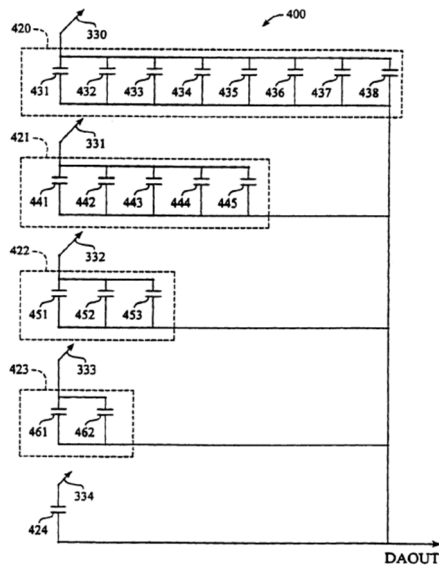


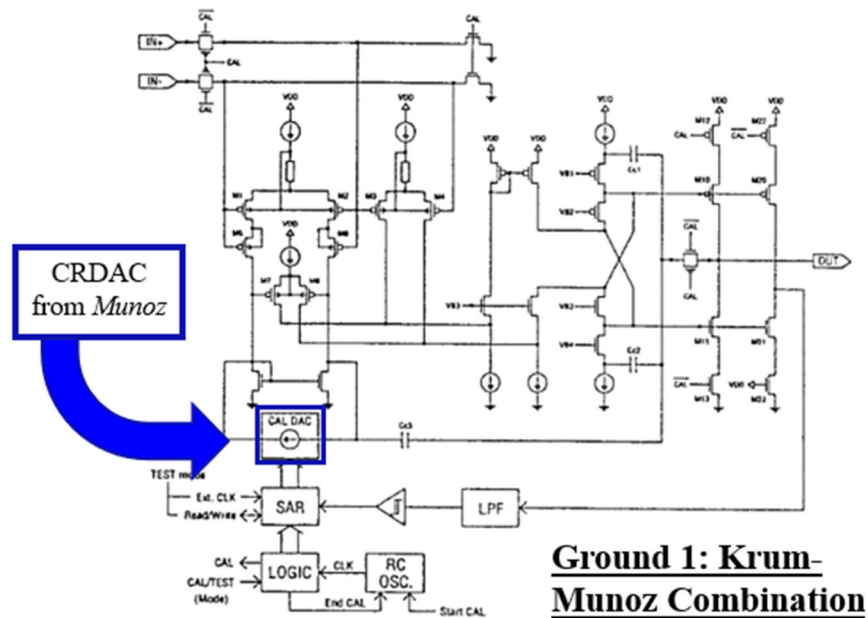
Fig. 3B

Ex. 1008, Fig. 3B, 7:30-54; Ex. 1003, ¶¶71-72. By using capacitors with similar capacitances, the CRDAC in Fig. 3B achieves relative capacitances of the capacitance banks 420, 421, 422, 423, 424 of 8, 5, 3, and 2 respectively. Ex. 1008, 7:54-60; Ex. 1003, ¶72. Thus, the radices are $8/5$ for elements 420 and 421; $5/3$ for elements 421 and 422; $3/2$ for elements 422 and 423; and $2/1$ for elements 423 and 424. Ex. 1003, ¶72.

Munoz further teaches that “instead of capacitors, other charge carrying components such as resistors can be substituted as a separate embodiment according to the present invention”. Ex. 1008, 9:18-19. Instead of capacitor banks, *Munoz* explains that resistors or other charge carrying components may be used. Ex. 1008, 6:67-7:3, 9:18-19; Ex. 1003, ¶72.

B. Motivation to Combine

A POSITA would have been motivated to combine the teachings of *Krum* and *Munoz*, and modify *Krum*'s binary-weighted CALDAC to be a DAC with radix of less than 2, according to the teachings of *Munoz*:



Ex. 1003, ¶¶97, 100.

Both *Krum* and *Munoz* are analogous art to the '665 Patent. A POSITA who was interested in researching stringent matching requirements found in optical amplifier systems would look to systems like *Munoz* which provide increased redundancy in successive approximation systems and accordingly, decrease the matching parameters in optical amplifier systems. Ex. 1008, 2:24-42; Ex. 1003, ¶101. Likewise, a POSITA interested in improving amplifiers with offset compensation circuitry would look to other amplifier systems which rely on offset

compensation circuitry like *Krum*. Ex. 1001, 2:22-39; Ex. 1005, 1; Ex. 1003, ¶101.

A POSITA would recognize and be motivated to improve *Krum*'s system with *Munoz*'s teachings. Ex. 1003, ¶102. A POSITA would be motivated to combine the two references because (1) *Krum* requires implementation of a monotonic DAC, with little explanation of said DAC, and *Munoz* provides a monotonic DAC; and (2) *Munoz*'s DAC would improve *Krum*'s system by providing redundancy and enabling recovery from noise induced errors. Ex. 1003, ¶103.

Krum's system utilizes a CALDAC to perform offset calibration. Ex. 1005, 1; Ex. 1003, ¶104. *Krum* does not provide significant details regarding the CALDAC besides that “[t]he linearity of the CALDAC, however, is not important as long as its monotonicity is guaranteed.” Ex. 1005, 1; Ex. 1003, ¶104.

A POSITA who wanted to implement *Krum*'s system would look to compatible systems that also provided monotonic DACs. Ex. 1003, ¶104. Indeed, it is understood that monotonicity can aid in the precision of the DAC in certain applications. Ex. 1013, 1.

Munoz provides a monotonic DAC. Ex. 1003, ¶105. In fact, *Munoz* provides a system that “ensures monotonicity in successive approximation and avoids erroneous, noise induced inclusion of a too-large balancing capacitor [or resistors] in the final set of balancing capacitors [or resistor].” Ex. 1008, 9:15-19; Ex. 1003, ¶105. *Munoz*'s system also describes a companion bit and successive radix scaled

components to monotonically approach a sampled voltage level. Ex. 1008, 8:55-58; Ex. 1003, ¶105. Indeed, *Munoz*'s companion bit "provides an envelope or margin which prevents noise induced over approximation of sampled values" which "promotes monotonicity and convergence to the approximated value without discontinuance or gaps in resolution." Ex. 1008, 16:53-58. As *Munoz*'s DAC "remains monotonic and symmetrically noise tolerant during decision making incident to successive approximation[,]" a POSITA would be motivated to implement it with *Krum*. Ex. 1008, 17:45-48; Ex. 1003, ¶107.

A POSITA would also be motivated to improve *Krum* with *Munoz*'s teachings of a radix of less than two, which provides redundancy in DACs. Ex. 1003, ¶108. *Munoz*'s DAC provides a designed redundancy that allows *Munoz*'s system to accommodate noise induced erroneous bits. Ex. 1003, ¶111. *Munoz*'s DAC provides alternative expressions (or redundant expressions) in the DAC to approximate particular values in case of erroneous bit decisions. Ex. 1008, 5:67-6:2, 7:67-8:5; Ex. 1003, ¶109.

In a DAC "with a radix 2 series, there is no redundancy which permits alternative expressions of particular voltage or capacitance levels" leading to "the binary non-overlap problem" Ex. 1008, 1:66-2:4, 2:40-42; Ex. 1003, ¶109. By using a radix-less-than two array, the DAC can compensate for erroneous bits that occur during the calibration or SAR process due to noise or some other mechanism. Ex.

1008, 8:5-14. Indeed, a radix of less than two avoids gaps that otherwise occur in a DAC output with a radix of two. Ex. 1008, 5:15-21, 7:67-8:13; Ex. 1003, ¶110.

A POSITA would be motivated to implement a system that addresses the well-known problem of gaps in a DAC output. Ex. 1013, 1 (“This important feature allows guaranteeing that the converter will have no missing code, even when low-precision components are used.”); Ex. 1018, 1 (“In this way, we can guarantee the smallest possible gaps in input/output characteristics”); Ex. 1019, 2:10-15 (“If a conventional binary weighted DAC were utilized, gaps might appear in the output range of the DAC, with the result that certain desired correction analog output could not be generated. The use of a non-binary weighting overcomes this problem.”); Ex. 1003, ¶112. A radix of less than two would also allow for use of DAC elements with greater mismatches while still avoiding large gaps in the DAC output range. Ex. 1013, 1; Ex. 1003, ¶113.

A POSITA would modify *Krum* with the teaching of *Munoz* using routine engineering with a reasonable expectation of success. Ex. 1003, ¶114. Indeed, *Munoz* notes that a control logic circuit interfaces with a DAC to provide control signals including SAR control signals and configuration control signals (like in *Krum*). Ex. 1005, 1; Ex. 1008, Fig. 1A, 4:58-60; Ex. 1003, ¶¶114-115. Additionally, *Munoz*’s DAC is described in relation to all types of DACs and could be used to replace *Krum*’s current mode DAC. Ex. 1005, 1; Ex. 1008, 6:67-7:3; Ex. 1003, ¶116.

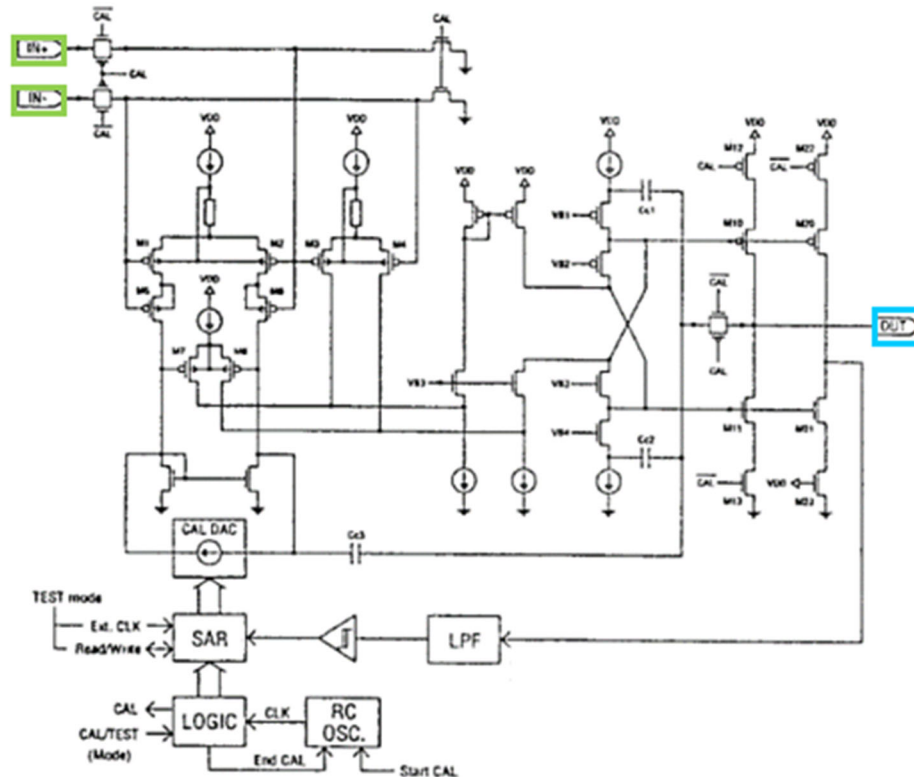
Accordingly, a POSITA would be motivated and capable of achieving the described combination. Ex. 1003, ¶117.

C. Independent Claim 1

The '665 Patent makes use of a known amplifier with power on calibration. Ex. 1001, Fig. 1, 2:40-41. Such a system, including “a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator[,]” is disclosed in *Krum*. Further, *Munoz* describes use of a DAC “with a radix of less than 2 for at least the most significant bits[.]” Accordingly, the *Krum-Munoz* combination renders Claim 1 obvious.

**1. [1pre] An amplifier system having an amplifier system
input and an amplifier system output comprising:**

To the extent it is limiting, the *Krum-Munoz* combination teaches an amplifier system having an amplifier system input and an amplifier system output. Ex. 1003, ¶118. For example, *Krum* discloses an amplifier circuit with two inputs (IN+ and IN-) (in green) and an output (OUT) (in blue):

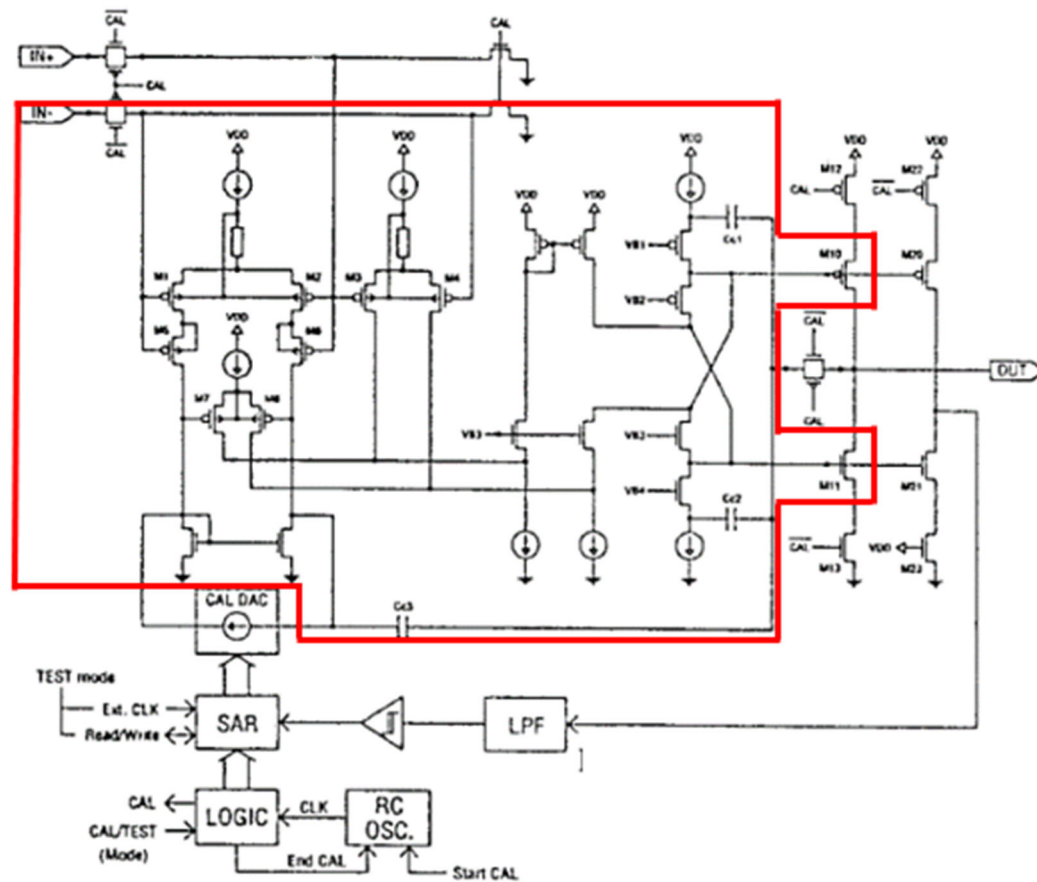


Ex. 1005, Fig. 1; Ex. 1003, ¶118.

2. [1a] a first amplifier;

The *Krum-Munoz* combination renders this limitation obvious. Ex. 1003,

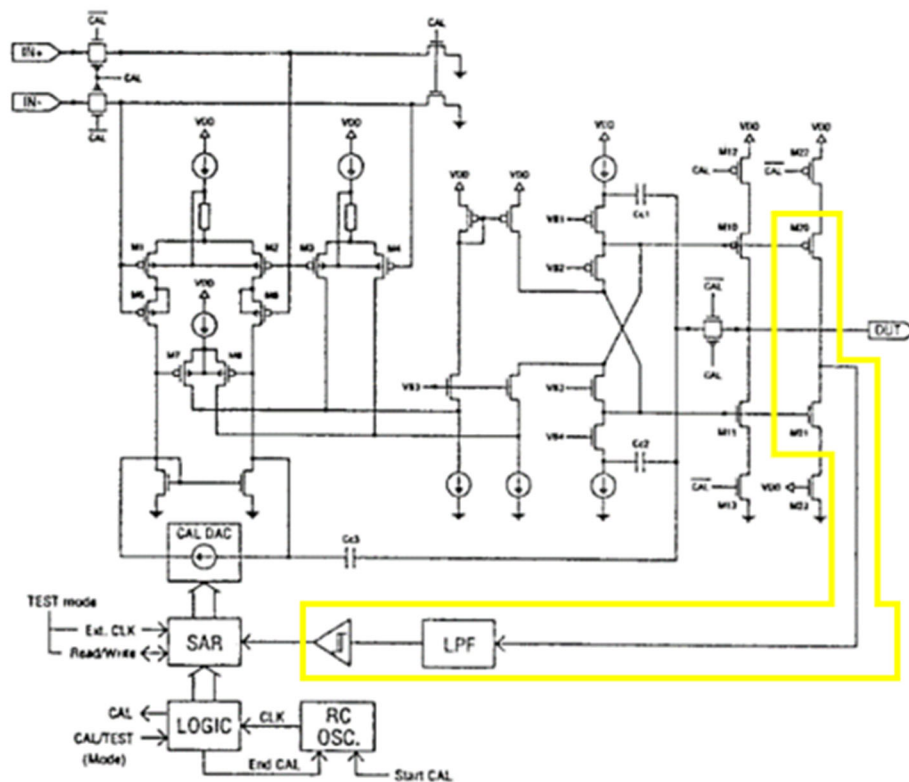
¶119. *Krum* discloses an amplifier, in red below:



Ex. 1005, Fig. 1; Ex. 1003, ¶119. *Krum*'s amplifier, in the form of an opamp, is confirmed in its title: "A High-Performance Autozeroed CMOS **Opamp** with 50µV offset." Ex. 1005, Title; Ex. 1003, ¶120. Accordingly, a POSITA would find that the *Krum-Munoz* combination discloses an amplifier.

3. [1b] a comparator;

The *Krum-Munoz* combination renders this limitation obvious. Ex. 1003, ¶121. *Krum* discloses a comparator system formed by M20, M21, the LPF, and the Schmitt trigger as depicted in yellow below:

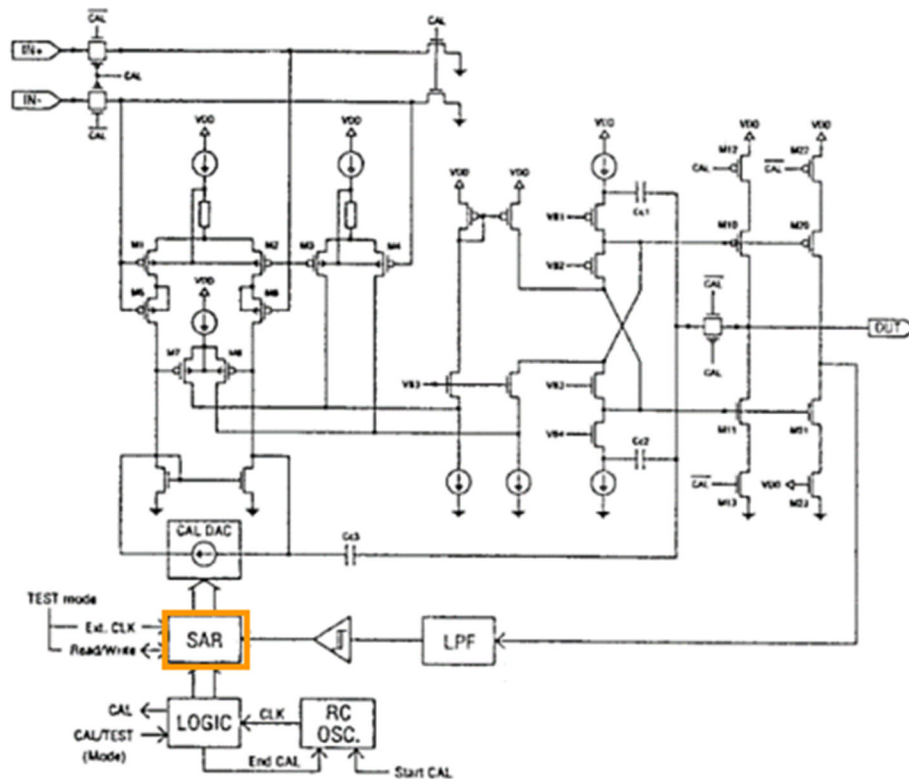


Ex. 1005, 1 (“transistors M20 & M21... are used to provide the amplifier output signal for the calibration circuit.”), Fig. 1; Ex. 1003, ¶122. The transistors M20 and M21 provide replica outputs of the transistors M10 and M11. Ex. 1003, ¶123. *Krum* teaches that the LPF’s role is only to eliminate the effect of “high-frequency noise”, and thus plays no role in the autozeroing scheme itself. Ex. 1005, 1. Further, a POSITA would know that a Schmitt trigger, such as that in *Krum*, is a comparator with hysteresis. Ex. 1003, ¶123.

4. [1c] a successive approximation register having an input coupled to an output of the comparator;

The *Krum-Munoz* combination renders this limitation obvious. Ex. 1003,

¶124. *Krum* discloses a successive approximation register depicted below in orange:



Ex. 1005, Fig. 1; Ex. 1003, ¶125. *Krum* teaches that a (SAR) is used for autozeroing.

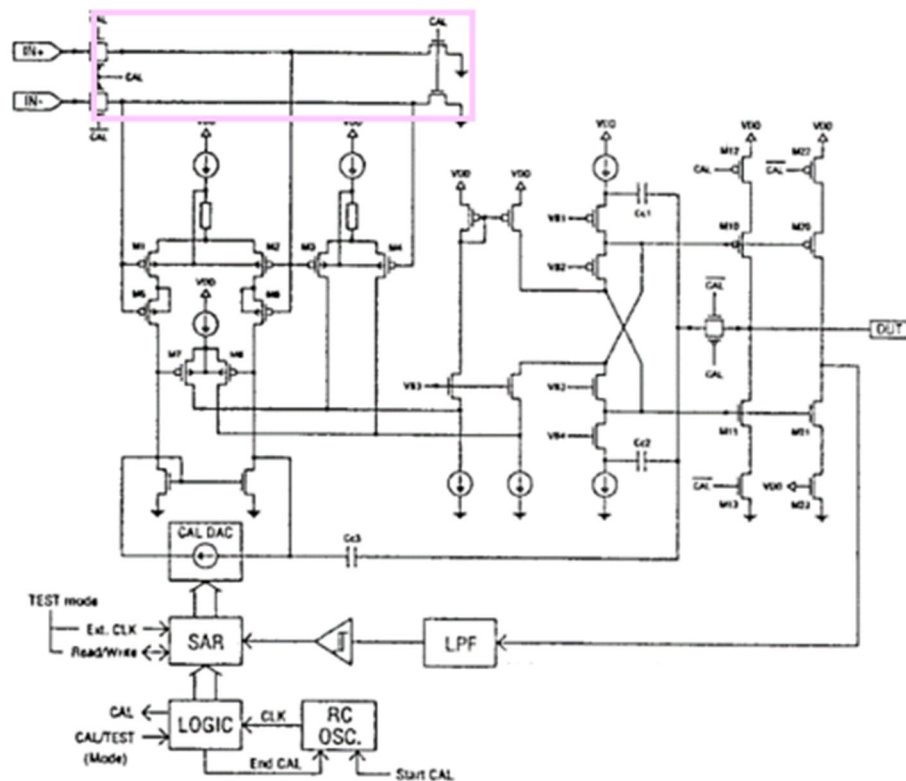
Ex. 1005, 1. *Krum*'s SAR input is also coupled to a comparator. For example, Fig. 1 shows the output of the Schmitt trigger (the comparator system outlined in yellow *Supra* Section VIII.C.3) is connected to the SAR. Ex. 1005, 1; Ex. 1003, ¶126.

5. [1d] a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

The *Krum-Munoz* combination teaches this limitation. Ex. 1003, ¶127. The '665 Patent notes that “the word switch as used herein and in the claims is used in

the general sense and includes single or **multiple** switches[.]” Ex. 1001, 10:40-42. The multiple switches would be “operated substantially simultaneously[.]” Ex. 1001, 10:42-45.

Krum teaches that “[d]uring autocalibration, when CAL=1, the opamp is removed from the signal path. Both inputs are tied to GND[.]” Ex. 1005, 1. *Krum* ties both inputs to GND using a switch, comprised of two NMOS transistors and two pass gates operated simultaneously, as depicted below in pink:



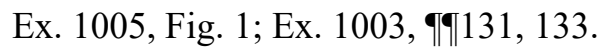
Ex. 1005, Fig. 1; Ex. 1003, ¶128.

The depicted first switch system operates as two NMOS transistors as

claimed, switching the gate of M1 (an input of the first amplifier) from being coupled to system input IN- to being shorted to the gate of M2. Ex. 1003, ¶129.

6. [1e] a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator,

The *Krum-Munoz* combination renders this limitation obvious. Ex. 1003, ¶130. During prosecution, the lack of a second switch was specifically identified as a reason for allowance. Ex. 1002, 213. However, *Krum* teaches that “during autocalibration[,]” “the opamp is removed from the signal path” and “transistors MI0 and M11 are disconnected from their respective supplies.” Ex. 1005, 1. “The output is thus floating[.]” *Id.* The claimed “second switch” is comprised of transistors M12, M13, M22, and M23 as depicted below in **green**:

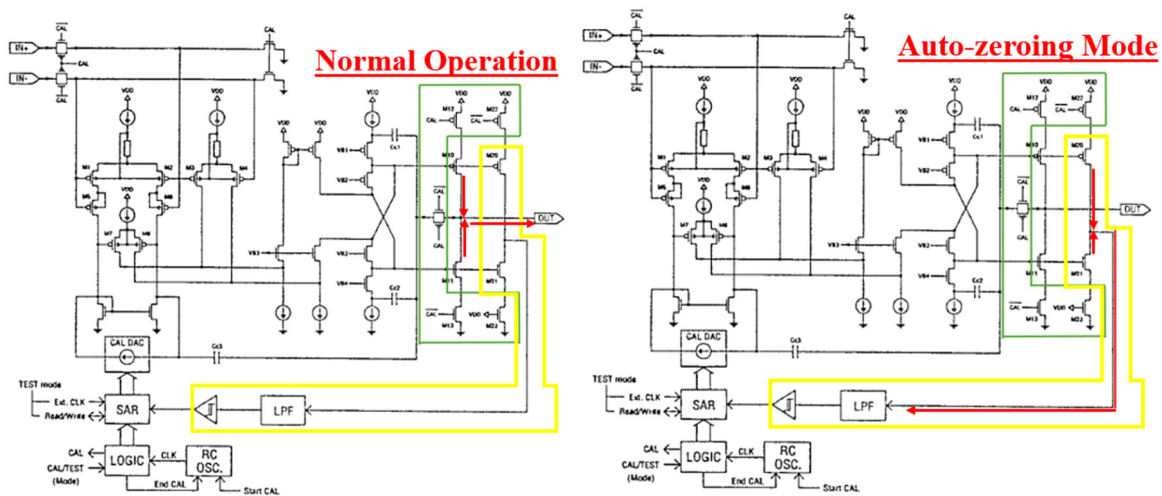


The transistors M12 and M13 enable and disable the output from transistors M10 and M11, and transistors M22 and M23² enable and disable the (replica) output from transistors M20 and M21. Ex. 1003, ¶134. So, transistors M12 and M13 effectively disconnect the amplifier output OUT from the amplifier output stage (transistors M10/M11) and transistors M22 and M23 couple the replica output stage (transistors M20/21) to the LPF input, which is part of the comparator system. Ex.

² A POSITA would appreciate the connection between M23 and VDD in Fig. 1 of *Krum* is a typographical error in Fig. 1, and M23 should instead be connected to CAL. Ex. 1003, ¶132.

1003, ¶135.

The communications path of the output of the second switch system is shown below for both the normal operation and the autozeroing mode:

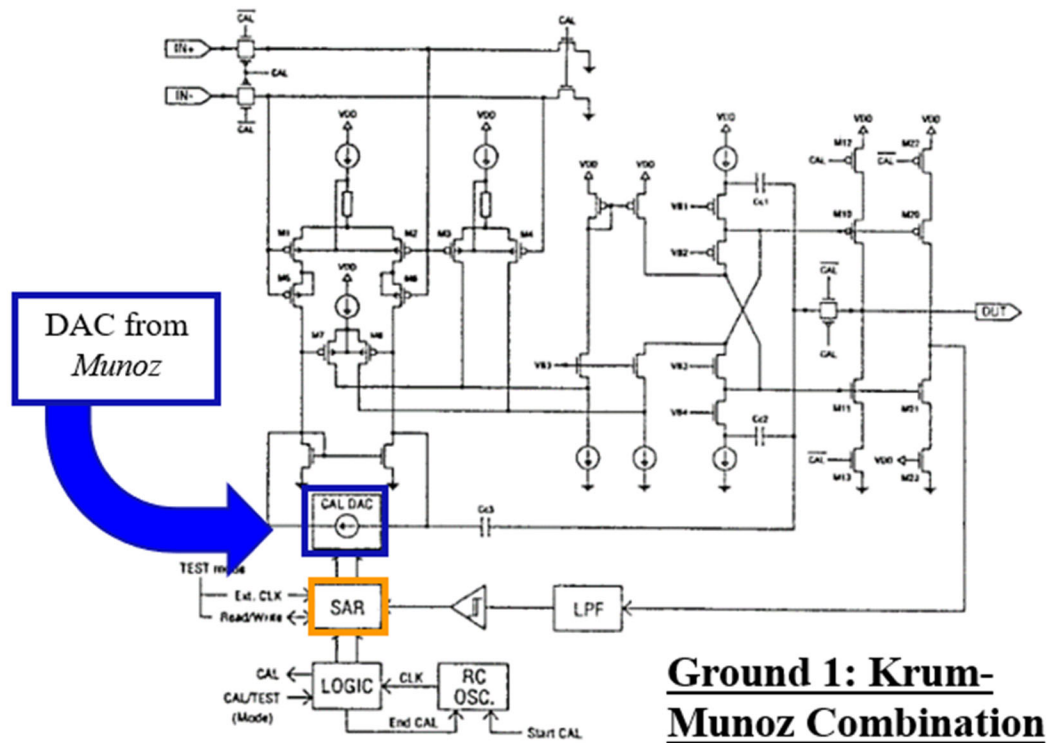


Ex. 1003, ¶136. The red arrows show the coupling of an amplifier output via the second switch system (green): to the system output; or to the comparator input. Ex. 1003, ¶137. Accordingly, the *Krum-Munoz* combination depicts a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator.

**7. [1f] an output of the successive approximation register
being coupled to an N bit digital to analog (D/A) converter;**

The *Krum-Munoz* combination teaches this limitation. Ex. 1003, ¶138. As described *supra* Section VIII.C.4, the combination includes a SAR. Indeed, the combination includes the DAC from *Munoz* shown in blue which is connected to the

SAR in orange:



Ex. 1005, Fig. 1; Ex. 1003, ¶139. The DAC of *Munoz* is a digital to analog converter.

Ex. 1008, 6:45-51. *Munoz*'s DAC is also a n-bit DAC because it is configured to convert an n-bit word. Ex. 1003, ¶143; Ex. 1008, 8:36-41, Fig. 4.

By implementing *Munoz*'s DAC with its radix of less than 2, *Krum*'s system is improved to account for erroneously kept bits. Ex. 1008 2:32-40, 7:67-8:5; Ex. 1013, 1; Ex. 1003, ¶¶140-141. This implementation also reduces the strict matching requirements of the DAC. Ex. 1013, 1; Ex. 1003, ¶142.

Therefore, the *Krum-Munoz* combination discloses this claim limitation.

8. [1g] the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

The *Krum-Munoz* combination teaches this limitation. *Munoz* describes a DAC that has a radix of less than two:

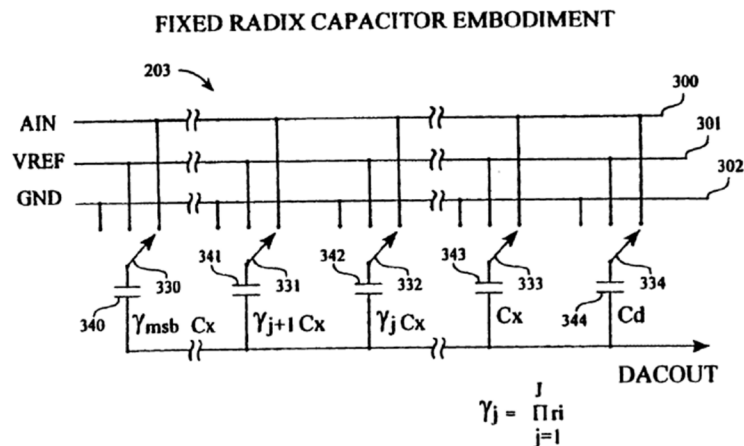


Fig. 3A

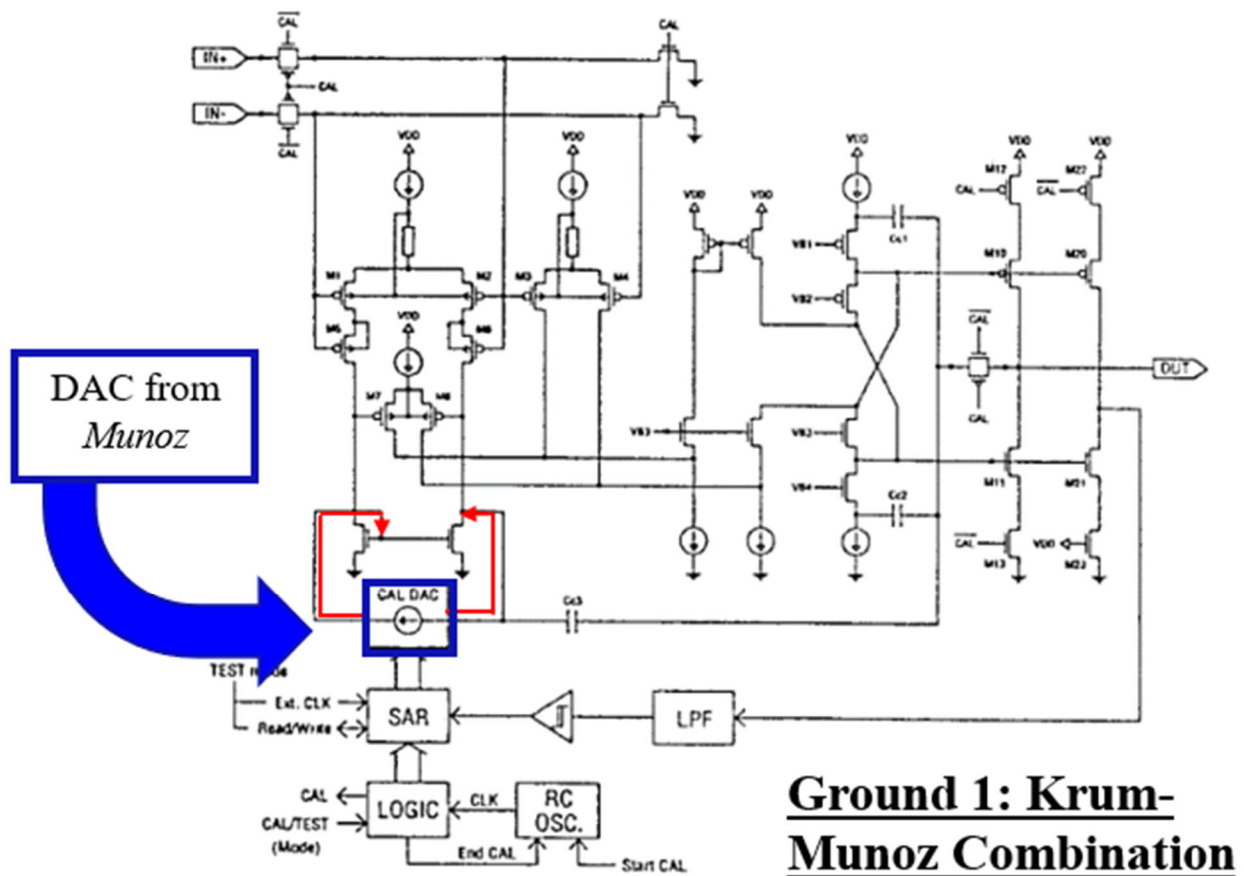
Ex. 1008, 6:45-48, Fig. 3A. A radix of less than two is achieved through design of a bank of capacitors or resistors. Ex. 1003, ¶145; Ex. 1008, 6:64-7:3.

Each capacitor is used for approximation in the course of the SAR calibration process. Ex. 1003, ¶146; *See* Ex. 1008, 7:3-13. The radix values associated with bits are calculated based on the ratio between capacitance of the associated subsequent capacitor. Ex. 1003, ¶146; *See* Ex. 1008, 7:16-20. Indeed, the value of respective capacitors γ_j , is given by the formula $\gamma_j = \prod_{i=1}^J r_i$ where r_i is the radix value. Ex. 1008, 7:3-10. *Munoz* teaches that the radix of the most significant bit is between 1 and 2 for each bit. Ex. 1008, 7:10-11.

Munoz further teaches that “instead of capacitors, other charge carrying components such as resistors can be substituted as a separate embodiment according to the present invention.” Ex. 1008, 6:67-7:3, 9:18-19; Ex. 1003, ¶147. Use of resistors rather than capacitors is necessary to ensure that the DAC outputs a continuous time level. Ex. 1003, ¶147. Thus, *Krum*’s CALDAC modified according to the teachings of *Munoz*’ Fig. 3A, and implemented with resistors, is the claimed “D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits.” *See*, Ex. 1003, ¶146.

**9. [1h] an output of the D/A converter being coupled to the
first amplifier to control the input offset of the first amplifier.**

The *Krum-Munoz* combination teaches this limitation. Ex. 1003, ¶148. For offset cancellation, the left output of *Krum*’s CALDAC is coupled to both gates of the bottom NMOS transistors as depicted by the red arrows:



Ex. 1005, Fig. 1; Ex. 1003, ¶149. The DAC then sends signals to compensate for the input offset of the amplifier. Ex. 1005, 1; Ex. 1003, ¶150.

D. Claim 2

1. The amplifier system of claim 1 wherein the radix is approximately 1.9.

The *Krum-Munoz* combination renders this limitation obvious. Ex. 1003, ¶151. For example, as described *supra* Section VIII.C.8, the radix values of bits are provided by the ratio of the capacitance between subsequent capacitor banks. Ex. 1008, 7:57-8:13. *Munoz* expressly teaches that a radix value of 1.9 is possible, with

the system remaining monotonic. Ex. 1008, 17:43-48; Ex. 1003, ¶¶152-153.

E. Claim 3

- 1. The amplifier system of claim 2 wherein the radix for the least significant bit is 2.**

The *Krum-Munoz* combination renders this limitation obvious. Ex. 1003, ¶154. The *Krum-Munoz* combination discloses wherein the radix of the least significant bit (LSB) is 2. Fig. 3B describes a floating radix charge redistribution system 400, which can be used in a CRDAC with a radix of less than two:

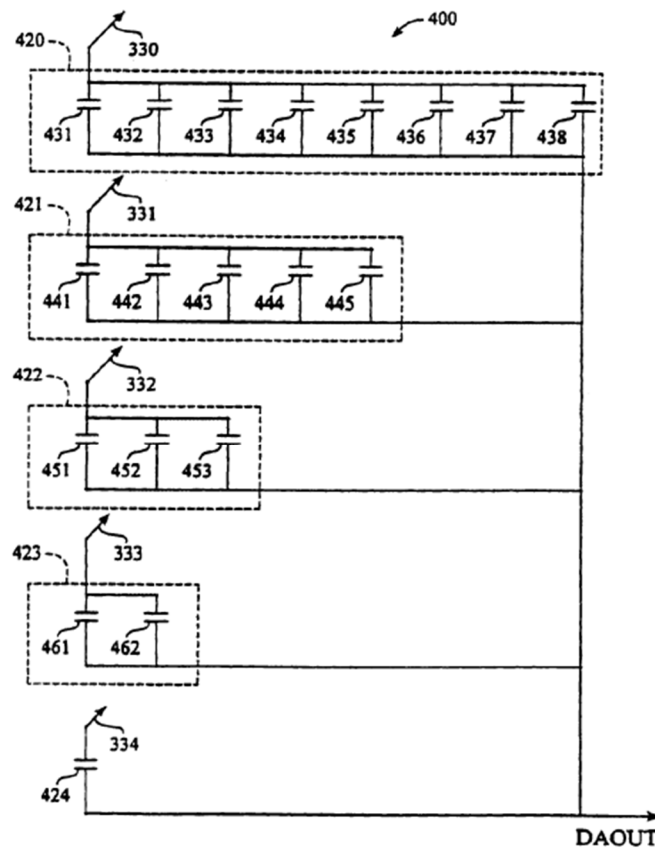


Fig. 3B

Ex. 1003, ¶155; Ex. 1008, Fig. 3B, 7:27-34.

The CRDAC system includes a plurality of switches 330-334 between sets or banks 420-424 of capacitors 431-438, 441-445, 451-453, 461-462, 424. Ex. 1008, 7:30-34, 7:49-53. Each of these groupings of capacitors has a unit capacitance value. Ex. 1008, 7:53-57. Specifically, the DAC is taught to have bits with radix of less than two. Ex. 1008, 7:35-40 (“According to one embodiment of the present invention, capacitors 420-424 are a step-wise floating radix redundant array of capacitors. In other words, the value relationship between successive components (e.g., capacitors) may still be radix-less-than two, but it will not necessarily be the same radix value for particular selected pairs of components.”); Ex. 1003, ¶156. The radix for the most significant bit (MSB) is equivalent to the ratio of the capacitance between bank 420 and bank 421, 1.6. Similarly, for the next MSB, the value is $5/3$, or approximately 1.7 due to the ratio between bank 421 and 422.

Fig. 3B includes a LSB where the radix is 2. As the radix is determined by the ratio between successive capacitor pairs (Ex. 1008, 7:62-66), the radix of the LSB will be given by the ratio of capacitances between bank 423 and 424, which is 2 (or 2:1). Ex. 1003, ¶156. Accordingly, the least significant bit having a radix of 2 is taught by the *Krum-Munoz* combination.

F. Claim 4

- 1. The amplifier system of claim 1 wherein the D/A converter further comprises one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits.**

The *Krum-Munoz* combination renders this limitation obvious. Ex. 1003, ¶157. *Munoz* discloses one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits. As described *supra* Section VIII.E.1, the radix of the least significant bit is two.

In Fig. 3B, five banks of capacitors are shown, 420, 421, 422, 423, and 424:

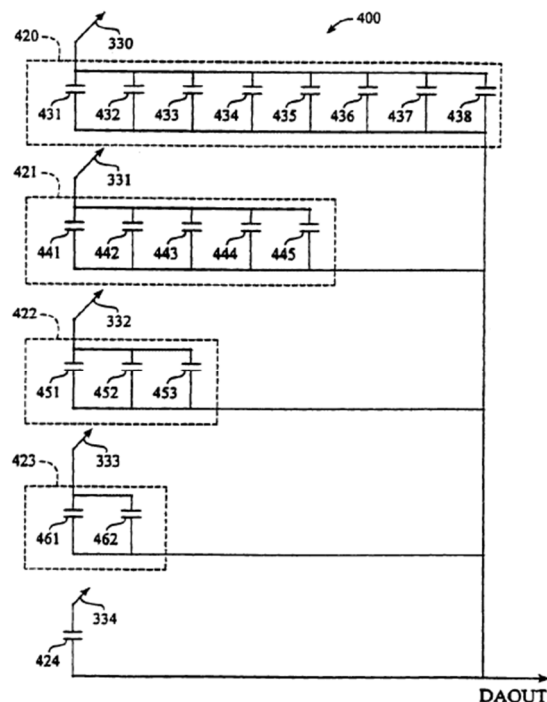
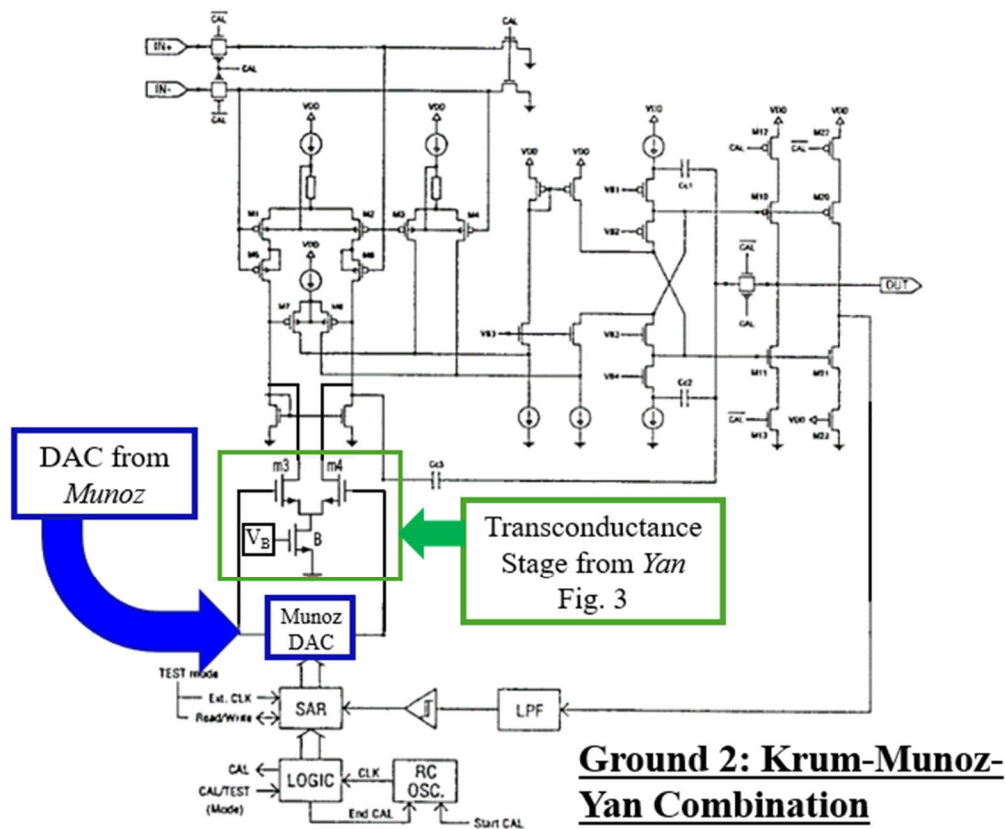


Fig. 3B

Ex. 1008, Fig 3B. Accordingly, where the one additional bit corresponds to capacitor bank 424 a POSITA would understand, the input offset control would be one half the input offset control from 423 (the LSB before 424 is added). Ex. 1003, ¶¶158-160.

IX. GROUND 2: KRUM AND MUNOZ, IN VIEW OF YAN RENDERS OBVIOUS CLAIMS 1 AND 5-7

The *Krum-Munoz-Yan* combination of Ground 2, like the *Krum-Munoz* combination provides a DAC having a radix less than 2 from *Munoz*. However, the *Krum-Munoz-Yan* combination implements this DAC as a voltage mode DAC rather than a current mode DAC, so it requires an additional transconductance stage as taught by *Yan*. Ex. 1003, ¶161. The *Krum-Munoz-Yan* combination is depicted below:



Ex. 1003, ¶161.

A. Overview of Ground 2

1. Yan

Yan was filed on October 30, 2007 and issued as U.S. Patent No. 7,642,846 on January 5, 2010, so it is prior art under 102(e). Ex. 1007, Title Page; Ex. 1003, ¶74. *Yan* discloses methods for providing offset compensation for opamps. Ex. 1007, Title. Ex. 1003, ¶75.

Yan provides a prior art example of a conventional amplifier with offset compensation for autozeroing:

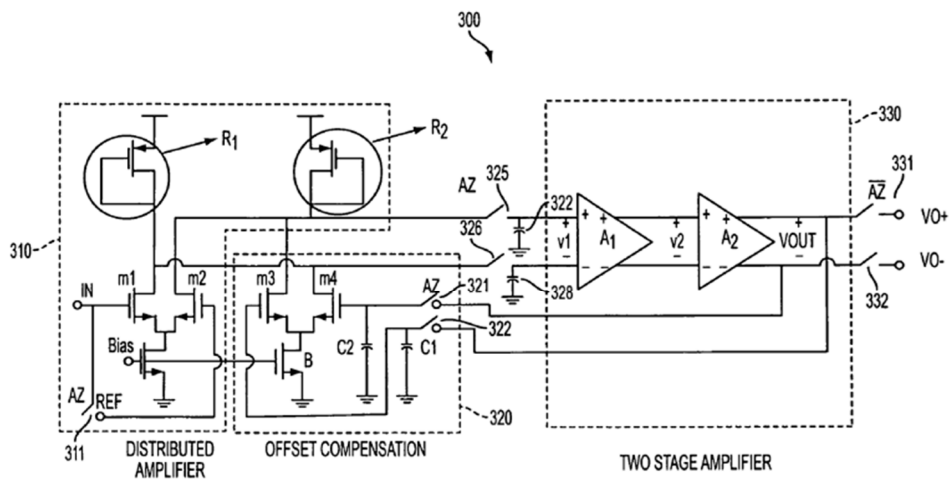


FIG. 3
PRIOR ART

Ex. 1007 [Yan] Fig. 3. The amplifier block 330 is connected to an input gain stage 310 and offset compensation stage 320. Ex. 1007, 2:22-25; Ex. 1003, ¶76. A gain stage, like the one depicted above, is known to have a differential pair m1 and m2 and an offset compensation stage 320 is known to include a differential pair m3 and m4. Ex. 1003, ¶76. Both stages have their inputs connected together. Ex. 1007, Fig. 3; Ex. 1003, ¶76.

B. Motivation to Combine

A POSITA would have been motivated to combine the teachings of *Krum* and *Munoz* to modify *Krum*'s binary-weighted DAC to be a DAC with radix of less than 2 according to *Munoz* as described *supra* Section VIII.B. See also, Ex. 1005, 1; Ex. 1008, 1:66-2:4, 2:24-42, 4:58-60, 5:15-21, 5:67-6:2, 7:67-8:14 8:55-58, 9:15-19, 16:53-58, 17:45-48, Fig. 1A; Ex. 1013, 1; Ex. 1018, 1; Ex. 1019, 2:10-15; Ex. 1003,

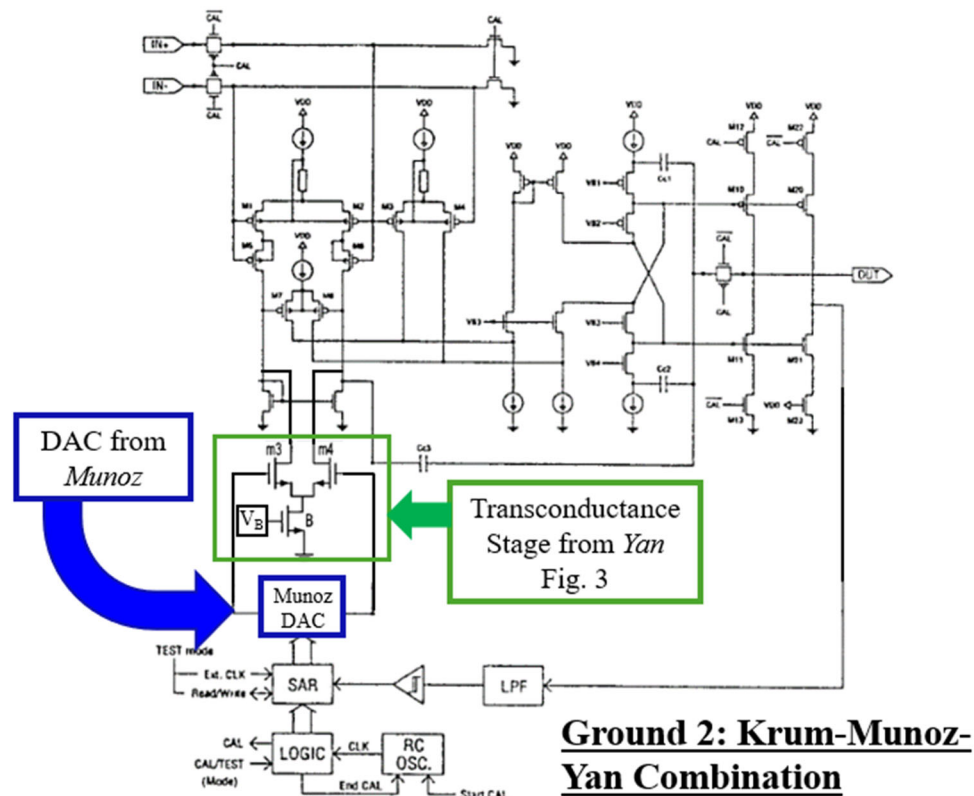
¶¶97, 101-105, 107-117, 162.

Munoz describes a DAC generally, which a POSITA would understand to be applicable to all types of DACs. Ex. 1003, ¶116. It would be obvious to a POSITA based on the teachings of *Munoz* to implement a voltage mode DAC rather than the current mode DAC (of the *Krum-Munoz* combination). Ex. 1003, ¶166. To implement a voltage mode DAC in *Krum's* system would also require use of an additional transconductance stage, which is described as prior art in *Yan*. Ex. 1005, 1 (“The offset cancelation uses a current-mode DAC”); Ex. 1007, 2:22-34; Fig. 3 (prior art); Ex. 1003, ¶163. *Yan*, like the '665 Patent, falls in the field of endeavor of operation amplifiers with offset compensation circuitry. Ex. 1001, 1:5-8, 1:28-44, Ex. 1007, 1:5-10; Ex. 1003, ¶164.

A POSITA would implement *Munoz's* DAC as a voltage mode DAC with use of an additional transconductance stage to convert a voltage difference into a current. Ex. 1003, ¶166. The use of *Yan's* transconductance stage with the DAC of *Munoz* and the amplifier of *Krum* is no more than “the predictable use of prior art elements according to their established functions.” *KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007). Indeed, implementation of *Yan's* circuitry would be well within the skills of a POSITA and would yield predictable results. Each prior art element (the transconductance stage of *Yan*, the DAC of *Munoz*, and the amplifier of *Krum*) has an established function and would perform such established function in the

proposed combination. Ex. 1003, ¶¶165-166. The proposed combination would operate in a predictable manner. Ex. 1003, ¶166.

The *Krum-Munoz-Yan* combination would be achieved with a reasonable expectation of success as depicted below:



Ex. 1003, ¶167.

As depicted, the drains of m3 and m4 in *Yan* are connected to the drains of the transistors M5 and M6 in *Krum*. Ex. 1003, ¶167. *Yan*'s capacitors C1 and C2 can be removed as the function of the memory elements is replaced by the DAC which drives the gates of m3 and m4. Ex. 1003, ¶167. Lastly, the transistor B's gate

would be connected to a biasing voltage. Ex. 1003, ¶167. Such implementation is achieved with a reasonable expectation of success. Ex. 1003, ¶167.

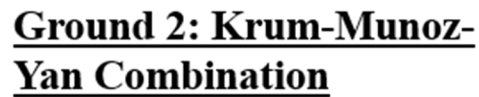
C. Independent Claim 1

**1. [1pre] An amplifier system having an amplifier system
input and an amplifier system output comprising:**

To the extent the preamble is limiting, it is obvious for the reasons described with respect to the *Krum-Munoz* combination. *Supra* Section IX.C.1; Ex. 1005, Fig. 1; Ex. 1003, ¶¶118, 168.

2. [1a] a first amplifier;

The *Krum-Munoz-Yan* combination renders this limitation obvious for the reasons described with respect to the *Krum-Munoz* combination. *Supra* Section VIII.C.2; *See also* Ex. 1005, Title, Fig. 1; Ex. 1003, ¶¶119-120, 169. The first amplifier is depicted below in red:



3. [1b] a comparator;

4. [1c] a successive approximation register having an input coupled to an output of the comparator;

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VIII.C.4; *See also* Ex. 1005, 1, Fig. 1; Ex. 1003, ¶¶125, 172.

- 5. [1d] a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;**

The *Krum-Munoz-Yan* combination renders this limitation obvious for the reasons described with respect to the *Krum-Munoz* combination. *Supra* Section VIII.C.5; *See also* Ex. 1005, 1, Fig. 1; Ex. 1003, ¶¶128-129, 173.

- 6. [1e] a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator,**

The *Krum-Munoz-Yan* combination renders this limitation obvious for the reasons described with respect to the *Krum-Munoz* combination. *Supra* Section VIII.C.6; *See also* Ex. 1005, 1, Fig. 1; Ex. 1003, ¶¶129, 131, 133-137, 174.

- 7. [1f] an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;**

The *Krum-Munoz-Yan* combination renders this limitation obvious for the reasons described with respect to the *Krum-Munoz* combination. *Supra* Section VIII.C.7; *See also* Ex. 1005, Fig. 1; Ex. 1008, 2:32-40, 6:45-51, 7:67-8:5, 8:36-41, Fig. 4; Ex. 1013, 1; Ex. 1003, ¶¶139-143, 175.

8. [1g] the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

The *Krum-Munoz-Yan* combination renders this limitation obvious for the reasons described with respect to the *Krum-Munoz* combination. *Supra* Section VIII.C.8; *See also* Ex. 1008, 6:45-48, 6:54-7:13, 7:16-20, 9:18-19; Ex. 1003, ¶¶145-147, 176.

9. [1h] an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

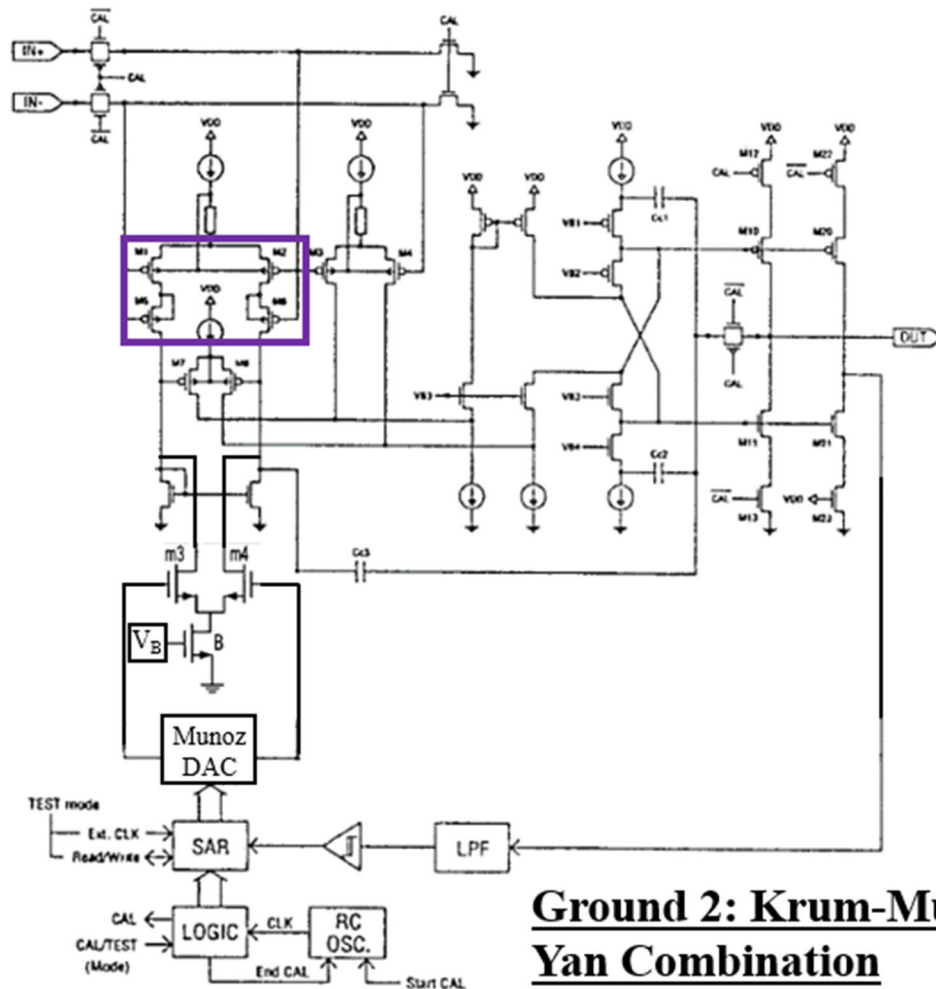
The *Krum-Munoz-Yan* combination renders this limitation obvious for the reasons described with respect to the *Krum-Munoz* combination. *Supra* Section VIII.C.9; *See also* Ex. 1005, 1, Fig. 1; Ex. 1003, ¶¶149-150, 177.

D. Claim 5

1. [5a] The amplifier system of claim 1 wherein the first amplifier has a first transconductance differential input stage coupled to the first amplifier input,

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003, ¶178. *Krum* teaches that “[t]he input pair M1 and M2 is cascoded by transistors M5 and M6”. Ex. 1005, 1. A POSITA would recognize that PMOS transistors M1, M2, M5, and M6 form a transconductance differential stage. Ex. 1003, ¶179. Transistors M1 and M2 are configured in a common-source scheme, and consistent with element

[1d] the gate of M1 is mapped to the first amplifier input. Ex. 1003, ¶180. Thus, the claimed “first transconductance differential input stage” includes PMOS transistors M1, M2, M5, and M6 depicted in purple:

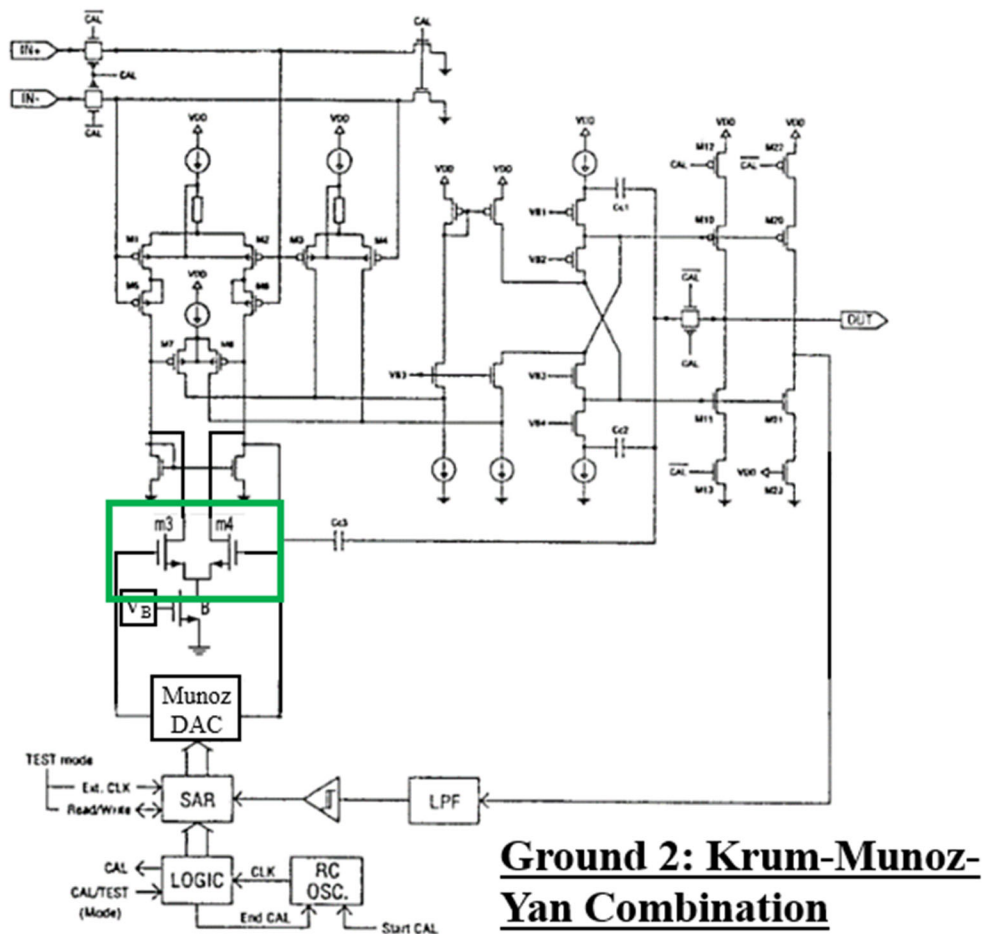


Ex. 1005, Fig. 1; Ex. 1003, ¶179.

2. [5b] and wherein the first amplifier is further comprised a second transconductance differential input stage,

The *Krum-Munoz-Yan* combination render this limitation obvious. Ex. 1003, ¶181. The combination teaches the first amplifier further comprised of a second

transconductance differential input stage. A POSITA would recognize that the transistors m3 and m4 depicted in green are coupled in a common-source scheme and are acting as inputs for the offset calibration signal coming from the CALDAC, thus teaching the second transconductance differential input stage:



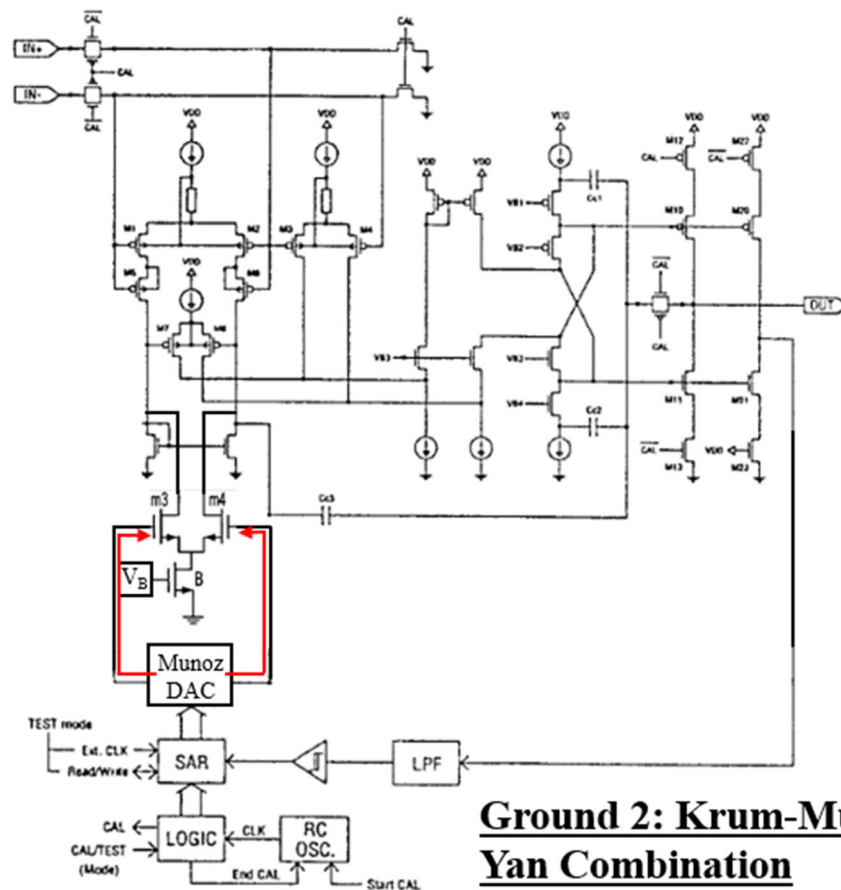
The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003,

Ground 2: Krum-Munoz-Yan Combination

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4. [5d] the output of the D/A converter being coupled to inputs of the second transconductance differential input stage

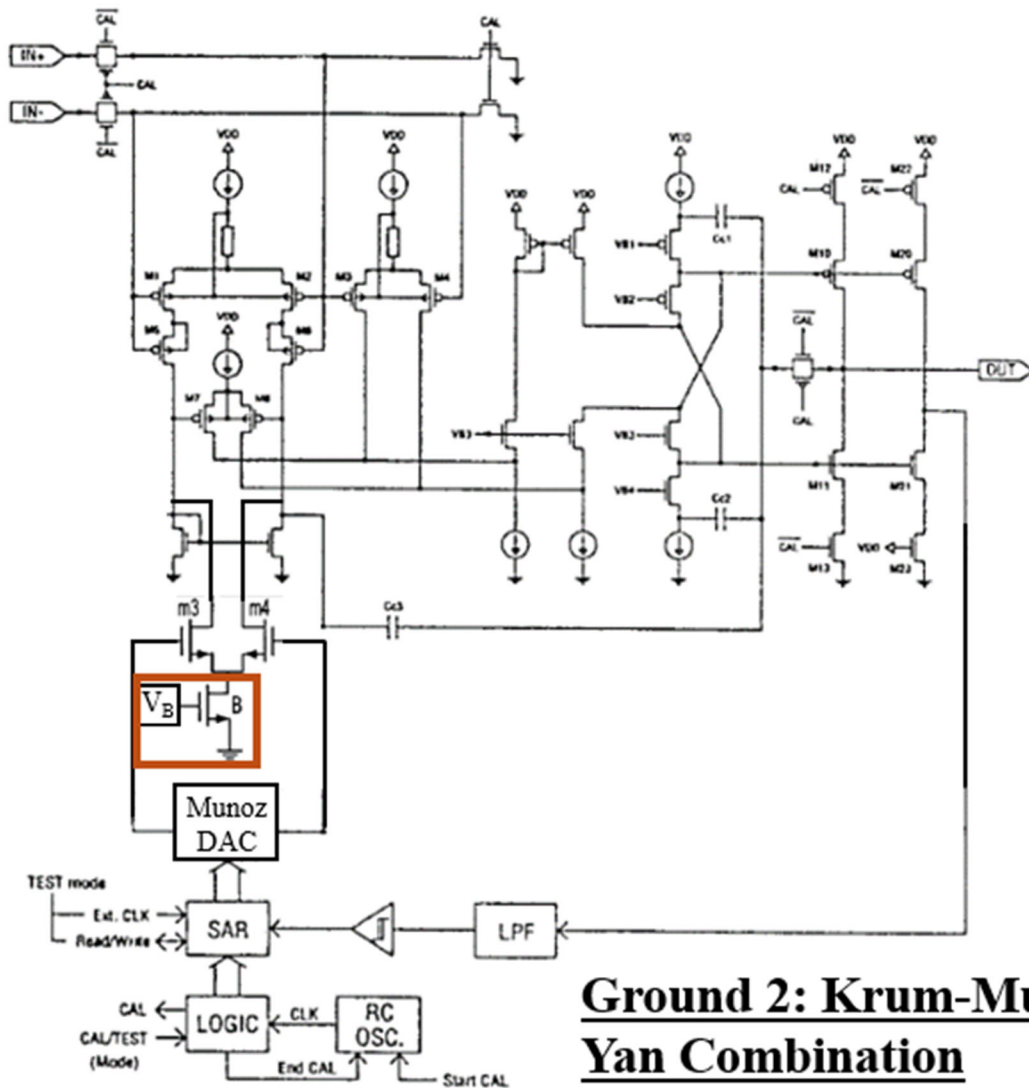
The *Krum-Munoz-Yan* combination renders this element obvious. Ex. 1003, ¶187. For example, the output of the D/A converter is depicted with the red arrows as connecting to the inputs of the second transconductance differential input stage:



Ex. 1005, Fig. 1; Ex. 1003, ¶188.

5. [5e] to divide a current source coupled to the second transconductance differential input stage between the differential outputs of the first transconductance differential input stage in a proportion to reduce the input offset of the first amplifier.

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003, ¶189. Both transistors m3 and M4 are connected to, and biased by, a current source (V_B) connected to the biasing transistor B:



Ex. 1005, Fig. 1; Ex. 1003, ¶190. Transistors m3 and m4 include drains which couple to the drains of transistors M5 and M6 respectively. Ex. 1003, ¶191. M5 and M6, as the differential input stage, receive portions of the current from the second transconductance amplifier current source. *Id.* When there is an offset voltage, the currents from m3 and m4 will become unequal and the DAC output will adjust the division of the current (from V_B) between the two branches to reduce the offset

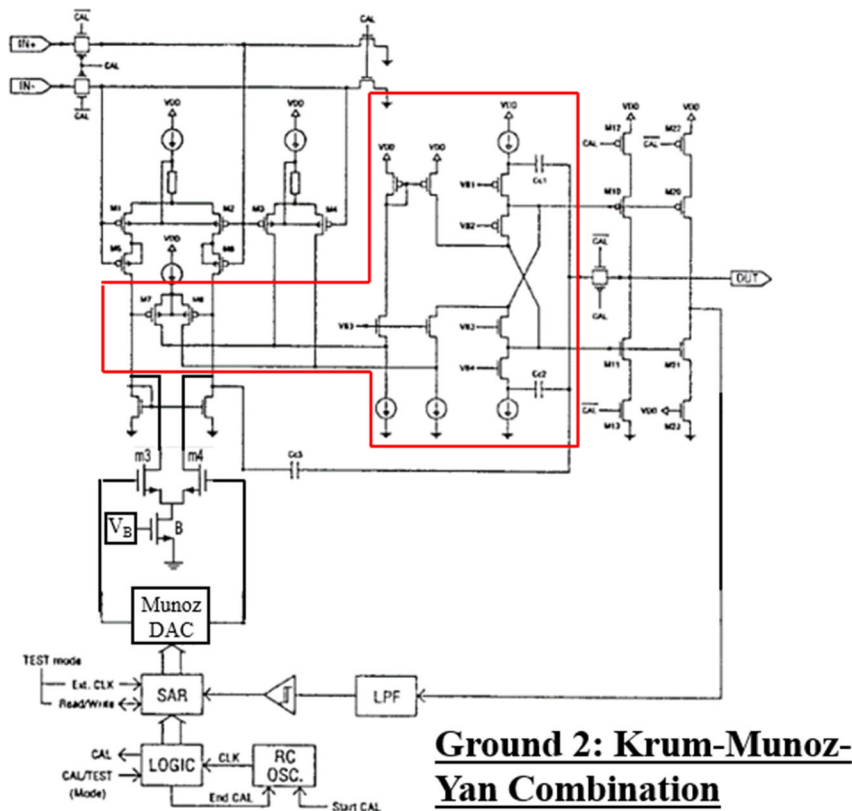
voltage. Ex. 1003, ¶192.

E. Claim 6

1. [6a] The amplifier system of claim 5 wherein the first amplifier further comprises an intermediate stage having an input coupled to the parallel connected outputs of the first and second transconductance differential input stages,

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003,

¶193. For example, *Krum* includes an intermediate stage depicted in red:

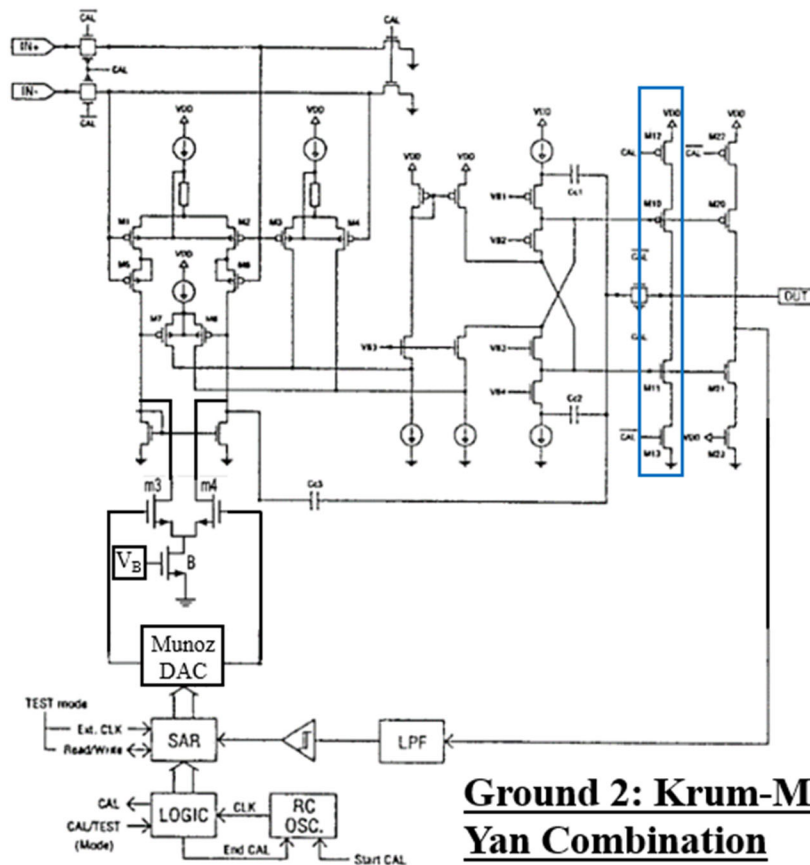


Ex. 1005, Fig. 1; Ex. 1003, ¶194. The intermediate stage has two inputs—the gates of M7 and M8. The gate of M7 is coupled to the parallel connections of the drains

of transistors M5 and m3, which together are outputs of the first and second transconductance differential input stages. Ex. 1003, ¶195. Likewise, the gate of M8 is coupled to the parallel connections of the drains of transistors M6 and m4, which are also outputs of the first and second transconductance differential input stage. *Id.*

2. [6b] a first output stage providing the first amplifier output,

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003, ¶196. The claimed “first output stage” includes transistors M10, M11, M12, and M13 as depicted below in blue:

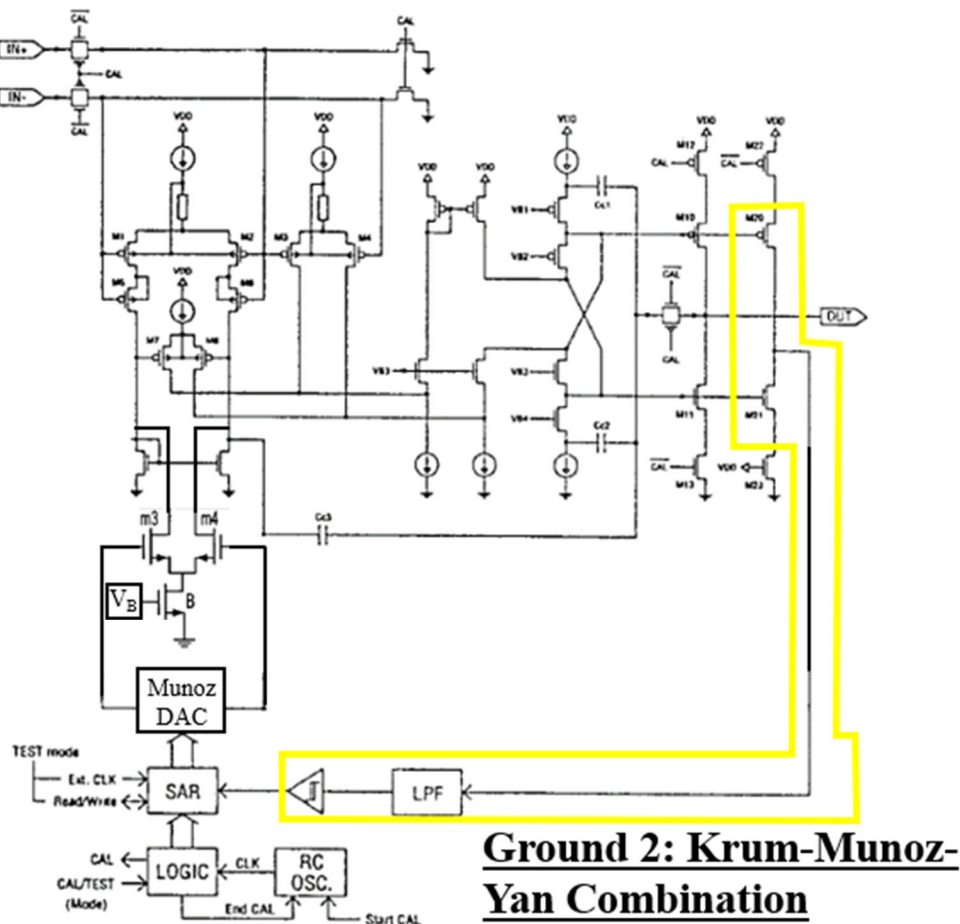


Ground 2: Krum-Munoz-Yan Combination

Ex. 1005, Fig. 1; Ex. 1003, ¶197. The outputs of transistors M10 and M11 are the first amplifier output. Ex. 1003, ¶197.

3. [6c] a second output stage forming the comparator,

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003, ¶198. The second output stages forms a comparator as shown in yellow below including elements M20, M21, the low pass filter, and a Schmitt trigger:



Ex. 1005, Fig. 1; Ex. 1003, ¶198. During autozeroing, a replica signal is provided to the comparator systems by transistors M20 and M21. Ex. 1003, ¶199.

4. [6d] the second switch for switching an output of the intermediate stage between inputs to the first and second output stages.

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003, ¶200. The second switch was depicted with respect to limitation 1[e] for Ground 1. *See supra* Section VIII.C.6. The second switch switches between transistors M10 and M11 (first output stage) and the transistors M20 and M21 (second output stage). Ex. 1003, ¶200.

As noted in *Krum*, “[d]uring autocalibration.... output transistors M10 and M11 are disconnected from their respective supplies” and the “small replica transistors M20 & M21 (scaled to M10 & M11) are used to provide the amplifier output signal for the calibration circuit.” Ex. 1005, 1; Ex. 1003, ¶201.

F. Claim 7

1. [7a] The amplifier system of claim 6 wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage,

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003, ¶202. As noted above, the second switch includes transistors M12, M13, M22, and M23. *See Supra* Section VIII.C.6. In autozeroing mode, transistors M20 and M21

are both on, thus coupling the intermediate stage with the comparator. Ex. 1003, ¶¶203-204. Also, during autozeroing mode, the switches M12 and M13 (which are included as part of the second switch) are off, which sets the first output stage to a high impedance state. Ex. 1005, 1 (“incorporates additional switches (M12 and M13) to put the output node into high-impedance mode during auto-calibration”); Ex. 1003, ¶205.

2. [7b] and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

The *Krum-Munoz-Yan* combination renders this limitation obvious. Ex. 1003, ¶206. For example, during normal operation, transistors M10 and M11 are powered on (through transistors M12 and M13). Ex. 1003, ¶207. Transistors M10 and M11 provide an output from the intermediate stage. *Id.* In other words, the second switch couples the input of the first output stage to the output of the intermediate stage. *Id.*

At the same time, transistors M20 and M21 are set to a high impedance state by transistors M22 and M23. Ex. 1003, ¶208. Accordingly, Claim 7 is obvious.

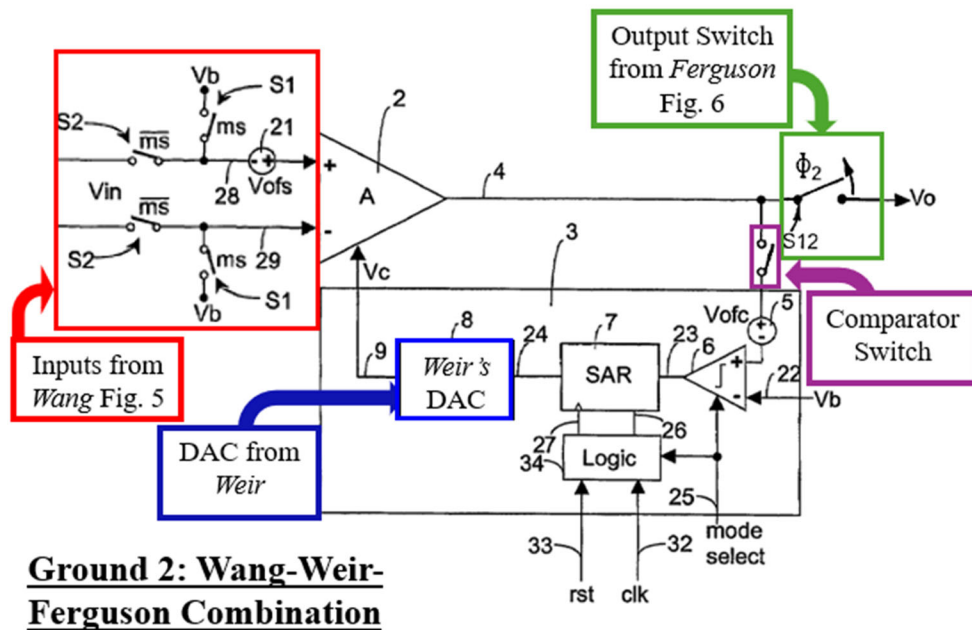
X. GROUND 3: WANG IN VIEW OF WEIR AND FERGUSON RENDERS OBVIOUS CLAIMS 1-4 AND 9

A. Overview of Ground 3

Wang teaches a system in which “the offset of at least one operational

amplifier is compensated by a dedicated circuitry.” Ex. 1009 1:5-7; Ex. 1003, ¶209. *Wang*’s system uses a feedback system including a comparator, a SAR, and a DAC. *Wang* does not teach any details about the structure of its DAC, and its opamp is connected to the system output during offset calibration. Ex. 1003, ¶209.

Weir teaches a SAR DAC “in which a non-binary sequence is employed, and which does not require precise components.” Ex. 1014, 1:13-15; Ex. 1003, ¶210. Recognizing the benefits of *Weir*’s DAC, a POSITA would substitute *Weir*’s DAC (in blue) into *Wang*’s system with routine engineering. A POSITA would also modify *Wang* to include switches to reduce the risk of voltage glitches as described in *Ferguson* (in green) and *Wang* itself (in purple). Further, the input switch structure (in red) described in *Wang* Fig. 5 is implemented as contemplated by the specification. Ex. 1009, 4:45-46; Ex. 1003 ¶212. Accordingly, a POSITA would arrive at a combination of *Weir*, *Wang*, and *Ferguson*:



Ex. 1003, ¶211.

1. Wang

Wang (Ex. 1009), claims priority to a foreign filing filed February 11, 2003, was filed as a PCT application on January 28, 2004, issued September 4, 2007. Ex. 1009, Title; Ex. 1003, ¶77. Accordingly, it is prior art under 35 U.S.C. § 102(b).

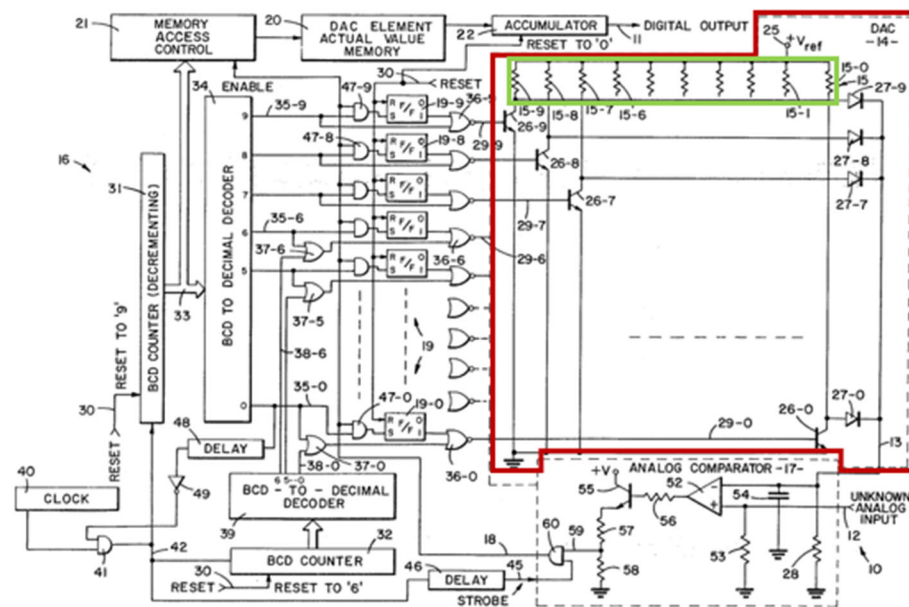
Wang provides an integrated circuit which includes dedicated circuitry used to compensate for offset of operational amplifiers. Ex. 1009, 1:4-8. *Wang's* system automatically compensates for a range of offset voltages in operational amplifiers while preserving high precision without requiring a lot of circuit overhead. Ex. 1009, 1:63-2:4; Ex. 1003, ¶78. *Wang* compensates for the opamp offset by using a successive approximation register. Ex. 1009, 2:53-3:7. *Wang's* system compensated for the offset of an amplifier 2 through a self-zeroing control unit 3

[illegible]

Ex. 1009, Fig. 3, 3:8-11. *Wang's* comparator, SAR, and DAC are standard circuit elements. Ex. 1009, 3:12-13; Ex. 1003, ¶¶78-79. The DAC output signal is applied to one node of the opamp 2 when the self-zeroing is performed and input 28 receives a DC voltage in the self-zeroing mode. Ex. 1009, 3:30-38; Ex. 1003, ¶80.

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compensated for at later steps. Ex. 1014, 2:51-56; Ex. 1003, ¶82. Instead, by employing a non-binary sequence where the sum of the preceding series elements exceeds the value of the next element (i.e. a series where the radix is less than 2) the accuracy requirements of the comparator are substantially reduced. Ex. 1014, 3:8-12; Ex. 1003, ¶83.



3. Ferguson

1010, Title; Ex. 1003, ¶85. Accordingly, it is prior art under pre-AIA 35 U.S.C. § 102(b).

Ferguson teaches a system “designed to reduce voltage glitches at an output of a circuit of a circuit when an output of an amplifier is switched out and back into the circuit in order to undergo, for example, offset calibration.” Ex. 1010, 11:64-67; Ex. 1003, ¶86. *Ferguson*’s Fig. 6 depicts switches S11, S12, and S13 used to reduce voltage glitches:

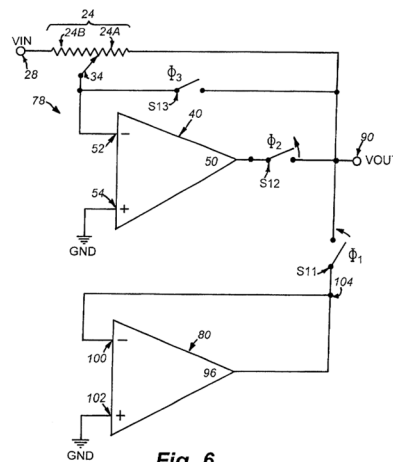


Fig. 6

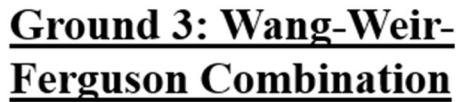
Ex. 1010, Fig. 6, 11:64-67; Ex. 1003, ¶86. Catching amplifier 80 is designed to be proportional to the main amplifier 40, although catching amplifier 80 may be significantly smaller. Ex. 1010, 12:13-22. Switches S11, S12, and S13 are configured to open and close based on specific clock signals to mute the main amplifier. Ex. 1010, 12:22-51, Fig. 8, Fig. 9. Switch S11 connects the output 86 of catching amplifier 80 to the output node 90 of the circuit, switch S12 connects the

output 50 of the main amplifier 40 and the output node 90, and switch S13 connects the output node 90 and inverting input 52 of main amplifier 40. Ex. 1010, 12:26-37; Ex. 1003, ¶¶87-90.

B. Motivation to Combine

A POSITA would be motivated to (1) improve the circuit used to compensate for opamp offset described in *Wang* by implementing the nonbinary DAC described in *Weir* (in blue) and (2) implement an output switch from *Ferguson* (in green) to reduce voltage glitches at *Wang*'s output. Ex. 1003, ¶¶212-213. Further, the input switch structure (in red) described in *Wang* Fig. 5 and a comparator switch is implemented as contemplated by the specification. Ex. 1009, 4:45-46, 5:34-41. The proposed combination is depicted below³:

³ For simplicity, the additional anti-glitch circuitry, which would be part of the combination, is omitted from the Ground 3 Combination diagram. Ex. 1003, ¶¶222-224.



Wang, *Weir*, and *Ferguson* are analogous art to the '665 Patent. *Wang* and *Ferguson*, like the '665 Patent, fall into the field of endeavor: operational amplifier with offset compensation circuitry. See, Ex.1001, Title, 1:5-8; Ex. 1009, Abstract, 1:4-7; Ex. 1010, Title, Abstract, 1:5-7; Ex. 1003, ¶214. *Weir* addresses the pertinent problem of the '665 Patent, namely, improvements to successive approximation converters, which are often used in opamps to improve for offset voltages. Ex. 1001, 1:20-57, 2:41-55, 7:30-35; Ex. 1014, 1:10-15, 1:23-26; Ex. 1003, ¶214.

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taught by *Ferguson* and *Wang* itself.

A POSITA would be motivated to implement the DAC with nonbinary elements from *Weir* into *Wang*. Ex. 1003, ¶216. *Wang* recognizes the need for a system to automatically compensate for a high range of offset in optical amplifiers while still preserving a high level of precision. Ex. 1009, 1:63-67; Ex. 1003, ¶215. Another objective of *Wang* is to implement a circuit to compensate for offset voltage that requires reduce circuit overhead. Ex. 1009, 2:1-4; Ex. 1003, ¶215. To accomplish this goal, *Wang's* system used a successive approximation procedure. Ex. 1009, 3:9-11; Ex. 1003, ¶215. A POSITA would be motivated to modify *Wang's* successive approximation procedure to improve its precision. Ex. 1003, ¶216.

Successive approximation systems may suffer reduced accuracy if the error in a specific DAC element in a successive approximation system has an error greater than the magnitude of the smallest element in that series. Ex. 1014, 2:11-17; Ex. 1003, ¶216. A POSITA concerned with improving the accuracy of the successive approximation procedure would be motivated to implement teachings from *Weir*, as *Weir* substantially reduces the strict accuracy requirements of DAC elements. Ex. 1014, 3:8-12; Ex. 1003, ¶¶216-217. Indeed, a person interested in implementing improvements to the offset voltage compensation system of *Wang* would be motivated to combine its circuit with the improved DAC of *Weir*. Ex. 1003, ¶218.

Further, *Weir* also provides additional details regarding the operations of a

DAC not described in *Wang*. For example, *Weir* provides additional details regarding the internal structure of a DAC which would assist a POSITA in implementing *Wang*'s teachings. Ex. 1003, ¶219. *Wang* itself does not provide this level of detail. Accordingly, *Wang*'s teachings can be supplemented with the teachings of a reference with greater details, such as *Weir*.

A POSITA would also be motivated to implement additional standard switches into *Wang*. Ex. 1003, ¶220. First, it would be obvious to implement a comparator switch in *Wang*'s system. The comparator of *Wang*'s system is configured to turn off when the self-zeroing mode is not occurring. Ex. 1009, 5:34-40. The on/off function of *Wang*'s comparator already has the effect of a switch leading to the self-zeroing circuitry. Ex. 1003, ¶220. It would be obvious to a POSITA to implement a comparator switch as a separate circuit element to avoid modifying the circuitry of a comparator. Ex. 1003, ¶221. Indeed, *Wang* itself describes a system which uses a switch between the output of an opamp and a comparator to toggle between self-zeroing modes for different components. Ex. 1009, 6:66-7:1; Ex. 1003, ¶220.

Wang also teaches the importance of isolating the self-zeroing circuitry from different stages of the integrated circuit and achieves this improved isolation through use of one or more switches. *See* Ex. 1009, 4:43-5:33. Accordingly, it would be obvious to include a comparator switch as a separate component.

Additionally, a POSITA would also be motivated to implement anti-glitch circuitry as described in *Ferguson*. *Ferguson* describes implementing switches and a catching amplifier into an offset calibration system to avoid unwanted voltage glitches. Ex. 1010, 11:64-67. During offset calibration, the anti-glitch circuitry has the effect of muting the amplifier. Ex. 1010, 12:49-51. This prevents unwanted voltage glitches at an output. Ex. 1003, ¶222. A POSITA would be motivated to make this modification to *Wang* to improve the precision of *Wang*'s system output.

Accordingly, it would be obvious for a POSITA to modify *Wang*'s amplifier with self-zeroing circuitry to include a DAC with nonbinary elements, an output switch, and a comparator switch. Ex. 1003, ¶¶222-224; *see also* Ex. 1010, 11:67-64.

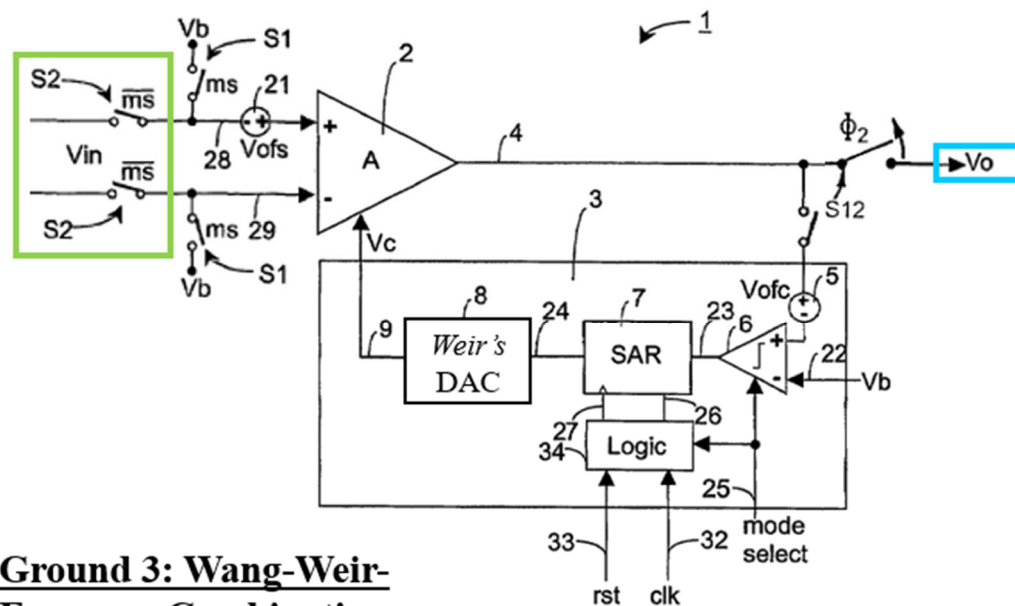
In this combination, the components continue to work in predictable ways to perform their tasks outputting the desired outcome as set forth in *Wang* and *Weir*. Ex. 1003, ¶225. *Wang*'s system needs to preserve “high precision” and provides a residual offset error of the autozeroing process that requires a correct decision when “all N bits have been decided by the SAR.” Ex. 1009, 1:62-67, 4:19-20. Error-free DACs are provided by *Weir*, “in which an error in comparison at one step of the DAC output can be compensated for during subsequent DAC output steps.” Ex. 1014, 3:6-8. The substitution of DACs is simply an exchange of known elements to obtain predictable results. Ex. 1003, ¶225. Likewise, switches are known circuit

elements which could be implemented into circuitry like *Wang* with routine engineering. Ex. 1003, ¶225. *Wang* itself teaches use of standard circuit elements which makes any modification simpler. Ex. 1009, 3:12-13; Ex. 1003, ¶225. Accordingly, construction of the *Wang-Weir-Ferguson* combination could be achieved with a reasonable expectation of success. Ex. 1003, ¶225.

C. Independent Claim 1

1. [1pre] An amplifier system having an amplifier system input and an amplifier system output comprising:

To the extent the preamble is limiting, the *Wang-Weir-Ferguson* combination renders the preamble obvious. For example, the combination discloses an input V_{in} shown in green and an output V_o shown in blue



Ground 3: Wang-Weir-Ferguson Combination

Ex. 1003, ¶226; Ex. 1009, Fig. 3, Fig. 5.

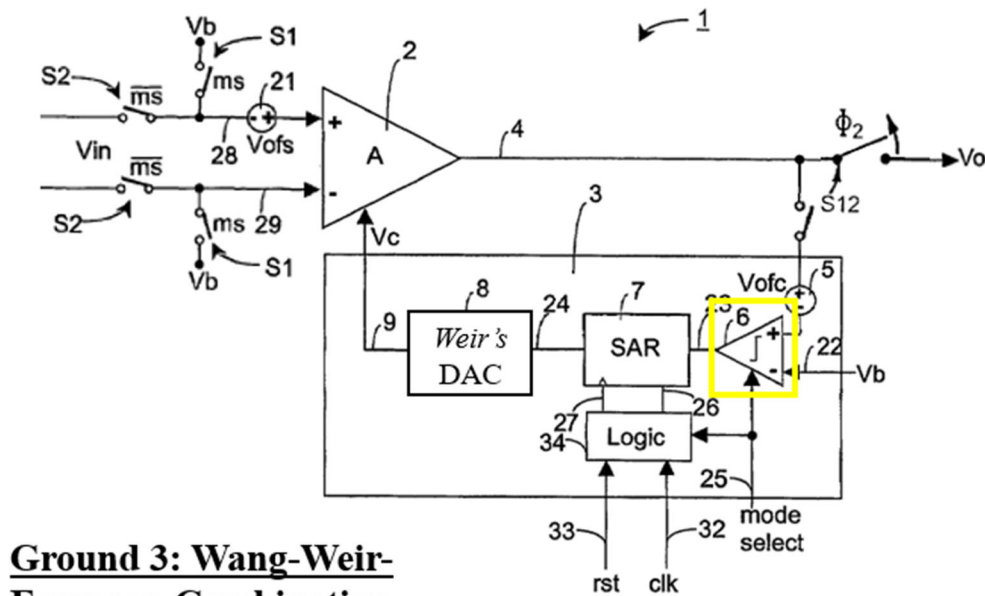
2. [1a] a first amplifier;

Wang discloses a first amplifier shown in red:

Ground 3: Wang-Weir-Ferguson Combination

Ex. 1009, Fig. 3; Ex. 1003, ¶227. As noted in *Wang*, the output of the DAC is in communication with the amplifier, and when *Weir's* DAC is substituted, the DAC output would remain in the same location. Ex. 1009, 3:30-35; Ex. 1003, ¶228.

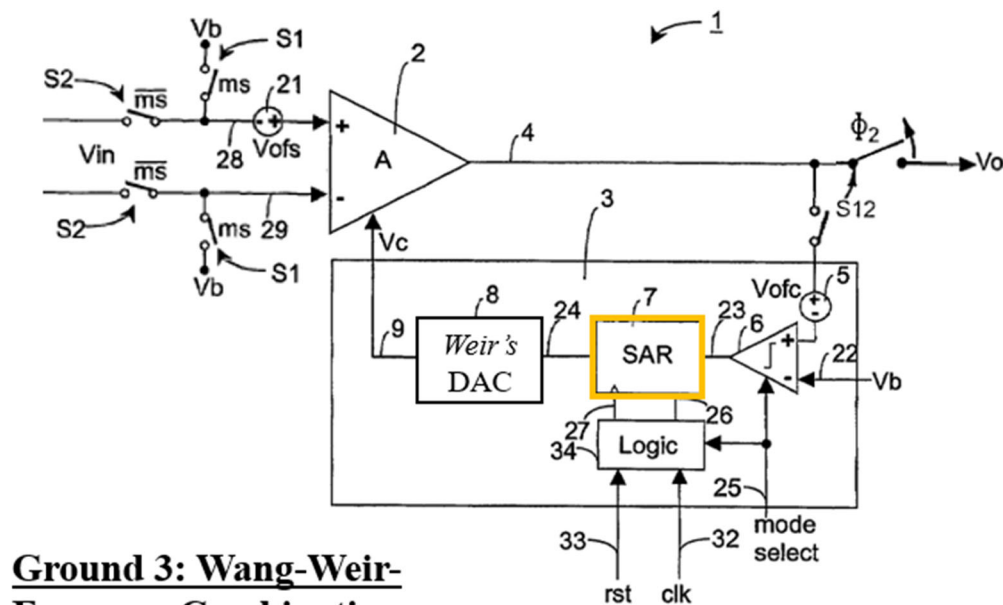
The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶229. The combination discloses a comparator depicted in yellow:



Ex. 1009, Fig. 3; Ex. 1003, ¶230.

4. [1c] a successive approximation register having an input coupled to an output of the comparator;

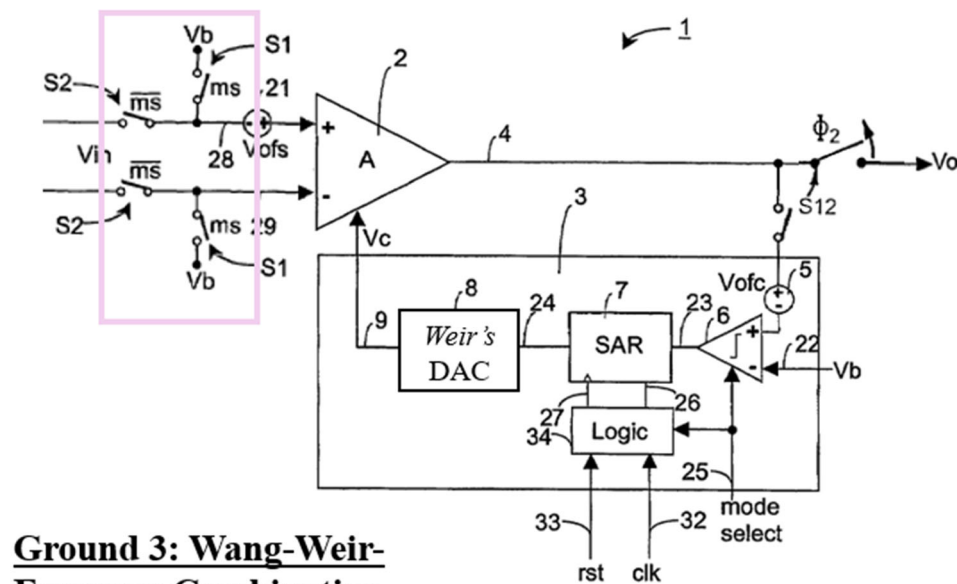
The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶231. *Wang* discloses a successive approximation register (SAR) (orange) having an input coupled to the output of the comparator:



Ex. 1009, Fig. 3; Ex. 1003, ¶232. The SAR is used to control the self-zeroing process and receives and input from the comparator. Ex. 1009, 3:8-9, 3:35-38; Ex. 1003, ¶232.

5. [1d] a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶233. *Wang* discloses a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input depicted in pink:



Ground 3: Wang-Weir-Ferguson Combination

Ex. 1009, Fig. 5; Ex. 1003, ¶234. As noted in the specification of the '665 Patent, the word switch may include a single or multiple switches as appropriate. Ex. 1001, 10:40-45. In autozeroing mode, both inputs of opamp 2 are shorted together resulting in a voltage of V_b . Ex. 1009, 3:39-42; Ex. 1003, ¶235. Additionally, switches S2 open to disconnect the inputs of the amplifier from the system inputs. Ex. 1009, 4:51-53; Ex. 1003, ¶235.

6. [1e] a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶236.

The *Wang-Weir-Ferguson* combination includes two switches shown in green

[illegible]

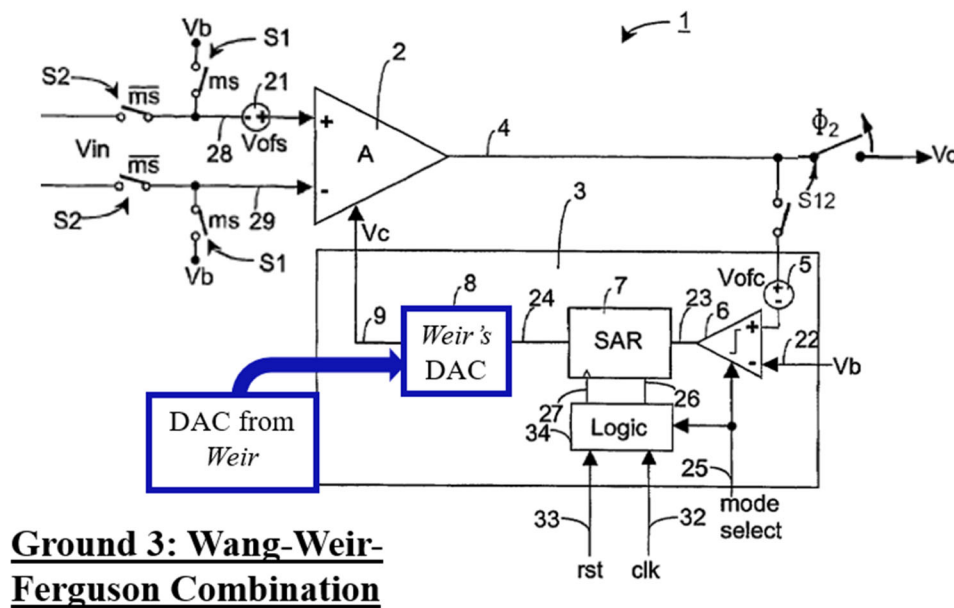
Ex. 1009, 5:34-40, Ex. 1010, 11:64-67; Ex. 1003, ¶¶237-238. The switch that leads to the comparator is open in normal operating mode. Ex. 1009, 5:37-41; Ex. 1003, ¶¶239-240. As depicted, the switches may be used for switching the output of the amplifier to the input of a comparator. Ex. 1003, ¶240. Indeed, *Wang* discloses using switches that are closed to enable the self-zeroing mode. Ex. 1009, 6:66-7:1. *Wang* also describes its comparator as turning off when the self-zeroing mode is not being performed. Ex. 1009, 5:34-41.

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zeroing and the output switch is closed only during normal operation. Ex. 1003, ¶240.

**7. [1f] an output of the successive approximation register
being coupled to an N bit digital to analog (D/A) converter;**

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶241. For example, as depicted below, the SAR can be implemented to couple to Weir's DAC shown in **blue**:



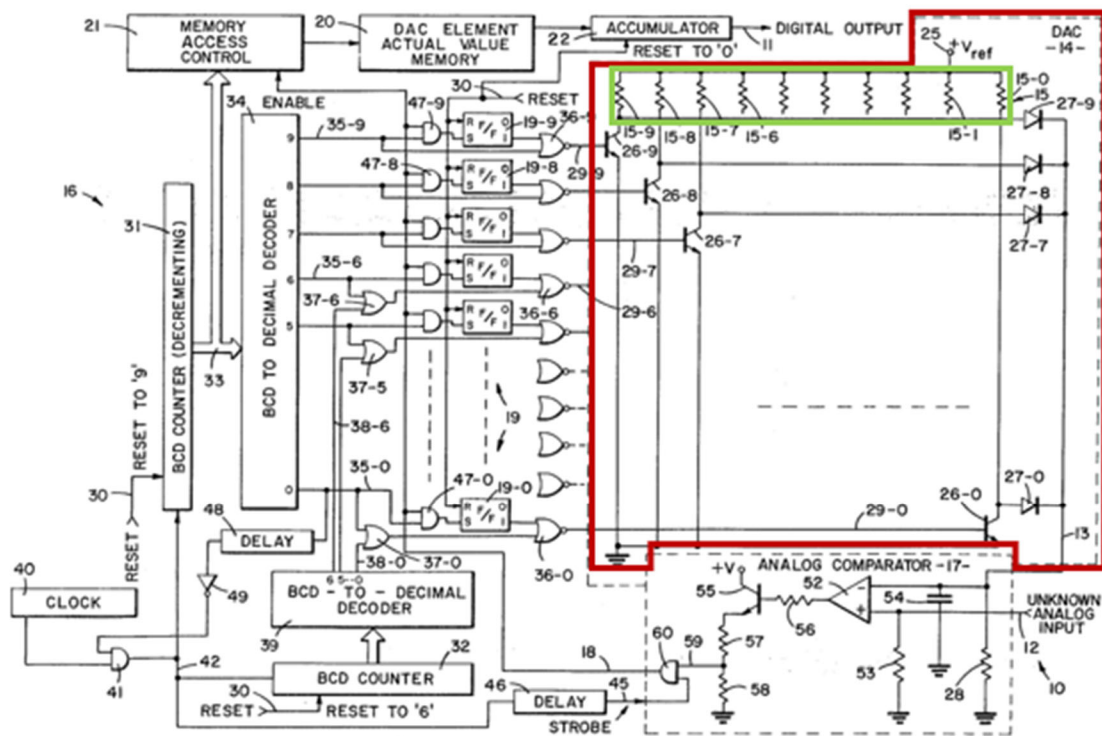
Ex. 1009, Fig. 3; Ex. 1003, ¶242. As described in *Wang*, the “SAR 7 here works in a very similar manner to a conventional and well known SAR ADC” where “a reference voltage VREF is provided to [a] K-bit digital-to-analog converter (DAC).” Ex. 1009, 2:59-61, 3:27-29; Ex. 1003, ¶243. A POSITA would also understand the DAC described in *Weir* to be an n-bit DAC. Ex. 1014, 1:31-33; Ex. 1003, ¶244.

Accordingly, the *Wang-Weir-Ferguson* combination renders obvious an output of the SAR coupled to an N-bit digital to analog converter.

8. [1g] the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶245. *Weir* is described as including resistive elements selected so that the DAC “can produce signals having magnitudes corresponding to the nonbinary series of $[ka^0, ka^1, ka^2, ka^3, ka^4, \dots ka^n]$ where $1 < a < 2$.” Ex. 1003, ¶246; Ex. 1014, 3:30-31. *Weir* further provides the example where a is equal to 1.8. Ex. 1014, 3:31-53; Ex. 1003, ¶247. The resistive elements provide the steps for the successive analog steps. Ex. 1014, Abstract. The resistive elements would enable *Weir*’s DAC to use a radix of less than two for at least the most significant bits. Ex. 1003, ¶246.

These resistive elements annotated in green within the DAC annotated in red are depicted below:



Ex. 1014, Fig. 1; Ex. 1003, ¶248.

9. [1h] an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶249. For example, *Wang* states that “the output 9 of the DAC 8 in Fig. 3 is applied to one node of the operational amplifier 2 on which the self zeroing is performed.” Ex. 1009, 3:32-35. Indeed, *Wang*’s system is constructed so that *Wang*’s DAC provides an output representing the offset at the opamp that is compensated. Ex. 1009, 3:66-4:2; Ex. 1003, ¶250. Accordingly, the *Wang-Weir-Ferguson* combination teaches using the DAC to control the input offset of the first

amplifier.

D. Claim 2

1. [2a] The amplifier system of claim 1 wherein the radix is approximately 1.9.

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶251. *Weir* provides for radix values between 1 and 2. Ex. 1014, 3:31-35. *Weir*'s system uses an example of a DAC with a radix of approximately 1.8. Ex. 1014 8:25-35; Ex. 1003, ¶253. *Weir* teaches that “the DAC resistance elements 15 need not have the precise values required to produce analog voltages or currents in the exact ratios of the series given by equation 1. What is required, however, is that the step values produced by the resistors 15 be known, and that these values be stored in the actual memory value 20.” Ex. 1014, 5:1-7; Ex. 1003, ¶252. *Weir* also teaches that “each such resistance element 15 may vary by as much as say 5% from the corresponding series exact value[.]” Ex. 1014, 8:58-60; Ex. 1003, ¶252. In fact, Table 1 of *Weir* describes the equation as providing “nominal” values for elements, but not the exact values. Ex. 1014, 5:12-28. Indeed, if both resistors may have an error of 5%, the radix range targeted at 1.8 could actually vary from between 1.63 to 1.99. Ex. 1003, ¶253. So, *Weir* renders obvious a ratio between successive resistive elements (and accordingly the radix) to result in a radix of approximately 1.9. *Id.*

E. Claim 3

1. [3a] The amplifier system of claim 2 wherein the radix for the least significant bit is 2.

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶254. *Weir* suggests a radix of 2. Ex. 1003, ¶255. As noted *supra* Section X.D.1, *Weir* contemplates a radix value between 1.63 and 1.99. Using a radix of 2 is also known to a POSITA. Ex. 1013, 1 (“In conventional digital-to-analog converters, the weights are powers of 2”); Ex. 1014, 1:52-55 (“For example, the DAC may employ a set of resistors which are selected to produce voltages or currents having values of 512, 256, 128, 64, 32, 16, 8, 4, 2 and 1”); Ex. 1019, 4:20-30. It would be obvious to attempt a radix of 2 in the least significant bit in light of these teachings and *Weir*’s contemplated range. Ex. 1003, ¶¶255-257; *See* Ex. 1013, 1; Ex. 1014, 1:52-55; Ex. 1019, 4:20-30.

Also, a POSITA would appreciate, reading *Weir* that the radix of the LSB being less than 2 is not needed to improve *Wang*. *Weir* is concerned with “error [that] can not be compensated for in later steps[,]” but there are no later steps than the LSB. Ex. 1014 [Weir] 2:52-56; Ex. 1003, ¶258. Further, any error would be insignificant compared to errors in the MSB. Ex. 1014, 2:11-17; Ex. 1003, ¶259. So, it would be obvious to a POSITA that the benefit of having a radix of less than 2 is not necessary at the LSB.

F. Claim 9

- 1. [9a] The amplifier system of claim 1 further comprised of One-Time-Programmable memory for permanently storing an output of the successive approximation register,**

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶260. *Weir* shows that the bit coefficients can be read from a memory 20, and teaches that “the actual value memory 20 may comprise a read-only memory which is preprogrammed at the time of manufacture.” Ex. 1014, 13:6-9. One time programmable (OTP) memory is a well know memory circuit used in integrated circuits. *See e.g.*, Ex. 1019 [Boyacigiller] 3:12-14; Ex. 1003, ¶261. It would be obvious to use OTP for the memory on the *Wang-Weir-Ferguson* combination.

- 2. [9b] whereby a single output of the D/A converter controlling the input offset of the first amplifier may be permanently maintained.**

The *Wang-Weir-Ferguson* combination renders this limitation obvious. Ex. 1003, ¶262. The output identified in element [1h] (i.e., signal VC) *supra* Section X.C.9 is permanently connected to the opamp and controls the input offset. Ex. 1009, 3:30-35; Ex. 1003, ¶263.

XI. DISCRETIONARY DENIAL IS NOT WARRANTED

A. *Fintiv* Denial Is Improper

Fintiv does not apply as the only co-pending district court matter is not a patent infringement action, such that no other district court is presently analyzing the validity of any claim of the '665 Patent. As a result, none of the *Fintiv* factors are applicable to this proceeding. Regardless, the compelling evidence of unpatentability in this Petition confirms that institution should occur.

Moreover, the co-pending case in NDCA, which is not a patent action, to the extent the findings in the PTAB would be helpful, is highly likely to be stayed should the request be filed. There is little, to no, duplication of efforts as infringement and invalidity are not at issue in the NDCA case.

To the extent changes are made to the now-governing standards regarding discretionary denial, Petitioner reserves its right to respond.

A. 35 U.S.C. § 325(d) Denial Is Improper

The factors in *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (PTAB Dec. 15, 2017), favor institution. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8-11 (PTAB Feb. 13, 2020) (precedential).

And while *Krum* was cited in an IDS (Ex. 1002, 83), it was not used in a rejection and the clear teachings in *Krum* of the sole element the examiner found to

be lacking in the prior art confirm that the examiner erred and overlooked the teachings of *Krum* as it relates to the '665 Patent.

The remaining references were not before the patent office and no rejections over any prior art occurred during prosecution. As such, neither the same, nor substantially the same arguments were previously presented.

XII. CONCLUSION

Petitioner requests institution of *inter partes* review and cancellation of Claims 1-7 and 9.

Dated: January 30, 2025

Respectfully submitted,

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CLAIM APPENDIX

[1pre] An amplifier system having an amplifier system input and an amplifier system output comprising:

[1a] a first amplifier;

[1b] a comparator;

[1c] a successive approximation register having an input coupled to an output of the comparator;

[1d] a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

[1e] a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;

[1f] an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

[1g] the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

[1h] an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

[2a] The amplifier system of claim 1 wherein the radix is approximately 1.9.

[3a] The amplifier system of claim 2 wherein the radix for the least significant bit is 2.

[4a] The amplifier system of claim 1 wherein the D/A converter further comprises one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits.

[5a] The amplifier system of claim 1 wherein the first amplifier has a first transconductance differential input stage coupled to the first amplifier input,

[5b] and wherein the first amplifier is further comprised a second transconductance differential input stage,

[5c] the outputs of the first and second transconductance differential input stages being coupled in parallel,

[5d] the output of the D/A converter being coupled to inputs of the second transconductance differential input stage to divide a current source coupled to the second transconductance differential input stage between the differential outputs of the first transconductance differential input stage

[5e] in a proportion to reduce the input offset of the first amplifier.

[6a] The amplifier system of claim 5 wherein the first amplifier further comprises

an intermediate stage having an input coupled to the parallel connected outputs of the first and second transconductance differential input stages,

[6b] a first output stage providing the first amplifier output,

[6c] a second output stage forming the comparator,

[6d] the second switch for switching an output of the intermediate stage between inputs to the first and second output stages.

[7a] The amplifier system of claim 6 wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage,

[7b] and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

[9a] The amplifier system of claim 1 further comprised of One-Time-Programmable memory for permanently storing an output of the successive approximation register,

[9b] whereby a single output of the D/A converter controlling the input offset of the first amplifier may be permanently maintained.

Certification of Word Count Under 37 C.F.R. § 42.24(d)

The undersigned hereby certifies that the foregoing contains 11,788 words according to the word count of the word-processing software used to prepare the foregoing.

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CERTIFICATE OF SERVICE

A copy of this Petition for *Inter Partes* Review and supporting materials has been served at the following correspondence address of record for the subject patent via Federal Express Priority Overnight® on this 30th day of January, 2025:

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