UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANALOG DEVICES, INC.,
Petitioner,

v.

NUMBER 14 B.V.,
Patent Owner.

IPR2025-00551
U.S. Patent 7,812,665

CERTIFIED FILE HISTORY OF U.S. PATENT NO. 7,812,665
(Ex. 1002)

FILE HISTORY

US 7,812,665

PATENT:	7,812,665
INVENTORS:	ESCHAUZIER RUDY G H VAN RIJN NICO
TITLE:	Amplifiers with input offset trim and methods
APPLICATION NO:	US2009390684A
FILED:	23 FEB 2009
ISSUED:	12 OCT 2010
COMPILED:	03 JAN 2025

7,812,665

AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

Transaction History

Date	Transaction Description
02-23-2009	Information Disclosure Statement considered
02-23-2009	Reference capture on IDS
02-23-2009	Information Disclosure Statement (IDS) Filed
02-23-2009	Applicants have given acceptable permission for participating foreign
02-23-2009	Information Disclosure Statement (IDS) Filed
02-23-2009	Initial Exam Team nn
03-17-2009	Corrected Paper
03-17-2009	Filing Receipt
05-18-2009	Additional Application Filing Fees
05-18-2009	Applicant has submitted new drawings to correct Corrected Papers problems
05-18-2009	Applicant has submitted a new specification to correct Corrected Papers problems
05-27-2009	Sent to Classification Contractor
05-28-2009	Filing Receipt - Updated
06-17-2009	Application Dispatched from OIPE
04-30-2010	Transfer Inquiry to GAU
05-17-2010	Case Docketed to Examiner in GAU
05-27-2010	Notice of Allowance Data Verification Completed
06-01-2010	Mail Examiner's Amendment
06-01-2010	Mail Notice of Allowance
08-26-2010	PG-Pub Issue Notification
08-31-2010	Information Disclosure Statement considered
08-31-2010	Reference capture on IDS
08-31-2010	Information Disclosure Statement (IDS) Filed
08-31-2010	Issue Fee Payment Verified
08-31-2010	Information Disclosure Statement (IDS) Filed
08-31-2010	Issue Fee Payment Received
09-07-2010	Miscellaneous Communication to Applicant - No Action Count
09-08-2010	Application Is Considered Ready for Issue
09-09-2010	Dispatch to FDC
09-09-2010	Mail Miscellaneous Communication to Applicant
09-22-2010	Issue Notification Mailed
10-12-2010	Recordation of Patent Grant Mailed
10-12-2010	Patent Issue Date Used in PTA Calculation
04-12-2018	Payment of Maintenance Fee, 8th Year, Large Entity
04-12-2022	Payment of Maintenance Fee, 12th Year, Large Entity
05-29-2024	Application ready for PDX access by participating foreign offices
05-29-2024	Application ready for PDX access by participating foreign offices

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12390684	ESCHAUZIER ET AL.
	Examiner	**Art Unit**
	Henry K Choe	2817

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
330	9	H 0 3 F 1 / 02 (2006.01.01)	

CROSS REFERENCE(S)

CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
327	124				

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1														
2	2														
3	3														
4	4														
5	5														
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7	7														
8	8														
9	9														
10	10														
11	11														
12	12														

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	12	
/Henry K Choe/ Primary Examiner.Art Unit 2817	5/26/2010	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	8

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12390684	ESCHAUZIER ET AL.
	Examiner	**Art Unit**
	Henry K Choe	2817

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/26/2010								
1	1	=								
2	2	=								
3	3	=								
4	4	=								
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	13	-								
	14	-								
	15	-								
	16	-								
	17	-								
	18	-								
	19	-								
	20	-								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12390684	ESCHAUZIER ET AL.
	Examiner	**Art Unit**
	Henry K Choe	2817

SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
330	9	5/25/10	/hc/
327	124, 307	5/25/10	/hc/

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
Tech Search (EAST)	5/25/10	/hc/

INTERFERENCE SEARCH			
Class	**Subclass**	**Date**	**Examiner**
Searched Above, See Attachment		5/25/10	/hc/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S8	8360	amplifier and offset and comparator and Digital adj4 analog adj2 converter	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/05/25 12:35
S9	6650	S8 and switch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/05/25 12:35
S10	668	S9 and second adj switch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/05/25 12:36
S11	264	S10 and differential adj amplifier	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/05/25 12:36
S12	151	S11 and register	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2010/05/25 12:37

5/25/10 1:07:32 PM
C:\Documents and Settings\hchoe\My Documents\EAST\Workspaces\qwer.wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	88	amplifier and offset and comparator and Digital adj4 analog adj2 converter and second adj switch and register	US-PGPUB	OR	ON	2010/05/25 13:08
L2	45	1 and differential adj amplifier	US-PGPUB	OR	ON	2010/05/25 13:10

5/25/10 1:11:30 PM
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US007812665B2

(12) **United States Patent**
Eschauzier et al.

(10) **Patent No.: US 7,812,665 B2**
(45) **Date of Patent: Oct. 12, 2010**

(54) **AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS**

(75) Inventors: **Rudy G. H. Eschauzier**, Bergschenhoek (NL); **Nico van Rijn**, Katwijk (NL)

(73) Assignee: **Number 14 B.V.**, Bergschenhoek (NL)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 29 days.

(21) Appl. No.: **12/390,684**

(22) Filed: **Feb. 23, 2009**

(65) **Prior Publication Data**

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(51) **Int. Cl.**
H03F 1/02 (2006.01)

(52) **U.S. Cl.** **330/9**; 327/124

(58) **Field of Classification Search** 330/9; 327/124, 307

See application file for complete search history.

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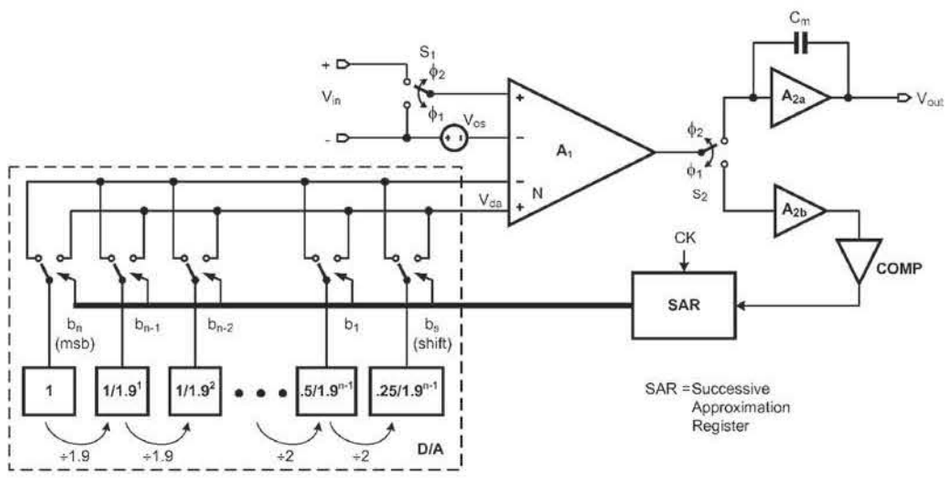
(Continued)

Primary Examiner—Henry K Choe
(74) *Attorney, Agent, or Firm*—Blakely Sokoloff Taylor & Zafman LLP

(57) **ABSTRACT**

Amplifiers with power-on trim and methods using an amplifier system having an amplifier system input and an amplifier system output, an amplifier, a comparator, a successive approximation register having an input coupled to an output of the comparator, a first switch for switching an input of the amplifier from the amplifier system input to shorting the amplifier input, a second switch for switching an output of the amplifier from the amplifier system output to an input of the comparator, an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter, the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits, and an output of the D/A converter being coupled to the amplifier to control the input offset of the amplifier. Novel embodiments for the amplifier, comparator and D/A converter are disclosed.

12 Claims, 10 Drawing Sheets



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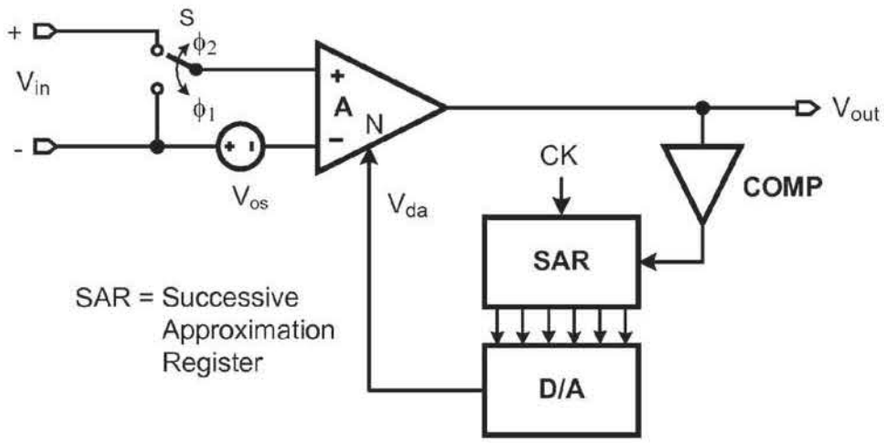


Fig. 1 (Prior Art)

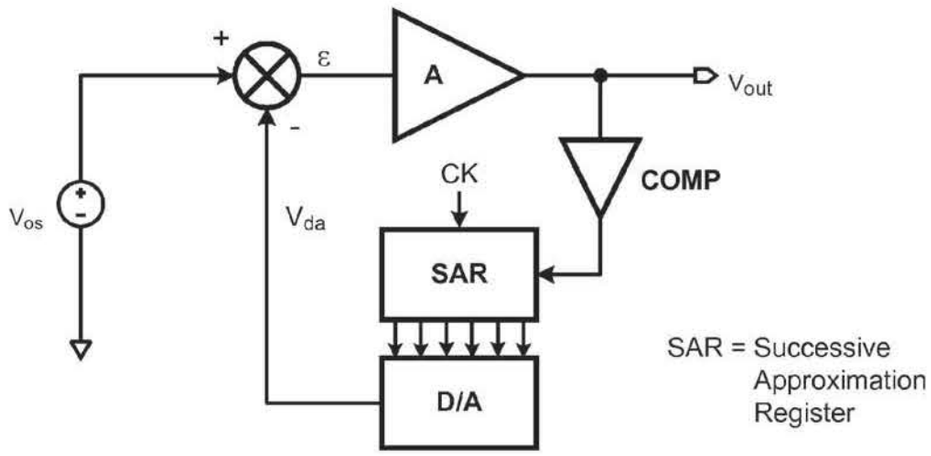


Fig. 2 (Prior Art)

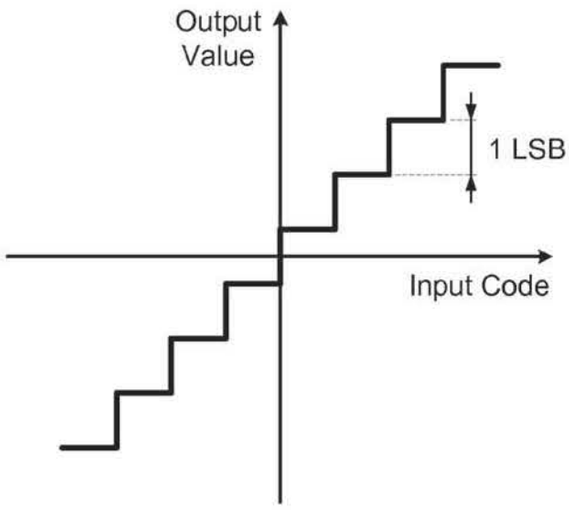

Output
Value
1 LSB
Input Code

Fig. 3

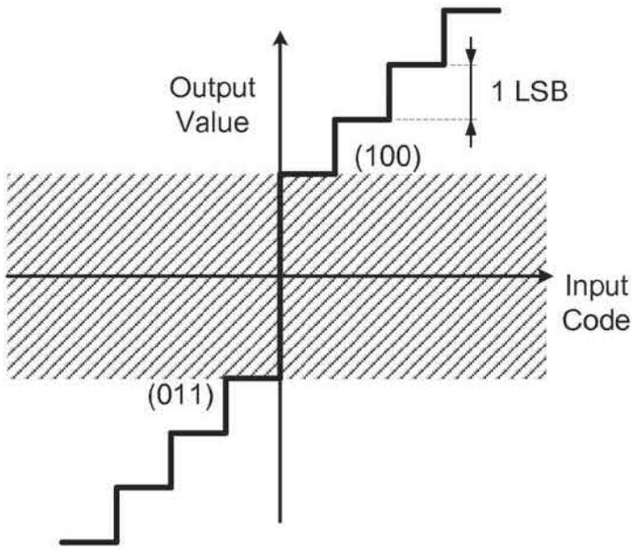

Output
Value
1 LSB
(100)
Input
Code
(011)

Fig. 4

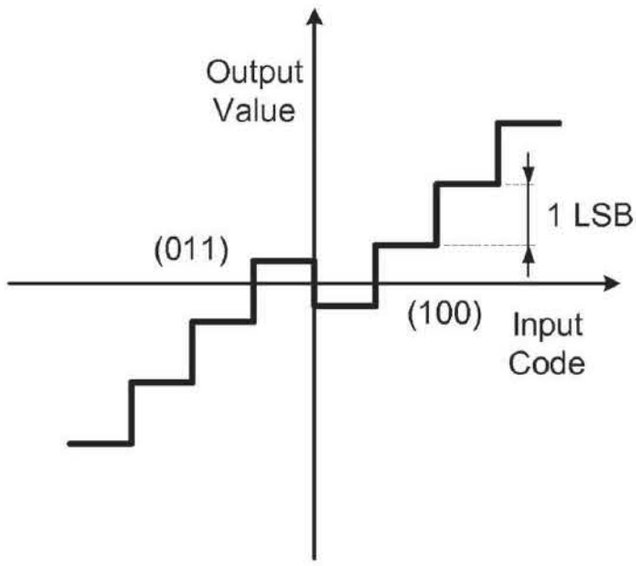

Output
Value
1 LSB
(011)
(100)
Input
Code

Fig. 5

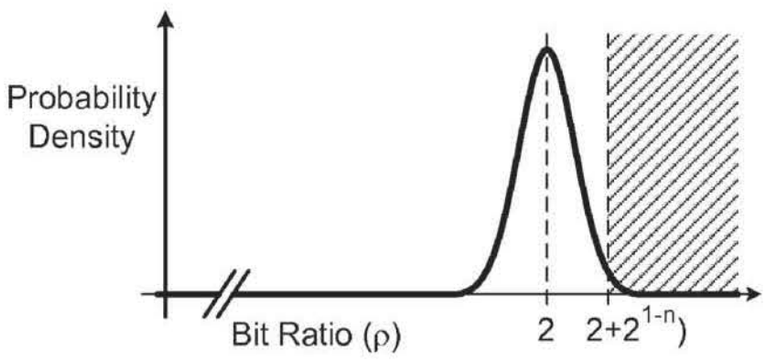

Probability
Density
Bit Ratio (ρ)
2
2+2^1-n)

Fig. 6

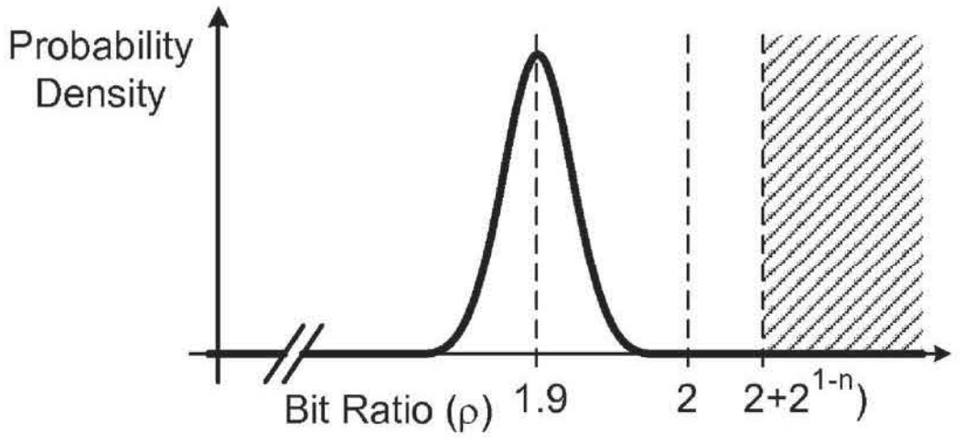


Fig. 7

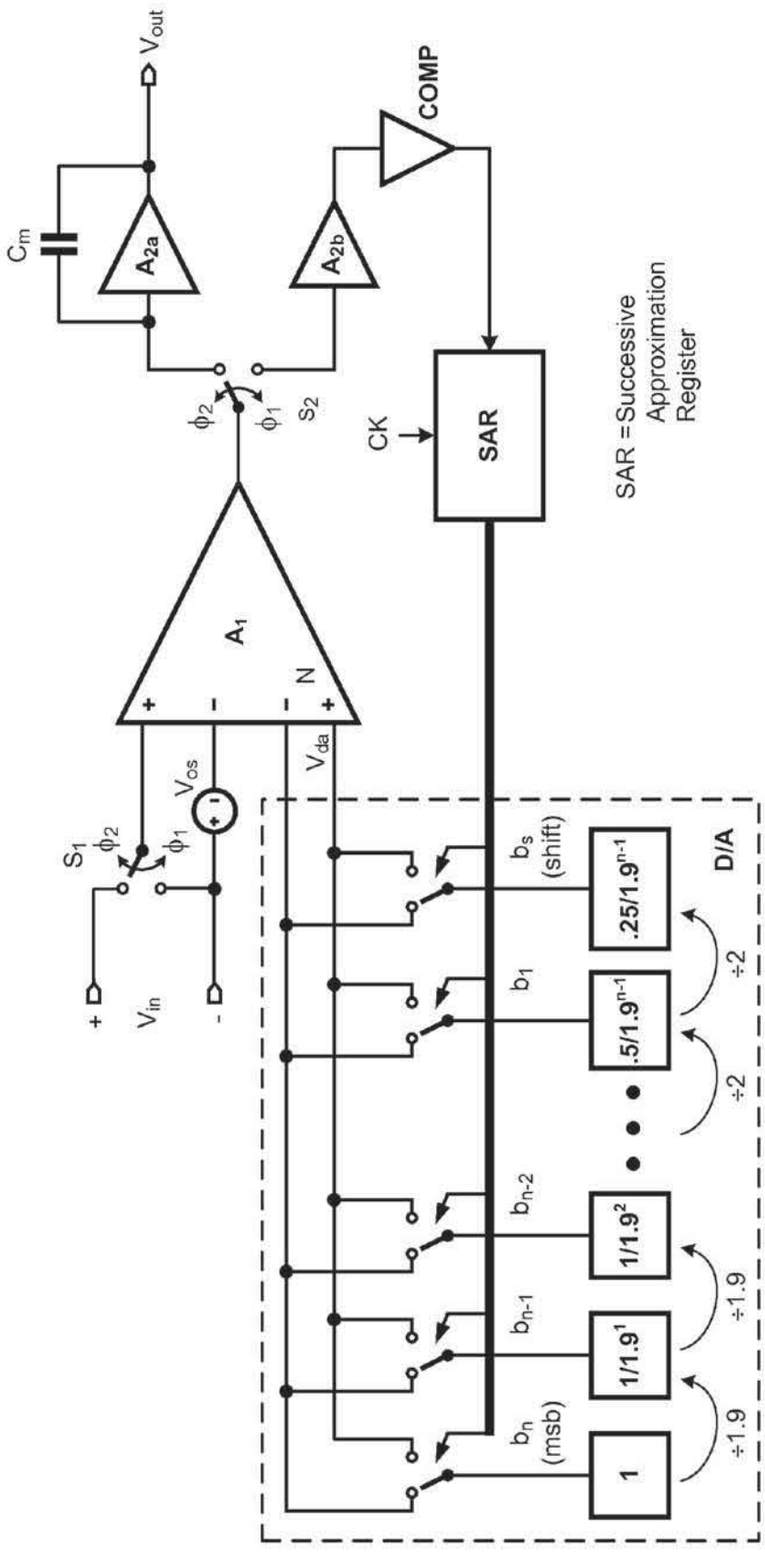

V_{out}
COMP
C_m
A_{2a}
A_{2b}
ϕ_2
ϕ_1
S_2
CK
SAR
SAR = Successive Approximation Register
A_1
N
V_{os}
V_{da}
S_1
V_{in}
b_s (shift)
b_1
b_{n-2}
b_{n-1}
b_n (msb)
$.25/1.9^{n-1}$
$.5/1.9^{n-1}$
$1/1.9^2$
$1/1.9^1$
1
÷2
÷1.9
D/A

Fig. 8

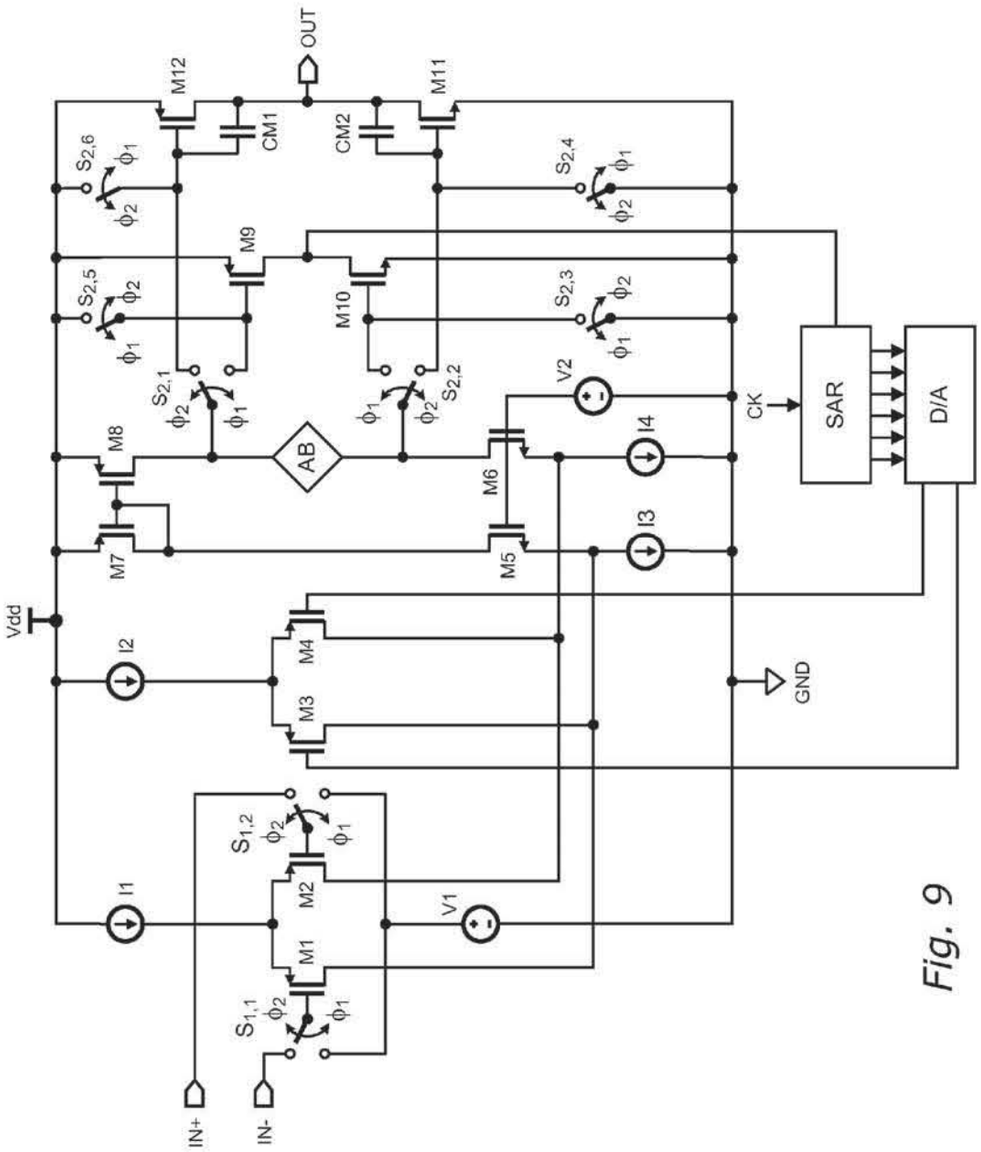

OUT
M12
M11
CM1
CM2
S2,6
S2,4
M9
M10
S2,5
S2,3
S2,1
S2,2
V2
CK
SAR
D/A
M8
AB
M6
I4
M7
M5
I3
Vdd
I2
M4
M3
GND
S1,2
I1
M2
V1
M1
S1,1
IN+
IN-

Fig. 9

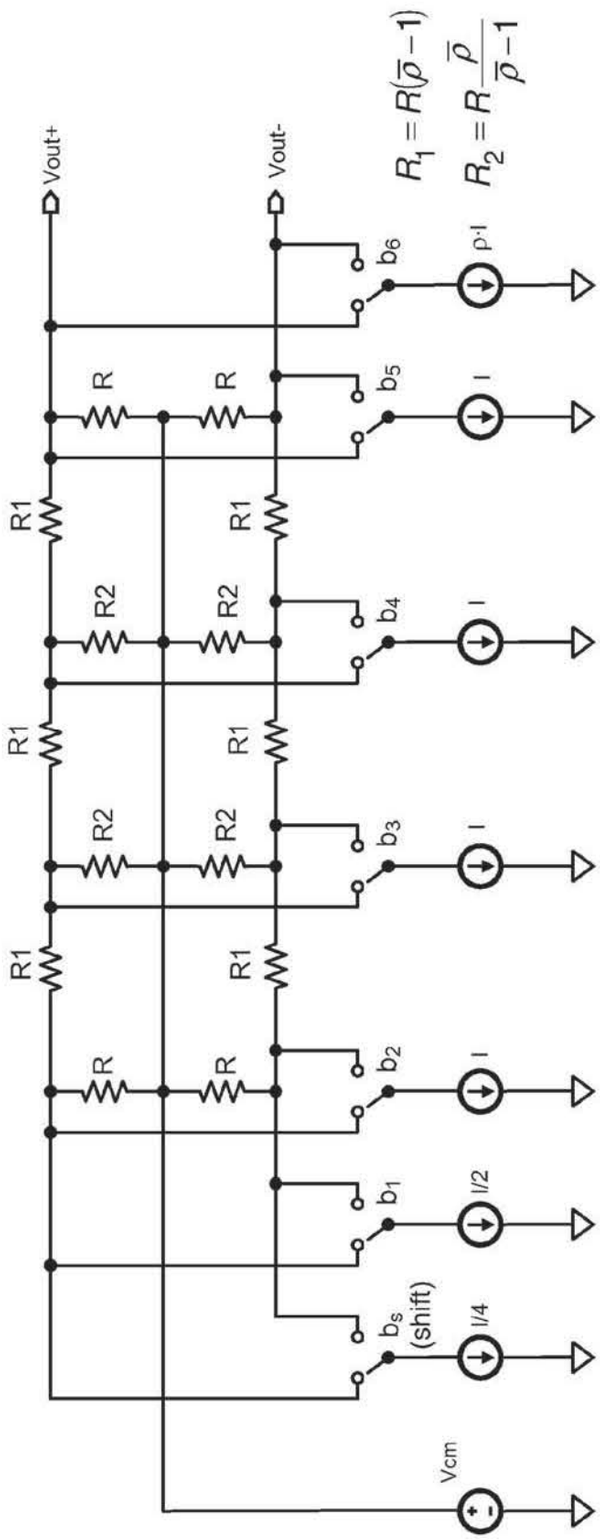

Vout+
Vout-
$R_1 = R(\bar{\rho} - 1)$
$R_2 = R\frac{\bar{\rho}}{\bar{\rho} - 1}$
R
R1
R2
b6
b5
b4
b3
b2
b1
bs
(shift)
ρ·I
I
I/2
I/4
Vcm

Fig. 10

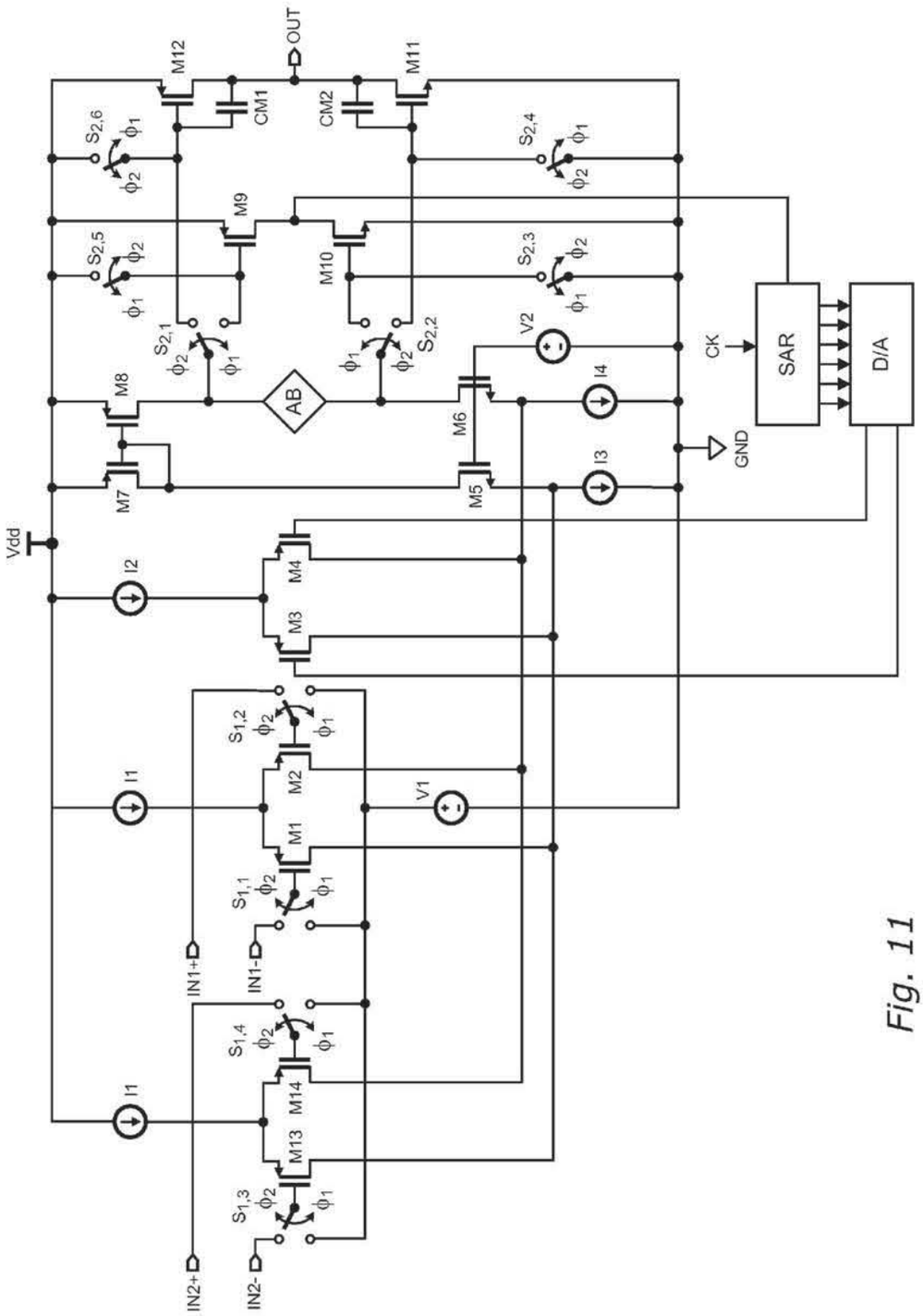

OUT
M12
M11
CM1
CM2
M9
M10
M8
M7
M6
M5
M4
M3
M2
M1
M14
M13
AB
V1
V2
I1
I2
I3
I4
Vdd
GND
CK
SAR
D/A
IN1+
IN1-
IN2+
IN2-
S2,6
S2,5
S2,4
S2,3
S2,1
S2,2
S1,2
S1,1
S1,4
S1,3
ϕ1
ϕ2

Fig. 11

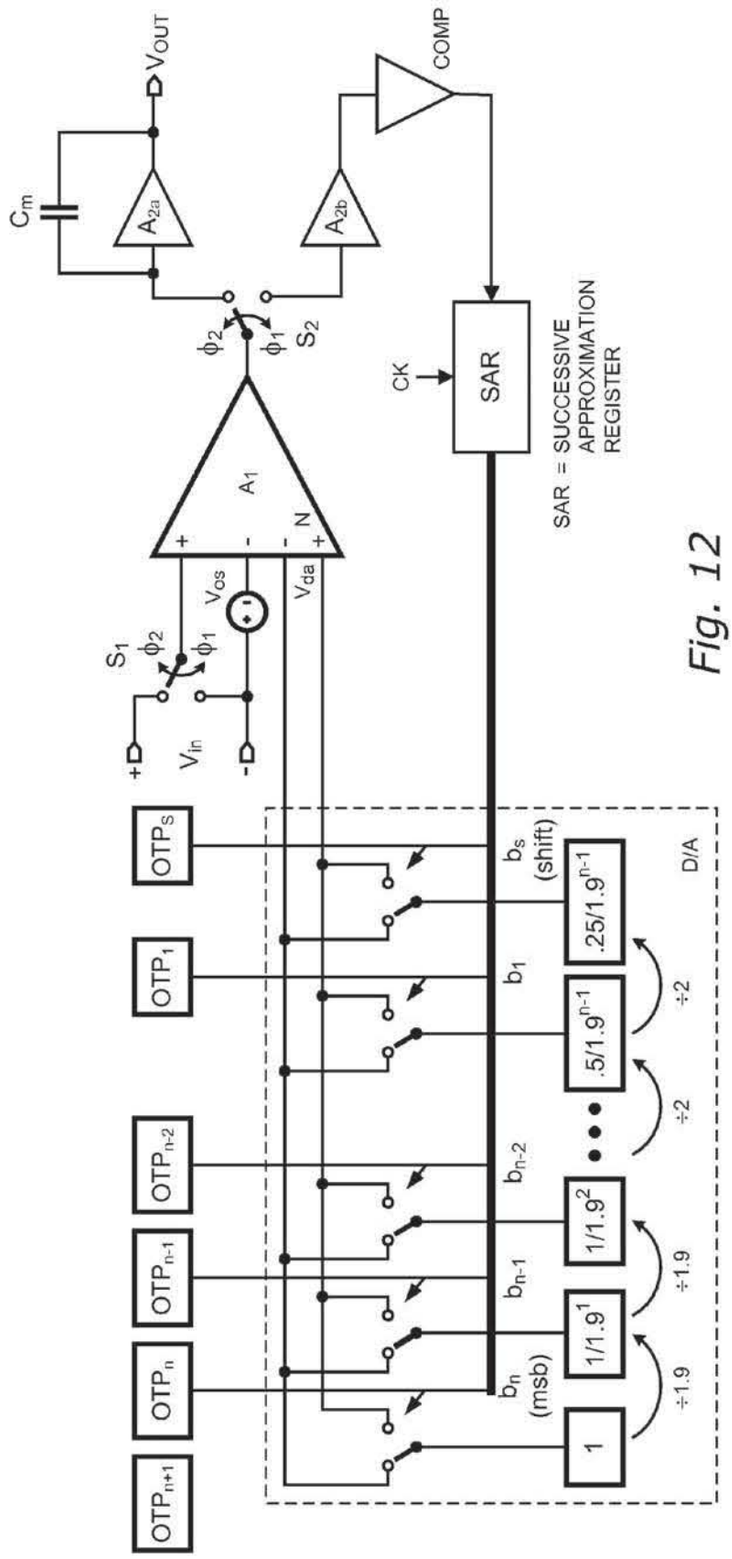

VOUT
COMP
Cm
A2a
A2b
ϕ2
ϕ1
S2
CK
SAR
SAR = SUCCESSIVE APPROXIMATION REGISTER
A1
N
Vos
Vda
S1
Vin
+
-
OTPS
OTP1
OTPn-2
OTPn-1
OTPn
OTPn+1
bs (shift)
b1
bn-2
bn-1
bn (msb)
.25/1.9n-1
.5/1.9n-1
1/1.92
1/1.91
1
÷2
÷2
÷1.9
÷1.9
D/A

Fig. 12

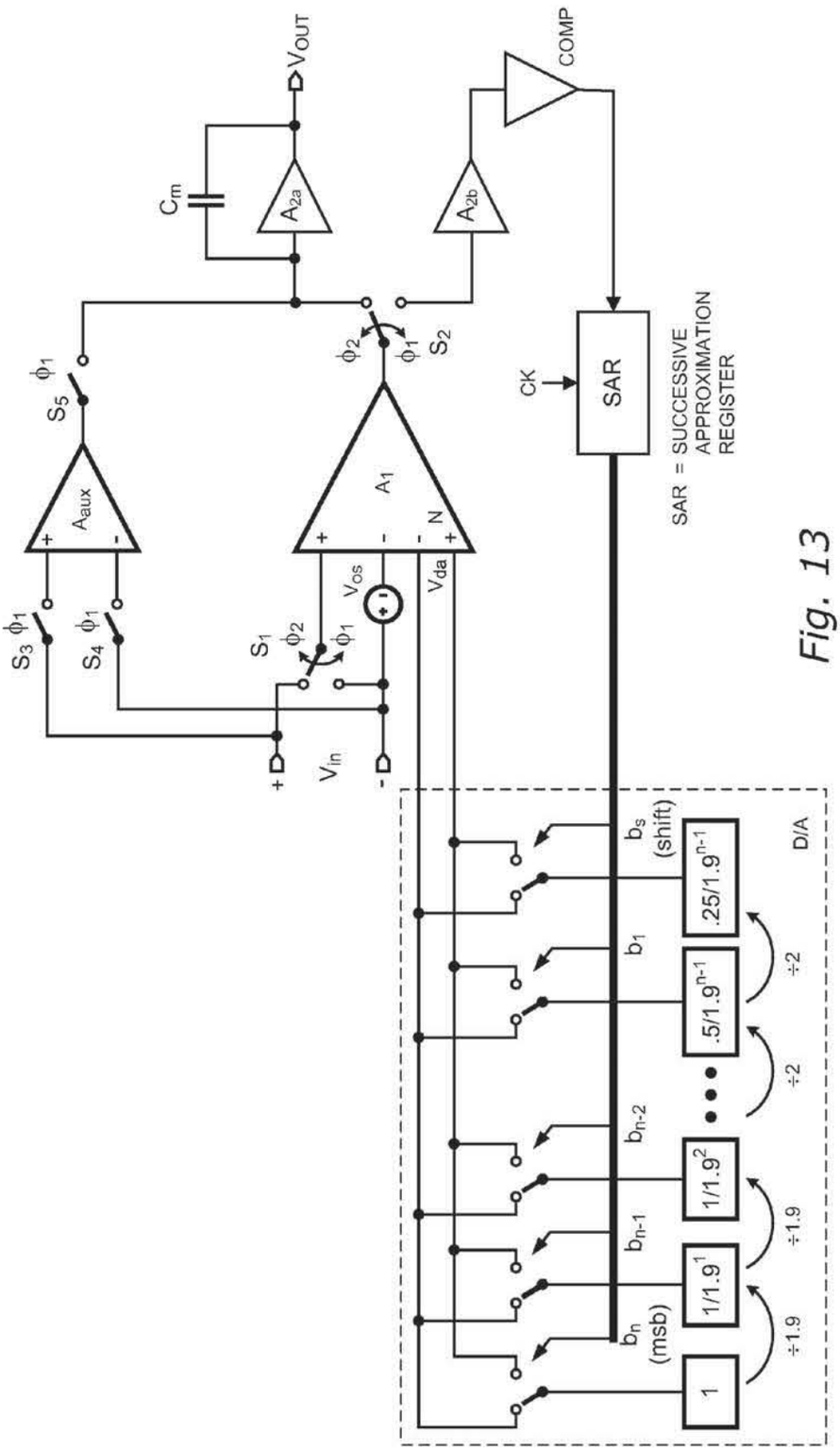

VOUT
COMP
Cm
A2a
A2b
S2
S5
Aaux
A1
N
CK
SAR
SAR = SUCCESSIVE APPROXIMATION REGISTER
S3
S4
S1
Vos
Vda
Vin
bs (shift)
b1
bn-2
bn-1
bn (msb)
.25/1.9n-1
.5/1.9n-1
1/1.92
1/1.91
1
÷2
÷1.9
D/A

Fig. 13

AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of operational and instrumentation amplifiers.

2. Prior Art

One of the key performance specifications of an operational amplifier is its DC error or offset voltage. The offset voltage limits the ability of the amplifier to resolve small DC input voltages. The total offset voltage is usually specified assuming a single source of error at the input terminals. The value of this imaginary voltage source represents the input referred offset voltage of the amplifier. The significance of this parameter lies in the fact that the amplifier will not be able to resolve any DC voltages at its input that are smaller than the input referred offset voltage.

In monolithically integrated operational amplifiers, the input referred offset voltage (also called input offset, offset voltage or just offset for short) is mostly due to statistical mismatch between critical components in the circuit. Commonly, these critical components include the input stage transistors, but other devices may contribute significantly to the offset as well. Typical offset voltages due to component mismatch lay in the order of several millivolts.

A well-known technique to reduce the input referred offset voltage of an amplifier is by trimming each amplifier during manufacturing. At some stage in the production process—usually while electrically screening the parts for defects—the native offset of the part is measured, and corresponding modifications are made to the part to compensate for this offset. The modifications to the part need to be permanent, in order for the offset to remain compensated for over the life of the product.

Many techniques have been proposed and used in the past to make permanent changes to an IC in order to store the offset compensation voltage. Examples include trimming resistors with a laser, blowing links with a laser, shorting out zener diodes by a high reverse voltage, blowing metal fuses with a high current, modifying the resistivity of a poly-silicon resistor with a high current and storing digital bits onto a non-volatile memory (e.g. flash).

Based on the timing of the trimming during the production process, all trimming techniques can be classified into one of two categories:

1. pre-package trim
2. post-package trim

As the name implies, pre-package trim includes all trim techniques that take place before the silicon die is packaged into its final package. Reversely, post-package trim is done after packaging the part.

The distinction between pre and post-package trim is a critical one, since the packaging process can lead to significant offset shifts of the part. Especially plastic packages, which include the majority of all parts being shipped today, can inflict high mechanical stresses to the silicon die. The piezoelectric properties of silicon convert the mechanical stresses into offset voltage shifts of the circuit. These offset shifts in their turn cause the input referred offset voltage of the part to change randomly after packaging. Typical offset shifts due to packaging are on the order of several 100s of microvolts.

A part that was trimmed for zero offset before packaging (pre-package trim), will most likely show a non-zero offset after being assembled. Therefore, pre-package trim is not able to guarantee very high accuracies of the trimmed offset voltage.

Post-package trim, on the other hand, takes into account offset shift due to packaging and will compensate for it. Very high trim accuracies can be achieved this way.

Despite its high end-accuracy, there are two main disadvantages associated with post-package trim. The first disadvantage of post-package trim is the need for some sort of on-die non-volatile memory. Most process technologies used for fabricating operational amplifiers do not offer non-volatile memory, and if they do, bit cells tend to be not very area-efficient.

The second disadvantage is the need to offer means to externally control the trim state and store the offset compensation value. In many cases this will require the addition of pins to the package, and increase cost. Alternatively, the part can employ some sophisticated multiplex approach to reuse the existing pins for controlling the offset trim algorithm. Such setup requires complex circuitry, however, adding to the die size and cost.

An approach to post-package trim that does not require non-volatile memory and external control of the trim algorithm is so-called power-on calibration. Using this technique, the part is not trimmed during manufacturing, but instead each time the part is powered up (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", C. C. Enz and G. C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, November 1996, pp. 1584-1614 and "A high-performance autozeroed CMOS opamp with 50 μV offset", Krummenacher et al., Solid-State Circuits Conference, 1997, Digest of Technical Papers, pp. 350-351, 483). Since the stored offset compensation value needs to be retained only while the supply power is available, power-on calibration alleviates the need for non-volatile memory. Instead, volatile memory can be used. This type of memory offers small die size, and it is ubiquitously available in any CMOS process technology in the form of flip-flops.

FIG. **1** shows the block diagram of an amplifier with power-on calibration.

It uses the successive approximation algorithm to cancel out the random input referred offset voltage V_{os}. Offset calibration of amplifier A is achieved through switch S, comparator COMP, the successive approximation state-machine SAR and finally the digital-to-analog converter D/A that feeds an offset correction voltage to amplifier A. When the amplifier is powered on, switch S is closed. This forces a differential input voltage that is equal to the input referred offset voltage V_{os} at the input of amplifier A. Since there is no feedback, the amplifier A operates in the comparator mode: if the differential input voltage is greater than zero, its output will jump to the positive rail, and vice verse (assuming the offset correction voltage at port N is zero).

FIG. **2** shows a simplified representation of the amplifier circuit in FIG. **1** during calibration.

While calibrating, the input switch in FIG. **1** connects the offset source V_{os} between the two differential inputs of amplifier A. This is represented by the offset source V_{os} in FIG. **2**. Since the D/A output voltage V_{da} drives offset compensation port N on amplifier A_1 in FIG. **1**, the effect of V_{da} can be thought of as being subtracted from the offset voltage V_{os} at the input of the amplifier. This is indicated in FIG. **2** by the plus sign for the voltage V_{os}, and the minus sign for the voltage V_{da}. The difference between offset voltage V_{os} and correction voltage V_{da} is error voltage ϵ. The sign of the error

voltage ϵ, through amplifier A and comparator COMP, drives the decisions of the successive approximation algorithm.

After power-up the circuit will start its successive approximation state-machine to find a value for the offset correction voltage V_{da} at the secondary input N that minimizes the input referred offset voltage of the overall circuit. The successive approximation operates as follows (see Analog-To-Digital and Digital-To-Analog Converters, R. J. van de Plassche, Springer, 1994). The circuit starts off with all bits to the digital-to-analog converter D/A set to zero. This causes the most negative voltage V_{da} to be set on the offset compensation input N. If the offset compensation range is large enough, this negative voltage will always cause the output of amplifier A to trip high (E>0). In the next cycle, the most significant bit (MSB or b_n) of D/A will be tested high. If this causes the output of A to go low (ϵ<0), the bit will be returned to its low state before proceeding to the next bit. Otherwise, if the output of A does not change due to setting the MSB (ϵ>0), the bit will remain high. The state of the MSB will be stored into a register and does not change during the remainder of the calibration process. In the following step, the bit below the MSB (b_{n-1}) will be tested high and the resulting bit value stored into the register. This process continues successively through all bits, high to low, until the least significant bit is tested and its value stored.

Table 1 shows an example of the offset calibration procedure for a 3-bits SAR register in the simple case that the offset voltage V_{os} is zero.

TABLE 1

Example of the successive approximation algorithm, assuming Vos = 0

Step	b_3 (±1 V)	b_2 (±0.5 V)	b_1 (±0.25 V)	V_{da} [V]	ϵ [V] (V_{os} − V_{da})	Comment
0	0	0	0	−1.75	+1.75	Initial State
1	1	0	0	+0.25	−0.25	ϵ < 0, b_2 = 0
2	0	1	0	−0.75	+0.75	ϵ > 0, b_1 = 1
3	0	1	1	−0.25	+0.25	ϵ > 0, b_0 = 1
4	0	1	1	−0.25	+0.25	Final State

The table assumes that the MSB b_3 switches between the values −1V (bit low) and +1V (bit high). The other bits are binary weighted, such that b_2=±0.5V and b_1=±0.25V. Bits tested by the algorithm are underlined. The error value ϵ in the example of Table 1 approaches zero within the step size of one LSB (0.5V). The resulting binary code is (011) (see the bottom row).

Table 2 gives a similar example of the successive approximation algorithm, now assuming that the input offset voltage Vos is 1.6V. In this case the bits converge to the code (110), with a remaining error ϵ of 0.35V, which is again within one LSB step size.

TABLE 2

Example of the successive approximation algorithm, assuming Vos = 1.6

Step	b_3 (±1 V)	b_2 (±0.5 V)	b_1 (±0.25 V)	V_{da} [V]	ϵ [V] (V_{os} − V_{da})	Comment
0	0	0	0	−1.75	+3.35	Initial State
1	1	0	0	+0.25	+1.35	ϵ > 0, b_2 = 1
2	1	1	0	+1.25	+0.35	ϵ > 0, b_1 = 1
3	1	1	1	+1.75	−0.15	ϵ < 0, b_0 = 0
4	1	1	0	+1.25	+0.35	Final State

Notice how in the examples in Table 1 and Table 2 the remaining output error ϵ is always greater than zero. This is a property of the successive approximation algorithm: if a particular bit is tested high and the error voltage ϵ becomes smaller than zero, the bit is reset to zero. As a result, the algorithm does not allow the error ϵ to become negative.

In fact, the distribution of the error ϵ is between zero and one LSB step size S_{lsb}. Ideally, we would like to see the error centered around zero. Doing so will half the maximum error ϵfrom +1 S_{lsb} to ±½ S_{lsb}. In order to perform the re-centering, we will need to add a value equal to ½ S_{lsb}, to the D/A converter voltage V_{da} after the calibration completes. The shift of the final D/A converter voltage V_{da} can be achieved by adding one more bit to the D/A converter, below the least significant bit b_1 (LSB). This additional bit is held at zero during the calibration process, and subsequently set to one, once the calibration is done. Table 3 illustrates the addition of a shift bit to the algorithm.

TABLE 3

Example of the successive approximation algorithm with a shift bit, assuming Vos = 1.6

Step	b_3 (±1 V)	b_2 (±0.5 V)	b_1 (±0.25 V)	b_s (±0.125 V)	V_{da} [V]	ϵ [V] (V_{os} − V_{da})	Comment
0	0	0	0	0	−1.875	+3.475	Initial State
1	1	0	0	0	+0.125	+1.475	ϵ > 0, b_2 = 1
2	1	1	0	0	+1.125	+0.475	ϵ > 0, b_1 = 1
3	1	1	1	0	+1.625	−0.025	ϵ < 0, b_0 = 0
4	1	1	0	1	+1.375	+0.225	Final State

In this example, the error ϵ in the final state is 0.225V (bottom row), which is less than half an LSB step size (0.25V).

Even though the successive approximation algorithm is very powerful in calibrating out the offset of an amplifier at power-up, it suffers from a major drawback. In order for the algorithm to be able to guarantee a certain end-accuracy of the calibration, matching of the various components in the D/A converter needs to be extremely tight. Especially matching of the MSB step size S_{msb}, to the other bits turns out to be critical. The matching error of the MSB step size S_{msb}, must be significantly less than one LSB step size S_{lsb}, in order for the mismatch not to affect the overall accuracy appreciably:

$$\Delta S_{msb} \ll S_{lsb} \tag{1}$$

This can be rewritten as

$$\frac{\Delta S_{msb}}{S_{msb}} \ll \frac{S_{lsb}}{S_{msb}} = \frac{1}{2^{n-1}} \tag{2}$$

where n equals the number of bits of the D/A converter.

Accepting a maximum error due to mismatch of the MSB equal to half an LSB step size ½ S_{lsb}, the expression for the maximum matching error of the MSB simplifies to

$$\frac{\Delta S_{msb}}{S_{msb}} \leq 2^{-n} \tag{3}$$

Similar constraints as for the MSB on the maximum matching error occur for the other bits of the A/D converter, albeit with progressively looser matching requirements. The

step size of the bits becomes smaller by a factor two for each step when going from the MSB to the LSB. Therefore the expression for the maximum matching error of individual bits becomes

$$\frac{\Delta S_b}{S_b} \le 2^{-b} \tag{4}$$

where b equals the bit number (b=n for the MSB, b=1 for the LSB).

Clearly, matching of the MSB will be the most critical.

To illustrate the effect of mismatch on the transfer function of the D/A converter, FIG. **3** shows an example of the output voltage vs. input code of a 3-bit converter without any mismatch error.

The output steps through all eight possible output values with even step sizes as the input code progresses from (000) through (111). The ideal D/A converter of FIG. **3** can generate any voltage needed to compensate for the offset of the overall amplifier within half an LSB step size (½ S_{lsb}).

FIG. **4** shows the transfer function of the same D/A converter, now assuming a mismatch error that causes the MSB step size to be too large.

Note how the output voltage jumps when the input code goes from (011) to (100). This is because during this transition, the MSB is switched on. Turning on the MSB is supposed to almost make up for all other bits switching off, leaving a positive difference of 1 LSB step size S_{lsb} between the output levels for codes (011) and (100). Since in this example the MSB step size S_{msb}, is too large, the MSB overcompensates for the other bits switching off, causing the difference between the two levels to be too large. This creates a gap between the output voltage levels for input codes (011) and (100).

The hatched area is a range of output voltages that is not covered by the D/A converter. If the voltage V_{da} that is needed to compensate for the offset of the overall amplifier falls somewhere in the middle of the hatched voltage range, the offset voltage most likely cannot be corrected for within half an LSB step size, or ½ S_{lsb}.

When matching errors cause the MSB step size S_{msb} to be too small, we obtain a D/A response similar to FIG. **5**. The transfer function is not monotonic anymore and has a slightly reduced dynamic range compared to the ideal case of FIG. **3**.

Despite these two factors, all output voltages within the dynamic range of the converter can now be produced within half an LSB step size (½ S_{lsb}). In other words, despite the MSB mismatch error, we can continue to guarantee that any offset voltage of the overall amplifier can be compensated for within ½ S_{lsb}. Note that monotonicity of the D/A transfer function is not required for the successive approximation algorithm to function properly.

Summarizing the effects of MSB mismatch on the successive approximation algorithm, we find the following:

1. A mismatch error that causes the MSB to be too large will deteriorate the worst-case offset voltage of the overall amplifier after calibration.

2. A mismatch error that causes the MSB to be too small does not significantly affect the overall accuracy of the offset calibration.

FIG. **6** illustrates this conclusion.

On the x-axis, it shows the ratio between the value of the MSB b_n and the next bit b_{n-1} (bit ratio ρ), while the y-axis represents the probability of a certain bit ratio ρ. Ideally, the bit ratio ρ is 2 (MSB b_n twice as large as the next bit b_{n-1}). Due to mismatch between the components used to manufacture the circuit, the actual bit ratio ρ will vary around the mean value of 2 with a normal distribution having standard deviation σ_ρ. In order to make sure that the overall error due to component mismatches does not exceed half an LSB step size (½ S_{lsb}), the bit ratio ρ should not be too large.

The relation between the error Δρ of the bit ratio ρ and the mismatch $\Delta S_n/S_n$ of the MSB step size can be found as follows

$$S_n = 2 \cdot S_{n-1} \tag{5}$$

$$S_n + \Delta S_n = (2 + \Delta\rho) \cdot S_{n-1} \Rightarrow$$

$$\frac{\Delta S_n}{S_n} = \frac{\Delta\rho \cdot S_{n-1}}{S_n} = \frac{\Delta\rho}{2}$$

Using Eq. 3 and Eq. 5, we can now find for the maximum allowed error $\Delta\rho_{max}$

$$\Delta\rho_{max} = 2 \cdot 2^{-n} \tag{6}$$

From Eq. 6 we can find the expression for the maximum acceptable absolute value of the bit ratio ρ_{max}

$$\rho_{max} = \bar{\rho} + \Delta\rho_{max} = 2 + 2^{1-n} \tag{7}$$

where $\bar{\rho}$ is the mean or targeted bit ratio

The hatched area in FIG. **6** indicates the forbidden range of bit ratios ρ. Values of the bit ratio ρ that lie above $2+2^{1-n}$, indicated by the dashed line, lead to the calibration of the overall circuit potentially being out of spec (point **1** above), whereas any value of the bit ratio ρ below this limit guarantees a calibrated offset within the specifications (see point **2** above).

Based on Eq. 7, we can determine the maximum matching error of the bit ratio

$$\frac{\Delta\rho_{max}}{\bar{\rho}} = 2^{-n} \tag{8}$$

Note how the maximum acceptable matching error $\Delta\rho_{max}/\bar{\rho}$ goes down exponentially with the number of bits. Especially with high bit counts, this can result in very tight matching requirements.

Considering n=10 bits as an example, the maximum allowable mismatch error of the bit ratio $\Delta\rho_{max}/\bar{\rho}$ equals 2^{-10}, or about 0.1% (Eq. 8). Requiring this to be a 6σ limit (probability of exceeding the spec limit smaller than ~1 ppb, assuming a normal distribution), means the standard deviation of the MSB bit ratio matching σ_ρ must be smaller than 0.016%.

The matching requirements that follow from Eq. 8 are often very hard—if not impossible—to achieve in practical monolithically integrated circuits. Therefore, current state-of the art amplifiers with power-on calibration rely heavily on production screening of all possible D/A output levels to guarantee that the input referred offset will be within specs across wide ranges of operating conditions. Due to the large number of possible output levels (1024 for n=10), this production screening is both time-consuming and costly.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a prior art amplifier with power-on calibration.

FIG. **2** shows a prior art power-on calibrated amplifier in calibration mode.

FIG. **3** shows an ideal 3-bit D/A transfer function.

FIG. **4** shows a 3-bit D/A converter transfer curve: MSB too large.

FIG. **5** shows a 3-bit D/A converter transfer curve: MSB too small.

FIG. **6** shows the probability-density function of the bit ratio ρ of a SA D/A converter.

FIG. **7** shows the probability-density function of the bit ratio ρ for the proposed calibration circuit.

FIG. **8** shows a preferred embodiment of power-on calibration using a non-binary weighted D/A converter.

FIG. **9** is a simplified example of the circuit implementation of the proposed invention.

FIG. **10** shows an example of the circuit implementation of the non-binary weighted A/D converter.

FIG. **11** shows an example of an instrumentation amplifier with power-on calibration.

FIG. **12** presents an exemplary configuration to trim at production, while storing the results in one-time programmable memory.

FIG. **13** shows the addition of an auxiliary amplifier to control the output during calibration.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Traditional successive approximation approaches to power-on calibration lead to excessively tight matching specifications of the D/A converter components. The present invention proposes a method to relax the matching requirements. Allowing for more variation will greatly improve the manufacturability of power-on calibration circuits.

The key to improving the robustness of the power-on calibration lays in the use of a targeted bit ratio $\bar{\rho}$ that is smaller than the traditional $\bar{\rho}$=2. Note from FIG. **6** and Eq. 7 that any ratio ρ below $2+2^{1-n}$ (with a practical under limit of ρ=1) guarantees the accuracy of the calibration. By choosing a target bit ratio $\bar{\rho}$ less than 2, meeting the limit set by Eq. 7 becomes progressively easier.

This is illustrated by FIG. **7**.

This plot again shows the probability density function of the bit ratio ρ between the MSB b_n and the adjacent bit b_{n-1}, assuming a normal distribution. The maximally allowable ratio ρ that guarantees proper calibration of the amplifier's offset is indicated by the dashed line at $\rho_{max}=2+2^{1-n}$. The hatched area indicates "forbidden" values for the ratio ρ. The main difference between the prior-art plot in FIG. **6** and the plot of FIG. **7** is that the bit ratio is now centered around a value that is slightly smaller than the traditional value of 2. FIG. **7** uses a mean bit ratio of $\bar{\rho}$=1.9 as an example.

A consequence of choosing a smaller mean bit ratio is that the peak of the probability density function moves away from the upper limit. A greater distance between the peak and the upper limit suggests it will be easier to meet the spec in production. This can be quantified as follows. The difference between the mean of the bit ratio $\bar{\rho}$ and the spec limit ρ_{max} is given by

$$\rho_{max}-\bar{\rho}=2+2^{1-n}-\bar{\rho} \tag{9}$$

Since the number of bits n>>1 in most practical cases, this reduces to

$$\rho_{max}-\bar{\rho}2-\bar{\rho} \tag{10}$$

The matching requirement for the bit ratio ρ now becomes

$$\frac{\Delta\rho_{max}}{\bar{\rho}} \approx \frac{2-\bar{\rho}}{\bar{\rho}} \approx \frac{2-\bar{\rho}}{2} \tag{11}$$

The right hand side of Eq. 11 assumes the target bit ratio $\bar{\rho}$. is close to 2.

Note that the matching requirement that follows from Eq. 11 is independent of the total number of bits. In the prior-art case of $\bar{\rho}$=2 (binary weighted), the matching spec became exponentially tighter with a rising number of bits (Eq. 8).

By substituting our example of $\bar{\rho}$=1.9 into Eq. 11, we find the maximum allowable mismatch of the bit ratio as 5%. Again requiring a 6σ limit, this leads to a maximum standard deviation of the mismatch of the MSB bit ratio σ_ρ equal to 0.8%. This is much looser than the 0.016% of the binary weighted prior art example. In fact, matching ratios on the order of 0.8% can routinely be realized in standard manufacturing processes without the need for additional trimming or production testing.

FIG. **8** shows the preferred embodiment of the proposed invention.

It consists of amplifier input stage A_1, and the two selectable output stages A_{1a} and A_{1b}. Power-on offset calibration is performed through the comparator COMP, the successive approximation register SAR and a non-binary weighted D/A converter. The D/A converter comprises the switches b_n through b_s, and the non-binary weighted bit values 1 through $1/1.9^{n-2}$, plus binary weighted values for the least significant bit controlled by switch b_1 and the shift bit b_s. At power up of the circuit, the input switch S_1 shorts out the inputs to the amplifier input stage A_1. As a result, the input referred offset voltage V_{os} will be present between its differential input terminals. Output switch S_2 connects the input stage A_1 to the secondary output stage A_{2b}. Because of its connection to the secondary output stage A_{2b}, the comparator COMP can now drive the decisions of the successive approximation algorithm implemented by the register SAR. The least significant bit is given a binary weighting because of the fact that any error in that weighting does not cause an error that must be made up by subsequent bits, and the shift bit is given a binary weighting relative to the least significant bit as its purpose is to compensate for one half the least significant bit to cause the error ε to be centered around zero instead of always being on one side of zero, thereby cutting the maximum error in half.

Once the power-on offset calibration completes, switch S_1 connects the input terminals of the overall amplifier to the input stage A_1, while switch S_2 activates output stage A_{2a}. Also, the SAR register activates the shift bit b_s. Note that the ratio between the LSB b_1 and the shift bit b_s remains two, even if all other bits are non-binary weighted. The amplifier is now in its normal mode of operation, with the register SAR holding a digital code that corresponds to a voltage V_{da} that (mostly) compensates for the input referred offset V_{os}.

Even though the use of the two selectable output stages A_{2a} and A_{2b}, along with output switch S_2 is not necessarily required for the invention to work properly, this setup has several key advantages over using a single output stage for both calibration and normal mode. First of all, selecting between the two output stages will prevent spurious signals or glitches to appear at the output terminal of the amplifier while the amplifier is being calibrated. A second benefit of duplicating the output stage is that the secondary output stage A_{2b} can now be implemented without the addition of a compen-

sation capacitor for closed loop stability. Frequency compensation capacitor C_m is required during normal operation to ensure stability of the amplifier with overall feedback. Since the amplifier is operated in an open-loop comparator mode during power-on calibration, no frequency compensation is needed. Leaving out the compensation capacitor speeds up the decisions during the successive approximation procedure, reducing the total time spent in calibration mode.

As an alternative to a power-up event, the calibration sequence can also be initiated by any other trigger. In that case, the system performs on-demand-calibration as opposed to power-on calibration as described before.

FIG. **9** shows a simplified example of a circuit implementation of the present invention.

It consists of the transconductance input stage with transistors M_1 and M_2. The gates of these devices are connected to switches $S_{1,1}$ and $S_{1,2}$. In normal mode, the switches directly connect the gates of M_1 and M_2 to the input terminals IN+ and IN−. During calibration, the inputs are shorted out and connected to the reference common-mode voltage V_1. Devices M_5 through M_8 implement a traditional folded cascode turn-around stage. The first or primary output stage used for normal operation comprises the devices M_{11} and M_{12}, together with frequency compensation capacitors C_{M1} and C_{M2}. The secondary output stage used during calibration includes devices M_9 and M_{10}. This secondary output stage does not require any frequency compensation components, since it will only be used in comparator mode. Switches $S_{2,1}$ and $S_{2,2}$ select between the two output stages. The block AB implements class-AB quiescent current control of the output stage devices (either M_{11} and M_{12}, or M_9 and M_{10}, depending on the states of $S_{2,1}$ and $S_{2,2}$). When the primary output state M**11** and M**12** is selected, switches $S_{2,3}$ and $S_{2,5}$ are closed, putting the secondary output stage in a high output impedance state, and when the secondary output state M**9** and M**10** is selected, switches $S_{2,4}$ and $S_{2,6}$ are closed, putting the primary output stage in a high output impedance state.

The parallel input stage M_3/M_4 implements the offset control input. A differential voltage between the gates of M_3 and M_4 will cause a differential output current at their drains. This differential drain current flows in parallel to the drain current of the input stage M_1/M_2. A suitable differential voltage at the gates of M_3 and M_4 can compensate for a random offset of the input stage M_1/M_2. Since the range of offset voltages that the parallel input stage needs to compensate for is much smaller than the expected signal swing at the input of the amplifier, the tail current I_2 through devices M_3 and M_4 can be chosen smaller than the bias current of the input stage I_1.

The register SAR and the non-binary weighted D/A converter D/A implement the successive approximation algorithm as before.

FIG. **10** shows an example of a 6-bit implementation of the non-binary weighted D/A converter.

It consists of a three-section differential resistive ladder with resistor values R, R_1 and R_2. The common-mode voltage of the ladder is set by voltage source V_{cm}. Note that this voltage is not related to any common mode voltage of an input signal IN+,IN−, as the transistors M**3** and M**4** operate in a differential mode to control the division of the current I**2** (FIG. **9**), independent of the operation of the differential input stage transistors M**1** and M**2**. The switches b_s through b_6 steer the currents from the bottom current sources to either side of the differential ladder, depending on the states of the input bits. In this example, the weighting of the bits b_2 through b_4 is done through the resistive ladder, while weighting of b_s, b_1 and b_6 is implemented through scaling of the respective current sources. This choice is arbitrary, and not critical to the operation of the circuit.

Targeting a bit ratio of $\bar{\rho}$, the values of the resistors can be found as follows

$$R_1 = R \cdot (\bar{\rho} - 1) \tag{12}$$

$$R_2 = R \cdot \frac{\bar{\rho}}{\bar{\rho} - 1}$$

where R is the characteristic impedance of the ladder.

Note how choosing a bit ratio $\bar{\rho}$=2 (standard binary weighing) transforms the D/A converter of FIG. **10** into a traditional R-2R ladder (R_1=R, R_2=2R).

By adding an additional input stage to the circuit of FIG. **9**, it can easily be transformed into a so-called instrumentation amplifier (see Operational Amplifiers, Theory and Design, J. Huijsing, pp. 52-53, Boston, Kluwer Academic Publishers, 2001). Instrumentation amplifiers have two sets of differential input terminals and are capable of sensing small differential signals in the presence of a large common-mode disturbance.

In order for the power-on calibration to work properly in the modified circuit, only the input stage devices and the input switches need to be repeated from the original amplifier. The offset calibration can be performed across both input stages combined and therefore does not require any other additional components.

FIG. **11** shows the instrumentation amplifier that results from modifying the circuit depicted in FIG. **9**. The components added to the circuit are the two input stage with M_{13} and AU, along with the corresponding input switches $S_{1,3}$ and $S_{1,4}$, which would be operated simultaneously with $S_{1,1}$ and $S_{1,2}$.

The embodiments shown herein in FIGS. **9** and **11** are MOS embodiments, though other active devices may be used, such as bipolar devices. Also the word switch as used herein and in the claims is used in the general sense, and includes single or multiple switches, as appropriate. When the word switch is used in the context of multiple switches, such multiple switches would be operated substantially simultaneously, though perhaps with a preferred nonoverlapping phasing. By way of example, a switch for switching an input of the amplifier from the amplifier system input to shorting the amplifier input might be a single switch such as switch S in FIG. **1** or two switches $S_{1,1}$ and $S_{1,2}$ in FIG. **9**, or, by way of another example, might be four switches, two for disconnecting the differential input stage from the differential amplifier input, and two to short the input to the differential input stage. In this latter case, one normally would prefer to disconnect the differential amplifier input before shorting the differential input stage, thereby defining a nonoverlapping operation.

Similarly, a reference to an input or an output herein and in the claims is a reference to an input or an output generally, independent of whether the input or output is a single signal relative to a circuit ground, or a differential signal.

The approach of FIG. **8** can be extended to perform one-time calibration during the fabrication of the device. In that case, the circuit requires some form of One-Time-Programmable memory, or OTP, to store the result of the calibration during the life-time of the product. FIG. **12** shows an example.

When the device is powered up for the first time, the circuit will go through its auto-calibration cycle. Once the cycle

completes, the resulting values for the bits b_n through b_s will be stored onto the non-volatile memory OTP. On subsequent power-up events, the stored offset compensation bits will be read from the OTP memory, and used to control the bit switches b_n through b_s. One additional OTP cell OTP_{n+1} is needed to establish the fact that the part has been programmed. This will avoid future attempts at calibrating the offset when the part is powered up in its application.

During auto-calibration, the overall amplifier in FIG. **8** is non-responsive to external signals. This is caused by switches S_1 and S_2 that disconnect the amplifier from the external circuitry. Since the auto-calibration time can be short, disabling the amplifier will not cause issues in many, if not most, applications. In the situations where a controlled output voltage is needed, even during the auto-calibration sequence, the circuit of FIG. **13** brings a solution.

The circuit of FIG. **13** adds an auxiliary amplifier A_{aux} to the base circuit of FIG. **8**, along with the switches S_3 through S_5. When the part is auto-calibrating, the switches S_3 through S_5 are closed, and the auxiliary amplifier A_{aux} and the output stage A_{2a} create a signal path from the input terminals V_{in} to the output V_{out}. Since the calibration time is short, so the auxiliary amplifier will not have enough time to settle to a very high accuracy anyhow, offset and other demands on the auxiliary amplifier can be relaxed compared to the main circuit. As a result, a very simple circuit suffices in most practical cases.

Thus while certain preferred embodiments of the present invention have been disclosed and described herein for purposes of illustration and not for purposes of limitation, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

What is claimed is:

1. An amplifier system having an amplifier system input and an amplifier system output comprising:

a first amplifier;

a comparator;

a successive approximation register having an input coupled to an output of the comparator;

a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;

an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

2. The amplifier system of claim **1** wherein the radix is approximately 1.9.

3. The amplifier system of claim **2** wherein the radix for the least significant bit is 2.

4. The amplifier system of claim **1** wherein the D/A converter further comprises one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits.

5. The amplifier system of claim **1** wherein the first amplifier has a first transconductance differential input stage coupled to the first amplifier input, and wherein the first amplifier is further comprised a second transconductance differential input stage, the outputs of the first and second transconductance differential input stages being coupled in parallel, the output of the D/A converter being coupled to inputs of the second transconductance differential input stage to divide a current source coupled to the second transconductance differential input stage between the differential outputs of the first transconductance differential input stage in a proportion to reduce the input offset of the first amplifier.

6. The amplifier system of claim **5** wherein the first amplifier further comprises an intermediate stage having an input coupled to the parallel connected outputs of the first and second transconductance differential input stages, a first output stage providing the first amplifier output, a second output stage forming the comparator, the second switch for switching an output of the intermediate stage between inputs to the first and second output stages.

7. The amplifier system of claim **6** wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage, and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

8. The amplifier system of claim **6** wherein the first amplifier is further comprised of a third transconductance differential input stage, the outputs of the first, second and third transconductance differential input stages being coupled in parallel, the first switch for shorting the first amplifier input by shorting the differential input to the first transconductance differential input stage and shorting the differential input to the third transconductance differential input stage at the same time.

9. The amplifier system of claim **1** further comprised of One-Time-Programmable memory for permanently storing an output of the successive approximation register, whereby a single output of the D/A converter controlling the input offset of the first amplifier may be permanently maintained.

10. The amplifier system of claim **1** further comprised of a second amplifier, the first switch coupling the amplifier system input to an input of the second amplifier when shorting the input to the first amplifier, the second switch coupling an output of the second amplifier to the amplifier system output when switching the output of the first amplifier from the amplifier system output to an input of the comparator.

11. The amplifier system of claim **1** wherein the D/A converter comprises a common reference line, and at least in part, resistor ladders symmetrical about the common reference line, and third switches for selectively switching equal current sources to ladder nodes on either side of the common reference line responsive to the successive approximation register, the resistor ladders being $R(\rho-1)$,$R\rho/(\rho-1)$ ladders, where ρ is less than 2.

12. The amplifier system of claim **11** wherein ρ is approximately 1.9.

* * * * *

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BIB DATA SHEET

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APPLICANTS

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**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

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35 USC 119(a-d) conditions met	☐ Yes ☑ No					
Verified and Acknowledged	/HENRY CHOE/ Examiner's Signature	Initials	NETHERLANDS	7	20	2

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TITLE

Amplifiers with Input Offset Trim and Methods

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First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	55123P377_20090223_ADS.pdf	835909 da6cd0ba114d961ac14a18f16b393880741032e7	no	4
Warnings:					
Information:					
2		55123P377_20090223_App.pdf	174475 9073971b658a383a77b6817df3671f8ca17c165a	yes	39
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	31	
	Drawings-only black and white line drawings		32	38	
	Abstract		39	39	
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3	Drawings-only black and white line drawings	55123P377_20090223_Figs.pdf	157725 3042278dcbc3c62c1494dfa43a4ff4a5e9da57aa	no	7
Warnings:					
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4	Information Disclosure Statement Letter	55123P377_20090223_IDS_Letter.PDF	71255 4cc1feca9eec7df26401b24f7cd1b93cec8fabd9	no	1
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5	Information Disclosure Statement (IDS) Filed (SB/08)	55123P377_20090223_IDS.pdf	30758 1c25328e04fc4ab5690486b017a13089b11f2760	no	1
Warnings:					
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6	Foreign Reference	JP2288616.pdf	596276 5275c5d82169d38d1270c5f3b4a385160ff7eb13	no	11
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7	NPL Documents	Enz_et_al.pdf	2326332 2d3a6a068eff761ae71fe509e3d3dca0872b66fc	no	31
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9	Oath or Declaration filed	55123P377_20090223_Decl_POA.pdf	135616 50f0e1984f5c68250da15f56d46fddd44bc71e48	no	4
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10	NPL Documents	Krummenacher_et_al.pdf	502656 08b9e48ad3763dbb0be3df6ac5339e4fd906ddfb	no	2
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	55123P377
	Application Number	
Title of Invention	Amplifiers with Input Offset Trim and Methods	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

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Applicant 2 Remove

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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	55123P377
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Title of Invention	Amplifiers with Input Offset Trim and Methods	

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Application Information:

Title of the Invention	Amplifiers with Input Offset Trim and Methods		
Attorney Docket Number	55123P377	**Small Entity Status Claimed** ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	7	**Suggested Figure for Publication (if any)**	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	55123P377
	Application Number	
Title of Invention	Amplifiers with Input Offset Trim and Methods	

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Signature	/RWB/			Date (YYYY-MM-DD)	2009-02-23
First Name	Roger	Last Name	Blakely	Registration Number	25831

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Atty Docket No. 55123P377

UNITED STATES PATENT APPLICATION

FOR

AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

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55123P377

AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of operational and instrumentation amplifiers.

2. Prior Art

One of the key performance specifications of an operational amplifier is its DC error or offset voltage. The offset voltage limits the ability of the amplifier to resolve small DC input voltages. The total offset voltage is usually specified assuming a single source of error at the input terminals. The value of this imaginary voltage source represents the input referred offset voltage of the amplifier. The significance of this parameter lies in the fact that the amplifier will not be able to resolve any DC voltages at its input that are smaller than the input referred offset voltage.

In monolithically integrated operational amplifiers, the input referred offset voltage (also called input offset, offset voltage or just offset for short) is mostly due to statistical mismatch between critical components in the circuit. Commonly, these critical components include the

input stage transistors, but other devices may contribute significantly to the offset as well. Typical offset voltages due to component mismatch lay in the order of several millivolts.

A well-known technique to reduce the input referred offset voltage of an amplifier is by trimming each amplifier during manufacturing. At some stage in the production process - usually while electrically screening the parts for defects - the native offset of the part is measured, and corresponding modifications are made to the part to compensate for this offset. The modifications to the part need to be permanent, in order for the offset to remain compensated for over the life of the product.

Many techniques have been proposed and used in the past to make permanent changes to an IC in order to store the offset compensation voltage. Examples include trimming resistors with a laser, blowing links with a laser, shorting out zener diodes by a high reverse voltage, blowing metal fuses with a high current, modifying the resistivity of a poly-silicon resistor with a high current and storing digital bits onto a non-volatile memory (e.g. flash).

Based on the timing of the trimming during the production process, all trimming techniques can be classified into one of two categories:

1. pre-package trim
2. post-package trim

As the name implies, pre-package trim includes all trim techniques that take place before the silicon die is packaged into its final package. Reversely, post-package trim is done after packaging the part.

The distinction between pre and post-package trim is a critical one, since the packaging process can lead to significant offset shifts of the part. Especially plastic packages, which include the majority of all parts being shipped today, can inflict high mechanical stresses to the silicon die. The piezoelectric properties of silicon convert the mechanical stresses into offset voltage shifts of the circuit. These offset shifts in their turn cause the input referred offset voltage of the part to change randomly after packaging. Typical offset shifts due to packaging are on the order of several 100s of microvolts.

A part that was trimmed for zero offset before packaging (pre-package trim), will most likely show a non-zero offset after being assembled. Therefore, pre-package trim is not able to guarantee very high accuracies of the trimmed offset voltage.

Post-package trim, on the other hand, takes into account offset shift due to packaging and will compensate for it. Very high trim accuracies can be achieved this way.

Despite its high end-accuracy, there are two main disadvantages associated with post-package trim. The first disadvantage of post-package trim is the need for some sort of on-die non-volatile memory. Most process technologies used for fabricating operational amplifiers do not offer non-volatile memory, and if they do, bit cells tend to be not very area-efficient.

The second disadvantage is the need to offer means to externally control the trim state and store the offset compensation value. In many cases this will require the addition of pins to the package, and increase cost. Alternatively, the part can employ some sophisticated multiplex approach to reuse the existing pins for controlling the offset trim algorithm. Such setup requires complex circuitry, however, adding to the die size and cost.

An approach to post-package trim that does not require non-volatile memory and external control of the trim algorithm is so-called power-on calibration. Using this technique, the part is not trimmed during manufacturing, but instead each time the part is powered up (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections:

Autozeroing, Correlated Double Sampling, and Chopper Stabilization", C.C. Enz and G.C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, Nov. 1996, pp. 1584-1614 and "A high-performance autozeroed CMOS opamp with 50 μV offset", Krummenacher et al., Solid-State Circuits Conference, 1997, Digest of Technical Papers, pp. 350 - 351, 483). Since the stored offset compensation value needs to be retained only while the supply power is available, power-on calibration alleviates the need for non-volatile memory. Instead, volatile memory can be used. This type of memory offers small die size, and it is ubiquitously available in any CMOS process technology in the form of flip-flops.

Figure 1 shows the block diagram of an amplifier with power-on calibration.

It uses the successive approximation algorithm to cancel out the random input referred offset voltage V_{os}. Offset calibration of amplifier A is achieved through switch S, comparator COMP, the successive approximation state-machine SAR and finally the digital-to-analog converter D/A that feeds an offset correction voltage to amplifier A. When the amplifier is powered on, switch S is closed. This forces a differential input voltage that is equal to the input referred offset voltage V_{os} at the input of amplifier A. Since there is no feedback, the amplifier A operates in the

comparator mode: if the differential input voltage is greater than zero, its output will jump to the positive rail, and vice verse (assuming the offset correction voltage at port N is zero).

Figure 2 shows a simplified representation of the amplifier circuit in Figure 1 during calibration.

While calibrating, the input switch in Figure 1 connects the offset source V_{os} between the two differential inputs of amplifier *A*. This is represented by the offset source V_{os} in Figure 2. Since the *D/A* output voltage V_{da} drives offset compensation port *N* on amplifier A_1 in Figure 1, the effect of V_{da} can be thought of as being subtracted from the offset voltage V_{os} at the input of the amplifier. This is indicated in Figure 2 by the plus sign for the voltage V_{os}, and the minus sign for the voltage V_{da}. The difference between offset voltage V_{os} and correction voltage V_{da} is error voltage ε. The sign of the error voltage ε, through amplifier *A* and comparator *COMP*, drives the decisions of the successive approximation algorithm.

After power-up the circuit will start its successive approximation state-machine to find a value for the offset correction voltage V_{da} at the secondary input *N* that minimizes the input referred offset voltage of the overall circuit. The successive approximation operates as follows (see Analog-To-

Digital and Digital-To-Analog Converters, R.J. van de Plassche, Springer, 1994). The circuit starts off with all bits to the digital-to-analog converter *D/A* set to zero. This causes the most negative voltage V_{da} to be set on the offset compensation input *N*. If the offset compensation range is large enough, this negative voltage will always cause the output of amplifier *A* to trip high ($\varepsilon>0$). In the next cycle, the most significant bit (MSB or b_n) of *D/A* will be tested high. If this causes the output of *A* to go low ($\varepsilon<0$), the bit will be returned to its low state before proceeding to the next bit. Otherwise, if the output of *A* does not change due to setting the MSB ($\varepsilon>0$), the bit will remain high. The state of the MSB will be stored into a register and does not change during the remainder of the calibration process. In the following step, the bit below the MSB (b_{n-1}) will be tested high and the resulting bit value stored into the register. This process continues successively through all bits, high to low, until the least significant bit is tested and its value stored.

Table 1 shows an example of the offset calibration procedure for a 3-bits SAR register in the simple case that the offset voltage V_{os} is zero.

Step	b_3 (±1V)	b_2 (±0.5V)	b_1 (±0.25V)	V_{da} [V]	ε [V] (V_{os}-V_{da})	Comment
0	0	0	0	-1.75	+1.75	Initial State
1	<u>1</u>	0	0	+0.25	-0.25	ε <0, b_2=0
2	0	<u>1</u>	0	-0.75	+0.75	ε >0, b_1=1
3	0	1	<u>1</u>	-0.25	+0.25	ε >0, b_0=1
4	0	1	1	-0.25	+0.25	Final State

Table 1. Example of the successive approximation algorithm, assuming Vos=0

The table assumes that the *MSB* b_3 switches between the values −1V (bit low) and +1V (bit high). The other bits are binary weighted, such that b_2=±0.5V and b_1=±0.25V. Bits tested by the algorithm are underlined. The error value ε in the example of Table 1 approaches zero within the step size of one *LSB* (0.5V). The resulting binary code is (011) (see the bottom row).

Table 2 gives a similar example of the successive approximation algorithm, now assuming that the input offset voltage Vos is 1.6V. In this case the bits converge to the code (110), with a remaining error ε of 0.35V, which is again within one LSB step size.

Step	b_3 (±1V)	b_2 (±0.5V)	b_1 (±0.25V)	V_{da} [V]	ε [V] (V_{os}-V_{da})	Comment
0	0	0	0	-1.75	+3.35	Initial State
1	<u>1</u>	0	0	+0.25	+1.35	ε >0, b_2=1
2	1	<u>1</u>	0	+1.25	+0.35	ε >0, b_1=1
3	1	1	<u>1</u>	+1.75	-0.15	ε <0, b_0=0
4	1	1	0	+1.25	+0.35	Final State

Table 2. Example of the successive approximation algorithm, assuming Vos=1.6

Notice how in the examples in Table 1 and Table 2 the remaining output error **ε** is always greater than zero. This is a property of the successive approximation algorithm: if a particular bit is tested high and the error voltage **ε** becomes smaller than zero, the bit is reset to zero. As a result, the algorithm does not allow the error **ε** to become negative.

In fact, the distribution of the error **ε** is between zero and one LSB step size S_{lsb}. Ideally, we would like to see the error centered around zero. Doing so will half the maximum error **ε** from +1 S_{lsb} to ±½ S_{lsb}. In order to perform the re-centering, we will need to add a value equal to ½ S_{lsb} to the *D/A* converter voltage V_{da} after the calibration completes. The shift of the final *D/A* converter voltage V_{da} can be achieved by adding one more bit to the *D/A* converter, below the least significant bit b_1 (LSB). This additional bit is held at zero during the calibration process, and subsequently set to one, once the calibration is done. Table 3 illustrates the addition of a shift bit to the algorithm.

Step	b_3 (±1V)	b_2 (±0.5V)	b_1 (±0.25V)	$\boldsymbol{b_s}$ **(±0.125V)**	V_{da} [V]	ε [V] (V_{os}-V_{da})	Comment
0	0	0	0	**0**	-1.875	+3.475	Initial State
1	<u>1</u>	0	0	**0**	+0.125	+1.475	ε >0, b_2=1
2	1	<u>1</u>	0	**0**	+1.125	+0.475	ε >0, b_1=1
3	1	1	<u>1</u>	**0**	+1.625	-0.025	ε <0, b_0=0
4	1	1	0	**1**	+1.375	+0.225	Final State

Table 3. Example of the successive approximation algorithm with a shift bit, assuming Vos=1.6

In this example, the error ε in the final state is 0.225V (bottom row), which is less than half an LSB step size (0.25V).

Even though the successive approximation algorithm is very powerful in calibrating out the offset of an amplifier at power-up, it suffers from a major drawback. In order for the algorithm to be able to guarantee a certain end-accuracy of the calibration, matching of the various components in the D/A converter needs to be extremely tight. Especially matching of the MSB step size S_{msb} to the other bits turns out to be critical. The matching error of the MSB step size S_{msb} must be significantly less than one LSB step size S_{lsb} in order for the mismatch not to affect the overall accuracy appreciably:

$$\Delta S_{msb} << S_{lsb} \tag{1}$$

This can be rewritten as

$$\frac{\Delta S_{msb}}{S_{msb}} << \frac{S_{lsb}}{S_{msb}} = \frac{1}{2^{n-1}} \tag{2}$$

where n equals the number of bits of the D/A converter.

Accepting a maximum error due to mismatch of the MSB equal to half an LSB step size ½ S_{lsb}, the expression for the maximum matching error of the MSB simplifies to

ANALOG EXHIBIT 1002
Page 46 of 321

$$\frac{\Delta S_{msb}}{S_{msb}} \leq 2^{-n} \qquad (3)$$

Similar constraints as for the MSB on the maximum matching error occur for the other bits of the A/D converter, albeit with progressively looser matching requirements. The step size of the bits becomes smaller by a factor two for each step when going from the MSB to the LSB. Therefore the expression for the maximum matching error of individual bits becomes

$$\frac{\Delta S_b}{S_b} \leq 2^{-b} \qquad (4)$$

where b equals the bit number (b=n for the MSB, b=1 for the LSB).

Clearly, matching of the MSB will be the most critical.

To illustrate the effect of mismatch on the transfer function of the D/A converter, Figure 3 shows an example of the output voltage vs. input code of a 3-bit converter without any mismatch error.

The output steps through all eight possible output values with even step sizes as the input code progresses from (000) through (111). The ideal D/A converter of Figure 3 can generate any voltage needed to compensate for the offset of the overall amplifier within half an LSB step size (½ S_{lsb}).

ANALOG EXHIBIT 1002
Page 47 of 321

Figure 4 shows the transfer function of the same D/A converter, now assuming a mismatch error that causes the MSB step size to be too large.

Note how the output voltage jumps when the input code goes from (011) to (100). This is because during this transition, the MSB is switched on. Turning on the MSB is supposed to almost make up for all other bits switching off, leaving a positive difference of 1 LSB step size S_{lsb} between the output levels for codes (011) and (100). Since in this example the MSB step size S_{msb} is too large, the MSB over-compensates for the other bits switching off, causing the difference between the two levels to be too large. This creates a gap between the output voltage levels for input codes (011) and (100).

The hatched area is a range of output voltages that is not covered by the D/A converter. If the voltage V_{da} that is needed to compensate for the offset of the overall amplifier falls somewhere in the middle of the hatched voltage range, the offset voltage most likely cannot be corrected for within half an LSB step size, or ½ S_{lsb}.

When matching errors cause the MSB step size S_{msb} to be too small, we obtain a D/A response similar to Figure 5. The transfer function is not monotonic anymore and has a slightly reduced dynamic range compared to the ideal case of Figure 3.

Despite these two factors, all output voltages within the dynamic range of the converter can now be produced within half an LSB step size (½ S_{lsb}). In other words, despite the MSB mismatch error, we can continue to guarantee that any offset voltage of the overall amplifier can be compensated for within ½ S_{lsb}. Note that monotonicity of the D/A transfer function is not required for the successive approximation algorithm to function properly.

Summarizing the effects of MSB mismatch on the successive approximation algorithm, we find the following:

1. A mismatch error that causes the MSB to be too *large* will deteriorate the worst-case offset voltage of the overall amplifier after calibration.

2. A mismatch error that causes the MSB to be too *small* does not significantly affect the overall accuracy of the offset calibration.

Figure 6 illustrates this conclusion.

On the x-axis, it shows the ratio between the value of the MSB b_n and the next bit b_{n-1} (bit ratio ρ), while the y-axis represents the probability of a certain bit ratio ρ. Ideally, the bit ratio ρ is 2 (MSB b_n twice as large as the next bit b_{n-1}). Due to mismatch between the components used to manufacture the circuit, the actual bit ratio ρ will vary

ANALOG EXHIBIT 1002
Page 49 of 321

around the mean value of 2 with a normal distribution having standard deviation σ_ρ. In order to make sure that the overall error due to component mismatches does not exceed half an LSB step size (½ S_{lsb}), the bit ratio ρ should not be too large.

The relation between the error $\Delta\rho$ of the bit ratio ρ and the mismatch $\Delta S_n/S_n$ of the MSB step size can be found as follows

$$\begin{aligned} &S_n = 2 \cdot S_{n-1} \\ &S_n + \Delta S_n = (2 + \Delta\rho) \cdot S_{n-1} \Rightarrow \\ &\frac{\Delta S_n}{S_n} = \frac{\Delta\rho \cdot S_{n-1}}{S_n} = \frac{\Delta\rho}{2} \end{aligned} \qquad (5)$$

Using Eq. 3 and Eq. 5, we can now find for the maximum allowed error $\Delta\rho_{max}$

$$\Delta\rho_{\max} = 2 \cdot 2^{-n} \qquad (6)$$

From Eq. 6 we can find the expression for the maximum acceptable absolute value of the bit ratio ρ_{max}

$$\rho_{\max} = \overline{\rho} + \Delta\rho_{\max} = 2 + 2^{1-n} \qquad (7)$$

where $\overline{\rho}$ is the *mean* or targeted bit ratio

The hatched area in Figure 6 indicates the forbidden range of bit ratios ρ. Values of the bit ratio ρ that lie above $2+2^{1-n}$, indicated by the dashed line, lead to the

calibration of the overall circuit potentially being out of spec (point 1 above), whereas any value of the bit ratio ρ below this limit guarantees a calibrated offset within the specifications (see point 2 above).

Based on Eq. 7, we can determine the maximum matching error of the bit ratio

$$\frac{\Delta\rho_{\max}}{\overline{\rho}} = 2^{-n} \qquad (8)$$

Note how the maximum acceptable matching error $\Delta\rho_{\max}/\overline{\rho}$ goes down exponentially with the number of bits. Especially with high bit counts, this can result in very tight matching requirements.

Considering n=10 bits as an example, the maximum allowable mismatch error of the bit ratio $\Delta\rho_{\max}/\overline{\rho}$ equals 2^{-10}, or about 0.1% (Eq. 8). Requiring this to be a 6σ limit (probability of exceeding the spec limit smaller than ~1 ppb, assuming a normal distribution), means the standard deviation of the MSB bit ratio matching σ_ρ must be smaller than 0.016%.

The matching requirements that follow from Eq. 8 are often very hard - if not impossible - to achieve in practical monolithically integrated circuits. Therefore, current state-of the art amplifiers with power-on calibration rely heavily on production screening of all possible D/A output

ANALOG EXHIBIT 1002
Page 51 of 321

levels to guarantee that the input referred offset will be within specs across wide ranges of operating conditions. Due to the large number of possible output levels (1024 for n=10), this production screening is both time-consuming and costly.

ANALOG EXHIBIT 1002
Page 52 of 321

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art amplifier with power-on calibration.

Figure 2 shows a prior art power-on calibrated amplifier in calibration mode.

Figure 3 shows an ideal 3-bit D/A transfer function.

Figure 4 shows a 3-bit D/A converter transfer curve: MSB too large.

Figure 5 shows a 3-bit D/A converter transfer curve: MSB too small.

Figure 6 shows the probability-density function of the bit ratio ρ of a SA D/A converter.

Figure 7 shows the probability-density function of the bit ratio ρ for the proposed calibration circuit.

Figure 8 shows a preferred embodiment of power-on calibration using a non-binary weighted D/A converter.

Figure 9 is a simplified example of the circuit implementation of the proposed invention.

Figure 10 shows an example of the circuit implementation of the non-binary weighted A/D converter.

ANALOG EXHIBIT 1002
Page 53 of 321

Figure 11 shows an example of an instrumentation amplifier with power-on calibration.

Figure 12 presents an exemplary configuration to trim at production, while storing the results in one-time programmable memory.

Figure 13 shows the addition of an auxiliary amplifier to control the output during calibration.

ANALOG EXHIBIT 1002
Page 54 of 321

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Traditional successive approximation approaches to power-on calibration lead to excessively tight matching specifications of the D/A converter components. The present invention proposes a method to relax the matching requirements. Allowing for more variation will greatly improve the manufacturability of power-on calibration circuits.

The key to improving the robustness of the power-on calibration lays in the use of a targeted bit ratio $\overline{\rho}$ that is smaller than the traditional $\overline{\rho}=2$. Note from Figure 6 and Eq. 7 that any ratio ρ below $2+2^{1-n}$ (with a practical under limit of $\rho=1$) guarantees the accuracy of the calibration. By choosing a target bit ratio $\overline{\rho}$ less than 2, meeting the limit set by Eq. 7 becomes progressively easier.

This is illustrated by Figure 7.

This plot again shows the probability density function of the bit ratio ρ between the MSB b_n and the adjacent bit b_{n-1}, assuming a normal distribution. The maximally allowable ratio ρ that guarantees proper calibration of the amplifier's offset is indicated by the dashed line at $\rho_{max}=2+2^{1-n}$. The hatched area indicates "forbidden" values for the ratio ρ.

The main difference between the prior-art plot in Figure 6 and the plot of Figure 7 is that the bit ratio is now centered around a value that is slightly smaller than the traditional value of 2. Figure 7 uses a mean bit ratio of $\overline{\rho}=1.9$ as an example.

A consequence of choosing a smaller mean bit ratio is that the peak of the probability density function moves away from the upper limit. A greater distance between the peak and the upper limit suggests it will be easier to meet the spec in production. This can be quantified as follows. The difference between the mean of the bit ratio $\overline{\rho}$ and the spec limit ρ_{max} is given by

$$\rho_{\max}-\overline{\rho}=2+2^{1-n}-\overline{\rho} \tag{9}$$

Since the number of bits $n>>1$ in most practical cases, this reduces to

$$\rho_{\max}-\overline{\rho}\approx 2-\overline{\rho} \tag{10}$$

The matching requirement for the bit ratio ρ now becomes

$$\frac{\Delta\rho_{\max}}{\overline{\rho}}\approx\frac{2-\overline{\rho}}{\overline{\rho}}\approx\frac{2-\overline{\rho}}{2} \tag{11}$$

The right hand side of Eq. 11 assumes the target bit ratio $\overline{\rho}$ is close to 2.

Note that the matching requirement that follows from Eq. 11 is *independent* of the total number of bits. In the prior-art case of $\overline{\rho}=2$ (binary weighted), the matching spec became exponentially tighter with a rising number of bits (Eq. 8).

By substituting our example of $\overline{\rho}=1.9$ into Eq. 11, we find the maximum allowable mismatch of the bit ratio as 5%. Again requiring a 6σ limit, this leads to a maximum standard deviation of the mismatch of the MSB bit ratio σ_ρ equal to 0.8%. This is much looser than the 0.016% of the binary weighted prior art example. In fact, matching ratios on the order of 0.8% can routinely be realized in standard manufacturing processes without the need for additional trimming or production testing.

Figure 8 shows the preferred embodiment of the proposed invention.

It consists of amplifier input stage A_1, and the two selectable output stages A_{2a} and A_{2b}. Power-on offset calibration is performed through the comparator *COMP*, the successive approximation register *SAR* and a non-binary weighted D/A converter. The D/A converter comprises the switches b_n through b_s, and the non-binary weighted bit values 1 through $1/1.9^{n-2}$, plus binary weighted values for the least significant bit controlled by switch b_1 and the shift bit b_s.

ANALOG EXHIBIT 1002
Page 57 of 321

At power up of the circuit, the input switch S_1 shorts out the inputs to the amplifier input stage A_1. As a result, the input referred offset voltage V_{os} will be present between its differential input terminals. Output switch S_2 connects the input stage A_1 to the secondary output stage A_{2b}. Because of its connection to the secondary output stage A_{2b}, the comparator *COMP* can now drive the decisions of the successive approximation algorithm implemented by the register *SAR*. The least significant bit is given a binary weighting because of the fact that any error in that weighting does not cause an error that must be made up by subsequent bits, and the shift bit is given a binary weighting relative to the least significant bit as its purpose is to compensate for one half the least significant bit to cause the error ε to be centered around zero instead of always being on one side of zero, thereby cutting the maximum error in half.

Once the power-on offset calibration completes, switch S_1 connects the input terminals of the overall amplifier to the input stage A_1, while switch S_2 activates output stage A_{2a}. Also, the SAR register activates the shift bit b_s. Note that the ratio between the LSB b_1 and the shift bit b_s remains two, even if all other bits are non-binary weighted. The amplifier is now in its normal mode of operation, with the register *SAR* holding a digital code that corresponds to a

ANALOG EXHIBIT 1002
Page 58 of 321

voltage V_{da} that (mostly) compensates for the input referred offset V_{os}.

Even though the use of the two selectable output stages A_{2a} and A_{2b}, along with output switch S_2 is not necessarily required for the invention to work properly, this setup has several key advantages over using a single output stage for both calibration and normal mode. First of all, selecting between the two output stages will prevent spurious signals or glitches to appear at the output terminal of the amplifier while the amplifier is being calibrated. A second benefit of duplicating the output stage is that the secondary output stage A_{2b} can now be implemented without the addition of a compensation capacitor for closed loop stability. Frequency compensation capacitor C_m is required during normal operation to ensure stability of the amplifier with overall feedback. Since the amplifier is operated in an open-loop comparator mode during power-on calibration, no frequency compensation is needed. Leaving out the compensation capacitor speeds up the decisions during the successive approximation procedure, reducing the total time spent in calibration mode.

As an alternative to a power-up event, the calibration sequence can also be initiated by any other trigger. In that case, the system performs on-demand-calibration as opposed to power-on calibration as described before.

ANALOG EXHIBIT 1002
Page 59 of 321

Figure 9 shows a simplified example of a circuit implementation of the present invention.

It consists of the transconductance input stage with transistors M_1 and M_2. The gates of these devices are connected to switches $S_{1,1}$ and $S_{1,2}$. In normal mode, the switches directly connect the gates of M_1 and M_2 to the input terminals *IN+* and *IN-*. During calibration, the inputs are shorted out and connected to the reference common-mode voltage V_1. Devices M_5 through M_8 implement a traditional folded cascode turn-around stage. The first or primary output stage used for normal operation comprises the devices M_{11} and M_{12}, together with frequency compensation capacitors C_{M1} and C_{M2}. The secondary output stage used during calibration includes devices M_9 and M_{10}. This secondary output stage does not require any frequency compensation components, since it will only be used in comparator mode. Switches $S_{2,1}$ and $S_{2,2}$ select between the two output stages. The block *AB* implements class-AB quiescent current control of the output stage devices (either M_{11} and M_{12}, or M_9 and M_{10}, depending on the states of $S_{2,1}$ and $S_{2,2}$). When the primary output state M11 and M12 is selected, switches $S_{2,3}$ and $S_{2,5}$ are closed, putting the secondary output stage in a high output impedance state, and when the secondary output state M9 and M10 is selected, switches $S_{2,4}$ and $S_{2,6}$ are closed, putting the primary output stage in a high output impedance state.

ANALOG EXHIBIT 1002
Page 60 of 321

The parallel input stage M_3/M_4 implements the offset control input. A differential voltage between the gates of M_3 and M_4 will cause a differential output current at their drains. This differential drain current flows in parallel to the drain current of the input stage M_1/M_2. A suitable differential voltage at the gates of M_3 and M_4 can compensate for a random offset of the input stage M_1/M_2. Since the range of offset voltages that the parallel input stage needs to compensate for is much smaller than the expected signal swing at the input of the amplifier, the tail current I_2 through devices M_3 and M_4 can be chosen smaller than the bias current of the input stage I_1.

The register *SAR* and the non-binary weighted D/A converter *D/A* implement the successive approximation algorithm as before.

Figure 10 shows an example of a 6-bit implementation of the non-binary weighted D/A converter.

It consists of a three-section differential resistive ladder with resistor values R, R_1 and R_2. The common-mode voltage of the ladder is set by voltage source V_{cm}. Note that this voltage is not related to any common mode voltage of an input signal IN+,IN-, as the transistors M3 and M4 operate in a differential mode to control the division of the current I2 (Figure 9), independent of the operation of the differential

ANALOG EXHIBIT 1002
Page 61 of 321

input stage transistors M1 and M2. The switches b_8 through b_6 steer the currents from the bottom current sources to either side of the differential ladder, depending on the states of the input bits. In this example, the weighting of the bits b_2 through b_4 is done through the resistive ladder, while weighting of b_8, b_1 and b_6 is implemented through scaling of the respective current sources. This choice is arbitrary, and not critical to the operation of the circuit.

Targeting a bit ratio of $\overline{\rho}$, the values of the resistors can be found as follows

$$R_1 = R \cdot (\overline{\rho} - 1)$$
$$R_2 = R \cdot \frac{\overline{\rho}}{\overline{\rho} - 1} \qquad (12)$$

where R is the characteristic impedance of the ladder.

Note how choosing a bit ratio $\overline{\rho} = 2$ (standard binary weighing) transforms the D/A converter of Figure 10 into a traditional R-2R ladder (R_1=R, R_2=$2R$).

By adding an additional input stage to the circuit of Figure 9, it can easily be transformed into a so-called instrumentation amplifier (see Operational Amplifiers, Theory and Design, J. Huijsing, pp. 52-53, Boston, Kluwer Academic Publishers, 2001). Instrumentation amplifiers have two sets of differential input terminals and are capable of sensing

small differential signals in the presence of a large common-mode disturbance.

In order for the power-on calibration to work properly in the modified circuit, only the input stage devices and the input switches need to be repeated from the original amplifier. The offset calibration can be performed across both input stages combined and therefore does not require any other additional components.

Figure 11 shows the instrumentation amplifier that results from modifying the circuit depicted in Figure 9. The components added to the circuit are the two input stage with M_{13} and M_{14}, along with the corresponding input switches $S_{1,3}$ and $S_{1,4}$, which would be operated simultaneously with $S_{1,1}$ and $S_{1,2}$.

The embodiments shown herein in Figures 9 and 11 are MOS embodiments, though other active devices may be used, such as bipolar devices. Also the word switch as used herein and in the claims is used in the general sense, and includes single or multiple switches, as appropriate. When the word switch is used in the context of multiple switches, such multiple switches would be operated substantially simultaneously, though perhaps with a preferred nonoverlapping phasing. By way of example, a switch for switching an input of the amplifier from the amplifier system input to shorting the

amplifier input might be a single switch such as switch S in Figure 1 or two switches $S_{1,1}$ and $S_{1,2}$ in Figure 9, or, by way of another example, might be four switches, two for disconnecting the differential input stage from the differential amplifier input, and two to short the input to the differential input stage. In this latter case, one normally would prefer to disconnect the differential amplifier input before shorting the differential input stage, thereby defining a nonoverlapping operation.

Similarly, a reference to an input or an output herein and in the claims is a reference to an input or an output generally, independent of whether the input or output is a single signal relative to a circuit ground, or a differential signal.

The approach of Figure 8 can be extended to perform one-time calibration during the fabrication of the device. In that case, the circuit requires some form of One-Time-Programmable memory, or OTP, to store the result of the calibration during the life-time of the product. Figure 12 shows an example.

When the device is powered up for the first time, the circuit will go through its auto-calibration cycle. Once the cycle completes, the resulting values for the bits b_n through b_s will be stored onto the non-volatile memory OTP. On

ANALOG EXHIBIT 1002
Page 64 of 321

subsequent power-up events, the stored offset compensation bits will be read from the OTP memory, and used to control the bit switches b_n through b_s. One additional OTP cell OTP_{n+1} is needed to establish the fact that the part has been programmed. This will avoid future attempts at calibrating the offset when the part is powered up in its application.

During auto-calibration, the overall amplifier in Figure 8 is non-responsive to external signals. This is caused by switches S_1 and S_2 that disconnect the amplifier from the external circuitry. Since the auto-calibration time can be short, disabling the amplifier will not cause issues in many, if not most, applications. In the situations where a controlled output voltage is needed, even during the auto-calibration sequence, the circuit of Figure 13 brings a solution.

The circuit of Figure 13 adds an auxiliary amplifier A_{aux} to the base circuit of Figure 8, along with the switches S_3 through S_5. When the part is auto-calibrating, the switches S_3 through S_5 are closed, and the auxiliary amplifier A_{aux} and the output stage A_{2a} create a signal path from the input terminals V_{in} to the output V_{out}. Since the calibration time is short, so the auxiliary amplifier will not have enough time to settle to a very high accuracy anyhow, offset and other demands on the auxiliary amplifier can be relaxed

ANALOG EXHIBIT 1002
Page 65 of 321

compared to the main circuit. As a result, a very simple circuit suffices in most practical cases.

Thus while certain preferred embodiments of the present invention have been disclosed and described herein for purposes of illustration and not for purposes of limitation, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

ANALOG EXHIBIT 1002
Page 66 of 321

CLAIMS

What is claimed is:

1. An amplifier system having an amplifier system input and an amplifier system output comprising:

a first amplifier;

a comparator;

a successive approximation register having an input coupled to an output of the comparator;

a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;

an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

2. The amplifier system of claim 1 wherein the radix is approximately 1.9.

3. The amplifier system of claim 2 wherein the radix for the least significant bit is 2.

4. The amplifier system of claim 1 wherein the D/A converter further comprises one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits.

5. The amplifier system of claim 1 wherein the first amplifier has a first transconductance differential input stage coupled to the first amplifier input, and wherein the first amplifier is further comprised a second transconductance differential input stage, the outputs of the first and second transconductance differential input stages being coupled in parallel, the output of the D/A converter being coupled to inputs of the second transconductance differential input stage to divide a current source coupled to the second transconductance differential input stage between the differential outputs of the first transconductance differential input stage in a proportion to reduce the input offset of the first amplifier.

6. The amplifier system of claim 5 wherein the first amplifier further comprises an intermediate stage having an input coupled to the parallel connected outputs of the first

and second transconductance differential input stages, a first output stage providing the first amplifier output, a second output stage forming the comparator, the second switch for switching an output of the intermediate stage between inputs to the first and second output stages.

7. The amplifier system of claim 6 wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage, and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

8. The amplifier system of claim 6 wherein the first amplifier is further comprised of a third transconductance differential input stage, the outputs of the first, second and third transconductance differential input stages being coupled in parallel, the first switch for shorting the first amplifier input by shorting the differential input to the first transconductance differential input stage and shorting the differential input to the third transconductance differential input stage at the same time.

9. The amplifier system of claim 1 further comprised of One-Time-Programmable memory for permanently storing an

output of the successive approximation register, whereby a single output of the D/A converter controlling the input offset of the first amplifier may be permanently maintained.

10. The amplifier system of claim 1 further comprised of a second amplifier, the first switch coupling the amplifier system input to an input of the second amplifier when shorting the input to the first amplifier, the second switch coupling an output of the second amplifier to the amplifier system output when switching the output of the first amplifier from the amplifier system output to an input of the comparator.

11. The amplifier system of claim 1 wherein the D/A converter comprises a common reference line, and at least in part, resistor ladders symmetrical about the common reference line, and third switches for selectively switching equal current sources to ladder nodes on either side of the common reference line responsive to the successive approximation register, the resistor ladders being $R(\rho-1), R\rho/(\rho-1)$ ladders, where ρ is less than 2.

12. The amplifier system of claim 11 wherein ρ is approximately 1.9.

ANALOG EXHIBIT 1002
Page 70 of 321

13. An amplifier system having an amplifier system input and an amplifier system output comprising:

an amplifier having a first transconductance differential input stage coupled to the amplifier input, and a second transconductance differential input stage, the outputs of the first and second transconductance differential input stages being coupled in parallel, the amplifier further having an intermediate stage having an input coupled to the parallel connected outputs of the first and second transconductance differential input stages, a first output stage providing the amplifier output, a second output stage forming the comparator;

a successive approximation register having an input coupled to an output of the second transconductance differential input stage;

a first switch for switching an input of the first transconductance differential input stage from the amplifier system input to shorting the input of the first transconductance differential input stage;

a second switch for switching an output of the intermediate stage between inputs to the first and second output stages;

an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

an output of the D/A converter being coupled to the second transconductance differential input stage to control the input offset of the amplifier.

14. The amplifier system of claim 13 wherein the radix is approximately 1.9.

15. The amplifier system of claim 13 wherein the radix for the least significant bit is 2.

16. The amplifier system of claim 13 wherein the D/A converter further comprises one additional bit providing an input offset control of the amplifier of one half that of the least significant bit of the N bits.

17. The amplifier system of claim 13 wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage, and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

18. The amplifier system of claim 13 wherein the amplifier is further comprised of a third transconductance

differential input stage, the outputs of the first, second and third transconductance differential input stages being coupled in parallel, the first switch for shorting the amplifier input by shorting the differential input to the first transconductance differential input stage and shorting the differential input to the third transconductance differential input stage at the same time.

19. The amplifier system of claim 13 wherein the D/A converter comprises a common reference line, and at least in part, resistor ladders symmetrical about the common reference line, and third switches for selectively switching equal current sources to ladder nodes on either side of the common reference line responsive to the successive approximation register, the resistor ladders being $R(\rho-1)$,$R\rho/(\rho-1)$ ladders, where ρ is less than 2.

20. The amplifier system of claim 19 wherein ρ is approximately 1.9.

ANALOG EXHIBIT 1002
Page 73 of 321

ABSTRACT

Amplifiers with power-on trim and methods using an amplifier system having an amplifier system input and an amplifier system output, an amplifier, a comparator, a successive approximation register having an input coupled to an output of the comparator, a first switch for switching an input of the amplifier from the amplifier system input to shorting the amplifier input, a second switch for switching an output of the amplifier from the amplifier system output to an input of the comparator, an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter, the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits, and an output of the D/A converter being coupled to the amplifier to control the input offset of the amplifier. Novel embodiments for the amplifier, comparator and D/A converter are disclosed.

ANALOG EXHIBIT 1002
Page 74 of 321

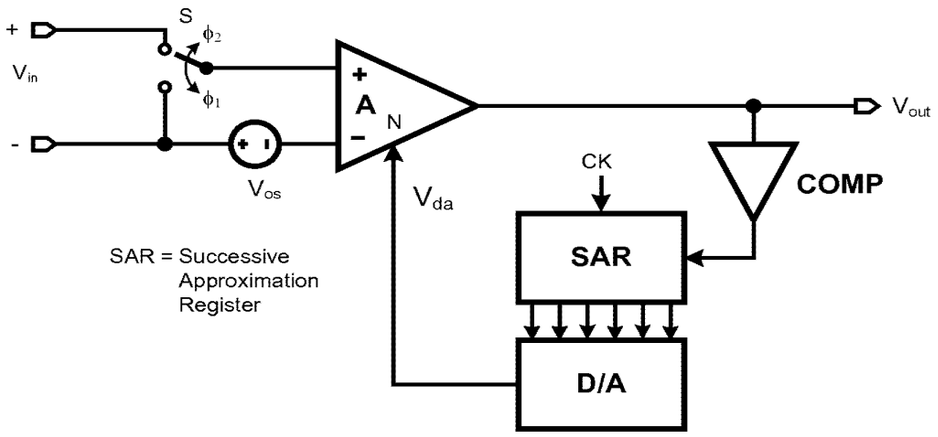


Figure 1. Prior Art: Amplifier with power-on calibration.

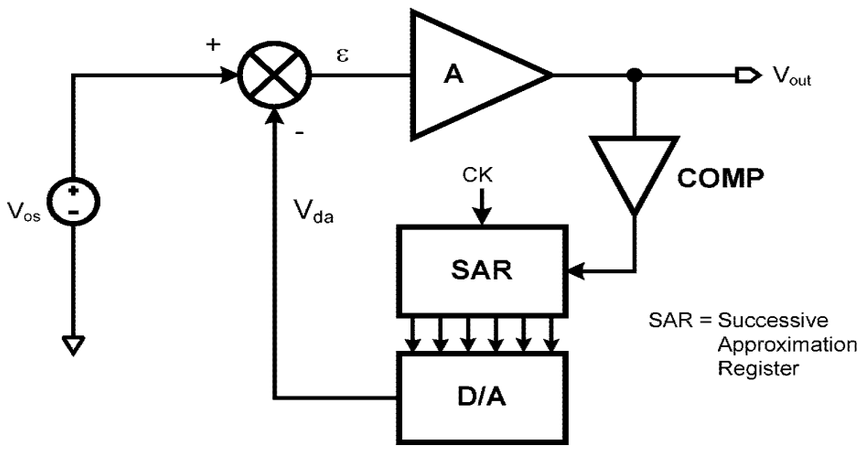


Figure 2. Prior Art: Power-on calibrated amplifier in calibration mode.

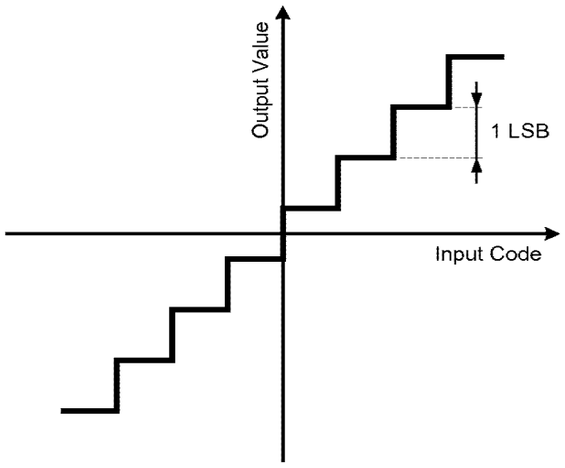


Figure 3. Ideal 3-bit D/A transfer function.

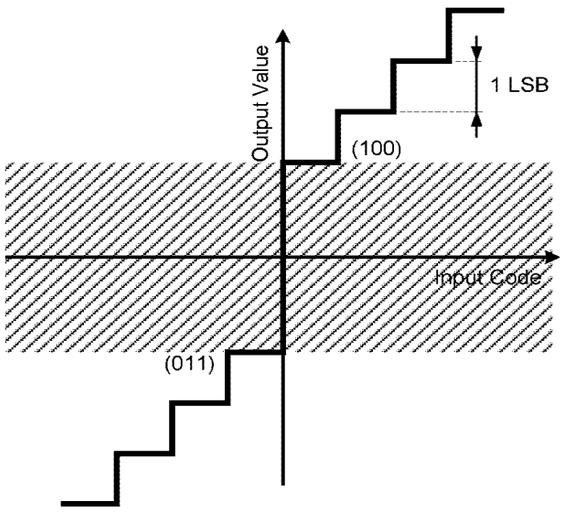


Figure 4. 3-bit D/A converter transfer curve: MSB too large.

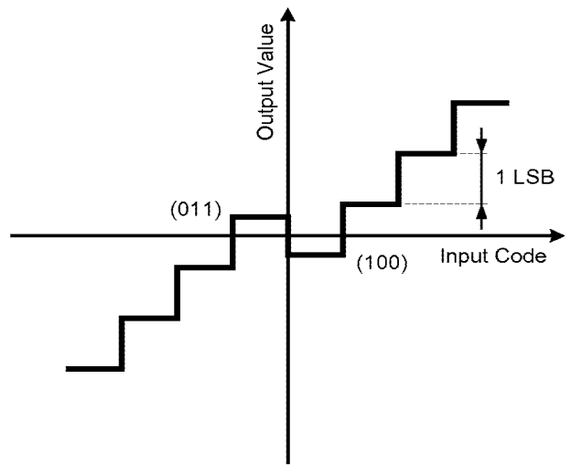


Figure 5. 3-bit D/A converter transfer curve: MSB too small.

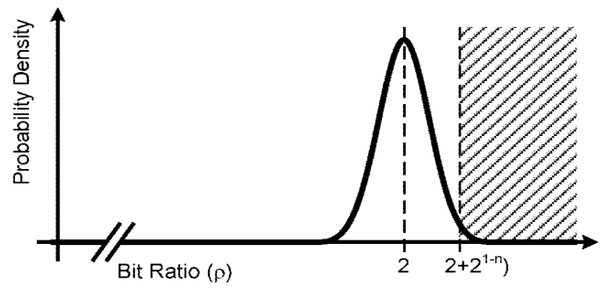


Figure 6. Probability-density function of the bit ratio ρ of a SA D/A converter.

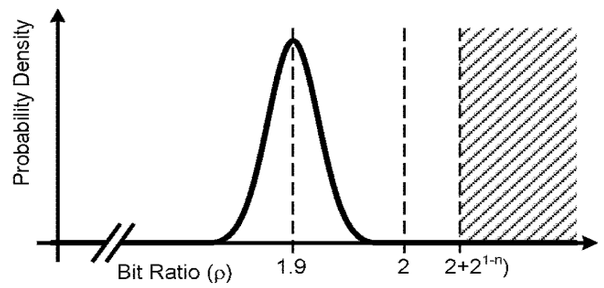


Figure 7. Probability-density function of the bit ratio ρ for the proposed calibration circuit.

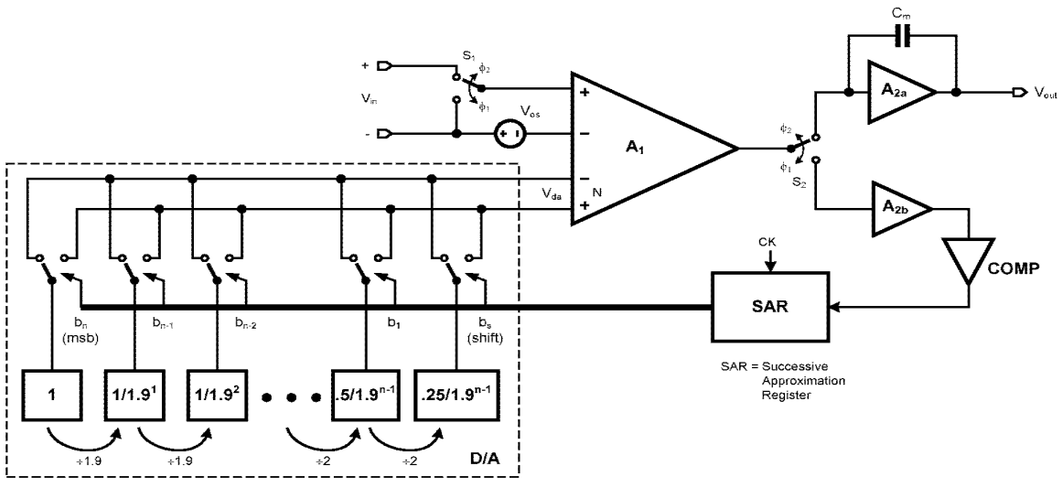


Figure 8. Preferred embodiment of power-on calibration using a non-binary weighted D/A converter.

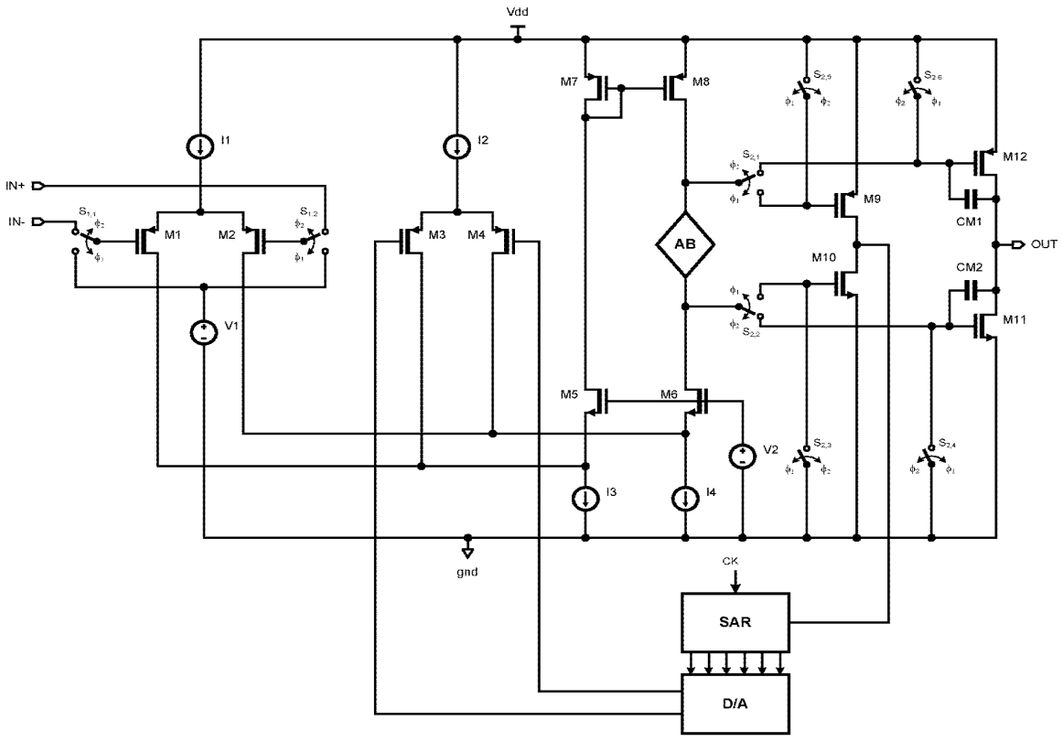


Figure 9. Simplified example of the circuit implementation of the proposed invention.

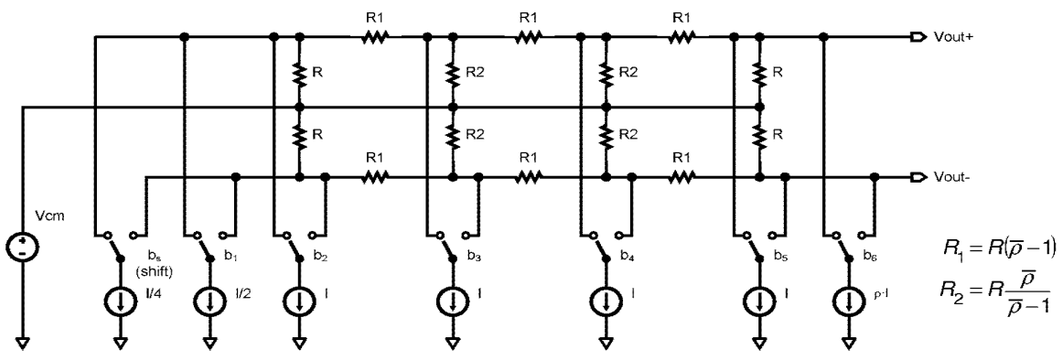


Figure 10. Example of the circuit implementation of the non-binary weighted D/A converter.

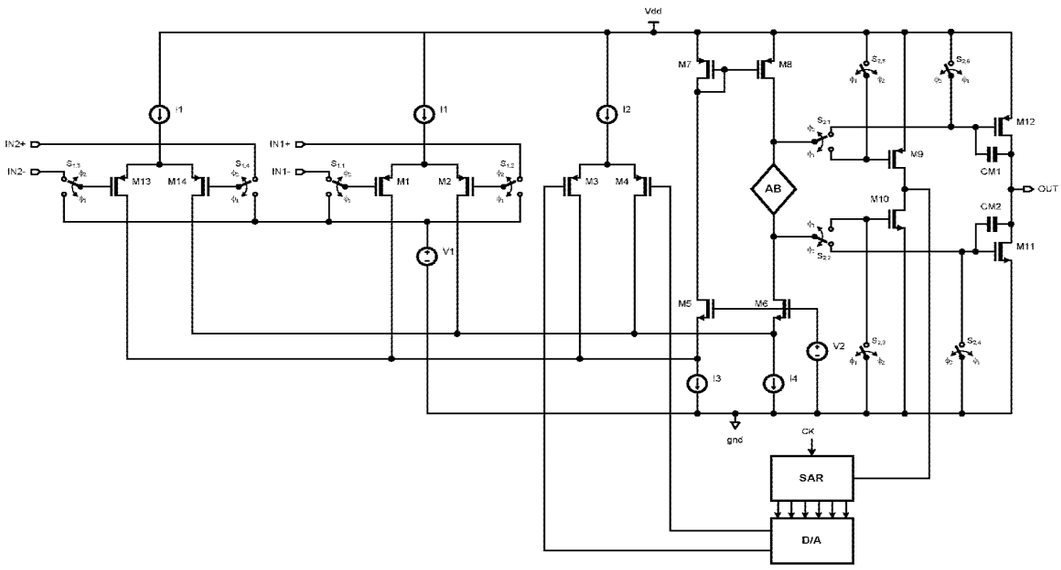


Figure 11. Example of an instrumentation amplifier with power-on calibration.

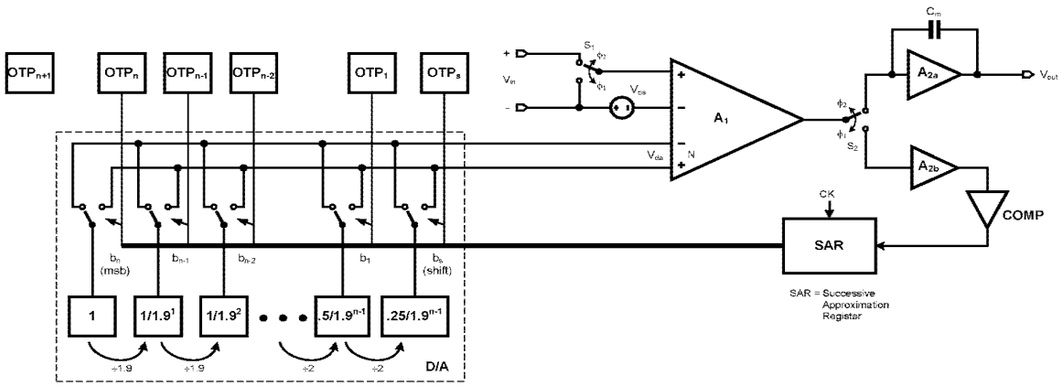


Figure 12. Example of configuration to trim at production time, while storing the results in OTP.

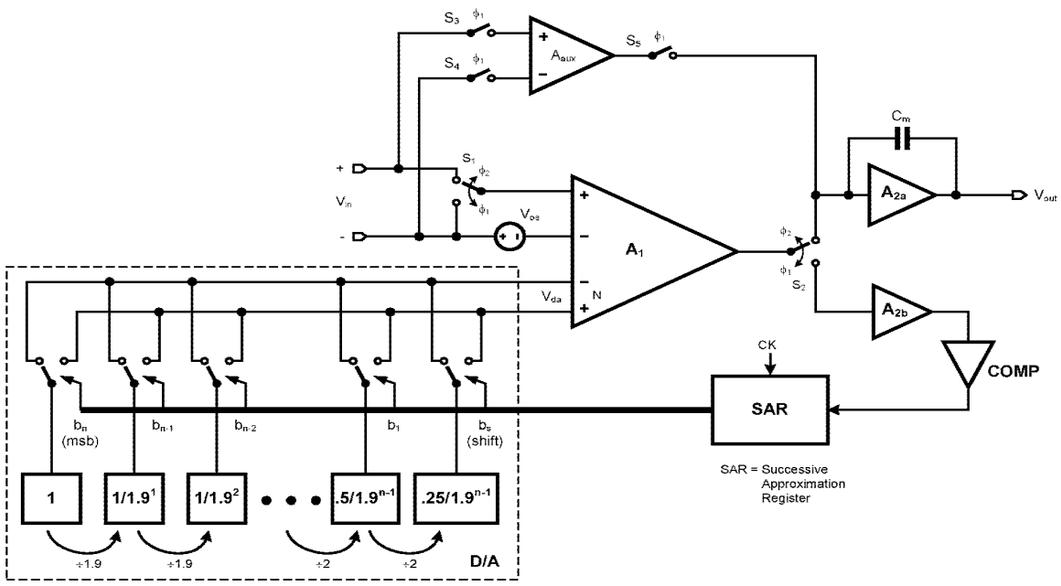


Figure 13. Addition of an auxiliary amplifier to control the output during calibration.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application No.	
	Filing Date	
	First Inventor	Rudy G. H. Eschauzier, et al.
	Art Unit	
	Examiner Name	
	Attorney Docket No.	55123P377 Conf. No.

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the Utility Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 02-2666.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	Roger W Blakely	Date (YYYY-MM-DD)	2009- 02-23
Name/Print	Roger W. Blakely, Jr.	Registration Number	25,831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Jessica A. Clark Jessica A Clark *Date* *02-23-09*

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	Not Yet Assigned
	Filing Date	Even Date Herewith
	First Named Inventor	Rudy G. H. Eschauzier
	Group Art Unit	
	Examiner Name	
Sheet 1 of 1	Attorney Docket No: 55123P377	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-6,130,632	10/10/2000	Opris, Ion E.	
		US-6,348,885	02/19/2002	Munoz, Carlos E., et al.	
		US-6,486,806	11/26/2002	Munoz, Carlos E., et al.	
		US-6,707,403	03/16/2004	Hurrell, Christopher P.	
		US-6,828,927	12/07/2004	Hurrell, Christopher P., et al.	
		US-7,026,866	04/11/2006	Llewellyn, William D.	
		US-7,038,609	05/02/2006	Hurrell, Christopher P.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
		JP-2-288616	11/28/1990	Nene, Yoshito , et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		ENZ, CHRISTIAN C., et al., "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", Proceedings of the IEEE, Vol. 84, No. 11, (November 1996), Pgs. 1584-1614	
		HUIJSING, J , "Operational Amplifiers, Theory and Design", Kluwer Academic Publishers, (2001), Pgs. 52-53	
		KRUMMENACHER, FRANCOIS , et al., "A High-Performance Autozeroed CMOS Opamp with 50uV Offset", IEEE International Solid-State Circuits Conference, Session 21, Amplifiers, Paper SA 21.3, (1997), Pgs. 350-351	
		VAN DE PLASSCHE, R J., "Analog-To-Digital and Digital-To-Analog Converters", Springer, (1994), Pgs 280-283	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

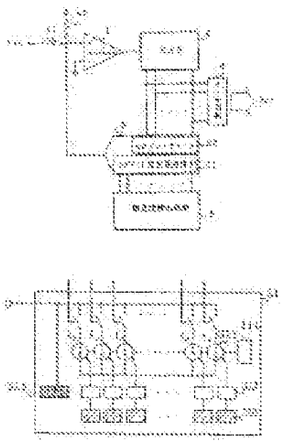
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

SELF-CALIBRATION TYPE D/A CONVERTER AND SELF-CALIBRATION TYPE A/D CONVERTER USING THE D/A CONVERTER

Publication number: JP2288616 (A)
Publication date: 1990-11-28
Inventor(s): NENE YOSHITO; HOTTA MASAO; MAIO KENJI; TOTANI HIROSHI
Applicant(s): HITACHI LTD; HITACHI MICROCUMPUTER ENG
Classification:
- international: ***H03M1/10;*** **H03M1/10;** (IPC1-7): H03M1/10
- European:
Application number: JP19890110854 19890428
Priority number(s): JP19890110854 19890428

Abstract of **JP 2288616 (A)**

PURPOSE:To attain high processing speed and high accuracy by varying an output current or a voltage of a constant current source or a constant voltage source so as to reduce any of the nonlinearity error, offset error and gain error of D/A converter. CONSTITUTION:A main D/A converter 3 is a current output type D/A converter consisting of a segment type constant current source array 31 and of a segment decoder 32 converting an input digital value from a Successive Approximation Register (SAR) 2 into a segment code. The segment type constant current source array 31 consists of plural constant current sources 311 generating the same value. Then any of the nonlinearity error, offset error and gain error of a D/A converter is decreased by varying an output current of each constant current source 311. Thus, a self-calibration type D/A converter with high speed and high accuracy is obtained.



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⑲日本国特許庁（JP）　⑪特許出願公開

⑫公開特許公報（A）　平2－288616

⑤1Int. Cl.⁵	識別記号	庁内整理番号	⑬公開　平成2年(1990)11月28日
H 03 M 1/10	A	6832－5J	
	B	6832－5J	

審査請求　未請求　請求項の数 21　（全10頁）

⑤4発明の名称　自己較正型ＤＡ変換器およびこれを用いる自己較正型ＡＤ変換器

⑳特　願　平1－110854
㉒出　願　平1(1989)4月28日

⑦2発明者　禰寝　義人　東京都国分寺市東恋ケ窪1丁目280番地　株式会社日立製作所中央研究所内
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⑦4代理人　弁理士　磯村　雅俊

最終頁に続く

明細書

1．発明の名称

自己較正型ＤＡ変換器および
これを用いる自己較正型ＡＤ変換器

2．特許請求の範囲

1．複数の定電流源あるいは定電圧源で構成されるＤＡ変換器において、前記定電流源あるいは定電圧源各々の出力電流値あるいは電圧値を変化させることによって、前記ＤＡ変換器の出力の非直線性誤差，オフセット誤差，利得誤差のいずれかを低減させることを特徴とする自己較正型ＤＡ変換器。

2．前記定電流源あるいは定電圧源の各出力電流値あるいは電圧値を変化させる手段を有することを特徴とする請求項1記載の自己較正型ＤＡ変換器。

3．前記複数の定電流源あるいは定電圧源が、同一の電流値あるいは電圧値を出力する定電流源あるいは定電圧源である、セグメント型ＤＡ変換器であり、該定電流源あるいは定電圧源の出力電流値あるいは電圧値がすべて同じ値になるように較正することを特徴とする請求項1または2記載の自己較正型ＤＡ変換器。

4．入力ディジタル値の上位ビットに対応する定電流源あるいは定電圧源はセグメント型定電流源列あるいは定電圧源列で、下位ビットに対応する定電流源あるいは定電圧源は、2進符号に対応して重み付けされた定電流源列あるいは定電圧源列で構成され、上位ビットに対応するセグメント型定電流源列あるいは定電圧源列中のすべての定電流源あるいは定電圧源の値が、下位ビットに対応する重み付け定電流源列あるいは定電圧源列のフルスケール出力に最下位ビット分の電流値あるいは電圧値を加えた値と同じ値となるように較正されることを特徴とする請求項1または2記載の自己較正型ＤＡ変換器。

5．前記セグメント型定電流源列あるいは定電圧源列が、入力ディジタル値のビット数をＮとしたとき、2^N個以上の数の 定電流源あるいは定

ANALOG EXHIBIT 1002
Page 85 of 321

電圧源からなることを特徴とする請求項３または４記載の自己較正型ＤＡ変換器。

６．前記２進符号に対応して重み付けされた各定電流源列あるいは定電圧源列を構成する定電流源あるいは定電圧源の出力電流値あるいは電圧値を、当該定電流源あるいは定電圧源より下位のビットに対応するすべての定電流源あるいは定電圧源の、出力電流値あるいは電圧値の総和と最下位ビット分の電流値あるいは電圧値を加えた値と同じ値になるように較正することを特徴とする請求項４記載の自己較正型ＤＡ変換器。

７．前記定電流源の出力電流の較正値を、該出力電流を電圧に変換する負荷抵抗と基準電圧源と比較器回路とアップダウンカウンタおよび該定電流源の出力電流を増減させる回路とから成る帰還回路によって決定することを特徴とする請求項３，４または６記載の自己較正型ＤＡ変換器。

８．前記基準電圧源として、較正される複数の定電流源のいずれかを用いることを特徴とする請求項７記載の自己較正型ＤＡ変換器。

９．前記定電圧源の出力電圧の較正値を、基準電圧源と比較器回路とアップダウンカウンタおよび該定電圧源の出力電圧を増減させる回路とから成る帰還回路によって決定することを特徴とする請求項３，４または６記載の自己較正型ＤＡ変換器。

10．前記基準電圧源として、較正される複数の定電圧源のいずれかを用いることを特徴とする請項９記載の自己較正型ＤＡ変換器。

11．比較器回路とＳＡＲとＤＡ変換回路とを有する逐次比較型ＡＤ変換器において、前記ＤＡ変換回路を複数の定電流源で構成し、該定電流源の各出力電流値を変化させることによって、該ＡＤ変換器の出力の非直線性誤差，オフセット誤差，利得誤差のいずれかを低減させることを特徴とする自己較正型ＡＤ変換器。

12．前記定電流源の各出力電流値を変化させる手段を有することを特徴とする請求項11記載の自己較正型ＡＤ変換器。

13．前記複数の定電流源が、同一の電流値を出力する定電流源である、セグメント型ＤＡ変換器であり、該定電流源の出力電流値がすべて同じ値になるように較正することを特徴とする請求項11または12記載の自己較正型ＡＤ変換器。

14．入力ディジタル値の上位ビットに対応する定電流源はセグメント型定電流源列で、下位ビットに対応する定電流源は、２進符号に対応して重み付けされた定電流源列で構成され、上位ビットに対応するセグメント型定電流源列中のすべての定電流源の値が、下位ビットに対応する重み付け定電流源列のフルスケール出力に最下位ビット分の電流値を加えた値と同じ値となるように較正されることを特徴とする請求項11または12記載の自己較正型該ＡＤ変換器。

15．前記セグメント定電流源列は、入力ディジタル値のビット数をＮとしたとき、2^N個以上の数の定電流源から構成されることを特徴とする請求項13または14項記載の自己較正型ＡＤ変換器。

16．前記２進符号に対応して重み付けされた各定電流源列を構成する定電流源の出力電流値を、当該定電流源より下位のビットに対応するすべての定電流源の、出力電流値の総和と最下位ビット分の電流値を加えた値と同じ値になるように較正することを特徴とする請求項14記載の自己較正型ＤＡ変換器。

17．前記定電流源の出力電流の較正値を、該出力電流を電圧に変換する負荷抵抗と基準電圧源と比較器回路とアップダウンカウンタおよび該定電流源の出力電流を増減させる回路とから成る帰還回路によって決定することを特徴とする請求項13，14または16記載の自己較正型ＤＡ変換器。

18．前記基準電圧源として、較正される複数の定電流源のいずれかを用いることを特徴とする請求項17記載の自己較正型ＤＡ変換器。

19．比較器回路とＳＡＲおよび電流出力型のＤＡ変換回路から成る逐次比較型ＡＤ変換器において、前記ＤＡ変換回路の出力電流と負荷抵抗に

ANALOG EXHIBIT 1002
Page 86 of 321

よって参照電圧を発生させ、前記負荷抵抗の抵抗値を変化させることによって、ＡＤ変換出力の非直線性誤差，オフセット誤差，利得誤差のいずれかを低減させることを特徴とする自己較正型ＡＤ変換器。

20．前記負荷抵抗の抵抗値を変化させる手段を有することを特徴とする請求項19記載の自己較正型ＡＤ変換器。

21．前記該負荷抵抗の抵抗値を変化させる手段が、前記負荷抵抗と並列に、複数の抵抗器が任意の数だけ接続あるいは切り離しされる回路で構成されることを特徴とする請求項20記載の自己較正型ＡＤ変換器。

3．発明の詳細な説明

〔産業上の利用分野〕

本発明は、自己較正型ＤＡ変換器およびこれを用いる高精度の自己較正機能を有する逐次比較型ＡＤ変換器に関する。

〔従来の技術〕

一般に、12ビット以上のＡＤ変換器をＬＳＩにレイで構成したものである。各ビットに対応するキャパシタの容量は、各々重み付けされており、自己較正は、それらの容量比が常に一定となる如く、各キャパシタの容量値を調整することによって達成される。また、自己較正動作はＡＤ変換動作の合間をぬって行われ、見掛け上、特別な較正時間を設けなくてもよくなっている。

〔発明が解決しようとする課題〕

上記従来技術においては、ＤＡ変換回路部分にキャパシタ・アレイを使用するため、逐次比較操作によって行われるＡＤ変換に要する時間は、それらのキャパシタを充放電する時間によって制限される。このため、高速化には限界があった。また、キャパシタ・アレイに蓄えられた電荷による電圧でアナログ電圧レベルを表現するので、電荷を一定に保つ回路を構成するのが難しいバイポーラ・プロセスでは、この技術を使用することができなかった。

本発明は上記事情に鑑みてなされたもので、その目的とするところは、従来の技術における上述の如き問題を解消し、高速かつ高精度の自己較正型ＤＡ変換器、および、これを用いる自己較正機能を有する逐次比較型ＡＤ変換器を提供することにある。

〔課題を解決するための手段〕

本発明の上記目的は、複数の定電流源あるいは定電圧源で構成されるＤＡ変換器において、前記定電流源あるいは定電圧源各々の出力電流値あるいは電圧値を変化させることによって、前記ＤＡ変換器の出力の非直線性誤差，オフセット誤差，利得誤差のいずれかを低減させることを特徴とする自己較正型ＤＡ変換器、および、比較器回路とＳＡＲとＤＡ変換回路とを有する逐次比較型ＡＤ変換器において、前記ＤＡ変換回路を複数の定電流源で構成し、該定電流源の各出力電流値を変化させることによって、該ＡＤ変換器の出力の非直線性誤差，オフセット誤差，利得誤差のいずれかを低減させることを特徴とする自己較正型ＡＤ変換器によって達成される。

〔作用〕

する場合、プロセス精度に依存する素子特性のばらつきがあるため、何らかの較正を施さないと非直線性誤差等が所望の範囲には収まらない。この較正方法として、従来はレーザ・トリミング技術が主に用いられてきた。しかし、このレーザ・トリミング技術では、大量のＬＳＩに対して一括して較正を施すことはできないため、コストがかかり、また、この較正は製作時の１度しかできないため、経時変化による誤差を較正することは不可能であった。

このような問題を解決するため、最近では、自己較正機能を持たせたＡＤ変換ＬＳＩが開発されている。これについては、例えば、「Ａ-Ｄ変換器ＬＳＩをチップ上で較正する，12，16ビットの製品に適用」(日経エレクトロニクス,1988年6月27日号、pp.201～209)等に詳述されている。ここで紹介されているＡＤ変換器ＬＳＩは、電荷再分配型の逐次比較方式のものである。これは、第11図に示す如く、一般的な逐次比較方式のＡＤ変換器において、そのＤＡ変換回路部分をキャパシタ・ア

ANALOG EXHIBIT 1002
Page 87 of 321

本発明に係る自己較正型ＤＡ変換器は、複数の定電流源あるいは定電圧源から構成される。そして、上記定電流源あるいは定電圧源各々の出力電流値あるいは電圧値を較正する回路は、すべての定電流源あるいは定電圧源の出力値が、常に適切な値となるように調整を行う。これによってＤＡ変換回路の非直線性誤差が低減される。また、上述のＤＡ変換回路を用いて逐次比較型ＡＤ変換器を構成すれば、ＡＤ変換器としての精度が較正されるようになる。

更に、上記ＤＡ変換回路の出力電流と負荷抵抗によって、逐次比較動作に必要な参照電圧を発生させれば、キャパシタ・アレイを用いたＤＡ変換器を用いた場合に比べ、逐次比較動作に用いる参照電圧の発生が高速になり、ＡＤ変換動作の高速化を図ることが可能となる。

〔実施例〕

以下、本発明の実施例を図面に基づいて詳細に説明する。

第１図は本発明の一実施例を示す自己較正型ＡＤ変換器の全体のブロック図である。Ｖinより入力されたアナログ信号は、第１図中の変換用コンパレータ１と、ＳＡＲ（Successive App-roximation Register）２と、主ＤＡ変換回路（以下、「主ＤＡＣ」という）３と、負荷抵抗41,42とによって、よく知られた逐次比較方式でＡＤ変換される。変換出力ディジタル信号は、ラッチ回路６によって保持される。

上述の主ＤＡＣ３は、電流出力型のＤＡ変換回路で、セグメント型定電流源列31と、ＳＡＲ２からの入力ディジタル値をセグメントコードに変換するセグメントデコーダ32から成る。

上記セグメント型定電流源列31は、第２図に示す如く、同じ値を発生する複数の定電流源 311から構成される。また、上記各定電流源 311には、それぞれ、較正回路 312が付加されている。この較正回路 312は、定電流源 311の出力値を微小に変化させる。更に、各較正回路 312には、較正値保持回路 313が付属している。また、利得調整回路 314は、すべての定電流源 311の出力電流値をその比を保ったまま変化させる。これらの定電流源 311としては、例えば、第３図中に示す如きバイポーラトランジスタと抵抗器とからなる定電流源回路が、また、較正回路 312および利得調整回路 314としては、例えば、第３図中に示す如き小規模なＤＡ変換回路等が考えられる。較正値保持回路 313としては、一般的なレジスタ回路等が考えられる。

一方、第１図に示した較正値検出回路５は、第４図に示す如く、較正用コンパレータ51と、アップダウンカウンタ（以下、「ＵＤＣ」という）52と、負荷抵抗53とからなる。なお、コンパレータ出力はＵＤＣ52のＵＰ／ＤＯＷＮ制御入力に接続されている。

上述の如く構成される主ＤＡＣ３の較正は、以下のように行われる。まず、主ＤＡＣ３中の各定電流源 311は、スイッチの切替えによって、一つずつ順次この較正用コンパレータ51の入力端の一方に接続される。次に、その電流値と負荷抵抗53とで発生する電圧が、外部から与えられる基準電圧 Ｖrefと比較される。

定電流源 311の出力電流と負荷抵抗53とで発生する電圧が上記 Ｖrefより大きかった場合、コンパレータ51の出力は論理“１”レベルとなり、これを受けてＵＤＣ52は、その出力ディジタル値を１ずつ増加させる。これを受ける較正回路 312は、定電流源 311のトランジスタのベース電位を上げて、定電流源 311の出力電流を増加させる。この結果、定電流源 311の出力電流と負荷抵抗53とで発生する電圧は下降し Ｖrefより小さくなる。そのため、今度はコンパレータ51の出力は論理“０”となり、ＵＤＣ52は出力値を減少させて、較正回路 312は定電流源 311の出力を減少させる。そして、再びコンパレータ出力は論理“１”となる。この動作が繰り返され、ＵＤＣ52出力が収束するようになったら、その時のＵＤＣ52の出力を較正値として、較正値保持回路 313に記憶させておく。そしてＡＤ変換動作時には、この較正値によって補正された出力を出すようにする。

このような動作をすべての定電流源 311に対し

ANALOG EXHIBIT 1002
Page 88 of 321

て行えば、それらの出力値はすべて等しいものとなり、主ＤＡＣ３として見たときには、その非直線性誤差が低減される。このため、この主ＤＡＣ３を用いた逐次比較型ＡＤ変換器は、その非直線性誤差が低減される。なお、セグメント型定電流源列31を構成する定電流源の数は、ＤＡ変換回路３への入力ビット数をＮとすると、2^N-1個あれば十分である。しかし、定電流源を2^N-1個より多く用意すれば、ＡＤ変換動作時に使用されずに余っている定電流源の較正を、ＡＤ変換動作と並行してが行うことができることになり、自己較正のための時間を、ＡＤ変換動作に使用する時間以外に取る必要がなくなる。

主ＤＡＣ３の非直線性誤差を上記の方法で較正した後、主ＤＡＣ３へのディジタル入力の全ビットを論理“１”としてフルスケール出力させ、アナログ入力端Ｖinにはフルスケール電圧を与え、変換用比較器１をＵＤＣ51に接続し、ＵＤＣ52の出力を前述の利得調整回路 314に接続する。利得調整回路 314は、主ＤＡＣ３中のセグメント型定電流源列31のすべての定電流源の出力電流を、それらの比を保ったまま変化させる。このループにおいても、上述の非直線性誤差の較正の場合と同様にＵＤＣ52の出力の収束が起こり、収束時のＵＤＣ出力を利得較正値として利得調整回路 314に使用すれば、主ＤＡＣ３の利得誤差を較正できる。

更に、主ＤＡＣ３へのディジタル入力の全ビットを論理“０”としてゼロスケール出力させ、アナログ入力端Ｖinにはゼロスケール電圧を与え、変換用比較器１をＵＤＣ51に接続し、ＵＤＣ52の出力をオフセット調整回路 315に接続する。オフセット調整回路 315は、主ＤＡＣ３中のセグメント型定電流源列31の出力電流に、オフセット電流を重畳させる。このループにおいても上記の非直線性誤差の較正、および利得較正の場合と同様に、ＵＤＣ52の出力の収束が起こり、収束時のＵＤＣ出力をオフセット較正値としてオフセット調整回路 315に使用すれば、主ＤＡＣ３のオフセット誤差を較正できる。

なお、この利得誤差較正およびオフセット誤差較正は、上述のようにフルスケールやゼロスケールで行わずに、主ＤＡＣ３へのディジタル入力の最上位ビットのみを論理“１”とした中間スケールで行っても、同様の効果が得られる。

さて、上述の第一の実施例では、較正値を見出す方法として、各定電流源の電流値と負荷抵抗53とで発生する電圧を、外部から与えられる較正用基準電圧 Ｖrefと比較する方法を採っていた。しかし、第５図に示す如く、外部から与えられる基準電圧Ｖrefの代わりに、較正用基準電流源Ｉrefと、負荷抵抗53と同じ値を持つもう一つの負荷抵抗54とを用意し、これらで発生する電圧を用いても同様の効果が得られることは明らかである。

更に、第６図に示す如く、上述の較正用基準電流源 Ｉrefとして、その時較正を実施している定電流源 311以外の他の定電流源 311を用いて、互いに等しい電流値になるように較正しても、同様の効果が得られることは明らかである。

一方、このような比較を行う際に必要な負荷抵抗53および54の値は、速度が許す限り大きくし、コンパレータへの入力振幅を大きくとった方が、コンパレータ自身のゲインを小さく設定できるため、発振などのトラブルを避けやすくなる。

次に、本発明の第二の実施例について説明する。

上述の第一の実施例においては、主ＤＡＣ３をセグメント型定電流源列31によって構成する例を説明した。しかし、この主ＤＡＣ３を第７図に示す如く、入力ディジタル値の上位ビットに対応する部分と下位ビットに対応する部分とに分け、前者をセグメント型定電流源で、後者を重み付け定電流源で構成し、前者についてのみ上記第一の実施例で示したような較正を行っても、実用上充分な精度を得られる場合もある。

また、セグメント型定電流源31の替わりに、すべて重み付け定電流源で構成されたＤＡ変換回路を使用し、

$$I_{MSB}=\frac{I_{MSB}}{2}+\cdots\cdots+I_{LSB}+I_{LSB}' \quad (1)$$

$$\frac{I_{MSB}}{2}=\frac{I_{MSB}}{4}+\cdots\cdots+I_{LSB}+I_{LSB}' \quad (2)$$

ANALOG EXHIBIT 1002
Page 89 of 321

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となる如く各定電流源を較正しても、上述の実施例と同様な効果を得ることができる。但し、上述の式(1),(2)中のI_{LSB}'は、最下位ビット分の電流を発生させるダミー電流源の出力値を意味している。

次に、本発明の第三の実施例について説明する。

上記各実施例においては、定電流源の値を微小に変更する方法として、各定電流源ごとに用意した較正回路 312を用いていた。しかし、第８図に示す如く、較正回路 312と較正値保持回路 313を取り除いた主ＤＡＣ３ａ中に用いる定電流源列とは別に、較正用補助定電流源７を主ＤＡＣ３ａと並列に設け、その時ＯＮとなる主ＤＡＣ３ａ中の定電流源の各々の較正値の総和電流を、この較正用補助定電流源回路７で加えてやることによっても、前述の実施例と同様の効果を得ることができる。もちろん、この場合には、ＤＡ変換回路中の各定電流源の較正値を、前述の第一、第二の実施例に示した方法等で、あらかじめ見出しておく必要がある。

次に、本発明の第四の実施例について説明する。

前述の各実施例においては、主ＤＡＣ３の非直線性誤差を較正する方法として、主ＤＡＣ３の出力電流値を微小に変化させる方法を採っていた。しかし、第９図に示す如く、変換用コンパレータ１の入力に接続されている負荷抵抗41の値を微小に変化させる可変抵抗回路８を設け、主ＤＡＣ３の非線形性を補うように、負荷抵抗41の値を変化させることによっても、前記実施例と同等の効果を得ることができる。この負荷抵抗値を微小に変化させる可変抵抗回路８としては、例えば、第10図に示す如き、負荷抵抗41に並列に接続される複数の小抵抗と、較正する量に応じてそれらの小抵抗を接続したり切離したりする複数のスイッチ群とからなる回路が考えられる。もちろん、この場合にも、ＤＡ変換回路中の定電流源の各々に対する負荷抵抗41の較正量を、前述の第一、第二の実施例に示した方法等で、あらかじめ見出しておく必要がある。

〔発明の効果〕

以上、詳細に説明した如く、本発明によれば、温度変化や経時変化によって生じる非直線性誤差を、常に較正できる自己較正回路を内蔵した逐次比較型ＡＤ変換器の、高速化を図ることが出来ると共に、そのような逐次比較型ＡＤ変換器をバイポーラプロセスによって製造することが可能となり、高速かつ高精度な自己較正型ＤＡ変換器および、これを用いる自己較正型ＡＤ変換器を実現できるという顕著な効果を奏するものである。

4．図面の簡単な説明

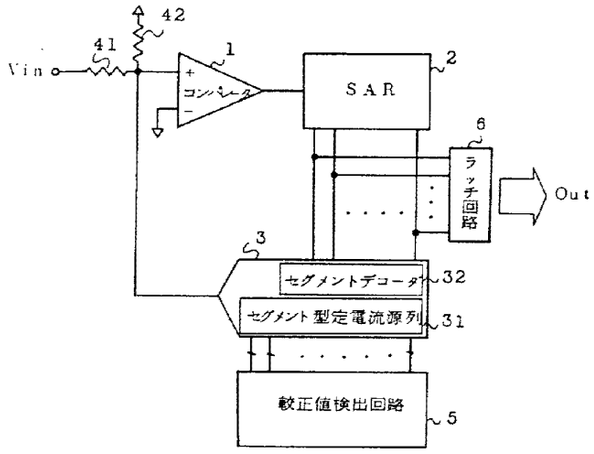
第１図は本発明の第一の実施例を示すブロック図、第２図は第１図中の主ＤＡＣに使用されているセグメント型定電流源列の詳細図、第３図は第２図中の定電流源と較正回路の具体例を示す図、第４図は第１図中の較正回路の詳細を示す図、第５図は第４図の較正回路で使用する基準となる電圧の第２の発生方法を示す図、第６図は第４図の較正回路で使用する基準となる電圧の第３の発生方法を示す図、第７図は本発明の第二の実施例の主ＤＡ変換回路部分の詳細を示す図、第８図は本発明の第三の実施例を示すブロック図、第９図は本発明の第四の実施例のブロック図、第10図は第９図中に示された負荷抵抗を微小に変化させる手段の一例を示す図、第11図は従来の例を示す図である。

１：変換用コンパレータ、２：ＳＡＲ、３，３ａ：主ＤＡ変換回路、31：セグメント型定電流源列、311：定電流源、312：較正回路、313：較正値保持回路、314：利得調節回路、315：オフセット調節回路、32：セグメントデコーダ、41，42：負荷抵抗、５：較正値検出回路、51：較正用コンパレータ、52：アップダウンカウンタ、53，54：負荷抵抗、６：ラッチ回路、７：較正用補助定電流源回路、８：可変抵抗回路。

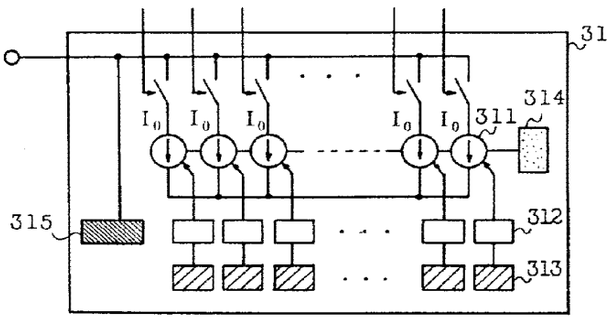
代理人　弁理士　磯村雅俊

ANALOG EXHIBIT 1002
Page 90 of 321

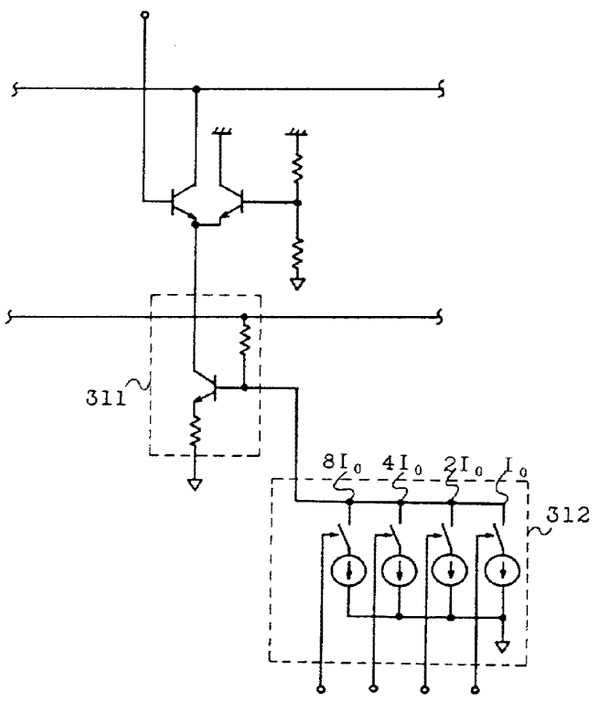
第　1　図



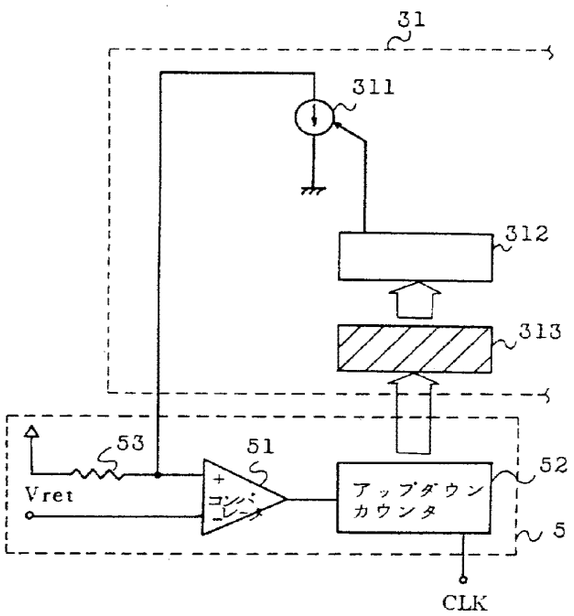
第　2　図



第　3　図

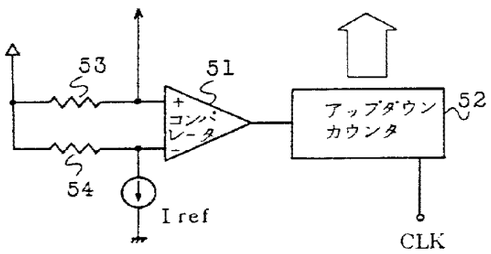


第　4　図

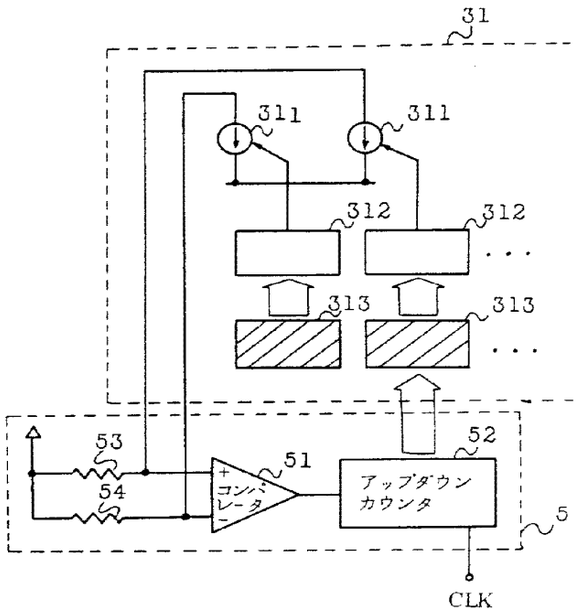


ANALOG EXHIBIT 1002
Page 91 of 321

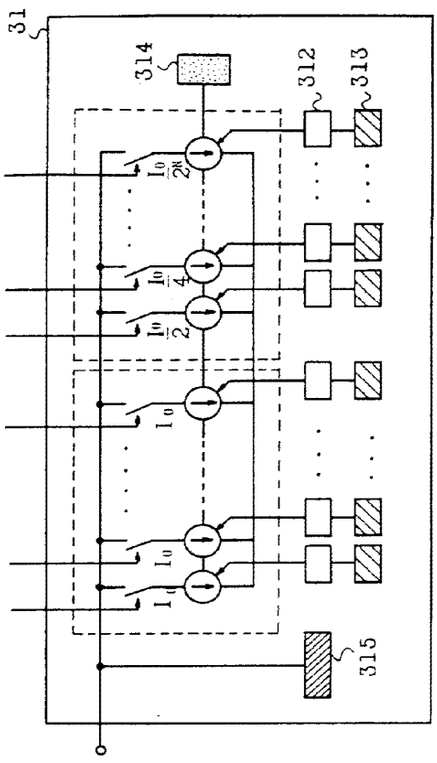
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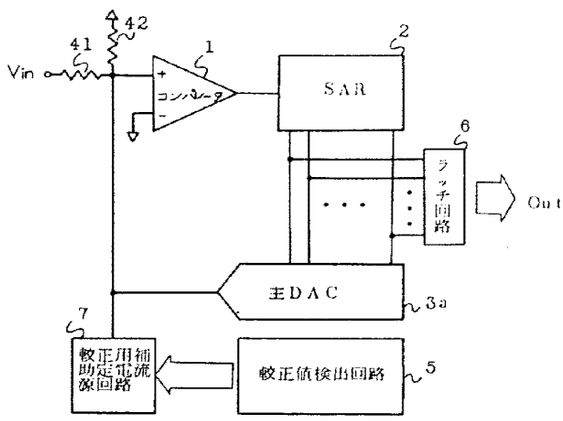
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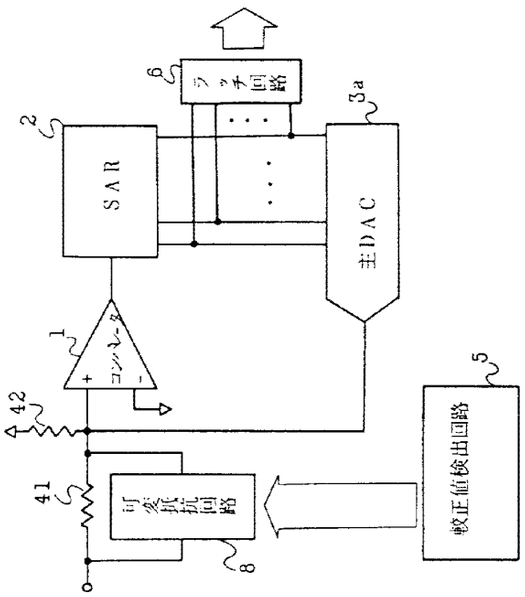


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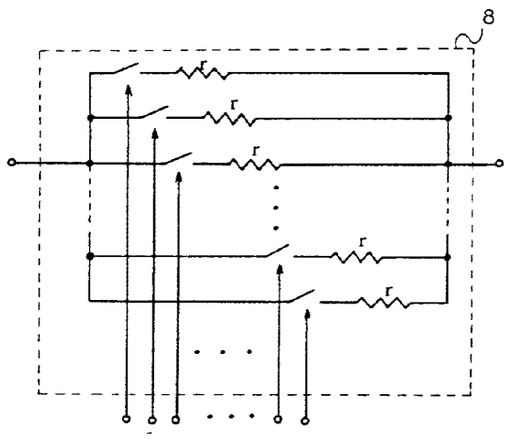


ANALOG EXHIBIT 1002
Page 92 of 321

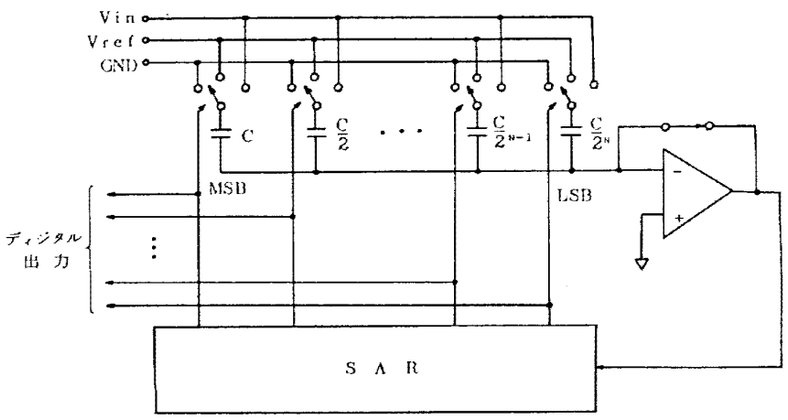
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第　１１　図



ANALOG EXHIBIT 1002
Page 93 of 321

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ANALOG EXHIBIT 1002
Page 94 of 321

Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization

CHRISTIAN C. ENZ, MEMBER, IEEE, AND GABOR C. TEMES, FELLOW, IEEE

Invited Paper

In linear IC's fabricated in a low-voltage CMOS technology, the reduction of the dynamic range due to the dc offset and low-frequency noise of the amplifiers becomes increasingly significant. Also, the achievable amplifier gain is often quite low in such a technology, since cascoding may not be a practical circuit option due to the resulting reduction of the output signal swing. In this paper, some old and some new circuit techniques will be described for the compensation of the amplifier most important nonideal effects including the noise (mainly thermal and $1/f$ noise), the input-referred dc offset voltage, as well as the finite gain resulting in a nonideal virtual ground at the input.

I. INTRODUCTION[1]

In linear active circuits, the active element most often used is the operational amplifier (op-amp), whose main function in the circuit is to create a virtual ground, i.e., a node with a zero (or constant) voltage at its input terminal without sinking any current. Using op-amps with MOS input transistors, the op-amp input current at low frequencies can indeed be made extremely small; however, the input voltage of a practical op-amp is usually significantly large (typically of the order of 1–10 mV), since it is affected by several nonideal effects. These include noise (most importantly, $1/f$ and thermal noise), the input-referred dc offset voltage, as well as the signal voltage needed to generate the desired output voltage of the op-amp. Normally, the thermal noise occupies a wide frequency band, while the $1/f$ noise, offset and input signal are narrowband low-frequency signals.

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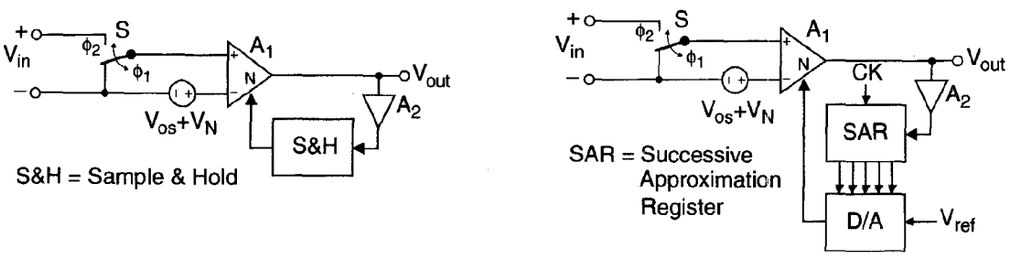
[1] This work is dedicated to Prof. Karoly Simonyi on his 80th birthday.

The purpose of the circuit techniques discussed in this paper is to reduce the effects of the narrow-band noise sources at the virtual ground of an op-amp stage. By reducing the low-frequency noise and offset at the op-amp input, hence the dynamic range of the circuit is improved; by reducing the signal voltage at the virtual ground terminal, the effect of the finite low-frequency gain of the op-amp on the signal-processing characteristics of the stage is decreased. Both improvements are especially significant for low-supply voltage circuits, which have limited signal swings and where the op-amp gain may be low since headroom for cascoding may not be available. The proposed techniques are applicable to such important building blocks as voltage amplifiers, ADC and DAC stages, integrators and filters, sample-and-hold (S/H) circuits, analog delay stages, and comparators.

Sections II and III present the two basic techniques that are used to reduce the offset and low-frequency noise of op-amps, namely the autozero (AZ) and chopper stabilization (CHS) techniques. A clear distinction is made between autozeroing, which is a sampling technique, and CHS, which is a modulation technique, mainly with respect to their effect on the amplifier broadband noise. The correlated double sampling (CDS) technique is described in Section II as a particular case of AZ where, as its name indicates, the amplifier noise and offset are sampled twice in each clock period. Then, Section IV treats the most important practical issues at the transistor and circuit level that are faced when implementing the offset and noise reduction techniques discussed previously. Section V presents fundamental building blocks that are used for sampled-data analog signal processing. They are all realized as switched-capacitor (SC) circuits and therefore exploit the CDS technique not only for reducing the offset and the $1/f$ noise, but also to lower the sensitivity of the circuit performance to the finite amplifier gain. Examples of SC S/H stages, voltage amplifiers, integrators, and filters are

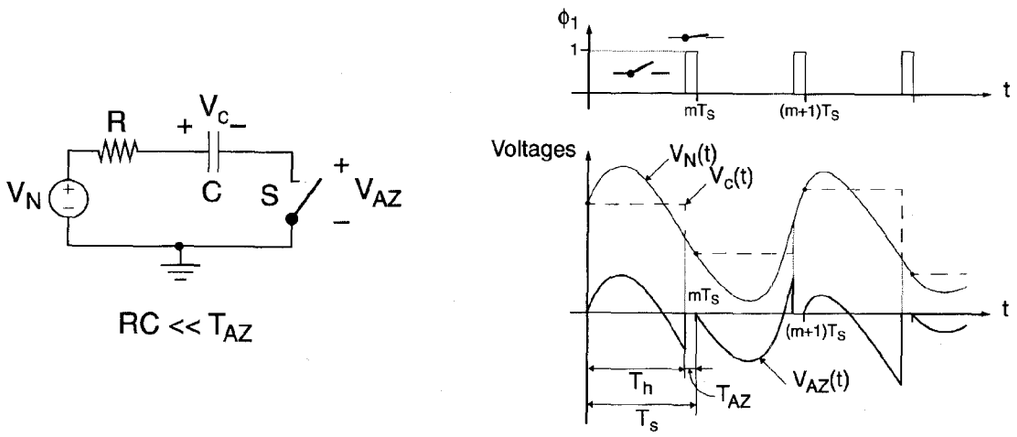
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ANALOG EXHIBIT 1002
Page 95 of 321



(a) (b)

Fig. 1. Basic autozeroed stages. (a) Analog offset control storage and (b) digital offset control storage.



(a) (b)

Fig. 2. (a) Basic AZ circuit and autozeroed signal: (b) shows voltages in (a).

presented. An example of the use of the CHS technique to realize a low-noise and low-offset micropower amplifier for intrumentation applications is presented in Section VI. Finally, a summary is given in Section VII, where the two techniques discussed in this paper are compared.

II. Autozeroing and Correlated Double Sampling Techniques

In this section, the principle of AZ and CDS techniques will be introduced and their effect on offset and noise analyzed.

A. Basic Principle

The basic idea of AZ is sampling the unwanted quantity (noise and offset) and then subtracting it from the instantaneous value of the contaminated signal either at the input or the output of the op-amp. This cancellation can also be done at some intermediate node between the input and the output of the op-amp, using an additional input port defined as the nulling input and identified with the letter N in the schematics of Fig. 1.

If the noise is constant over time (like a dc offset) it will be cancelled, as needed in a high-precision amplifier or high-resolution comparator. If the unwanted disturbance is low-frequency random noise (for example, $1/f$ noise), it will be high-pass filtered and thus strongly reduced at low frequencies but at the cost of an increased noise floor due to aliasing of the wideband noise inherent to the sampling process. The general principle of the AZ process will first be described considering only the input referred dc offset voltage V_{os} and will then be extended to the input referred random noise voltage V_N.

The AZ process requires at least two phases: a sampling phase (ϕ_1) during which the offset voltage V_{os} and the noise voltage V_N are sampled and stored, and a signal-processing phase (ϕ_2) during which the offset-free stage is available for operation. The two major categories of AZ are shown in Fig. 1. During the sampling phase (shown in Fig. 1), the amplifier is disconnected from the signal path, its inputs are short-circuited and set to an appropriate common-mode voltage. The offset is nulled using an auxiliary nulling input port N by means of an appropriate feedback configuration and/or a dedicated algorithm. The control quantity x_c is next sampled and stored, either in an analog form as a voltage using a S/H stage [Fig. 1(a)] or in a digital form, using for example a register [Fig. 1(b)]. The output V_{out} is forced to a small value in these particular configurations. The input terminals of the amplifier can afterwards be connected back to the signal source for amplification. If

ANALOG EXHIBIT 1002
Page 96 of 321

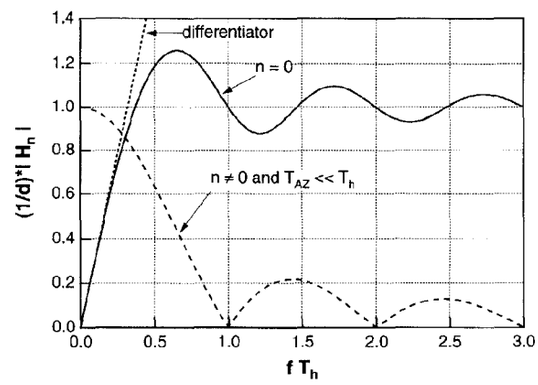


Fig. 3. Autozero baseband and foldover bands transfer functions.

it is used under the same conditions as during sampling, the amplifier will ideally be free from any unwanted offset.

B. The Effect of AZ on the Noise

The autozero principle can be used not only to cancel the amplifier offset but also to reduce its low-frequency noise, for example $1/f$ noise. But unlike the offset voltage, which can be considered constant, the amplifier's noise and particularly its wideband thermal noise component is time-varying and random. The efficiency of the AZ process for the low-frequency noise reduction will thus strongly depend on the correlation between the noise sample and the instantaneous noise value from which this sample is subtracted. The autocorrelation between two samples of $1/f$ noise separated by a time interval τ decreases much slower with increasing τ than it does for white noise, assuming they have the same bandwidth. The AZ process is thus efficient for reducing the $1/f$ noise but not the broadband white noise.

Another way of looking at the effect of AZ is to note that it is equivalent to subtracting from the time-varying noise a recent sample of the same noise. For dc or very low-frequency noise this results in a cancellation. This indicates that AZ effectively high-pass filters the noise.

In addition to this basic high-pass filtering process, since AZ is a sampling technique, the wideband noise is aliased down to the baseband, increasing the resulting in-band power spectral density (PSD) unless the system is already a sampled-data one.

The effects of AZ on the amplifier's noise can be better understood by analyzing the simple circuit shown in Fig. 2, where source V_N may represent the noise at the output of the amplifier in the autozero phase [see, i.e., Fig. 21(a)]. Each time switch S is closed, the output voltage V_{AZ} is reset to zero and the noise source voltage V_N appears across resistor R and capacitor C. Assuming $RC \ll T_{\mathrm{AZ}}$, at the end of the sampling phase (when switch S opens) the noise voltage V_N is sampled onto capacitor C. The output voltage becomes equal to the difference between the instantaneous voltage V_N and the voltage V_c stored on capacitor C. This eliminates the dc component of V_N, but not its time-varying part. It can be shown [8] that if source voltage $V_N(t)$ corresponds to a stationary random noise with a PSD $S_N(f)$, the PSD of the autozero voltage across the switch can be decomposed into two components: one caused by the baseband noise (which is reduced by the AZ process) and the other by the foldover components introduced by aliasing. Thus

$$S_{\mathrm{AZ}}(f) = \underbrace{|H_0(f)|^2 S_N(f)}_{\text{baseband}} + \underbrace{S_{fold}(f)}_{\text{foldover}} \tag{1}$$

where

$$S_{\mathrm{fold}}(f) \equiv \sum_{\substack{n=-\infty \\ n\neq 0}}^{+\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right). \tag{2}$$

The foldover component results from the replicas of the original spectrum shifted by the integer multiples of the sampling frequency. The baseband transfer function $|H_0(f)|^2$ is given by (see (3) at the bottom of the page) where $d \equiv T_h/T_s$ is the duty cycle of the clock signal [Fig. 2(b)]. The magnitude of $H_0(f)$ normalized to the duty cycle d is plotted as a function of fT_h in Fig. 3, which shows its high-pass characteristic. Note that for $\pi f T_h \ll 1$, $H_0(f)$ acts like a differentiator

$$|H_0(f)| \cong \pi f T_h. \tag{4}$$

It imposes a zero at the origin of frequency axis that cancels out any dc component present in $V_N(t)$. The other transfer functions $|H_n(f)|^2$ for $n \neq 0$ are derived in the Appendix. Their shape depends on the duty cycle d, but they all merge to a common function in the case the AZ time T_{AZ} can be considered much smaller than the hold time ($T_{\mathrm{AZ}} \ll T_h$)

$$|H_n(f)|^2 \cong [d \cdot \operatorname{sinc}(\pi f T_h)]^2 \quad \text{for } n \neq 0 \text{ and } T_{\mathrm{AZ}} \ll T_h \tag{5}$$

where $\operatorname{sinc}(x) \equiv \sin(x)/x$. $|H_n(f)|$ is plotted in Fig. 3.

The PSD at the output of the AZ circuit clearly depends on the PSD of the source which is autozeroed. The low-frequency input-referred noise PSD of an amplifier generally contains both a white and a $1/f$ noise component. It can be written in the following convenient form:

$$S_N(f) = S_0\left(1 + \frac{f_k}{|f|}\right) \tag{6}$$

$$|H_0(f)|^2 = d^2\left\{\left[1 - \frac{\sin(2\pi f T_h}{2\pi f T_h}\right]^2 + \left[\frac{1-\cos(2\pi f T_h)}{2\pi f T_h}\right]^2\right\} \tag{3}$$

ANALOG EXHIBIT 1002
Page 97 of 321

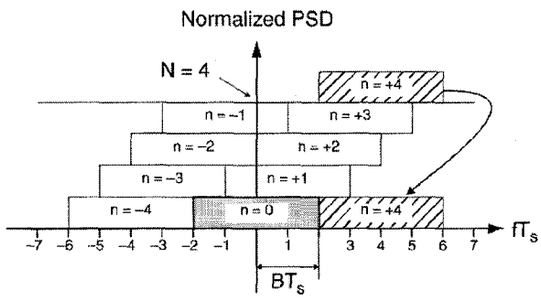


Fig. 4. Aliasing of an ideally low-pass filtered white noise having a bandwidth equal to twice the sampling frequency.

where S_0 represents the white noise PSD and f_k is the corner frequency, defined as the frequency for which the $1/f$ noise PSD becomes equal to the white noise S_0. The corner frequency of amplifiers having MOS input devices can be relatively high (typically ranging from 1 kHz to as high as 100 kHz), which means that in the absence of aliasing the input noise is often dominated by the $1/f$ noise component in the frequency range of interest. The effect of AZ will be examined separately for each of these PSD components, starting with the white noise.

The foldover component defined by (2) can easily be calculated if the amplifier's broadband white noise is considered as an ideally low-pass filtered white noise having a bandwidth equal to B. The aliasing effect introduced by the sampling process in this case is illustrated in Fig. 4 for $BT_s = 2$ (i.e., for a noise bandwidth B = four times the Nyquist frequency). Fig. 4 clearly shows the effect of undersampling the broadband white noise: the original noise power spectrum is shifted by multiples n of the sampling frequency and summed, resulting in a white noise of PSD value approximately equal to NS_0, where N is the integer closest to the *undersampling factor* defined by $2BT_s$. Thus

$$\sum_{n=-\infty}^{+\infty} S_N\left(f - \frac{n}{T_s}\right) \cong 2BT_sS_0. \tag{7}$$

The signal corresponding to (7) has no physical reality since its power is infinite. The power is actually bounded by the $\text{sinc}^2(\pi fT_s)$ function introduced by the hold operation. The foldover component in the Nyquist range is then simply derived from (7) by subtracting the original band ($n = 0$) and multiplying the remainder by the $\text{sinc}^2(\pi fT_s)$ function:

$$S_{\text{fold-white}}(f) = (2BT_s - 1)S_0 \,\text{sinc}^2(\pi fT_s). \tag{8}$$

This result can be extended to the case of a first-order low-pass filtered white noise with a PSD

$$S_{N\text{-white}}(f) = \frac{S_0}{1 + \left(\frac{f}{f_c}\right)^2} \tag{9}$$

where f_c is the 3-dB noise bandwidth, which typically corresponds to the amplifier gain-bandwidth product when the noise is sampled with the op-amp in a unity-gain configuration. Therefore, f_c is generally much larger than the sampling frequency $f_s \equiv 1/T_s$. The detailed analysis given in [8] shows that (8) also holds for the foldover component of a first-order low-pass filtered white noise if B is replaced by the equivalent noise bandwidth defined by

$$B \equiv \frac{1}{S_0}\int_{-\infty}^{+\infty} S_{N\text{-white}}(f)\,df = \frac{\pi}{2}f_c. \tag{10}$$

If the undersampling factor $2BT_s = \pi f_cT_s$ is much larger than unity, the foldover component dominates, since the baseband term $|H_0(f)|^2$ is bounded by 1.6. The autozeroed white noise is thus dominated by the aliased broadband noise component and can be approximated by

$$S_{\text{AZ}} - \text{white}(f) \cong S_{\text{fold}} - \text{white}(f) \cong (pif_cT_s - 1)S_0\,\text{sinc}^2(\pi fT_s). \tag{11}$$

The PSD of a first-order low-pass filtered white noise having a bandwidth five times larger than the sampling frequency[2] ($f_cT_s = 5$) and the different PSD components resulting from the AZ process are plotted in Fig. 5. It clearly shows that the autozeroed noise PSD is dominated by the foldover component in the Nyquist band ($|fT_s| \leq 0.5$).

A similar analysis can be carried out for a first-order low-pass filtered $1/f$ noise having a PSD given by

$$S_{N-1/f}(f) = \frac{S_0f_k}{|f|\left[1 + \left(\frac{f}{f_c}\right)^2\right]}. \tag{12}$$

As shown in Fig. 6, the input $1/f$ noise is zeroed, removing the original divergence of the $1/f$ noise occurring at the origin of frequency. Although $1/f$ noise has a narrow bandwidth, it still has a foldover component due to the aliasing of all the tails of the $1/f$ noise. This foldover component and the original baseband PSD are plotted in Fig. 6 for $f_cT_s = 5$ and for a corner frequency equal to the sampling frequency ($f_kT_s = 1$).

The foldover component for the $1/f$ noise can be approximated [8] in the Nyquist range by

$$S_{\text{fold-}1/f} \cong 2S_0f_kT_s[1 + \ln(\tfrac{2}{3}f_cT_s)]\text{sinc}^2(\pi fT_s). \tag{13}$$

Comparing $S_{\text{fold-}1/f}$ to the corresponding term obtained for the white noise (8), it can be seen that it increases proportionally to f_cT_s for the white noise, but only logarithmically for the $1/f$ noise. The effect of aliasing on the $1/f$ noise is thus not as dramatic as on the broadband white noise.

The PSD at the output of the AZ circuit at low frequencies, considering both the white and the $1/f$ component given by (6) and assuming $\pi f_cT_s \gg 1$, can simply be obtained from (11) and (13):

$$S_{\text{AZ}}(f) = |H_0(f)|^2S_N(f) + S_{\text{fold}} \tag{14}$$

[2]This selection reflects the requirement $f_cT_s \geq 5$ needed for the full settling of an SC stage [10].

ANALOG EXHIBIT 1002
Page 98 of 321

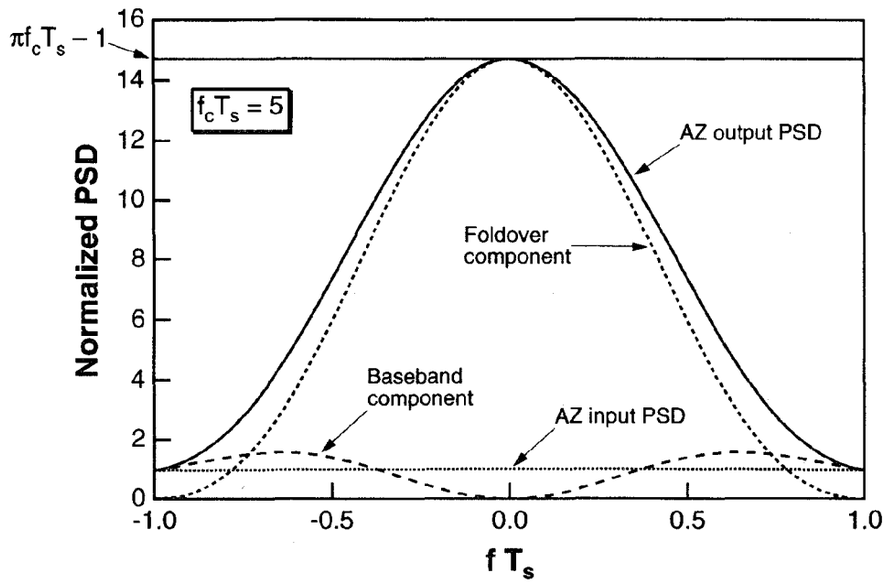


Fig. 5. Effect of the AZ process on a first-order low-pass filtered white noise with a bandwidth five times larger than the sampling frequency.

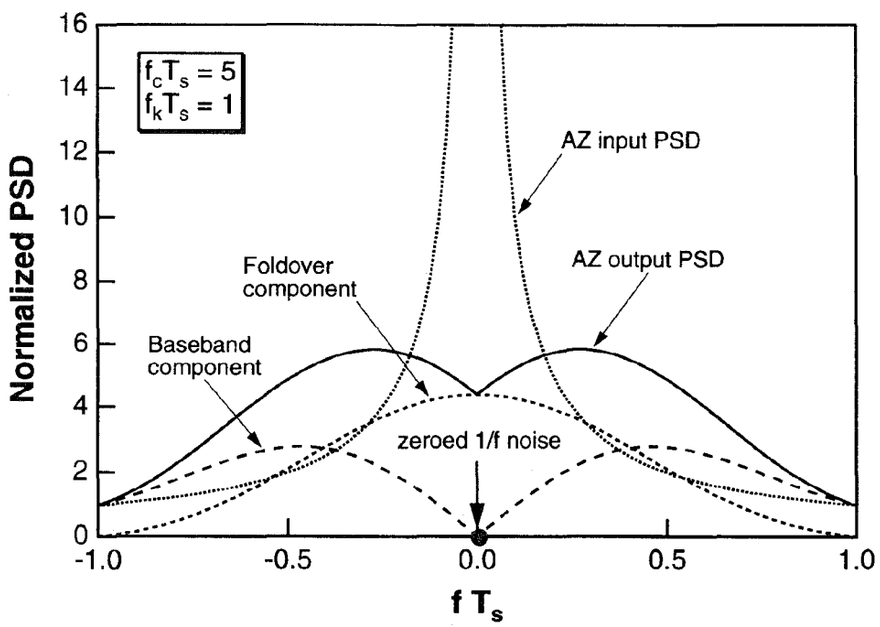


Fig. 6. Effect of the AZ process on a first-order low-pass filtered $1/f$ noise having a bandwidth five times larger than the sampling frequency.

where the total foldover component is given by

$$S_{\text{fold}} = S_0\{(\pi f_c T_s - 1) + 2f_k T_s[1 + \ln(\tfrac{2}{3} f_c T_s)]\} \cdot \text{sinc}^2(\pi f T_s). \quad (15)$$

The corner frequency for which the $1/f$ noise foldover component [given by (13)] is equal to the foldover component coming from the white noise [as given by (8)] is plotted against the normalized white-noise bandwidth in Fig. 7. The total foldover term given by (15) is thus dominated by the $1/f$ noise contribution for parameter values $(f_k T_s, f_c T_s)$ falling in the region above this curve, while it is dominated by the broadband white noise contribution below the curve. For example, an amplifier autozeroed at 100 kHz and having a gain-bandwith product equal to $7 \times f_s = 700$ kHz should have a corner frequency larger than $4.13 \times f_s = 413$ kHz for the $1/f$ noise foldover to dominate.

ANALOG EXHIBIT 1002
Page 99 of 321

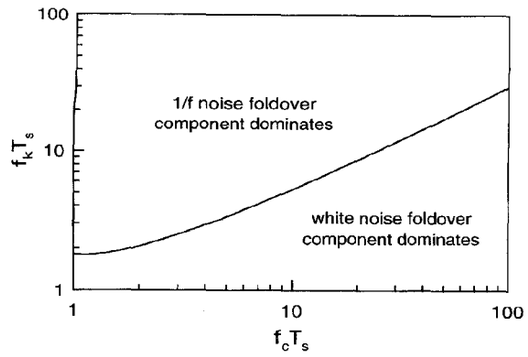


Fig. 7. Comparison between the $1/f$ and white noise contribution to the total foldover component as a function of the white-noise bandwidth.

This demonstrates that in most practical cases the foldover component is dominated by the broadband white noise.

In conclusion, it was shown in this section that the AZ process not only cancels the amplifier's offset, but it also strongly reduces the amplifier $1/f$ noise thanks to the double zero introduced by the AZ baseband power transfer function. This improvement is obtained at the cost of an increased white noise foldover component due to the aliasing of the amplifier's thermal and as well as $1/f$ noise. In most practical cases, this foldover term is dominated by the aliased thermal noise component, which is approximately equal to the amplifier's original broadband thermal noise multiplied by the ratio of the equivalent noise bandwidth to the Nyquist frequency.

C. Residual Offset

Next, the effectiveness of the stages of Fig. 1 in eliminating the effects of V_{os} will be discussed. Since the additional input used in the amplifiers of Fig. 1 for nulling the offset can either be a voltage or a current, it will generally be denoted as a control variable x_c. Changing this input when the amplifier is in the sampling phase, as shown in Fig. 1, allows the zeroing of the output voltage for a particular value of the control variable.

Let the input-referred offset V_{ios} be defined as the output voltage during the offset sampling phase divided by the differential gain of the amplifier in the amplification mode. The relation between this input-referred offset and the control variable is schematically plotted in Fig. 8, and is first assumed to be linear (see the continuous straight line in Fig. 8). Assume that the amplifier has an initial offset as shown in Fig. 8(a). The appropriate feedback configuration or the dedicated algorithm will have to bring this offset very close to zero. When the loop has settled or the algorithm is completed, the control information is stored. During the storage process, there might be some error Δx_c introduced into the control variable, due for example to charge injection by the sampling switch, or to the quantization error of the A/D converter, that leads to a residual offset $V_{\text{ios-lin}}$ or $V_{\text{ios-NL}}$ depending if the compensation characteristic is linear or not. It is important to notice that the characteristics

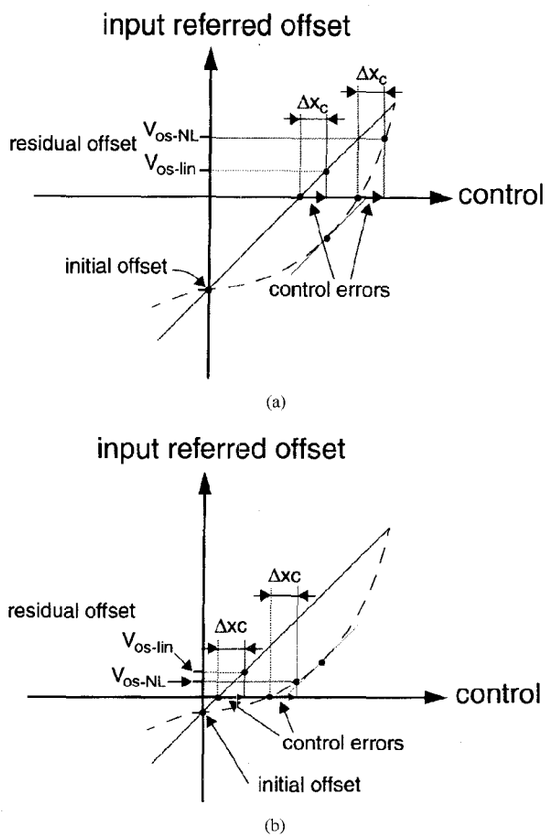


Fig. 8. Input-referred offset versus nulling control variable: (a) large initial offset and (b) small initial offset.

between the control variable and the input-referred offset voltage is not required to be linear. An example of a nonlinear characteristic is illustrated in broken lines in Fig. 8(a) and (b). Let ΔV be defined as the difference between the initial offset and the offset corresponding to the point where the incremental gain on the nonlinear characteristic equals the slope of the linear characteristic. The resulting residual offsets of the linear ($V_{\text{ios-lin}}$) and the nonlinear ($V_{\text{ios-NL}}$) characteristics resulting from equal control errors Δx_c are compared in Fig. 8(a) for an initial offset larger than ΔV. The residual error of the nonlinear characteristic is obviously larger. On the other hand, if the initial offset is already small compared to ΔV [Fig. 8(b)], the residual offset of the nonlinear characteristic becomes smaller. A nonlinear offset-nulling characteristic can thus potentially reduce the sensitivity to control errors and hence reduce the residual offset. But this only happens if the initial offset is already small. The choice between a linear or a nonlinear control characteristic depends on the anticipated initial offset reduction strategy and the test methodology.

D. Correlated Double Sampling

In the AZ principle described in Fig. 1, the amplifier has to be disconnected from the signal path during phase ϕ_1 in

ANALOG EXHIBIT 1002
Page 100 of 321

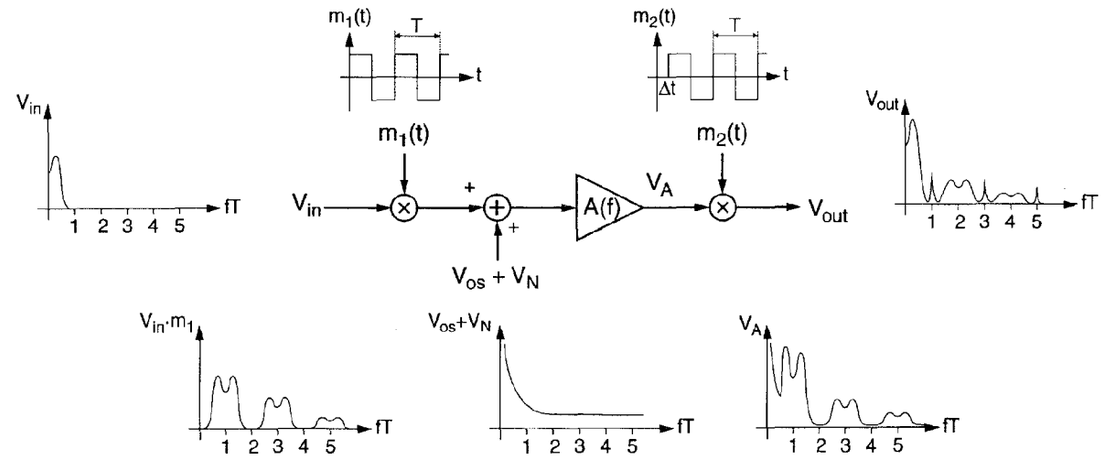


Fig. 9. The chopper amplification principle [19].

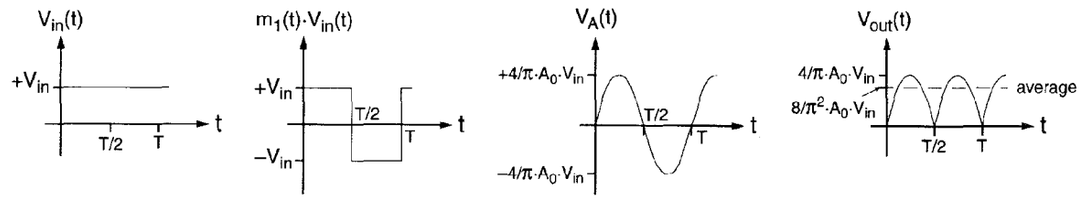


Fig. 10. Waveforms appearing along the chopper amplifier for a dc input and an amplifier bandwidth limited to twice the chopper frequency.

order to S/H its own offset and noise. It is therefore only available for amplification during phase ϕ_2. Although this may be incompatible with continuous-time applications, it is well suited to sampled-data systems such as SC circuits where all the signals are sampled at the end of a phase and held during the complementary time interval. The amplifier can then be autozeroed while the voltages are held and connected back for amplification when needed [20]. After the AZ phase, the output of the amplifier is then sampled again by the next stage (SC integrator or SC amplifier). There are thus two sampling operations: a first one to sample the amplifier noise and offset (AZ) followed by a second sampling of the signal and the instantaneous (or direct) noise of the amplifier in hold mode. Note that the AZ phase may require one additional phase [20].

The CDS technique which has originally been introduced to reduce the noise produced in charged-coupled devices (CCD's) [13], [14] can be described as an AZ operation followed by a S/H. It is widely used in sampled-data systems and particularly in SC circuits (see Section V).

Although the signal at the output of a circuit using CDS is now S/H, the effect of CDS on the amplifier offset and noise is very similar to that of the AZ process. The baseband transfer function $H_0(fT_s)$ still imposes a zero at the origin of frequency that cancels any offset and strongly reduces the $1/f$ noise in the same way the AZ technique does. On the other hand, although the transfer functions for $n \neq 0$ are different from those obtained for the AZ process, the foldover component due to aliasing is comparable since the wideband noise has already been sampled once.

III. The Chopper Stabilization Technique

In this section, an alternative technique for the suppression of the low-frequency noise, called (for historic reasons) chopper stabilization (CHS), will be introduced. Its properties will be analyzed and compared with those of the AZ and CDS schemes.

A. Basic Principle

The CHS technique was introduced about 50 years ago to realize high-precision dc gains with ac-coupled amplifiers. These were originally constructed using vacuum tubes and mechanical relay choppers. When solid-state components became available, they were then made with modular and hybrid techniques. Now they can easily be realized on-chip by taking advantage of integrated switches.

Unlike the AZ process, the CHS technique does not use sampling, but rather applies modulation to transpose the signal to a higher frequency where there is no $1/f$ noise, and then demodulates it back to the baseband after amplification. The chopper amplification principle is illustrated in Fig. 9.

Suppose that the input signal has a spectrum limited to half of the chopper frequency so no signal aliasing occurs, and that the amplifier is ideal, with no noise or offset. This

ANALOG EXHIBIT 1002
Page 101 of 321

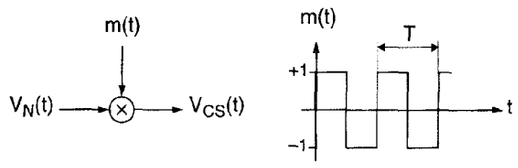


Fig. 11. Chopper modulation.

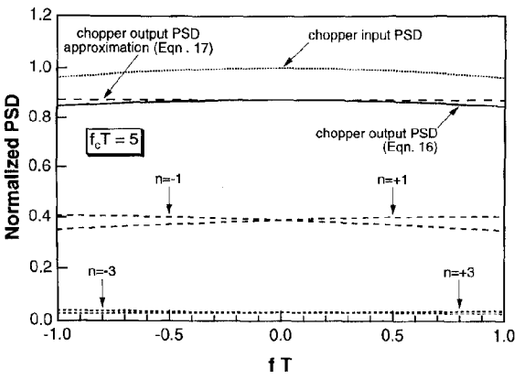


Fig. 12. Chopper output PSD for a first-order low-pass filtered white noise.

input signal is multiplied by the square-wave carrier signal $m_1(t)$ with period $T = 1/f_{\text{chop}}$. After this modulation, the signal is transposed to the odd harmonic frequencies of the modulation signal. It is then amplified and demodulated back to the original band. Assuming that the input of the chopper amplifier is a dc signal V_{in}, the signal at the output of the first chopper modulator is a square wave of period T and amplitude V_{in}. If the amplifier has a gain A_0, an infinite bandwidth and does not introduce any delay, the signal at its output is simply the same square wave with an amplitude $A_0 \cdot V_{in}$ and the signal after demodulation is again a dc signal of value $A_0 \cdot V_{in}$. To illustrate a less ideal solution, assume now that the amplifier has a constant gain A_0 up to twice the chopper frequency and is zero otherwise (ideal low-pass). As shown in Fig. 10, the amplifier output signal $V_A(t)$ is now a sinewave corresponding to the fundamental component of the chopped dc signal with an amplitude $(4/\pi)(A_0 \cdot V_{in})$. The output of the second modulator is then a rectified sinewave containing even-order harmonic frequencies components. The dc value after low-pass filtering is $(8/\pi^2)(A_0 \cdot V_{in})$, corresponding to an equivalent dc gain of $(8/\pi^2) \cdot A_0 \cong 0.8 \cdot A_0$. This example shows that the finite bandwidth of the amplifier introduces some spectral components around the even harmonics of the chopper frequency which have to be low-pass filtered to recover the amplified signal. The gain of the chopper amplifier is also sensitive to the delay introduced by the main amplifier. Assume again that the input is a dc signal V_{in} and that the amplifier has an infinite bandwidth but introduces a constant delay, say of a quarter of a period $T/4$. If the input and output modulators are in phase, the output signal is a chopped cosine wave, without a dc

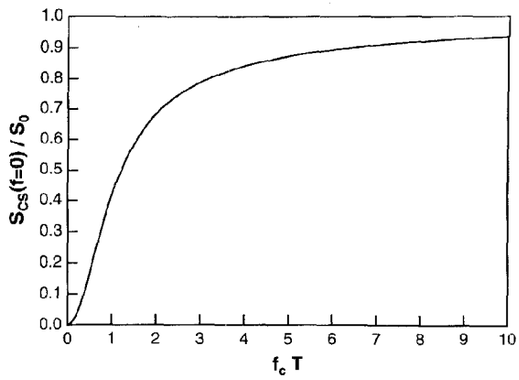


Fig. 13. Chopper modulated white noise at zero frequency as a function of the original white noise bandwidth.

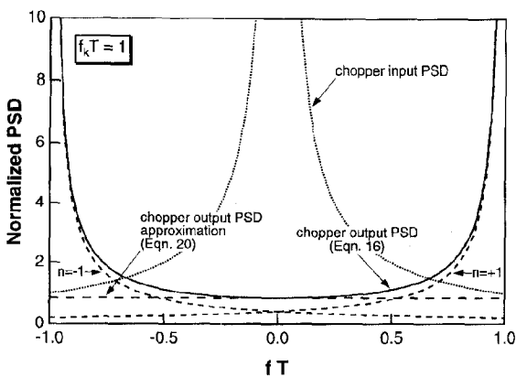


Fig. 14. Chopper output PSD for a $1/f$ noise.

component and containing only odd harmonics. This means that the dc gain of the overall chopper amplifier is zero. If the same constant delay is introduced between the input and the output modulators, the output signal is again a rectified sine wave. This shows that in order to maintain a maximum dc gain, the phase shift between the input and the output modulators has to match precisely the phase shift introduced by the amplifier.

Since the noise and offset are modulated only once, they are transposed to the odd harmonics of the output chopping square wave, leaving the amplifier ideally without any offset and low-frequency noise.

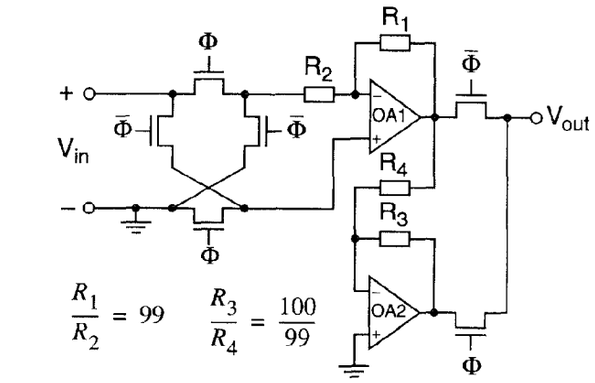
B. The Effect of Chopping on the Amplifier Noise

The effect of the chopper modulation on the amplifier noise can be analyzed from Fig. 11 where $V_N(t)$ is the noise and $m(t)$ the carrier signal.

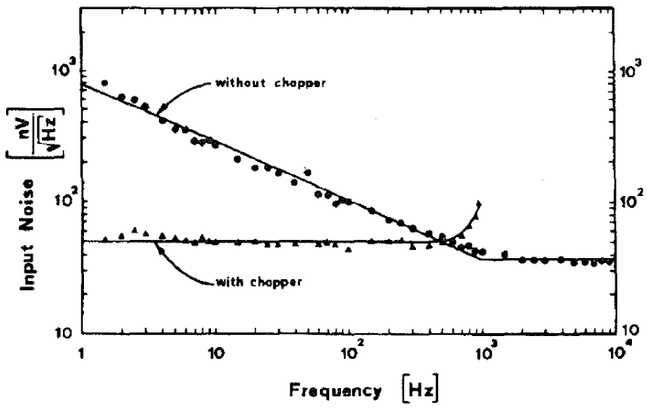
The bilateral PSD of the chopped output signal $V_{CS}(t)$ is given by

$$S_{CS}(f) = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n \text{ odd}}}^{+\infty} \frac{1}{n^2} S_N\left(f - \frac{n}{T}\right). \qquad (16)$$

ANALOG EXHIBIT 1002
Page 102 of 321



(a)



(b)

Fig. 15. Experimental chopper amplifier. (a) Experimental chopper amplifier schematic. The chopper frequency has been set to the amplifier corner frequency $f_{chop} = f_k = 1$ kHz. (OA1 and OA2 are, respectively, a CA3420 and μ A 741 and the switches are MC14016.) (b) Measured input referred PSD without and with the chopper.

The output PSD, resulting from the summation of the replicas of the original spectrum shifted to the odd harmonics of the chopper frequency, is plotted in Fig. 12 for $n = 1, -1, 3, -3$ and for an amplifier cut-off frequency f_c equal to five times the chopper frequency $1/T$. It can be approximated in the baseband ($|fT| \leq 0.5$) by a white noise PSD

$$S_{CS\text{-white}}(f) \cong S_{CS\text{-white}}(f = 0) = S_0 \left[1 - \frac{\tanh\left(\frac{\pi}{2} f_c T\right)}{\frac{\pi}{2} f_c T} \right] \quad (17)$$

which for $f_c T \gg 1$ which can further be approximated by

$$S_{CS\text{-white}}(f) \cong S_0 \quad \text{for} \quad |fT| \leq 0.5 \text{ and } f_c T \gg 1. \quad (18)$$

Unlike the AZ technique, the chopper modulation does not introduce aliasing of the broadband noise, which for AZ causes the PSD in the baseband to increase proportionally with the ratio of the noise bandwidth and the sampling frequency. As shown by (17), the baseband PSD resulting from the chopper modulation is nearly constant (white noise), and it tends to the value of the input white noise S_0 for a large $f_c T$. This is due to the fact that the noise is not sampled nor held, just periodically inverted without changing the general properties of the noise in the time domain. Although the chopper modulator output PSD results from a summation as for the S/H process, in the chopper modulation the replicas are multiplied by $1/n^2$, making their contribution to the baseband decrease very rapidly.

The PSD given in (17) is plotted in Fig. 13 against the white-noise bandwidth normalized to the chopper frequency. It shows that the chopper-modulated PSD is always smaller than the PSD of the original white noise, and tends asymptotically to it for very large cutoff to chopper frequency ratios. It becomes equal to 90% of the original spectrum for $f_c T$ slightly larger than six.

The effect of the chopper modulation on the $1/f$ noise can also be analyzed using (16), assuming a cutoff fre-

ANALOG EXHIBIT 1002
Page 103 of 321

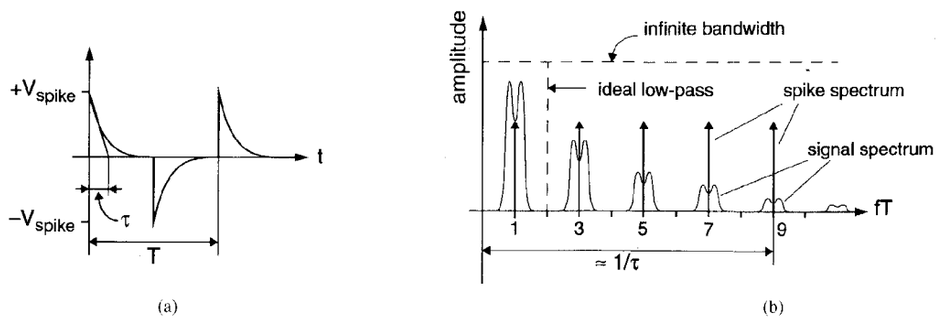


Fig. 16. Spike signal appearing at the input of the amplifier and causing residual offset. (a) Spike signal at the amplifier input and (b) spike signal and chopper modulated signal spectra with amplifier bandwidth characteristics.

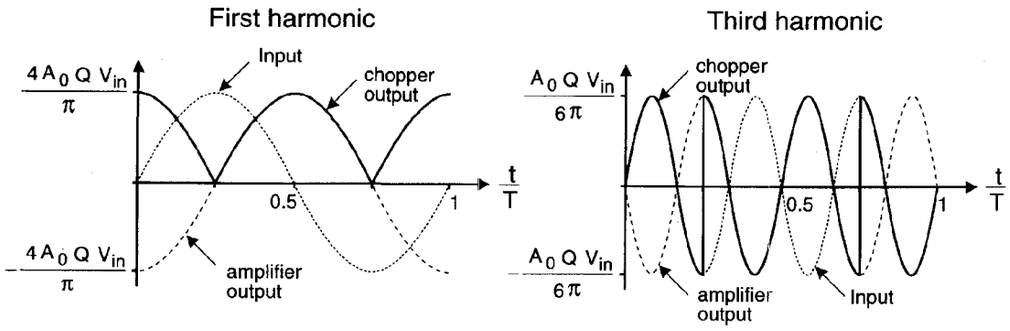


Fig. 17. Effect of the phase shift introduced by a second-order low-pass selective amplifier on the first and third harmonics.

quency much larger than the chopper frequency and an input PSD given by

$$S_{N-1/f}(f) = S_0 \frac{f_k}{|f|} = S_0 \frac{f_k T}{|fT|}. \tag{19}$$

The result of the summation is plotted in Fig. 14, which clearly shows that the $1/f$ noise pole has disappeared from the baseband since it has been transposed to $\pm 1/T$ and to the odd harmonics of the chopper frequency. It also shows that the chopped $1/f$ noise PSD can be approximated in the baseband by a white noise component

$$S_{CS\text{-}1/f}(f) \cong 0.8525 S_0 f_k T. \tag{20}$$

The total residual noise in the baseband for a typical amplifier input referred noise given by (6) can be obtained by adding (18) and (20), resulting in

$$S_{CS}(f) \cong S_0(1 + 0.8525 f_k T) \quad \text{for } |fT| \leq 0.5 \text{ and } f_c T \gg 1. \tag{21}$$

According to (21), a good compromise is obtained by choosing the chopper frequency equal to the amplifier corner frequency. The resulting white noise PSD increase is then less than 6 dB. Equation (21) has been verified experimentally on a breadboard circuit. The schematic is presented in Fig. 15(a), and the measured input referred noise PSD with and without the chopper is shown in Fig. 15(b). The chopper frequency was set equal to the amplifier corner frequency at $1/T = f_k = 1$ kHz. The white noise component of the amplifier without the chopper was estimated to be 37 nV/$\sqrt{\text{Hz}}$, and the theoretical white noise of the amplifier with the chopper active as calculated from (21) was 50.4 nV/$\sqrt{\text{Hz}}$ which is very close to the measured result shown in Fig. 15(b).

C. Residual Offset

Residual offset is mainly due to the nonidealities of the chopper modulators and more specifically of the input modulator. If the modulators are realized with simple MOS switches, these nonidealities will include clock feedthrough and charge injection (see Section IV-A for a discussion of these and other nonideal effects). More generally, any spikes caused by the modulator nonidealities and appearing at the amplifier input will be amplified and demodulated by the output modulator, giving rise to a residual dc component. Since only the odd harmonics of the chopper frequency will contribute to the residual offset, the positive and negative spikes will have an odd symmetry (Fig. 16).

Since the time constant τ of these parasitic spikes is generally much smaller than the half chopper period $T/2$, most of the spike energy appears at frequencies higher than the chopper frequency. The spectra of the signal resulting from such spikes and of a chopper-modulated signal at the amplifier input are shown in Fig. 16(b). Since the spectral envelope is inversely proportional to frequency, the output

ANALOG EXHIBIT 1002
Page 104 of 321

signal after amplification and demodulation is essentially reconstructed by the fundamental component. Using an amplifier with a bandwidth much larger than the chopper frequency results in a maximum gain approximately equal to the dc gain of the amplifier A_0, but also leads to a maximum output offset voltage, since almost all the spectral component of the spike signal will contribute. The input referred offset can be calculated assuming that $\tau \ll T/2$ [8], [12]:

$$V_{os} \cong \frac{2\tau}{T} V_{\text{spike}} \tag{22}$$

where V_{spike} is the amplitude of the spikes at the chopper amplifier input as shown in Fig. 16(a). Keeping the same gain A_0 in the passband, but limiting the bandwidth to twice the chopper frequency slightly lowers the overall dc gain to $(8/\pi_2)A_0 = 0.81A_0$, but greatly reduces the offset voltage referred to the input. The new value is

$$V_{os} \simeq \left(\frac{2\tau}{T}\right)^2 V_{\text{spike}} \tag{23}$$

which is much smaller than that given by (22), since τ has been assumed to be much smaller than $T/2$. Therefore, the offset can be reduced drastically, without losing too much signal gain, by limiting the amplifier bandwidth to twice the chopper frequency. It can be shown that (23) also holds for a second-order low-pass or band-pass selective amplifier with its resonance frequency locked to the chopper frequency. This is essentially due to the phase characteristic of the selective amplifier. As illustrated in Fig. 17, for a constant input signal V_{in} and a low-pass selective amplifier, the fundamental component is delayed by a quarter of a period while all the harmonics are delayed by half a period, making their mean values equal to zero after demodulation. Since the offset is not further reduced by using higher-order selective filtering characteristics, the second-order selective amplifier is the best trade-off between circuit complexity and residual offset. Note that the band-pass selective amplifier is the simplest since it does not require any delay between the input and output chopper signals.

IV. Practical Implementation Issues

A. Nonideal Effects in Switches

The S/H circuit as well as the chopper modulator are most often realized using MOS switches. The MOS switch nonidealities include a nonzero and nonlinear on-resistance. However, the most important factors affecting residual offset are the following:

- clock feedthrough;
- channel charge injection;
- sampled noise;
- leakage current.

Clock feedthrough and channel-charge injection will be considered first.

Each time a switch is turned off, the charges in its conducting channel are released and removed through the

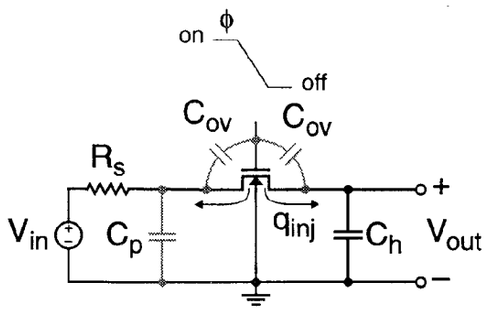


Fig. 18. Basic S/H circuit.

MOS source and drain terminals (the fraction of charges that flows to the substrate can generally be neglected). The partitioning of these charges between the source and drain depends mainly on the ratio of the total capacitance C_h at the switch drain (the hold capacitor) and at the source (C_p, corresponding to the total parasitic capacitance) and on the so called "switching parameter" [2] determined mainly by the transistor's "on" resistance R_{on} and the slope of the clock signal applied to the gate. The channel charge is split equally between source and drain only if either the capacitances C_p and C_h are equal (independent of the switching time), or if the switching transition time is much less than the $R_{on}C$ time constant (independent of C_p/C_h). In general, for slowly falling clock signals, the channel charge is divided unequally between source and drain, going mostly to the terminal showing the lower impedance. In the case where the source or drain capacitance is much larger than the other, most of the charge flows to the larger capacitance. The charge q_{inj} injected into the hold capacitor is thus difficult to predict accurately. There are, however, circuit techniques which can reduce the effect of charge injection. The simplest one uses complementary switches in such a way that the charges released by one switch are absorbed by the complementary device building its channel. This technique is rather inefficient, since the matching between the channel charges of the n-MOS and the p-MOS devices is poor and signal dependent. This charge mismatch is further degraded by phase jitter between the two complementary clocks. Other more efficient strategies include:

1) making capacitance C_p much larger than C_h (by adding an extra capacitor) and choosing a switching parameter much smaller than one (by choosing a slow clock transition) in order to attract most of the channel charge to C_p, reducing q_{inj} almost to zero [Fig. 19(a)]. This technique of course sets a limit on the maximum clock frequency. Furthermore, the charge flow due to the overlap capacitance C_{ov} is still present;
2) making C_p equal to C_h to force the channel charge to split equally between source and drain, and then compensating the injected charge by adding half-size dummy switches [Fig. 19(b)];

ANALOG EXHIBIT 1002
Page 105 of 321

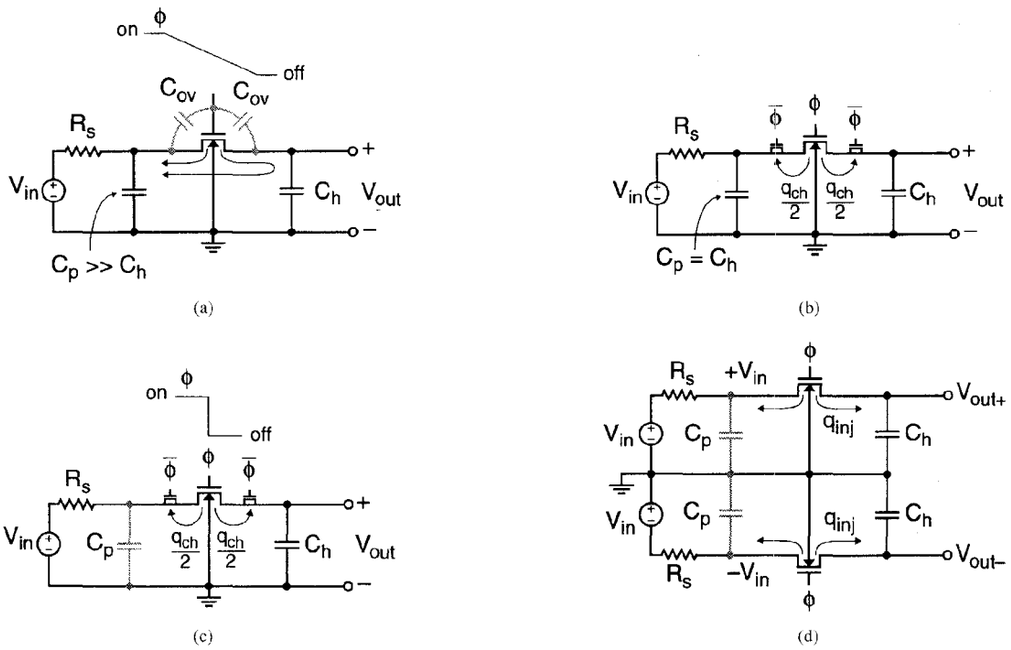


Fig. 19. First-order charge injection cancellation techniques: (a) large shunt capacitor and slow clock transition time, (b) symmetrical capacitances ($C_p = C_h$) with half-sized dummy switches, (c) short clock transition time with half-sized dummy switches, and (d) fully differential structure.

3) using a very short transition time to force the channel charge to split equally between source and drain and then compensating the injected charge by half-sized dummy switches [Fig. 19(c)];
4) using a fully differential structure. If the injected charges to the differential capacitors are matched, the resulting voltage appears as a common-mode voltage and is therefore rejected [Fig. 19(d)]. This usually requires the generation of delayed-cutoff clock phases.

It should be noted that none of the previous described techniques offers a perfect charge-injection cancellation. Furthermore, the efficiency of the half-sized dummy transistor technique depends on a proper layout in order to insure a good matching and a first-order insensitivity to doping gradient. The technique which usually offers the best results is a combination of a fully differential structure and the half-sized dummy transistor technique described in 3) and 4).

It is also important to notice that the simulation of the charge injection effect at the transistor level using a circuit simulator such as SPICE often does not yield accurate results. This is mainly due to the problem of inaccurate charge conservation inherent to such simulators, combined with an incorrect modeling of the MOS transistor's intrinsic charges and of the partitioning of the channel charge between source and drain [37]–[43]. A clear discussion of charge conservation in MOSFET models and SPICE is given in [43].

Each time the switch of Fig. 18 is opened, an additional error charge due to the thermal noise of the switch channel will be sampled on the hold capacitor C_h. The variance of this noise charge is equal to kTC_h [1], [2], corresponding to a sampled noise voltage variance equal to kT/C_h.

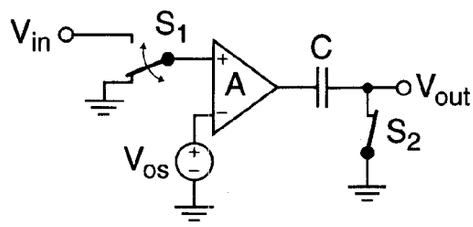


Fig. 20. Open-loop offset cancellation technique.

For very long hold time and/or for high-temperature operation [35], the leakage current I_{leak} associated with the drain-to-bulk junctions also has to be taken into account, since it will discharge the hold capacitor and thus introduce an additional error into the sampled voltage.

The total error ΔV in the sampled voltage across the hold capacitor due to clock feedthrough, charge injection, sampled noise and leakage current is given by

$$\Delta V = \alpha \frac{C_{ov}}{C_{ov} + C_h} V_{\text{swing}} + \frac{q_{inj}}{C_h} + \sqrt{\frac{kT}{C_h}} + \frac{I_{\text{leak}} T_h}{C_h} \tag{24}$$

where V_{swing} is the swing of the clock signal and I_{leak} the leakage current of the drain-to-bulk diodes at the operating temperature. The attenuation factor $\alpha < 1$ accounts for the part of the total charge $C_{ov}V_{\text{swing}}$ coming from the overlap capacitor and flowing to ground instead of the hold

ANALOG EXHIBIT 1002
Page 106 of 321

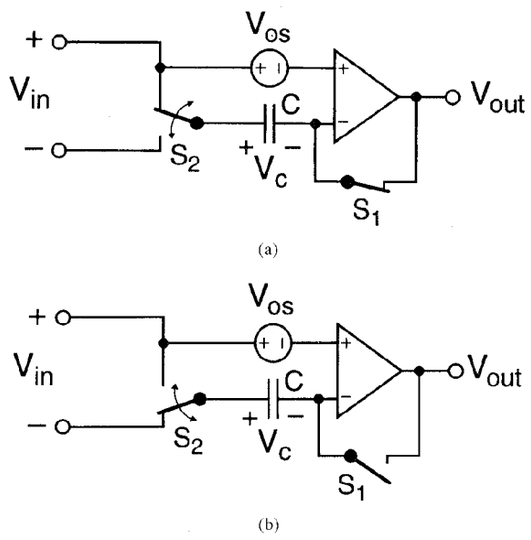


Fig. 21. Closed-loop-amplifier offset cancellation principle: (a) offset sampling phase (AZ) and (b) amplification phase.

capacitor. It is important to notice that all contributions appearing in (24) decrease if a larger hold capacitor is used. Since in most practical cases the second term of (24) dominates, the voltage change ΔV will be replaced by q_{inj}/C_h in the following discussions.

B. The Open-Loop Offset Cancellation Principle

The simplest way to implement offset cancellation is to sample the offset at the output of the amplifier as shown in Fig. 20. This technique is sometimes called output offset storage (OOS) [2], [6], [33]. During the AZ phase, the input switch S_1 and the output switch S_2 are both connected to ground. Switch S_2 is then opened and the offset voltage V_{os} multiplied by the amplifier gain A remains stored on capacitor C. This stored output voltage is altered by an error voltage q_{inj}/C caused by the charge injection occurring at the opening of switch S_2. After the AZ phase, the input terminal of the amplifier is connected back to the signal by switch S_1. The input-referred residual offset is thus limited by the charge injection q_{inj} (or charge injection mismatch Δq_{inj} in the case of a differential implementation)

$$V_{os\text{-}res} = \frac{1}{A}\frac{q_{inj}}{C}. \tag{25}$$

This technique is obviously effective only if the amplifier does not saturate during the offset-sampling phase. This requires that the output-referred offset remain smaller than the minimum saturation voltage. This is possible only if the amplifier gain is relatively small (typically, less than ten), or if C and S_2 follow the first stage of the amplifier.

C. The Closed-Loop Offset Cancellation Principle

The open-loop offset cancellation principle is not well suited to high-gain amplifiers. It is usually preferable there

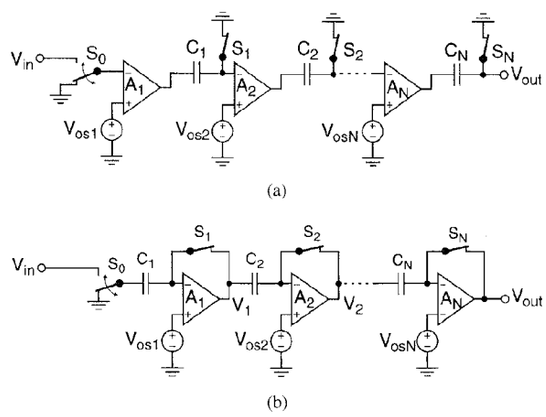


Fig. 22. Multistage offset cancellation principles.

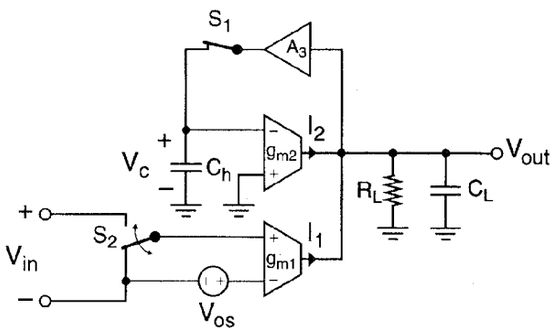


Fig. 23. Offset compensation using an additional offset nulling input.

to sense the amplifier's offset in a closed-loop configuration as shown in Fig. 21.

During the sampling phase, the amplifier is disconnected from the signal path and connected in a unity-gain configuration as shown in Fig. 21(a). Assuming that the open-loop gain A of the amplifier is much larger than one, the voltage V_c obtained across the storage capacitor C after the amplifier has settled is almost equal to its offset voltage V_{os}

$$V_c = \frac{A}{1+A} V_{os} \cong V_{os}. \tag{26}$$

This voltage (plus an additional error q_{inj}/C caused by the charge injection occurring when switch S_1 opens) is stored across capacitor C. The charge will remain trapped on capacitor C since the input current of the amplifier is zero for a MOS input stage, and hence capacitor C behaves like a floating voltage source equal to V_{os} plus the charge-injection error. After this sampling phase, the offset-compensated stage is available for amplification and is connected again to the signal path. The residual offset can then be found

$$\begin{aligned} V_{os\text{-}res} &= V_{os} - V_c \\ &\cong \frac{V_{os}}{A} + \frac{q_{inj}}{C}. \end{aligned} \tag{27}$$

ANALOG EXHIBIT 1002
Page 107 of 321

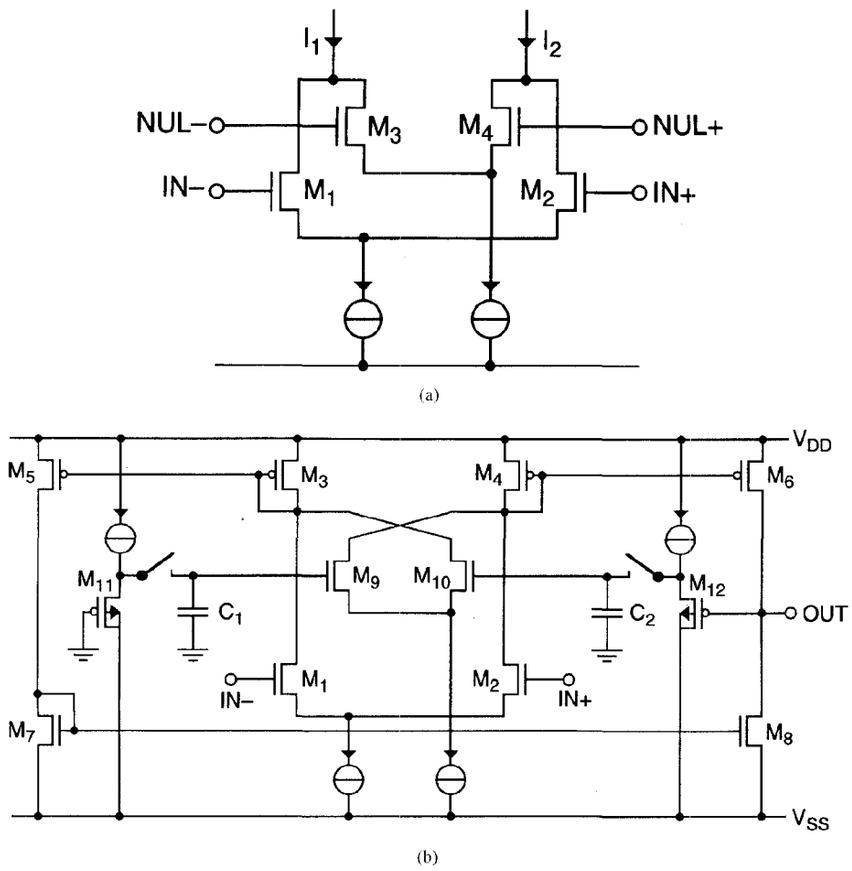


Fig. 24. Realization of the nulling input port using an additional differential pair connected in parallel with the main pair: (a) principle and (b) complete AZ scheme.

It is thus nearly equal to the original offset divided by the amplifier dc gain, and is ultimately limited by the charge-injection term q_{inj}/C. The latter could be reduced to a mismatch error of charge injections if a fully differential configuration is used.

The amplifier is in general connected in a closed-loop configuration for amplification, and in an open-loop configuration when it is used as a comparator.

In the scheme described above, the amplifier is not available to the external circuitry during the offset sampling phase. This is not a major drawback for most applications. In case continuous-time amplification is required, the offset-free amplifier can be duplicated and used in a time-shared ("ping-pong") operation [25], [26], or the continuous-time feedforward technique discussed below in Section IV-F may be used [22], [35], [36].

D. Multistage Offset Storage

If high gain and speed is required, several single-stage amplifiers can be cascaded as shown in Fig. 22 [33], [50]. The circuit of Fig. 22(a) operates as follows. In the offset sampling phase (shown in Fig. 22), the negative inputs of all the amplifiers are connected to ground. Switch S_1 is then opened first, causing some charge to be injected into capacitor C_1, which results in an error voltage appearing at the negative input of the second amplifier. This error voltage can be viewed as a change in the input-referred offset voltage of the second amplifier and will thus be cancelled along with V_{os2}. Subsequently, switches S_2, S_3, $\cdots$, S_N are opened successively, so that the only offset voltage affecting the output is due to the charge injection of switch S_N into capacitor C_N. Since the total gain is equal to the product of the individual gains, the equivalent input-referred offset is

$$V_{os\text{-}res} = \frac{1}{A_1 A_2 \cdots A_N} \cdot \frac{q_{inj-N}}{C_N} \tag{28}$$

which is obviously much lower than that obtained for a single-stage low-gain amplifier.

The circuit of Fig. 22(b) operates in a similar way. When switch S_1 opens, charge is injected onto capacitor C_1 resulting in an output voltage V_1 for the first amplifier equal to $V_{os1} + A_1 q_{inj1}/C_1$ for $A_1 \gg 1$. When switch S_2 opens, the sum of V_1, the offset voltage of the second amplifier V_{os2} and the charge injection voltage q_{inj2}/C_2 of switch S_2 is stored on capacitor C_2. The output voltage

ANALOG EXHIBIT 1002
Page 108 of 321

of the second amplifier when both switches S_1 and S_2 are opened sequentially is thus independent of the voltage V_1 and is simply equal to for $V_{os2} + A_2 q_{inj2}/C_2$ for $A_2 \gg 1$. This means that neither the offset nor the charge-injection errors propagate along the amplifier chain. The output offset is therefore affected only by the last stage, and equals $V_{osN} + A_N q_{injN}/C_N$. Hence, the equivalent input-referred offset is given by

$$V_{os\text{-}res} \cong \frac{V_{osN} + A_N \cdot \dfrac{q_{injN}}{C_N}}{A_1 A_2 \cdots A_N} \tag{29}$$

which is again much lower than the offset obtained for a single-stage low-gain amplifier.

High-gain and high-precision amplifiers or comparators can thus be realized simply by cascading low-gain stages and performing an input or output offset cancellation. If the switches are opened sequentially, the output offset is only determined by the last stage. The equivalent input-referred offset can thus be made extremely small. It should be noticed that this is true only if the delay between the edges of the clock pulses controlling switches S_1 to S_N is long enough to allow complete offset storage on the capacitors [6]. Note also that using a cascade of low-gain stages in a feedback amplifier may lead to stability problems.

E. Closed-Loop Offset Compensation Using an Auxiliary Input Port

The charge injection term appearing in (27) can be drastically reduced by storing the offset voltage at some intermediate node instead of at the amplifier input. The basic principle is that the gain A_1 from the signal input to the output is now higher than the gain A_2 from the nulling input to the output. The voltage change at the nulling input due to charge injection is therefore divided by the ratio A_1/A_2 which can be set much larger than one. The compensation is often realized using transconductance stages as shown in Fig. 23. Amplifier A_3 has been added to avoid loading the main amplifier with the hold capacitor C_h and therefore slowing down the AZ process. This allows the reduction of the effects of charge injected by switch S_1 and of the kT/C_h sampled noise by using a large hold capacitor C_h. It can also increase the compensation loop gain and therefore reduce the residual offset, as will be shown hereafter. In the case a compensation loop gain $g_{m2}R_L$ is sufficient, amplifier A_3 can be a simple voltage follower.

Assume that the input terminals of the main amplifier are short-circuited and that the compensation loop is still inactive (switch S_1 is open). The output voltage is zeroed if the current $I_2 = -g_{m2}V_c$ is equal to the current $-I_1 = g_{m1}V_{os}$, i.e., if the control voltage V_c is equal to $-(g_{m1}/g_{m2})V_{os}$. The ratio g_{m1}/g_{m2} should be chosen such that the control voltage V_c is much larger than the offset at the input of g_{m2} introduced by the nonidealities of the compensation loop containing transconductor g_{m2} and amplifier A_3. On the other hand, the maximum value $V_{c\text{-max}}$ of the control voltage before transconductor g_{m2} saturates should be

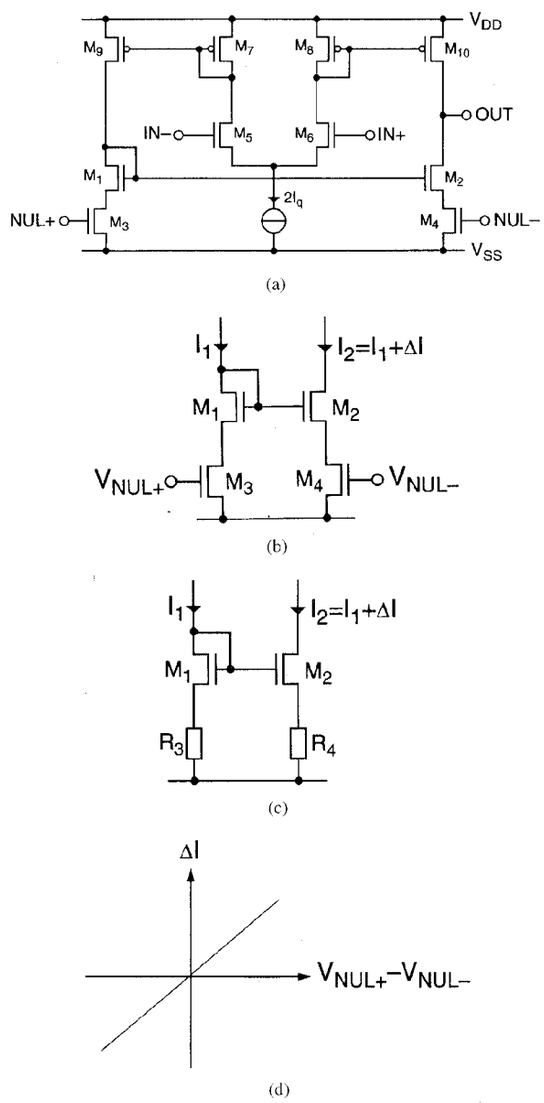


Fig. 25. Realization of the nulling input port using a degenerated current mirror: (a) principle, (b) adjustable current mirror, (c) equivalent schematic of (b), and (d) nulling current transfer characteristic.

chosen such that the maximum input offset voltage $V_{os\text{-max}}$ can still be compensated. This sets the maximum value for the ratio g_{m1}/g_{m2} equal to $|V_{c\text{-max}}/V_{os\text{-max}}|$.

The control voltage V_c is developed during the AZ phase by sensing the output voltage in a closed-loop configuration (with switch S_1 closed). Defining $A_1 \equiv g_{m1}R_L$, the resulting output voltage is then equal to the initial offset $-A_1 V_{os}$ at the output divided by the compensation loop gain (which is assumed to be much larger than one). The corresponding input-referred residual offset is given by

$$V_{os\text{-}res} \cong -\frac{V_{os}}{A_2 A_3} \tag{30}$$

ANALOG EXHIBIT 1002
Page 109 of 321

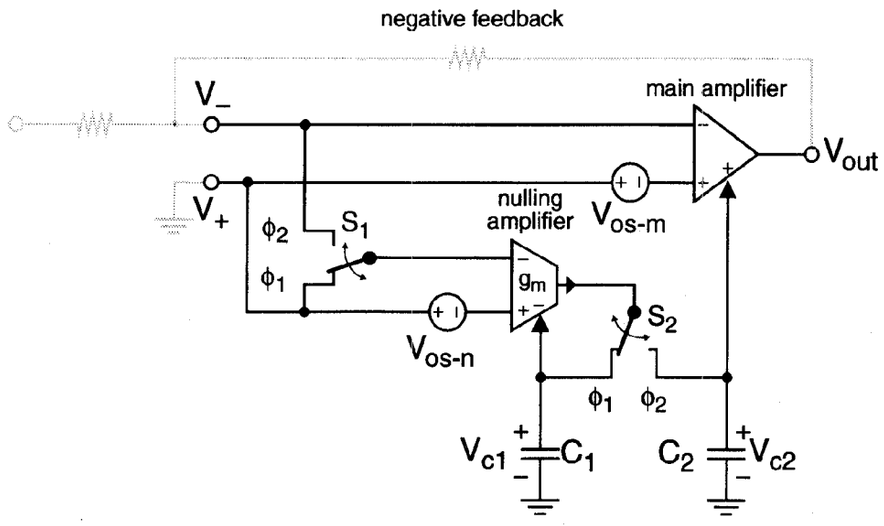


Fig. 26. Continuous-time AZ amplifier using feedforward technique.

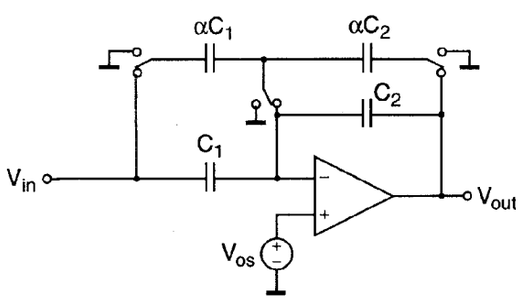


Fig. 27. Uncompensated SC voltage amplifier.

where $A_2 \equiv g_{m2}R_L$. The residual input-referred offset can thus be made small by choosing the loop gain A_2A_3 sufficiently large. Equation (30) ignores the charge injection occurring at the end of the AZ phase when switch S_1 opens. The input-referred residual offset voltage including charge injection of switch S_1 is given by

$$V_{os\text{-}res} \cong -\frac{V_{os}}{A_2A_3} - \frac{A_2}{A_1}\frac{q_{inj}}{C_h} = -\frac{V_{os}}{A_2A_3} - \frac{g_{m2}}{g_{m1}}\frac{q_{inj}}{C_h}. \tag{31}$$

As already mentioned, the first term of (31) can be made small by choosing a sufficiently large loop gain A_2A_3, whereas the effect of charge injection is essentially determined by the ratio of the transconductances g_{m2}/g_{m1}. Assuming that the first term of (31) can be made negligible, the minimum value of ratio g_{m1}/g_{m2} should then be chosen such that the current at the output of transconductor g_{m2} due to charge injection remains smaller than the output current of transconductor g_{m1} produced by the maximum tolerated residual offset voltage:

$$g_{m2}\frac{q_{inj}}{C_h} < g_{m1}V_{os\text{-}res\text{-}\max}. \tag{32}$$

The ratio g_{m1}/g_{m2} is thus limited by a lower bound set by the ratio of the voltage due to charge injection on C_h to the maximum acceptable residual offset. Its upper bound is determined by the ratio of the maximum admissible control voltage before the g_{m2} transconductor reaches saturation to the maximum initial offset to be compensated. Therefore, it must satisfy

$$\frac{\frac{q_{inj}}{C_h}}{V_{os\text{-}res\text{-}\max}} < \frac{g_{m1}}{g_{m2}} < \frac{V_{c\text{-}\max}}{V_{os\text{-}\max}}. \tag{33}$$

The minimum value of A_2A_3 should be such that the maximum residual offset due to finite gain remains smaller than the charge injection contribution:

$$\frac{V_{os\text{-}\max}}{A_2A_3} < \frac{A_2}{A_1}\frac{q_{inj}}{C_h} \tag{34}$$

leading to a condition on the gain A_2:

$$A_2 > \sqrt{\frac{A_1V_{os\text{-}\max}}{A_3\frac{q_{inj}}{C_h}}}. \tag{35}$$

There are several ways of realizing the additional nulling input port. Fig. 24(a) a shows a possible implementation where an additional differential pair M_3–M_4 (corresponding to transconductor g_{m2} in Fig. 23) is connected in parallel with the main input pair M_1–M_2 (corresponding to transconductor g_{m1} in Fig. 23) [1], [2], [4], [24]. Connecting both main inputs together to the common-mode voltage (to ground), the offset voltage of the main differential pair M_1–M_2 will produce a difference in the drain currents of M_1 and M_2. This offset current can then be cancelled by imposing the apropriate differential voltage on the nulling input, making the currents I_1 and I_2 equal. The complete AZ schematic is shown in Fig. 24(b), where two source followers M_{11}–M_{12}, two sampling switches and two hold

ANALOG EXHIBIT 1002
Page 110 of 321

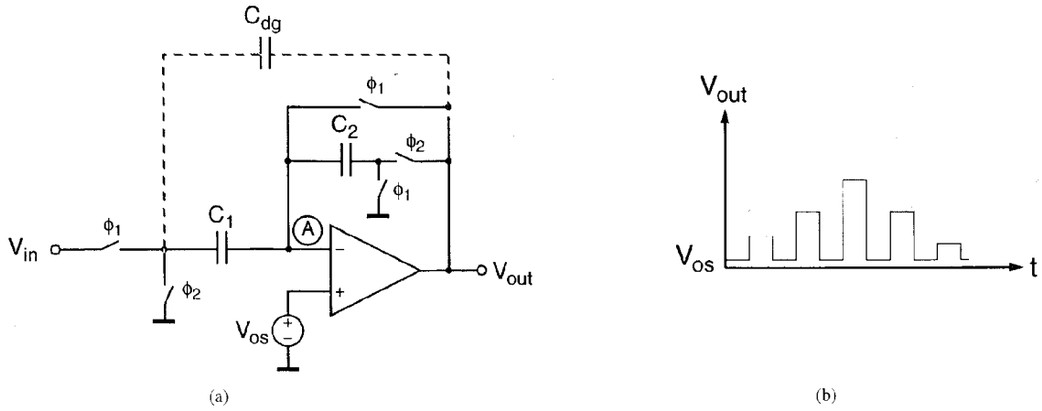


Fig. 28. Offset-compensated SC amplifier: (a) schematic and (b) output signal.

capacitors C_1, C_2 have been added to perform the AZ operation [1], [2].

Another way of realizing the nulling input port is presented in Fig. 25. The adjustable current mirror M_1–M_2 is degenerated by two transistors M_3–M_4 operating in their linear regions and behaving as two resistors R_3 and R_4 controlled by voltages V_{NUL+} and V_{NUL-}, respectively [Fig. 25(b) and (c)]. Setting V_{NUL+} higher than V_{NUL-} implies that resistance R_4 becomes smaller than R_3. For a given input current I_1, the source voltage of M_2 is then smaller than that of M_1 resulting in an increase ΔI of the drain current of M_2 with respect to I_1. The current increase ΔI is almost a linear function of the differential nulling voltage V_{NUL+} and V_{NUL} as shown in Fig. 25(d). This simple scheme has been used in several applications [1]–[4], and [26]. Residual offset voltages as small as 200 μV at a 3 V supply voltage have been reported [4].

F. Continuous-Time AZ Amplifiers

Some applications require continuous-time amplification and therefore the amplifier cannot be disconnected from the signal path in order to perform the AZ. This problem can be circumvented by duplicating the autozeroed amplifier and using one amplifier in its amplification mode while the other is being autozeroed. This time-sharing ("ping-pong") technique has been successfully used and described in [25], [26]. Nevertheless, switching the two amplifiers can result in spikes appearing at the output. This can be avoided by using another technique originally presented in [22] and recently used [35]. This scheme also uses two amplifiers as shown in Fig. 26: a main amplifier which is never disconnected from the signal path and an autozeroed amplifier (nulling amplifier) controlling the nulling input of the main amplifier. The basic idea behind this circuit is to use a low-offset amplifier to sense the main amplifier's offset and generate a correction voltage that is applied to the nulling input of the main amplifier to cancel its own offset. The nulling amplifier is autozeroed during phase ϕ_1 and its nulling voltage V_{c1} is stored on capacitor C_1 at the end of phase ϕ_1 and held during phase ϕ_2. The

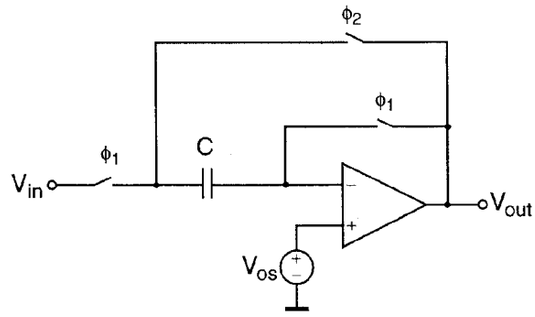


Fig. 29. A SC S/H stage.

nulling amplifier can therefore be considered as an almost offset-free amplifier that senses and zeroes the offset of the main amplifier during phase ϕ_2. The main amplifier nulling information V_{c2} is then sampled and held on capacitor C_2 during phase ϕ_1, while the nulling amplifier is zeroing its own offset. As shown in Fig. 26, this principle can only work if the overall amplifier is used with negative feedback in such a way that the voltage V_+–V_- appearing between the positive and negative input terminals is almost equal to the main amplifier offset $V_{os\text{-}m}$. This principle has been used in the commercially available op-amp ICL7650S [36] (which has been misnamed Super Chopper-Stabilized Operational Amplifier although it does not use CHS but rather AZ). This op-amp features a typical offset as low as $\pm 0.7\,\mu$V at room temperature [36]. Note that C_1 and C_2 are very large (typically 100 nF) off-chip capacitors in this application.

We shall next discuss the operation of the circuit in detail. During phase ϕ_1, corresponding to the state represented in Fig. 26, the nulling amplifier is disconnected from the signal path and is autozeroed. Its autocorrection voltage is then sampled on capacitor C_1 resulting in a control voltage V_{c1} across C_1 that is given by

$$V_{c1} = -\frac{A_n}{1+A_n'} V_{os\text{-}n} + \Delta V_{c1} \cong -\alpha_n V_{os\text{-}n} + \Delta V_{c1} \quad (36)$$

ANALOG EXHIBIT 1002
Page 111 of 321

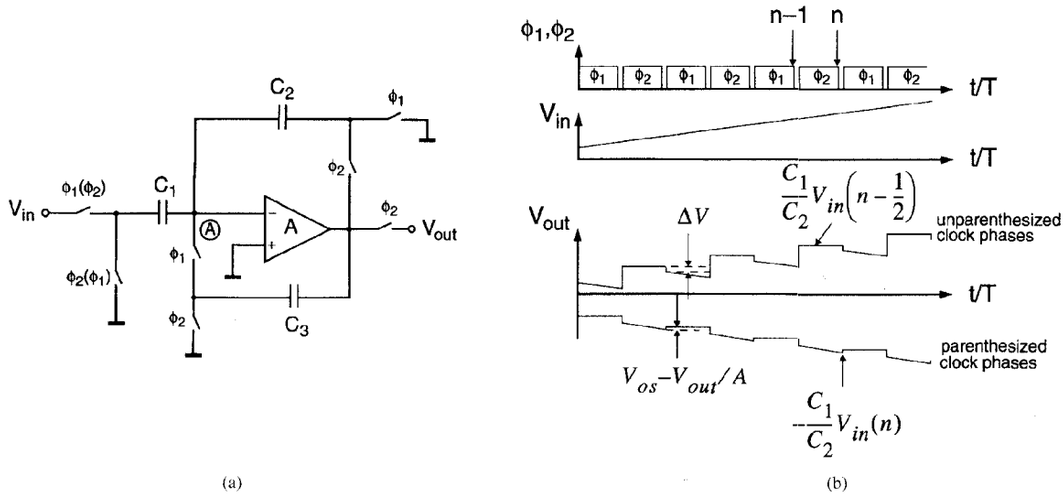


Fig. 30. Offset- and finite-gain compensated SC amplifier: (a) an offset and finite-gain compensated SC amplifier and (b) clock and signal waveforms.

where A_n is the gain of the nulling amplifier from its signal input, A_n' is its gain from the nulling input, and $\alpha_n = A_n/A_n'$. Voltage ΔV_{c1} corresponds to the voltage change due to charge injection, sampled noise, and leakage current. It is given by (24), where C_h is replaced by C_1.

In the next phase ϕ_2, the inverting input of the nulling amplifier is connected back to the signal and its output is switched to the nulling input of the main amplifier. The output voltage of the main amplifier is given by

$$V_{\text{out}} = A_m(V_+ - V_- - V_{os\text{-}m}) + A_m' V_{c2} \tag{37}$$

where A_m is the gain of the main amplifier from its signal input and $A_m' = A_m/\alpha_m$ is the gain from the nulling input. V_{c2} is the correction voltage applied to the nulling input which during phase ϕ_2 is given by

$$\begin{aligned} V_{c2} &= A_n(V_+ - V_- - V_{os\text{-}n}) - A_n' V_{c1} \\ &\cong A_n(V_+ - V_-) - \alpha_n V_{os\text{-}n} - A_n' \Delta V_{c1} \end{aligned} \tag{38}$$

where it has been assumed that $A_n' \gg 1$. By definition of the residual offset voltage $V_{os(2)}$, imposing $V_+ - V_- = -V_{os(2)}$ during phase ϕ_2 will bring the output voltage to zero. Hence, the offset voltage $V_{os(2)}$ of the main amplifier during phase ϕ_2 is obtained by introducing the expression of V_{c2} given by (38) into (37), setting the output voltage to zero and solving for $V_+ - V_- = V_{os(2)}$ which results in

$$V_{os(2)} \cong \frac{\alpha_m V_{os\text{-}m} + \alpha_n V_{os\text{-}n}}{A_n} + \frac{\Delta V_{c1}}{\alpha_n}. \tag{39}$$

Here it was assumed that the gain $A_n A_m'$ from the input $(V_+ - V_-)$ through the nulling amplifier to the output (V_{out}) is much larger than the gain A_m of the main amplifier alone. When switch S_2 opens at the end of phase ϕ_2, the output voltage will change by an amount $\Delta V_{\text{out}} = A_m' \Delta V_{c2}$, where the control voltage change ΔV_{c2} is due to charge injection, sampled noise and leakage current on capacitor C_2, and is given by (24) with C_h replaced by C_2. The

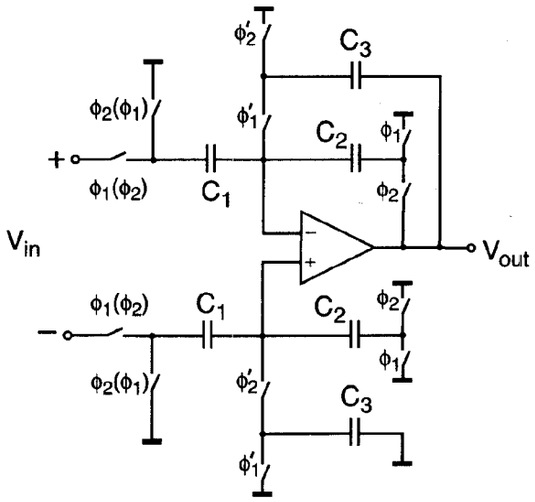


Fig. 31. An implementation of the scheme of Fig. 30. The primed clock phases cut off earlier than the unprimed ones.

initial input voltage equal to $V_{os(2)}$ should thus be reduced by an amount $\Delta V_{\text{out}}/A_m = \Delta V_{c2}/\alpha_m$ in order to bring the output voltage back to zero again. The resulting residual input-referred offset voltage $V_{os(1)}$ valid for phase ϕ_1 is therefore slightly different than for phase ϕ_2 due to charge injection onto C_2 and is given by

$$\begin{aligned} V_{os(1)} &= V_{os(2)} - \frac{\Delta V_{c2}}{\alpha_m} \\ &\cong \frac{\alpha_m V_{os\text{-}m} + \alpha_n V_{os\text{-}n}}{A_n} + \frac{\Delta V_{c1}}{\alpha_n} - \frac{\Delta V_{c2}}{\alpha_m}. \end{aligned} \tag{40}$$

In the case the gains of the main and nulling amplifiers from their signal inputs are equal to their gains from their nulling inputs (corresponding to $\alpha_n = \alpha_m = 1$, (39) and (40) show that the residual offset is basically equal to the

ANALOG EXHIBIT 1002
Page 112 of 321

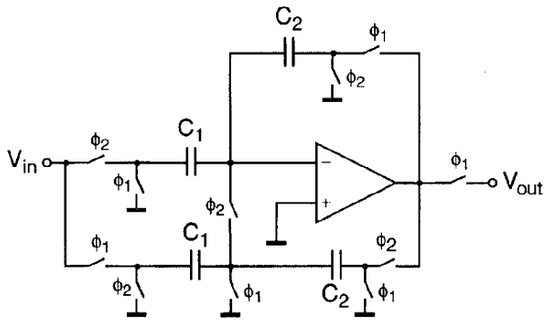


Fig. 32. A wideband compensated SC amplifier.

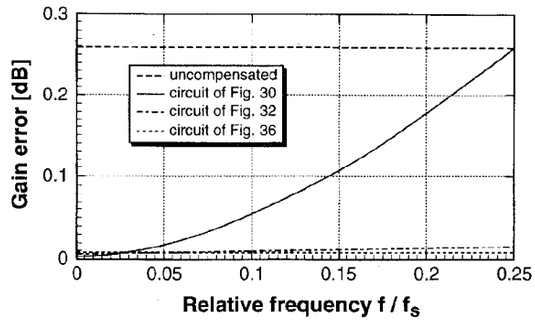


Fig. 33. Gain error versus frequency curves for compensated SC amplifier.

sum of the main and nulling amplifiers offsets, divided by the gain of the nulling amplifier A_n, plus the charge injection terms. The latter contribution can be reduced by decreasing the gains from the nulling input relative to the gains from the main inputs for both amplifiers. (This corresponds to setting both α_n and α_m larger than one.) The design criteria are very similar to those discussed in Section IV-E for the AZ scheme using an auxiliary input port.

As was suggested in [35], the injection terms contained in ΔV_{c1} and ΔV_{c2} can be reduced to a mismatch of injection by using a differential nulling input as shown in Fig. 24(a) or Fig. 25(a).

It should be noticed that during phase ϕ_2 the autozeroed amplifier has two forward signal paths: one directly through the main amplifier and the other through the nulling amplifier and the nulling input of the main amplifier. The dc gain is therefore equal to $A_m + A_n A_m^{'}$, but generally reduces to $A_n A_m^{'}$ corresponding to the gain from the input through the nulling amplifier and the main amplifier's nulling input.

The frequency responses of the main and nulling amplifiers must be designed so as to ensure that the autozeroed amplifier is stable during both phases. Stability during phase ϕ_1 requires that the main amplifier's primary input signal path and the nulling amplifier's auxiliary input signal path be unity-gain stable. The stability conditions during phase ϕ_2 depend on how the auxiliary inputs are realized. A detailed discussion of the stability of a particular implementation can be found in [35].

It should be noticed that since voltages V_{c1} and V_{c2} are generally not equal, a transient spike may appear at the amplifier output at the beginning of phase ϕ_2 when switch S_2 is connected to capacitor C_2. Assuming that no signal is present at the amplifier input, the instantaneous value of the amplifier output voltage during ϕ_2 after the transient has vanished might be slighly negative in order to compensate for a positive spike and maintain a zero mean value. Another potential problem is caused by signals that are near or equal to an integer multiple of the clock frequency and that appear at the virtual ground of the amplifier. Such signals are sampled on C_2 at the end of phase ϕ_2 and may be aliased down to dc [35]. This will result in an apparent offset which is different than the real main amplifier offset voltage $V_{os\text{-}m}$ which is to be compensated. To circumvent this problem, the voltage V_{c2} should be proportional to the mean value of the voltage at the virtual ground node. This can be achieved by low-pass filtering the signal when sensing the main amplifier input voltage during phase ϕ_2. A way to implement this low-pass filter is to use an operational transconductance amplifier (OTA) instead of an op-amp for the nulling amplifier [35] as shown in Fig. 26. The OTA is loaded by capacitor C_2 which is generally an external capacitor and can therefore be chosen rather large, setting the cut-off frequency at a very low frequency. The linear range of the OTA should be chosen sufficiently large in order to avoid any saturation due the sum of the dc offset to be compensated and the parasitic signal to be filtered.

V. Precision Building Blocks Using the Correlated Double Sampling Technique

This section presents some examples of basic building blocks such as S/H stages, voltage amplifiers, integrators, and filters, that use the CDS technique to reduce the amplifier's offset and noise as well as to lower the effect of the finite amplifier gain.

A. SC S/H and Voltage Amplifiers

The CDS technique described earlier in Section IV-C for AZ comparators can readily be applied to SC voltage amplifiers. Fig. 27 illustrates a conventional SC amplifier [50]. The nominal output is $V_{out} = -(C_1/C_2)V_{in}$, but finite op-amp gain changes the ideal voltage gain to

$$\hat{A}_v = \frac{A_v}{1 + \dfrac{1 + A_v}{A}} \tag{41}$$

where $A_v = -C_1/C_2$ is the ideal gain, and A is the dc gain of the op-amp. Thus for typical values of A and A_v, a gain error of 1% or more may occur. In some high-precision applications, e.g., if the amplifier is part of a DAC or ADC, this may be unacceptable.

Also, a nonzero input-referred dc op-amp offset V_{os} will introduce an output offset voltage $V_{os\text{-}out} = (1 + |A_v|)V_{os}$. Since V_{os} is typically 1–10 mV, and $|A_v|$ can have a value

ANALOG EXHIBIT 1002
Page 113 of 321

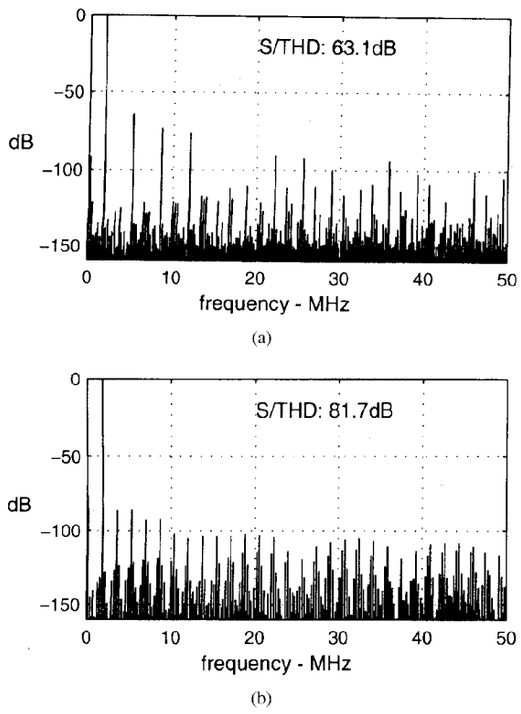


Fig. 34. Output spectra of SC amplifiers using nonlinear op-amps. The op-amp offset assumed was 5 mV, and the SC amplifier voltage gain was −2: (a) offset-compensated SC amplifier (Fig. 28) and (b) wideband compensated SC amplifier (Fig. 32).

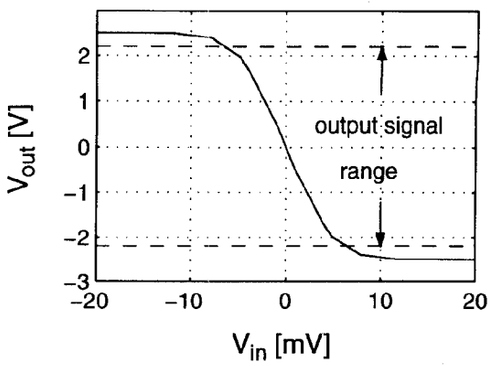


Fig. 35. The nonlinear op-amp transfer characteristics.

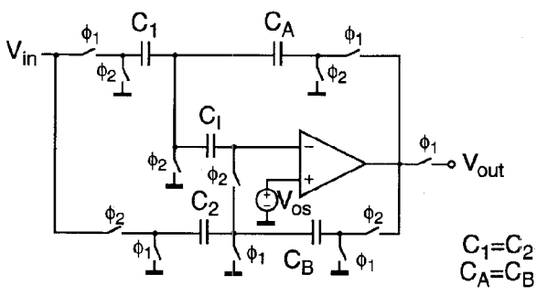


Fig. 36. SC amplifier with offset storage capacitor.

of 10 or more, the output offset may become a significant limitation on the permissible signal swing, especially in a low-voltage technology. It also may introduce ADC or DAC offset which needs to be calibrated.

If only the offset needs to be eliminated, the simple amplifier stage introduced by Gregorian [51] may be used [Fig. 28(a)]. Here, during the $\phi_1 = 1$ period, C_1 charges to V_{in}–V_{os}, and C_2 to V_{os}. V_{out} is developed during the $\phi_2 = 1$ interval. In this circuit, capacitors C_1 and C_2 are always connected to the virtual ground node Ⓐ, so if the input-referred offset voltage is constant, then when the switches driven by ϕ_2 close, the total charge entering node A is $C_1V_{in} + C_2V_{out} = 0$, which leads to the desired relation between V_{in} and V_{out} independent of V_{os}. However, as Fig. 28(b) illustrates, during the $\phi_1 = 1$ intervals the output is pulled to V_{os}, and the op-amp must have a high slew rate and fast settling time to enable V_{out} to slew back and forth at each clock transition. Also, the closed-loop gain of the stage is still affected by the dc gain of the op-amp the same way as in the circuit of Fig. 27.

Note that the small "deglitching" capacitor C_{dg} does not play a role in the signal charge redistribution. Its sole purpose is to prevent glitches in the op-amp output by providing negative feedback during the brief intervals when the nonoverlapping clock phases are both low, and the feedback path of the op-amp is otherwise open-circuited [52].

A unity-gain buffer stage, which can be used as a simple S/H circuit, or as an analog memory, or as an analog delay stage, and which also utilizes CDS to reduce dc offset effects, is shown in Fig. 29 [53]. Here, C charges to $V_{in}-V_{os}$ during $\phi_1 = 1$ period, and is connected as a feedback branch during $\phi_2 = 1$, causing $V_{out}(n) = V_{in}(n-1/2)$. As in the previous circuit, the op-amp output voltage is reset to V_{os} in every clock period, and hence the slew-rate and settling-time requirements are difficult to meet for high clock rates. Also, the op-amp gain affects V_{out}. Note that the operation of this circuit does not depend on the exact value of its single capacitor.

An SC amplifier which does not require a resetting of the output in each clock period and also reduces the effect of the op-amp gain, and hence allows more relaxed op-amp specifications for low-frequency inputs, is shown in Fig. 30(a) [54]. In this circuit, the feedback reset switch is replaced by the elementary S/H branch consisting of C_3 and its two associated switches. Assume that the circuit is used as a noninverting amplifier, and hence the clock phases shown outside of the parentheses in Fig. 30(a) are valid. Then, when $\phi_2 \rightarrow 1$, C_1 discharges into C_2, and the valid output voltage is generated. This voltage is stored in C_3. When $\phi_1 \rightarrow 1$ next, C_3 becomes the feedback capacitor, while C_1 samples the difference between the input and the voltage at node Ⓐ and C_2 discharges. If the signal bandwidth is much smaller than $f_s/2$, i.e., if the signal is significantly oversampled, then V_{out} does not vary much from one clock phase to the next. Thus for a finite dc

ANALOG EXHIBIT 1002
Page 114 of 321

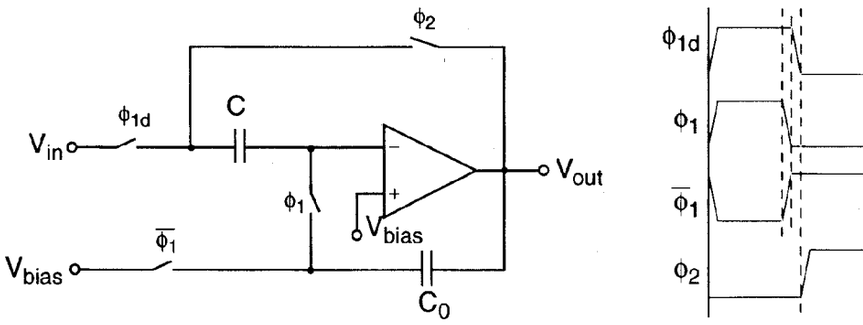


Fig. 37. Offset- and gain-compensated SC buffer.

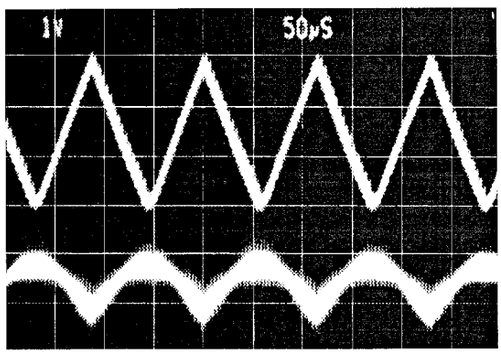


Fig. 38. Experimentally observed output voltages for offset-compensated SC buffers with a triangle-wave input at high clock rates. Top curve: buffer of Fig. 37; bottom curve: buffer of Fig. 29.

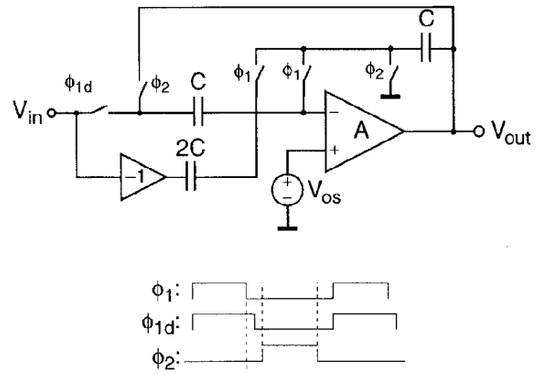


Fig. 39. A wide-band T/H stage.

op-amp gain A, the signal voltage $-V_{out}/A$ at the virtual ground is a slowly varying signal which is therefore nearly cancelled by the CDS switching of C_1 and C_2. This reduces the effect of finite A on the voltage gain of the stage.

Fig. 30(b) illustrates the clock phases and waveforms of the amplifier. When $\phi_1 \rightarrow 1$ and the reset phase begins, there is a small step $\Delta V = V_{os} - V_{out}/A - (C_1/C_3)\Delta V_{in}$ in the output voltage, where ΔV_{in} is the change in V_{in} during the $\phi_2 = 1$ interval (The ΔV_{in} term enters only for noninverting operation.) This step occurs because, as $\phi_2 \rightarrow 1, C_3$ is disconnected from ground and reconnected to the virtual ground. As ΔV is of the order of a few mVs, this does not require a fast settling time or a high slew rate from the op-amp. The dc output offset voltage is $(1 + C_1/C_2)(V_{os}/A)$, which is much smaller than V_{os}.

Detailed analysis [54] shows that the gain is now weakly frequency dependent due to the high-pass CDS effect on the virtual ground voltage, with the dc gain given by

$$H(z)|_{z=1} = \frac{-\frac{C_1}{C_2}}{1 + \frac{\left(1 + \frac{C_1}{C_2}\right)}{A^2}}. \tag{42}$$

As (42) demonstrates, the error term in the denominator of the transfer function is now proportional to A^{-2}, rather than A^{-1}. Thus the effective value of the op-amp gain as far as the dc gain is concerned is the square of the true value. Circuits with this property are called *gain-enhanced* or *gain-squaring* stages.

Fig. 31 shows a differential-input/single-ended-output SC amplifier incorporating the described principle [55]. Its CMOS implementation exhibited an accurate stage gain and a total of about 10 mV output offset, a 0.1–0.2% signal distortion and a 50 dB CMRR, in addition to a very low op-amp gain sensitivity.

The circuit of Fig. 30 was also successfully used in an GaAs SC amplifier, where the op-amp gain was restricted by the technology used [60].

The frequency dependence of the voltage gain of the compensated amplifier can be reduced, and thus the operation of the circuit extended to higher signal frequencies, by using the anticipatory compensation (prediction/correction) principle illustrated by the circuit shown in Fig. 32 [56]. Here, the precharging of the signal-processing capacitors is performed using the virtual-ground signal voltage that is expected to be present during the next amplification phase. This is achieved by essentially duplicating the SC branches used in the amplifier, and performing an anticipatory amplification step during the $\phi_2 = 1$ phase. If V_{in} changes only when $\phi_1 \rightarrow 1$, the operation will be independent of the rate of change of V_{in}, and hence of the signal frequency.

ANALOG EXHIBIT 1002
Page 115 of 321

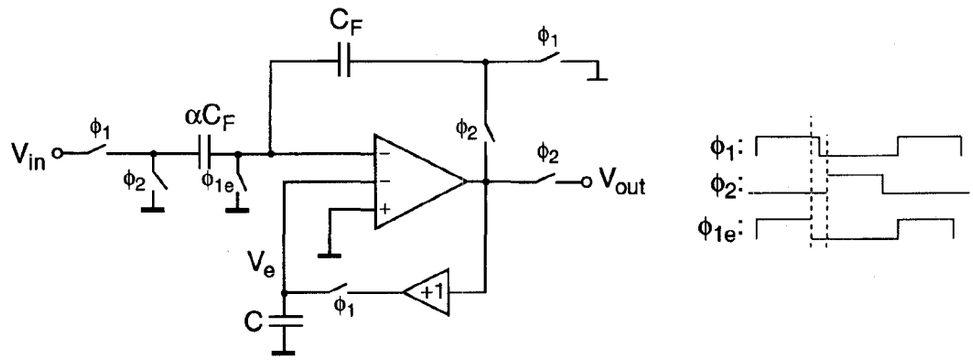


Fig. 40. Offset-compensated SC voltage amplifier using a low-sensitivity auxiliary input.

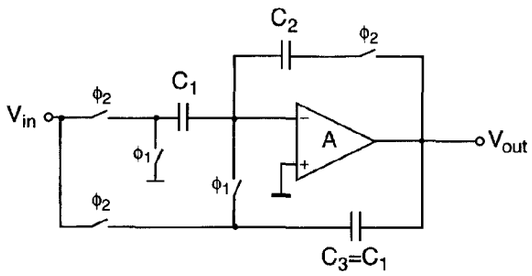


Fig. 41. Offset- and gain-compensated SC integrator.

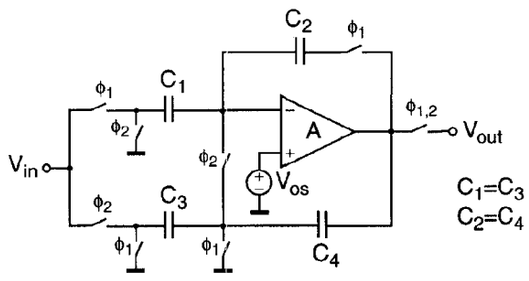


Fig. 42. Wideband compensated SC integrator.

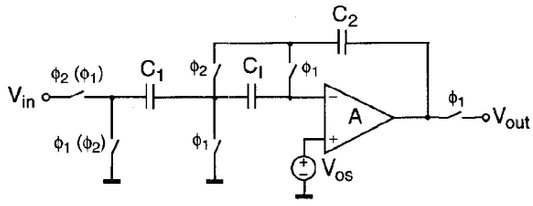


Fig. 43. SC integrator with offset-storing capacitor.

The effectiveness of this principle is illustrated in Fig. 33, which compares the gain error versus frequency responses of an uncompensated SC amplifier with that of the stage of Fig. 30, and of the circuits of Figs. 32 and 36. The ratio of the dc op-amp gain to the desired stage gain was about 30. As the curves illustrate, the dc gain error is higher for the anticipating stage (because the error term is now $(1 + C_1/C_2)^2/A^2$, rather than $(1 + C_1/C_2)/A^2$ as for the circuit of Fig. 30, but the error remains essentially constant all the way up to $f_s/4$. The output voltage step for a constant input due to offset and finite gain is $\Delta V = (1 + C_1/C_2)(V_{os} - V_{out}/A)$. This is again typically of the order of 10 mV, not putting much strain on the op-amp.

The gain-enhancing property of CDS also helps to reduce the harmonic distortion caused by the nonlinear op-amp gain characteristics [74]. This is illustrated in Fig. 34, which compares the output spectra of the amplifiers of Figs. 28 and 32 for a 4.4 V output sine-wave signal. The assumed op-amp gain characteristic is shown in Fig. 35.

A different implementation of the anticipatory compensation principle, which uses an offset-storage capacitor C_I playing a somewhat similar role to that of C in the autozeroed amplifier of Fig. 21, is shown in Fig. 36 [57]. Its frequency response is very similar to that of the circuit of Fig. 32, and is also included in Fig. 33 (bottom curve).

The gain-compensating techniques described above can also be extended to the design of unity-gain buffers, T/H stages and memory or delay stages. Fig. 37 shows an improved version of the offset-compensated buffer of Fig. 29, which does not require the resetting of the output voltage to V_{os} in every clock period [58]. Here, the reset switch is replaced by the S/H capacitor C_0 which holds the output voltage close to its previous value during the reset period. This also reduces the effects of the finite op-amp gain.

Fig. 38 shows some experimental results demonstrating the speed improvements achieved by this scheme over that of Fig. 29 [58].

An even faster version of the circuit, which relies on anticipating rather than storing the output voltage, is shown in Fig. 39 [59]. It is only practical to implement in fully differential form. In this circuit, the output signal tracks the input during the $\phi_1 = 1$ interval without inverting it. Hence, the virtual ground voltage at the instant when $\phi_2 \rightarrow 1$ will have the required value, independent of the signal frequency.

An alternative approach to offset compensation, which can also include the compensation of clock-feedthrough effects, but which does not enhance the effective value of

ANALOG EXHIBIT 1002
Page 116 of 321

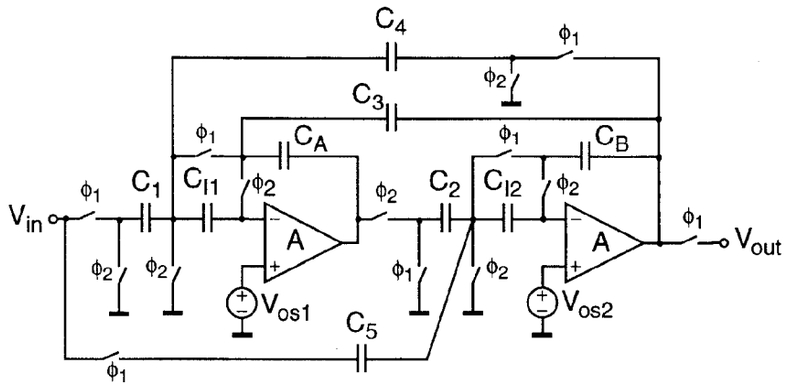


Fig. 44. Gain- and offset-compensated high-Q biquad.

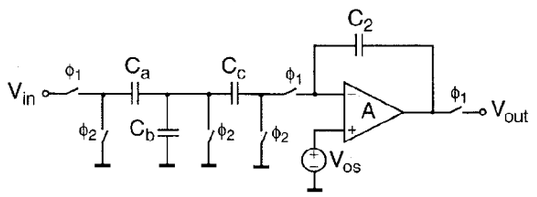


Fig. 45. Basic very-large-time-constant (VLT) integrator.

the dc op-amp gain, was discussed in Section IV-E earlier. It is shown schematically in Fig. 40. In this circuit, during the compensation phase ($\phi_1 = 1$), an error correction voltage V_e is developed across C. To reduce the effect of charge injection occurring when C is disconnected from the buffer as $\phi_2 \rightarrow 0$, the gain $|V_{\text{out}}/V_e|$ should be much lower than the signal gain of the op-amp. (See Section IV-E for a discussion of the optimization of this circuit.)

B. SC Integrators and Filters

The compensation schemes described in Section V-A are, with minor modifications, applicable also to SC integrators. As an overview of Section V-A reveals, these schemes fall into the following categories:

1) output is reset to V_{os}; input capacitor stores and then subtracts V_{os} (Figs. 28 and 29);
2) output is held during reset; input and feedback capacitors are referenced to the previous value of virtual-ground voltage V_A (Figs. 30, 31, and 37);
3) output during reset anticipates the next signal output; signal-path capacitors are referenced to the anticipated value of V_A with (Fig. 36) or without (Figs. 32 and 39) the use of an extra offset-storage capacitor C_I;
4) auxiliary input signal is established during reset; then it compensates for slowly varying noise effects (offset, $1/f$ noise, clock feedthrough); see Fig. 40.

As discussed above, the circuits using techniques 1) and 4) are relatively simple, but they cannot provide finite-gain compensation. Those using scheme 2) are more complex, but they perform also gain squaring at or near dc. Finally, the circuits using the anticipatory compensation scheme 3) tend to be even more elaborate, but they provide gain compensation over a wide signal-frequency range. This improves the linearity of the stage. The use of more switches may, however, increase the sampled wideband noise in the output signal of these circuits.

Next, we shall briefly discuss how these CDS techniques can be used in SC integrators. In Fig. 28(a), by eliminating the switch grounding the right-side terminal of C_2 during reset, an offset- (but not gain-) compensated integrator results [51]. Similarly, it is possible to leave out the grounding switch of C_2 in the circuit of Fig. 30(a) to obtain an offset- and gain-compensated SC integrator [61]. However, the charge flow into node A from C_1 as $\phi_1 \rightarrow 1$ is now not balanced by an equal and opposite charge from C_2 as in Fig. 30(a), and hence, the gain compensation becomes inaccurate. This problem can be solved for an inverting integrator by a slight change in the switching arrangement for C_3 [54], as shown in Fig. 41. For noninverting integration, a slightly more elaborate circuit is needed [54].

Similarly, the wideband amplifier of Fig. 32 can be transformed into a gain- and offset-compensated integrator [56] by eliminating the switches discharging the feedback capacitor C_2 (Fig. 42).

Efficient gain- and offset-compensated integrators can also be obtained by using an offset-storage capacitor C_I. Fig. 43 illustrates a noninverting integrator [57] based on this principle. The circuit can also be used as an inverting integrator with a full clock period delay, if the clock phases of the input switches are interchanged. It was later independently recognized by several researchers [62], [63] that the integrator of Fig. 43 can also be used as a delay-free inverting integrator, by changing its switching scheme and choosing the value of C_I equal to that of the feedback capacitor C_2.

It is also possible to apply scheme 4) (i.e., auxiliary input compensation) to SC integrators [64]. As before, the correction reduces the low-frequency noise (including that due to charge injection), but it does not compensate for

ANALOG EXHIBIT 1002
Page 117 of 321

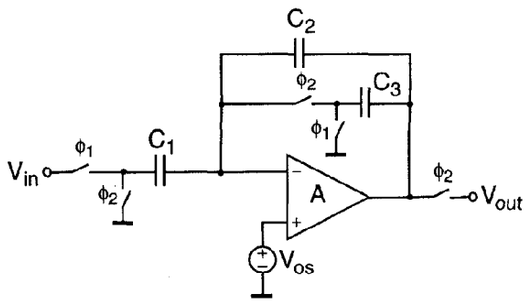


Fig. 46. Improved VLT integrator.

finite op-amp gain effects. It was used successfully in a high-accuracy low-voltage CMOS A/D converter [66].

Using the compensated integrators as building blocks, SC filters can thus be made insensitive to offset, $1/f$ noise and finite-gain effects. As an illustration, Fig. 44 shows a gain- and offset-compensated high-Q biquad [67] based on the modified version of the integrator of Fig. 43.

An important application of offset- and gain-compensated integrators is in delta-sigma A/D converters. Low-frequency noise and offset in the input integrator of the converter enters the output signal unfiltered, and hence should be suppressed. Also, in the cascade (MASH) architecture, the finite gain of the op-amp of the input stage allows the leakage of large unfiltered 1-b quantization noise into the output signal. Both problems can be remedied by using a compensated integrator in the input stage. Successful implementations of delta-sigma converters using offset- and gain-compensated front ends have been reported in [68]–[70].

C. SC Filters with Very Large Time Constants

In some applications, the magnitudes $|p_i|$ of the poles realized by SC filters are much smaller than the clock frequency $f_s = 1/T$. Since the time constants TC_2/C_1 of the integrators used in the filter are around $1/|p_i|$, now $C_2/C_1 \approx 1/(|p_i| \cdot T) \gg 1$ is required. This results in large chip area requirements. To remedy this situation, several ingenious schemes have been proposed. One option [72] is to use a T-cell attenuator at the input (Fig. 45). As a result of the charge redistribution in the T-cell, the capacitance spread $S = C_{\max}/C_{\min}$ can be reduced approximately to $\sqrt{S}$, and the chip area will be correspondingly smaller.

The T-cell integrator is sensitive to the stray capacitance in parallel with C_b, and it requires two large capacitors (normally, $C_b = C_2 \approx \sqrt{S} \cdot C_a = \sqrt{S} \cdot C_c$ are chosen). An improved very-large-time-constant (VLT) integrator [73] is shown in Fig. 46. Analysis shows that the circuit is equivalent to an integrator with a capacitance ratio $C_2/C_1 > 1$, followed by a voltage division by $1+C_2/C_3$. If $C_1 = C_3 \approx C_2/\sqrt{S}$ are chosen, the ideal performance of the circuit will be the same as that of the T-cell integrator; however, it is stray-insensitive, and it needs only one large capacitor, C_2.

A major flaw of both VLT circuits is their extreme sensitivity to offset, noise and charge-injection effects. To illustrate this point, consider the dc offset performance

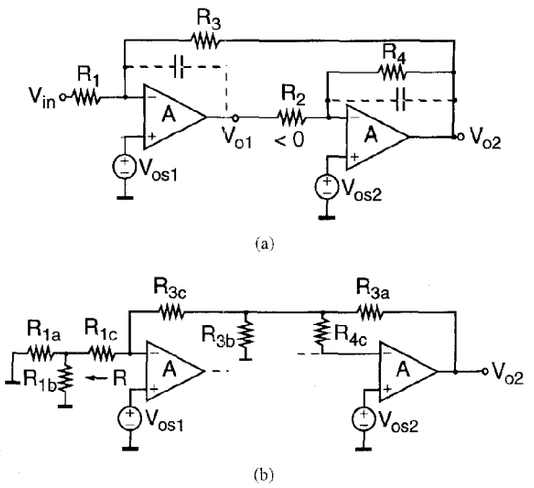


Fig. 47. The dc equivalent circuits: (a) dc equivalent circuit of a low-Q biquad and (b) dc equivalent circuit of a VLT biquad using T-cells.

of a conventional two-integrator loop where the familiar SC $\leftrightarrow$ R equivalence [50] was used [Fig. 47(a)]. Since V_{o2} has to generate V_{os1} at the virtual ground of the first op-amp by voltage division, we obtain $V_{02} = (1+R_3/R_1)V_{os1}$. For a VLT biquad, R_3 and R_1 are both large, and $V_{02} \approx 2V_{os}$ to $10\,V_{os}$ results. By contrast, for a T-cell biquad, as the dc equivalent circuit of Fig. 47(b) illustrates, V_{o2} is divided twice before producing V_{os1}. This requires a much larger output offset voltage V_{o2}, often as large as $100\,V_{os1}$ to $200\,V_{os1}$. A similar argument shows that charge injection will also cause a large output offset. While the explanation is not so obvious for the VLT integrator of Fig. 46, it leads to a similar result: small dc offsets become amplified 100 times or more in the output signal of filters containing such stages.

To reduce this sensitivity, the VLT integrators should be compensated for their low-frequency noise, offset, and (if possible) charge injection. Figs. 48 and 49 illustrate the use of offset-storing capacitors in the circuits of Figs. 45 and 46, respectively [71]. These circuits reduce the low-frequency noise, and also the finite-gain effect on the frequency response. They do not, however, compensate for charge feedthrough; hence, the VLT filters should make full use of the well-known techniques (fully differential circuitry, delayed-cutoff clock signals, dummy switches, etc.) for reducing clock-feedthrough effects.

The improvement in finite-gain performance afforded by the compensated integrators is illustrated in Fig. 50. This shows the simulated gain responses of an eighth-order SC low-pass filter with Bessel–Chebyshev characteristics, a clock rate $f_s = 9.766$ kHz and a cutoff frequency of 2.5 Hz. The circuit of Fig. 46 was used, with (top curve) and without (bottom curve) gain- and offset-compensation. An op-amp gain of only 40 dB was assumed. The phase response is also distorted by the finite op-amp gain and restored by using CDS.

ANALOG EXHIBIT 1002
Page 118 of 321

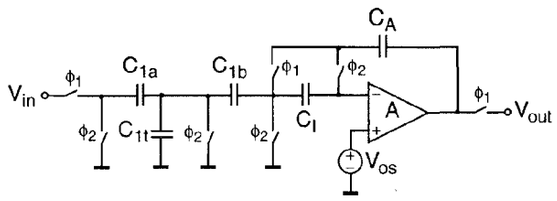


Fig. 48. T-cell integrator with offset compensation.

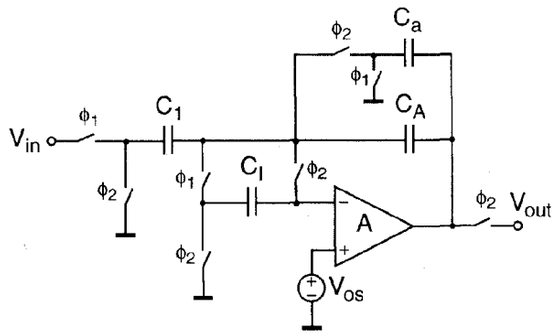


Fig. 49. The VLT integrator of Fig. 46 with offset compensation.

VI. A Micropower Low-Noise Chopper Amplifier Using the Chopper Stabilization Technique

This section presents a practical example of the use of the CHS technique in an amplifier to reduce its offset and $1/f$ noise without degrading the wideband noise. Unlike the many examples of the use of CDS in SC circuits, some of which were presented in Section V, there are very few examples of circuits that use CHS. The latter are generally low-noise continuous-time amplifiers, mainly used for instrumentation applications such as biomedical electronics.

Some applications such as electronic sensor interfaces require not only a very small offset and offset drift, but also very low noise. Often, the CHS technique is best suited to such applications. The electronics containing the front-end low-noise amplifier and the signal conditioning circuits, combined with the sensor, forms a microsystem which often has to be portable or stand alone, and is therefore battery powered. Hence, the power consumption of the electronics has to be small. It is therefore even more crucial to eliminate the $1/f$ noise and to reduce the noise down to the fundamental thermal noise which is mainly determined by the allowable current consumption of the input stage.

Examples of low-noise chopper amplifiers with a very low power consumption have been presented in [8], [12]. The design objective was to reach the microvolt level for both offset and noise, with a bandwidth limited to a few hundred Hz, while maintaining the power consumption below 100 μW. This chopper amplifier used a selective stage with its center frequency locked to the chopper frequency in order to minimize the residual offset, as explained in Section III. The chopper amplifier presented in Fig. 9 where the amplifier is replaced by a selective amplifier and the

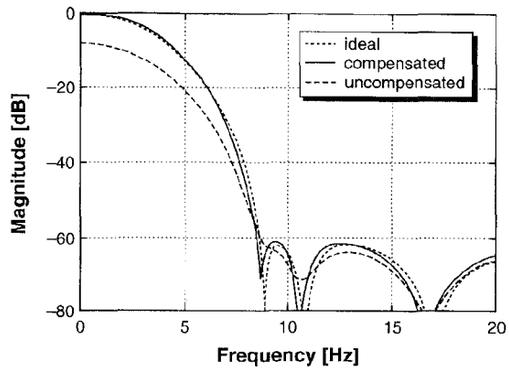


Fig. 50. Frequency responses of VLT filters.

output is low-pass filtered at half the chopper frequency, has an overall low-pass transfer function given by

$$G_0(s) \cong \frac{8}{\pi^2} \frac{A_{\max}}{1 + s/\omega_c} \tag{43}$$

where $\omega_c = \omega_0/(2Q)$ is the chopper amplifier's cutoff frequency, determined by the selective amplifier's resonant frequency ω_0 and quality factor Q. $A_{\max}$ corresponds to the gain of the selective amplifier at the resonant frequency. Equation (43) has been obtained assuming that $Q \gg 1$ and is valid for $|s \ll \omega_0$. It shows that the chopper amplifier's dc gain is only $\pi^2/8 = 1.234$ (or approximately 2 dB less than the gain of the selective amplifier at the resonant frequency).

The selective amplifier can be realized using either a low-pass [12] or a band-pass second-order $g_m - C$ continuous-time filter [44]–[49]. The advantage of choosing the band-pass circuit is that the input and output chopper modulation signals can be identical, since there is no phase shift at the resonant frequency. The filter's resonant frequency can be locked to the chopper frequency by means of a PLL using either a voltage-controlled reference filter [44], [48] or a voltage-controlled oscillator built using the same resonator as the selective amplifier [44], [47], and [49].

An example of such a band-pass filter is presented in Fig. 51. The gain $A_{\max}$ at the resonant frequency is given by the ratio g_{m1}/g_{m4}, where g_{m1} and g_{m4} are the transconductances of the input and output stages, respectively. This ratio has to be large in order to have a sufficient dc gain for the chopper amplifier. Typically, for a dc gain of 500, the g_{m1}/g_{m4} ratio has to be 617! This large gain imposes the use of linearized transconductors for realizing the integrators and the output load [47], in order to limit the distortion and intermodulation. Another problem arising from this large gain is the mistuning effect resulting from the difference between the bias currents of the integrators. This is due to the fact that the offset of the input differential pair T_1–T_1' appears at the low-pass output multiplied by the corresponding dc gain, while the band-pass output offset stays at zero. This offset voltage is fed to the input of differential pair T_3–T_3' and compensates the offset current due to the input differential pair, forcing the band-pass

ANALOG EXHIBIT 1002
Page 119 of 321

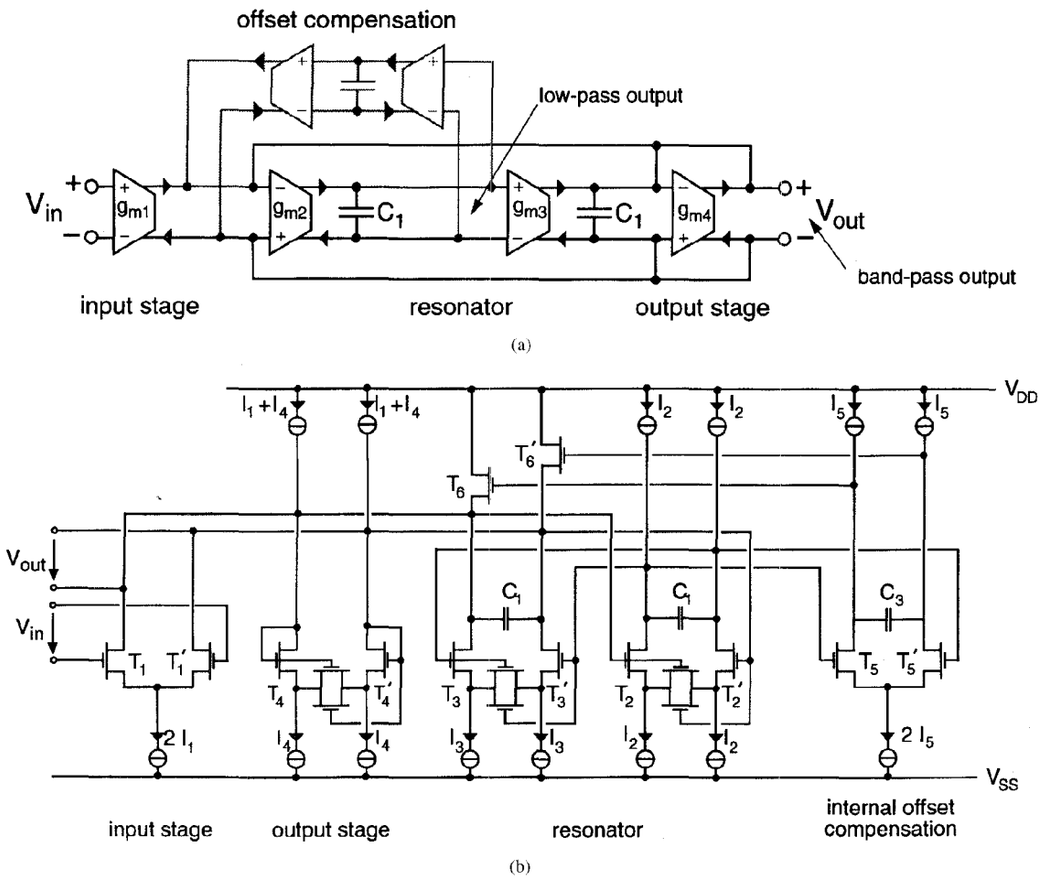


Fig. 51. Second-order $g_m - C$ continuous-time band-pass filter used to realize the selective amplifier: (a) principle and (b) implementation.

output to stay at zero. The resulting mismatch between the biasing points of the two integrators gives rise to a nonzero phase shift at the chopper frequency, which is unacceptable for the chopper amplifier. Fortunately, since the signal is modulated and amplified at high frequency, the current offset ΔI_1 produced by the mismatch of input differential pair T_1–T_1' can be compensated without changing the signal transfer function. This offset compensation can be realized as shown in Fig. 51, by sensing the offset voltage with differential pair T_5–T_5' at the low-pass output (i.e., at the input of differential pair T_3–T_3' and injecting the current necessary to compensate the offset current ΔI_1 using transistors T_6–T_6'. This compensation does not require any S/H action since the signal is mainly centered around the resonant frequency. The feedback loop can therefore be held closed continuously if a compensation capacitance C_3 is added at the output of differential pair T_5–T_5' to ensure stability.

The measured frequency responses of the selective amplifier and the chopper amplifier are shown in Fig. 52(a) and (b), respectively. The gain measured at the filter's 4 kHz resonance frequency is equal to 56.8 dB, corresponding to a 54.8 dB dc gain for the chopper amplifier. The quality factor is 5.4 which sets the -3 dB cut-off frequency of the chopper amplifier to 367 Hz.

Using (21), the chopper amplifier's input-referred noise can be found from

$$S_{Nin} = \frac{\pi^2}{8} 4\gamma kTR_{Nin}\left(1 + 0.8525\frac{f_k}{f_{chop}}\right) \qquad (44)$$

where R_{Nin} is the equivalent input thermal noise resistance of the selective amplifier, which is inversely proportional to the transconductance g_{m1} of the input differential pair. Noise factor γ is defined as the product $g_{m1}R_{Nin}$ and accounts for the excess thermal noise coming from sources other than the input stage.

The low-frequency output noise of the chopper amplifier has been measured and is shown in Fig. 53. As expected, the $1/f$ noise has disappeared, leaving a white noise PSD corresponding to an equivalent input-referred white noise of 43 nV/$\sqrt{\text{Hz}}$, which can still be made lower at the expense of an increase of the input differential pair bias current and thus of the total power consumption.

The input and output chopper modulators are simply realized by four switches controlled by complementary phases,

ANALOG EXHIBIT 1002
Page 120 of 321

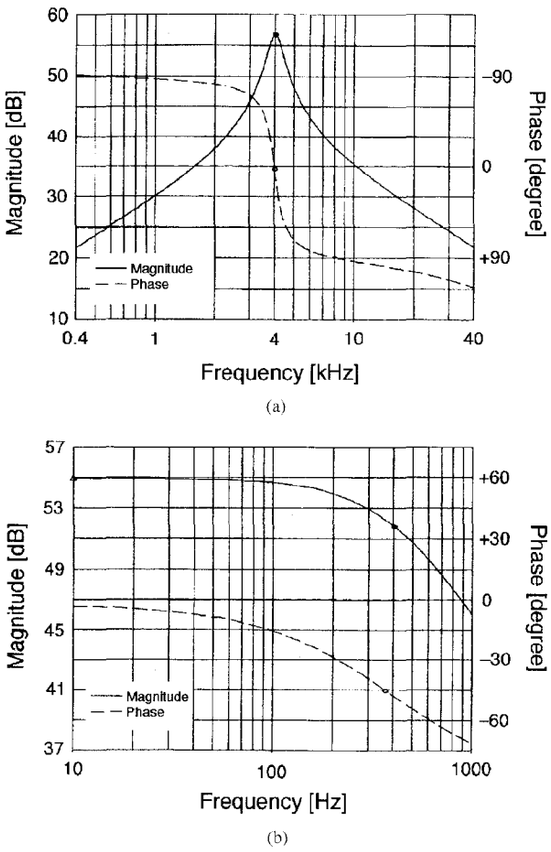


Fig. 52. Measured frequency response of the selective amplifier (a) and the chopper amplifier (b) with a chopper frequency locked to the 4 kHz resonance frequency.

as shown in Fig. 54, where capacitance C_{in} represents the differential input capacitance of the selective amplifier.

At each switching instant, error charges Δq_i $(i = 1, 2, 3)$ result from charge injection and clock-feedthrough mismatches between the different switches. Charges Δq_1 and Δq_3 flow to capacitor C_{in}, while charge Δq_2 flows to ground through the source resistance R_S, producing some spikes at the input of the selective amplifier. An estimation of the residual input-referred offset V_{os} of the chopper amplifier due to the injection of these charges can be derived by assuming that:

1) clock rise and fall times are much smaller than the time constant τ of the spikes;
2) the output modulator is ideal;
3) $\Delta q_1 = \Delta q_2 = -\Delta q_3 - \Delta q$ (representing the worst case);
4) all switches have the same on-resistance R_{on};
5) the source resistance R_S is much smaller than R_{on}.

This leads to [8], [12]

$$V_{os} \cong 4\pi f_{\text{chop}} \Delta q R_{on} (2\pi f_{\text{chop}} R_{on} C_{in} + Q\varepsilon_{tun}) \quad (45)$$

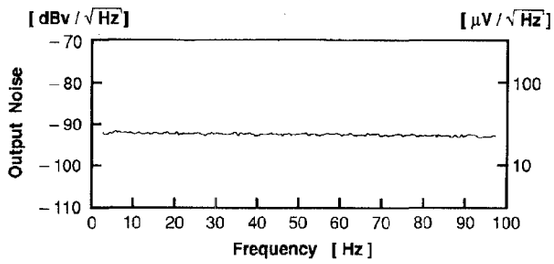


Fig. 53. Measured low-frequency output noise PSD of the complete chopper amplifier.

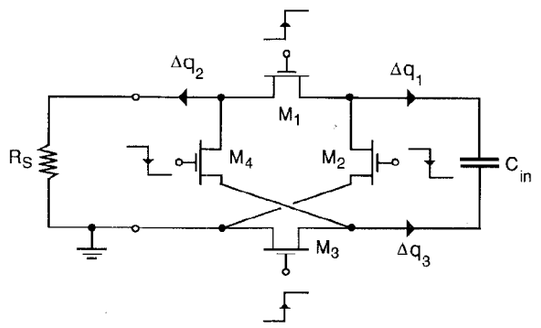


Fig. 54. Implementation of the input chopper modulator.

where $\varepsilon_{tun} \equiv |f_0/f_{\text{chop}} - 1|$ represents the tuning error between the resonance frequency f_0 and the chopper frequency f_{chop}. It can easily be shown that the product $\Delta q R_{on}$ is independent of the switch width W and is minimum for a minimum channel length. Equations (44) and (45) show that there is a trade-off between the noise and the offset with respect to the chopper frequency: according to (45), the chopper frequency should be chosen as small as possible, but nevertheless equal to or larger than the amplifier's corner frequency. In the case where both offset and noise have to be minimized, it is useful to define a total noise power as the sum $V_{os}^2 + V_{Nin}^2$ where V_{Nin} is the total input-referred noise rms voltage. An optimum value of the chopper frequency can be found such that this total noise power is minimum for a given signal bandwidth [8].

The linear dependence of the input-referred offset on small tuning errors as indicated by (45), has been verified experimentally and is presented in Fig. 55. An input-referred offset as small as 0.5 μV and a sensitivity to the tuning error of 0.47 μV per percent of mistuning has been measured.

In case the source resistance R_S is much larger than the switch on-resistance R_{on}, the input offset is still given by (45) but R_{on} has to be replaced by R_S. Hence, the input offset increases quadratically with the source resistance which is in accordance with the experimental results presented in Fig. 56.

The offset voltage drift could not be measured, but other chopper-stabilized amplifier have reported extremely good stability.

ANALOG EXHIBIT 1002
Page 121 of 321

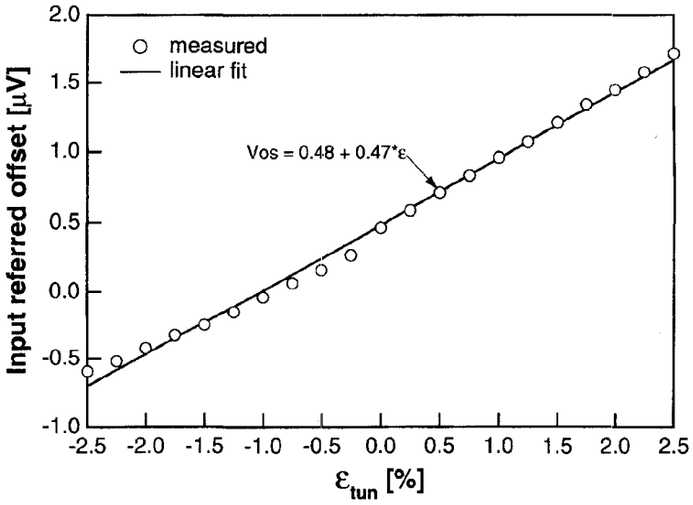


Fig. 55. Measured input referred offset versus tuning error.

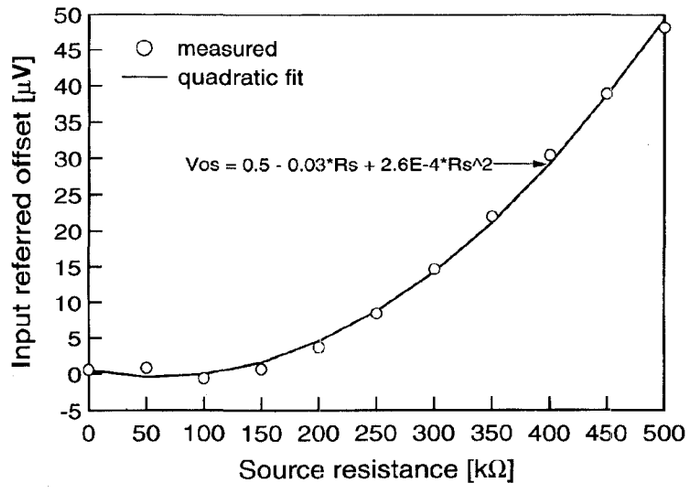


Fig. 56. Measured input referred offset versus source resistance.

VII. Conclusions

A detailed comparison of the relative advantages and disadvantages of the CHS technique versus CDS was given earlier [7], [8]. These are the main points.

1) CDS is inherently a sampled-data method; CHS is based on modulation rather than sampling, and hence can be used for continuous-time signals.
2) CDS reduces the low-frequency noise by highpass filtering; CHS translates it to some out-of-band frequency.
3) The output noise of a CDS stage is normally dominated by the undersampled wideband noise; in a continuous-time CHS stage the noise spectrum is not folded, and hence $1/f$ noise remains dominant in the baseband before the second modulation. After demodulation, white noise is folded into the baseband and replaces the $1/f$ noise. If the chopping frequency is much larger than the noise corner frequency, then the baseband white noise in the output is only very slightly larger than it was without CHS.
4) As shown earlier, CDS can also be used to enhance the effective gain of the op-amps used in the signal processing. A continuous-time CHS system, by contrast, causes the op-amp to amplify a higher-frequency signal, and hence its effective gain is usually reduced.

In conclusion, CDS is preferable in applications which inherently use sampled-data circuits (such as SC stages), so that the baseband noise behavior is not made worse by noise aliasing. Also, the dc offsets are eliminated, not just modulated to higher frequency, by CDS, which may improve the allowable signal swing. Finally, the gain-

ANALOG EXHIBIT 1002
Page 122 of 321

$$|H_n(f)|^2 = d^2\left\{\left[\frac{\sin\alpha}{\alpha} - \frac{\sin\beta}{\beta}\right]^2 + \left[\frac{1-\cos\alpha}{\alpha} - \frac{1-\cos\beta}{\beta}\right]^2\right\} \quad (50)$$

enhancing ability of CDS may be an important advantage in some applications. On the other hand, CHS is the method of choice if the system is a continuous-time one to start with, and if low baseband noise is an important requirement.

Appendix
Autozeroed Noise Analysis

The autozeroed voltage $v_{AZ}(t)$ shown in Fig. 2 can be approximated by

$$v_{AZ}(t) = \sum_{m=-\infty}^{+\infty} h(t - mT_s)[v_N(t) - v_N(mT_s)] \quad (46)$$

where it has been assumed that the RC time constant in the track mode is much smaller than the duration T_{AZ} of the AZ phase, i.e., that voltage $v_{AZ}(t)$ instantaneously goes down to zero at the beginning of the AZ phase. Here $h(t)$ is a window function corresponding to the hold phase:

$$h(t) \equiv \begin{cases} 1, & \text{for } 0 \le t < T_h, \\ 0, & \text{otherwise.} \end{cases} \quad (47)$$

If $v_N(t)$ is assumed to be a stationary random process having a PSD $S_N(f)$, the PSD of the autozeroed voltage is given by

$$S_{AZ}(f) \equiv \sum_{n=-\infty}^{+\infty} |H_n(f)|^2 S_N\left(f - \frac{n}{T_s}\right) \quad (48)$$

which consists of replicas of the original spectrum shifted by multiples of the sampling frequency and multiplied by the squared magnitude of the corresponding band transfer function. These transfer functions can be evaluated by calculating the Fourier transform of $v_{AZ}(t)$

$$H_n(f) = d[e^{-j\pi nd}\operatorname{sinc}(\pi nd) - e^{-j\pi\, dfT_s}\operatorname{sinc}(\pi\, dfT_s)] \quad (49)$$

where $d \equiv T_h/T_s$ is the duty cycle. The $|H_n(f)|^2$ functions are then readily obtained from (49) (see (50) at the top of the page) with $\alpha \equiv 2\pi\, dn$, $\beta \equiv 2\pi\, dfT_s$.

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ANALOG EXHIBIT 1002
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ANALOG EXHIBIT 1002
Page 125 of 321

A complete instrumentation voltage amplifier arises if we include the current-to-voltage conversion function of the load impedances Z_{L1} and Z_{L2}. In that case the reciprocal nominal overall voltage gain $1/A_{vn}$ and the overall CMCR $1/H_i$ are given by Eq.3.4.4.

$$1/A_{vn} = -1/Y_2 Z_{1d} \qquad (3.4.4)$$
$$1/H_i \approx 1/H_e + 1/F_e H_{iL}$$

with: $Z_{Ld}=Z_{L1}+Z_{L2}$, $1/H_{iL}=\triangle Z_{L1}/Z_{1d}$, $\triangle Z_{L1}=Z_{L1}-Z_{L2}$.

The reciprocal value of the discrimination factor is defined as: $1/F_e=(I_{2c}/V_{ic})/I_{2d}/V_{id})=1/Z_{tcce}Y_{tn}$.

From the above expression we see that a low overall CMCR $1/H_i$ can only be obtained if the amplifier has a low CMCR $1/H_e$ as well as a low reciprocal discrimination factor $1/F_e$. The effect of the latter term is further reduced by a low CMCR $1/H_{iL}$ of the load circuit.

Instrumentation Voltage Amplifier

An instrumentation voltage amplifier with a voltage-source character between the output terminals arises if we insert a balanced floating impedance amplifier with an OFA and two impedances Z_{11} and Z_{12} between the preceding example's instrumentation transadmittance amplifier and its load circuit [3.3, 3.4].
The complete instrumentation voltage amplifier circuit is drawn in Fig. 3.4.4 together with the source and load circuits.

The reciprocal nominal overall differential voltage gain and the CMCR of the complete amplifier are described by Eq.3.4.5.

$$1/A_{vn}=-1/Y_2 Z_{1s} \qquad (3.4.5)$$
$$1/H_i \approx 1/H_e + 1/F_e H_i$$

with: $Z_{1s}=Z_{11}+Z_{12}$, $1/H_1=\triangle Z_1/Z_s$, $\triangle Z_1=Z_{11}-Z_{12}$

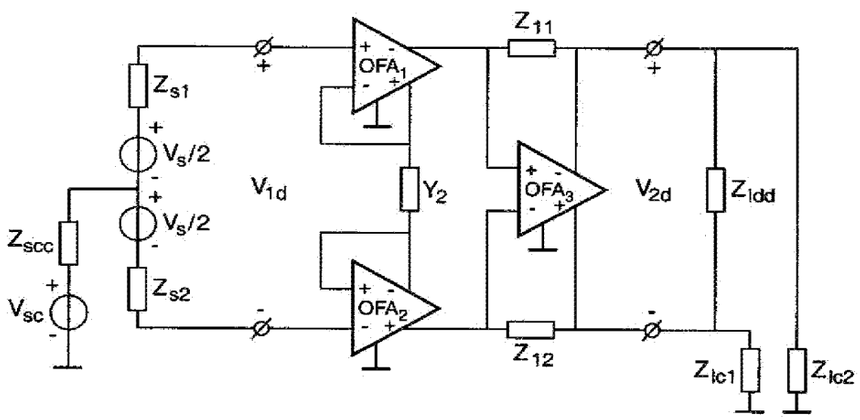


Fig. 3.4.4: Instrumentation voltage amplifier with source and load circuits

The instrumentation amplifier has a floating entrance port and an independently floating exit port. It measures the differential entrance voltage at nominal zero entrance currents. The differential exit port has a voltage source character.

Instrumentation Current Amplifier

If we change the sequence of the transadmittance and transimpedance amplifiers of the preceding example we obtain an instrumentation current amplifier. This circuit is drawn in Fig. 3.4.5 together with the source and load circuits.

The overall reciprocal nominal current gain is given by Eq.3.4.6.

$$1/A_{vn} = -1/Y_2 Z_{1s} \qquad (3.4.6)$$

SA 21.3: A High-Performance Autozeroed CMOS Opamp with 50μV Offset

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[3]Ganesan Consulting, Austin, TX

Bandwidth, dc gain, offset and noise are the major performance parameters that limit the applicability of operational amplifiers (opamps). The design of a general-purpose opamp in a digital CMOS process that offers excellent performance in all these categories is a long-standing challenge for the analog designer. While MOSFET amplifiers have extremely small bias currents, they exhibit much larger offset voltages and low-frequency noise than their BJT counterparts.

A high-performance opamp in a 1μm 5V digital CMOS technology achieves high dc gain, as well as excellent PSRR and CMRR and is capable of driving a 100Ω, 1nF load. It uses a mixed-mode (analog/digital) compensation loop to reduce input offset to <50μV. The loop uses digital offset extraction and storage circuitry, and has an analog current-mode output. Offset cancellation can be performed at power-up or upon request.

Unlike existing commercially available low-offset high-precision amplifiers, the opamp needs only a single 5V low-voltage supply, requires no trimming, and uses no BJTs or JFETs. Thus, although developed as a stand-alone product, it can potentially be used as an on-chip component of larger mixed-mode ICs.

A schematic of the autocalibrated offset opamp is shown in Figure 1. For high dc gain, large bandwidth, high CMRR and PSRR, and drive capability, the opamp is built around a 3-stage topology: two gain stages and one rail-to-rail, class AB output stage. The input pair M1 and M2 is cascoded by transistors M5 and M6 to maximize CMRR performance. A multipath nested Miller topology is used for frequency compensation [1]. The additional input pair M3 and M4 bypasses the intermediate stage M7 and M8 at high frequencies to improve stability.

A smooth transition from the high-gain, low-frequency path to the low-gain, high-frequency path requires matching transconductances of M1 and M2 to those of M3 and M4. The class-AB output stage features rail-to-rail voltage swing and incorporates additional switches (M12 and M13) to put the output node into high-impedance mode during auto-calibration [2]. The offset cancellation uses a current-mode DAC (CALDAC), the full-scale current of which is approximately 10% of the input pair tail current. This allows the cancellation of up to ±5 mV input offset. The digital code producing the cancellation current is stored in the successive approximation register (SAR).

During autocalibration, when CAL=1, the opamp is removed from the signal path. Both inputs are tied to GND and the output transistors M10 and M11 are disconnected from their respective supplies. The output is thus floating, while the small replica transistors M20 & M21 (scaled to M10 & M11) are used to provide the amplifier output signal for the calibration circuit. The compensation capacitors Cc1, Cc2 and Cc3 are no longer necessary since the opamp is now used in open-loop configuration as a comparator, and are also disconnected from the output terminal. When offset cancellation is initiated after power-up or user request, an on-chip RC oscillator is activated to provide timing of the successive approximation algorithm, which is completed after N clock cycles, where N is the number of bits required by the DAC.

During calibration, the output offset voltage approaches zero, and the amplifier enters its linear operating range. However, due to high-frequency noise, the output voltage may swing rapidly up and down, since the opamp is no longer band-limited by the compensation capacitors. This could severely limit the accuracy of an offset cancellation procedure (such as the successive approximation algorithm) that does not involve some kind of averaging.

This is the reason why a simple low-pass filter (LPF) is introduced in the decision chain. The LPF is implemented here in an analog manner and is followed by a Schmitt trigger to interface with the SAR logic. Note that filtering could be implemented digitally as well, but this was found to require more chip area.

The key opamp parameters CMRR, PSRR and offset drift are optimized for offset performance. The linearity of the CALDAC, however, is not important as long as its monotonicity is guaranteed. The DAC is implemented as a binary-weighted current array using a pseudo R-2R MOSFET ladder architecture that requires only 3N identical MOSFETS for N-bit resolution [3]. The DAC area is only 0.04mm² for N=12, including the control switches.

The ability to read from or to write into the SAR register directly is a feature of this architecture that allows easy monitoring of the offset performance by retrieving the digital code stored in the SAR after calibration. For example, during wafer test it is easy to check whether the offset stays within presribed limits by making sure that the opamp output changes from zero to VDD when lower and upper full-scale codes are entered successively into the SAR.

A die micrograph of the 2.2x1.9mm² chip containing two opamps is shown in Figure 2. It is in a 5V single-poly, double-metal, 1μm digital CMOS process. To fit into an 8-pin package while preserving compatibility with current industry standards, the circuit is programmed to perform offset auto-calibration automatically after power-up. Each opamp is protected against short-circuits and has its own biasing, calibration DAC and control logic. They share a 10kHz RC oscillator and frequency divider, power-on reset and test mode control logic. Autocalibration is simultaneous on both amplifiers and requires about 250ms. Performance of the op amp is summarized in Table 1, the offset and offset drift distributions are given in Figures 3 and 4. Equivalent noise input and amplification and phase margin variation with frequency are shown in Figures 5 and 6.

Acknowledgments

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References:

[1] Eschauzier, R. G. H., L. P. T. Kerklan, J. H. Huijsing, "A 100-MHz 100-dB Operational Amplifier with Multipath Nested Miller Compensation Structure," IEEE J. Solid-State Circuits, vol. SC-27. pp.1709-1717, Dec., 1992.

[2] Monticelli, D. M., "A Quad CMOS Single-Supply OP Amp with Rail-to-Rail Output Swing," IEEE J. Solid-State Circuits, vol. SC-21. pp.1026-1034, Dec., 1986.

[3] Vittoz, E. A., X. Arreguit, "Linear networks based on transistors," Electron. Lett., vol. 29, pp. 297-298, Feb., 1993.

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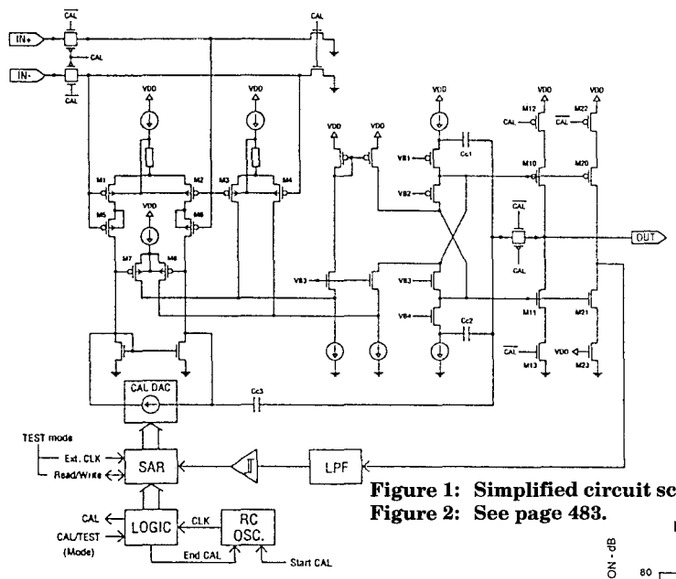


Figure 1: Simplified circuit schematic.

Figure 2: See page 483.

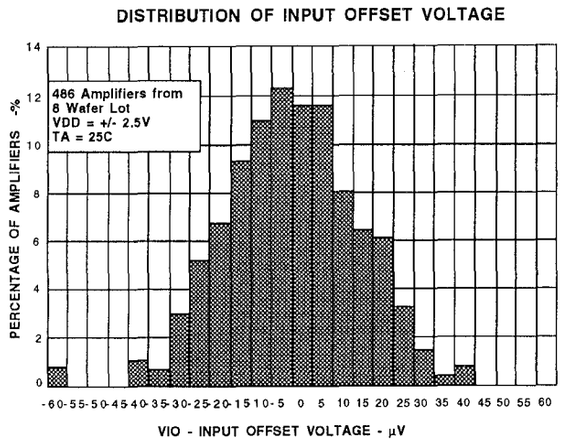


Figure 3: Distribution of input offset voltage.

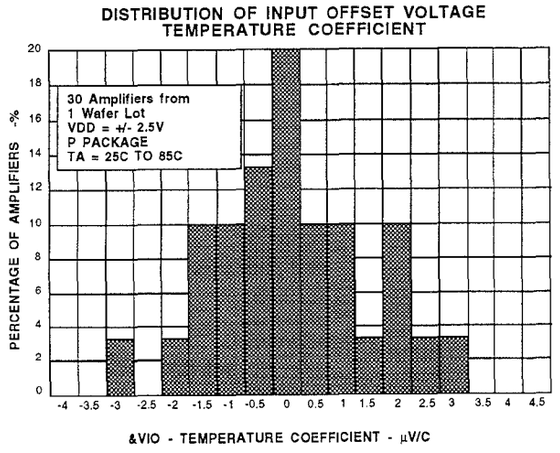


Figure 4: Input offset voltage temperature coefficient.

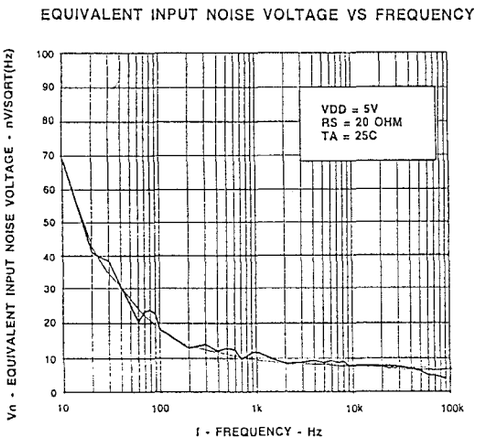


Figure 5: Equivalent input noise.

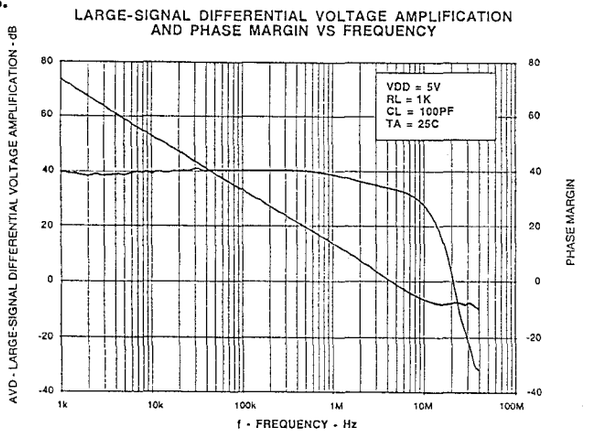


Figure 6: Amplification and phase margin vs. frequency.

	Min	Typ	Max	Unit
Input offset	-50	Figure 3	50	µV
Input offset drift	-3.0	Figure 4	3.0	µV/°C
Input offset		5		pA
Input bias		20		pA
Equivalent input noise at 10Hz/1kHz		70 /10		nV/√(Hz)
CMRR dc / 100kHz		105 / 65		dB
PSRR dc / 100kHz		120 / 65		dB
Common mode range	-0.2		3.2	V
Voltage gain (RL=1 kΩ)		4000		V/mV
Unity-gain bandwidth		4.5		MHz
Phase margin (CL=100 pF)	70			°
Full-power bandwidth		600		kHz
Slew rate	-33.		3.9	V/µs
Output swing (RL=600Ω)	0.1		4.9	V
Short-circuit current limiting		±60		mA
Supply current		1.3		mA
Supply voltage range	3.5		5.5	V
Offset calibration time		250		ms

Table 1 : Measured performance at VDD = 5V and Ta = 25°C.

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ANALOG EXHIBIT 1002
Page 129 of 321

Suppose that the current $\frac{I}{255}$ has an accuracy of $(1 - \delta)$; then after a full count of the fine integrator the error between the coarse current and the full fine integrated current value must be smaller than k LSB or:

$$I + \frac{I}{255} \times (1 - \delta) - 256 \times \frac{I}{255} \times (1 - \delta) \leq k \times \frac{I}{255}, \tag{7.4}$$

or

$$\delta \leq \frac{k}{255}. \tag{7.5}$$

In a 16-bits system a matching between the coarse and fine discharge currents better than 0.2 % is needed to obtain $\frac{1}{2}$ LSB differential linearity.

The accuracy with which the currents must be switched can be determined. Suppose that the clock time $t_0 = \frac{1}{f_{clock}}$, then with a time uncertainty in switching the current I of δt we obtain in case the fine full-scale integrated value must be smaller than k LSB error:

$$I \times (t_0 + \delta t) + \frac{I}{255} \times t_0 - 256 \times \frac{I}{255} \times t_0 \leq k \times t_0 \times \frac{I}{255}, \tag{7.6}$$

or

$$\delta t \leq \frac{k}{255} t_0. \tag{7.7}$$

With $t_0 = 40$ nsec and k = $\frac{1}{2}$ LSB we get $\delta t = 80$ psec.

7.5 Successive approximation converter system

The basic architecture of a successive approximation analog-to-digital converter is shown in Figure 7.6 The basic converter consists of a comparator stage (Comp.), the successive approximation register (SAR) and the digital-to-analog converter. A sample-and-hold and an anti-alias filter are added to limit the maximum analog input frequency and to convert the continuous time input signal into a discrete time signal. At the beginning of the conversion the MSB is switched on and the input signal is compared to the output signal of the D/A converter. When the input signal is larger than the output signal of the D/A converter, then the MSB remains on and the next bit is switched on and a comparison will be performed. A bit by bit operations is performed in this system to bring the D/A output signal within 1 LSB to the time discrete input signal. In the lower part of fig. 7.6 the conversion procedure as a function of bit weighting is shown. The output value

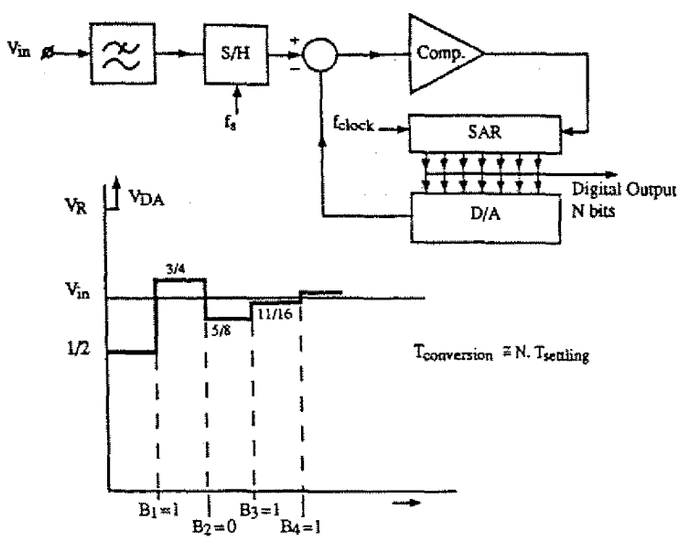


Figure 7.6 : Basic successive approximation A/D converter

in the figure equals 1011. A complete conversion in this system requires N switching and comparison operations to convert the input signal into a N-bit digital output value. The conversion time equals:

$$T_{conversion} = N.T_{settling}. \tag{7.8}$$

The settling time is defined as the time required to settle within $\frac{1}{2}$ LSB of the D/A converter. The linearity and accuracy of this system depends on the D/A converter.

7.5.1 Practical successive approximation A/D converter

A block diagram of a practical A/D converter [3] system is shown in Figure 7.7. The most important parts are the successive approximation logic, the D/A converter with the reference current source, the subtracter-comparator circuit using an operational amplifier to convert the analog input signal into a current, and the internal clock generator with the control logic. Digital input and outputs are TTL compatible. In the internal digital part current mode logic (CML) is used for speed. Because of the differential operation of

ANALOG EXHIBIT 1002
Page 131 of 321

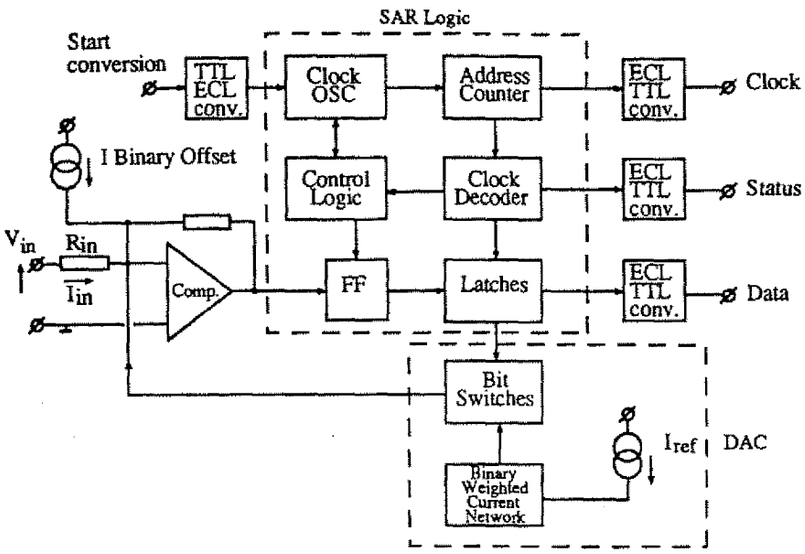


Figure 7.7 : Block diagram of the A/D converter system

the current mode logic low interference of the switching signals on the power supply lines is obtained. At the input a TTL-to-CML logic converter stage is incorporated, while at the output CML-to-TTL levels converters with output buffers are used. A scheme with addressable latches is used in the successive approximation register to minimize the number of components. Output data flow of the converter is in a serial mode to minimize the number of circuit pins and to reduce the noise generated by the TTL output signals. The start conversion pulse activates the internal clock and control logic for one conversion cycle. A constant "trial-and-decision" time period is used, except for the most significant bit which has a 50 percent longer decision time. A special output signal, "enable status," is available during the time in which the conversion is performed. With this signal an external sample-and-hold function can be switched from sample into hold mode. The aperture jitter of the enable pulse, which switches the sample-and-hold amplifier from sample into hold mode, is kept below the theoretical limit defined by the resolution and the maximum signal frequency. Then conversion starts. Because of the voltage-to-current input mode configuration, the input voltage signal is converted into a current by the resistor R_{in}. An extra offset binary current

ANALOG EXHIBIT 1002
Page 132 of 321

equal to the most significant bit value is available at the input of the converter to allow bipolar signals to be converted into offset binary output code.

All circuitry to operate the A/D converter is on chip except the input sample-and-hold amplifier, filtering capacitors to remove the ripple from the interchanging network and gain-setting resistors.

7.5.2 Comparator-subtracter circuit

As already said, a high-speed operational amplifier in the inverting mode is used for subtraction of the D/A converter output current from the analog input current. A simplified circuit diagram is shown in Figure 7.8. A wide

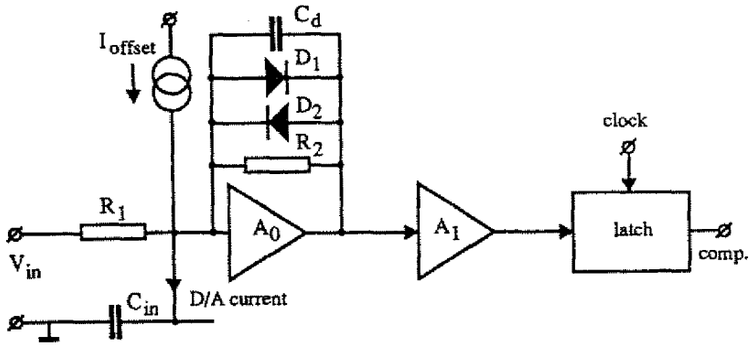


Figure 7.8 : Comparator-subtracter circuit diagram

band feed-forward coupled operational amplifier with a unity-gain-frequency-compensated bandwidth of 75 MHz is used. A high-value feedback resistor R_2 is used to have a large gain around the zero crossing of the signal. Diodes D_1 and D_2 are connected in parallel with the resistor R_2 to prevent large output voltage swings, which maybe even larger than the applied supply voltage of the converter, being generated at the output. With these diodes, the input voltage excursion remains very small, thus having no influence on the D/A converter performance and the input voltage-to-current transformation. Speed limitations in the system are due to the diode capacitance C_d across the feedback resistor R_2 and the input capacitance C_{in}. The output capacitance of the D/A converter in this case is the dominating contributor to the input capacitance C_{in}. In practice using a standard bipolar process, a value of approximately 20 pF for C_{in} is found. The comparator bandwidth

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		First Named Inventor	Rudy G. H. Eschauzier
		COMPLETE IF KNOWN	
☒ Declaration Submitted with Initial Filing OR ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16(e)) required)		Application Number	
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		Art Unit	
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Amplifiers with Input Offset Trim and Methods

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First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	55123P377

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12/390,684	02/23/2009	Rudy G. H. Eschauzier	55123P377

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CONFIRMATION NO. 5595

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FILING RECEIPT

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Date Mailed: 03/17/2009

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Applicant(s)

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Assignment For Published Patent Application

NUMBER 14 B.V., Bergschenhoek, NETHERLANDS

Power of Attorney: The patent practitioners associated with Customer Number 79124

Domestic Priority data as claimed by applicant

Foreign Applications

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/390,684**

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Title

Amplifiers with Input Offset Trim and Methods

Preliminary Class

330

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First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Customer Number:	79124
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Warnings:
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2		55123P377_20090518_App_Rplcmnt.pdf	173725 47fcefee1a95a3c40984933227599b47bb26f0c1	yes	39
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	Document Description		**Start**	**End**	
	Specification		1	31	
	Claims		32	38	
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3	Drawings-only black and white line drawings	55123P377_20090518_Figs_Rplcmnt.pdf	918291 a1d636f6f7d2bb1f854a1514e7b340328cf3c0f4	no	10
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ATTORNEY DOCKET NO.: 55123P377

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

RUDY G. H. ESCHAUZIER, ET AL.

Application No.: 12/390,684

Filed: February 23, 2009

For: **Amplifiers with Input Offset Trim and Methods**

Art Group:

Examiner:

Confirmation No.: 5595

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Sir:

In response to the Notice to File Corrected Application Papers mailed March 17, 2009, please find enclosed:

- substitute drawing(s) in compliance with 37 CFR § 1.84;
- substitute specification, applicant submits that the substitute specification contains no substantive new matter;

If any additional fee is required, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: May 18, 2009

Roger W. Blakely, Jr., Reg. No. 25,831

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

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UNITED STATES PATENT APPLICATION

FOR

AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

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55123P377

AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of operational and instrumentation amplifiers.

2. Prior Art

One of the key performance specifications of an operational amplifier is its DC error or offset voltage. The offset voltage limits the ability of the amplifier to resolve small DC input voltages. The total offset voltage is usually specified assuming a single source of error at the input terminals. The value of this imaginary voltage source represents the input referred offset voltage of the amplifier. The significance of this parameter lies in the fact that the amplifier will not be able to resolve any DC voltages at its input that are smaller than the input referred offset voltage.

In monolithically integrated operational amplifiers, the input referred offset voltage (also called input offset, offset voltage or just offset for short) is mostly due to statistical mismatch between critical components in the circuit. Commonly, these critical components include the

input stage transistors, but other devices may contribute significantly to the offset as well. Typical offset voltages due to component mismatch lay in the order of several millivolts.

A well-known technique to reduce the input referred offset voltage of an amplifier is by trimming each amplifier during manufacturing. At some stage in the production process - usually while electrically screening the parts for defects - the native offset of the part is measured, and corresponding modifications are made to the part to compensate for this offset. The modifications to the part need to be permanent, in order for the offset to remain compensated for over the life of the product.

Many techniques have been proposed and used in the past to make permanent changes to an IC in order to store the offset compensation voltage. Examples include trimming resistors with a laser, blowing links with a laser, shorting out zener diodes by a high reverse voltage, blowing metal fuses with a high current, modifying the resistivity of a poly-silicon resistor with a high current and storing digital bits onto a non-volatile memory (e.g. flash).

Based on the timing of the trimming during the production process, all trimming techniques can be classified into one of two categories:

1. pre-package trim
2. post-package trim

As the name implies, pre-package trim includes all trim techniques that take place before the silicon die is packaged into its final package. Reversely, post-package trim is done after packaging the part.

The distinction between pre and post-package trim is a critical one, since the packaging process can lead to significant offset shifts of the part. Especially plastic packages, which include the majority of all parts being shipped today, can inflict high mechanical stresses to the silicon die. The piezoelectric properties of silicon convert the mechanical stresses into offset voltage shifts of the circuit. These offset shifts in their turn cause the input referred offset voltage of the part to change randomly after packaging. Typical offset shifts due to packaging are on the order of several 100s of microvolts.

A part that was trimmed for zero offset before packaging (pre-package trim), will most likely show a non-zero offset after being assembled. Therefore, pre-package trim is not able to guarantee very high accuracies of the trimmed offset voltage.

Post-package trim, on the other hand, takes into account offset shift due to packaging and will compensate for it. Very high trim accuracies can be achieved this way.

Despite its high end-accuracy, there are two main disadvantages associated with post-package trim. The first disadvantage of post-package trim is the need for some sort of on-die non-volatile memory. Most process technologies used for fabricating operational amplifiers do not offer non-volatile memory, and if they do, bit cells tend to be not very area-efficient.

The second disadvantage is the need to offer means to externally control the trim state and store the offset compensation value. In many cases this will require the addition of pins to the package, and increase cost. Alternatively, the part can employ some sophisticated multiplex approach to reuse the existing pins for controlling the offset trim algorithm. Such setup requires complex circuitry, however, adding to the die size and cost.

An approach to post-package trim that does not require non-volatile memory and external control of the trim algorithm is so-called power-on calibration. Using this technique, the part is not trimmed during manufacturing, but instead each time the part is powered up (see "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections:

Autozeroing, Correlated Double Sampling, and Chopper Stabilization", C.C. Enz and G.C. Temes, *IEEE J. Solid-State Circuits*, vol. 84, Nov. 1996, pp. 1584-1614 and "A high-performance autozeroed CMOS opamp with 50 μV offset", Krummenacher et al., Solid-State Circuits Conference, 1997, Digest of Technical Papers, pp. 350 - 351, 483). Since the stored offset compensation value needs to be retained only while the supply power is available, power-on calibration alleviates the need for non-volatile memory. Instead, volatile memory can be used. This type of memory offers small die size, and it is ubiquitously available in any CMOS process technology in the form of flip-flops.

Figure 1 shows the block diagram of an amplifier with power-on calibration.

It uses the successive approximation algorithm to cancel out the random input referred offset voltage V_{os}. Offset calibration of amplifier A is achieved through switch S, comparator COMP, the successive approximation state-machine SAR and finally the digital-to-analog converter D/A that feeds an offset correction voltage to amplifier A. When the amplifier is powered on, switch S is closed. This forces a differential input voltage that is equal to the input referred offset voltage V_{os} at the input of amplifier A. Since there is no feedback, the amplifier A operates in the

comparator mode: if the differential input voltage is greater than zero, its output will jump to the positive rail, and vice verse (assuming the offset correction voltage at port N is zero).

Figure 2 shows a simplified representation of the amplifier circuit in Figure 1 during calibration.

While calibrating, the input switch in Figure 1 connects the offset source V_{os} between the two differential inputs of amplifier *A*. This is represented by the offset source V_{os} in Figure 2. Since the *D/A* output voltage V_{da} drives offset compensation port *N* on amplifier A_1 in Figure 1, the effect of V_{da} can be thought of as being subtracted from the offset voltage V_{os} at the input of the amplifier. This is indicated in Figure 2 by the plus sign for the voltage V_{os}, and the minus sign for the voltage V_{da}. The difference between offset voltage V_{os} and correction voltage V_{da} is error voltage ε. The sign of the error voltage ε, through amplifier *A* and comparator *COMP*, drives the decisions of the successive approximation algorithm.

After power-up the circuit will start its successive approximation state-machine to find a value for the offset correction voltage V_{da} at the secondary input *N* that minimizes

the input referred offset voltage of the overall circuit. The successive approximation operates as follows (see Analog-To-Digital and Digital-To-Analog Converters, R.J. van de Plassche, Springer, 1994). The circuit starts off with all bits to the digital-to-analog converter *D/A* set to zero. This causes the most negative voltage V_{da} to be set on the offset compensation input *N*. If the offset compensation range is large enough, this negative voltage will always cause the output of amplifier *A* to trip high ($\varepsilon>0$). In the next cycle, the most significant bit (MSB or b_n) of *D/A* will be tested high. If this causes the output of *A* to go low ($\varepsilon<0$), the bit will be returned to its low state before proceeding to the next bit. Otherwise, if the output of *A* does not change due to setting the MSB ($\varepsilon>0$), the bit will remain high. The state of the MSB will be stored into a register and does not change during the remainder of the calibration process. In the following step, the bit below the MSB (b_{n-1}) will be tested high and the resulting bit value stored into the register. This process continues successively through all bits, high to low, until the least significant bit is tested and its value stored.

Table 1 shows an example of the offset calibration procedure for a 3-bits SAR register in the simple case that the offset voltage V_{os} is zero.

Step	b_3 (±1V)	b_2 (±0.5V)	b_1 (±0.25V)	V_{da} [V]	ε [V] (V_{os}-V_{da})	Comment
0	0	0	0	-1.75	+1.75	Initial State
1	1	0	0	+0.25	-0.25	ε <0, b_2=0
2	0	1	0	-0.75	+0.75	ε >0, b_1=1
3	0	1	1	-0.25	+0.25	ε >0, b_0=1
4	0	1	1	-0.25	+0.25	Final State

Table 1. Example of the successive approximation algorithm, assuming Vos=0

The table assumes that the *MSB* b_3 switches between the values −1V (bit low) and +1V (bit high). The other bits are binary weighted, such that b_2=±0.5V and b_1=±0.25V. Bits tested by the algorithm are underlined. The error value ε in the example of Table 1 approaches zero within the step size of one *LSB* (0.5V). The resulting binary code is (011) (see the bottom row).

Table 2 gives a similar example of the successive approximation algorithm, now assuming that the input offset voltage Vos is 1.6V. In this case the bits converge to the code (110), with a remaining error ε of 0.35V, which is again within one LSB step size.

Step	b_3 (±1V)	b_2 (±0.5V)	b_1 (±0.25V)	V_{da} [V]	ε [V] (V_{os}-V_{da})	Comment
0	0	0	0	-1.75	+3.35	Initial State
1	1	0	0	+0.25	+1.35	ε >0, b_2=1
2	1	1	0	+1.25	+0.35	ε >0, b_1=1
3	1	1	1	+1.75	-0.15	ε <0, b_0=0
4	1	1	0	+1.25	+0.35	Final State

Table 2. Example of the successive approximation algorithm, assuming Vos=1.6

Notice how in the examples in Table 1 and Table 2 the remaining output error **ε** is always greater than zero. This is a property of the successive approximation algorithm: if a particular bit is tested high and the error voltage **ε** becomes smaller than zero, the bit is reset to zero. As a result, the algorithm does not allow the error **ε** to become negative.

In fact, the distribution of the error **ε** is between zero and one LSB step size S_{lsb}. Ideally, we would like to see the error centered around zero. Doing so will half the maximum error **ε** from +1 S_{lsb} to ±½ S_{lsb}. In order to perform the re-centering, we will need to add a value equal to ½ S_{lsb} to the *D/A* converter voltage V_{da} after the calibration completes. The shift of the final *D/A* converter voltage V_{da} can be achieved by adding one more bit to the *D/A* converter, below the least significant bit b_1 (LSB). This additional bit is held at zero during the calibration process, and subsequently set to one, once the calibration is done. Table 3 illustrates the addition of a shift bit to the algorithm.

Step	b_3 (±1V)	b_2 (±0.5V)	b_1 (±0.25V)	$\boldsymbol{b_s}$ **(±0.125V)**	V_{da} [V]	ε [V] (V_{os}-V_{da})	Comment
0	0	0	0	**0**	-1.875	+3.475	Initial State
1	1	0	0	**0**	+0.125	+1.475	ε >0, b_2=1
2	1	1	0	**0**	+1.125	+0.475	ε >0, b_1=1
3	1	1	1	**0**	+1.625	-0.025	ε <0, b_0=0
4	1	1	0	**1**	+1.375	+0.225	Final State

Table 3. Example of the successive approximation algorithm with a shift bit, assuming Vos=1.6

In this example, the error ε in the final state is 0.225V (bottom row), which is less than half an LSB step size (0.25V).

Even though the successive approximation algorithm is very powerful in calibrating out the offset of an amplifier at power-up, it suffers from a major drawback. In order for the algorithm to be able to guarantee a certain end-accuracy of the calibration, matching of the various components in the D/A converter needs to be extremely tight. Especially matching of the MSB step size S_{msb} to the other bits turns out to be critical. The matching error of the MSB step size S_{msb} must be significantly less than one LSB step size S_{lsb} in order for the mismatch not to affect the overall accuracy appreciably:

$$\Delta S_{msb} << S_{lsb} \qquad (1)$$

This can be rewritten as

$$\frac{\Delta S_{msb}}{S_{msb}} << \frac{S_{lsb}}{S_{msb}} = \frac{1}{2^{n-1}} \qquad (2)$$

where n equals the number of bits of the D/A converter.

Accepting a maximum error due to mismatch of the MSB equal to half an LSB step size ½ S_{lsb}, the expression for the maximum matching error of the MSB simplifies to

$$\frac{\Delta S_{msb}}{S_{msb}} \leq 2^{-n} \qquad (3)$$

Similar constraints as for the MSB on the maximum matching error occur for the other bits of the A/D converter, albeit with progressively looser matching requirements. The step size of the bits becomes smaller by a factor two for each step when going from the MSB to the LSB. Therefore the expression for the maximum matching error of individual bits becomes

$$\frac{\Delta S_b}{S_b} \leq 2^{-b} \qquad (4)$$

where b equals the bit number ($b=n$ for the MSB, $b=1$ for the LSB).

Clearly, matching of the MSB will be the most critical.

To illustrate the effect of mismatch on the transfer function of the D/A converter, Figure 3 shows an example of the output voltage vs. input code of a 3-bit converter without any mismatch error.

The output steps through all eight possible output values with even step sizes as the input code progresses from (000) through (111). The ideal D/A converter of Figure 3 can generate any voltage needed to compensate for the offset of the overall amplifier within half an LSB step size (½ S_{lsb}).

Figure 4 shows the transfer function of the same D/A converter, now assuming a mismatch error that causes the MSB step size to be too large.

Note how the output voltage jumps when the input code goes from (011) to (100). This is because during this transition, the MSB is switched on. Turning on the MSB is supposed to almost make up for all other bits switching off, leaving a positive difference of 1 LSB step size S_{lsb} between the output levels for codes (011) and (100). Since in this example the MSB step size S_{msb} is too large, the MSB over-compensates for the other bits switching off, causing the difference between the two levels to be too large. This creates a gap between the output voltage levels for input codes (011) and (100).

The hatched area is a range of output voltages that is not covered by the D/A converter. If the voltage V_{da} that is needed to compensate for the offset of the overall amplifier falls somewhere in the middle of the hatched voltage range, the offset voltage most likely cannot be corrected for within half an LSB step size, or ½ S_{lsb}.

When matching errors cause the MSB step size S_{msb} to be too small, we obtain a D/A response similar to Figure 5. The

transfer function is not monotonic anymore and has a slightly reduced dynamic range compared to the ideal case of Figure 3.

Despite these two factors, all output voltages within the dynamic range of the converter can now be produced within half an LSB step size (½ S_{lsb}). In other words, despite the MSB mismatch error, we can continue to guarantee that any offset voltage of the overall amplifier can be compensated for within ½ S_{lsb}. Note that monotonicity of the D/A transfer function is not required for the successive approximation algorithm to function properly.

Summarizing the effects of MSB mismatch on the successive approximation algorithm, we find the following:

1. A mismatch error that causes the MSB to be too *large* will deteriorate the worst-case offset voltage of the overall amplifier after calibration.

2. A mismatch error that causes the MSB to be too *small* does not significantly affect the overall accuracy of the offset calibration.

Figure 6 illustrates this conclusion.

On the x-axis, it shows the ratio between the value of the MSB b_n and the next bit b_{n-1} (bit ratio ρ), while the y-axis represents the probability of a certain bit ratio ρ.

Ideally, the bit ratio ρ is 2 (MSB b_n twice as large as the next bit b_{n-1}). Due to mismatch between the components used to manufacture the circuit, the actual bit ratio ρ will vary around the mean value of 2 with a normal distribution having standard deviation σ_ρ. In order to make sure that the overall error due to component mismatches does not exceed half an LSB step size (½ S_{lsb}), the bit ratio ρ should not be too large.

The relation between the error $\Delta\rho$ of the bit ratio ρ and the mismatch $\Delta S_n/S_n$ of the MSB step size can be found as follows

$$\begin{aligned} &S_n = 2 \cdot S_{n-1} \\ &S_n + \Delta S_n = (2 + \Delta\rho) \cdot S_{n-1} \Rightarrow \\ &\frac{\Delta S_n}{S_n} = \frac{\Delta\rho \cdot S_{n-1}}{S_n} = \frac{\Delta\rho}{2} \end{aligned} \qquad (5)$$

Using Eq. 3 and Eq. 5, we can now find for the maximum allowed error $\Delta\rho_{max}$

$$\Delta\rho_{max} = 2 \cdot 2^{-n} \qquad (6)$$

From Eq. 6 we can find the expression for the maximum acceptable absolute value of the bit ratio ρ_{max}

$$\rho_{max} = \bar{\rho} + \Delta\rho_{max} = 2 + 2^{1-n} \qquad (7)$$

where $\bar{\rho}$ is the *mean* or targeted bit ratio

The hatched area in Figure 6 indicates the forbidden range of bit ratios ρ. Values of the bit ratio ρ that lie above $2+2^{1-n}$, indicated by the dashed line, lead to the calibration of the overall circuit potentially being out of spec (point 1 above), whereas any value of the bit ratio ρ below this limit guarantees a calibrated offset within the specifications (see point 2 above).

Based on Eq. 7, we can determine the maximum matching error of the bit ratio

$$\frac{\Delta\rho_{max}}{\overline{\rho}} = 2^{-n} \qquad (8)$$

Note how the maximum acceptable matching error $\Delta\rho_{max}/\overline{\rho}$ goes down exponentially with the number of bits. Especially with high bit counts, this can result in very tight matching requirements.

Considering n=10 bits as an example, the maximum allowable mismatch error of the bit ratio $\Delta\rho_{max}/\overline{\rho}$ equals 2^{-10}, or about 0.1% (Eq. 8). Requiring this to be a 6σ limit (probability of exceeding the spec limit smaller than ~1 ppb, assuming a normal distribution), means the standard deviation of the MSB bit ratio matching σ_ρ must be smaller than 0.016%.

ANALOG EXHIBIT 1002
Page 163 of 321

The matching requirements that follow from Eq. 8 are often very hard - if not impossible - to achieve in practical monolithically integrated circuits. Therefore, current state-of the art amplifiers with power-on calibration rely heavily on production screening of all possible D/A output levels to guarantee that the input referred offset will be within specs across wide ranges of operating conditions. Due to the large number of possible output levels (1024 for n=10), this production screening is both time-consuming and costly.

ANALOG EXHIBIT 1002
Page 164 of 321

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art amplifier with power-on calibration.

Figure 2 shows a prior art power-on calibrated amplifier in calibration mode.

Figure 3 shows an ideal 3-bit D/A transfer function.

Figure 4 shows a 3-bit D/A converter transfer curve: MSB too large.

Figure 5 shows a 3-bit D/A converter transfer curve: MSB too small.

Figure 6 shows the probability-density function of the bit ratio ρ of a SA D/A converter.

Figure 7 shows the probability-density function of the bit ratio ρ for the proposed calibration circuit.

Figure 8 shows a preferred embodiment of power-on calibration using a non-binary weighted D/A converter.

Figure 9 is a simplified example of the circuit implementation of the proposed invention.

Figure 10 shows an example of the circuit implementation of the non-binary weighted A/D converter.

ANALOG EXHIBIT 1002
Page 165 of 321

Figure 11 shows an example of an instrumentation amplifier with power-on calibration.

Figure 12 presents an exemplary configuration to trim at production, while storing the results in one-time programmable memory.

Figure 13 shows the addition of an auxiliary amplifier to control the output during calibration.

ANALOG EXHIBIT 1002
Page 166 of 321

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Traditional successive approximation approaches to power-on calibration lead to excessively tight matching specifications of the D/A converter components. The present invention proposes a method to relax the matching requirements. Allowing for more variation will greatly improve the manufacturability of power-on calibration circuits.

The key to improving the robustness of the power-on calibration lays in the use of a targeted bit ratio $\overline{\rho}$ that is smaller than the traditional $\overline{\rho}=2$. Note from Figure 6 and Eq. 7 that any ratio ρ below $2+2^{1-n}$ (with a practical under limit of $\rho=1$) guarantees the accuracy of the calibration. By choosing a target bit ratio $\overline{\rho}$ less than 2, meeting the limit set by Eq. 7 becomes progressively easier.

This is illustrated by Figure 7.

This plot again shows the probability density function of the bit ratio ρ between the MSB b_n and the adjacent bit b_{n-1}, assuming a normal distribution. The maximally allowable ratio ρ that guarantees proper calibration of the amplifier's offset is indicated by the dashed line at $\rho_{max}=2+2^{1-n}$. The hatched area indicates "forbidden" values for the ratio ρ.

ANALOG EXHIBIT 1002
Page 167 of 321

The main difference between the prior-art plot in Figure 6 and the plot of Figure 7 is that the bit ratio is now centered around a value that is slightly smaller than the traditional value of 2. Figure 7 uses a mean bit ratio of $\overline{\rho} = 1.9$ as an example.

A consequence of choosing a smaller mean bit ratio is that the peak of the probability density function moves away from the upper limit. A greater distance between the peak and the upper limit suggests it will be easier to meet the spec in production. This can be quantified as follows. The difference between the mean of the bit ratio $\overline{\rho}$ and the spec limit ρ_{max} is given by

$$\rho_{\max} - \overline{\rho} = 2 + 2^{1-n} - \overline{\rho} \tag{9}$$

Since the number of bits $n >> 1$ in most practical cases, this reduces to

$$\rho_{\max} - \overline{\rho} \approx 2 - \overline{\rho} \tag{10}$$

The matching requirement for the bit ratio ρ now becomes

$$\frac{\Delta\rho_{\max}}{\overline{\rho}} \approx \frac{2-\overline{\rho}}{\overline{\rho}} \approx \frac{2-\overline{\rho}}{2} \tag{11}$$

The right hand side of Eq. 11 assumes the target bit ratio $\overline{\rho}$ is close to 2.

Note that the matching requirement that follows from Eq. 11 is *independent* of the total number of bits. In the prior-art case of $\overline{\rho}=2$ (binary weighted), the matching spec became exponentially tighter with a rising number of bits (Eq. 8).

By substituting our example of $\overline{\rho}=1.9$ into Eq. 11, we find the maximum allowable mismatch of the bit ratio as 5%. Again requiring a 6σ limit, this leads to a maximum standard deviation of the mismatch of the MSB bit ratio σ_ρ equal to 0.8%. This is much looser than the 0.016% of the binary weighted prior art example. In fact, matching ratios on the order of 0.8% can routinely be realized in standard manufacturing processes without the need for additional trimming or production testing.

Figure 8 shows the preferred embodiment of the proposed invention.

It consists of amplifier input stage A_1, and the two selectable output stages A_{2a} and A_{2b}. Power-on offset calibration is performed through the comparator *COMP*, the successive approximation register *SAR* and a non-binary weighted D/A converter. The D/A converter comprises the switches b_n through b_s, and the non-binary weighted bit values 1 through $1/1.9^{n-2}$, plus binary weighted values for the least

ANALOG EXHIBIT 1002
Page 169 of 321

significant bit controlled by switch b_1 and the shift bit b_s. At power up of the circuit, the input switch S_1 shorts out the inputs to the amplifier input stage A_1. As a result, the input referred offset voltage V_{os} will be present between its differential input terminals. Output switch S_2 connects the input stage A_1 to the secondary output stage A_{2b}. Because of its connection to the secondary output stage A_{2b}, the comparator *COMP* can now drive the decisions of the successive approximation algorithm implemented by the register *SAR*. The least significant bit is given a binary weighting because of the fact that any error in that weighting does not cause an error that must be made up by subsequent bits, and the shift bit is given a binary weighting relative to the least significant bit as its purpose is to compensate for one half the least significant bit to cause the error ε to be centered around zero instead of always being on one side of zero, thereby cutting the maximum error in half.

Once the power-on offset calibration completes, switch S_1 connects the input terminals of the overall amplifier to the input stage A_1, while switch S_2 activates output stage A_{2a}. Also, the SAR register activates the shift bit b_s. Note that the ratio between the LSB b_1 and the shift bit b_s remains two, even if all other bits are non-binary weighted. The

amplifier is now in its normal mode of operation, with the register *SAR* holding a digital code that corresponds to a voltage V_{da} that (mostly) compensates for the input referred offset V_{os}.

Even though the use of the two selectable output stages A_{2a} and A_{2b}, along with output switch S_2 is not necessarily required for the invention to work properly, this setup has several key advantages over using a single output stage for both calibration and normal mode. First of all, selecting between the two output stages will prevent spurious signals or glitches to appear at the output terminal of the amplifier while the amplifier is being calibrated. A second benefit of duplicating the output stage is that the secondary output stage A_{2b} can now be implemented without the addition of a compensation capacitor for closed loop stability. Frequency compensation capacitor C_m is required during normal operation to ensure stability of the amplifier with overall feedback. Since the amplifier is operated in an open-loop comparator mode during power-on calibration, no frequency compensation is needed. Leaving out the compensation capacitor speeds up the decisions during the successive approximation procedure, reducing the total time spent in calibration mode.

ANALOG EXHIBIT 1002
Page 171 of 321

As an alternative to a power-up event, the calibration sequence can also be initiated by any other trigger. In that case, the system performs on-demand-calibration as opposed to power-on calibration as described before.

Figure 9 shows a simplified example of a circuit implementation of the present invention.

It consists of the transconductance input stage with transistors M_1 and M_2. The gates of these devices are connected to switches $S_{1,1}$ and $S_{1,2}$. In normal mode, the switches directly connect the gates of M_1 and M_2 to the input terminals *IN+* and *IN-*. During calibration, the inputs are shorted out and connected to the reference common-mode voltage V_1. Devices M_5 through M_8 implement a traditional folded cascode turn-around stage. The first or primary output stage used for normal operation comprises the devices M_{11} and M_{12}, together with frequency compensation capacitors C_{M1} and C_{M2}. The secondary output stage used during calibration includes devices M_9 and M_{10}. This secondary output stage does not require any frequency compensation components, since it will only be used in comparator mode. Switches $S_{2,1}$ and $S_{2,2}$ select between the two output stages. The block *AB* implements class-AB quiescent current control of the output stage devices (either M_{11} and M_{12}, or M_9 and M_{10},

ANALOG EXHIBIT 1002
Page 172 of 321

depending on the states of $S_{2,1}$ and $S_{2,2}$). When the primary output state M11 and M12 is selected, switches $S_{2,3}$ and $S_{2,5}$ are closed, putting the secondary output stage in a high output impedance state, and when the secondary output state M9 and M10 is selected, switches $S_{2,4}$ and $S_{2,6}$ are closed, putting the primary output stage in a high output impedance state.

The parallel input stage M_3/M_4 implements the offset control input. A differential voltage between the gates of M_3 and M_4 will cause a differential output current at their drains. This differential drain current flows in parallel to the drain current of the input stage M_1/M_2. A suitable differential voltage at the gates of M_3 and M_4 can compensate for a random offset of the input stage M_1/M_2. Since the range of offset voltages that the parallel input stage needs to compensate for is much smaller than the expected signal swing at the input of the amplifier, the tail current I_2 through devices M_3 and M_4 can be chosen smaller than the bias current of the input stage I_1.

The register *SAR* and the non-binary weighted D/A converter *D/A* implement the successive approximation algorithm as before.

Figure 10 shows an example of a 6-bit implementation of the non-binary weighted D/A converter.

It consists of a three-section differential resistive ladder with resistor values R, R_1 and R_2. The common-mode voltage of the ladder is set by voltage source V_{cm}. Note that this voltage is not related to any common mode voltage of an input signal IN+,IN-, as the transistors M3 and M4 operate in a differential mode to control the division of the current I2 (Figure 9), independent of the operation of the differential input stage transistors M1 and M2. The switches b_s through b_6 steer the currents from the bottom current sources to either side of the differential ladder, depending on the states of the input bits. In this example, the weighting of the bits b_2 through b_4 is done through the resistive ladder, while weighting of b_s, b_1 and b_6 is implemented through scaling of the respective current sources. This choice is arbitrary, and not critical to the operation of the circuit.

Targeting a bit ratio of $\overline{\rho}$, the values of the resistors can be found as follows

$$\begin{aligned} R_1 &= R \cdot (\overline{\rho} - 1) \\ R_2 &= R \cdot \frac{\overline{\rho}}{\overline{\rho} - 1} \end{aligned} \qquad (12)$$

where R is the characteristic impedance of the ladder.

Note how choosing a bit ratio $\overline{\rho}=2$ (standard binary weighing) transforms the D/A converter of Figure 10 into a traditional R-2R ladder (R_1=R, R_2=$2R$).

By adding an additional input stage to the circuit of Figure 9, it can easily be transformed into a so-called instrumentation amplifier (see Operational Amplifiers, Theory and Design, J. Huijsing, pp. 52-53, Boston, Kluwer Academic Publishers, 2001). Instrumentation amplifiers have two sets of differential input terminals and are capable of sensing small differential signals in the presence of a large common-mode disturbance.

In order for the power-on calibration to work properly in the modified circuit, only the input stage devices and the input switches need to be repeated from the original amplifier. The offset calibration can be performed across both input stages combined and therefore does not require any other additional components.

Figure 11 shows the instrumentation amplifier that results from modifying the circuit depicted in Figure 9. The components added to the circuit are the two input stage with M_{13} and M_{14}, along with the corresponding input switches $S_{1,3}$ and $S_{1,4}$, which would be operated simultaneously with $S_{1,1}$ and $S_{1,2}$.

The embodiments shown herein in Figures 9 and 11 are MOS embodiments, though other active devices may be used, such as bipolar devices. Also the word switch as used herein and in the claims is used in the general sense, and includes single or multiple switches, as appropriate. When the word switch is used in the context of multiple switches, such multiple switches would be operated substantially simultaneously, though perhaps with a preferred nonoverlapping phasing. By way of example, a switch for switching an input of the amplifier from the amplifier system input to shorting the amplifier input might be a single switch such as switch S in Figure 1 or two switches $S_{1,1}$ and $S_{1,2}$ in Figure 9, or, by way of another example, might be four switches, two for disconnecting the differential input stage from the differential amplifier input, and two to short the input to the differential input stage. In this latter case, one normally would prefer to disconnect the differential amplifier input before shorting the differential input stage, thereby defining a nonoverlapping operation.

Similarly, a reference to an input or an output herein and in the claims is a reference to an input or an output generally, independent of whether the input or output is a single signal relative to a circuit ground, or a differential signal.

ANALOG EXHIBIT 1002
Page 176 of 321

The approach of Figure 8 can be extended to perform one-time calibration during the fabrication of the device. In that case, the circuit requires some form of One-Time-Programmable memory, or OTP, to store the result of the calibration during the life-time of the product. Figure 12 shows an example.

When the device is powered up for the first time, the circuit will go through its auto-calibration cycle. Once the cycle completes, the resulting values for the bits b_n through b_s will be stored onto the non-volatile memory OTP. On subsequent power-up events, the stored offset compensation bits will be read from the OTP memory, and used to control the bit switches b_n through b_s. One additional OTP cell OTP_{n+1} is needed to establish the fact that the part has been programmed. This will avoid future attempts at calibrating the offset when the part is powered up in its application.

During auto-calibration, the overall amplifier in Figure 8 is non-responsive to external signals. This is caused by switches S_1 and S_2 that disconnect the amplifier from the external circuitry. Since the auto-calibration time can be short, disabling the amplifier will not cause issues in many, if not most, applications. In the situations where a controlled output voltage is needed, even during the auto-

calibration sequence, the circuit of Figure 13 brings a solution.

The circuit of Figure 13 adds an auxiliary amplifier A_{aux} to the base circuit of Figure 8, along with the switches S_3 through S_5. When the part is auto-calibrating, the switches S_3 through S_5 are closed, and the auxiliary amplifier A_{aux} and the output stage A_{2a} create a signal path from the input terminals V_{in} to the output V_{out}. Since the calibration time is short, so the auxiliary amplifier will not have enough time to settle to a very high accuracy anyhow, offset and other demands on the auxiliary amplifier can be relaxed compared to the main circuit. As a result, a very simple circuit suffices in most practical cases.

Thus while certain preferred embodiments of the present invention have been disclosed and described herein for purposes of illustration and not for purposes of limitation, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

CLAIMS

What is claimed is:

1. An amplifier system having an amplifier system input and an amplifier system output comprising:

a first amplifier;

a comparator;

a successive approximation register having an input coupled to an output of the comparator;

a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;

an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

2. The amplifier system of claim 1 wherein the radix is approximately 1.9.

ANALOG EXHIBIT 1002
Page 179 of 321

3. The amplifier system of claim 2 wherein the radix for the least significant bit is 2.

4. The amplifier system of claim 1 wherein the D/A converter further comprises one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits.

5. The amplifier system of claim 1 wherein the first amplifier has a first transconductance differential input stage coupled to the first amplifier input, and wherein the first amplifier is further comprised a second transconductance differential input stage, the outputs of the first and second transconductance differential input stages being coupled in parallel, the output of the D/A converter being coupled to inputs of the second transconductance differential input stage to divide a current source coupled to the second transconductance differential input stage between the differential outputs of the first transconductance differential input stage in a proportion to reduce the input offset of the first amplifier.

6. The amplifier system of claim 5 wherein the first amplifier further comprises an intermediate stage having an input coupled to the parallel connected outputs of the first

and second transconductance differential input stages, a first output stage providing the first amplifier output, a second output stage forming the comparator, the second switch for switching an output of the intermediate stage between inputs to the first and second output stages.

7. The amplifier system of claim 6 wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage, and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

8. The amplifier system of claim 6 wherein the first amplifier is further comprised of a third transconductance differential input stage, the outputs of the first, second and third transconductance differential input stages being coupled in parallel, the first switch for shorting the first amplifier input by shorting the differential input to the first transconductance differential input stage and shorting the differential input to the third transconductance differential input stage at the same time.

9. The amplifier system of claim 1 further comprised of One-Time-Programmable memory for permanently storing an

output of the successive approximation register, whereby a single output of the D/A converter controlling the input offset of the first amplifier may be permanently maintained.

10. The amplifier system of claim 1 further comprised of a second amplifier, the first switch coupling the amplifier system input to an input of the second amplifier when shorting the input to the first amplifier, the second switch coupling an output of the second amplifier to the amplifier system output when switching the output of the first amplifier from the amplifier system output to an input of the comparator.

11. The amplifier system of claim 1 wherein the D/A converter comprises a common reference line, and at least in part, resistor ladders symmetrical about the common reference line, and third switches for selectively switching equal current sources to ladder nodes on either side of the common reference line responsive to the successive approximation register, the resistor ladders being $R(\rho-1)$,$R\rho/(\rho-1)$ ladders, where ρ is less than 2.

12. The amplifier system of claim 11 wherein ρ is approximately 1.9.

ANALOG EXHIBIT 1002
Page 182 of 321

13. An amplifier system having an amplifier system input and an amplifier system output comprising:

an amplifier having a first transconductance differential input stage coupled to the amplifier input, and a second transconductance differential input stage, the outputs of the first and second transconductance differential input stages being coupled in parallel, the amplifier further having an intermediate stage having an input coupled to the parallel connected outputs of the first and second transconductance differential input stages, a first output stage providing the amplifier output, a second output stage forming the comparator;

a successive approximation register having an input coupled to an output of the second transconductance differential input stage;

a first switch for switching an input of the first transconductance differential input stage from the amplifier system input to shorting the input of the first transconductance differential input stage;

a second switch for switching an output of the intermediate stage between inputs to the first and second output stages;

an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

an output of the D/A converter being coupled to the second transconductance differential input stage to control the input offset of the amplifier.

14. The amplifier system of claim 13 wherein the radix is approximately 1.9.

15. The amplifier system of claim 13 wherein the radix for the least significant bit is 2.

16. The amplifier system of claim 13 wherein the D/A converter further comprises one additional bit providing an input offset control of the amplifier of one half that of the least significant bit of the N bits.

17. The amplifier system of claim 13 wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage, and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

18. The amplifier system of claim 13 wherein the amplifier is further comprised of a third transconductance

differential input stage, the outputs of the first, second and third transconductance differential input stages being coupled in parallel, the first switch for shorting the amplifier input by shorting the differential input to the first transconductance differential input stage and shorting the differential input to the third transconductance differential input stage at the same time.

19. The amplifier system of claim 13 wherein the D/A converter comprises a common reference line, and at least in part, resistor ladders symmetrical about the common reference line, and third switches for selectively switching equal current sources to ladder nodes on either side of the common reference line responsive to the successive approximation register, the resistor ladders being $R(\rho-1)$,$R\rho/(\rho-1)$ ladders, where ρ is less than 2.

20. The amplifier system of claim 19 wherein ρ is approximately 1.9.

ANALOG EXHIBIT 1002
Page 185 of 321

ABSTRACT

Amplifiers with power-on trim and methods using an amplifier system having an amplifier system input and an amplifier system output, an amplifier, a comparator, a successive approximation register having an input coupled to an output of the comparator, a first switch for switching an input of the amplifier from the amplifier system input to shorting the amplifier input, a second switch for switching an output of the amplifier from the amplifier system output to an input of the comparator, an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter, the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits, and an output of the D/A converter being coupled to the amplifier to control the input offset of the amplifier. Novel embodiments for the amplifier, comparator and D/A converter are disclosed.

ANALOG EXHIBIT 1002
Page 186 of 321

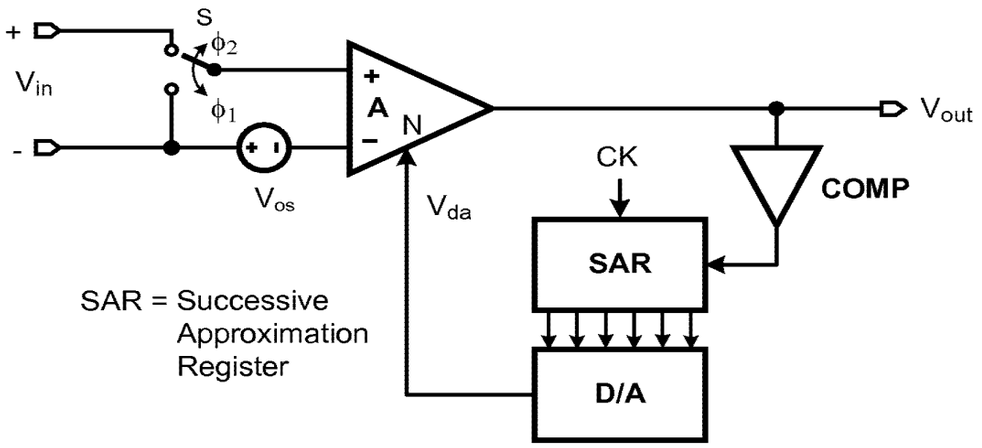


Fig. 1 (Prior Art)

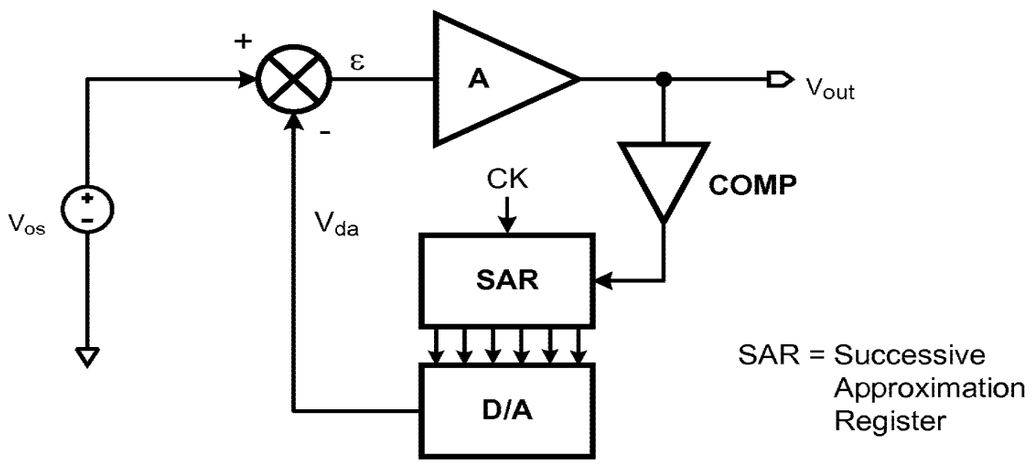


Fig. 2 (Prior Art)

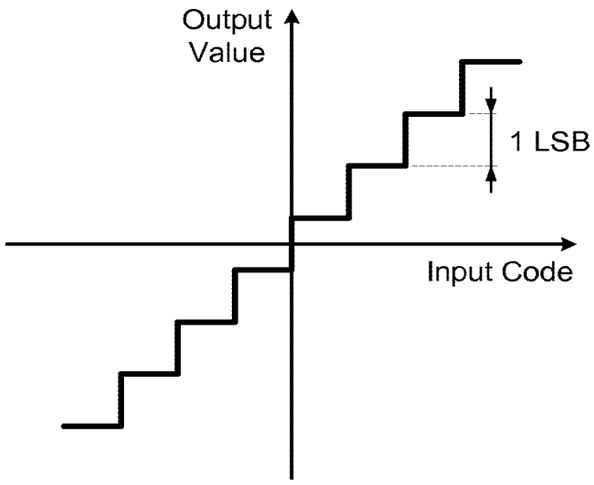

Output
Value
1 LSB
Input Code

Fig. 3

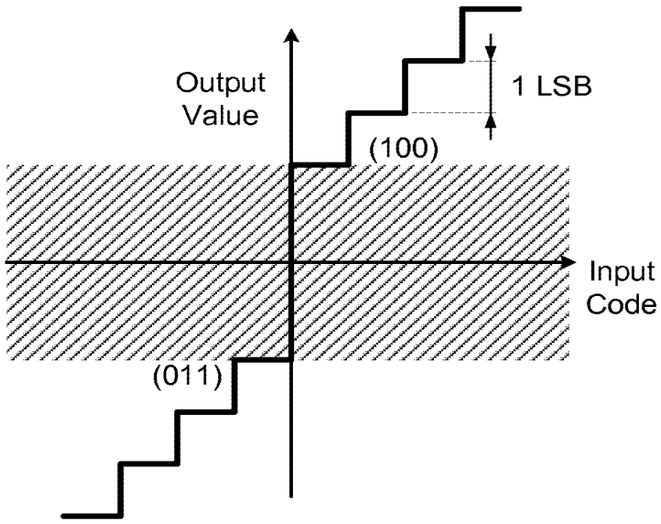

Output
Value
1 LSB
(100)
Input
Code
(011)

Fig. 4

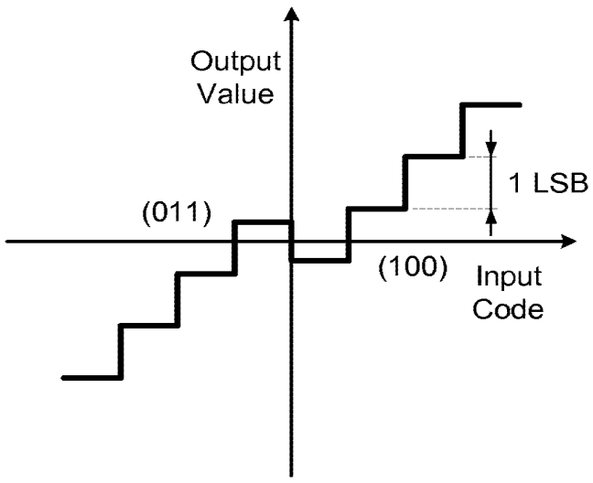

Output
Value
1 LSB
(011)
(100)
Input
Code

Fig. 5

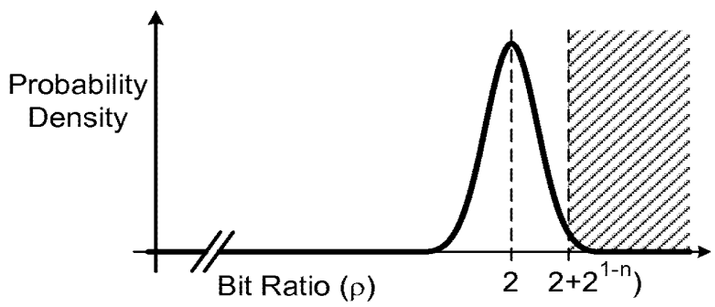

Probability
Density
Bit Ratio (ρ)
2
2+2^1-n)

Fig. 6

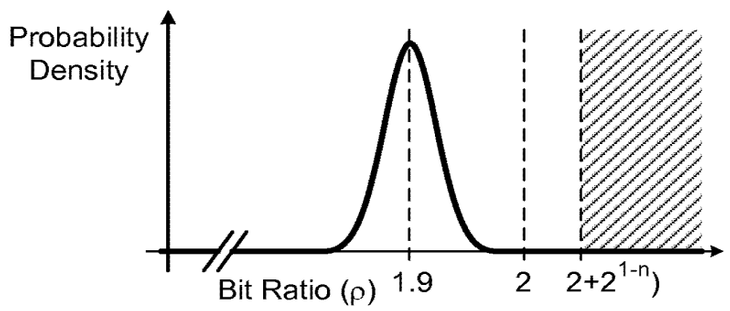


Fig. 7

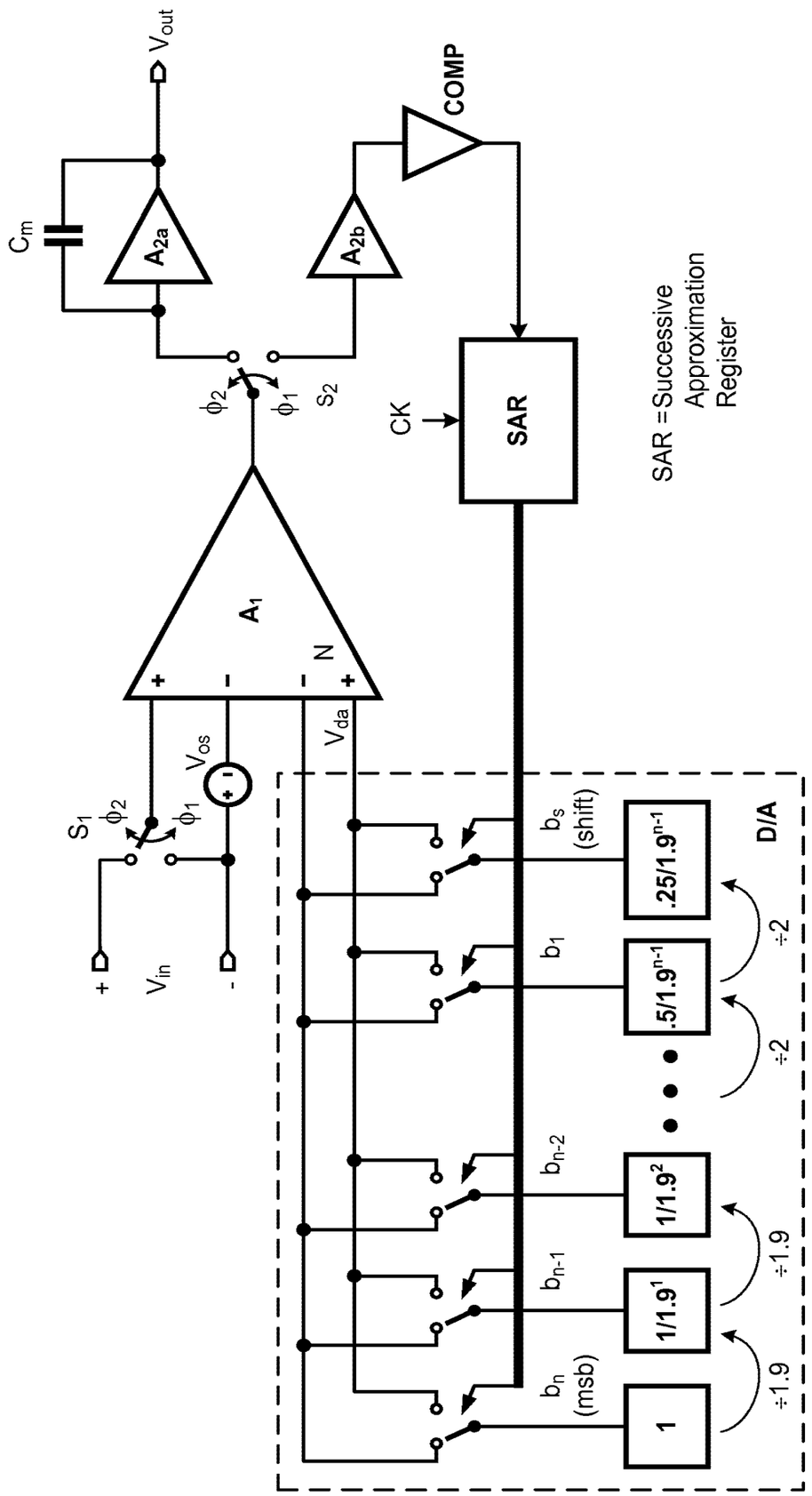

V_{out}
C_m
A_{2a}
A_{2b}
COMP
ϕ_2
ϕ_1
S_2
CK
SAR
SAR =Successive Approximation Register
A_1
N
V_{os}
V_{da}
S_1
V_{in}
b_s (shift)
b_1
b_{n-2}
b_{n-1}
b_n (msb)
$.25/1.9^{n-1}$
$.5/1.9^{n-1}$
$1/1.9^2$
$1/1.9^1$
1
÷2
÷1.9
D/A

Fig. 8

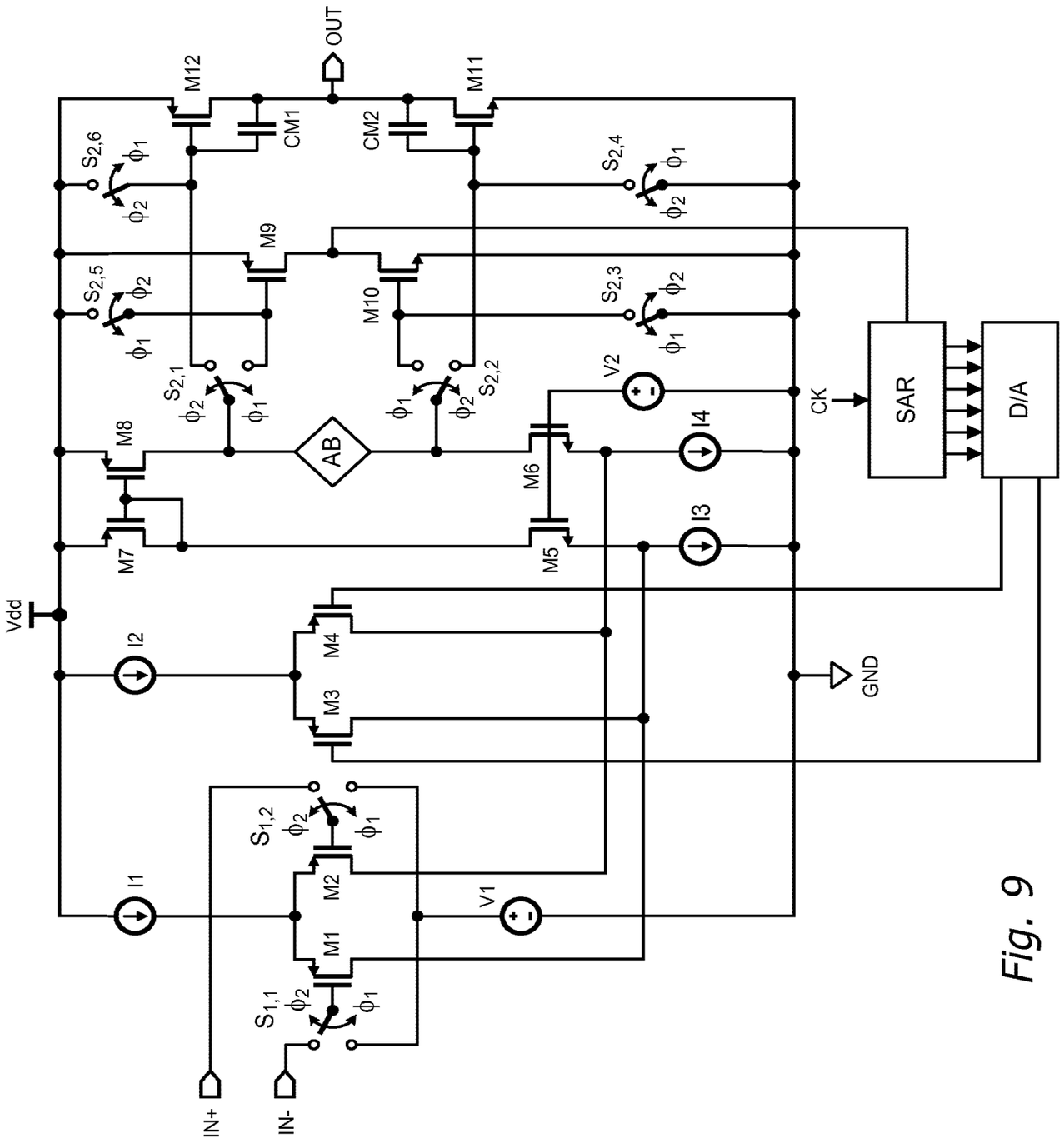

OUT
M12
M11
CM1
CM2
S2,6
S2,4
S2,5
S2,3
S2,1
S2,2
M9
M10
M8
M7
M6
M5
AB
V2
I4
I3
CK
SAR
D/A
Vdd
I2
M4
M3
GND
S1,2
S1,1
M2
M1
I1
V1
IN+
IN-

Fig. 9

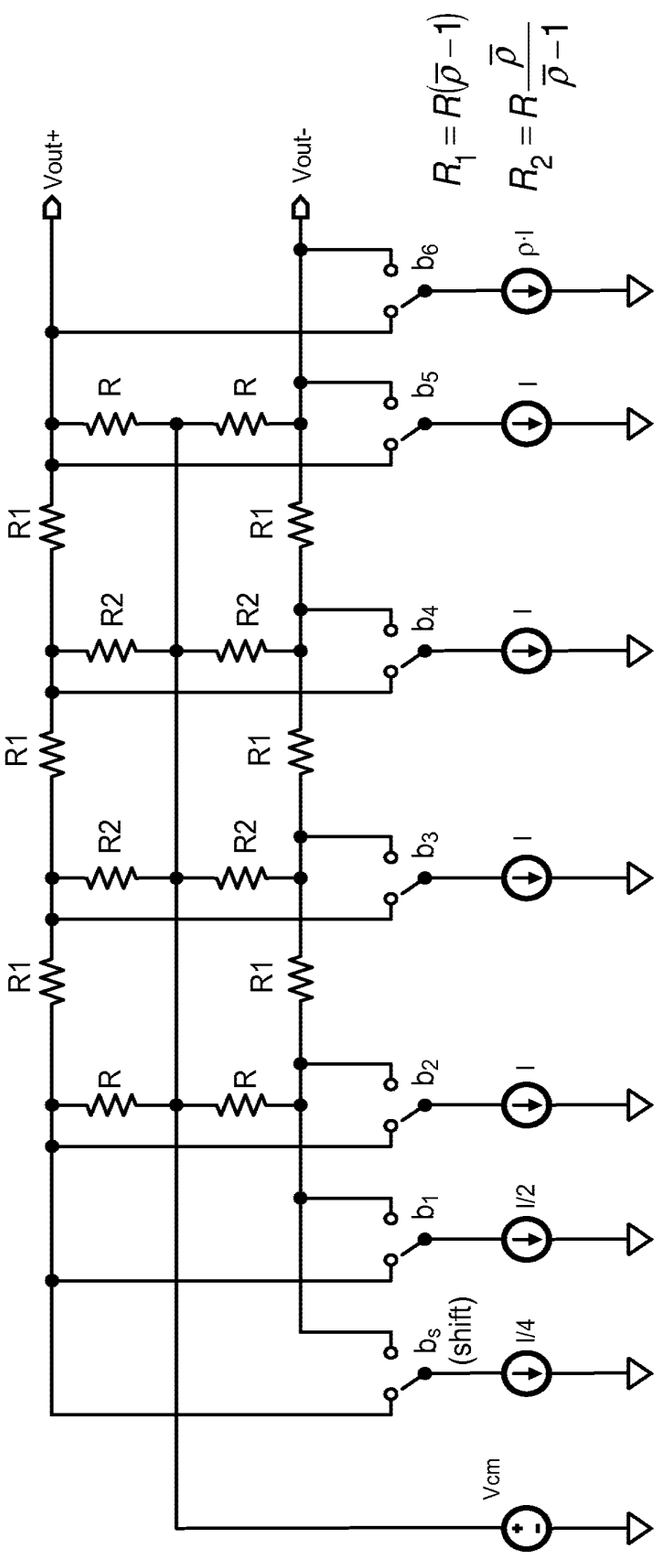

Vout+
Vout-
$R_1 = R(\bar{\rho} - 1)$
$R_2 = R\frac{\bar{\rho}}{\bar{\rho} - 1}$
R
R1
R2
b_6
b_5
b_4
b_3
b_2
b_1
b_s (shift)
ρ·I
I
I/2
I/4
Vcm

Fig. 10

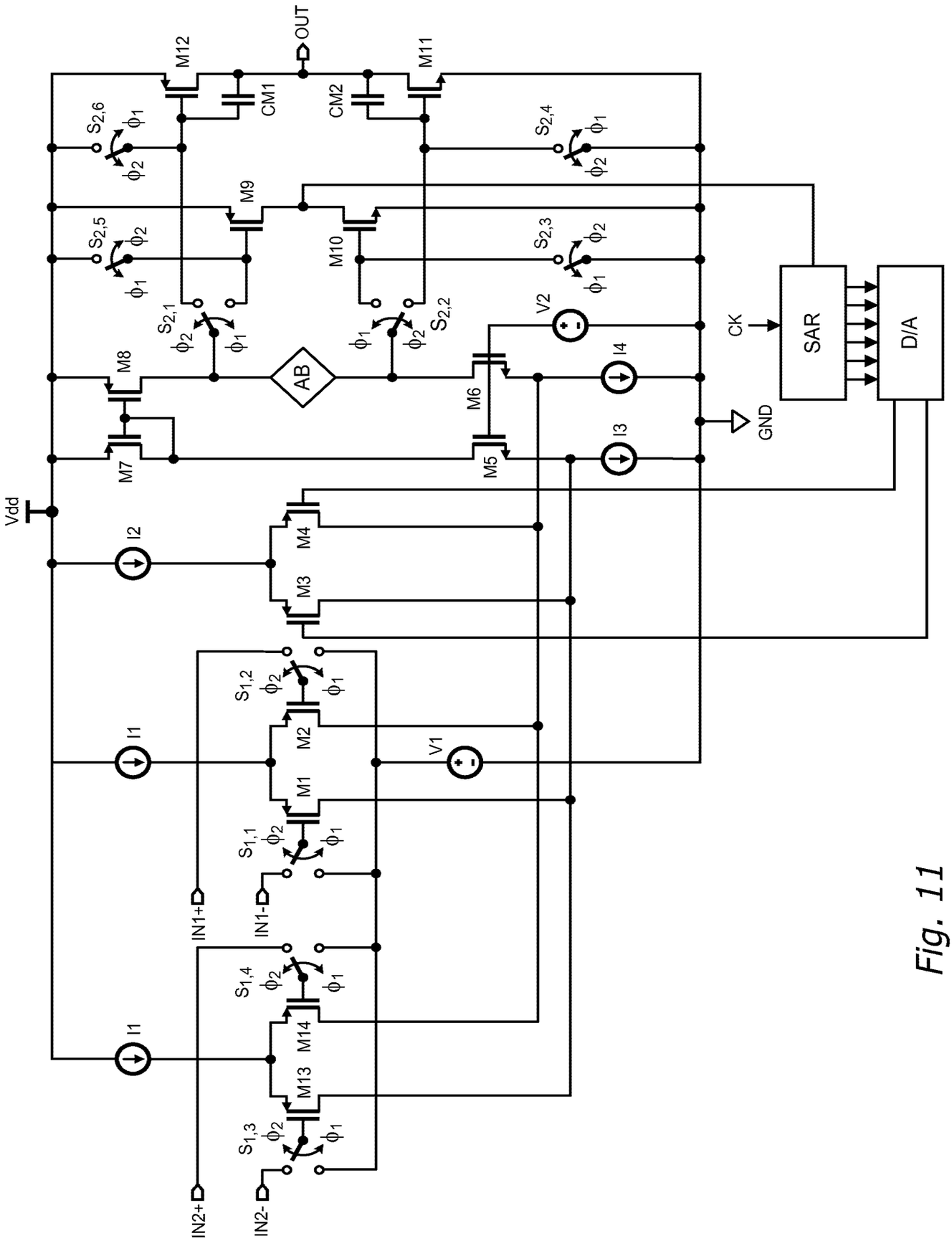

Vdd
I2
I1
I1
M4
M3
M2
M1
M14
M13
M12
M11
M10
M9
M8
M7
M6
M5
CM1
CM2
OUT
AB
V1
V2
I3
I4
GND
CK
SAR
D/A
IN1+
IN1-
IN2+
IN2-
S1,1
S1,2
S1,3
S1,4
S2,1
S2,2
S2,3
S2,4
S2,5
S2,6
ϕ1
ϕ2

Fig. 11

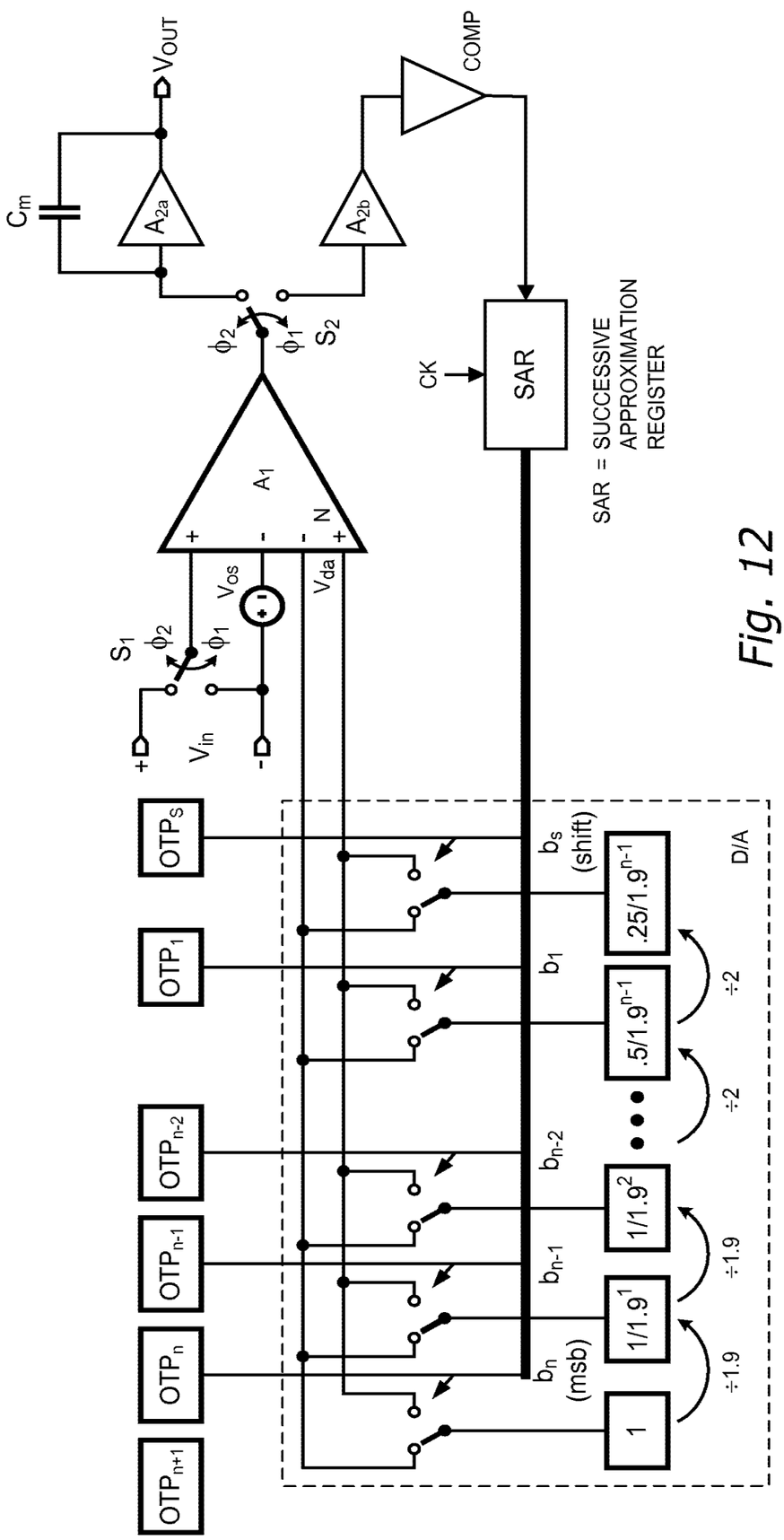

C_m
V_{OUT}
A_{2a}
A_{2b}
COMP
ϕ_2
ϕ_1
S_2
CK
SAR
SAR = SUCCESSIVE APPROXIMATION REGISTER
A_1
+
-
-
N
+
V_{os}
V_{da}
S_1
ϕ_2
ϕ_1
V_{in}
+
-
OTP_S
OTP_1
OTP_{n-2}
OTP_{n-1}
OTP_n
OTP_{n+1}
b_s (shift)
b_1
b_{n-2}
b_{n-1}
b_n (msb)
$.25/1.9^{n-1}$
$.5/1.9^{n-1}$
$1/1.9^2$
$1/1.9^1$
1
÷2
÷2
÷1.9
÷1.9
D/A

Fig. 12

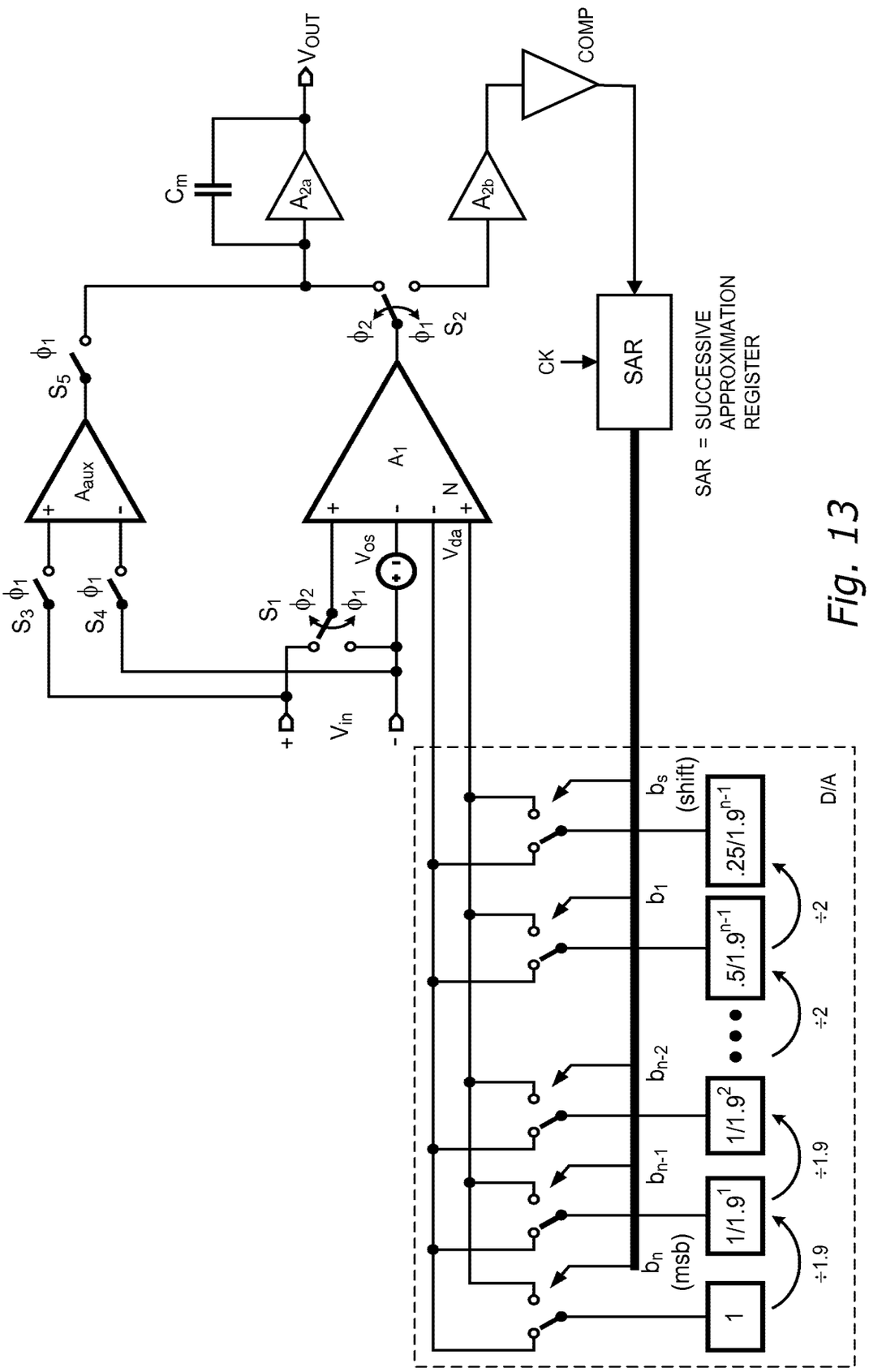

VOUT
COMP
Cm
A2a
A2b
S5
S2
CK
SAR
SAR = SUCCESSIVE APPROXIMATION REGISTER
Aaux
A1
S3
S4
S1
Vos
Vda
Vin
bs (shift)
b1
bn-2
bn-1
bn (msb)
.25/1.9n-1
.5/1.9n-1
1/1.92
1/1.91
1
÷2
÷1.9
D/A

Fig. 13

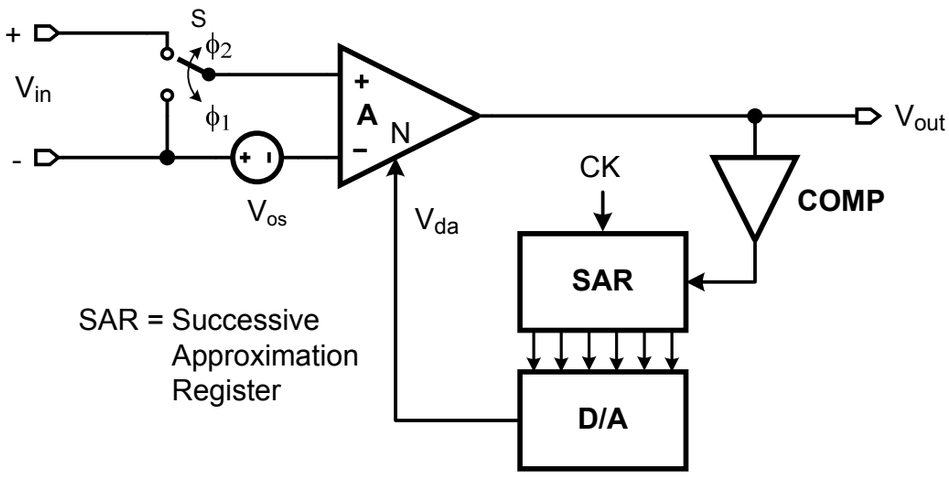


Fig. 1 (Prior Art)

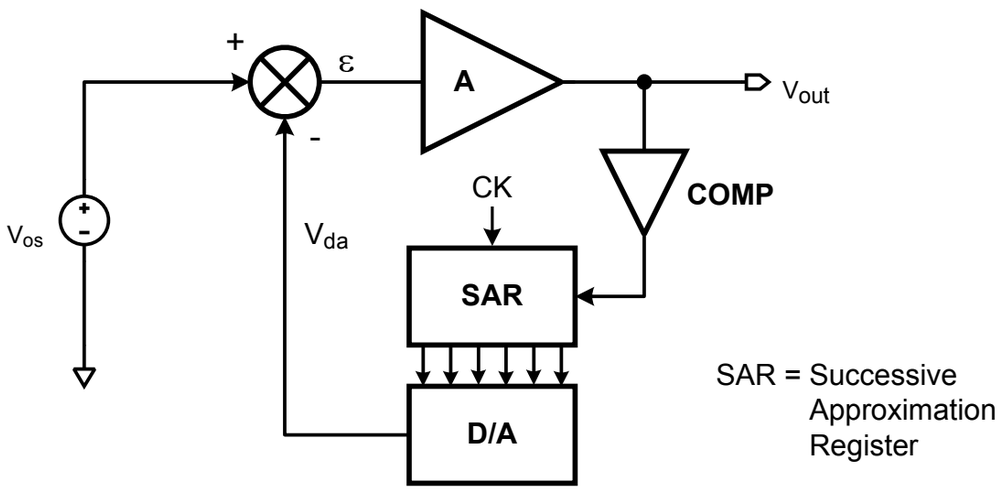


Fig. 2 (Prior Art)

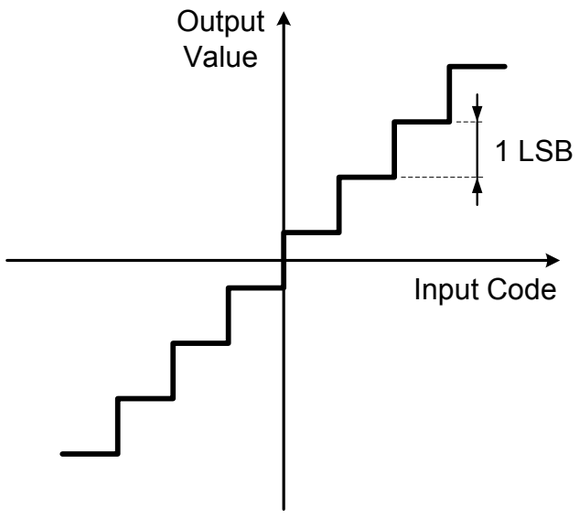

Output
Value
1 LSB
Input Code

Fig. 3

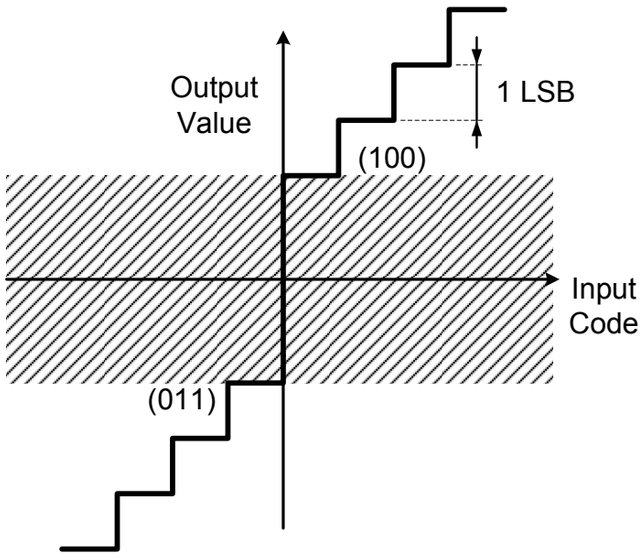

Output
Value
1 LSB
(100)
Input
Code
(011)

Fig. 4

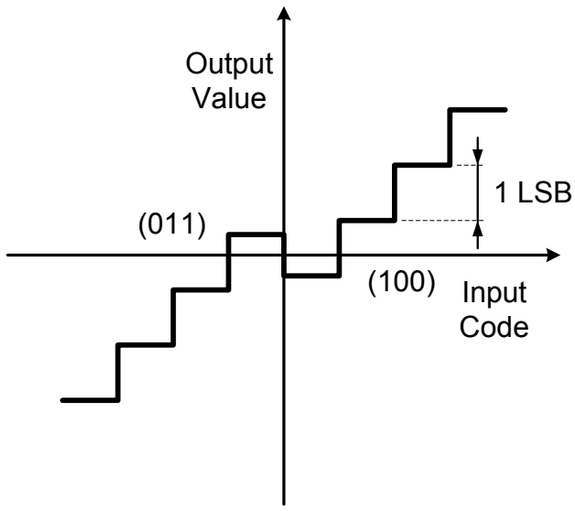

Output
Value
1 LSB
(011)
(100)
Input
Code

Fig. 5

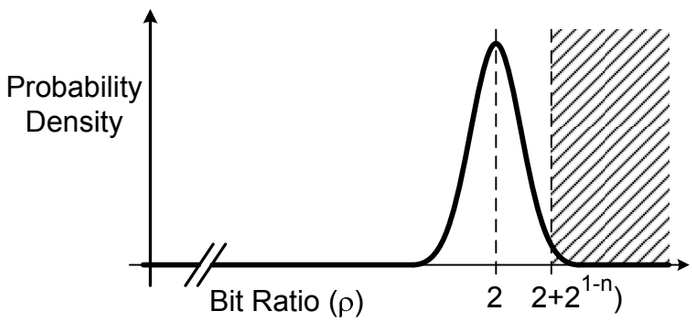

Probability
Density
Bit Ratio (ρ)
2
2+2^1-n)

Fig. 6

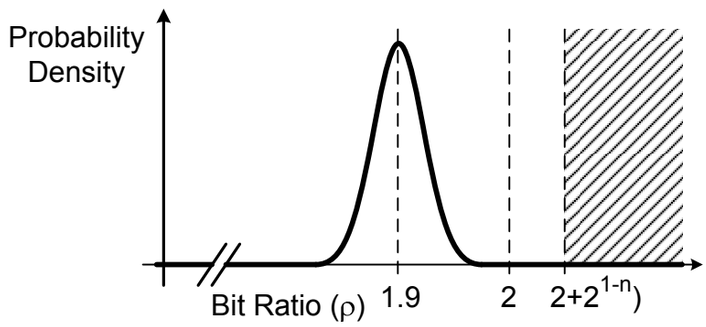


Fig. 7

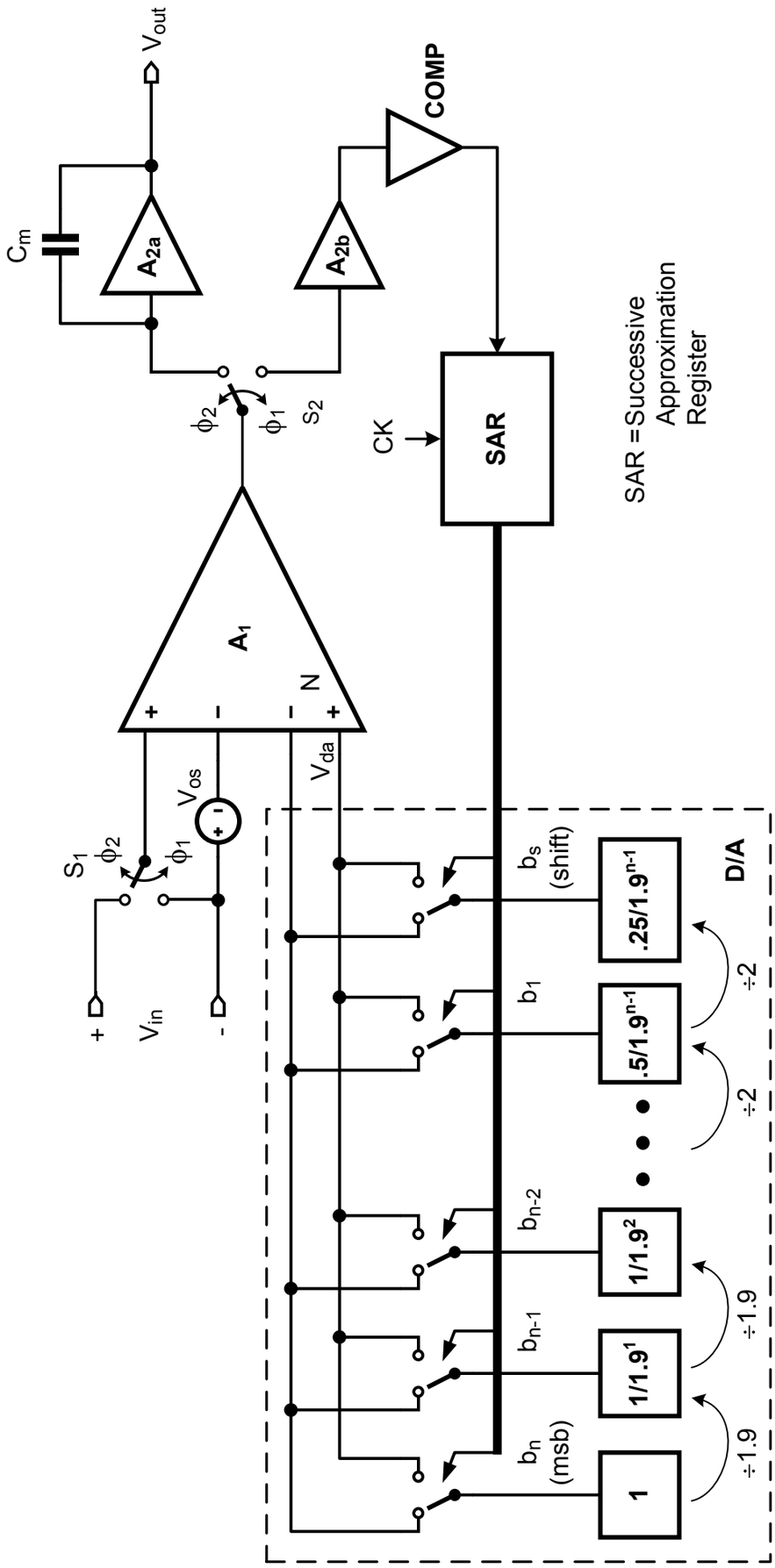

V_{out}
C_m
A_{2a}
A_{2b}
COMP
ϕ_2
ϕ_1
S_2
CK
SAR
SAR =Successive Approximation Register
A_1
+
-
-
+
N
V_{os}
V_{da}
S_1
ϕ_2
ϕ_1
+
V_{in}
-
b_s (shift)
b_1
b_{n-2}
b_{n-1}
b_n (msb)
.25/1.9^{n-1}
.5/1.9^{n-1}
1/1.9^2
1/1.9^1
1
D/A
÷2
÷2
÷1.9
÷1.9

Fig. 8

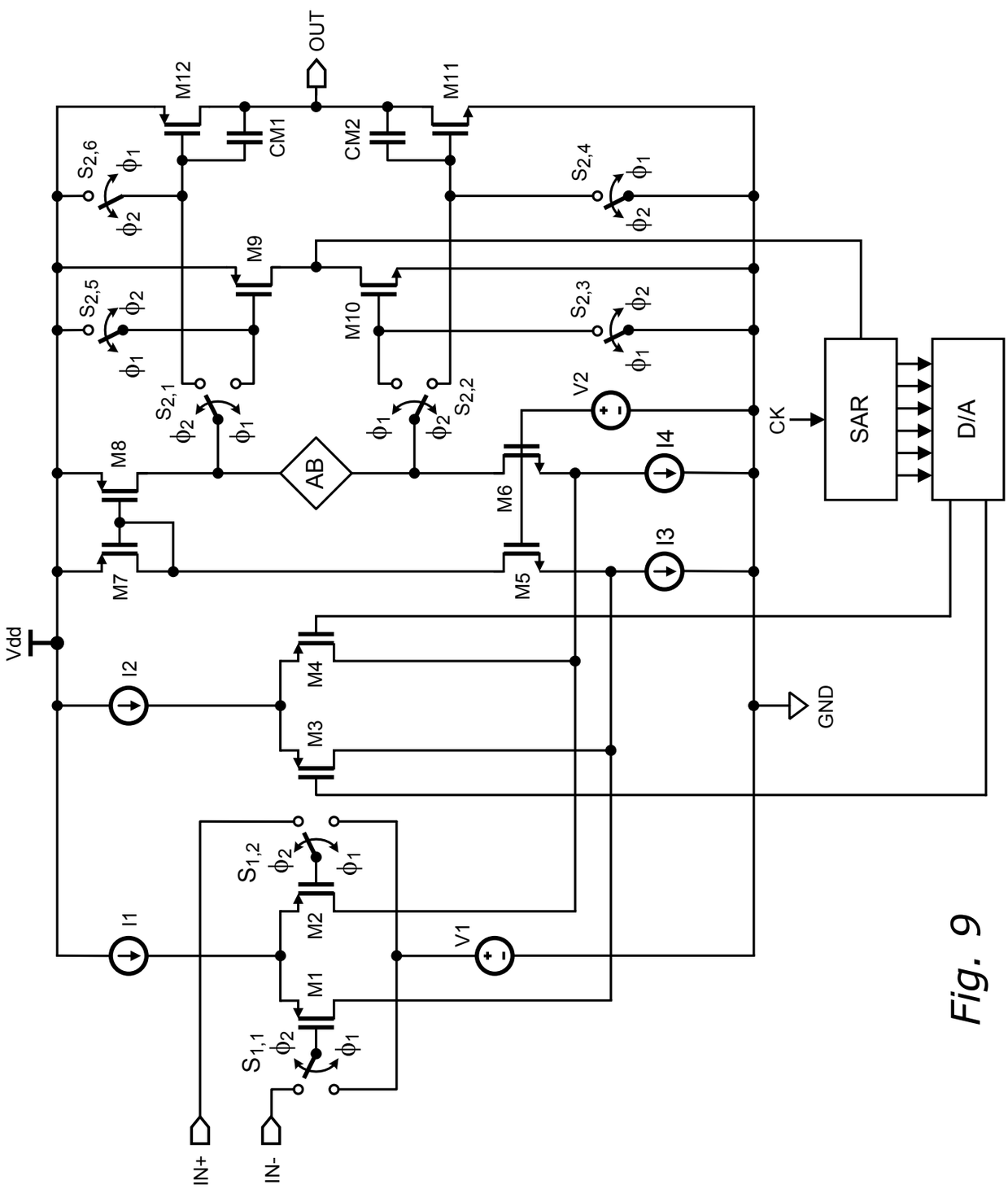

OUT
M12
M11
CM1
CM2
S2,6
S2,4
S2,5
S2,3
S2,1
S2,2
M9
M10
M8
M7
M6
M5
AB
V2
I4
I3
CK
SAR
D/A
Vdd
I2
M4
M3
GND
S1,2
M2
M1
I1
V1
S1,1
IN+
IN-

Fig. 9

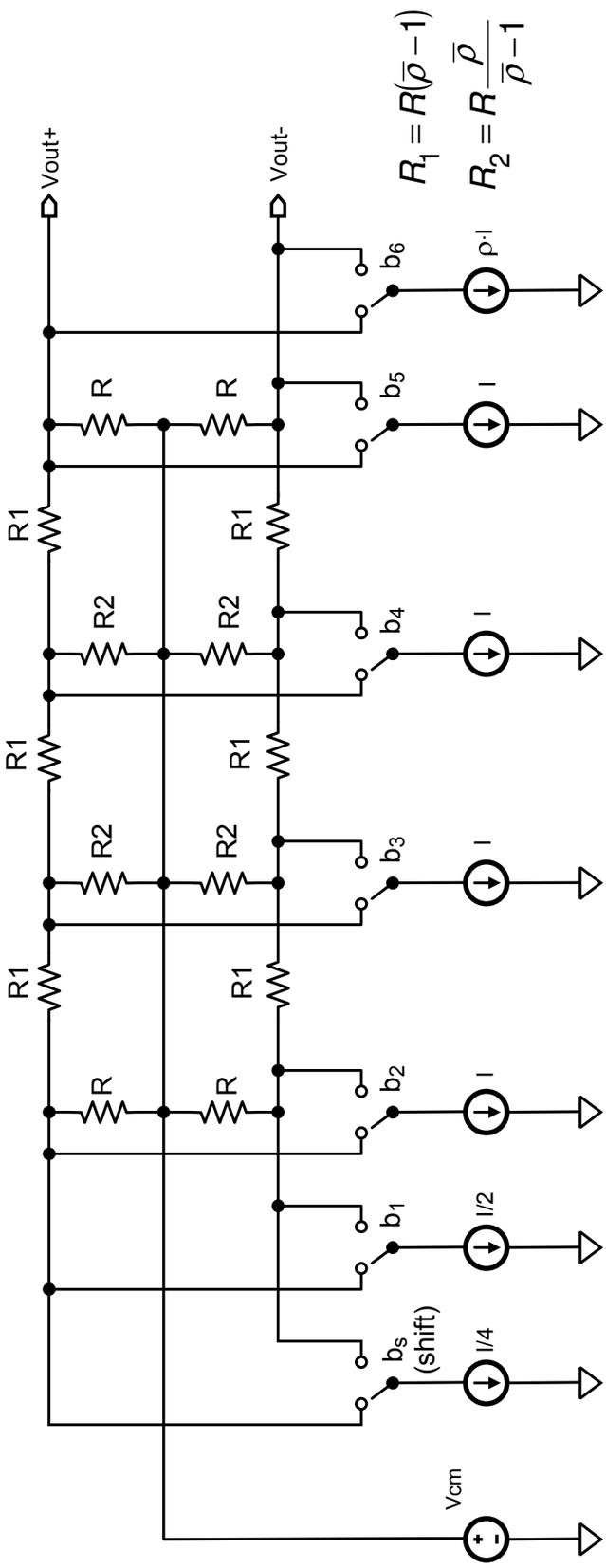

Vout+
Vout-
$R_1 = R(\overline{\rho} - 1)$
$R_2 = R\frac{\overline{\rho}}{\overline{\rho} - 1}$
R
R1
R2
b6
b5
b4
b3
b2
b1
bs
(shift)
ρ·I
I
I/2
I/4
Vcm

Fig. 10

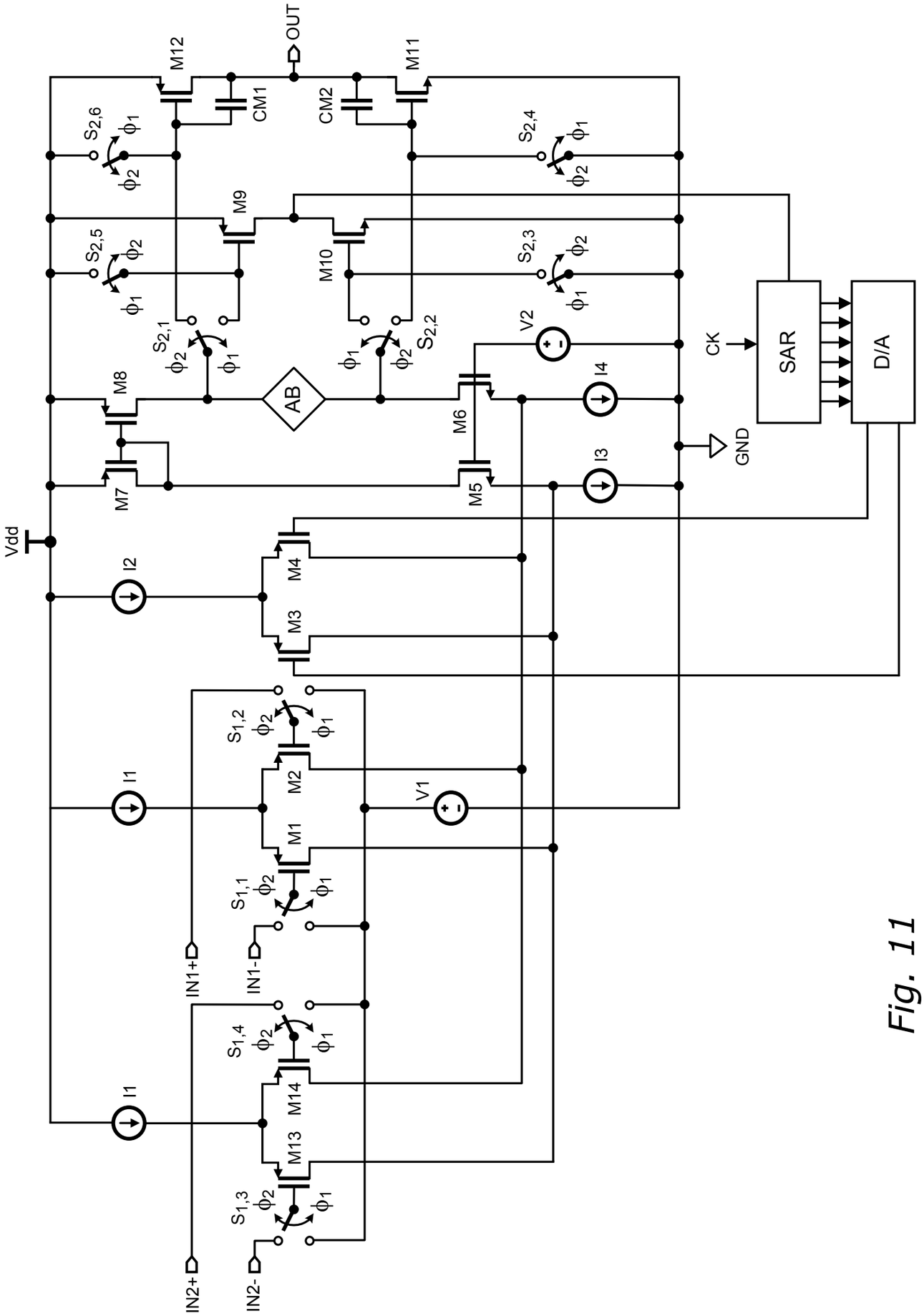

Vdd
I1
I2
I3
I4
I1
M1
M2
M3
M4
M5
M6
M7
M8
M9
M10
M11
M12
M13
M14
CM1
CM2
V1
V2
AB
OUT
GND
CK
SAR
D/A
IN1+
IN1-
IN2+
IN2-
S1,1
S1,2
S1,3
S1,4
S2,1
S2,2
S2,3
S2,4
S2,5
S2,6
ϕ1
ϕ2

Fig. 11

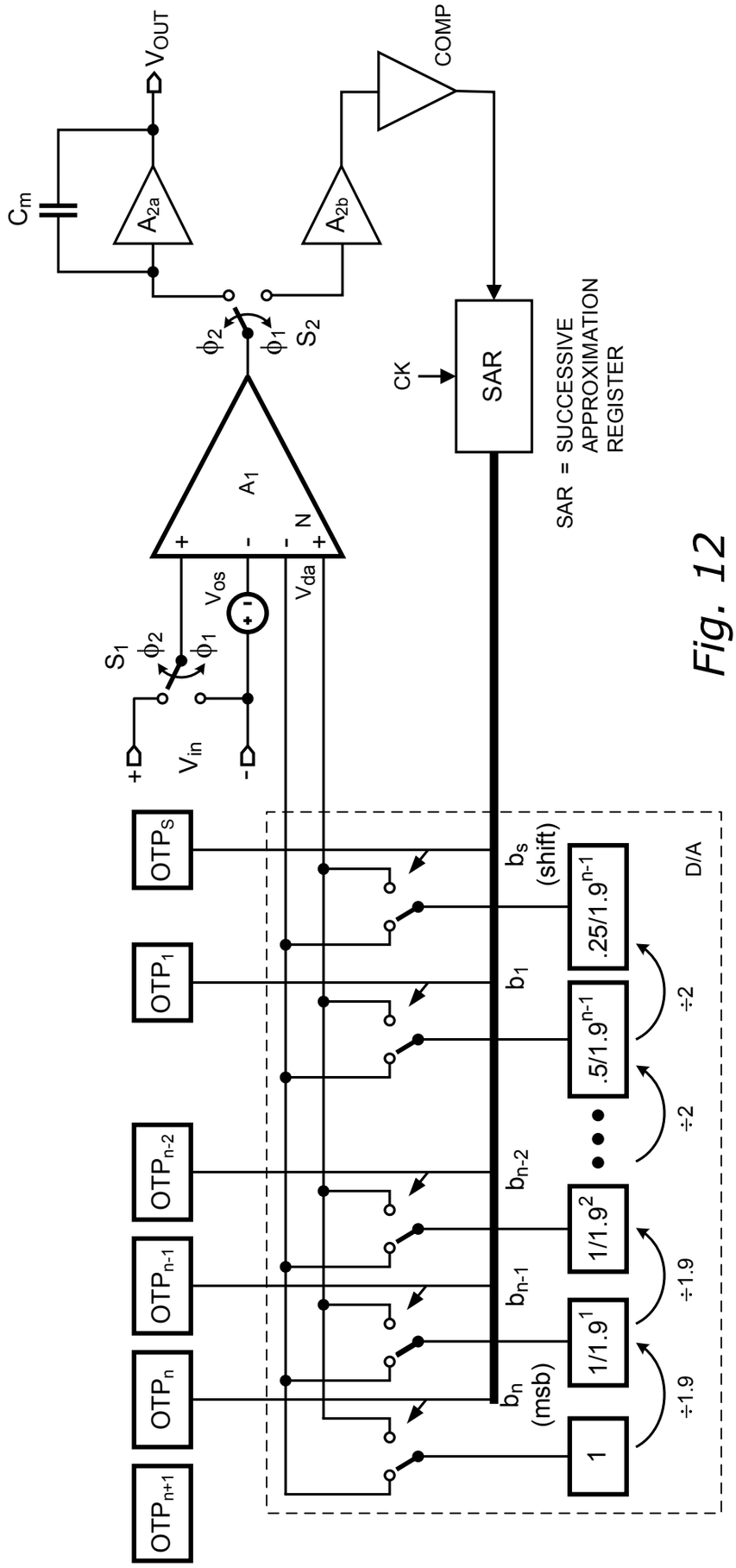

VOUT
COMP
Cm
A2a
A2b
ϕ2
ϕ1
S2
CK
SAR
SAR = SUCCESSIVE APPROXIMATION REGISTER
A1
+
-
-
+
N
Vos
Vda
S1
ϕ2
ϕ1
Vin
+
-
OTPS
OTP1
OTPn-2
OTPn-1
OTPn
OTPn+1
bs (shift)
b1
bn-2
bn-1
bn (msb)
.25/1.9n-1
.5/1.9n-1
1/1.92
1/1.91
1
÷2
÷2
÷1.9
÷1.9
D/A

Fig. 12

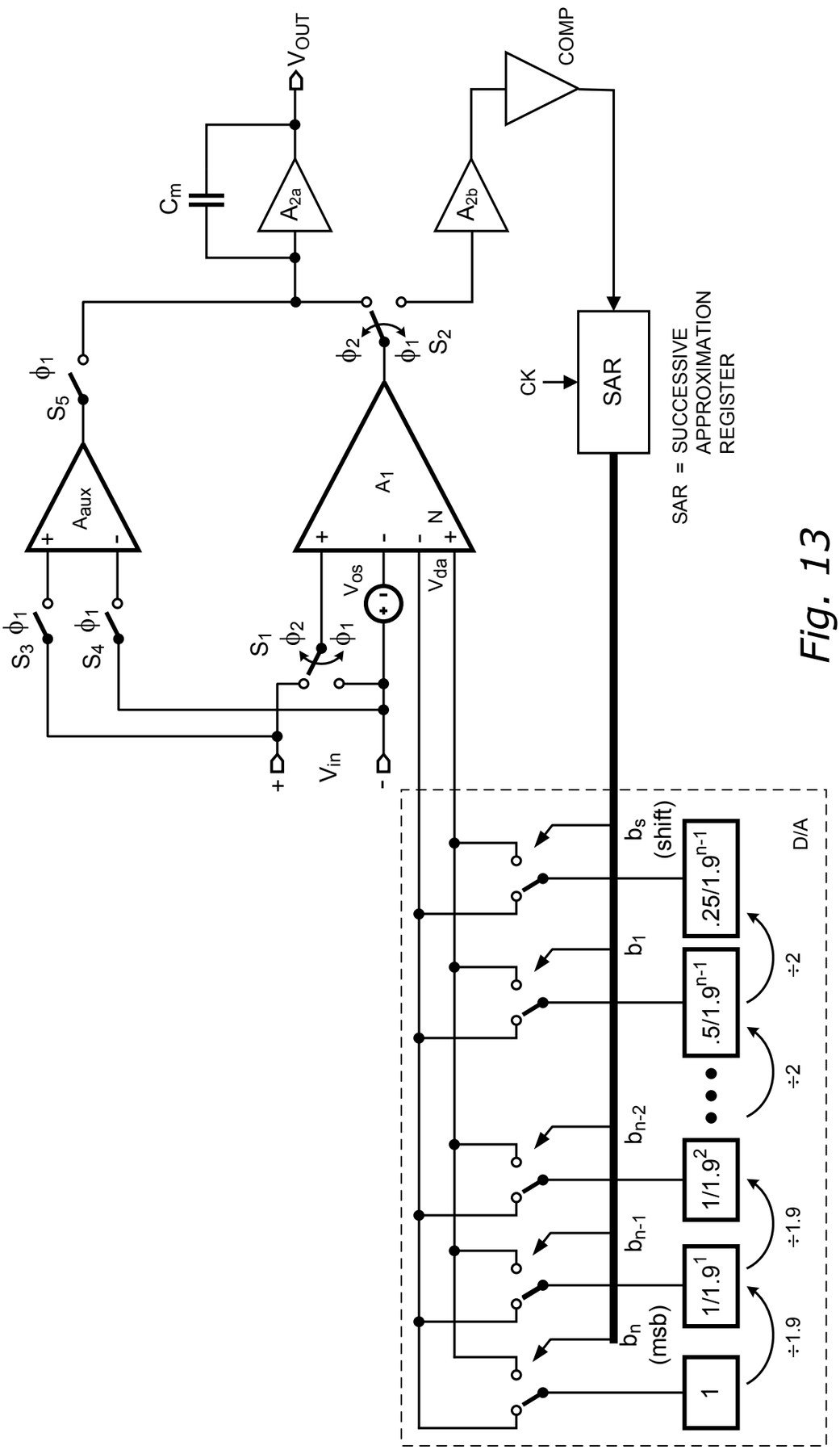

VOUT
COMP
Cm
A2a
A2b
ϕ2
ϕ1
S2
ϕ1
S5
Aaux
A1
CK
SAR
SAR = SUCCESSIVE APPROXIMATION REGISTER
S3 ϕ1
S4 ϕ1
S1 ϕ2 ϕ1
Vos
Vda
Vin
bs (shift)
b1
bn-2
bn-1
bn (msb)
.25/1.9n-1
.5/1.9n-1
1/1.92
1/1.91
1
÷2
÷2
÷1.9
÷1.9
D/A

Fig. 13

DocCode - SCORE

SCORE Placeholder Sheet for IFW Content

Application Number: 12390684 Document Date: 5/18/2009

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions developed by SIRA.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://es/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: February 8, 2006

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/390,684	02/23/2009	2817	1090	55123P377	20	2

CONFIRMATION NO. 5595

UPDATED FILING RECEIPT

79124
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

OC00000036149642

Date Mailed: 05/28/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Rudy G. H. Eschauzier, Bergschenhoek, NETHERLANDS;
Nico van Rijn, Katwijk, NETHERLANDS;

Assignment For Published Patent Application

NUMBER 14 B.V., Bergschenhoek, NETHERLANDS

Power of Attorney: The patent practitioners associated with Customer Number 79124

Domestic Priority data as claimed by applicant

Foreign Applications

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 03/12/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/390,684**

Projected Publication Date: 08/26/2010

Non-Publication Request: No

Early Publication Request: No

Title

Amplifiers with Input Offset Trim and Methods

Preliminary Class

330

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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Transaction History Date 2010-06-01
Date information retrieved from USPTO Patent Application Information Retrieval (PAIR) system records at www.uspto.gov

Notice of Allowability	Application No.	Applicant(s)	
	12/390,684	ESCHAUZIER ET AL.	
	Examiner	Art Unit	
	Henry K. Choe	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application filed on 5/18/09*.

2. ☒ The allowed claim(s) is/are *1-12*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 2/23/09
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Henry K Choe/
Primary Examiner, Art Unit 2817

DETAILED ACTION

Election/Restriction

This application contains claims directed to the following patentably distinct species of the claimed invention:

Species	Figure(s).	
I	8	(claims 1-12)
II	9	(claims 13-20)

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

A telephone call was made to Mr. Roger Blakeley on 5/25/10 to request an oral election to the above restriction requirement. Applicant elected the specie I without a traverse. Therefore, the claims 13-20 are considered non-elected claims.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Claims 13-20 have been cancelled.

Reasons for Allowance

Claims 1-12 are allowed.

The following is an examiner's statement of reasons for allowance: Regarding claim 1, the closest prior art of record, Leung et al (Fig. 1) does not disclose the following limitations: the functional limitations of the second switch.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (571) 272-1760.

/Henry K Choe/

Primary Examiner, Art Unit 2817

Notice of References Cited	Application/Control No. 12/390,684	Applicant(s)/Patent Under Reexamination ESCHAUZIER ET AL.	
	Examiner Henry K. Choe	Art Unit 2817	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,456,220	09-2002	Leung et al.	341/155
*	B	US-5,627,475	05-1997	Strosser, Richard P.	324/546
*	C	US-4,764,753	08-1988	Yukawa, Akira	341/166
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt Date: 2/23/09

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	Not Yet Assigned 12/390,684
	Filing Date	Even Date Herewith 2/23/09
	First Named Inventor	Rudy G. H. Eschauzier
	Group Art Unit	2817
	Examiner Name	Henry Choe
Sheet 1 of 1	Attorney Docket No: 55123P377	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/H.C./		US-6,130,632	10/10/2000	Opris, Ion E.	
/H.C./		US-6,348,885	02/19/2002	Munoz, Carlos E., et al.	
/H.C./		US-6,486,806	11/26/2002	Munoz, Carlos E., et al.	
/H.C./		US-6,707,403	03/16/2004	Hurrell, Christopher P.	
/H.C./		US-6,828,927	12/07/2004	Hurrell, Christopher P., et al.	
/H.C./		US-7,026,866	04/11/2006	Llewellyn, William D.	
/H.C./		US-7,038,609	05/02/2006	Hurrell, Christopher P.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
/H.C./		JP-2-288616	11/28/1990	Nene, Yoshito , et al.		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
/H.C./		ENZ, CHRISTIAN C., et al., "Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization", Proceedings of the IEEE, Vol. 84, No. 11, (November 1996), Pgs. 1584-1614	
/H.C./		HUIJSING, J , "Operational Amplifiers, Theory and Design", Kluwer Academic Publishers, (2001), Pgs. 52-53	
/H.C./		KRUMMENACHER, FRANCOIS , et al., "A High-Performance Autozeroed CMOS Opamp with 50uV Offset", IEEE International Solid-State Circuits Conference, Session 21, Amplifiers, Paper SA 21.3, (1997), Pgs. 350-351	
/H.C./		VAN DE PLASSCHE, R J., "Analog-To-Digital and Digital-To-Analog Converters", Springer, (1994), Pgs 280-283	

EXAMINER	/Henry Choe/	DATE CONSIDERED	05/25/2010

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

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NOTICE OF ALLOWANCE AND FEE(S) DUE

79124 7590 06/01/2010

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SUNNYVALE, CA 94085-4040

EXAMINER	
CHOE, HENRY	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/01/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/390,684	02/23/2009	Rudy G. H. Eschauzier	55123P377	5595

TITLE OF INVENTION: AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/01/2010

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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PTOL-85 (Rev. 08/07) Approved for use through 08/31/2010.

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(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/390,684	02/23/2009	Rudy G. H. Eschauzier	55123P377	5595

TITLE OF INVENTION: AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/01/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOE, HENRY	2817	330-009000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

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Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

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❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/390,684	02/23/2009	Rudy G. H. Eschauzier	55123P377	5595

79124 7590 06/01/2010

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EXAMINER	
CHOE, HENRY	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/01/2010

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 39 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 39 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/390,684	02/23/2009	Rudy G. H. Eschauzier	55123P377

CONFIRMATION NO. 5595

79124
MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

PUBLICATION NOTICE

OC000000043224255

Title:AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

Publication No.US-2010-0213983-A1
Publication Date:08/26/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Electronic Acknowledgement Receipt	
EFS ID:	8330294
Application Number:	12390684
International Application Number:	
Confirmation Number:	5595
Title of Invention:	AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS
First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Customer Number:	79124
Filer:	Roger W. Blakely/Jessica Clark
Filer Authorized By:	Roger W. Blakely
Attorney Docket Number:	55123P377
Receipt Date:	31-AUG-2010
Filing Date:	23-FEB-2009
Time Stamp:	16:57:35
Application Type:	Utility under 35 USC 111(a)

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6	NPL Documents	Pastre_et_al_2006.PDF	848928 fa43fb0f995465187a3d18890255cd14c2bce039	no	31
Warnings:					
Information:					
7	NPL Documents	Pastre_et_al_2009.PDF	448615 c2475516d56111cd1e9088a300ea6c1fe2605318	no	6
Warnings:					
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8	Issue Fee Payment (PTO-85B)	55123P377_20100831_IssueFeeTrans_FeeAddr.PDF	67202 6face6da2686532abd657925d5cb1027a7cdf4ad	no	2

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9	Fee Worksheet (PTO-875)	fee-info.pdf	33908 5db1eb6474eed22d9ed387f8254ffedb17ddefaa	no	2
Warnings:					
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			Total Files Size (in bytes):	3261559	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	12/390,684
Filing Date	February 23, 2009
First Inventor	Rudy G. H. Eschauzier, et al.
Art Unit	2817
Examiner Name	Choe, Henry
Attorney Docket No.	55123P377 Conf. No. 5595

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted on or before payment of the Issue Fee. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The references were cited in a Search Report dated July 7, 2010 (copy enclosed herewith and, if not in the English language, a cover sheet with English language translation is attached).

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

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OR

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☒ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	Roger W Blakely	Date (MM-DD-YYYY)	08-31-2010
Name/Print	Roger W. Blakely, Jr.	Registration Number	25,831

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Jessica A. Clark Jessica A Clark *Date* *08-31-10*

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	12/390,684
	Filing Date	02/23/2009
	First Named Inventor	Rudy G. H. Eschauzier
	Group Art Unit	2817
	Examiner Name	Choe, Henry
Sheet 1 of 1	Attorney Docket No: 55123P377	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-2003/0214351	11/20/2003	Nandy, Tapas, et al.	

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Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
		WO-2004/073163	08/26/2004	Wang, Zhenhua		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
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		"Partial European Search Report Dated 07 July 2010", European Patent Application No. 10153869.2	
		GUSTAT, HANS, "A DC-10 GHz amplifier with digital offset correction", Materials Science in Semiconductor Processing, Proceedings of the Second International SIGE Technology and Device Meeting (ISTDM 2004), Vol. 8, (13 October 2004), pp. 439-443	
		PASTRE, MARC, et al., Methodology for the Digital Calibration of Analog Circuits and Systems, with Case Studies, Published by Springer, (2006), pp. 12-14, 23-35, 52-62, 106-107	
		PASTRE, MARC, et al., "Methodology for the Digital Calibration of Analog Circuits and Systems Using Sub-binary Radix DACs", Mixed Design of Integrated Circuits and Systems, MIXDES 2009, 16th International Conference, (June 25-27, 2009), pp. 456-461	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

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26 August 2004 (26.08.2004)

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(10) International Publication Number
WO 2004/073163 A1

(51) International Patent Classification[7]: H03F 3/45

(21) International Application Number:
PCT/IB2004/000318

(22) International Filing Date: 28 January 2004 (28.01.2004)

(25) Filing Language: English

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(30) Priority Data:
03100281.9 11 February 2003 (11.02.2003) EP

(71) Applicant *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N. V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

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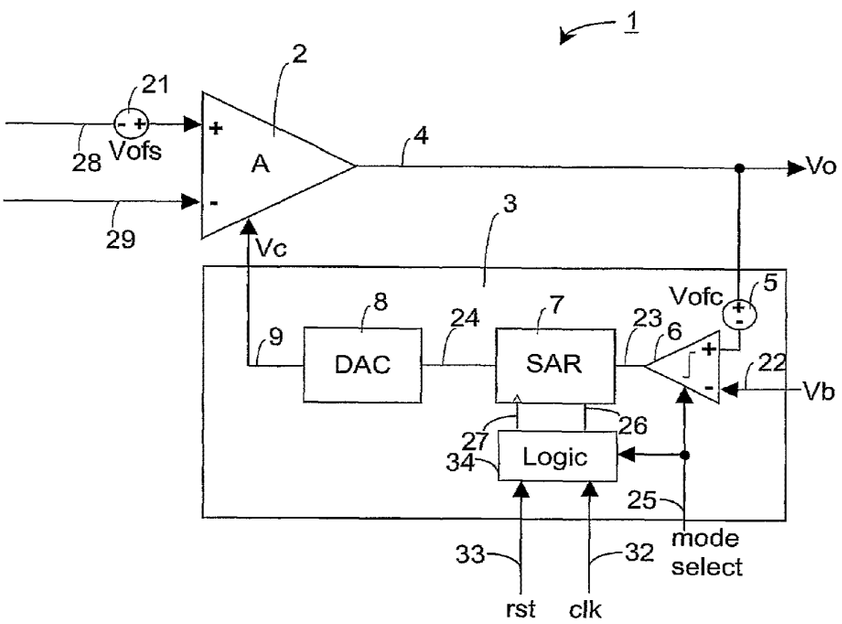
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(54) Title: SELF ZEROING FOR CRITICAL, CONTINUOUS-TIME APPLICATIONS



(57) Abstract: Apparatus (1) for continuous-time application, comprising an operational amplifier (2) and a self-zeroing control unit (3) for reducing an offset of the operational amplifier (2). The self-zeroing control unit (3) provides for a self zeroing operation mode and a normal operation mode. It comprises a comparator (6), a successive approximation register (7), and a digital-to-analog converter (8).

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Self zeroing for critical, continous-time applications

The present invention concerns apparatus and integrated circuits for continuous-time applications where the offset of at least one operational amplifier is compensated by a dedicated circuitry. The present invention also concerns a method for offset compensation.

Integrated circuits quite often require operational amplifiers. These amplifiers are typically employed to process signals such as amplification, filtering, etc. Depending on the application for which the integrated circuit is being used, the voltage offset of the operational amplifiers may have a detrimental impact on the circuit's performance.

The internal offset voltage has long been a serious problem with CMOS operational amplifiers, and large internal offsets can not be tolerated in precision applications, for instance. The difficulty in offset reduction lies at the fact that this offset is a random quantity, as well, and it not only depends strongly on the matching of the used devices, but also varies with temperature, supply voltage, and so forth. Moreover, the systematic offset is also subject to process variations.

For critical continuous-time applications, so far, low-offset design must rely on large transistor sizes leading to a high current consumption, or on very expensive post-trimming. It is thus obvious that all these known approaches are very limited.

Some known techniques such as chopper and auto zero are more effective, but can not be applied to continuous-time applications, because they are time discrete.

There is a need for low-offset operational amplifiers for telecommunication applications such as channel filters, smooth filters, anti-aliasing filters, automated gain control (AGC), high precision measurement systems, and so

forth.

A scheme for offset calibration of operational amplifiers is described in US patent 5,397,944. The offset calibration proposed in this US patent requires the respective operational amplifier to be in an open loop circuit. A plurality of switches is required that are used for the calibration only. It also requires a dedicated resistor accompanied by a switch both being used only for the compensation. Each of the amplifiers has associated with it a calibration logic which includes a ripper counter and a digital-to analog converter (DAC). The counter provides output signals to the DAC which in turn provides varying amounts of bias currents to a node inside the amplifier. The US patent 5,397,944 embodies kind of a trial-and-error approach where the offset calibration is done step by step until the right bias current is found. It is a disadvantage of the scheme proposed in this US patent, that for a 6 bit DAC resolution, 64 clock cycles are required to complete the calibration. The circuit proposed suffers from supply and substrate noise, since one of the switches must be connected directly to the inverting input terminal of the operational amplifiers. This is a serious problem because the inverting input terminal of an operational amplifier is the most sensitive node in such an amplifiers. Due to this, the supply and substrate noise will degrade the circuit performance.

It is thus an objective of the present invention to provide a scheme for efficiently reducing the offset of operational amplifiers.

Accordingly, it is an object of the invention to provide an integrated circuit solution capable of automatically compensating a high range of offset components in an analog input signal of an operational amplifier while preserving the high precision.

It is a further object of the invention to provide an integrated circuit solution with reduced offsets at the operational amplifiers but without requiring a lot of circuit overhead.

An apparatus in accordance with the present invention is claimed in claim 1. Various advantageous embodiments are claimed in claims 2 through 8.

An integrated circuit in accordance with the present invention is claimed

in claim 9. Various advantageous embodiments are claimed in claims 10 through 12.

A method in accordance with the present invention is claimed in claim 13. Various advantageous methods are claimed in claims 14 and 15.

Immediate benefits of this invention are improved reliability, flexibility, and competitiveness.

Other advantages of the present invention are addressed in connection with the detailed embodiments.

For a more complete description of the present invention and for further objects and advantages thereof, reference is made to the following description, taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a schematic block diagram of a first apparatus, according to the present invention;

Fig. 2 is a schematic block diagram of a conventional successive approximation register analog-to-digital converter (SAR ADC);

Fig. 3 is a schematic block diagram of a second apparatus, according to the present invention;

Fig. 4 is a schematic representation of the mode select signal, according to the present invention;

Fig. 5 is a schematic block diagram of a third apparatus, according to the present invention;

Fig. 6 is a schematic block diagram of a fourth apparatus, according to the present invention;

Fig. 7 is a schematic block diagram of a fifth apparatus, according to the present invention;

Fig. 8 is a schematic block diagram of a sixth apparatus, according to the present invention;

Fig. 9 is a schematic block diagram of a seventh apparatus, according to the present invention;

Fig. 10 is a schematic block diagram of an eighth apparatus, according to

the present invention;

Fig. 11 is a schematic representation of some signals, according to the present invention.

The present invention is based on the following principle. The key component that makes self zeroing possible for continuous-time applications is a self-zeroing control (SZC) unit 3 in connection with the operational amplifier 2 whose offset (Vofs) has to be reduced or even cancelled (this process is hereinafter referred to as offset compensation). The basic block diagram of an apparatus 1 with self zeroing, according to the present invention, is depicted in Fig. 1.

Since the various embodiments addressed herein are derived from the known successive approximation register analog-to-digital converter (SAR ADC) architecture, this architecture is briefly addressed.

Although there are many variations in the implementation of a SAR ADC 10, the basic architecture is quite simple (see Fig. 2). An analog input voltage (VIN) is applied to one input of a comparator 11 and a reference voltage VREF is provided to an K-bit digital-to-analog converter (DAC) 14. A comparison is then performed to determine if VIN is less than or greater than the voltage VDAC at the output of he DAC 14. If VIN is greater than VDAC, the comparator output is a logic high or '1' and the most significant bit (MSB) of the K-bit register remains at '1'. Conversely, if VIN is smaller than VDAC, the comparator output is a logic low and the MSB of the K-bit register 13 is cleared to logic '0'. A SAR control logic 12 is provided that then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the least significant bit (LSB). Once this is done, the conversion is complete, and an K-bit digital word is available in the K-bit register 13.

Turning now to Fig. 3, the basic principles of a SZC unit 3, according to present invention, are addressed. The SZC unit 3 comprises a comparator 6, a successive approximation register (SAR) 7, and a digital-to-analog converter (DAC) 8. Preferably, all these units 6 through 8 are standard circuit elements (standard library cells). The apparatus 1 has at least two basic modes of operation: (1) self zeroing mode

and (2) normal operation mode. The mode of operation may be controlled by a mode select signal (e.g., a operational amplifier select signal that is suited to select one out of a plurality of operational amplifiers). One possible relation between the mode select signal and the two modes (1) and (2) is depicted in Fig. 4. Normally, the apparatus 1 first enters the self zeroing mode (1) after a power on event. The apparatus may be implemented so that an update is possible from time to time. In case of an update, the self zeroing mode (1) is entered temporarily before returning to the normal mode of operation (2).

At the core of the SZC unit 3 is the SAR 7, which controls the entire self zeroing process. The SAR 7 here works in a very similar manner as a conventional and well known SAR ADC 10, that was briefly addressed above. However, some major differences are worth mentioning. While in a SAR ADC 10 (cf. Fig. 2), the DAC output signal of the DAC 14 is fed back to one input of the comparator 11, the output 9 of the DAC 8 in Fig. 3 is applied to one node of the operational amplifier 2 on which the self zeroing is to be performed. Also, in a SAR ADC 10, the other input of the comparator 11 is the analog signal VIN to be converted to digital, while in Fig. 3 this input 28 is connected to a DC voltage Vb during the self zeroing mode (1). Vb may be a voltage that is set to midrail, i.e., Vb = (Vdd+Vss)/2. It should be noted that Vo=Vb if the inputs 28 and 29 of the operational amplifier 2 are short circuited and if the operational amplifier 2 is free of offset (i.e., Vofs = 0). While in a SAR ADC 10 the output voltage of the DAC 14 at the end of each conversion step is the closest reproduction of the analog input voltage VIN (via both ADC and DAC), in the present system neither the value nor the polarity of the offset at the inputs 28, 29 can be predicted. The voltage Vc at the output 9 is thus not predictable either. For convenience, a known polarity is assigned to the offset voltage Vofs throughout this description.

The SAR 7 has an input 23 for receiving an analog input signal from the comparator 6 and an output 24 at which a digital output signal representing the value of the analog input signal is made available at a selected time. The SAR 7 performs an analog to digital conversion. The digital output signal is fed to the DAC 8. The DAC 8 (also known as D/A converter) is an electronic circuit that converts the digital representation of the quantity at the SAR's output 24 into a discrete analog value. The input signal to the DAC 8 is a digital binary code, and this code, along with a known

reference voltage, results in a voltage Vc or current at the DAC output 9. By increasing the resolution of the DAC 9, the number of discrete steps can be increased and the step size can be reduced (which reduces the quantization error), resulting in a signal that closer approximates a continuous time signal. That is, the DAC 8 provides at its output 9 an analog output voltage Vc (or in some embodiments an analog output current) representing the offset at the operational amplifier that is to be compensated. The DAC 8 receives a sequence of digital signals generated by the SAR 7 at successive times and provides in response to each digital signal of the sequence the output voltage Vc corresponding to said digital signal. The DAC 8 converts the digital input signal having N bits to a substantially equivalent analog output voltage Vc.

In the present embodiment, the SZC 3 comprises a logic unit 34 that is designed to generate a clock signal and a reset signal for the SAR 7. This clock signal is applied to an input 27 and this reset signal is applied to an input 26. These two signals are generated by the logic unit 34 by combining the input signals clk, rst and mode select, which are fed to the unit 34 via the inputs 32, 33, and 25. The unit 34 may comprise two AND gates for example.

The self zeroing process is considered to be completed when all N bits have been decided by the SAR 7. Then, the apparatus 1 is ready for the normal operation mode (2). It can be shown that for a properly designed apparatus 1 and an K-bit DAC 8, a residual error remains, given roughly by equation (A):

$$|\varepsilon| \leq \frac{\Lambda}{2^{N+1}} + \left|\frac{Vofc}{A}\right| \qquad \text{(A)}$$

where Λ is the maximum input offset of the operational amplifier 2 prior to the self zeroing process, Vofc is the input offset of the comparator 6, and A is the DC gain of the operational amplifier 2. From the equation (A), this residual error ϵ can be reduced with an increase in the DAC's resolution and a lowering of the comparator's offset Vofc. The second term of equation (A) can be reduced to a negligible level if a chopper comparator is used as comparator 6, or if the gain A of the operational amplifier 2 is high enough.

For precise self zeroing, the operational amplifier in the self zeroing mode (1) has to be isolated from its preceding stage. For this purpose, several switches S1 and S2 may be added to the embodiment of Fig. 3, as illustrated in Fig. 5. The mode

select signal is in the present embodiment used to switch from the self zeroing mode (1) to the normal operation mode (2) and back. For this purpose, the mode select signal (ms) is applied to the switches S1 and the inverted mode select signal ($\overline{ms}$) is applied to the switches S2. If the mode select signal ms is logic "1" (cf. Fig. 4), the switches S1 are closed and the switches S2 are open. The apparatus 30 is decoupled (isolated) from any preceding stage 31 during the self zeroing mode (1). If the mode select signal ms is logic "0" (cf. Fig. 4), the switches S1 are open and the switches S2 are closed. In this case the apparatus 30 is in the normal operation mode (2). This apparatus 30 has, however, implications, which can best be explained in connection with an embodiment 50, illustrated in Fig. 6. Here only two switches S3 and S4 are needed at the input side of the operational amplifier 42. In the self zeroing mode (1), the switch S4 is open and the switch S3 is closed. After the self zeroing process, the switch S3 is open and S4 is closed. Due to the presence of the switch S4, the gain of this stage 50 is altered to:

$$A = \frac{R2}{R1 + RS4}\,, \qquad \text{(B)}$$

where RS4 is the on-resistance of the switch S4. With large-size transistors, this effect can be reduced, but it is most desirable to eliminate during the normal operation mode (2) the switch S4 completely from the signal path between the preceding stage 51 and the stage 50, while still providing for the necessary isolation of the two stages 51 and 50 during the self zeroing mode (1). If the operational amplifier in the preceding stage 51 (not fully visible in Fig. 6) is not equipped with a power-down mode, the two switches S5 and S6 may be added to the output transistors T1 and T2 at the output side of this operational amplifier, as depicted on the left hand side of Fig. 6. When the switches S5 and S6 are closed, both pMOS and nMOS output transistors T1 and T2 are turned off. The switch S3 is closed too, so that the input 49 of the operational amplifier 42 is connected to Vb. In this way, the isolation of the two stages 50, 51 is ensured during the self zeroing mode (1). During the normal mode of operation (2), the switches S3, S5 and S6 are all open, and there is no closed switch in the signal path. That is, there is thus no on-resistance of a switch that is to be considered. The term RS4 disappears from the equation (B) if one removes the switch S4 completely. This switch S4 can be removed, either if the preceding stage 51 is equipped with a power-down mode, or if the output transistors T1 and T2 are equipped with switches S5 and

S6, as illustrated.

As mentioned above, the self zeroing process can be carried out upon power-on, or, if desired, at any time if an update is called for. The normal mode of operation (2) commences once the self zeroing process is completed. In order to safe power, the comparator 6, or 76, or 96, or 106 may be designed so that it turns off when the mode select signal ms is logic low.

As mentioned, the clock signal (clk) and the reset signal (rst) may be combined by a logic unit 34 comprising AND gates. If these two signals clk and rst are ANDed with the mode select signal ms before being applied to the inputs 26, 27 of the SAR 7, as shown in Fig. 3, the SAR 7 keeps its output states at the output 24 unchanged as long as the mode select signal ms is logic low. Upon completion of the self zeroing process, the only circuit element of the stage 1 that keeps running would be the DAC 8, which alone determines the power consumption of the SZC unit 3 during the normal mode of operation. This power saving feature is optional.

In the following, various self zeroing embodiments are addressed. On an integrated circuit (IC), e.g., a typical mixed-signal IC, there may be as many as a few dozens of operational amplifiers employed. Some of them are used for continuous-time applications and their input offset may be so critical that the specification can not be easily met without post-trimming, or self zeroing, as proposed herein. Then, the self zeroing has to be performed on all those critical operational amplifiers. If the number of operational amplifiers is N, a total of M=N SZC units has to be added, one to each of the critical operational amplifiers. This means that N comparators, N SARs, N DACs and so forth would be needed. In Fig. 7 an embodiment 60 with N=3 operational amplifiers 62 and M=3 SZC units 63 is depicted, that is N=M. This considerably adds to the overall overhead. It is therefore of importance how to use the resources efficiently in order to keep the overhead at a minimum. Different element sharing embodiments are addressed in the following sections.

In the present context, the strategy mainly aims at minimizing the overhead while preserving the high precision of the embodiments addressed so far. The basic idea is to let as few as possible common circuit elements be shared by as many operational amplifiers as possible. Another factor to be considered is the time (number of clock cycles) required for the self zeroing process. If a K-bit DAC is employed, for

one stage the self zeroing takes K clock periods to complete. This statement is only true for an embodiment similar to the one depicted in Fig. 1, 3, 5, or 6, for instance. Due to the element sharing, it will take longer since the self zeroing will have to be performed somehow sequentially rather than simultaneously. The longer time needed for completion of the self zeroing process is not assumed to be a big issue and the main focus in the present context is the reduction of the area overhead. Three basic element sharing embodiments are addressed below.

(I) Sharing a common SZC unit: In precision applications, it is often required for operational amplifiers to handle fully differential signals. This may be the case for example in an IC where a differential smoothing filter is required after the DAC part of a transmitter. Instead of a single fully differential operational amplifier, the IC 70 may comprise two conventional operational amplifiers 71, 72 (OP1 and OP2), as illustrated in Fig. 8. Because each operational amplifier 71, 72 has its own offset (Vof1 and Vof2, respectively), the resultant differential operational amplifier 80 is free of offset if both operational amplifiers 71, 72 have zero offset. In order to achieve this, M=2 SZC blocks would have to be added, one to each operational amplifier 71, 72 (as in Fig. 7). However, it is noted that the output offset becomes zero as long as Vof1=Vof2. This is permitted if both Vof1 and Vof2 are small and if the circuit meets all the requirements except the offset. Then only one SZC unit 73 is required, as illustrated in Fig. 8. The self zeroing voltage Vc can be applied to one of the two operational amplifiers (OP2 in Fig. 8) in order to cut the overhead to a half. In the present embodiment, the outputs 74 and 75 are coupled to the input side of the comparator 76, as illustrated.

(II) Sharing a common comparator: In order to make the second term in the equation (A) negligible, the inherent offset of the comparator of the SZC unit has to be much lower than the quantization error of the SAR. This implies that the qualified comparator may occupy considerable silicon area of the IC. It is thus desirable to use just one comparator for some or for all operational amplifiers, especially if the number (N) of operational amplifiers is large. An embodiment 90 sharing a common comparator 96 is illustrated in Fig. 9 with N=3 and M=1. The SZC unit 95 comprises N=3 DACs 97.1 through 97.3 and N=3 SARs 98.1 through 98.3, but just one comparator 96. This embodiment can be expanded to any number N of operational amplifiers within an IC.

The embodiment 90 comprises N=3 operational amplifiers 91 through 93. Here, all the operational amplifiers 91 through 93 share one common comparator 96. Due to the sharing, the self zeroing can only be performed on one amplifier stage at one time. To facilitate a stage-by-stage offset compensation, an input switch S10 and an output switch S9 are added. The isolation between two stages can be achieved as described above in connection with Figs. 5 or 6. In order to perform the self zeroing on the first operational amplifier 91 (OP1), for example, both switches S9 and S10 are put in position 1. If the switches S9 and S10 are in this position, a circuit is obtained that is similar to the one shown in Fig. 1. For N operational amplifiers, the saving that can be achieved is N-1 comparators, if compared to the embodiment of Fig. 7. The Fig. 9 shows a general case in which all stages are not necessarily in cascade. Consequently, self zeroing is done for each operational amplifier 91 through 93 each time the comparator 96 is connected to the output terminal 99.1 through 99.3 of one operational amplifier 91 through 93, via the switch S9. If several operational amplifiers are connected in series, such as in a high order filter for example, such an arrangement is not suitable because the residual errors of each stage would accumulate. A solution to overcome this problem is described in connection with Fig. 10.

(III) Sharing both comparator and SAR: Even more saving can be accomplished if the SAR unit is shared among several operational amplifiers. The apparatus 100 in Fig. 10 makes this possible. The SZC unit 105 comprises N=3 DACs 107 – 109 and N=3 D-Latches 110 – 112, but just one SAR 104 and one comparator 106. In this embodiment, only the output 113 of the operational amplifier 103 is connected to one of the inputs of the comparator 106. The other input of the comparator 106 is connected to analog ground. Comparing it with the apparatus 90 of Fig. 9, the input switch S10 and output switch S9 are no longer needed here. For a simple discussion of the principle, one K-bit DAC 107 through 109 is assumed for each of the N=3 operational amplifiers 101 through 103. Because the SAR 104 is shared among all operational amplifiers 101 through 103, D-latches 110 through 112, whose truth table is given below, have to be inserted between the SAR 104 and the DACs 107 through 109 in order to store data.

Truth table of D-Latches in Fig. 10		
D	Cp	Q
L	H	L
H	H	H
X	L	Qo

Preferably, the self zeroing process starts with the last operational amplifier 103 in the cascade and ends with the first operational amplifier 101. In order to compensate the 2nd operational amplifier in a chain of N=3 amplifiers, for example, the cp2 signal is set to be logic high (while all other signals cp1 and cp3 are logic low), and the input switch S12 is closed. With cp2 high, the added latch to the 2nd operational amplifier 102 is transparent, so that the output of the SAR 104 is directly applied to the DAC 108 of the 2nd operational amplifier. After the self zeroing of the 2nd stage, the cp2 goes logic low, and the output states of the latch 111 maintains until the next self zeroing on this operational amplifier 102 takes place. This strategy saves N-1 comparators as well as

N-1 SARs and it stops the error accumulation of the residual errors of each amplifier stage. It is a disadvantage that N D-latches 110 through 112 and a K-bit wide data bus 113 are needed. The principle of Fig. 10 can be extended to any number (N) of operational amplifiers.

Some important waveforms are shown in Fig. 11. These waveform can be used in connection with the apparatus 100 of Fig. 10. The Fig. 11 shows the signals clk, rst, cp1, cp2 and cp3.

While the strategy (I) takes only K clock cycles, the other two strategies (II) and (III) take N times K clock cycles. In order to reduce the required time, operational amplifiers can be grouped and for each group the best strategy can be chosen independently. This approach can yield best performance in terms of silicon area, required clock cycle time, and power consumption.

The architecture presented herein allows for high performance, low power circuits to be packaged in small form factors for today's demanding applications. It is well suited for filters, automated gain control circuits, and bandgap reference circuits.

It is a key issue that, according to the present invention, the zeroing is

done automatically and independently from any control or management circuit. All that is required is some kind of mode select signal (e.g., ms) that "triggers" the self zeroing process for a particular operational amplifier.

A circuit technique was presented that permits self zeroing for continuous-time applications. With the techniques presented herein, the overhead can be kept at a minimum while a high precision is preserved.

It is an advantage of the present invention that it works with operational amplifiers in an open loop or in a closed loop. It is another advantage of the invention presented herein, that it take only very few clock cycles for the compensation process.

It is a further advantage of the present invention that it requires only very few modifications of an existing circuit when adding the self zeroing means. The present invention allows a high degree of circuit element sharing, as addressed in connection with the examples given in Figures 8 through 10. According to the present invention, it is for example possible to share the SAR, leading to reduced costs and smaller silicon area being occupied by the offset compensation means.

The present invention does not require a specially designed current DAC, like the offset calibration approach described in the US patent 5,397,944. The scheme presented herein works for all kinds of DACs. The method presented herein can use a current or a voltage as a control signal (Vc) for the operational amplifier.

The present invention can be realized using standard library cells and there is thus no need for special circuits.

It is appreciated that various features of the invention which are, for clarity, described in the context of separate embodiments may also be provided in combination in a single embodiment. Conversely, various features of the invention which are, for brevity, described in the context of a single embodiment may also be provided separately or in any suitable sub combination.

In the drawings and specification there has been set forth preferred embodiments of the invention and, although specific terms are used, the description thus given uses terminology in a generic and descriptive sense only and not for purposes of limitation.

CLAIMS:

1. Apparatus (1; 10; 30; 50; 60; 70; 90; 100) for continuous-time application, comprising an operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103) and a self-zeroing control unit (3; 43; 63; 73; 95; 105) for reducing an offset of the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103), said self-zeroing control unit (3; 43; 63; 73; 95; 105) providing for the following two modes of operation

(a) self zeroing operation performing a self-zeroing process and

(b) normal operation

wherein the self-zeroing control unit (3; 43; 63; 73; 95; 105) comprises

- a comparator (6; 76; 96; 106),
- a successive approximation register (7; 77; 98.1 – 98.3; 104), and
- a digital-to-analog converter (8; 78; 97.1 – 97.3; 107 - 109).

2. The apparatus of claim 1, wherein the self-zeroing control unit (3; 43; 63; 73; 95; 105) is switcheable between the two modes by a mode select signal (ms).

3. The apparatus of claim 1, comprising switching means (S1, S2; S3 - S6) allowing the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103) during the self zeroing operation to be separated from a stage (31; 51), that precedes the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103).

4. The apparatus of claim 2 or 3, wherein the offset of the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103) is adjustable by an output voltage (Vc; Vc1 – Vc3) provided at an output (9; 79) of the digital-to-analog converter (8; 78; 97.1 – 97.3; 107 - 109).

5. The apparatus of claim 1 or 2, wherein the comparator (6; 76; 96; 106)

comprises a first input node and a second input node (22), the first input node being connected to an output (4; 44; 75; 99.1 – 99.3; 113) of the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103) and the second input node (22) being connectable to a reference voltage (Vb) or to analog ground.

6. The apparatus of claim 1 or 2, wherein the comparator (6; 76; 96; 106) is turned off when the mode select signal (ms) turns logic zero.

7. The apparatus of claim 3, wherein the switching means (S1, S2; S3 - S6) comprises switches being switchable by the mode select signal (ms) or the inverted mode select signal ($\overline{ms}$).

8. The apparatus of one of the preceding claims, wherein the comparator (76; 96; 106) and preferably the successive approximation register (77; 104) are shared by two or more operational amplifiers (71, 72; 91 – 93; 101 – 103).

9. Integrated circuit (IC), preferably a mixed-signal integrated circuit, comprising N operational amplifiers (62; 71, 72; 91 – 93; 101 – 103) with excessive offsets that have to be reduced, and M self-zeroing control units (63; 73; 95; 105) for reducing an offset of the operational amplifiers (62; 71, 72; 91 – 93; 101 – 103), with N ≥M, said self-zeroing control units (63; 73; 95; 105) providing for the following two modes of operation

(c) self zeroing operation performing a self-zeroing process and

(d) normal operation.

whereby at least one of the M self-zeroing control units (63; 73; 95; 105) comprises

- a comparator (76; 96; 106),
- a successive approximation register (77; 98.1 – 98.3; 104), and
- a digital-to-analog converter (78; 97.1 – 97.3; 107 - 109).

10. The integrated circuit (60) of claim 10 with N=M.

11. The integrated circuit (60) of claim 10 with M=1, whereby said self-zeroing control unit (95) comprises

- one comparator (96),
- N successive approximation registers, and
- N digital-to-analog converters.

12. The integrated circuit (100) of claim 10 with M=1, whereby said self-zeroing control unit (105) comprises

- one comparator (106),
- one successive approximation register (104),
- N digital-to-analog converters; and
- N D-Latches (110 – 112).

13. Method for performing a self-zeroing process in an integrated circuit that comprises an operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103) with excessive offset that has to be reduced by the self-zeroing process, and a self-zeroing control unit (3; 43; 63; 73; 95; 105) for reducing the offset of the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103), said method comprising the steps:

- applying a mode select signal (ms) to the self-zeroing control unit (3; 43; 63; 73; 95; 105),
- comparing an output signal of the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103) with a reference voltage (Vb) in order to provide a corresponding analog signal,
- providing the analog signal to an input (23; 83) of a successive approximation register (7; 77; 104) in order for this analog signal to be transformed into a digital signal, said digital output signal representing the value of the analog signal,
- applying this digital signal to a digital-to-analog converter (8; 78; 97.1 –97.3; 107 - 109) for generating an analog output signal (Vc),
- applying this analog output signal (Vc) to a node of the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103).

14. Method of claim 13, whereby the operational amplifier (2; 42; 62; 71, 72; 91 – 93; 101 – 103) is separated from a preceding stage of the integrated circuit when

performing the self-zeroing process.

15. Method of claim 13 or claim 14, whereby the self-zeroing process is carried out after a power-on event.

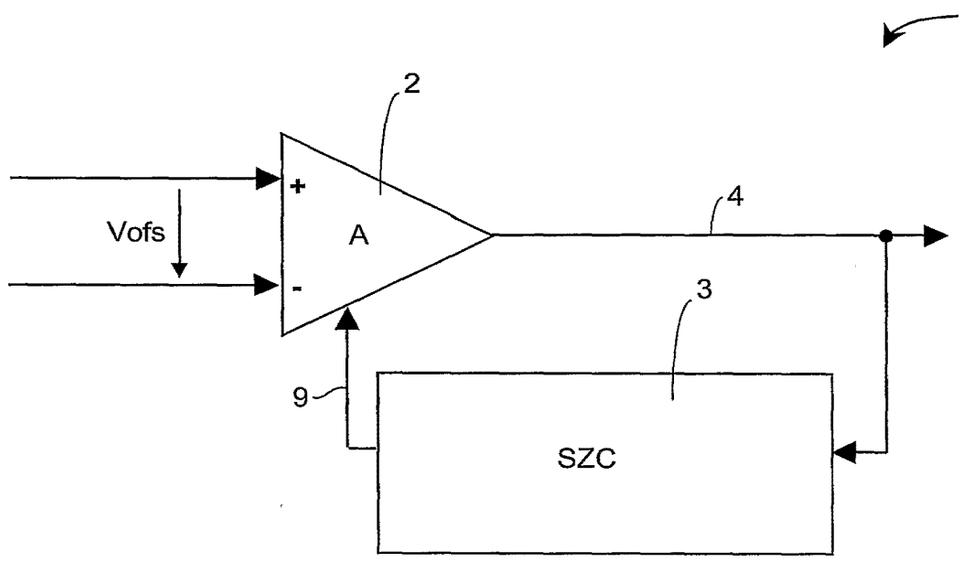

1
2
+
-
A
Vofs
4
3
9
SZC

Fig. 1

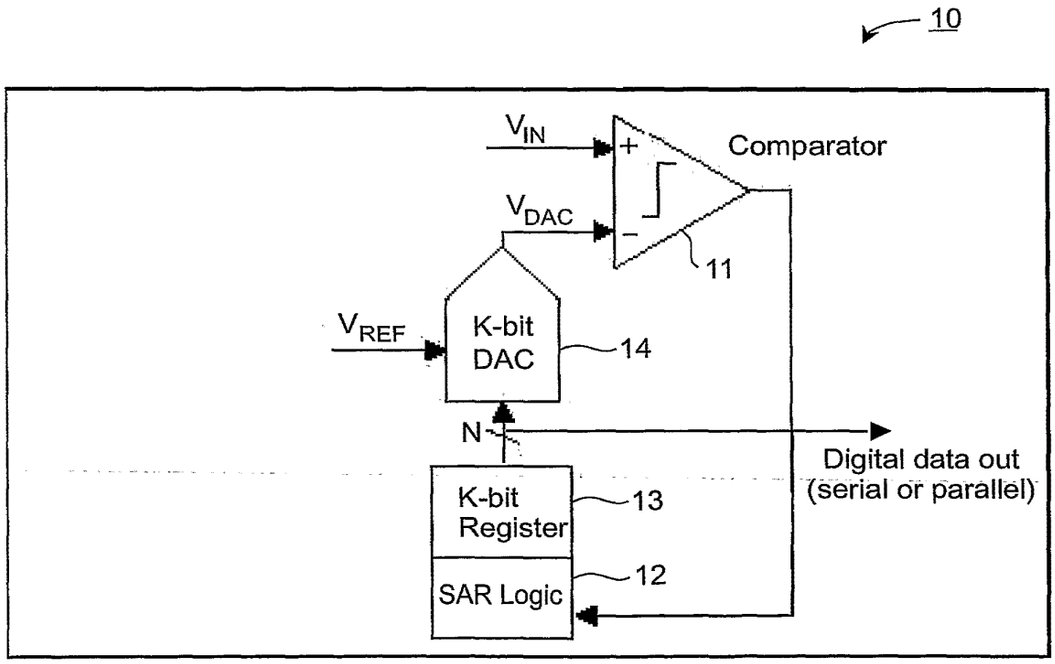

10
V_{IN}
V_{DAC}
+
-
Comparator
11
V_{REF}
K-bit
DAC
14
N
Digital data out
(serial or parallel)
K-bit
Register
13
SAR Logic
12

Fig. 2

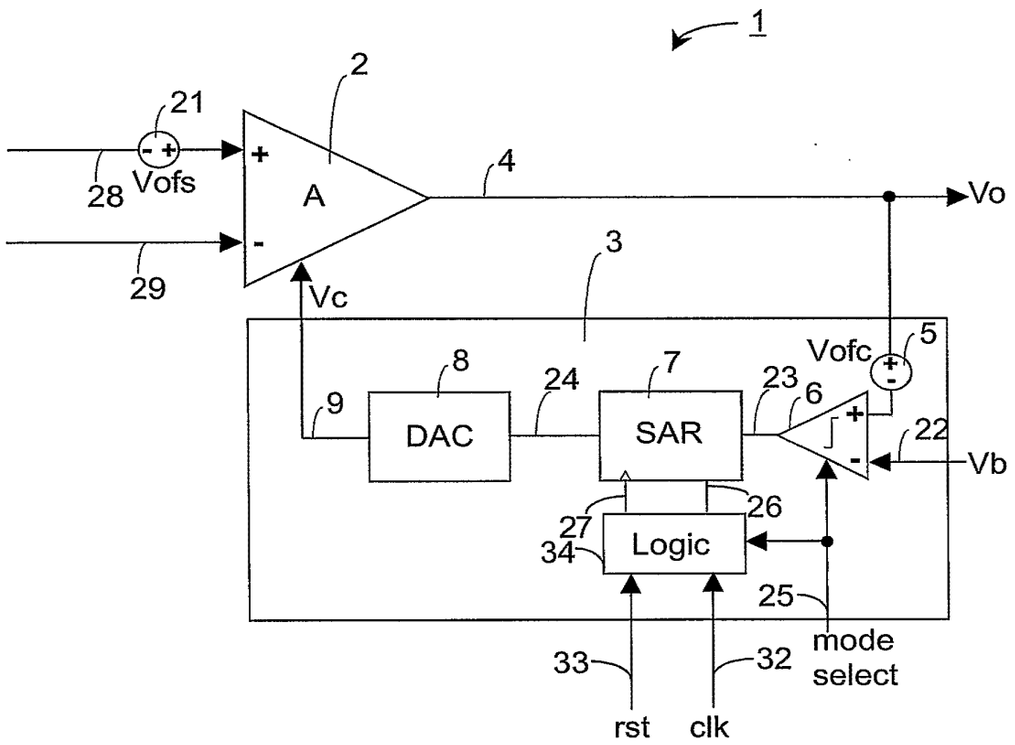

1
2
21
28
Vofs
A
4
Vo
29
3
Vc
Vofc
5
8
24
7
23
6
9
DAC
SAR
22
Vb
27
26
34
Logic
25
mode
select
33
32
rst
clk

Fig. 3

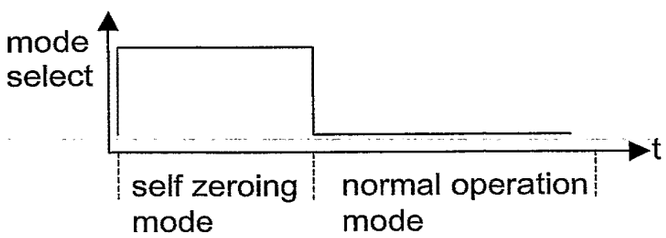

mode
select
t
self zeroing
mode
normal operation
mode

Fig. 4

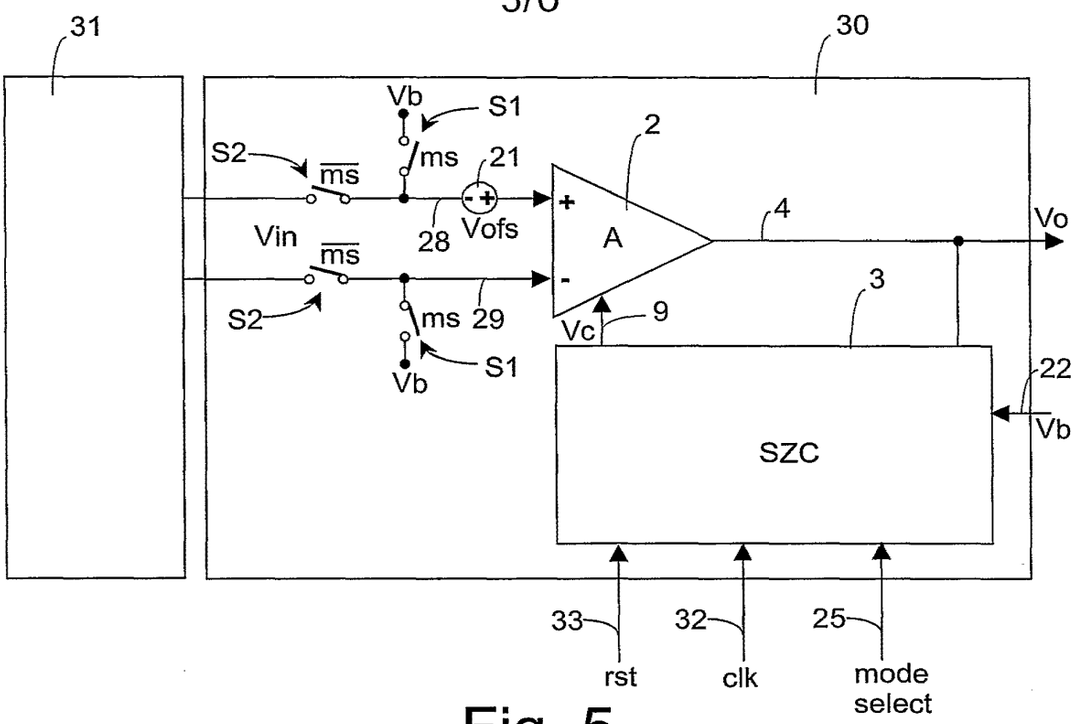

31
30
Vb
S1
S2
ms
21
2
+
-
A
4
Vo
Vin
28
Vofs
29
3
9
Vc
22
SZC
33
32
25
rst
clk
mode
select

Fig. 5

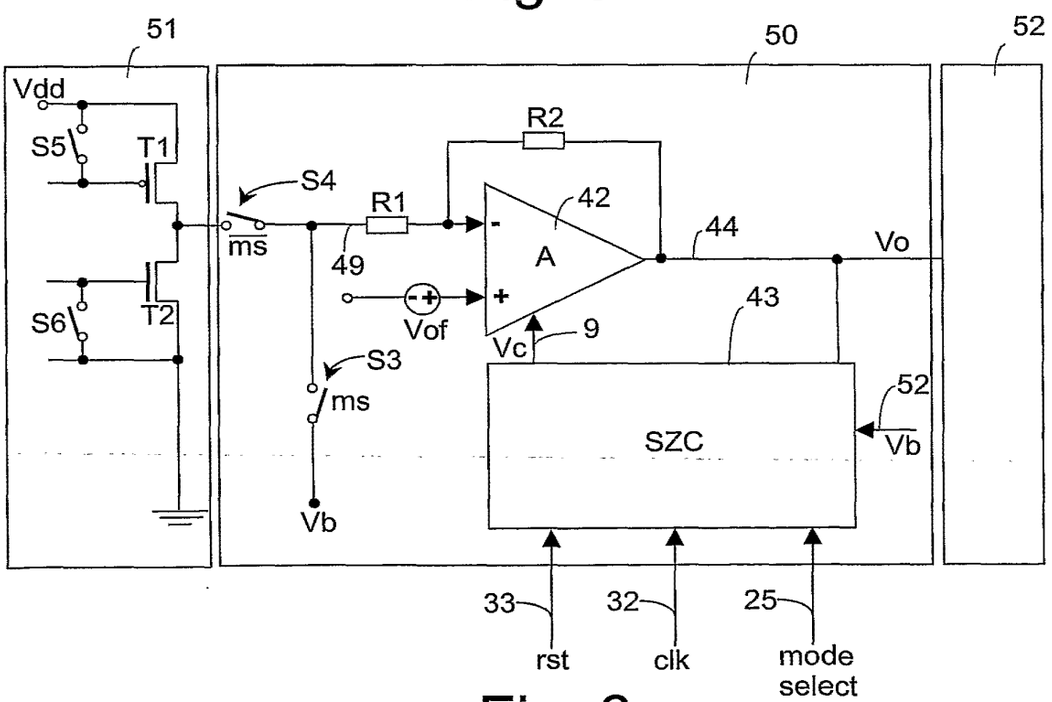

51
50
52
Vdd
S5
T1
S6
T2
S4
R1
R2
42
44
Vo
49
Vof
43
9
Vc
S3
52
SZC
33
32
25
rst
clk
mode
select

Fig. 6

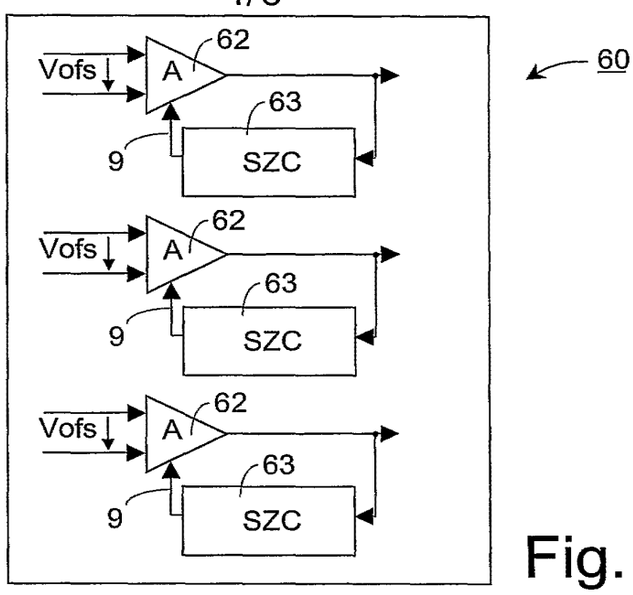

60
Vofs
A
62
63
SZC
9

Fig. 7

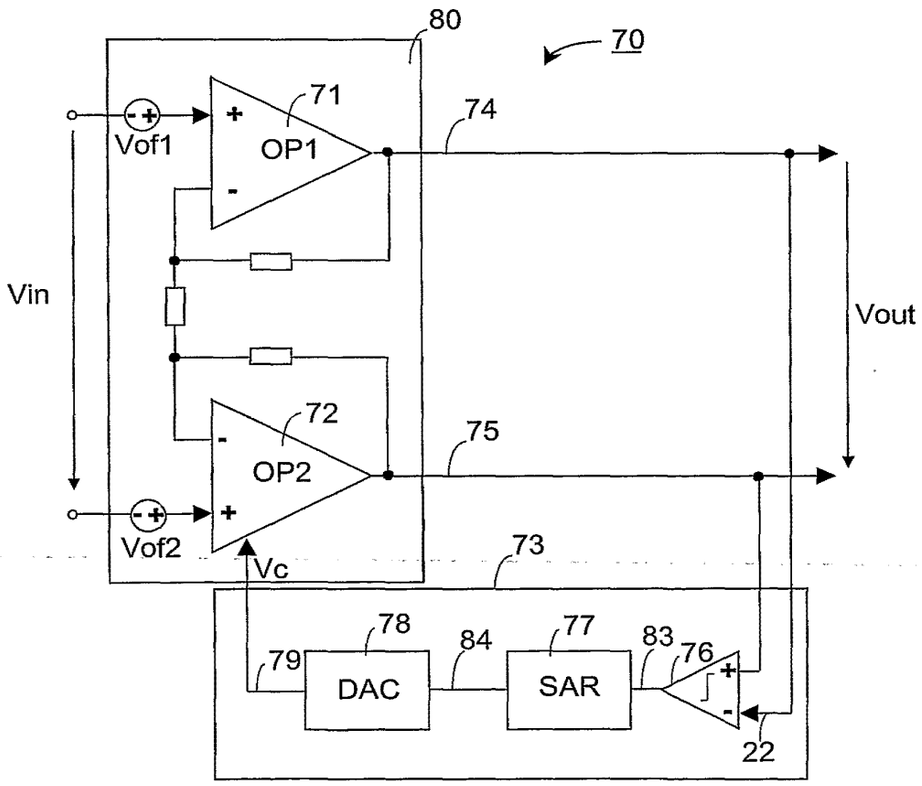

80
70
71
OP1
Vof1
74
Vin
Vout
72
OP2
75
Vof2
Vc
73
78
79
DAC
84
77
SAR
83
76
22

Fig. 8

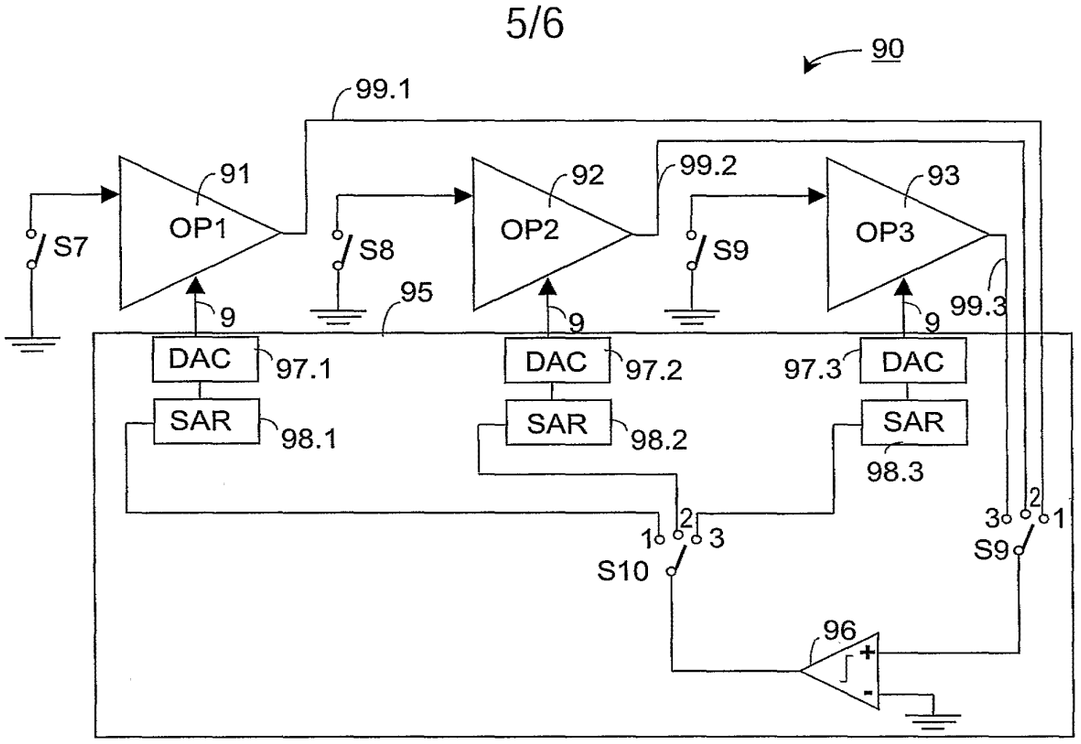

90
99.1
91
OP1
92
OP2
99.2
93
OP3
S7
S8
S9
95
9
99.3
DAC
97.1
97.2
97.3
SAR
98.1
98.2
98.3
1
2
3
S10
96

Fig. 9

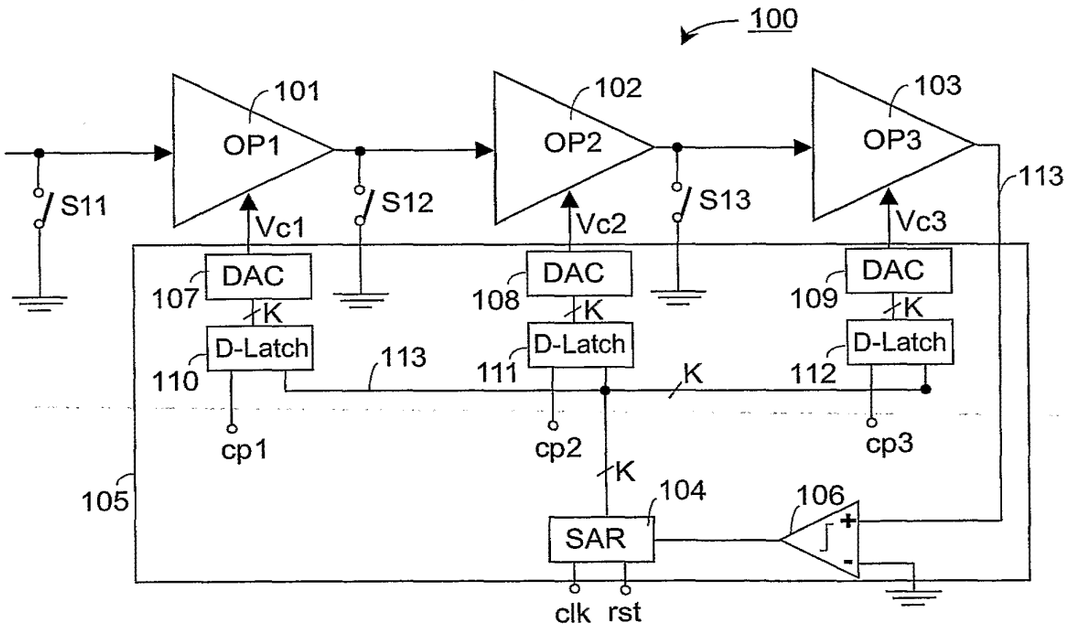

100
101
OP1
102
OP2
103
OP3
113
S11
S12
S13
Vc1
Vc2
Vc3
DAC
107
108
109
K
D-Latch
110
111
112
cp1
cp2
cp3
105
104
106
SAR
clk
rst

Fig. 10

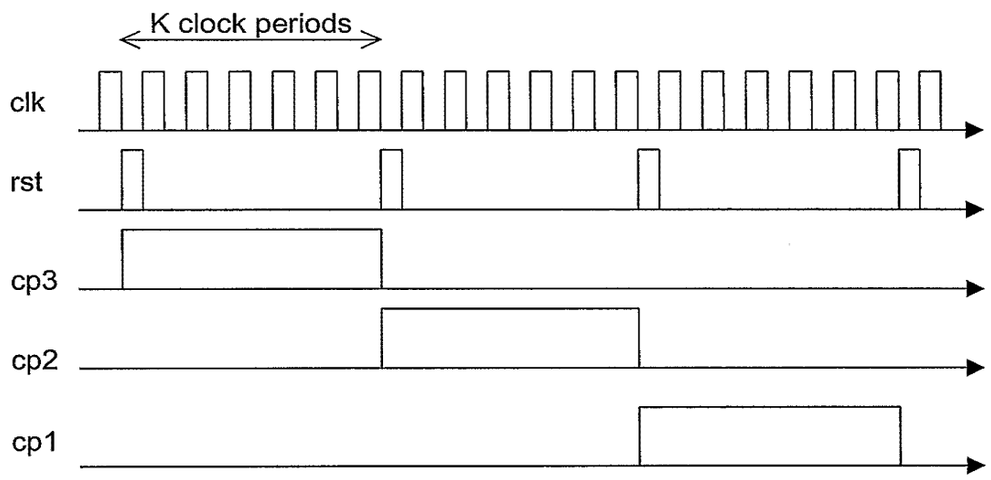


Fig. 11

INTERNATIONAL SEARCH REPORT

ational Application No
../IB2004/000318

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03F3/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
WPI Data, EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2002/186075 A1 (LLEWELLYN WILLIAM D) 12 December 2002 (2002-12-12) page 2, paragraph 26 -page 3, paragraph 39; figure 1 ---	1-15
X	KAYAL M ET AL: "Auto-zero differential difference amplifier" ELECTRONICS LETTERS, IEE STEVENAGE, GB, vol. 36, no. 8, 13 April 2000 (2000-04-13), pages 695-696, XP006015132 ISSN: 0013-5194 the whole document -----	1-15

[ ] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 May 2004	21/05/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lorenzo, C

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

tional Application No
/IB2004/000318

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002186075 A1	12-12-2002	WO 02087073 A2	31-10-2002

Form PCT/ISA/210 (patent family annex) (January 2004)

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For any questions about this communication:
Tel. +31 (0)70 340 45 00

Date
07.07.10

Reference	Application No /Patent No.
N 148EP	10153869.2 - 2215

Applicant/Proprietor
Number 14 B.V.

Communication

The partial European search report (R. 64 EPC) is enclosed.

The applicant is informed that if the European search report is also to cover inventions other than the invention(s) already searched and for which a meaningful search can be carried out, a further search fee must be paid for each of these inventions, in the present instance

5 search fee(s)

within **two months** after notification of this communication.

The amount payable for each further search is EUR 1105,00.

Note to users of the automatic debiting procedure
Unless the EPO receives prior instructions to the contrary, the fee(s) will be debited on the last day of the period for payment. For earlier payment(s) another method of payment must be used. For further details see the Arrangements for the automatic debiting procedure (see Supplement to OJ EPO 3/2009).

If applicable, a European search opinion covering those invention(s) for which a search fee has been paid will then be sent together with the European search report.

Copies of documents cited in the European search report are attached.

☑ 1 additional set(s) of copies of such documents is (are) enclosed as well.

The following have been approved:

☑ Abstract ☑ Title

☐ The Abstract was modified and the definitive text is attached to this communication.

The following figure(s) will be published together with the abstract: 9

Registered letter
EPO Form 1507U 04.10 (RTB)

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Following any amendment to the Rules relating to Fees, the amount(s) mentioned in this communication may be different from the amount(s) **actually due on the date of payment.** The latest version of the Schedule of fees and expenses, published as a Supplement to the Official Journal of the EPO, is also available on the EPO website (**www.epo.org**) and can be found under **www.epoline.org**, which allows the viewing, downloading and searching for individual fee amounts, both current and previous.

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PARTIAL EUROPEAN SEARCH REPORT

under Rule 64, paragraph 1 of the European Patent Convention

Application Number EP 10 15 3869

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	Marc Pastre, Maher Kayal: "Methodology for the Digital Calibration of Analog Circuits and Systems: with Case Studies (Kluwer International Series in Engineering and Computer Science)" 6 December 2005 (2005-12-06), Springer , Netherlands , XP002587083 ISBN: 1402042523 * page 12 - page 14; figure 10 * * page 23 - page 35 * * page 52 - page 62 * * page 106 - page 107; figure 75 *	1-3	INV. H03M1/06 H03F3/45

-/--

TECHNICAL FIELDS SEARCHED (IPC)

H03M
H03F

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

The present partial European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims.

Place of search	Date of completion of the search	Examiner
Munich	17 June 2010	Kurzbauer, Werner

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04E27)

ANALOG EXHIBIT 1002
Page 254 of 321

Europäisches Patentamt
European Patent Office
Office européen des brevets

PARTIAL EUROPEAN SEARCH REPORT

Application Number
EP 10 15 3869

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (IPC)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
X,P	MARC PASTRE ET AL: "Methodology for the digital calibration of analog circuits and systems using sub-binary radix DACs" MIXED DESIGN OF INTEGRATED CIRCUITS&SYSTEMS, 2009. MIXDES '09. MIXDES-16TH INTERNATIONAL CONFERENCE, IEEE, PISCATAWAY, NJ, USA, 25 June 2009 (2009-06-25), pages 456-461, XP031548289 ISBN: 978-1-4244-4798-5 * page 458, left-hand column - page 460, right-hand column *	1,2	
A	WO 2004/073163 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]; WANG ZHENHUA [DE]) 26 August 2004 (2004-08-26) * page 10, line 10 - line 17; figure 9 *	1-3	TECHNICAL FIELDS SEARCHED (IPC)
A	HANS GUSTAT: "A DC-10GHz amplifier with digital offset correction" MATERIALS SCIENCE IN SEMICONDUCTOR PROCESSING, PROCEEDINGS OF THE SECOND INTERNATIONAL SIGE TECHNOLOGY AND DEVICE MEETING (ISTDM 2004) KLEIST-FORUM, vol. 8, no. 1-3, 16 May 2004 (2004-05-16), - 19 May 2004 (2004-05-19) pages 439-443, XP002587084 Frankfurt (Oder), Germany * page 440, right-hand column - page 442, left-hand column; figures 1,2,4 *	1-3	
A	US 6 486 806 B1 (MUNOZ CARLOS ESTEBAN [US] ET AL) 26 November 2002 (2002-11-26) * column 6, line 16 - column 9, line 28; figures 2,3,4,5 *	1-3	
A	US 2003/214351 A1 (NANDY TAPAS [IN] ET AL) 20 November 2003 (2003-11-20) * the whole document *	1-3	

EPO FORM 1503 03.82 (P04C10)

ANALOG EXHIBIT 1002
Page 255 of 321

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-3

An amplifier system having an amplifier system input and an amplifier system output comprising: a first amplifier; a comparator;
a successive approximation register having an input coupled to an output of the comparator;
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;
an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier, wherein the radix is approximately 1.9 and the radix for the least significant bit is 2.

---

2. claim: 4

An amplifier system having an amplifier system input and an amplifier system output comprising: a first amplifier; a comparator;
a successive approximation register having an input coupled to an output of the comparator;
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;
an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier, wherein the D/A converter further comprises one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits.

---

3. claims: 5-8, 13-20

An amplifier system having an amplifier system input and an

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

amplifier system output comprising: a first amplifier; a comparator;
a successive approximation register having an input coupled to an output of the comparator;
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;
an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier, wherein the first amplifier has a first transconductance differential input stage coupled to the first amplifier input, and wherein the first amplifier is further comprised a second transconductance differential input stage, the outputs of the first and second transconductance differential input stages being coupled in parallel, the output of the D/A converter being coupled to inputs of the second transconductance differential input stage to divide a current source coupled to the second transconductance differential input stage between the differential outputs of the first transconductance differential input stage in a proportion to reduce the input offset of the first amplifier.

---

4. claim: 9

An amplifier system having an amplifier system input and an amplifier system output comprising: a first amplifier; a comparator;
a successive approximation register having an input coupled to an output of the comparator;
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;
an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier, further comprised of One-Time-Programmable memory

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

for permanently storing an output of the successive approximation register, whereby a single output of the D/A converter controlling the input offset of the first amplifier may be permanently maintained.

---

5. claim: 10

An amplifier system having an amplifier system input and an amplifier system output comprising: a first amplifier; a comparator;
a successive approximation register having an input coupled to an output of the comparator;
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;
an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier,further comprised of a second amplifier, the first switch coupling the amplifier system input to an input of the second amplifier when shorting the input to the first amplifier, the second switch coupling an output of the second amplifier to the amplifier system output when switching the output of the first amplifier from the amplifier system output to an input of the comparator.

---

6. claims: 11, 12

An amplifier system having an amplifier system input and an amplifier system output comprising: a first amplifier; a comparator;
a successive approximation register having an input coupled to an output of the comparator;
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier, wherein the D/A converter comprises a common reference line, and at least in part, resistor ladders symmetrical about the common reference line, and third switches for selectively switching equal current sources to ladder nodes on either side of the common reference line responsive to the successive approximation register, the resistor ladders being R(p-1),Rp/(p-1) ladders, where p is less than 2.

The common subject matter of all above claims or groups of claims is an amplifier system having an amplifier system input and an amplifier system output comprising: a first amplifier; a comparator; a successive approximation register having an input coupled to an output of the comparator;
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;
a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator;
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;
an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

The reduction of the radix of an SAR is known in the art and e.g. discussed in the book Pastre, Kayal,"Methodology for the digital calibration of analog circuits and system", Springer 2006, which discloses in detail an amplifier system having an amplifier system input and an amplifier system output comprising: a first amplifier; a comparator;
a successive approximation register having an input coupled to an output of the comparator (cf. page 13, Fig.10);
a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input (cf. page 13, Fig.10: Sin);
an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter (cf. page 13, Fig.10: DAC);
the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits (cf. p23, chapt.1,2, p.24, chapt.3, p.31, chapt.4.1-4.3 and page 35, lines 16-18);
an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier (cf. p23, chapt.1,2)
The only difference between the common subject matter and the subject matter as disclosed in the prior art is a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator.
The common objective problem in the light of the known subject matter is

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

thus how to disconnect the amplifier from the comparator.
The solution to this problem does not provide an inventive step as despite the principle circuit depicted on page 13 fig.10 does not show such a switch, a skilled person would realize that even though once the offset calibration has been performed the output of the operational amplifier is still unnecessarily loaded by the comparator input and he would simply add such a switch in order to disconnect the comparator input from the amplifier once the offset calibration has been performed.
Therefore the above stated common subject matter does not provide a common inventive concept as required by Article 82 EPC.
The additional features claimed in the various claims or groups of claims (i.e. addition of an additional bit, input structure of the operational amplifier to be compensated, output structure of the operational amplifier to be compensated, storage of the conversion result, structure of the D/A converter) do not provide features which are dependent on the reduction of the radix of an SAR but are also applicable to a usual radix 2 converter.

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 10 15 3869

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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17-06-2010

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2004073163 A1	26-08-2004	CN 1748362 A	15-03-2006
		JP 2006517765 T	27-07-2006
		KR 20050101201 A	20-10-2005
		US 2006244520 A1	02-11-2006
US 6486806 B1	26-11-2002	NONE	
US 2003214351 A1	20-11-2003	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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Materials Science in Semiconductor Processing 8 (2005) 439–443
MATERIALS SCIENCE IN SEMICONDUCTOR PROCESSING

A DC–10 GHz amplifier with digital offset correction

Hans Gustat*

IHP, Circuit Design Department, Im Technologiepark 25, D-15236 Frankfurt (Oder), Germany

Available online 13 October 2004

Abstract

This work presents a SiGe:C wideband amplifier with a binary CMOS counter for digital offset adjustment. The application of the "radix < 2" approach to accurate offset correction in a digital calibration loop results in smaller area and less power than common static high-resolution offset correction circuits. The counter bits are weighted with a radix of 1.6, leading to 25% error tolerance, and thus simple circuits and small devices. A BiCMOS test chip in a 0.25-μm-CMOS 200-GHz-SiGe:C technology exhibits a correction accuracy well below the measurement noise floor of 50 μV at only 1 mW additional power consumption. The amplifier operates from DC to 10 GHz on a 3 V supply voltage. Since the adjustment compensates device mismatch, minimum-size transistors can be used. This in turn enhances the RF performance.
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Keywords: SiGe technology; BiCMOS amplifier; Wideband amplifier; Offset correction; Digital calibration; RF amplifier; Non-binary radix; High resolution; Low power; Error tolerance

1. Introduction

Integrated circuits fabricated in BiCMOS technology are often wireless systems consisting of a large fraction of digital CMOS circuitry, mainly for the baseband part of the system, and a much smaller analog area containing primarily RF functions. For example, a recent single-chip 5 GHz-modem fabricated in the IHP SiGe:C BiCMOS technology contains 3 million transistors, with only 502 bipolars [1].

On the other hand, adding CMOS logic to analog bipolar systems can provide a high additional value, too. Here, the digital fraction is much smaller. Digital control can provide a new level of analog performance, for example self-adjustment or even complex optimization as presented in [2]. Adding CMOS logic functionality to high-performance bipolar circuits is therefore another promising area for BiCMOS technology.

2. Self-adjustment to relax process dependence

Many analog circuits rely heavily on process-dependent parameters, such as device mismatch, long-term stability or temperature drift. Therefore, commercial analog chips are often fabricated in a conservative technology with less density and performance than the state of the art, because a mature process is essential for the yield. Self-calibration functions added to analog circuits can greatly relax this dependency on tight process tolerances, allowing to use leading-edge technology for any kind of analog circuits. Once an analog system is redesigned for self-adjustment, migration towards more advanced technologies can keep pace with the process scaling, similarly to digital designs. Thus, self-adjustment provides a key to simplified scaling of analog circuits.

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Analog self-calibration is very common in low-frequency circuits, for example in chopper or auto-zeroing amplifiers. In addition to offset, many more analog parameters could be self-calibrated, e.g. gain, impedance matching, transfer characteristics, circuit symmetry or resonant frequency. This could not only simplify the adaptation to technology scaling, but also improve yield and lead to new levels of performance. This potential is still not much exploited.

2.1. Different refresh time scales

One reason for this lag may lie in the high repetition rate required for the refresh of the volatile storage of the correction values. If the correction value generated by the analog feedback loop is stored on a capacitor, the droop rate of the stored value requires periodic refresh within about a millisecond or less, depending on temperature and accuracy. Many analog systems cannot tolerate high refresh rates. The refresh can generate unwanted spectral components in the signal. Further, continuous operation may not be interrupted for the full length of a data transmission.

In most cases, a high refresh rate is only caused by capacitive storage. From the viewpoint of parameter change due to drift or temperature dependence, the desired refresh period is much larger, in the region of seconds or more. To balance process variations, even power-up adjustment is sufficient. Repeated adjustment at a very low rate is acceptable for many applications. It demands static storage of the analog values in the digital domain. Two conversions must be inserted in the calibration loop: an A/D conversion to obtain the digital value, and a D/A conversion to feed it back to the analog circuit. The first conversion is easily carried out by a binary counter in a correction loop with an analog comparator, e.g. in [3]. The counter value also serves as the digital memory. The second conversion is usually performed with a D/A converter (DAC).

2.2. Precise digital adjustment at low cost

For highly accurate calibration, the DAC imposes strong requirements either on process parameters or on chip area. For instance, the smallest published 14-bit DAC still requires 0.1 mm^2 of core chip area and 20 mW power consumption [4], involving another calibration DAC in itself. This makes calibration of simple analog circuits expensive both in power and area. The problem becomes more important if multiple circuits per chip are to be corrected, since the DACs have to operate continuously, and can hardly be shared.

In fact, a true DAC is not required to convert the digital value back to analog. Even an overall monotonicity is not necessary. The counter-based correction loop already has the intrinsic ability to cope with large weighting errors, as long as all the steps larger than one LSB are pointing to the negative direction of the transfer curve. If a DAC can be replaced by a simple small weighting circuit, digital adjustment at high accuracy is possible on small area and at very low power consumption. This would allow a much wider application range of self-calibration, including simple RF circuits, e.g. amplifiers and mixers.

Sufficiently small positive steps demand the effective weighting radix $r_{\mathrm{eff}} = r(1 + e_r)$ of each weighting element to be less than two in any case. Here, e_r is the relative error of the weight r of a weighting element. If $e_{\max}$ is an upper limit to e_r, then it is sufficient to design the weighting radix r of an element as

$$r = 2/(1 + e_{\max}). \tag{1}$$

With a value of r significantly below two, large relative errors are tolerated, allowing simple circuits and small devices. Together with the binary input, this non-binary radix generates intentional negative steps in the transfer curve. On the other hand, it limits the positive steps to an LSB value of the weighting block. The bit width of the counter determines the resolution of the adjustment. Such a weighting block with an asymmetric dynamic non-linearity (DNL) is not a true DAC anymore, because it has a non-linear characteristic with large negative steps, even in the ideal case. In a DAC, DNL is usually caused by errors rather then imposed by design.

Due to the smaller radix, the non-linear weighting block needs a slightly wider counter than a DAC. Thereby, the calibration speed is reduced. Digital adjustment is mainly aimed at calibrating at large time intervals, e.g. to cope with process variations or to track temperature changes.

Though weighting with a radix less than two is well known in some fields, it is not yet common practice in analog RF applications. In this work, the non-binary weighting approach is applied to digitally adjust the offset voltage of a SiGe:C wideband amplifier.

3. Offset voltage correction of a wideband amplifier

In analog systems, DC offset voltage is one of the key parameters. Low DC offset is important for many applications in low-frequency regions, but also in RF systems. In the latter, even perfect device matching would not solve the problem, because DC offset can be caused by various sources within the system, e.g. RF leakage of the local oscillator frequency [5,6], and shall thus be adjusted at the system level.

The test chip provides precise DC offset adjustment based on CMOS circuitry to a bipolar wideband amplifier for operation from DC up to 10 GHz.

BNSDOCID: <XP 2587084A I >

ANALOG EXHIBIT 1002
Page 263 of 321

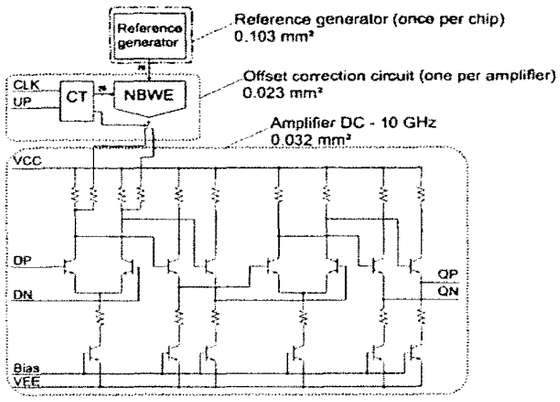


Fig. 1. Amplifier circuit and offset correction blocks.

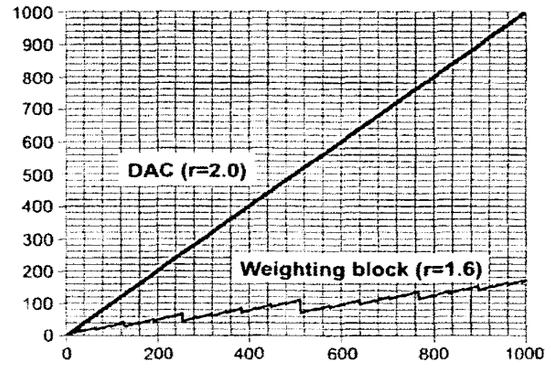


Fig. 2. Ideal transfer curves of a DAC and of a non-linear weighting block with $r = 1.6$.

Fig. 1 shows the simplified circuit of the bipolar wideband amplifier, together with the blocks for offset correction. The binary counter has a 20-bit output to control the non-binary weighting elements. Another control signal sets the polarity of the offset correction by switching the correction current to one or the other branch of the differential amplifier stage. The weighting elements are minimum-sized transistors biased by a chain of equal MOS current mirrors with a ratio of r. In the test chip, the weighting value r is 1.6, resulting in an output range of about 12100 LSB, which corresponds to 13.6 binary bits.

The big advantage of the non-binary weighting compared to a binary DAC is the greatly improved tolerance to device mismatch in the weighting element. The radix of 1.6 guarantees that positive steps in the weighting transfer curve are definitely smaller than 1 LSB, as long as the device error is less than 25%. On the other hand, it causes substantial non-linearity of the offset correction circuit by introducing large negative steps into the transfer curve.

Fig. 2 compares the ideal transfer curves of a DAC and of a weighting block with a radix of 1.6 for each weighting element.

Together with the counter in the loop, the negative steps do not affect the correction accuracy. The counter will continue counting up until the desired correction value is reached. Negative steps will only increase the counting time, but do not prevent to achieve the desired value with an accuracy of better than 1 LSB.

The test chip was fabricated in the SGC25C technology of the IHP (0.25-μm CMOS; SiGe:C BiCMOS with $f_t = 200$ GHz, $f_{max} = 200$ GHz [7]). In Fig. 3, the chip areas for the different blocks of Fig. 1 are marked. The largest chip area is devoted to generating reference voltages for biasing the current sources. In a multi-amplifier chip, the reference block would appear only once. To distinguish it from the parts required per input channel, the reference block in Figs. 1 and 3 enclosed by dashed–dotted lines.

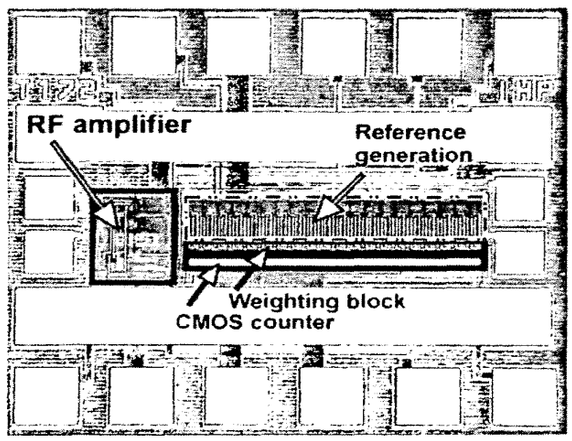


Fig. 3. Chip micrograph.

4. Measured results

4.1. DC performance

Fig. 4 illustrates the measured behavior during adjustment. It shows an oscilloscope plot of the test chip in permanent correction mode, i.e. the counter is continuously counting upwards for demonstration. In a true offset correction, the counter would stop counting upwards when both output signals are crossing. The gray line shows the negative output of the amplifier, and

BNSDOCID: <XP 2587084A 1 >

ANALOG EXHIBIT 1002
Page 264 of 321

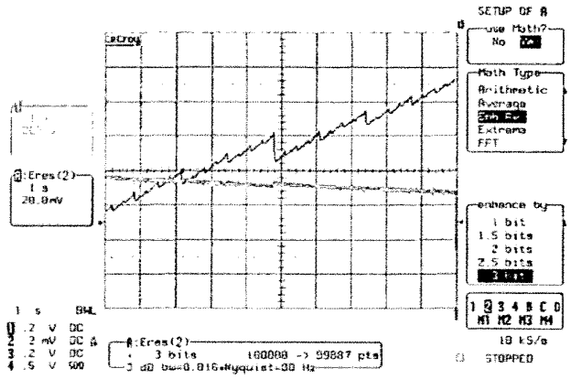


Fig. 4. Oscilloscope plot during the correction mode.

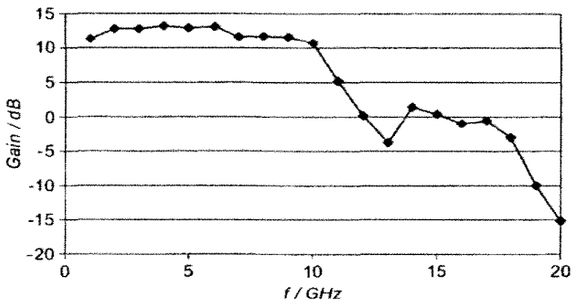


Fig. 5. Measured preamplifier frequency response.

Table 1
Measurement results for the wideband amplifier test chip

Total test chip area	1.3 mm^2
Core area of the amplifier	0.032 mm^2
Core area of offset correction blocks required per amplifier	0.023 mm^2
Core area of the reference block	0.103 mm^2
Technology	IHP SiGe:C BiCMOS (0.25 µm; 200/200 GHz [7])
Supply voltage	−3 V
Power consumption	67 mW
Power consumption for offset correction	1 mW
Bandwidth	10 GHz
Offset correction step size	< 3.3 µV
Measured offset correction accuracy	< 50 µV (noise limited)

the black line shows the positive output at a ten times larger magnification. Large negative steps of the positive output occur at regular intervals, where the more significant bits (MSB) of the counter are toggling.

Each MSB transition from one to zero causes a negative step. Higher bits cause larger steps. The positive steps remain small, so that any value can be reached with a low positive slope.

On the time scale, one grid division in Fig. 4 represents 50,000 calibration steps. The calibration circuit is designed to achieve about ±20 mV offset variation, allowing to calibrate even the large offset of a CMOS amplifier. Bipolar SiGe:C transistors are used here because of superior RF performance. Thus, the counter width could be reduced for this application. The adjustment accuracy of the 20-bit loop with $r = 1.6$ equals that of a conventional loop using a 14-bit DAC with an effective number of bits (ENOB) of 13.6. This corresponds to an offset correction down to 3.3 µV. The average step size is below 1 µV. These small steps were hidden in the 50 µV noise floor of the measurement setup.

4.2. RF performance

The wideband gain of the preamplifier has been measured using an HP spectrum analyser E4407B and a R&S signal generator SMR40. The resulting curve in Fig. 5 shows a bandwidth of about 10 GHz. All measurements have been done with the chip wire-bonded on a board. The external elements such as bond wires and connectors cause irregularities in the frequency response. Though the amplifier is fully differential, the RF measurements have been carried out single-endedly, i.e. the curve shows 3 dB less than the differential gain. Since the DC offset adjustment is separated by large resistors from the RF signal path, it does not reduce the bandwidth. Table 1 gives a survey of the measured parameters.

The resulting amplifier combines a bandwidth of 10 GHz based on 200-GHz SiGe:C HBT transistors with a digitally adjustable offset at a resolution of about 3 µV. This circuit is well-suited for applications where both speed and DC accuracy are important. The correction loop is not closed within the amplifier, so that further stages can be included within the loop, to calibrate at the system level. As a side effect of offset correction, the input transistors are minimum-sized, because device matching is not critical, Thus, the input capacitance is below 0.05 pF (without pads), enhancing the RF properties of the system.

This test chip illustrates the benefits of applying non-binary digital adjustment to RF circuits. With the growing availability of dense CMOS logic cells together with high-performance bipolar transistors, accurate self-calibration at low cost is beneficial for various parameters of RF circuits.

BNSDOCID: <XP 2587084A I >

ANALOG EXHIBIT 1002
Page 265 of 321

5. Conclusion

The offset voltage of a wideband amplifier can be accurately adjusted in a digital calibration loop using a smaller area and less power than common high-resolution offset correction circuits. The usual DAC can be replaced by a simple error-tolerant non-binary weighting element. A BiCMOS test chip exhibits a correction accuracy well below the measurement noise floor of 50 μV at only 1 mW additional power consumption. The accuracy of the DC correction does not deteriorate at a device mismatch of up to 25%. The bipolar SiGe:C amplifier operates from DC to 10 GHz on a 3 V supply voltage. Since device matching is not critical anymore, minimum-size transistors can be used throughout the design, improving the RF behavior.

Acknowledgement

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During the second phase, the amplifier is used in its normal processing configuration. The autozero capacitor is connected so that it cancels the effect of the parasitic voltage source.

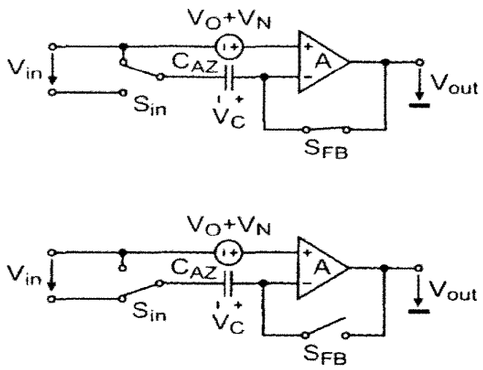


Figure 8. Autozero amplifier principle
Top: Sampling phase; *Bottom*: Processing phase

4.2 Analysis

The circuit presented in figure 8 does not correspond to the usual implementation of an autozero amplifier. There are actually more convenient ways to realize the same functionality.

For this example topology, the offset and the noise voltages are stored in a capacitor. Usually, their magnitude is smaller than 10 mV. The switches are implemented as transmission gates (see figure 6), or simply as single transistors. Therefrom arises one important problem due to the imperfections of MOS switches. When such a switch is opened, the well-known charge injection [8] phenomenon occurs. The charges that remain in the channel of the transistor flow into its source and drain, causing an undesired voltage variation across the sampling capacitor.

There are techniques for reducing charge injection. One can take special care when designing the switches, reduce the slope of the clock signal that triggers the switch, increase the size of the capacitor, etc. Nevertheless, this effect cannot be cancelled completely and it is difficult to manage when the signal level to which it is compared is small, like the 10 mV stored in C_{AZ}. It is thus advantageous to increase the voltage V_C in order to limit the effect of charge injection. But this cannot be achieved using this topology.

BNSDOCID: <XP 2587083A I >

ANALOG EXHIBIT 1002
Page 267 of 321

Figure 9 presents another autozeroed amplifier, for which charge injection is less problematic. In this circuit, the amplifier has an additional input Z used for offset nulling. During the offset sampling phase, the feedback loop including an auxiliary gain/attenuation stage A' and the sample and hold circuit adjusts the nulling signal so that V_{out}, and consequently also the amplifier offset, become null. The compensation value is then held during the second phase when the circuit is in the normal amplification mode.

The advantage of this technique over the one described before (figure 8) is that the signal level in the offset storage capacitor can be arbitrarily increased. It depends on the gain of the nulling input of the amplifier.

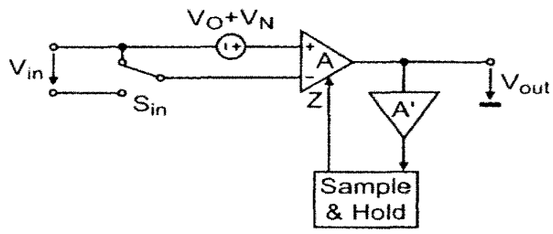


Figure 9. Analogically compensated autozero amplifier

Using the same topology, one can perform the offset cancellation in the digital domain with the circuit of figure 10.

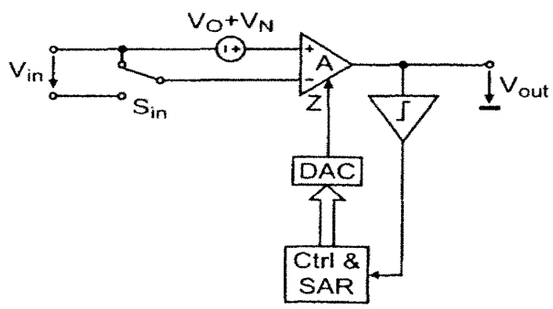


Figure 10. Digitally compensated autozero amplifier

The sample and hold circuit is in this case a digital-to-analog converter, which is controlled by a digital circuit performing successive approximations (see also section 3 in chapter 3). Since the information necessary to decide

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whether the value of the DAC is too large or not is the sign of V_{out}, the gain/attenuation stage of the previous fully analog circuit is here a comparator.

The advantage of the digital approach is that it allows the compensation information to be stored during an unlimited time, whereas the analog sample and hold memory used in the analog solution needs periodic refreshing. However, this is an advantage only if one considers one-time calibration. In the case of periodic offset nulling, which is interesting because it also cancels 1/f noise, the attractiveness of the digital solution diminishes. On the other hand, the problem of charge injection, which is one of the limitations of the analog solution, is not present if a digital compensation is implemented. In this case, the quality of the compensation depends on the resolution of the DAC.

4.3 Noise

If the autozero process is carried out at a sufficiently high frequency, it also reduces the low-frequency 1/f noise. A detailed analysis of the effect of autozero on noise can be found in [6]. This section presents only the most important results.

The resulting noise after autozero S_{AZ} has two components: the remaining baseband noise below the autozero frequency f_{AZ} (period T_{AZ}), and a foldover component which is aliased to the baseband because of the noise sampling that is done by the autozero process:

$$S_{AZ}(f) = S_{base}(f) + S_{fold}(f) = |H_0(f)|^2 S_N(f) + \sum_{\substack{n=-\infty \\ n\neq 0}}^{n=\infty} |H_n(f)|^2 S_N(f - nf_{AZ}) \tag{2.3}$$

with

$$|H_n(f)|^2 = \begin{cases} \left(1 - \dfrac{\sin(2\pi f T_{AZ})}{2\pi f T_{AZ}}\right)^2 + \left(\dfrac{1-\cos(2\pi f T_{AZ})}{2\pi f T_{AZ}}\right)^2 & n = 0 \\ \dfrac{\sin(\pi f T_{AZ})}{\pi f T_{AZ}} & n \neq 0 \end{cases} \tag{2.4}$$

In equations 2.3 and 2.4, S_N and S_{AZ} are the power spectral density of the noise without and with autozero respectively. S_{base} and S_{fold} are the power spectral densities of the baseband and the foldover noise contributions. H_0 is the noise transfer function in the baseband, and H_n ($n \neq 0$) is the transfer func-

BNSDOCID <XP 2587083A I >

ANALOG EXHIBIT 1002
Page 269 of 321

Chapter 3

Digital compensation circuits and sub-binary digital-to-analog converters

This and the next chapter present a complete methodology for digital compensation of analog circuits. In chapter 3, all the necessary circuits are presented. Chapter 4 focuses on the design methodology for digitally compensated circuits. The techniques and circuits presented are based on successive approximations algorithms. After an introduction to the algorithm and its working condition, sub-binary digital-to-analog converters are presented. As successive approximations algorithms neither require monotonic nor linear converters, it is possible to design very high-resolution sub-binary DACs with limited design effort. Different sub-binary topologies are described in this chapter, in particular the current-mode $M/2^{+}M$ converter.

1 INTRODUCTION

Among the compensation techniques presented in chapter 2, the digital correction is the most versatile. Without requiring major adaptations, it can be used in a large variety of situations to compensate for analog circuit imperfections.

This chapter presents successively all the elements needed for digital compensation. First, the successive approximations algorithm is presented. Then, different structures of digital-to-analog converters that can be used in conjunction with this algorithm are studied and their performance compared.

2 DIGITAL COMPENSATION

To foster understanding, this chapter refers to digital compensation on the basis of the example presented in figure 17, unless otherwise specified. The circuit is the same as in figure 10.

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ANALOG EXHIBIT 1002
Page 270 of 321

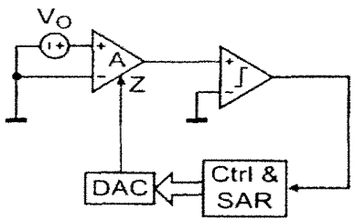


Figure 17. Digital compensation of the offset of an operational amplifier

The sign of the offset voltage V_O of the amplifier A is detected using a comparator connected to its output. The amplifier has an extra analog offset nulling input Z, which is considered positive[1] by convention. It can be a voltage, a current, or another physical quantity, but remains here without unit to keep the presentation as general as possible.

The feedback loop between the output of the comparator and the correction input is the digital compensation circuit. The digital information available at the output of the comparator, namely the sign of the offset, is sufficient[2] to allow complete offset cancellation. If the offset is positive, the correction circuit decreases it by diminishing the Z input value. Conversely, if the sign is negative, Z is increased.

On this basis, it is possible to design a compensation circuit consisting of an adapted algorithm realizing the function described above and a digital-to-analog converter driving the compensation input. This chapter analyses these blocks and presents the simplifications and optimizations that can be made.

3 SUCCESSIVE APPROXIMATIONS

The successive approximations algorithm allows to find quickly a digital value by dichotomic search. By performing a sequence of comparisons, it converges to the desired value. The algorithm is presented here as a means for calibrating circuits. However, it has other well-known applications, in analog-to-digital converters for example [7].

Let's consider that the DAC of figure 17 is an ideal binary-radix digital-to-analog converter with n bits of resolution. It has a digital input bus D, consisting in n digital inputs (d_1, ..., d_n), where d_1 corresponds to the least significant bit (LSB) and d_n to the most significant bit (MSB). The analog output value A

1. i.e. increasing the input value Z increases the offset voltage V_O.

2. because the relation between Z and V_O is a strictly monotonic function.

BNSDOCID: <XP 2587083A I. >

ANALOG EXHIBIT 1002
Page 271 of 321

of the DAC for each bit is b_1, ..., b_n. They are binary weighted and perfectly linear, and $b_1 = 1$ arbitrarily. Consequently:

$$b_i = 2^{i-1} \qquad \forall i \in [1 \ldots n] \tag{3.1}$$

The output of the DAC for a digital input word D is:

$$A = \sum_{i=1}^{n} d_i b_i \tag{3.2}$$

with $d_i = 0$ if bit i is cleared, and $d_i = 1$ if bit i is set.

The input/output characteristics of such an ideal DAC with 4 bits (n = 4) is shown in figure 18. The grey line is the identity function y = x.

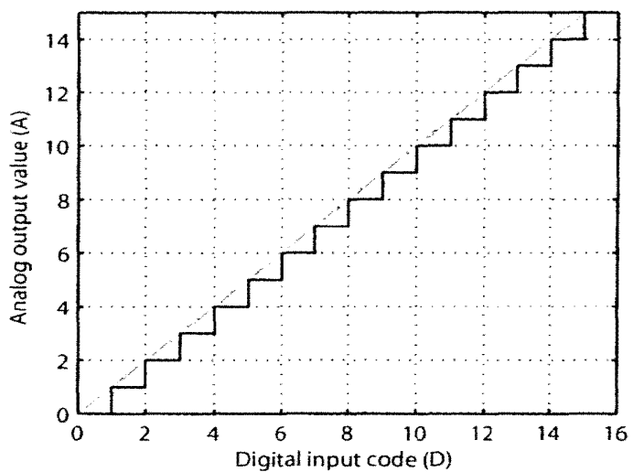


Figure 18. Ideal 4-bits DAC input/output characteristics

3.1 Principle

In the example of section 2, the goal of the algorithm is to find the most suitable digital control value for the DAC which produces the smallest residual offset.

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To keep the reflection as general as possible and to simplify the presentation, the offset voltage is not represented directly. Instead, an equivalent compensation value Z_0 is used, which corresponds to the necessary correction value generated by the DAC in order to completely cancel the offset. This is strictly equivalent since there is a direct relation between the nulling input Z and the input-referred offset of the amplifier.

In figure 19, Z_0 is set at 10.5 and plotted in grey. This number has voluntarily no unit (see section 2). If the DAC generates a compensation value above Z_0, the resulting offset is positive and the output of the comparator is also positive. If the compensation value is below 10.5, the output of the comparator becomes negative.

To find the DAC code that lies closest to Z_0, the successive approximations algorithm (figure 20) is used.

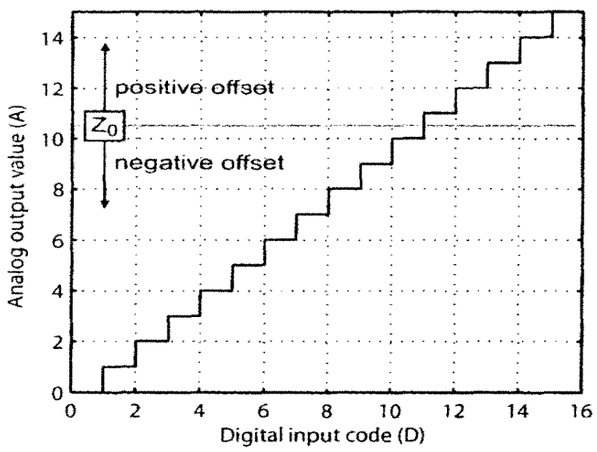


Figure 19. Equivalent offset

```
reset all di = 0
for i = n downto 1
  set di = 1
  if Cout > 0
    reset di = 0
  end if
end for
```

Figure 20. Successive approximations algorithm

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First, all bits are cleared (D = 0). Then, the bits are tested successively in a loop, starting with the MSB and going down to the LSB. For each bit, the output value of the comparator C_{out} is examined when the bit is set. If the value is negative, this signifies that the remaining offset is negative and that the DAC value has still to be increased. For this reason, the bit is kept. If on the contrary C_{out} is positive, the currently tested code is too high (above Z_0) and the tested bit is reset. The algorithm then performs the same test with the next less significant bit, until reaching the LSB.

Figure 21 shows the analog output value of the DAC versus time (algorithm step). Table 2 shows which comparisons are made and which bits are kept.

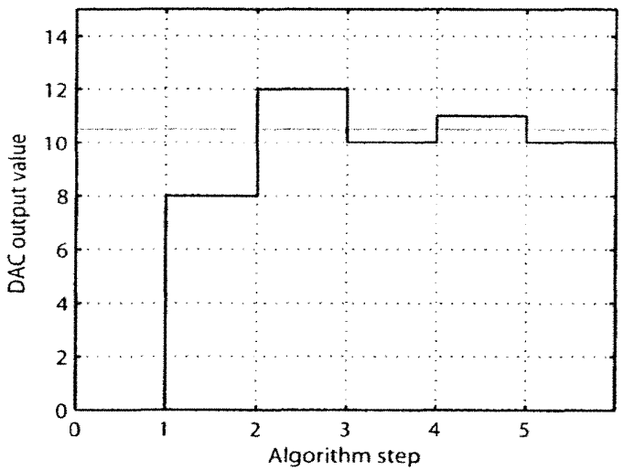


Figure 21. Successive approximations algorithm timing

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Table 2. Successive approximations algorithm timing

Step	DAC output value	Comparison result	Comment
0	0	-	reset
1	8	$8 < Z_0$	bit 4 is kept
2	12	$12 > Z_0$	bit 3 is rejected
3	10	$10 < Z_0$	bit 2 is kept
4	11	$11 > Z_0$	bit 1 is rejected
5	10	-	final value

3.2 Working condition

At the end of the successive approximations algorithm, it can be proven that the adjusted DAC output value A_{final} is not more distant than one LSB from the ideal value Z_0:

$$|A_{final} - Z_0| \leq b_1 \tag{3.3}$$

Furthermore, the final value never exceeds the ideal value:

$$A_{final} \leq Z_0 \tag{3.4}$$

These properties are the consequence of the construction of the algorithm. Equation 3.4 is valid because the bits elevating the DAC output above Z_0 are systematically rejected. By adapting the algorithm, it is possible to have the converse relation.

Equation 3.3 is true only if the converter has no missing code:

$$b_i \leq b_1 + \sum_{j=1}^{i-1} b_j \qquad \forall i \in [2 \ldots n] \tag{3.5}$$

BNSDCCID: <XP 2587083A I >

ANALOG EXHIBIT 1002
Page 275 of 321

In addition, the value to adjust must be comprised in the DAC full scale:

$$0 \leq Z_0 \leq \sum_{i=1}^{n} b_i \tag{3.6}$$

Equation 3.5 guarantees that the sum of the less significant bits of any bit b_i in the DAC is not inferior by more than one LSB to the bit itself (b_i). This important condition ensures that if a bit b_i is rejected during a given step of the successive approximations algorithm, the remaining steps using only less significant bits cover the complete range of values up to the just rejected value. If this condition is not satisfied, equation 3.3 is no longer valid.

Let's look again at equation 3.5 and compare it to the values of the weights of the bits in a binary DAC like the one that is used in the preceding examples. In this DAC, equation 3.1 can be rewritten as:

$$b_i = 2^{i-1} = b_1 + \sum_{j=1}^{i-1} b_j \tag{3.7}$$

This equation is the limit case of inequation 3.5. It means that at each step of the algorithm, the remaining codes are just sufficient to produce the necessary number of values. In other words, the binary digital-to-analog converter has no missing code.

3.3 Reverse successive approximations algorithm

As stated by equation 3.4, the adjusted value of the algorithm is never higher than the ideal value. In some cases, one is interested in the reverse property, i.e. that the adjusted value is never lower than Z_0:

$$A_{final} \geq Z_0 \tag{3.8}$$

This is achieved by inverting all the bits and the decision in the algorithm. As a result, the reverse successive approximations algorithm (figure 22) is obtained.

BNSDOCID: <XP 2587083A_1_>

ANALOG EXHIBIT 1002
Page 276 of 321

```
set all d_i = 1
for i = n downto 1
   reset d_i = 1
   if C_out < 0
      set d_i = 1
   end if
end for
```

Figure 22. Reverse successive approximations algorithm

Equation 3.3 still applies to this modified algorithm, guaranteing that the maximum distance to the ideal value is 1 LSB.

Figure 23 and table 3 show the execution of this modified algorithm.

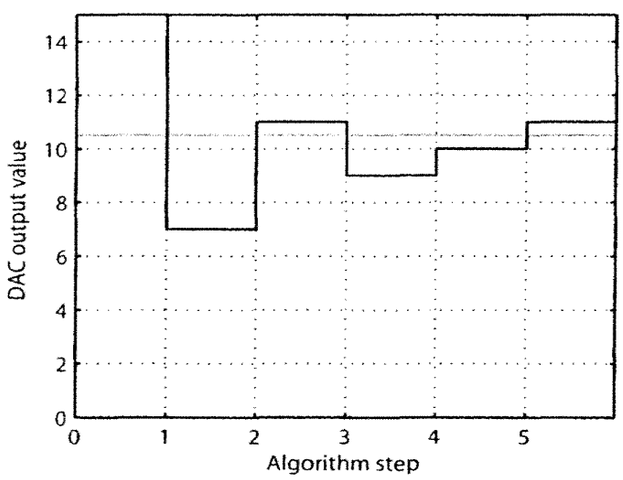


Figure 23. Reverse successive approximations algorithm timing

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Table 3. Reverse successive approximations algorithm timing

Step	DAC output value	Comparison result	Comment
0	15	-	reset
1	7	$7 < Z_0$	bit 4 is rejected
2	11	$11 > Z_0$	bit 3 is kept
3	9	$9 < Z_0$	bit 2 is rejected
4	10	$10 < Z_0$	bit 1 is rejected
5	11	-	final value

3.4 Complexity

For a DAC with n bits, the successive approximations algorithm uses n calibration steps (the loop of the algorithm). Compared to the number N of different possible output values, this represents:

$$n = \log_2(N) \tag{3.9}$$

This well-known result shows that the dichotomic search performed by successive approximations is much faster than a systematic testing of all codes, which can be done by replacing the control block of figure 17 by a counter.

4 SUB-BINARY RADIX DACS

4.1 Use of sub-binary DACs for successive approximations

As already discussed in section 3.2, using a binary-radix DAC with a successive approximations algorithm exploits the limit of the working condition. Furthermore, such DACs are difficult to design unless the number of bits is small, because the weight of each bit needs to be precisely set to avoid missing codes and redundancies. For this reason, they usually occupy an important circuit area.

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The working condition (equation 3.5) of the successive approximations algorithm does not impose precise bit weights. Whereas missing codes are not allowed, redundancies are not problematic. This can be turned into an advantage, because it allows the use of imprecise converters. By voluntarily introducing redundancies, the risk of missing codes is reduced and the sub-binary converters can be designed using less effort and area without degrading the performance of the algorithm.

Sub-binary converters should systematically be used with successive approximations algorithms. There is no reason for preferring a conventional radix-2 converter.

4.2 Characteristics

In a sub-binary radix DAC, the weights of the different bits are based on a radix R that is smaller than 2:

$$b_i = R^{i-1} \qquad \forall i \in [1 \ldots n] \tag{3.10}$$

Figures 24 and 25 show the input/output characteristics of sub-binary radix DACs with R equal to 1.75 and 1.5 respectively. In both figures, the grey line is the identity function y = x. See also figure 18 for the R = 2 case.

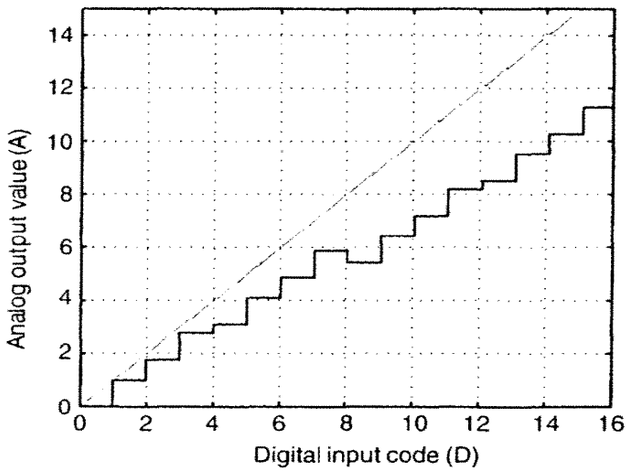


Figure 24. Input/output characteristics of a radix 1.75 DAC

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When the radix is decreased, the characteristics move down from the ideal y = x line. The converter becomes non-linear, non-monotonic (some steps are down instead of up) and redundant (the same output code is generated by two or more different input words).

The advantage of the sub-binary radix converter is that it is less likely to have missing codes than a radix-2 converter. Actually, a mismatch problem in a sub-binary converter has the same effect as changing its radix. Provided the radix is sufficiently far from the limit value 2, this does not create missing codes.

The radix has to be chosen carefully to account for variations and to make sure the value 2 is not exceeded. The more variations are expected, the lower the radix must be. The exact choice of the radix depends on the structure of the DAC and the tolerances on its components. This is discussed in sections 5, 6 and 10, which present 3 different topologies of digital-to-analog converters and how they can be made sub-binary.

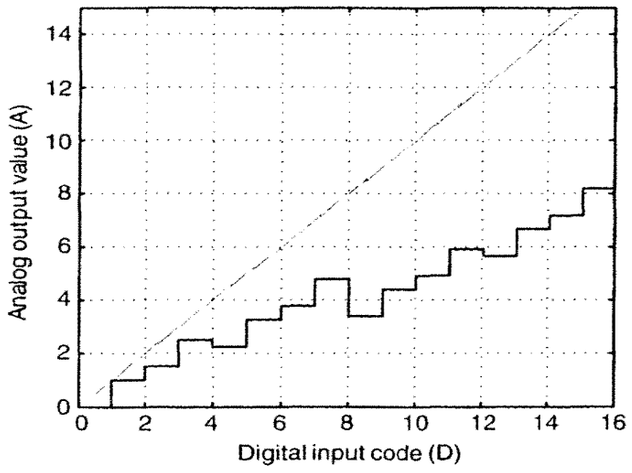


Figure 25. Input/output characteristics of a radix 1.5 DAC

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4.3 Resolution

The resolution of a digital-to-analog converter is the ratio between the full scale FS (the range of possible output values) and the LSB value (the smallest difference between two codes). It and can be calculated easily if the radix R is constant:

$$Res = \frac{FS}{LSB} = \frac{b_1 + \sum_{i=1}^{n} b_i}{b_1} = \frac{R^n}{R-1} \tag{3.11}$$

The resolution is usually expressed in bits, by calculating the $\log_2$ of the previous equation.

The advantage of code redundancy of sub-binary radix converters is also their slight disadvantage. By creating duplicate codes, the full scale is reduced, and consequently also the resolution. In the example of the radix-1.5 converter (figure 25) for instance, the full-scale of this 4 bits DAC is about 8, which is only half of an equivalent radix-2 converter (figure 18). The 4 bits sub-binary converter has only 3 bits of resolution. The extra bit creates code redundancies.

4.4 Tolerance to radix variations

This section presents a simple design rule for sub-binary converters (equation 3.13). Although it is more restrictive than required, it is easy to translate into a circuit condition.

Since the radix in sub-binary converters is subject to variations due to the tolerances of the components, one can rewrite equation 3.10 as follows:

$$b_i = r_i b_{i-1} \qquad \forall i \in [2 \ldots n] \tag{3.12}$$

where r_i is the "local" radix of stage i.

In this case, a *sufficient but not imperative* condition for the DAC to respect the working condition of the successive approximations algorithm (equation 3.5, is the following:

$$r_i \leq 2 \qquad \forall i \in [2 \ldots n] \tag{3.13}$$

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Eventually, the radix r_i at a given stage can also be slightly higher than 2, but only if the remaining radixes of the less significant bits are sufficiently low (and some of them strictly lower than 2). Taking this parameter into account increases the complexity of the condition, transforming it back into equation 3.5.

Usually, equation 3.13 can easily be translated into a circuit constraint ensuring proper functioning of the converter with the successive approximations algorithm. Furthermore, this constraint is simple to guarantee for all the stages of the converter, even the higher order ones (most significant bits). Adding an extra bit is not more complex at a high or low stage (e.g. adding a 16th bit is not more difficult than adding a 4th). This means that *a sub-binary DAC can be designed with low effort for any given resolution, without increasing circuit complexity.*

Finally, it is not necessary to choose the same radix for all the stages of the converter (i.e. choosing all r_i equal), as long as the local radixes respect the general rule of equation 3.5, or the more restrictive rule of equation 3.13.

5 COMPONENT ARRAYS

The most intuitive manner to compensate for imperfections of analog components is to correct their parameters directly. For instance, if the value of a resistor or capacitor influences a time constant which has to be well controlled in a filter [20], it is possible to tune the value of the devices. Another example is the tuning of capacitors in DACs [21].

Figures 26 and 27 present the implementation of digitally adjustable components. By using the switches, it is possible to trim the value of the component. The sub-components can be connected in parallel (figure 26) or in series (figure 27).

The choice of the values of the components in the array can be optimized. Usually, such an array replaces a single component for which the required accuracy cannot be achieved without calibration.

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The resistor in the vertical branches has here a value xR, and the terminator $x_T R$. The case with

$$x = x_T = 2 \tag{3.39}$$

corresponds to the R/2R ladder. On the opposite, choosing

$$x > 2 \tag{3.40}$$

makes the converter sub-binary. This special case is analyzed below. A theoretical study of the R/xR structure can be found in [36]. Here, a more circuit-oriented analysis is done.

In each stage of the network, the incoming current i_{i+1} is divided into 2 currents b_i and i_i:

$$i_{i+1} = b_i + i_i \tag{3.41}$$

with

$$b_i = i_{i+1} \frac{R_{eq;i}}{xR + R_{eq;i}} \tag{3.42}$$

and

$$i_i = i_{i+1} \frac{xR}{xR + R_{eq;i}} \tag{3.43}$$

More interesting is the ratio ρ_i between these two currents:

$$\rho_i = \frac{b_i}{i_i} = \frac{R_{eq;i}}{xR} \tag{3.44}$$

BNSDOCID: <XP 2587083A I >

ANALOG EXHIBIT 1002
Page 283 of 321

In fact, this ratio can be used to derive the condition which allows the ladder to be used for successive approximations. Let's make two small modifications in the ladder: Using the terminator current as a bit in the converter instead of dumping it, and numbering the bits by taking care to exchange the last two currents to have:

$$b_1 = i_2 = i_3 \frac{x_T}{x_T + x} \tag{3.45}$$

and

$$b_2 = i_3 \frac{x}{x_T + x} \tag{3.46}$$

Figure 40 shows the resulting circuit.

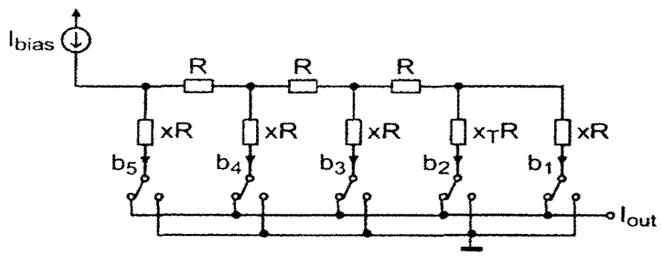


Figure 40. Modified R/xR ladder

10.2 Working condition

In each stage of the ladder in figure 40, the remaining current i_i is equal to the sum of the less significant bits:

$$i_i = \sum_{j=1}^{i-1} b_j \tag{3.47}$$

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To allow the converter to work with a successive approximations algorithm, it is sufficient that in all stages but the last one the remaining current (which is also the sum of all less significant bits), is higher than the corresponding bit current. In other words, the value of the equivalent resistance of the remaining right part of the ladder has to be lower than the vertical resistor xR. By imposing:

$$\rho_i \leq 1 \qquad \forall i \in [3 \ldots n] \tag{3.48}$$

which is, by equation 3.44, equivalent to:

$$b_i \leq i_i \qquad \forall i \in [3 \ldots n] \tag{3.49}$$

the working condition of the successive approximations algorithm (equation 3.5) is respected indeed, because:

$$b_i \leq \sum_{j=1}^{i-1} b_j \leq b_i + \sum_{j=1}^{i-1} b_j \qquad \forall i \in [3 \ldots n] \tag{3.50}$$

And for i = 2, in order to guarantee the working condition, one must have:

$$b_2 \leq 2b_1 \Rightarrow x \leq 2x_T \tag{3.51}$$

10.3 Terminator calculation

One particularly interesting value for x_T is the one that ensures that:

$$R_{eq;3} = R + (x_T R \parallel xR) = R + \frac{R^2 x_T x}{R(x_T + x)} = x_T R \tag{3.52}$$

because in this case, all the $R_{eq;i}$ (i > 2) are equal to $x_T R$.
Simplifying equation 3.52 gives:

$$x_T^2 - x_T - x = 0 \tag{3.53}$$

The only solution of this equation is:

BNSDOCID: <XP 2587083A_1_>

ANALOG EXHIBIT 1002
Page 285 of 321

$$x_{T;stat} = \frac{1 + \sqrt{1 + 4x}}{2} \tag{3.54}$$

Choosing $x_T = x_{T;stat}$ makes the ladder stationary, i.e. in all the stages of the ladder, the equivalent resistor $R_{eq;i}$ ($i > 2$) has the same value $x_{T;stat}R$ and the current is divided exactly with the same ratio ρ_{stat}:

$$\rho_{stat} = \frac{x_{T;stat}R}{xR} = \frac{1 + \sqrt{1 + 4x}}{2x} \tag{3.55}$$

In the last stage, the ratio is inverted. It is now obvious that the two last bits had to be exchanged to ensure that $b_2 \geq b_1$. This is because:

$$x_{T;stat}R \leq xR \qquad \forall x \geq 2 \tag{3.56}$$

This is the case indeed (see equations 3.40 and 3.54). Furthermore, to ensure proper functioning of the last stage of the ladder, equation 3.51 has to be respected. It is easy to prove by replacing 3.54 in 3.51 that this is the case if:

$$x \leq 6 \tag{3.57}$$

Such a high value of x is never implemented anyway. It leads to a very low radix that makes the converter inefficient.

10.4 Terminator implementation

As shown by equation 3.54, the ideal value of the terminator is not an integer. To solve the implementation problem, [36] proposed to realize the terminator using additional R/xR stages. But this is not necessary, because an integer value of x_T satisfying all the working conditions can be chosen. In fact, the sufficient condition for x_T is simply:

$$\frac{x}{2} \leq x_T \leq x_{T;stat} \tag{3.58}$$

The left inequation is directly derived from equation 3.51, whereas the right part is explained as follows: To ensure the working condition, section 10.2 shows that a sufficient condition is:

BNSDOCID: <XP 2587083A I >

ANALOG EXHIBIT 1002
Page 286 of 321

$$R_{eq;i} \leq xR \tag{3.59}$$

This is ensured in the stationary case (equation 3.56). If the value of x_T is voluntarily chosen smaller than $x_{T;stat}$, according to equation 3.58, it can be proven that the $R_{eq;i}$ become a series converging to the value $x_{T;stat}R$. Furthermore, the series has the property of being strictly increasing for increasing values of i. This is due to the fact that the first value is chosen lower than the limit value $x_{T;stat}R$.

Figure 41 shows the effect of choosing a 2R terminator ($x_T = 2$) in a R/3R ladder ($x = 3$). The value of the equivalent resistor at each stage is plotted. The equivalent value converges quickly to the limit value ($x_{T;stat} \cong 2.3$ with $x = 3$), without ever exceeding it. The limit $x_{T;stat}$ is plotted in grey in the figure.

To explain the result presented in this section in other words, choosing $x_T \leq x_{T;stat}$ puts the converter in an even more favorable case with respect to the working condition. Indeed, the highest $R_{eq;i}$ value is reached in the last stage (MSB) instead of being equal in every stage to $x_{T;stat}R$ (sationary case). This is particularly important when the ladder is sized for a given component matching quality. The liberty given for the choice of the terminator value can be exploited to simplify the ladder implementation, without impacting negatively on the immunity of the circuit to variations of the component values.

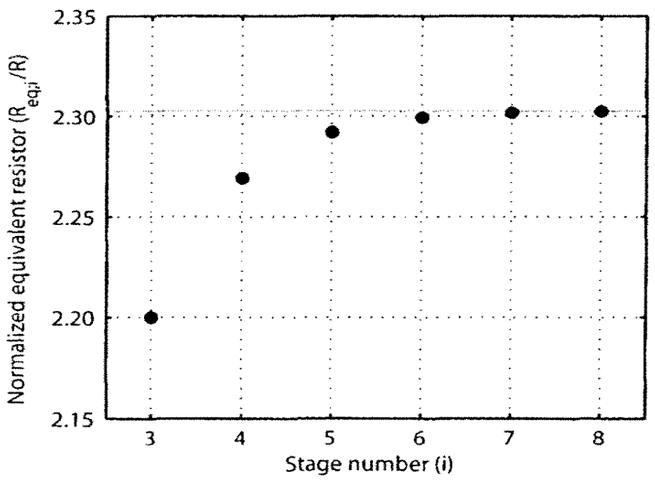


Figure 41. 2R terminator in a R/3R ladder

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10.5 Ladder sizing

The same analysis as in section 5.1 is made here for the R/xR converter to calculate x as a function of the component matching parameter δ. The terminator sizing is covered in the next section.

Remember that if all the components composing the converter are not matched using the rules of chapter 2, section 2.1, δ represents the tolerance of the components.

Let's rewrite equation 3.49 in the worst case:

$$b_i(1+\delta) \le i_i(1-\delta) \tag{3.60}$$

Which is, using equation 3.44, equivalent to:

$$R_{eq;i}(1+\delta) \le xR(1-\delta) \tag{3.61}$$

The worst case (highest possible value) for $R_{eq;i}$ is $x_{T;stat}R$ if the terminator is chosen according to equation 3.58:

$$x_{T;stat}R(1+\delta) \le xR(1-\delta) \tag{3.62}$$

From equation 3.53, one can write:

$$x = x_{T;stat}(x_{T;stat}-1) \tag{3.63}$$

Replacing 3.63 in 3.62 and simplifying:

$$(1+\delta) \le (x_{T;stat}-1)(1-\delta) \tag{3.64}$$

Finally, using 3.54 and simplifying again, one has:

$$x \ge 2\frac{1+\delta}{(1-\delta)^2} \tag{3.65}$$

The optimum resistor ratio can thus be determined, for a given imperfection level δ, using equation 3.65. This relation can also be reversed, in order to calculate the allowable error δ in function of the resistor ratio x:

$$\delta \le 1 + \frac{1-\sqrt{1+4x}}{x} \tag{3.66}$$

BNSDOCID: <XP 2587083A_1_>

10.6 Terminator sizing

For the terminator, the left inequation 3.58 can also be rewritten in the worst case:

$$\frac{x}{2}(1+\delta) \le x_T(1-\delta) \tag{3.67}$$

Which is equivalent to:

$$x_T \ge x\frac{1+\delta}{2(1-\delta)} \tag{3.68}$$

In the worst case, the right side of inequation 3.58 remains:

$$x_T \le x_{T;stat} \tag{3.69}$$

because equation 3.62 already accounts for the tolerance $(1+\delta)$ on x_T. Combining equations 3.68 and 3.69 results in:

$$x\frac{1+\delta}{2(1-\delta)} \le x_T \le \frac{1+\sqrt{1+4x}}{2} \tag{3.70}$$

If the left inequality is violated, i.e. x_T is chosen too small, the local radix r_2 (the b_2/b_1 ratio) becomes higher than 2. In this case, the converter works perfectly, but with a LSB corresponding to b_2 instead of b_1. If the right inequality 3.70 is not respected, the converter works, but only if the tolerances of the components are sufficiently small, at any rate smaller than the limit value δ_{max} calculated from equation 3.66:

$$\delta_{max} = 1 + \frac{1-\sqrt{1+4x}}{x} \tag{3.71}$$

The upper limit for x_T (equation 3.69) ensures that the worst case for the current division is reached in the highest stage of the converter. If on the contrary, x_T becomes larger than $x_{T;stat}$, the worst case is reached in the third stage, because the $R_{eq;i}$ series is then strictly decreasing. The working condition in the third stage is still $\rho_3 \le 1$ (equation 3.48), which becomes in the worst case:

BNSDOCID: <XP 2587083A_1_>

$$\rho_3 = \frac{R_{eq;3}(1+\delta)}{xR(1-\delta)} = \frac{R + (xR \parallel x_T R)}{xR} \cdot \frac{(1+\delta)}{(1-\delta)}$$
$$= \frac{1 + \frac{xx_T}{x + x_T}}{x} \cdot \frac{1+\delta}{1-\delta} \leq 1 \tag{3.72}$$

which gives:

$$\delta \leq \frac{x^2 - x - x_T}{x^2 + x + 2xx_T + x_T} \tag{3.73}$$

This equation has no solution when:

$$x_T > x^2 - x \tag{3.74}$$

as in this case, $R_{eq;3}$ becomes larger than xR and even with perfect components, ρ_3 is higher than 1. Figure 42 shows the maximum allowable mismatch δ in function of the terminator value x_T in the case of a R/3R ladder (x = 3). When $x_T \leq x_{T;stat}$, equation 3.66 applies, whereas equation 3.73 is valid when $x_T \geq x_{T;stat}$. For $x_T = x_{T;stat}$ both are equivalent, as expected. In the case of an R/3R ladder, $\delta_{max} \cong 0.13$ (equation 3.71) and $x_{T;stat} \cong 2.30$ (equation 3.54). The minimum value for x_T when $\delta = \delta_{max}$ is calculated with equation 3.68 and is about 1.95.

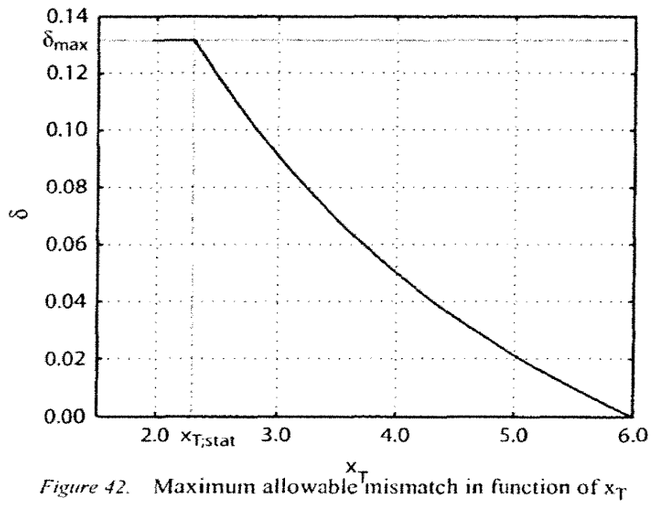


Figure 42. Maximum allowable mismatch in function of x_T

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As shown here above, choosing $x_T > x_{T;stat}$ reduces the allowable mismatch and should thus be avoided. The optimum choice is $x_{T;stat}$ because it still allows $\delta = \delta_{max}$ without decreasing the local radix in the last stages. This happens when $x_T < x_{T;stat}$ because the equivalent resistor in the last stages is lower than $x_{T;stat}R$ (figure 41). This reduction also decreases ρ (equation 3.44) and thus the local radix, which depends on ρ (see equation 3.75). This choice is thus also sub-optimal as it diminishes the resolution of the converter. But if an integer value has to be chosen to simplify the realization of the terminator, it is better to choose a value $x_T \leq x_{T;stat}$.

The two last sections have shown how to size a R/xR ladder. Knowing the mismatch between components, it is possible to choose a resistor ratio x with equation 3.65, and a terminator with 3.70 that allows the use of the converter with a successive approximations algorithm. As is to be expected, these equations would speak in favor of the R/2R ladder if perfect components ($\delta = 0$) existed.

10.7 Radix

In the case where $x_T = x_{T;stat}$, the radix of the ladder (for $i > 2$) can be easily calculated:

$$R = \frac{b_i}{b_{i-1}} = \frac{b_i}{i_i}\left(1 + \frac{1}{\rho_{stat}}\right) = \rho_{stat}\left(1 + \frac{1}{\rho_{stat}}\right) = \rho_{stat} + 1 \tag{3.75}$$

By taking the limit case of inequation 3.65 and replacing it in 3.55 gives:

$$\rho_{stat} = \frac{1 - \delta}{1 + \delta} \tag{3.76}$$

And substituting the latter in 3.75:

$$R = \frac{2}{1 + \delta} \tag{3.77}$$

BNSDOCID: <XP 2587083A I >

Considering the last stage of the ladder, the limit choice for x_T is given by equation 3.68 and is:

$$r_2 = \frac{b_2}{b_1} = \frac{xR}{x_T R} = \frac{2(1-\delta)}{1+\delta} \tag{3.78}$$

Obviously, choosing this limit value for the terminator makes the ladder non-stationary and equation 3.77 not valid any more. However, equations 3.77 and 3.78 reflect the maximum allowable radixes as a function of the mismatches (or tolerances) of the components, respectively in the ladder and in the last stage.

A particularly remarkable fact is that these two equations are *exactly equivalent* to equation 3.17, which is the limit condition for component arrays. This is not surprising however, since even if the two structures are different, they both have exactly the same function and the same component mismatches. Achieving equal performance is a logical result, even if its proof is not trivial. To gain a little more insight in the relation of the radix with the mismatch, figure 43 plots the function of equation 3.77.

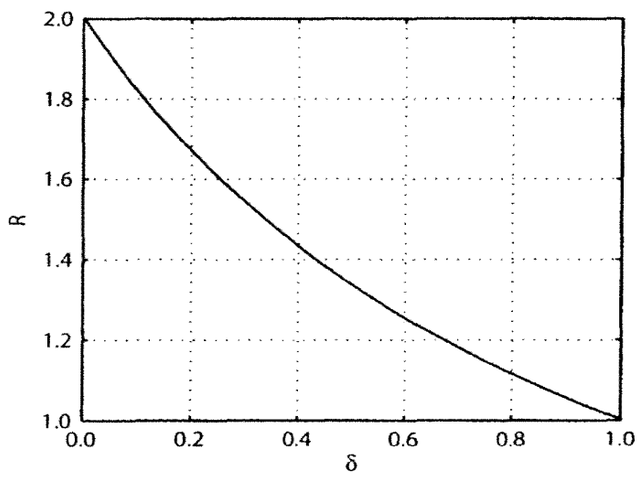


Figure 43. Best-achievable radix with a sub-binary converter

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With perfect components, $\delta = 0$ and the radix can be binary. This corresponds to a R/2R ladder or a binary-weighted component array.

With components having 100% mismatch in the worst case, the best achievable radix is 1, which corresponds to a thermometer coding (all the bits have the same nominal value).

Between these two extreme situations, the function is 1/x shaped. The largest loss in high radix value possibilities is made for a small δ increase when δ is close to 0. Any further increment has less impact, since the slope of the function decreases (in absolute value) when δ increases.

11 M/2$^+$M LADDERS

Using the same technique as for M/2M ladders, some R/xR ladders can easily be realized using pseudo-resistors. Two particularly interesting variants of M/2$^+$M (sub-binary) ladders are the M/3M and M/2.5M ladders. They are presented in this section.

11.1 M/3M ladders

The M/3M is the implementation of the R/3R structure using MOS transistors to realize pseudo-resistors of unit value R. Figure 44 presents an M/3M ladder.

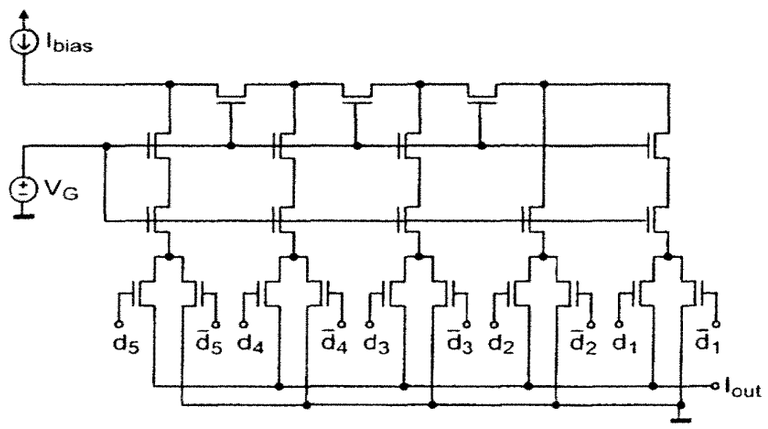


Figure 44. M/3M ladder

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of the transistor and the ideal case, multiplied by the transconductance g_m at the bias point:

$$I_{offset} = g_m V_O \tag{4.22}$$

In fact, it is usually not the absolute value of the V_T of one single transistor that is important, but the mismatch between the threshold voltages of two transistors. In this case, the difference can be minimized by using matching and increasing circuit area. But the simplified model presented above also applies.

Consequently, the offset current I_{offset} corresponds to the input offset voltage that has to be compensated. This can be done by injecting a compensation current I_{comp} into the output node (the drain D) to cancel I_{offset}:

$$I_{comp} = -I_{offset} \tag{4.23}$$

The offset is cancelled and the transistor behaves exactly as if the V_T was ideal, i.e. the output voltage is:

$$v_{out} = Z_{out}[g_m(v_{GS} + V_O) + I_{comp}] = Z_{out} g_m v_{GS} \tag{4.24}$$

It is noteworthy that these equations represent only the small signals, and that the DC bias point is not considered. Furthermore, the offset is included into this small-signal analysis, in spite of the fact that it is also a DC signal. This is done on purpose to show an approximation of the value of the offset current I_{offset} and consequently the compensation current I_{comp}. However, this representation is of no other interest in circuit modelling.

Let's analyze how the compensation current can be injected and how to choose the most appropriate compensation node based on the example of the Miller operational amplifier. Different approaches can be implemented. In [47], [48] and [49], a second differential pair is connected in parallel and the offset is corrected by applying a compensation voltage V_{comp}. Figure 75 presents such a circuit.

This topology has the disadvantage of being very sensitive to the voltage difference V_{comp}. In fact, the main differential pair is usually designed for high gain, and it is difficult to design a second differential pair with a much degraded gain using similar devices. The compensation voltage V_{comp} thus remains in the order of magnitude of the offset voltage to be compensated, typically a few millivolts. This reduced signal level degrades the signal-to-noise ratio and is not optimal. Another disadvantage of this technique is that it

BNSDOCID: <XP_____2587083A_I_>

ANALOG EXHIBIT 1002
Page 294 of 321

uses a voltage compensation signal. If the digital-to-analog converter used to generate the compensation signal has a current output, it is necessary to transform it to a voltage.

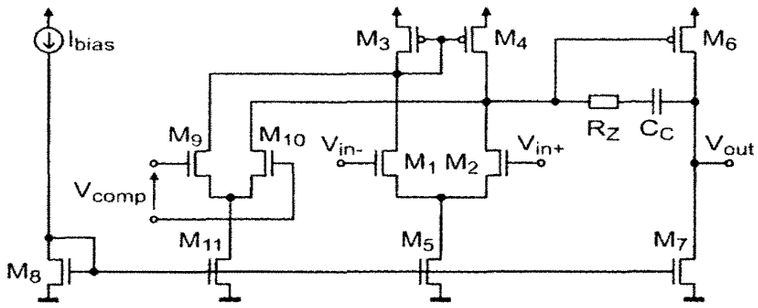


Figure 75. Offset correction by additional differential pair

A second approach is to modify the current mirror [50] that implements the active load of the differential pair [13]. One additional transistor is added in series with each branch of the current mirror. They are operated in the linear region and act as variable resistors controlled by their gate voltage. By applying a voltage difference V_{comp} to the gates of these transistors, the current mirror is unbalanced and the offset is compensated. Figure 76 shows how a degenerated active load is realized.

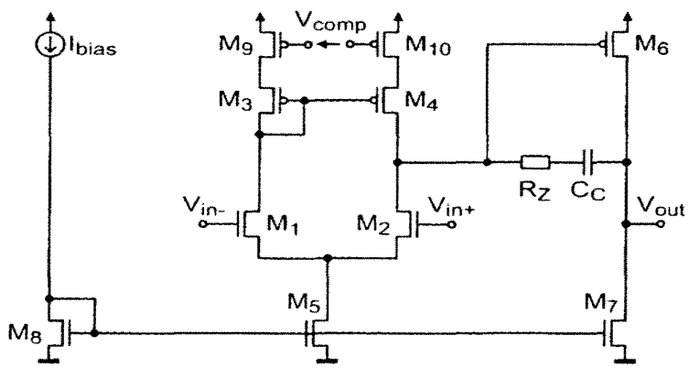


Figure 76. Offset correction by degenerated current mirror

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METHODOLOGY FOR THE DIGITAL CALIBRATION OF ANALOG CIRCUITS AND SYSTEMS

with Case Studies

by

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Springer

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Methodology for the Digital Calibration of Analog Circuits and Systems Using Sub-binary Radix DACs

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Abstract—**This paper presents a methodology for digitally calibrating analog circuits and systems. Based on the detection of an imperfection by a simple comparator, a successive approximations algorithm tunes a compensation current. The latter is generated by a sub-binary radix M/2^{i}M DAC, which has the advantage of allowing reaching arbitrarily high resolutions at the cost of extremely small area. The methodology proposed allows the removal of any type of imperfections, at the expense of two shift registers, a few logical gates and a DAC which is smaller than the shift register.**

Index Terms—**Calibration, sub-binary DACs, M/2^{i}M, offset compensation, deep sub-micron, variability.**

I. Introduction

The evolution of integrated circuit manufacturing technologies renders even basic analog systems difficult to design today. With the size reduction, the intrinsic precision of the components degrades. In parallel, the supply voltage decreases, limiting the topologies which can be used. Many modern technologies are specifically suited for pure digital circuits, and some analog devices, like capacitors, are not available. In these conditions, analog design is a challenge even for experienced designers. To relieve the extreme design constraints in analog circuits, digital calibration becomes a must. It allows a low-precision component to be used in high-performance systems. If the calibration is repeated, it can even cancel the effect of temperature drift and ageing.

The digital calibration is compatible with the evolution of fabrication technologies, which ever more facilitates the integration of digital solutions at the cost of a dramatic reduction of analog performances. Thanks to the reduction of the size of digital devices, even complex digital calibration solutions can be integrated and become a viable alternative to intrinsically precise analog designs. Digital calibration allows realizing high-performance analog systems with modern technologies. This enables pure analog designs to be implemented even in fully digital processes. In existing mixed-signal designs, the full system realization also becomes possible with technologies providing higher integration density. Finally, because circuit performances rely on digital calibration, retargeting is simplified. The digital blocks can be synthesized automatically, whereas only a limited design effort is invested in the analog circuit.

The methodology presented in this paper is versatile. It can be applied at circuit or system level, for analog circuits, but also mixed-mode circuits like sensor interfaces [1][2][3], and even purely digital systems like memories [4][5][6].

II. Digital Compensation of Analog Circuits

Figure 1 presents a synoptic view of a digitally calibrated analog system. The digital calibration shown in grey aims cancelling an imperfection of the analog system. As explained above, this is a viable alternative to building an intrinsically precise analog system which reaches high specifications on its own, without requiring calibration.

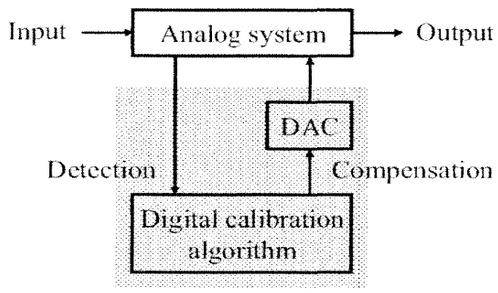


Figure 1. Digital calibration of an analog system.

To allow the digital compensation of an imperfection in an analog circuit by the injection of a compensation current, two nodes must be identified in the analog system: a *detection node* and a *compensation node*. Furthermore, a *detection configuration* of the compensated analog circuit must be found. The observation of the detection node allows determining whether the imperfection to be corrected is lower or higher than the error-free nominal value to be reached by calibration. For example, the offset of an operational amplifier is positive or negative around the nominal value 0. Based on the information gathered in the detection node, an adequate decision is taken to compensate the imperfection by increasing it if it is lower than expected or decreasing it if it is higher than the nominal value.

A. Detection Configuration

The detection configuration is the condition in which the circuit imperfection can be observed in the detection node. In some cases, this is possible during normal circuit operation,

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BNSDOCID: <XP_____31548289A_1_>

ANALOG EXHIBIT 1002
Page 298 of 321

without modifying the circuit topology and interrupting signal processing. But in many cases, a different circuit configuration is necessary to measure the imperfection in the detection node. Usually, this is due to the low level of signal at the detection node during normal operation. Figures 2 and 3 present the typical example of the offset cancellation of an operational amplifier.

During normal operation in closed-loop (Figure 2), the offset of the amplifier can be sensed directly between its two inputs. The detection signal δ is:

$$\delta = V_{in+} - V_{in-} = -V_O \tag{1}$$

The detection signal level is problematic though. Indeed, at the end of the calibration procedure, the residual offset of the amplifier is:

$$V_{O,compensated} = V_{OC} \tag{2}$$

This imposes that the comparator used to determine the offset sign has an offset lower or equal to the expected residual offset of the amplifier after calibration.

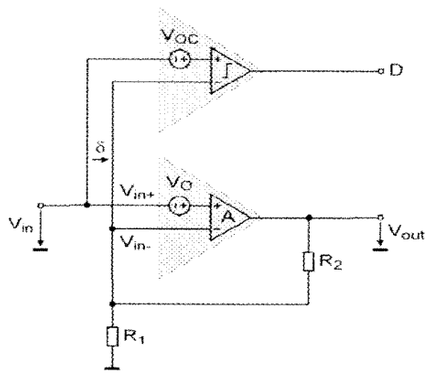


Figure 2. Closed-loop offset cancellation.

To overcome this severe limitation, two options can be considered. The first one is to compensate the offset of the comparator (in an open-loop configuration) before using it to correct the offset of the amplifier in closed-loop. The second possibility is to measure the offset of the amplifier using the open-loop configuration of Figure 3.

In this topology, the detection signal is:

$$\delta = AV_O \tag{3}$$

where A is the open-loop gain of the operational amplifier. This second configuration presents the advantage of having a detection signal being several orders of magnitude higher than the closed-loop one. As a consequence, the residual offset after calibration becomes:

$$V_{O,compensated} = -\frac{V_{OC}}{A} \tag{4}$$

The comparator offset is no more critical and thus doesn't need to be calibrated preliminarily.

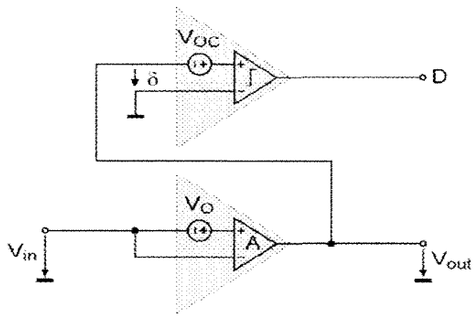


Figure 3. Open-loop offset cancellation.

The disadvantage of the open-loop configuration is the fact that it requires to remove the amplifier from its normal operation mode. In some applications, this is acceptable. If continuous signal processing is required, a strategy with two amplifiers being alternatively one calibrated and the other operating normally (ping-pong) can be implemented [7].

B. Detection Node

In the selected detection configuration, there should be a detection node identified where the imperfection to be compensated can be sensed appropriately. In particular, the signal level should be sufficiently high, and the signal measured should be a function of the imperfection alone. The imperfection can be sensed in current or voltage mode, single ended or differentially. If single-ended mode voltage detection is chosen and if the offset of the comparator is not critical, an implementation as simple as a digital inverter can be considered. Figure 4 shows how the circuit of Figure 3 can be simplified.

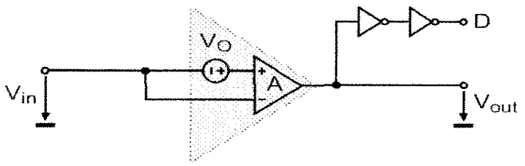


Figure 4. Digital calibration of an analog system.

C. Compensation Node

The correction is done by injecting a compensation current in an appropriate node of the analog circuit. The compensation

BNSDOCID: <XP_____31548289A_I_>

ANALOG EXHIBIT 1002
Page 299 of 321

node is chosen for its property to convert the injected current into a reduction/increase of the imperfection. In the ideal case, no other parameter should be affected by the compensation current. In practice, the correction node is chosen for the high correlation between the injected current and the imperfection, and the low correlation between the compensation current and any other parameter. Figure 5 shows the implementation of a differential current compensation of a Miller operational amplifier.

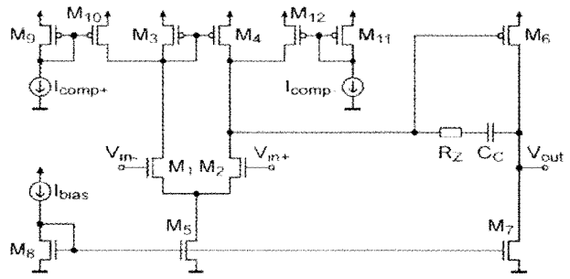


Figure 5. Differential compensation of a Miller operational amplifier.

In this circuit, the compensation current mirrors use PMOS transistors and the current is injected in the same direction differentially. This allows the direct connection of an M/2+M ladder to the compensation current inputs, transistors M9 and M11 being the current collectors. Alternative compensation circuits could inject the compensation current unilaterally.

For the choice of the compensation node, attention must be paid to not degrading circuit performance. This implies that the current mirrors added (transistors M10 and M12 in Figure 5) don't add significant parasitic capacitances to the compensation nodes, and that their output impedance is higher than the impedance in the compensation nodes.

The dimensioning of the compensation current mirrors in the case of the Miller operational amplifier is done as follows:

1. The maximum compensation current is determined.
2. The transistor length L is determined in order to have a sufficiently low channel conductance gds that does not affect much the impedance of the compensation node. The length must also be sufficient to limit the effect of voltage variations in the compensation node on the compensation current that is injected.
3. The transistor width W is calculated, considering that the output transistors of the current mirrors must remain in saturation. The width must be large enough to keep the saturation voltage below the voltage in the compensation node.

III. Successive Approximations

The successive approximations algorithm performs a search through the possible values of the compensation currents. It performs dichotomy at each step, by determining whether the tested bit generates a compensation value too high or not. The algorithm starts by testing the most significant bit (MSB), and goes down towards the least significant bit (LSB). Figure 6 presents a pseudo-code description of the algorithm, with d_i (i $\in$ {1, n}) being the digital input word of the n-bits DAC, and C_{out} the output of the comparator.

```
reset all d_i = 0
for i = n downto 1
   set d_i = 1
   if C_out > 0
      reset d_i = 0
   end if
end for
```

Figure 6. Successive approximations algorithm.

First, all bits are cleared (D = 0). Then, the bits are tested successively in a loop, starting with the MSB and going down to the LSB. For each bit, the output value of the comparator C_{out} is examined when the bit is set. If the value is negative, this signifies that the remaining imperfection is negative and that the DAC value has still to be increased. For this reason, the bit is kept. If on the contrary C_{out} is positive, the currently tested code is too high and the tested bit is reset. The algorithm then performs the same test with the next less significant bit, until reaching the LSB.

A. Working Condition

For the successive approximations algorithm to work properly, the following condition has to be met:

$$b_i \le b_1 + \sum_{j=1}^{i-1} b_j \ , \ i \in [2, n] \qquad (5)$$

The working condition guarantees that the sum of the less significant bits of any bit b_i in the DAC is not inferior by more than one LSB to the bit itself (b_i). This ensures that if a bit b_i is rejected during a given step of the successive approximations algorithm, the remaining steps using only less significant bits cover the complete range of values up to the value just rejected.

IV. Sub-Binary Radix DACs

Using a binary-radix DAC with a successive approximations algorithm exploits the limit of the working condition. Indeed, for a binary-radix DAC, one can write:

$$b_i = b_1 + \sum_{j=1}^{i-1} b_j \ , \ i \in [2, n] \qquad (6)$$

Binary-radix DACs are difficult to design unless the number of bits is small, because the weight of each bit needs to be precisely set to avoid missing codes and redundancies. For this reason, they usually occupy an important circuit area.

The working condition of the successive approximations algorithm does not impose precise bit weights. Whereas missing codes are not allowed, redundancies are not

BNSDOCID: <XP_____31548289A_1 >

ANALOG EXHIBIT 1002
Page 300 of 321

problematic. This can be turned into an advantage, because it allows the use of imprecise converters. By voluntarily introducing redundancies, the risk of missing codes is reduced and the sub-binary converters can be designed using less effort and area without degrading the performance of the algorithm.

Figure 7 presents the input/output characteristics of a 4-bits radix-1.5 DAC. One can see that it has a resolution of 3 bits (the LSB is 1 on a full scale of 8), and that it presents several redundancies, in particular for the codes where the MSBs change values.

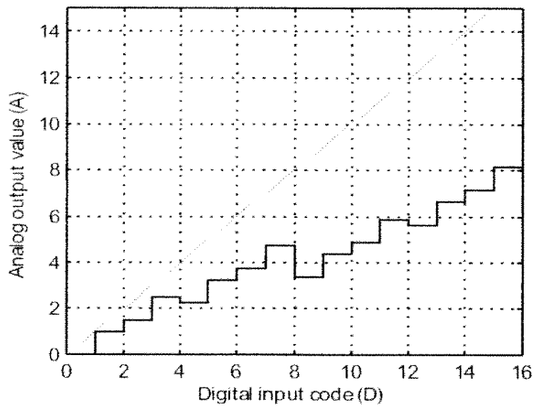


Figure 7. Input/output characteristics of a 4-bits radix-1.5 DAC.

It is noteworthy that the working condition of the successive approximations algorithm is achieved equally in each stage. This means that adding an extra bit does not imply an increase in circuit area for matching purpose. Each stage of the converter has a given area fixed by component mismatches, and adding an extra bit simply costs the area corresponding to one more stage.

Sub-binary converters should thus systematically be used with successive approximations algorithms. There is no reason for preferring a conventional radix-2 converter.

A. Radix choice

To limit the number of stages in the DAC, the radix should be chosen as high as possible (close to 2). However, the need to guarantee that the DAC will have no missing code, the maximum radix depends on component mismatch. Figure 8 presents the maximum radix R allowed for not violating the working condition of the successive approximations algorithm as a function of the worst-case component mismatch δ.

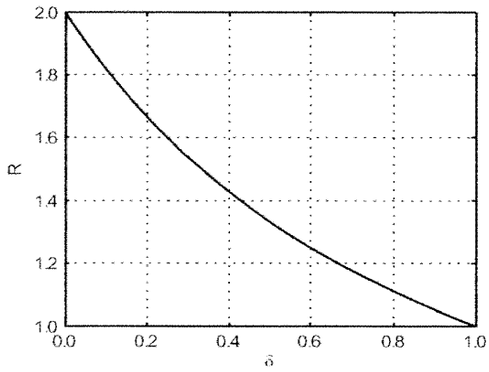


Figure 8. Maximum radix allowed for a given component mismatch.

It can be seen that for perfect components ($\delta = 0$), a radix-2 converter can be implemented. When the mismatch is 100%, the only choice is a thermometric scale, where each bit has the same weight. Typical values of mismatches lie around 10%, which corresponds to a radix value of 1.8.

B. Resolution

The full scale current of the DAC is chosen to cover the whole range of imperfection to be cancelled ($Imp_{uncompensated;max}$).

Then, the necessary resolution of the sub-binary DAC can be expressed as the ratio between the maximum magnitude of the imperfection to be compensated and the worst-case residual imperfection expected after calibration ($Imp_{compensated;max}$):

$$Resolution = \frac{FullScale}{LSB} = \frac{Imp_{uncompensated;max}}{Imp_{compensated;max}} \tag{7}$$

For a n-bits sub-binary radix-R DAC, the full scale is equal to:

$$FullScale = b_1 \frac{R^n - 1}{R - 1} \tag{8}$$

This corresponds to a radix-2 equivalent resolution of:

$$Resolution = \log_2\left(\frac{R^n - 1}{R - 1} + 1\right) \tag{9}$$

In practice, for radices close to 2, only a few additional bits are needed to reach the equivalent resolution of a radix-2 converter. A simple approximation gives:

$$N_{extra-bits} = N_{bits}\left(1 - \frac{R}{2}\right) \tag{10}$$

BNSDOCID: <XP_____31548289A_1_>

ANALOG EXHIBIT 1002
Page 301 of 321

where N_{bits} is the number of bits of the radix-2 implementation. This additional cost is negligible in terms of circuit area, because every stage in a sub-binary DAC occupies the same area and that the area per stage doesn't increase with resolution. This is not the case for binary radix DACs.

V. Sub-Binary R/2$^+$R DACs

Sub-binary radix DACs can be implemented advantageously in R/2R-like structures. Figure 9 shows such a ladder where the resistors in the vertical branches have a value xR, except the terminator which has a x_TR value.

When $x = x_T = 2$, the ladder is the well-known R/2R.

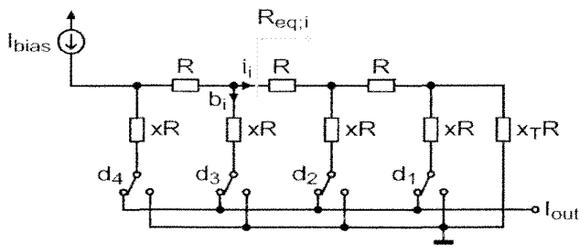


Figure 9. R/xR ladder.

For a R/2R ladder, the equivalent resistor $R_{eq;i}$ in each stage is equal to 2R. This implies that the current division in each branch is done equally, i.e. $b_i = i_i$. But since i_i is the sum of the least significant bits plus one LSB, equation (6) holds for this ladder. The consequence of this is that even the slightest mismatch on the resistor values translates into a missing code.

To avoid this situation, the ladder is made sub-binary by choosing a value of $x > 2$. The equivalent resistor $R_{eq;i}$ then becomes lower than xR, and the current division makes the sum of the remaining bits higher than the bit current:

$$b_i < i_i = b_1 + \sum_{j=1}^{i-1} b_j \qquad (11)$$

This is the favorable situation with respect to the working condition of the successive approximations algorithm (equation 5). The ladder now tolerates a resistor mismatch and the DAC will have no missing code if the radix, or equivalently the xR value, is chosen according to Figure 8.

VI. Sub-Binary M/2$^+$M DACs

The realization of sub-binary radix DACs with resistors is not optimal in terms of circuit area. An implementation based on transistors [8] is much more compact.

In the resistive ladder, each elementary resistor is replaced by a MOS transistor of fixed dimensions W over L (equal for all transistors). The gate voltages V_G are the same for all transistors in the ladder. At these conditions, the transistor-based circuit divides the current linearly as resistors [9][10].

Figure 10 shows the transistor translation (M/3M) of a R/3R ladder.

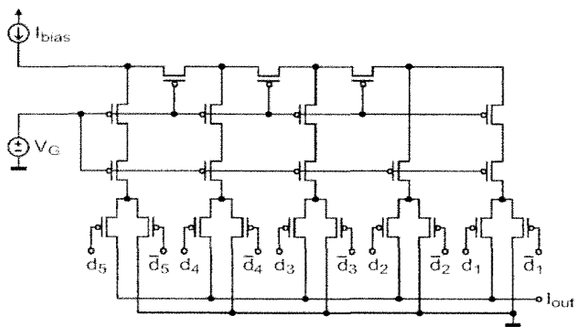


Figure 10. M/3M ladder.

In each stage horizontally, there is one single transistor implementing an equivalent R transistor. In each vertical branch, there are 3 transistors in series which implement an equivalent 3R resistor. In each stage, the two bottom-most transistors also have the role of switching the current either to the output or to ground. To achieve that, one transistor is biased with a gate voltage equal to V_G, which makes it behave like the third 1R resistor needed in each vertical branch, whereas the other transistor in parallel is disabled by applying a gate voltage equal to V_{dd}. In the network of Figure 10, an advantageous choice is to set $V_G = V_{ss}$, because this allows driving the d_i digital control signals directly with logic.

The penultimate (2) stage in the network is designed to generate locally a sub-binary current division for the LSB. Its implementation is kept as simple as possible so that the regular structure of the network is not broken.

Other radices can also be implemented with M/2$^+$M structures. Figure 11 shows an implementation of a M/2.5M ladder.

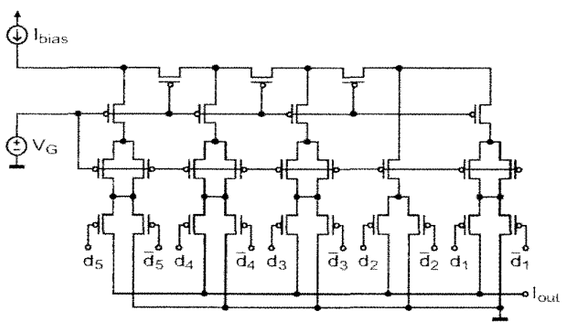


Figure 11. M/2.5M ladder.

In this circuit, the middle transistor in each vertical branch is put in parallel with a second one. The equivalent vertical resistance thus indeed becomes 2.5R.

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ANALOG EXHIBIT 1002
Page 302 of 321

The M/2.5M ladder exhibits a radix slightly higher than a M/3M ladder. This has the advantage of needing fewer additional bits, but imposes to have better matched transistors. Table I summarizes the characteristics of both networks.

TABLE I. M/2+M LADDER CHARACTERISTICS

Parameter	Value	
	M/2.5M	*M/3M*
Radix	1.86	1.77
Maximum allowed mismatch	7.3%	13%

A. Current collectors

The output current from the M/2$^+$M ladder can be collected by current mirrors. Figure 12 shows a differential output circuit collecting both currents from the current division network. The two outputs can be used to drive the compensation nodes, as shown in Figure 5.

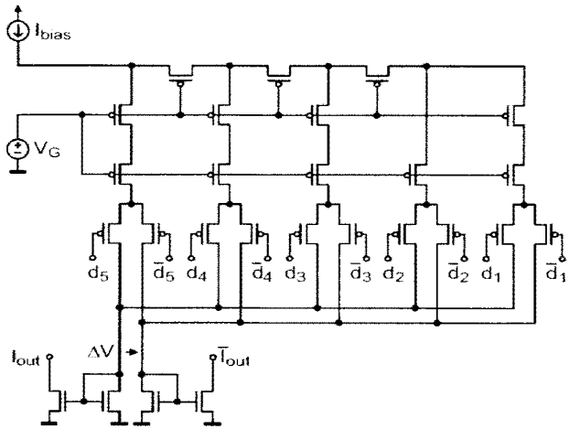


Figure 12. M/3M ladder with current collectors.

VII. CIRCUIT LAYOUT

The M/2$^+$M ladders are regular structures, whose layout can be done as arrays. Since the allowed transistor mismatch is around 10% and because an increased number of stages doesn't require better matching, the transistor dimensions (W and L) can be kept small. Figure 13 shows a micrograph of a 17 stages M/3M ladder, with two current mirrors as an output stage as in Figure 12, and a digital register used for storing the ADC input code. It can be observed that the DAC is smaller than the digital register, and that the output stage is also a compact structure.

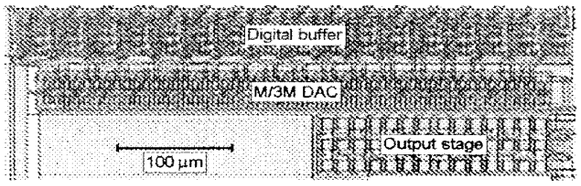


Figure 13. 17-stages M/3M ladder, with current collectors and input buffer.

VIII. CONCLUSION

The methodology presented in this paper allows the systematic and versatile compensation of imperfections in analog circuits using simple digital circuits and an area-efficient sub-binary DAC implementation. At the cost of a circuit area equivalent to only a few digital registers (including the DAC and its output stage), an imperfection can be corrected with an arbitrarily high resolution. This enables high-performance analog design even in deep sub-micron technologies, where process variability is problematic and the degrees of freedom for analog design are severely restricted.

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BNSDOCID: <XP_____31548289A__1_>

ANALOG EXHIBIT 1002
Page 303 of 321

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79124 7590 06/01/2010

MAXIM/BSTZ
Blakely Sokoloff Taylor & Zafman LLP
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Jessica A. Clark	(Depositor's name)
Jessica A Clark	(Signature)
August 31, 2010	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/390,684	02/23/2009	Rudy G. H. Eschauzier	55123P377	5595

TITLE OF INVENTION: AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1510	$300	$0	$1810	09/01/2010

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOE, HENRY	2817	330-009000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Blakely Sokoloff Taylor & Zafman LLP
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Number 14 B.V.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Bergschenhoek, Netherlands

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☒ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
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☐ Payment by credit card. Form PTO-2038 is attached.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-2666 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature Roger W Blakely Date August 31, 2010

Typed or printed name Roger W. Blakely, Jr. Registration No. 25,831

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
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For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 38062

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	12/390,684

Completed by (check one):

☐ Applicant/Inventor

☑ Attorney or Agent of record 25,831 (Reg. No.)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☐ Assignee recorded at Reel _____ Frame_____

Roger W. Blakely
Signature

Roger W. Blakely, Jr.
Typed or printed name

(714) 557-3800
Requester's telephone number

August 31, 2010
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☐ *** Total of _____forms are submitted.**

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal

Application Number:	12390684
Filing Date:	23-Feb-2009
Title of Invention:	AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS
First Named Inventor/Applicant Name:	Rudy G. H. Eschauzier
Filer:	Roger W. Blakely/Jessica Clark
Attorney Docket Number:	55123P377

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**1990**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/390,684	02/23/2009	Rudy G. H. Eschauzier	55123P377	5595

79124 7590 09/09/2010

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1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
CHOE, HENRY	
ART UNIT	**PAPER NUMBER**
2817	

MAIL DATE	DELIVERY MODE
09/09/2010	PAPER

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
12390684	2/23/09	ESCHAUZIER ET AL.	55123P377

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1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
Henry K. Choe	
ART UNIT	**PAPER**
2817	10

DATE MAILED:

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Commissioner for Patents

The IDS filed on 8/31/10 has been considered and entered.

/Henry K Choe/
Primary Examiner, Art Unit 2817

PTO-90C (Rev.04-03)

Receipt Date: 8/31/10

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	12/390,684
	Filing Date	02/23/2009
	First Named Inventor	Rudy G. H. Eschauzier
	Group Art Unit	2817
	Examiner Name	Choe, Henry
Sheet 1 of 1	Attorney Docket No: 55123P377	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/H.C./		US-2003/0214351	11/20/2003	Nandy, Tapas, et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
/H.C./		WO-2004/073163	08/26/2004	Wang, Zhenhua		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/H.C./		"Partial European Search Report Dated 07 July 2010", European Patent Application No. 10153869.2	
/H.C./		GUSTAT, HANS, "A DC-10 GHz amplifier with digital offset correction", Materials Science in Semiconductor Processing, Proceedings of the Second International SIGE Technology and Device Meeting (ISTDM 2004), Vol. 8, (13 October 2004), pp. 439-443	
/H.C./		PASTRE, MARC, et al., Methodology for the Digital Calibration of Analog Circuits and Systems, with Case Studies, Published by Springer, (2006), pp. 12-14, 23-35, 52-62, 106-107	
/H.C./		PASTRE, MARC, et al., "Methodology for the Digital Calibration of Analog Circuits and Systems Using Sub-binary Radix DACs", Mixed Design of Integrated Circuits and Systems, MIXDES 2009, 16th International Conference, (June 25-27, 2009), pp. 456-461	

EXAMINER	/Henry Choe/	DATE CONSIDERED	09/05/2010

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/390,684	10/12/2010	7812665	55123P377	5595

79124 7590 09/22/2010

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1279 OAKMEAD PARKWAY
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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 29 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

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APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Rudy G. H. Eschauzier, Bergschenhoek, NETHERLANDS;
Nico van Rijn, Katwijk, NETHERLANDS;

File History Content Report

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Document Date - 2018-04-12

Document Title - Applicant Communication Re: Payment of Maintenance Fee, 8th Year, Large Entity

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Document Title - Applicant Communication Re: Payment of Maintenance Fee, 12th Year, Large Entity

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UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

December 13, 2024

THIS IS TO CERTIFY THAT ANNEXED IS A TRUE COPY FROM THE RECORDS OF THIS OFFICE OF THE FILE WRAPPER AND CONTENTS OF:

APPLICATION NUMBER: ***12/390,684***
FILING DATE: ***February 23, 2009***
PATENT NUMBER: ***7812665***
ISSUE DATE: ***October 12, 2010***

UNITED STATES PATENT AND TRADEMARK OFFICE · DEPARTMENT OF COMMERCE

Certified by

Katherine Kelly Vidal

Performing the Functions and Duties of the
Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

PTO/SB/06 (12-04)

Filing Date: 02/23/09

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD
Substitute for Form PTO-875

Application or Docket Number
12/390,684

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**20** minus 20 =		x$26		OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**2** minus 3 =	*	x$110			x$220	
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	**1090**

APPLICATION AS AMENDED – PART II

		(Column 1)		(Column 2)	(Column 3)	SMALL ENTITY		OR	OTHER THAN SMALL ENTITY	
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)		RATE ($)	ADDI-TIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1)		(Column 2)	(Column 3)			OR		
		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE ($)	ADDI-TIONAL FEE ($)		RATE ($)	ADDI-TIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
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Search results for: PNS=(US7812665);
Collections searched: DWPI; ARIPO grant; Argentina UM; Argentina app; Armenia grant; Australia UM; Australia app; Australia grant; Austria UM; Austria app; Austria grant; Belarus UM; Belarus grant; Belgium app; Belgium grant; Brazil UM; Brazil app; Brazil grant; Bulgaria UM; Bulgaria app; Bulgaria grant; Canada app; Canada grant; China, Mainland UM; China, Mainland app; China, Mainland grant; Colombia app; Costa Rica UM; Costa Rica app; Croatia UM; Croatia app; Croatia grant; Cuba app; Cuba grant; Czech Republic UM; Czech Republic app; Czech Republic grant; Czechoslovakia grant; Denmark UM; Denmark app; Denmark grant; Estonia UM; Estonia app; Estonia grant; Eurasian (EAPO) grant; Europe (EP) app; Europe (EP) grant; Finland app; Finland grant; France app; France grant; Georgia grant; German Democratic Republic app; German Democratic Republic grant; Germany UM; Germany app; Germany grant; Greece app; Greece grant; Gulf Cooperation Council grant; Hong Kong UM; Hong Kong app; Hong Kong grant; Hungary grant; Iceland grant; India app; India grant; Indonesia UM; Indonesia app; Ireland UM; Ireland app; Ireland grant; Israel grant; Italy grant; Italy grant; Italy grant; Italy grant; Japan UM; Japan app; Japan grant; Korea UM; Korea app; Korea grant; Latvia grant; Lithuania grant; Luxembourgh app; Luxembourgh grant; Malaysia app; Malaysia grant; Mexico app; Mexico grant; Moldova UM; Moldova grant; Monaco grant; Mongolia UM; Mongolia grant; Morocco app; Morocco grant; Netherlands app; Netherlands grant; New Zealand grant; Norway app; Norway grant; OAPI grant; PCT (WO) app; Philippines UM; Philippines app; Philippines grant; Poland UM; Poland grant; Portugal UM; Portugal app; Portugal grant; Romania UM; Romania app; Romania granted; Russia UM; Russia app; Russia grant; Saudi Arabia app; Saudi Arabia grant; Serbia UM; Serbia app; Serbia grant; Singapore app; Singapore grant; Slovakia UM; Slovakia app; Slovakia grant; Slovenia UM; Slovenia grant; South Africa app; Spain UM; Spain app; Spain grant; Sweden app; Sweden grant; Switzerland app; Switzerland grant; Taiwan UM; Taiwan appl; Taiwan grant; Thailand UM; Thailand app; Thailand grant; Tunisia app; Turkey UM; Turkey app; UK app; UK grant; USSR grant; Ukraine UM; Ukraine grant; United States app; United States grant; Uruguay app; Vietnam UM; Vietnam app; Vietnam grant; Other

Table of Contents

1. US7812665B2 Amplifiers with input offset trim and methods

Family 1/1

1 record(s) per family

Record 1/1 US7812665B2 Amplifiers with input offset trim and methods

Title: Amplifiers with input offset trim and methods

Title - DWPI: Amplifier system has N-bit digital to analog (D/A) converter which is non-binary converter using radix of less than two for at least the most significant bits, while coupled to first amplifier

Priority Number: US2009390684A

Priority Date: 2009-02-23

Application Number: US2009390684A

Application Date: 2009-02-23

Publication Date: 2010-10-12

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
H03F000102	H	H03	H03F	H03F0001	H03F000102

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H03F000102	H	H03	H03F	H03F0001	H03F000102
H03F000130	H	H03	H03F	H03F0001	H03F000130
H03F000345	H	H03	H03F	H03F0003	H03F000345
H03K000522	H	H03	H03K	H03K0005	H03K000522
H03M000106	H	H03	H03M	H03M0001	H03M000106

Assignee/Applicant: Number 14 B.V.,Bergschenhoek,NL

JP F Terms:

JP FI Codes:

Assignee - Original: Number 14 B.V.

Any CPC Table:

Type	CPC - Current - Invention	CPC - Current - Additional	Version	Office
Current Current	**H03F 3/45753** H03M 1/0692	H03M 1/46 H03M 1/745	20130101 20130101	EP; US EP; US
Original Original	**H03F 3/45753** H03M 1/0692	H03M 1/46 H03M 1/745	20130101 20130101	US US

ECLA: H03F000345S3B3A1 | H03M000106M9R1 | T03M000146 | T03M000174J2

Abstract:

Amplifiers with power-on trim and methods using an amplifier system having an amplifier system input and an amplifier system output, an amplifier, a comparator, a successive approximation register having an input coupled to an output of the comparator, a first switch for switching an input of the amplifier from the amplifier system input to shorting the amplifier input, a second switch for switching an output of the amplifier from the amplifier system output to an input of the comparator, an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter, the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits, and an output of the D/A converter being coupled to the amplifier to control the input offset of the amplifier. Novel embodiments for the amplifier, comparator and D/A converter are disclosed.

Language of Publication: EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2022-04-12	MAFP	+
Description: MAINTENANCE FEE PAYMENT FEE PAYMENT YEAR 12 PAYMENT OF MAINTENANCE FEE, 12TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1553); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY		
2018-04-12	MAFP	+
Description: MAINTENANCE FEE PAYMENT FEE PAYMENT YEAR 8 PAYMENT OF MAINTENANCE FEE, 8TH YEAR, LARGE ENTITY (ORIGINAL EVENT CODE: M1552)		
2014-04-07	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 4		
2010-09-22	STCF	-
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2009-10-31	FEPP	-
Description: FEE PAYMENT PROCEDURE PAYOR NUMBER ASSIGNED (ORIGINAL EVENT CODE: ASPN); ENTITY STATUS OF PATENT OWNER: LARGE ENTITY		
2009-03-30	AS	-
Description: ASSIGNMENT NUMBER 14 B.V., NETHERLANDS ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNORS:ESCHAUZIER, RUDY G. H.; VAN RIJN, NICO; REEL/FRAME:022470/0349 2009-02-23		

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NUMBER 14 B.V.,BERGSCHENHOEK,NL	ESCHAUZIER, RUDY G. H.	2009-02-23	022470/0349	2009-03-30
	VAN RIJN, NICO	2009-02-23	-	-
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085				

Maintenance Status (US):

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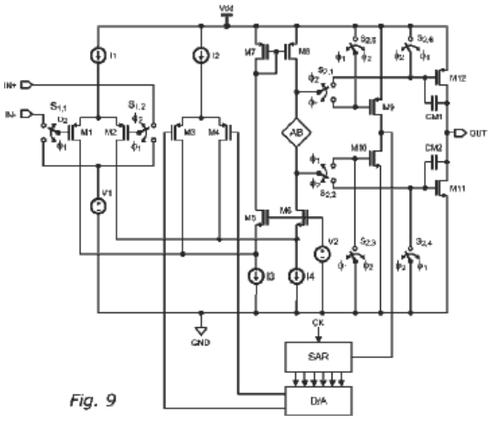


Fig. 9

Priority Number - DWPI: US2009390684A | US2010876008A
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AMPLIFIERS WITH INPUT OFFSET TRIM AND METHODS

PATENT #	APPLICATION #	FILING DATE	ISSUE DATE
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Payment Window Status

No maintenance fees are due.

WINDOW	STATUS	FEES
11.5 Year	Closed	Paid

Window	First Day to Pay	Surcharge Starts	Last Day to Pay	Status	Fees
3.5 Year	10/12/2013	04/15/2014	10/14/2014	Closed	Paid
7.5 Year	10/12/2017	04/13/2018	10/12/2018	Closed	Paid
11.5 Year	10/12/2021	04/13/2022	10/12/2022	Closed	Paid

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Entity Status UNDISCOUNTED

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