

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ANALOG DEVICES, INC.,
Petitioner,

v.

NUMBER 14 B.V.,
Patent Owner.

IPR2025-00551
U.S. Patent 7,812,665

DECLARATION OF DR. ION OPRIS (Ex. 1003)

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I, Dr. Ion Opris declare as follows:

1. I am over eighteen years of age, and I am competent to testify regarding the matters set forth in this declaration if called upon to do so.

2. I have been retained in this matter on behalf of Petitioner Analog Devices, Inc., (“ADI”).

3. I submit this declaration at the request of K&L Gates, counsel for ADI in this proceeding.

4. I have been asked to provide an opinion on U.S. Patent No. 7,812,665 (the “’665 Patent”). In preparing this declaration, I have studied the ’665 Patent (Ex. 1001 [’665 Patent]); its file history (Ex. 1002 [File History]); “A High-Performance Autozeroed CMOS Opamp with 550 μ V Offset,” Krummenacher et al., Solid-State Circuits Conference, 1997 Digest of Technical Papers, pp. 350-351, 483 (“*Krum*”) (Ex. 1005 [Krum]); U.S. Patent No. 7,642,846 (“*Yan*”) (Ex. 1007 [Yan]); U.S. Patent No. 6,486,806 (“*Munoz*”) (Ex. 1008 [Munoz]); U.S. Patent No. 7,265,611 (“*Wang*”) (Ex. 1009 [Wang]); U.S. Patent No. 5,789,974 (“*Ferguson*”) (Ex. 1010 [Ferguson]); “High-Precision DAC Based on a Self-Calibrated Sub-Binary Radix Converter,” M Pastre, M. Kayal, Electronics Laboratory (LEG) Swiss Federal Institute of Technology (EPFL), IMM-STI-LEG, CH-1015 Lausanne, Switzerland (“*Pastre*”) (Ex. 1013 [Pastre]); US Patent No. 4,336,526 (“*Weir*”) (Ex. 1014 [Weir]); “Optimal Resistor Ratio in the DAC with Low Precision Resistors – Statistical Approach,”

Dragović-Ivanović et al., Elektrotehnicki fakultet, University of Montenegro, 81000 Podgorica, Montenegro, Yugoslavia (“*Drago*”) (Ex. 1018 [Drago]); and U.S. Patent No. 4,465,996 (“Boyacigiller”) (Ex. 1019 [Boyacigiller]). I have also considered the other documents or references cited in this declaration.

5. In forming the opinions, I expressed below, I have considered the documents listed above, the relevant legal standards as provided to me by counsel, and my own knowledge and experience, as well as any other document referenced in this declaration.

6. I reserve the right to supplement my opinions in the future to respond to any arguments raised by the opposition and to take into account new information that becomes available to me.

I. BACKGROUND AND QUALIFICATIONS

7. This section briefly summarizes my career history education, publications, and other relevant qualification. My full *curriculum vitae* (“CV”) is included as Ex. 1004.

8. I received a Ph.D. in Electrical Engineering from Stanford University, Stanford, CA in 1996. I also hold an M.S. in Electrical Engineering from Stanford University, Stanford, CA in 1991 and a Diploma of Engineering Electronics and Telecommunications with highest honors from Bucharest Polytechnic Institute, Romania in 1986.

9. Since June 1996, I have been employed as an independent consultant at Opris Consulting designing analog, mixed-mode and ASIC IC devices, specializing in high performance analog circuits, such as analog to digital converters, digital to analog converters, communications circuits, and sensor interfaces.

10. I have completed over 200 design projects for extremely low power sensors read-out circuitry, ultrasonic imaging, audio/video interface products, CCD and CMOS light sensors, wired and RF data communications (DSL, Ethernet, RFID, Wi-Fi), MEMS accelerometers, gyroscopes, and MEMS based displays.

11. From April 2010 to October 2010, I was the Vice President of Product Design at MCube Inc. and from September 2009 to April 2010 I was also the Senior Director of IC Design responsible for the CMOS and MEMS design of MEMS base accelerometers and magnetic sensors.

12. From June 1994 to October 1997, I was a Principal Design Engineer at National Semiconductor Corp. responsible for system architecture and analog/digital circuit design for high speed/high resolution A/D converters, mixed-mode analog/digital ASICs, and complex behavioral simulations. I released to production a family of high performance 12-bit A/D converters.

13. From September 1990 to December 1995, I have also worked as a research assistant at Stanford University enrolled as a PhD candidate in Electrical Engineering conducting research in the areas of analog to digital converters, analog

nonlinear circuits and nonlinear control as well as low power/low noise amplifiers and continuous time filters for biological data acquisition.

14. From April 1989 to August 1990, I was a Design Engineer at Core International, Boca Raton, FL designing DMA adapters for tape drives and hard disk drives.

15. From 1991 to present, I have had various consulting jobs in hardware design/firmware with applications in RF data communication and spread spectrum technology.

16. Almost all analog circuits that I have worked on include design of operational amplifiers. Several projects with relevant experience in operational amplifiers design include as follows:

- several families of high speed, high resolution A/D converters, including the operational amplifiers embedded in these designs;
- several families of MEMS based sensors for accelerometer, gyroscopes and microphone application, including the operational amplifiers embedded in these designs;
- several sensor interfaces design for chemical or mechanical sensors based on resistive bridge sensors, including the operational amplifiers embedded in these designs.

17. I was ranked 2nd at the PhD Qualification Examination at Stanford University in January 1991 and awarded a School of Engineering Fellowship at Stanford University in 1990-1991.

18. I was ranked 1st in 1983, 1984, 1985, and 2nd in 1986 at the Romanian National Electronic Engineering contest. This is a highly competitive contest that is open to all undergraduate students in the country which tests both theoretical and practical skills.

19. I have been awarded over 85 US and international patents and I have authored over 30 technical papers.

20. Some of the relevant patents are:

- US Patent No. 7,375,665, (issued May 27, 2008) (“Image processing method and analog front end”);
- US Patent No. 6,130,632, (issued Oct. 10, 2000) (“Digitally self-cal D/A Converter”);
- US Patent No. 6,097,326, (issued Aug. 1, 2000) (“Algorithmic ADC with reduced DNL”);
- US Patent No. 5,929,796, (issued July 27, 1999) (“Self-calibrating reversible pipeline A/D and D/A converter”);
- US Patent No. 8,847,607 (issued Mar. 30, 1999) (“Split capacitor array for D/A conversion”); and

- US Patent No. 5,668,549 (issued Sept. 16, 1997) (“Radix-2 architecture and calibration technique for pipelined analog to digital converters”).

21. I am being compensated for my work associated with this case at my consulting rate of \$400.00 per hour. My compensation is not contingent on my opinions or the outcome of this case, and I have no other interest in the case or the parties thereto.

II. LEGAL STANDARDS

22. Although I am not a lawyer, I have been advised of the relevant legal principles by ADI’s counsel and have used them as a basis for my opinions. These are consistent with my understanding of the legal principles based on my prior experience with patent litigation matters.

A. Level of skill in the art

23. I understand that the person of ordinary skill in the art (POSITA) is a hypothetical person who is presumed to have known the relevant art at the time of the invention. I further understand that the factors that may be considered in determining the ordinary skill in the art include the following: the type of problems encountered in the art, prior art solutions to those problems, rapidity with which innovations are made, sophistication of the technology, and the educational level of workers in the field.

B. Claim Construction

24. I understand that the claims within a patent set forth what the inventors have presented as their inventions. I understand that claims can be independent or in dependent form, meaning that they depend from the identified independent claim and add requirements to those claims.

25. I understand that claim construction is a matter of law for the arbiter of law to decide. I further understand that claim terms should be given their ordinary and customary meaning within the context of the patent in which the terms are used, i.e., the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention in light of what the patent teaches.

26. I understand that to determine how a person of ordinary skill would understand a claim term, one should look to those sources available that show what a person of skill in the art would have understood disputed claim language to mean. Such sources include the words of the claims themselves, the remainder of the patent's specification, the prosecution history of the patent (all considered "intrinsic" evidence), and "extrinsic" evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.

27. I understand that a person of ordinary skill in the art is deemed to read a claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification. For

this reason, the words of the claim must be interpreted in view of the entire specification. The specification is the primary basis for construing the claims and provides a safeguard such that correct constructions closely align with the specification.

28. I understand that claim terms must be construed in a manner consistent with the context of the intrinsic record. In addition to consulting the specification, one should also consider the patent's prosecution history.

29. I understand that in addition to the intrinsic record, courts may also look to extrinsic evidence to construe claim terms. I understand that extrinsic evidence can be helpful in many ways, including to explain scientific principles, the meaning of technical terms, and terms of art that appear in the patent and prosecution history. However, any extrinsic evidence should be afforded less weight than the intrinsic evidence, as the intrinsic evidence is a better indicator of how the applicants understood their invention.

30. I understand that commonly, determining the ordinary and customary meaning of the claim requires examination of terms that have a particular meaning in a field of art. I understand that extrinsic evidence can educate the court regarding the field of the invention and can help the court determine what a person of ordinary skill in the art would understand claim terms to mean.

C. Invalidity

31. I understand that, unlike at the district court, patents subject to *inter partes* review, such as this proceeding, are not presumed to be valid, such that a lower burden of proof is used to judge the patentability of challenged claims. Unlike the district court's "clear and convincing" burden, here a "preponderance of the evidence" burden exists, meaning that to establish invalidity, the decision maker must simply find their factual findings "more likely than not."

1. Anticipation

32. I understand that a patent claim is invalid as "anticipated" by a single "prior art" reference if the reference discloses every single element of the claim with sufficient precision and detail to establish that the subject matter of the claim existed in the prior art. In particular, I understand that it is not sufficient to establish that all of the elements are collectively disclosed within the four corners of a particular document. Instead, the operative question is whether a person of ordinary skill would have understood the elements as being arranged as in the claim itself. I also understand that a prior art reference cannot "anticipate" a patent claim unless that reference enables one of ordinary skill in the art to make and use what is disclosed without undue experimentation. Thus, if the reference does not enable one of ordinary skill to make or use each and every claim limitation, then the claim cannot be "anticipated" by the reference.

33. I understand that a prior art reference can disclose a given claim element actually or inherently.

34. In the case of actual disclosure, I understand that a person of ordinary skill would need to have understood that the disclosure corresponds to the claim element in question. I also understand that such disclosure may be implicit rather than explicit. For example, prior art need not use the same words as the claimed invention. However, I understand that ambiguous references do not anticipate.

35. In the case of alleged “inherent” anticipation, I understand that the claim element in question must necessarily be present when practicing the described technology even though the prior art reference itself contains no express description of the element in question. In particular, I understand that “possibilities or probabilities” are not sufficient to establish inherency. The mere fact that a certain thing may result from a given set of circumstances is not sufficient. Instead, the essence of inherency is that one of ordinary skill in the art would recognize that a reference unavoidably teaches the property in question.

2. Obviousness

36. I understand that a patent claim may describe an invention that was new (i.e., not anticipated by any prior art reference), but nevertheless be invalid for “obviousness” if the differences between the patented subject matter and the prior

art are such that the subject matter as a whole would have been obvious to a person of ordinary skill in the art at the time of the invention was made.

37. I understand that an invention is not rendered obvious simply on the basis of two or more different disclosures that collectively disclose all of the claimed elements. In other words, an invention is not obvious just because all of the elements that comprise the invention may have been independently known in the prior art. Instead, a person of ordinary skill in the art must have had a reason or basis to make any alleged modification or combination as well as a reasonable expectation of success in pursuing the possibility that turns out to succeed and is claimed. In particular, I understand that knowledge of a goal does not itself render achievement of that goal obvious.

38. I also understand that determining whether or not a claimed invention would have been obvious requires assessing facts related to (1) the scope and content of the prior art, (2) the differences between the prior art and the claimed invention, (3) the level of ordinary skill in the art, and (4) any objective evidence (“secondary considerations”) of non-obviousness. I understand that this is known as consideration of the “Graham Factors.”

39. I further understand that an invention is not obvious just by demonstrating that each of its elements was, independently, known in the prior art. To prove that an invention is obvious, I understand that it can be important to point

to a reason or reasons, such as a teaching, suggestion, or motivation (although such a reason need not be found in the references themselves), that would have prompted a person of ordinary skill in the relevant field to combine or modify the elements in the way the claimed invention does. I understand that this is because inventions in most (if not all) instances rely upon building blocks already known, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known, therefore it can be important to point to such a reason or reasons. I understand that in identifying such a reason, the analysis need not require precise teachings in the prior art directed to the specific subject matter of the challenged claim.

40. I further understand that the reason or reasons that would have prompted a person of ordinary skill in the relevant field to combine or modify elements in the way the claimed invention does need not be the same reason or reasons identified in the specification of the challenged patent. Instead, the reason or reasons can be different from the alleged benefits or motivations identified in the specification of the challenged patent.

41. I understand that it will often be necessary for a court to look to interrelated teachings of multiple patents and the background knowledge possessed by a person having ordinary skill in the art in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the

patent at issue. I understand that any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed. I understand that when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. I understand that the combination of familiar elements according to known methods may be obvious when it does no more than yield predictable results.

42. I also understand that a claim is not invalid as obvious if it is more than the predictable use of prior art elements according to their established functions.

43. Further, I understand that while predictability is a touchstone of obviousness, the concept of a “predictable result” under the law refers not only to the expectation that prior art elements are capable of being physically combined, but also that the combination would have worked for its intended purpose.

44. I also understand that if the prior art teaches away from combining known elements in the manner claimed by the invention at issue, discovering a successful way to combine them is less likely to be obvious. In particular, I understand that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant, or would understand based on the reference that the line of

development flowing from the reference's disclosure is unlikely to be productive of the result sought by the applicant. Likewise, I understand that similar subject matter may not be sufficient motivation for a person of skill in the art to combine references if the references have conflicting elements.

45. Further, I understand that even if a reference does not necessarily “teach away,” its statements regarding preferences are relevant to a finding whether a person of ordinary skill would have had reason to combine that reference with another reference.

46. I also understand that one must be cautious and resist the temptation to rely on hindsight reasoning when attempting to combine references to suggest that a claim may be obvious. It is important to analyze validity based on the perspective of one at the time of the invention, which I understand is at least as early as the effective filing date. I understand that objective indicia (or “secondary considerations”) of non-obviousness or obviousness may be particularly probative and helpful in avoiding hindsight.

47. I also understand that the burden of persuasion concerning unpatentability (in other words, the ultimate burden to prove the relevant facts to the specified degree of certainty—here, preponderance of the evidence) remains at all times on the party challenging patentability. If the Board is left uncertain as to validity issues, Petitioner has thus failed to meet its burden.

III. LEVEL OF ORDINARY SKILL IN THE ART

48. I understand from counsel that the '665 Patent is analyzed from the viewpoint of a person of ordinary skill in the art ("POSITA") in and around May, 2009. My analysis and opinions below are given from the perspective of a POSITA in the technological field in the relevant time frame, unless stated otherwise.

49. I satisfied the definition of a POSITA long before the filing date of the application leading to the '665 Patent. I now consider myself an expert in the relevant field of technology for the '665 Patent.

50. It is my opinion that a POSITA of the '665 Patent would have a bachelor's degree in electrical engineering or a related field (or equivalent understanding through actual work experience) and had at least two or three years of experience relating to the design or implementation of analog integrated circuits. Also, additional professional experience could substitute for formal education and additional formal education could substitute for professional experience.

IV. TECHNICAL BACKGROUND

51. Operation amplifiers may exhibit input offset voltages (also called input referred offset voltage, input offset, voltage offset, or offset) due to imperfections in their circuitry. Ex. 1007 [Yan] 1:36-40. Offset voltages depend strongly on the matching of the used device and may also be impacted by other factors. Ex. 1009 [Wang] 1:18-21.

52. An offset voltage can be conceptualized as a voltage source at an input terminal of an opamp. Ex. 1009 [Wang] Fig. 1. Large offsets cannot be tolerated in precise applications. Ex. 1009 [Wang] 1:15-18.

53. Various systems have been used in attempts to compensate for offset voltages. For example, chopper stabilization, auto-zeroing, and correlated double sampling are all known techniques to compensate for offset voltages. Ex. 1007 [Yan] 1:40-44.

54. The '665 Patent itself acknowledges use of pre-package trimming and post-package trimming. Ex. 1001 ['665 Patent] 1:45-50. The '665 Patent specifically identifies *Krum* as a known approach to post-package trim. Ex. 1001 ['665 Patent] 2:22-33. *Krum* describes a system sometimes called auto-zeroing or offset calibration. Ex. 1005, 1.

55. The '665 Patent describes a prior art auto-zeroing system where an offset voltage V_{os} is compensated for through a successive approximation register (“SAR”) when a switch S shorts the inputs of an amplifier A depicted below:

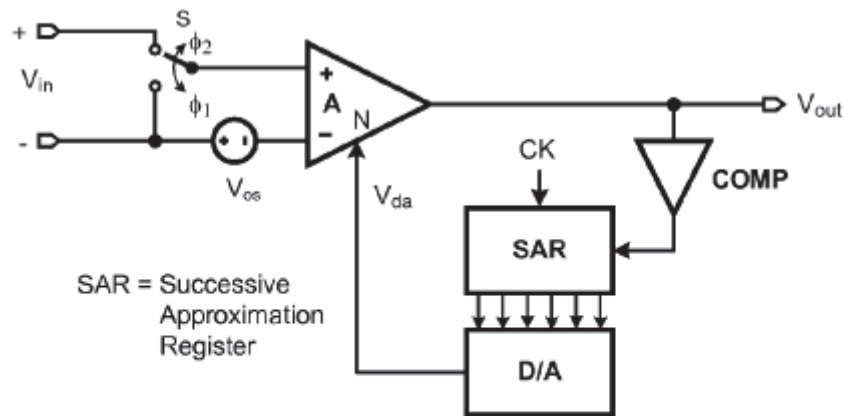


Fig. 1 (Prior Art)

Ex. 1001 ['665 Patent], Fig. 1, 2:41-42.

56. When the system is powered on, switch S shorts amplifier A's differential input. Ex. 1001 ['665 Patent] 2:48-51. The output of amplifier A is coupled to the comparator COMP, SAR, and D/A converter. The SAR and D/A Converter provide an output voltage V_{da} to compensate for the offset voltage V_{os} at the amplifier A offset compensation port N. Applying V_{da} to the compensation port, it can be thought of as subtracting from the input offset voltage V_{os} . Ex. 1001 ['665 Patent] 2:60-64. The residual offset determines an output error ϵ . Based on the sign of the error ϵ , the auto-zeroing systems will increase or decrease V_{da} until the value that minimizes the effects of the offset voltage is determined. Ex. 1001 ['665 Patent] 2:67-3:6.

57. V_{da} is provided based on a number of bits with different values, the most significant bit (MSB) having the highest value and the least significant bit (LSB) having the lowest value. A successive approximation system iteratively selects each bit (from MSB to LSB) until each bit state is determined and stored. Whether a bit state is stored as high or low depends on the sign of the error ϵ . Ex. 1001 ['665 Patent] 3:10-24.

58. One difficulty in SAR-based systems is the strict accuracy requirements of DAC elements to ensure SAR precision. For example, if a DAC element has an error greater than the magnitude of the least significant bit the system is unable to accommodate that error. Ex. 1014 [Weir] 2:13-15. Additionally, if a MSB has a value that exceeds the sum of all remaining bit values, an erroneously kept MSB cannot be compensated for. Ex. 1008 [Munoz] 2:24-40.

59. To reduce the accuracy requirements in the SAR, it was known to implement a DAC with a radix of less than 2. *See generally*, Ex. 1008, [Munoz]; Ex. 1014 [Weir]. In this context a radix is the ratio between successive bits in the DAC.

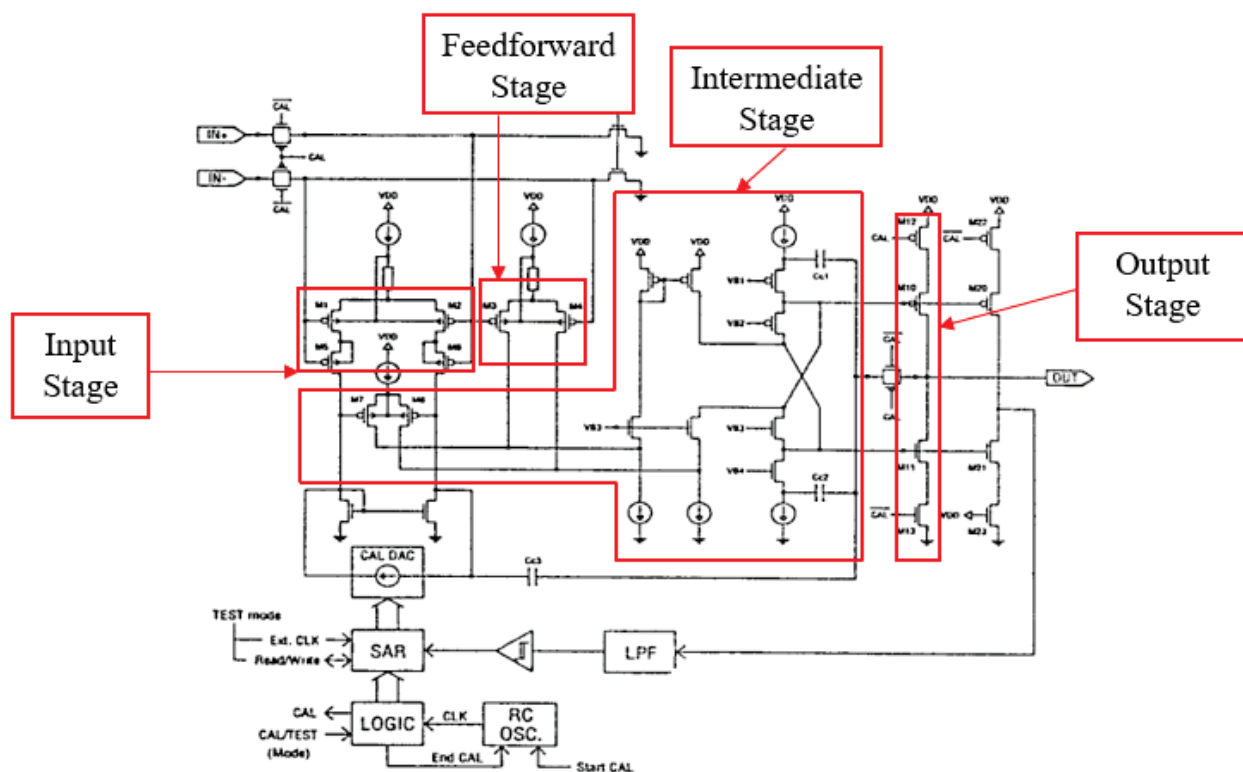
A. *Krum*

60. *Krum* is a proceedings condensate from a presentation at the International Solid-State Circuits Conference. Ex. 1005 [Krum] 1. *Krum* is cited in the '665 Patent background and was listed in its IDS. Ex. 1001 ['665 Patent] 2:30-

33; Ex. 1002 [File History] 29, 83, 128-129. *Krum* is dated February 8, 1997. Ex. 1005 [Krum] 2.

61. A condensate does not expressly provide all the technical details that were within the level of skill of a POSITA in 1997.

62. *Krum* provides a high-performance auto-zeroed opamp. Ex. 1005 [Krum] 1. The opamp is a three-stage amplifier. The first stage is a gain stage differential amplifier with M1/M2/M5/M6 and the NMOS loads. The intermediate stage is a folded cascode with M7/M8 and the current folding structure up to the output stage. The output stage is a single ended class AB with M10-M13. M3 and M4 is a feedforward stage for stability. This amplifier is annotated below:



Ex. 1005, 1, Fig. 1.

63. When the opamp performs autocalibration, the opamp inputs IN+ and IN- are disconnected from the first stage input and are shorted together to a ground using a first switch. Ex. 1005 [Krum] 1. The opamp output stage and the frequency compensation are disabled. Ex. 1005 [Krum] 1.

64. The opamp is auto-zeroed by connecting the opamp output signal through a low pass filter (LPF) and a Schmidt trigger to the SAR logic circuit. The CALDAC receives the digital code from the SAR logic and provides two currents at the output of the first gain stage to compensate for the input offset.

65. The output stage replica stage with M20-M21 sends the opamp output to a low-pass filter to reduce high-frequency noise, and to a Schmitt trigger. Ex. 1005 [Krum] 1. The SAR receives the signal from the Schmitt trigger and the CALDAC provides a differential current at the output of the first gain stage to compensate for the input offset. Ex. 1005 [Krum] 1.

B. Munoz

66. *Munoz* was filed on September 9, 1999 and issued as U.S. Patent No. 6,486,806 on November 26, 2002. Ex. 1008 [Munoz] Title Page.

67. *Munoz* describes systems and methods for adaptive auto-calibration of Radix<2 A/D SAR Converters with Internally Generated Stimuli. Ex. 1008 [Munoz] Title. *Munoz* identifies that in a binary sequence an n-bit DAC value may exceed

the sum of the remaining less significant bits, thus such a system is disadvantageous due to lack of redundancy. Ex. 1008 [Munoz] 2:24-27. This proves to be a problem if the MSB is erroneously kept during the successive approximation process because not even all of the remaining bits can compensate for this error. Ex. 1008 [Munoz] 2:27-32. *Munoz* notes that for this reason, systems with a radix of 2 are disadvantageous due to their lack of redundancy. Ex. 1008 [Munoz] 2:32-42. By redundancy, *Munoz* is referring to having multiple digital representations of a particular output voltage or analog level. Ex. 1008 [Munoz] 2:40-42. Gaps in the analog output range can be reduced by having overlap between different analog output regions.

68. Munoz outlines a successive approximation system converter in Fig. 2:

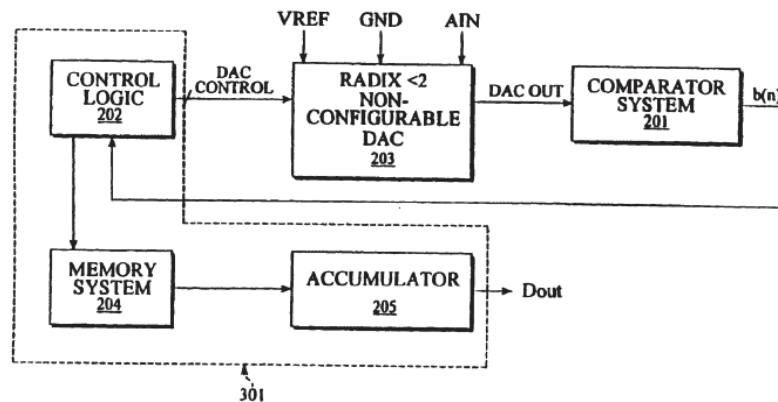


Fig. 2

Ex. 1008 [Munoz] Fig. 2, 6:16-24. As depicted, this system requires use of a DAC, which is described in more detail in Fig. 3A and 3B.

69. For example, Fig. 3A illustrates a charge redistribution DAC, which Munoz refers to as a DAC:

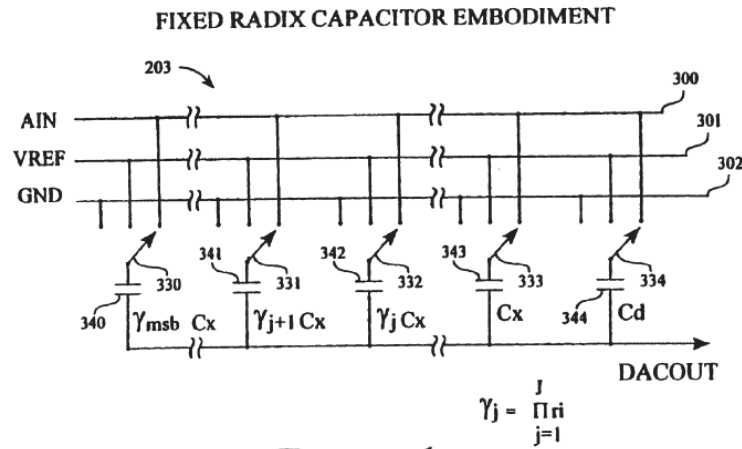


Fig. 3A

Ex. 1008 [Munoz] Fig. 3A.

70. The DAC includes an input voltage (AIN) lead 300, a ground (GND) lead 302, a reference voltage (VREF) lead 301, multiple switches 330-334 and capacitors 340-344. Ex. 1008 [Munoz] 6:45-60. The capacitance of a capacitor γ_j , is given by the formula $\gamma_j = \prod_{i=1}^J r_i$ where r_i is the radix value. Ex. 1008 [Munoz] 7:3-10. These separate capacitors 330-334 correspond to the separate bits (from LSB to MSB) in the successive approximation register. The radix value, r_i is designed to have a value between one and two, but the value may vary for each capacitor pair. Ex. 1008 [Munoz] 7:10-13.

71. An alternative structure for the DAC may include Fig. 3B:

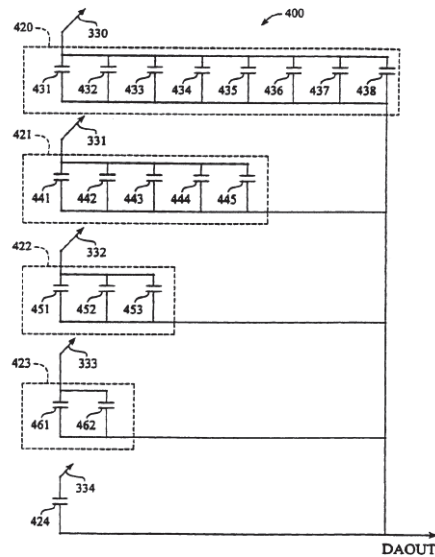


Fig. 3B

Ex. 1008 [Munoz] Fig. 3B.

72. Rather than the individual capacitors of Fig. 3A, Fig. 3B includes multiple separate banks of unit capacitors 420-424 connected by switches 330-334. Ex. 1008 [Munoz] 7:30-34. The unit capacitor banks achieve relative capacitances of 8 (for bank 420), 5 (bank 421), 3 (bank 422), 2 (bank 423) and 1 (bank 424). Ex. 1008 [Munoz] 7:54-60. Here in Fig. 3B, as with Fig. 3A, the radix value of corresponding bits in the successive approximation process is the ratio between successive banks of capacitors. *See* Ex. 1008 [Munoz] 7:57-8:13. In Fig. 3B, the radix values for the bits are variable. From MSB to LSB, the radix is $8/5$, $5/3$, $3/2$, and $2/1$. While *Munoz* uses capacitors, *Munoz* explains that other components may be substituted for the capacitors. Ex. 1008 [Munoz] 6:67-7:3 (“Instead of capacitors, other charge carrying components such as resistors can be substituted as a separate

embodiment according to the present invention.), 9:18-19. As such, a POSITA would understand the teachings of *Munoz* to equally apply to the use of resistors or current sources in place of the depicted capacitors, in particular with applications that require a continuous time analog level.

73. In addition to these embodiments, *Munoz* specifies that a radix of 1.7 and 1.9 may be utilized in its opamp. Ex. 1008 [*Munoz*] 17:43-45.

C. Yan

74. *Yan* was filed on October 30, 2007 and issued as U.S. Patent No. 7,642,846 on January 5, 2010.

75. *Yan* describes “apparatuses and methods for providing offset compensation for operational amplifiers.” Ex. 1007 [*Yan*] Title. *Yan* depicts a schematic for a conventional amplifier with offset compensation for auto-zeroing:

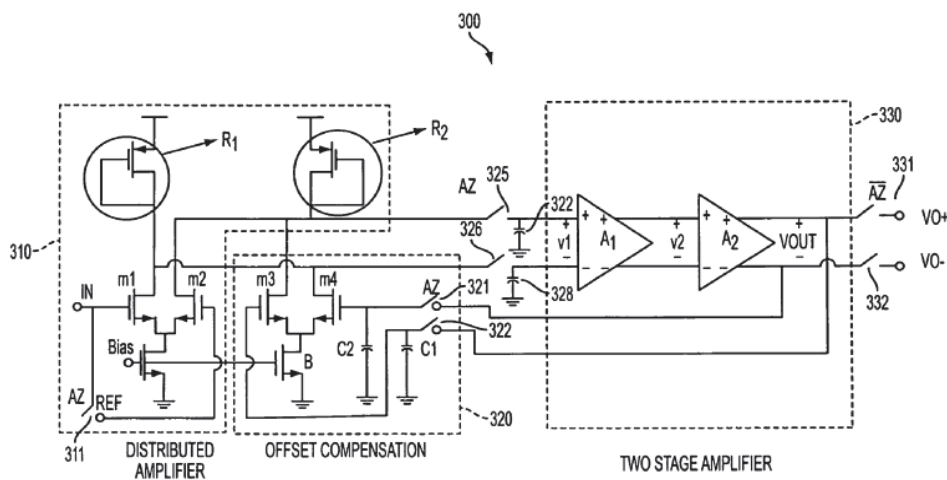


FIG. 3
PRIOR ART

Ex. 1007 [*Yan*] Fig. 3.

76. *Yan* includes an amplifier block 330 coupled to an input gain stage 310 and an offset compensation stage 320. Ex. 1007 [*Yan*] 2:22-25. The gain stage 310 includes the differential pair m1, m2 and the offset compensation stage 320 includes the differential pair m3, m4 and both transconductance amplifiers have their outputs connected together. Ex. 1007 [*Yan*] 2:25-34, Fig. 3. The offset compensation circuit 320 receives the auto-zero analog levels through switches 321 and 322 from the rest of the system.

D. Wang

77. *Wang* claims priority to a foreign filing filed February 11, 2003, was filed on January 28, 2004 as a PCT application and issued as US Patent No. 7,265,611 on September 4, 2007. Ex. 1009 [*Wang*] Title.

78. *Wang* describes a system used in self-zeroing for critical, continuous-time applications. Ex. 1009 [*Wang*] Title. *Wang* automatically compensates for a range of offset voltages in opamps without significant circuit overhead while still maintaining high precision. Ex. 1009 [*Wang*] 1:63-2:4. *Wang's* system involves a successive approximation register analog to digital converter. Ex. 1009 [*Wang*] 2:53-3:7. An example of *Wang's* system is provided in Fig. 3:

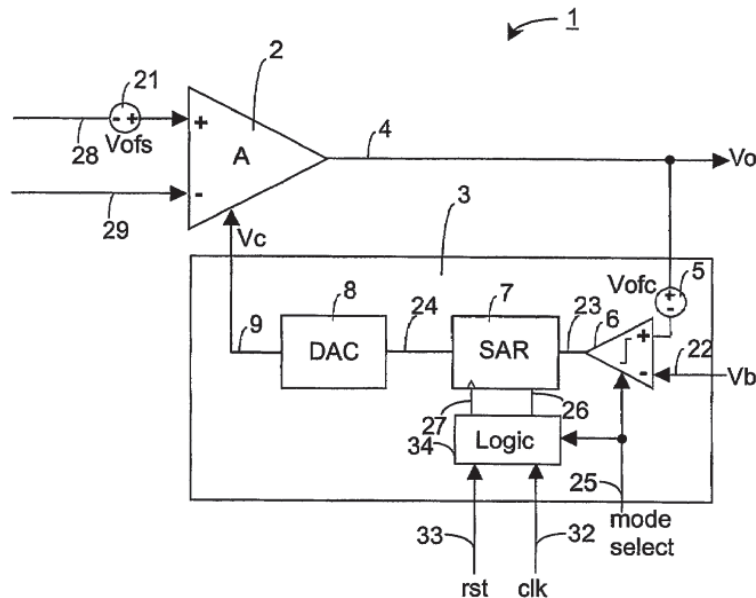


Fig. 3

Ex. 1009 [Wang] Fig. 3.

79. Much like the applicant admitted prior art of the '665 Patent, *Wang's* system also includes opamp 2, a comparator 6, a SAR, 7, and DAC 8. Ex. 1009 [Wang] 3:9-13. *Wang's* scheme works with all kinds of DACs. Ex. 1009 [Wang] 8:36-39. The SAR implement resembles a convention implementation besides for the DAC output signal being applied to one node of the opamp 2. Ex. 1009 [Wang] 3:30-35. Additionally, input 28 receives a DC voltage in the self-zeroing mode. Ex. 1009 [Wang] 3:35-38.

80. During auto-zeroing, the opamp is isolated from the previous stage with several switches S1 and S2 shown in Fig. 5:

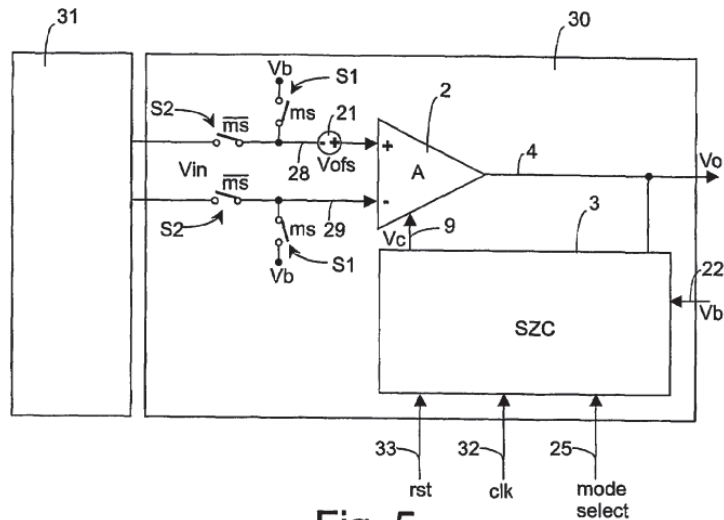


Fig. 5

Ex. 1009 [Wang] Fig. 5, 4:42-45. Switches S1, when closed, short the inputs of the opamps together and to the bias level Vb. The switches S1 and S2 switch the opamp from normal operation and self-zeroing mode; S2 are closed for normal operation and S1 is closed for auto-zeroing.

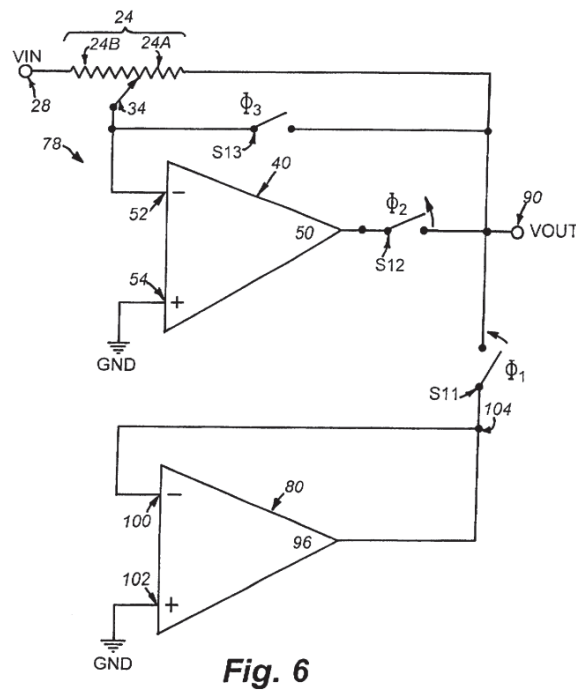
E. Weir

81. *Weir* was filed on April 22, 1980 and issued as US Patent No. 4,336,526 on June 22, 1982. Ex. 1014 [Weir] Title.

82. *Weir* is directed towards a successive approximation analog-to-digital converter using a non-binary series. Ex. 1014 [Weir] Title. *Weir* explains that “a convention successive approximation A/D converter employs a digital to analog converter (DAC) in a feedback loop with a comparator and a logic circuit referred to as a ‘successive approximation register’.” Ex. 1014 [Weir] 1:23-26. *Weir* recognizes that “each DAC element in the series must be accurate to a degree which

86. *Ferguson* provides systems for calibrating the dc-offset of amplifiers.

Ex. 1010 [Ferguson] Title. *Ferguson* teaches a circuit which is designed to reduce voltage glitches at an output of a circuit when an output of an amplifier is switched out and back into the circuit, like during offset calibration. Ex. 1010 [Ferguson] 11:64-67. An example of this circuit is provided in Fig. 6:



Ex. 1010 [Ferguson] Fig. 6.

87. The circuitry includes multiple switches S11, S12, and S13 and a catching amplifier 80. The catching amplifier 80 may be significantly smaller than the main amplifier 40. Ex. 1010 [Ferguson] 12:13-22. The three switches are open and closed based on separate clocks to have the effect of muting the amplifier. Ex. 1010 [Ferguson] 12:22-51.

88. For example, the switch S11 connects the output 96 of the catching amplifier 80 and output node 90 of the circuit during $\phi 1$. Ex. 1010 [Ferguson] 12:26-29. Switch S12 is connects the output 50 of the main amplifier 40 and output node 90 during $\phi 2$. Ex. 1010 [Ferguson] 12:29-33. Switch S13 connects the output node 90 and inverting input 52 of the main amplifier 40 to force the main amplifier 40 in a muting configuration during $\phi 3$. Ex. 1010 [Ferguson] 12:33-37.

89. When switch S11 is closed and switch S12 is open, output 90 of the circuit is driven by the catching amplifier 80 and will be configured to have a gain of about zero between the input node 28 and output node 90. Ex. 1010 [Ferguson] 12:57-61.

90. The following Figures depict the timing arrangements for $\phi 1$, $\phi 2$, and $\phi 3$ for entering (Fig. 8) and existing (Fig. 9) a calibration cycle:

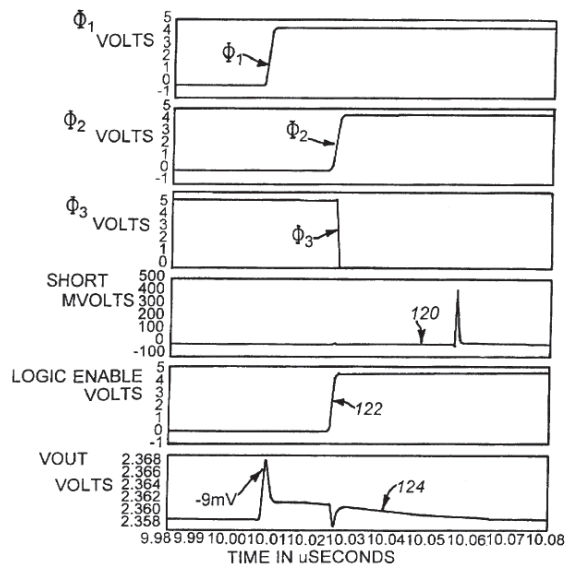


Fig. 8

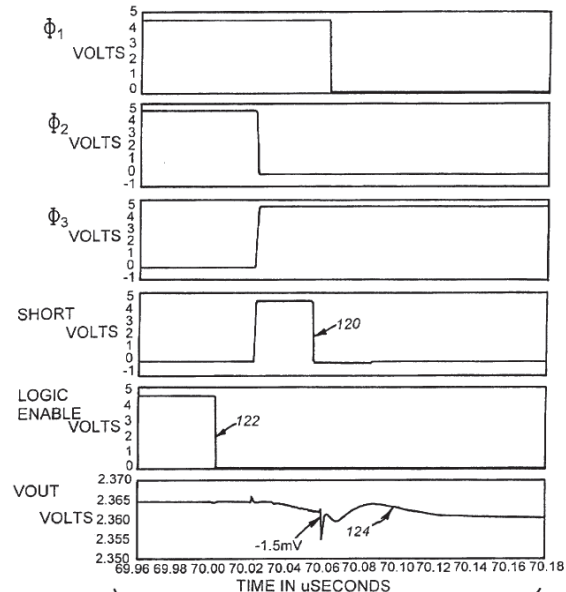
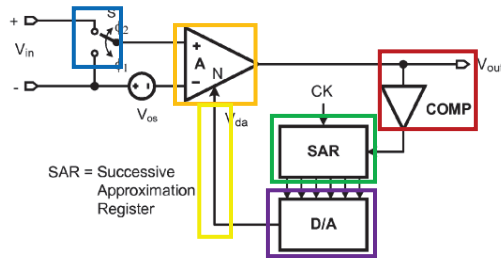


Fig. 9

Ex. 1010 [Ferguson] Fig. 8, Fig. 9; *See also* Ex. 1010 [Ferguson] 13:15-14:7.

V. THE '665 PATENT

91. The '665 Patent is directed towards an apparatus for auto-zeroing the input offset voltage of an amplifier. Ex. 1001 ['665 Patent] Cl. 1. In comparison to the applicant admitted prior art annotated below, Claim 1 adds a second switch and specifies that the D/A converter uses a radix of less than 2 for at least the most significant bits:



1. An amplifier system having an amplifier system input 35 and an amplifier system output comprising:

a first amplifier;

a comparator;

a successive approximation register having an input coupled to an output of the comparator;

a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

a second switch for switching an output of the first amplifier from the amplifier system output to an input of the 45 comparator;

an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits; 50

an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

Ex. 1001 [Ferguson] Fig. 1; Cl. 1. During prosecution, the Examiner found that the prior art taught all elements other than the second switch and allowed the '665 Patent. Ex. 1002 [File History] 213.

VI. CLAIM CONSTRUCTION

92. I have been informed by counsel that claim terms must receive their ordinary and customary meaning as would have been understood by a POSITA based on the specification, prosecution history, and extrinsic evidence.

A. “non-binary converter using a radix of less than 2 for at least the most significant bits” [claim 1]

93. The term *radix* is not defined in the '665 Patent specification. *See generally* Ex. 1001 ['665 Patent]. A POSITA would understand this term, “radix”, as addressing the ratio between two successive elements, such that it is my opinion that the term be construed as requiring the element ratio between bit N and bit (N-

1), and the element ratio between bit (N-1) and bit (N-2), to each be lower than 2, where the converter has N bits, and where the MSB is bit N and the LSB is bit 1.

94. In the context of successive approximation, a radix is the ratio between two elements associated with consecutive bits. However, the '665 Patent appears to apply this term to one bit, as opposed to two bits. Ex. 1001 ['665 Patent] Cl. 3. Claim 3 recites “the radix for the least significant bit is 2[,]” while Claim 1 uses bits (plural).

95. Thus, consistent with the patent language, the radix for an arbitrary bit P (not the MSB) is understood to refer to the ratio between the element (P+1) and the element P.

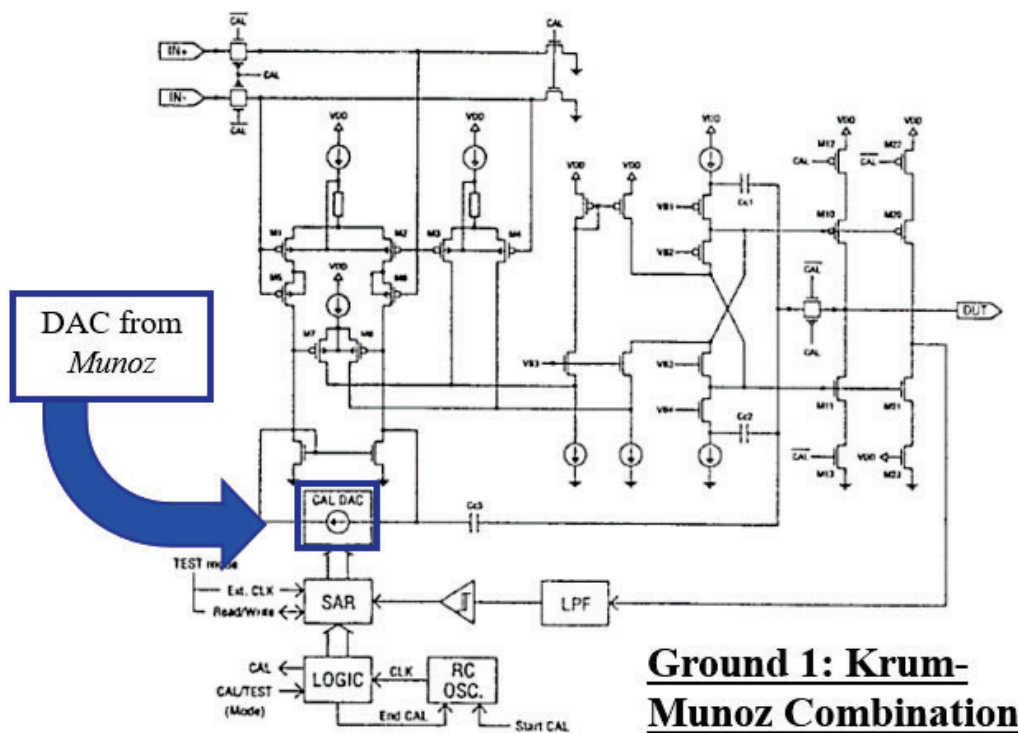
B. “coupled”, “being coupled” [claims 1, 5, 6, 7, 8]

96. The '665 Patent uses the term “coupled” only in the claims, and not in the specification. *See generally* Ex. 1001 ['665 Patent]. A POSITA would understand coupled to address a connection, either directly or indirectly, from one component to another. It is therefore my opinion that “coupled” or “being coupled” would be understood by a POSITA to mean connecting directly or indirectly through one or more intervening devices.

VII. GROUND 1 – *KRUMIN* VIEW OF *MUNOZ*

97. Ground 1 relies upon the high-performance auto-zeroed opamp of *Krum*, which a POSITA would then improve with the DAC system using a radix of

less than two described in *Munoz*. A diagram consistent with this combination is depicted below:



98. *Krum* itself includes a CMOS opamp capable of compensating the offset using a binary-weighted DAC driven by a SAR. This system is very similar to the system described in the '665 Patent and includes the claimed second switch. However, *Krum* lacks a radix of less than 2, which a POSITA would, as I outline below, seek to include.

99. *Munoz* clearly describes a DAC using a radix of less than two, instead of a binary weighted scheme. The combination of the two references renders the '655 Patent obvious.

A. Motivation to Combine

100. A POSITA would be motivated to improve the auto-zeroed opamp of *Krum* with the nonbinary-weighted DAC of *Munoz*.

101. *Krum* falls in the same field of endeavor of the '665 Patent because it describes an operational amplifier with offset compensation circuitry Ex. 1005 [Krum] 1. Likewise, *Munoz* address a pertinent problem of the '665 Patent because it improves the functionality of a successive approximation (like the one used in the '665 Patent) by implementing redundancy. Ex. 1008 [Munoz] Abstract.

102. A POSITA interested the “High-Performance Autozeroed CMOS Opamp” of *Krum* would recognize and that the teachings of *Munoz* could be utilized to improve *Krum* and be motivated to do so.

103. A POSITA would be motivated to implement *Munoz*'s DAC into *Krum*'s Opamp because (1) *Krum* specifically requires a monotonic DAC and *Munoz*'s DAC is monotonic; and (2) *Munoz*'s DAC provides redundancy which reduces the gaps at the DAC output and enables the system to recovery from a noise induced or erroneous MSB.

104. *Krum*'s system includes a DAC labeled CALDAC. Ex. 1005 [Krum] 1. The CALDAC must guarantee monotonicity. Ex. 1005 [Krum] 1 (“The linearity of the CALDAC, however, is not important as long as its monotonicity is

guaranteed.”). A POSITA reading *Krum* would be motivated to look to references that also provide a monotonic DAC.

105. *Munoz’s* DAC is monotonic. *Munoz* describes a “companion bit approximation [that] uses successive sets of radix scaled balancing capacitors ***monotonically*** to approach the level of the sampled voltage.” Ex. 1008 [Munoz] 8:55-58. The companion bit described in *Munoz* is used during a successive approximation and “ensures monotonicity in successive approximation and avoids erroneous, noise-induced including of a too-large balancing capacitor in the final set of balancing capacitors.” Ex. 1008 [Munoz] 9:11-17. Use of the companion bit “provides an envelope or margin which prevents noise induced over approximation of sampled values” which “promotes monotonicity and convergence to the approximated value without discontinuance or gaps in resolution.” Ex. 1008 [Munoz] 16:53-58.

106. Even though monotonicity is not required for the auto-zeroing calibration, the fact that *Munoz’s* DAC is monotonic does not prevent its use in this auto-zeroing application.

107. Accordingly, a POSITA, reading *Krum* (which requires a monotonic DAC) would be motivated to implement *Munoz’s* DAC which “remains monotonic and symmetrically noise tolerant during decision making incident to successive approximation.” Ex. 1008 [Munoz] 17:45-48.

108. A POSITA would also be encouraged and motivated to use *Munoz's* system due to the designed redundancy.

109. Munoz teaches that “with a radix 2 series, there is no redundancy which permits alternative expressions of particular voltage or capacitance levels” leading to “the binary non-overlap problem” Ex. 1008 [Munoz] 1:66-2:4, 2:40-42. Munoz proposes a system that uses redundant alternative expressions in the DAC to approximate particular values in case there is an erroneous bit decision. Ex. 1008 [Munoz] 5:67-6:2, 7:67-8:5.

110. Alternative expressions of particular voltage or capacitance levels allows the system to recover when a MSB is erroneously bit decision when a radix of less than two is implemented in the DAC. Ex. 1008 [Munoz] 7:67-8:13.

111. A POSITA would have been motivated to use *Munoz's* DAC with a radix less than 2 to improve *Krum's* system and avoid gaps in the DAC output and/or recover in the event of an erroneous, noise-induced approximation step. Ex. 1008, 5:15-21.

112. A POSITA would also appreciate the benefit in avoiding gaps in DAC outputs. The problem of gaps in the converter output is well known. Ex. 1013 [Pastre] 1 (“This important feature allows guaranteeing that the converter will have no missing code, even when low-precision components are used.”); Ex. 1018 [Drago] 1 (“In this way, we can guarantee the smallest possible gaps in input/output

characteristics”); Ex. 1019 [Boyacigiller] 2:10-15 (“If a conventional binary weighted DAC were utilized, gaps might appear in the output range of the DAC, with the result that certain desired correction analog output could not be generated. The use of a non-binary weighting overcomes this problem.”).

113. Indeed, the use of a DAC having a radix of less than 2 allows the use of DAC elements with greater mismatches (thus smaller elements) and still avoid large gaps in the DAC output range. Ex. 1013 [Pastre] 1.

114. It is my opinion that a POSITA would also be capable of combining *Munoz* and *Krum* with a reasonable expectation of success. Like the CALDAC in *Krum*, *Munoz*’s DAC is implementing with a control logic circuit. Ex. 1005 [Krum] 1 (“Each opamp is protected against short-circuits and has its own biasing, calibration DAC and control logic.”); Ex. 1008 [Munoz] 4:58-60 (“The control logic circuitry 102 is connected to the configurable DAC 103 with DAC control signals including SAR control signals and configuration control signals”).

115. As both systems involve successive approximations, the control logic of *Krum* can be applied to *Munoz*’s DAC with routine engineering. Ex. 1005, 1; Ex. 1008 [Munoz] 4:58-60. A POSITA would be capable of implementing *Munoz*’s DAC in *Krum*’s system by replacing *Krum*’s CALDAC with routine engineering.

116. Further, while *Krum*’s DAC is implemented as a current mode DAC (Ex. 1005 [Krum] 1), *Munoz* DAC is described generally and *Munoz*’s teachings are

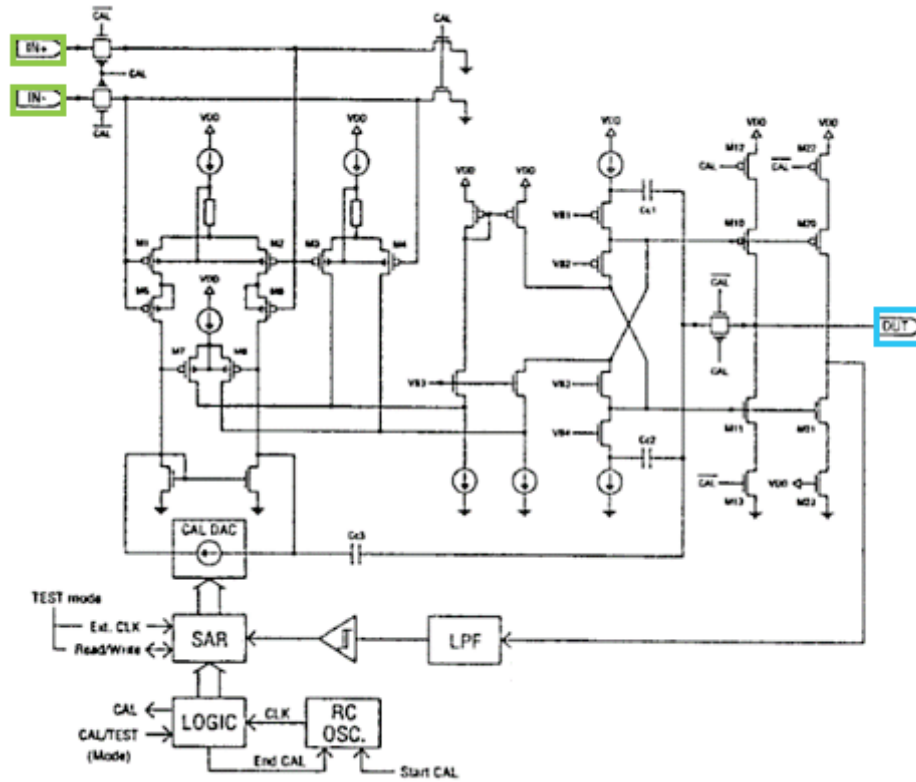
applicable to all types of DACs. Additionally, *Munoz* notes its system could use resistors rather than capacitors. Ex. 1008 [Munoz] 6:67-7:3.

117. For all these reasons, a POSITA would be both motivated and capable of achieving a combination between *Krum* and *Munoz*.

B. Independent Claim 1

1. [1pre] An amplifier system having an amplifier system input and an amplifier system output comprising:

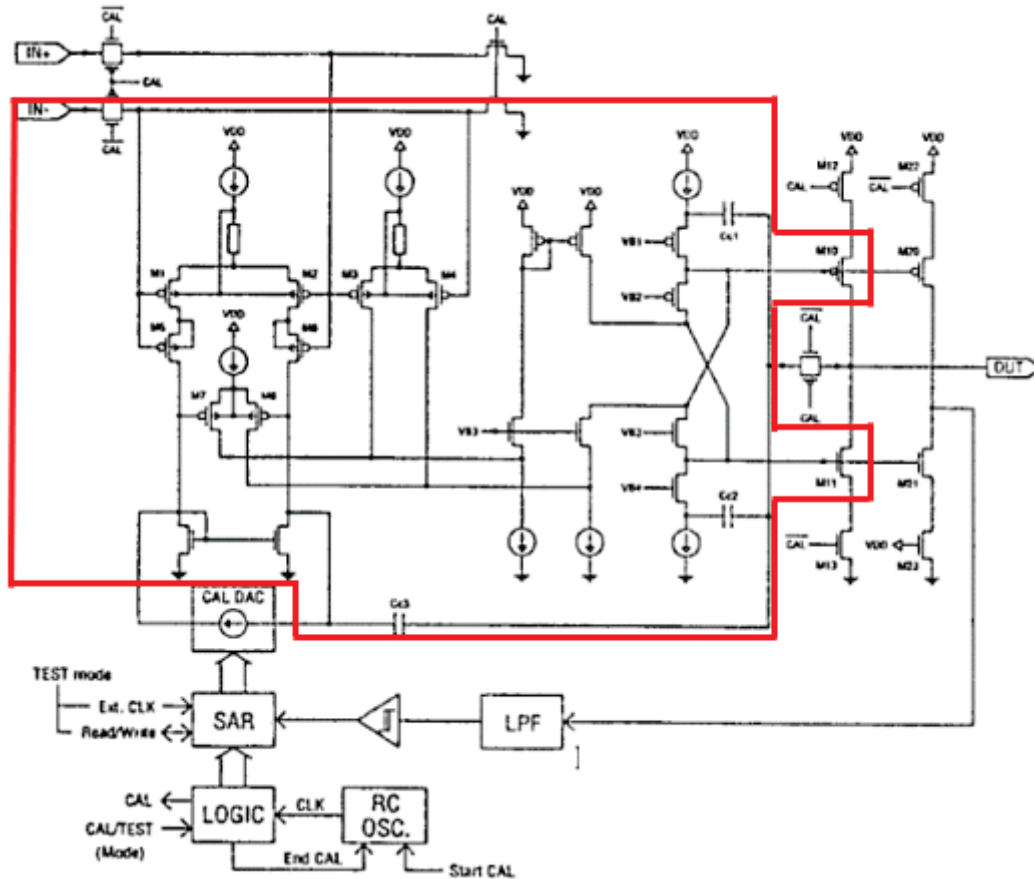
118. I have no opinion as to whether the preamble of Claim 1 is limiting. However, the preamble is obvious in light of the *Krum-Munoz* combination. For example, *Krum* discloses an amplifier circuit with an output (OUT) (in blue) and a differential inputs (IN+ and IN-) (in green):



Ex. 1001 [Krum] Fig. 1.

2. [1a] a first amplifier;

119. This limitation is obvious in light of the *Krum-Munoz* combination. For example, annotated below (in red) is an amplifiers:



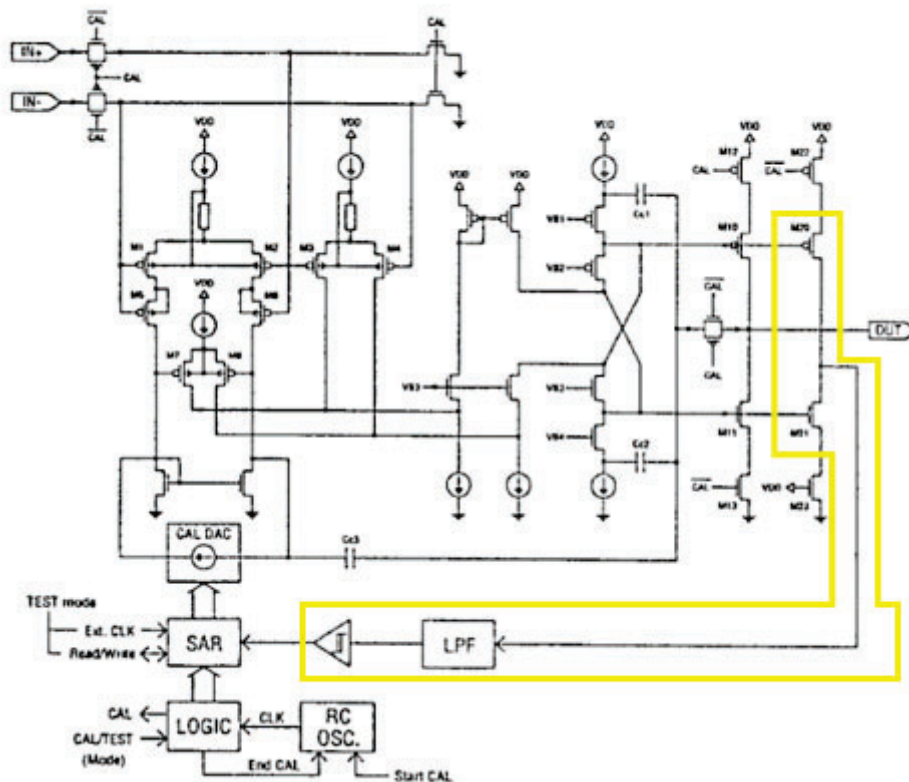
Ex. 1005 [Krum] Fig. 1.

120. *Krum's* disclosure of an amplifier is clear from its title of “A High-Performance Autozeroed CMOS Opamp with 50 μ V offset.” Ex. 1005 [Krum] Title.

3. [1b] a comparator;

121. This limitation is obvious in light of the *Krum-Munoz* combination.

122. Krum depicts a comparator system (in yellow):



Ex. 1005 [Krum] Fig. 1.

123. The comparator system includes M20, M21, a low pass filter (LPF) and a Schmitt trigger. The transistors M20 and M21 are used to provide a replica amplifier output signal to the calibration circuit. The replica signal of transistors M20 and M21 are replicas of the signals into transistors M10 and M11 respectively. The LPF's role is to eliminate high-frequency noise. Ex. 1005 [Krum] 1. The Schmitt trigger functions as a comparator with hysteresis.

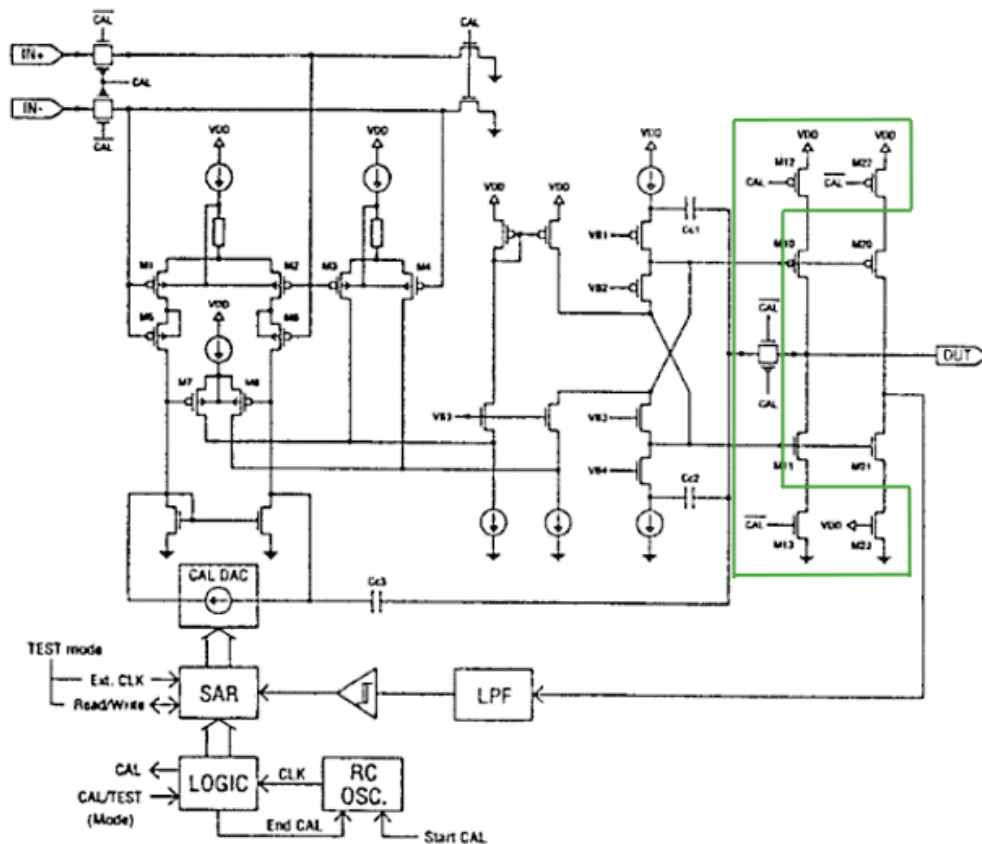
4. [1c] a successive approximation register having an input coupled to an output of the comparator;

124. This limitation is obvious in light of the *Krum-Munoz* combination.

6. [1e] a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator,

130. This limitation is obvious in light of the *Krum-Munoz* combination.

131. For example, *Krum* includes a second switch system (in green):



Ex. 1005 [Krum] Fig. 1.

132. A POSITA would appreciate the connection between M23 and VDD in Fig. 1 of *Krum* is a typographical error in Fig. 1. M23 should be connected to CAL

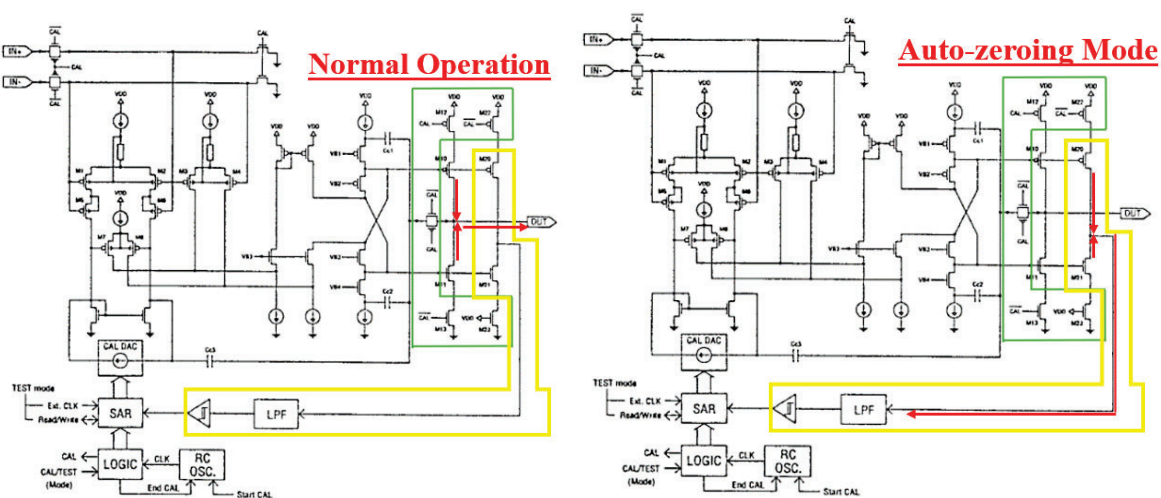
133. A POSITA would understand that the transistors M12, M13, M22, M23 are the second switch. The '665 Patent describes a switch in a general sense and

may involve multiple switches when appropriate. Ex. 1001 ['665 Patent] 10:40-42. The amplifier system output refers to the signal transmitted out of the amplifier. See Ex. 1001 ['665 Patent] Cl. 6. (“providing the first amplifier output”).

134. Transistors M22 and M23 act as an enable/disable switch for transistors M20, M21. Likewise, transistors M12 and M13 act as an enable/disable switch for transistors M10 and M11.

135. During the auto-zeroing phase, transistors M12 and M13 effectively disconnect the amplifier output OUT from the amplifier output stage with transistors M10 and M11 and transistors M22 and M23 connect the replica output stage with transistors M20/M21 to the LPF input, which is part of the comparator.

136. The pathway of the amplifier output during normal operation and the auto-zeroing mode is annotated below with a red arrow:



Ex. 1005, Fig. 1.

7. [1f] an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

139. The SAR below (in orange) is coupled to the systems DAC (in blue):



52

140. The use of *Munoz's* DAC improves the operation of *Krum*. A successive approximation DAC that has a radix of 2 does not permit alternative expressions of particular voltages or capacitance levels. Ex. 1008 [Munoz] 2:40-42.

141. Without alternative expressions of a particular voltage (i.e. redundancy), the system is unable to account for when a MSB is erroneously kept. Ex. 1008 [Munoz] 2:32-40. *Munoz's* DAC includes redundancy because the radix values are less than 2. Ex. 1008 [Munoz] 7:67-8:5. Accordingly, the *Krum-Munoz* combination is capable of accounting for erroneously kept bits.

142. A POSITA would also appreciate the benefits of including a radix of less than 2. A sub-binary radix is known to reduce gaps that may occur in the output of the successive approximation due to strict matching requirements in the DAC. Ex. 1013 [Pastre] 1 (“The analog part of the new DAC doesn’t need precise components.”).

143. The DAC of *Munoz* is an n-bit digital to analog converter. It is configured to convert an n-bit word. Ex. 1008 [Munoz] 8:36-41, Fig. 4.

8. [1g] the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

144. This limitation is obvious in light of the *Krum-Munoz* combination.

145. *Munoz*'s non-binary converter uses a radix of less than 2 for at least the most significant bits. For example, *Munoz*'s DAC that has a radix of less than two.

Ex. 1008 [Munoz] 6:45-48. The *Munoz* DAC is depicted below:

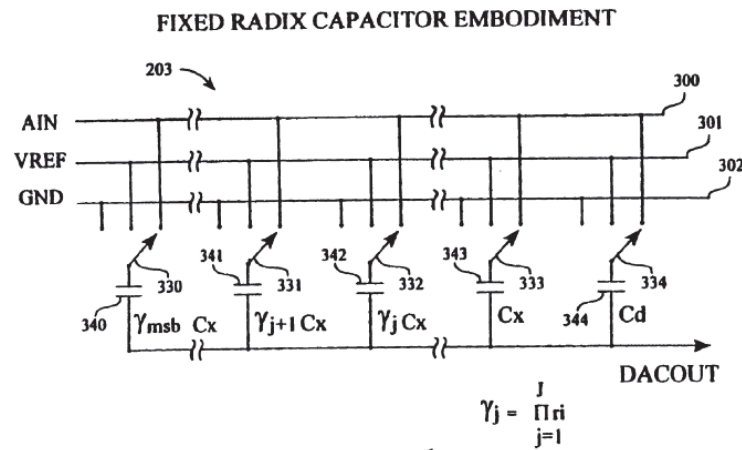


Fig. 3A

Ex. 1008 [Munoz] Fig. 3A.

146. The bank of components provides the bit values for the successive approximation, where each bank is used in the course of the SAR calibration process.

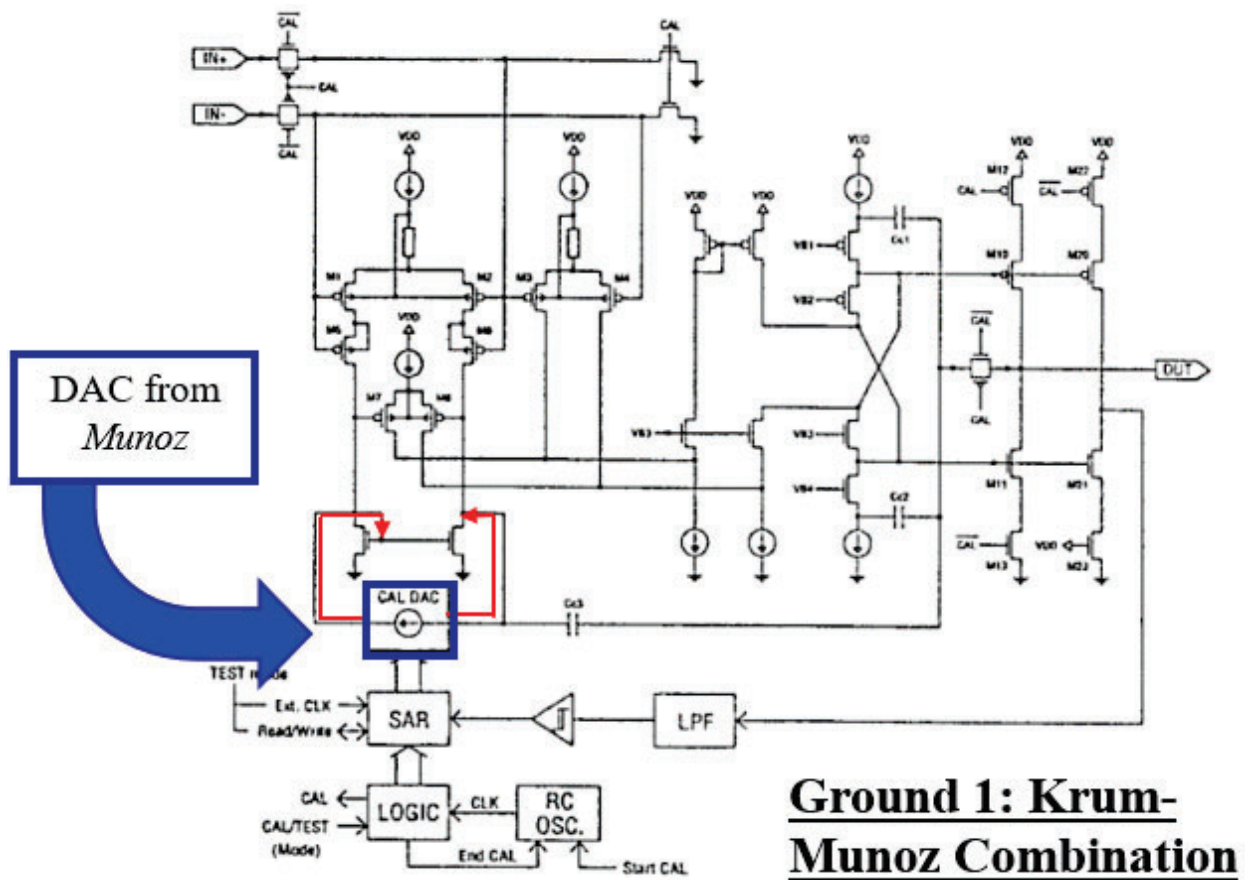
The values of respective capacitors γ_j , is given by the formula $\gamma_j = \prod_{i=1}^J r_i$ where r_i is the radix value. Ex. 1008 [Munoz] 7:3-10. The radix value is between one and two. Ex. 1008 [Munoz] 7:10-11. Accordingly, for the two most significant bits the radix value will be less than two.

147. Additionally, *Munoz* describes using resistors rather than capacitors. Ex. 1008 [Munoz] 6:67-7:3. Use of resistors would be beneficial in this application to provide a continuous time level.

9. [1h] an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

148. This limitation is obvious in light of the *Krum-Munoz* combination.

149. The output of the DAC in *Krum* is coupled to the first amplifier as depicted in with the red arrows:



Ex. 1005 [Krum] Fig. 1.

150. The DAC controls the input offset of the amplifier. Ex. 1005 [Krum] 1
 (“During calibration, the output offset voltage approaches zero”).

C. Claim 2

1. The amplifier system of claim 1 wherein the radix is approximately 1.9

151. This limitation is obvious in light of the *Krum-Munoz* combination.

152. *Munoz* describes use of radix values between one and two. Ex. 1008 [Munoz] 7:10-11. *Munoz* then teaches a specific radix value of 1.9, and notes that this radix value can be used. Ex. 1008 [Munoz] 17:43-48.

153. Instead of capacitors, resistors may be used. Ex. 1008 [Munoz] 9:18-19. A POSITA would know to use resistors in a SAR system that requires continuous time levels. The opamp of *Krum* uses a continuous time current. So, a system based on *Munoz's* teaches can be constructed with banks of resistors, where the radix value is approximately 1.9.

D. Claim 3

1. The amplifier system of claim 2 wherein the radix for the least significant bit is 2.

154. This limitation is obvious in light of the *Krum-Munoz* combination.

155. *Munoz* depicts a system where the radix of the LSB is 2:

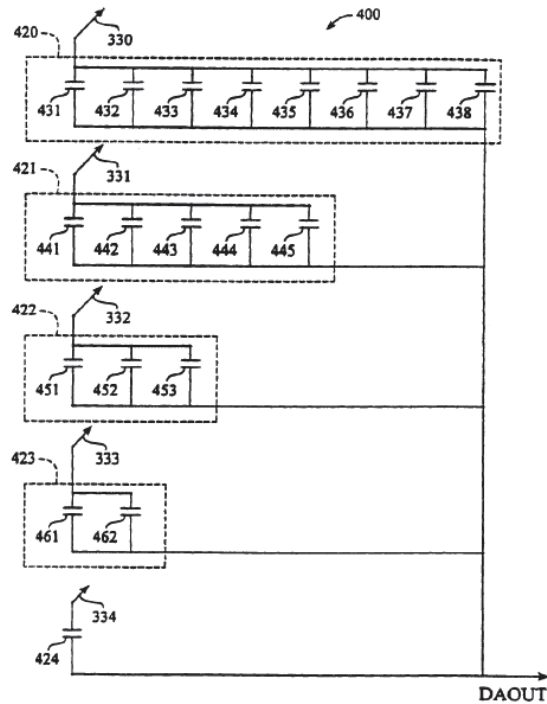


Fig. 3B

Ex. 1008 [Munoz] Fig. 3B.

156. The banks of capacitors in Fig. 3B may be implemented in a DAC. The DAC system includes a plurality of switches 330-334 between sets or banks 420-424 of capacitors 431-438, 441-445, 451-453, 461-462, 424. Ex. 1008 [Munoz] 7:30-34, 7:49-53. Each of the capacitors in these groupings of capacitors has a unit capacitance value. Ex. 1008 [Munoz] 7:53-57. A POSITA would understand that the DAC of *Munoz* may have a radix for the LSB that is different than the radix for the MSB. Ex. 1008 [Munoz] 7:35-40. The LSB radix values is determined by the ratio between capacitor bank 424 and capacitor bank 423 in Fig. 3B. Because each capacitor has a unit value, a POSITA would understand this figure to depict the

scenario where the system has a radix value of the LSB of 2, based on the ratio of the second bank (having two capacitors) to the first bank (having one capacitor).

E. Claim 4

1. The amplifier system of claim 1 wherein the D/A converter further comprises one additional bit providing an input offset control of the first amplifier of one half that of the least significant bit of the N bits.

157. This limitation is obvious in light of the *Krum-Munoz* combination.

158. For example, consider the *Krum-Munoz* combination wherein the additional bit corresponds to the last capacitor bank 424 in Fig. 3B, and the capacitor bank 423 corresponds to the LSB before the additional bit is added:

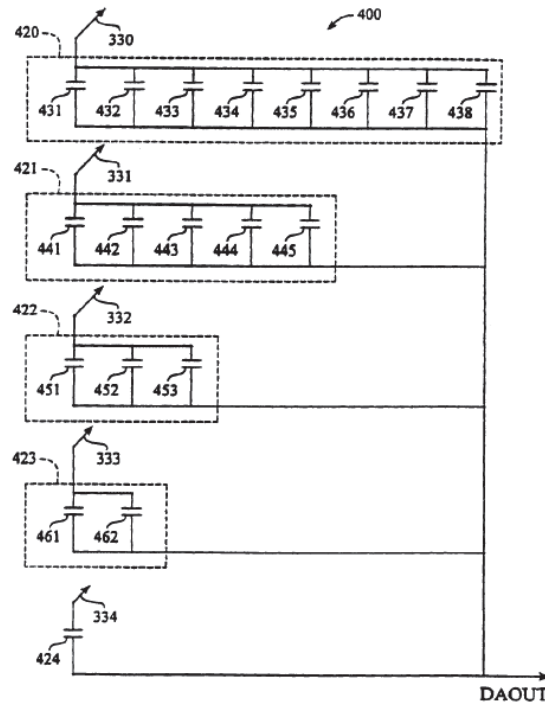


Fig. 3B

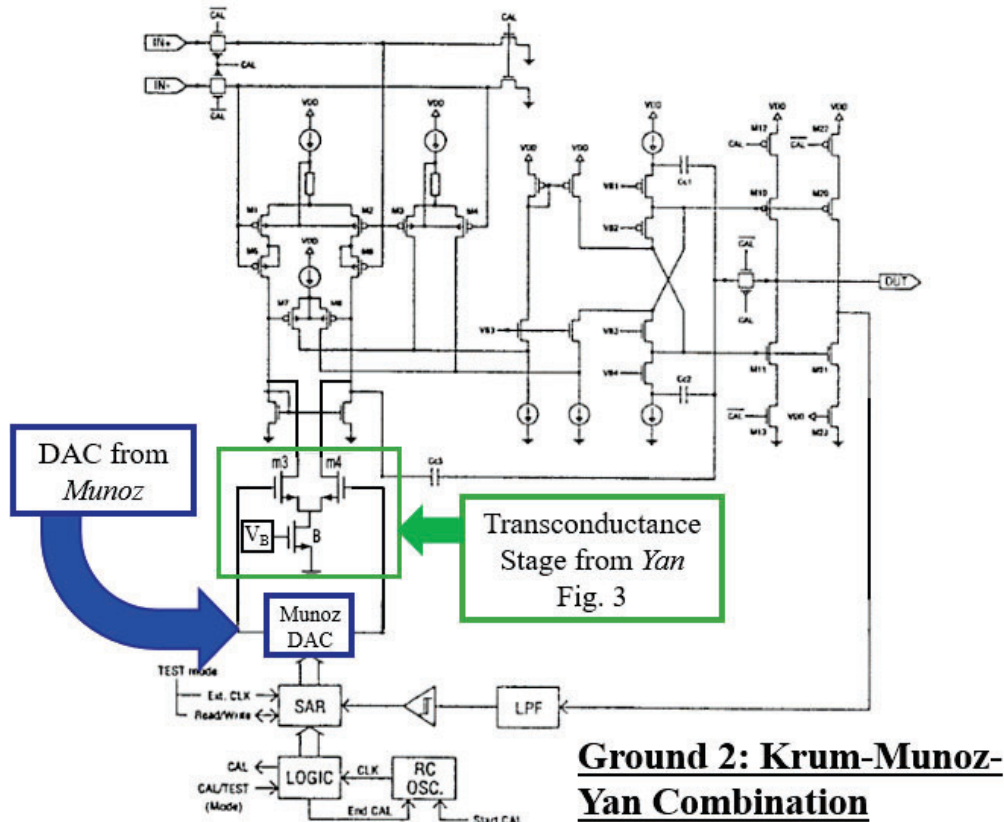
Ex. 1008 [Munoz] Fig. 3B.

159. As described in Section VII.D, the LSB radix value is determined by the ratio between capacitor bank 424 and capacitor bank 423 in Fig. 3B, and because each capacitor has a unit value, a POSITA would understand this figure to depict the scenario where the system has a radix value of the LSB of 2, based on the ratio of the second bank (having two capacitors) to the first bank (having one capacitor).

160. Here, the input offset control offered by the additional bit (corresponding to capacitor bank 424) is one half the input offset control offered by the LSB (corresponding to capacitor bank 423).

VIII. GROUND 2 – *KRUM* IN VIEW OF *MUNOZ* AND *YAN*

161. The Ground 2 combination, *Krum-Munoz-Yan* is configured similarly to the *Krum-Munoz* combination, but instead of implementing *Munoz*'s DAC as a current mode DAC, the CALDAC is implemented as a voltage mode DAC:



Ex. 1005 [Krum] Fig. 1; Ex. 1007 [Yan] Fig. 3.

A. Motivation to Combine

162. A POSITA would be motivated to implement *Munoz*'s DAC into *Krum*'s amplifiers for the same reasons outlined in Section VII.A. Further, it would be obvious to a POSITA to implement *Munoz*'s DAC as a voltage mode DAC instead of a current mode DAC.

163. Implementation of a voltage mode DAC into *Krum* would require an additional transconductance stage because *Krum*'s systems is designed to use a current mode DAC. Ex. 1005 [Krum] 1. An additional transconductance stage would be connected to the voltage mode DAC and output a current. A transconductance stage is described *Yan* Fig. 3.

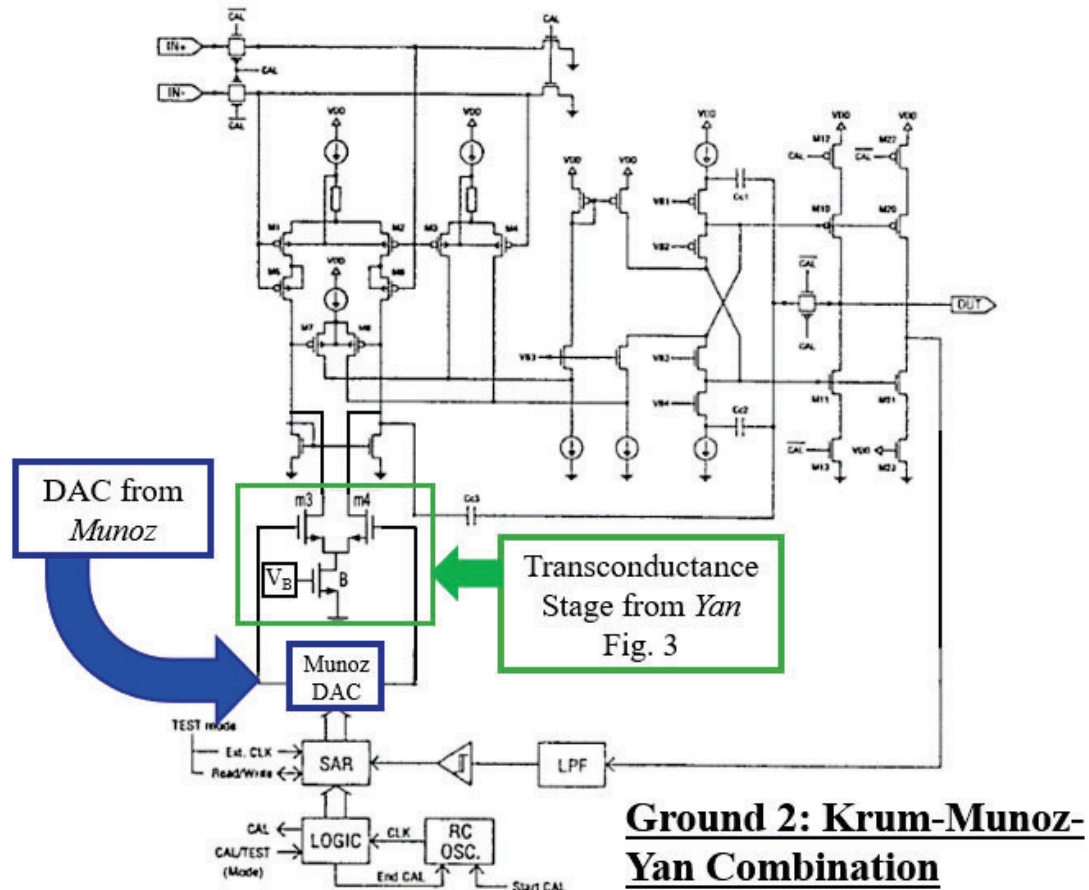
164. *Yan* falls in the same field of endeavor of the '665 Patent because *Yan* also describes an operational amplifier with offset compensation circuitry. Ex. 1007 [Yan] 1:5-10.

165. *Yan* acknowledges that the circuitry of Fig. 3 is known in the prior art. Ex. 1007 [Yan] Fig. 3 ("Prior Art"). Use of such circuitry would be well within the skills of a POSITA and would yield predictable results.

166. A POSITA interested in implementing *Munoz*'s DAC as a voltage mode DAC would know to use an additional transconductance stage to turn the voltage difference into a current. Use of the additional transconductance stage depicted in *Yan*'s Fig. 3 with *Krum*'s amplifier and *Munoz*'s DAC is nothing more than the predictable use of elements known in the prior art performing the same functions they were known to perform.

167. A POSITA would be capable of implementing *Yan* with a reasonable expectation of success. First, the capacitor Cc3 remains connected to the opamp of *Krum*. The drains of m3 and m4 in *Yan* are connected to drains of M5/M6 in *Krum*.

Yan is also implemented without the capacitors C1 and C2 as the memory element used in the offset compensation of *Yan* are replaced with the DAC which drive the gates of m3 and m4, and a digital memory. The transistor B's gate would also be connected to a biasing voltage:



Ex. 1005 [Krum] Fig. 1; Ex. 1007 [Yan] Fig. 3.

B. Independent Claim 1

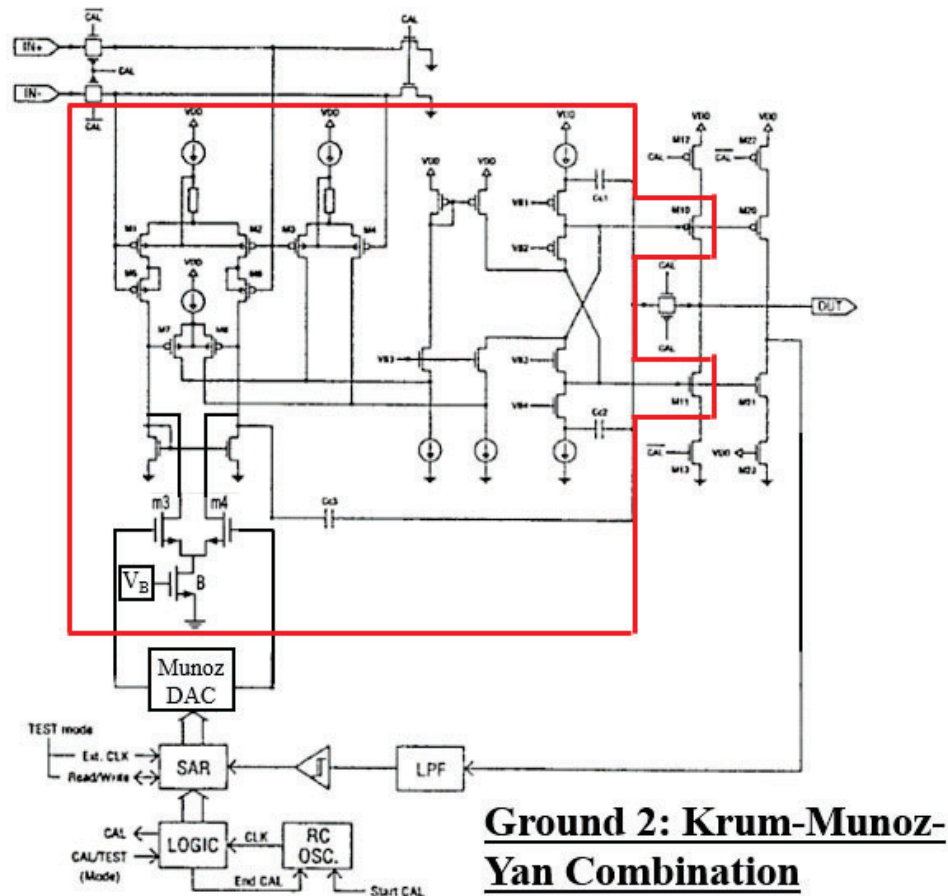
- 1. [1pre] An amplifier system having an amplifier system input and an amplifier system output comprising:**

168. I have no opinion as to whether the preamble of Claim 1 is limiting. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.1.

- 2. [1a] a first amplifier;**

169. This limitation is obvious for the same reasons described for ground 1 in Section VII.B.2.

170. With the addition of *Yan*'s transconductance stage, the first amplifier is mapped as shown below in red:



3. [1b] a comparator;

171. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.3. *See also*, Ex. 1005 [Krum] 1, Fig. 1.

4. [1c] a successive approximation register having an input coupled to an output of the comparator;

172. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.4. *See also*, Ex. 1005 [Krum] 1, Fig. 1.

5. [1d] a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

173. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.5. *See also*, Ex. 1005 [Krum] 1, Fig. 1.

6. [1e] a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator,

174. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.6. *See also*, Ex. 1005 [Krum] 1, Fig. 1.

7. [1f] an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

175. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.7. *See also*, Ex. 1005 [Krum] 1; Ex. 1008 [Munoz] 2:30-42, 7:67-8:5, 8:36-41, Fig. 4; Ex. 1013 [Pastre] 1.

8. [1g] the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

176. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.8. *See also*, Ex. 1008 [Munoz] 6:45-48, 6:67-7:11, Fig. 3A.

9. [1h] an output of the D/A converter being coupled to the first amplifier to control the input offset of the first amplifier.

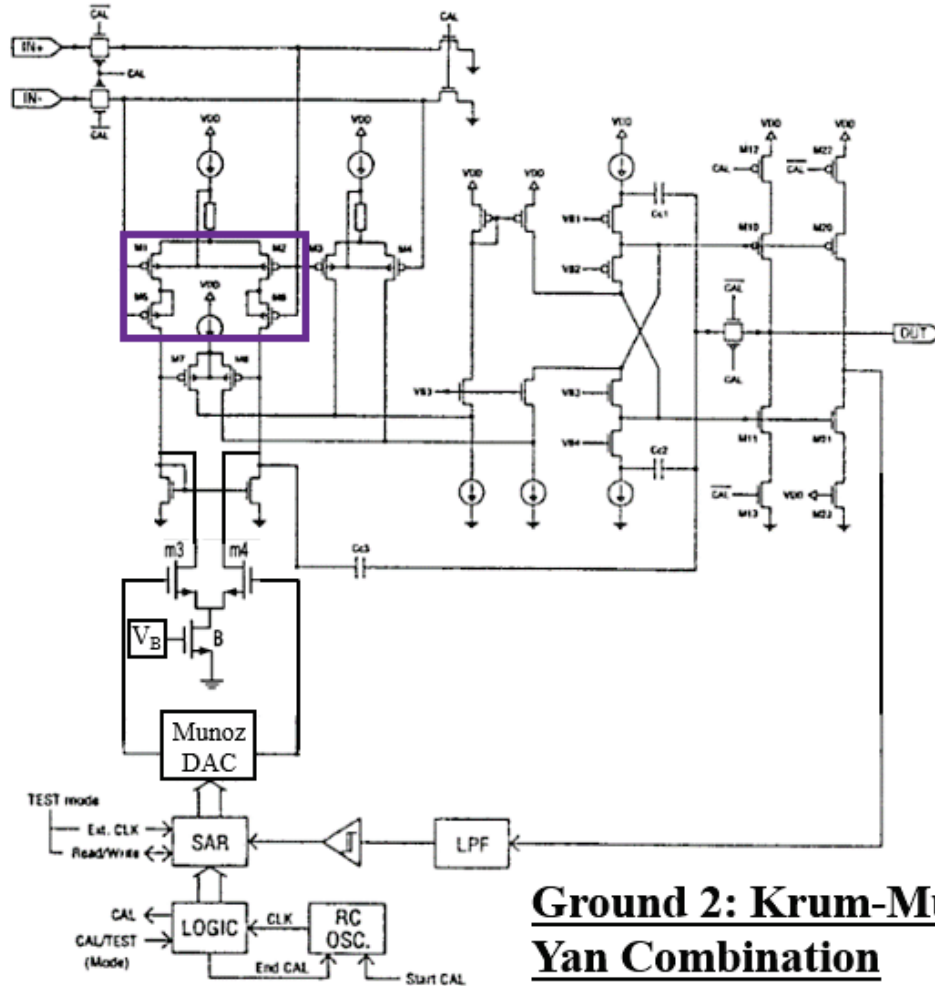
177. This limitation is obvious for the same reasons described for the *Krum-Munoz* combination in Section VII.B.9. *See also*, Ex. 1005 [Krum] Fig. 1

C. Claim 5

1. [5a] The amplifier system of claim 1 wherein the first amplifier has a first transconductance differential input stage coupled to the first amplifier input,

178. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

179. *Krum* describes the input pair M1 and M2 as cascaded by transistors M5 and M6. Ex. 1005 [Krum] 1. This forms a transconductance differential stage (in purple):



Ground 2: Krum-Munoz-Yan Combination

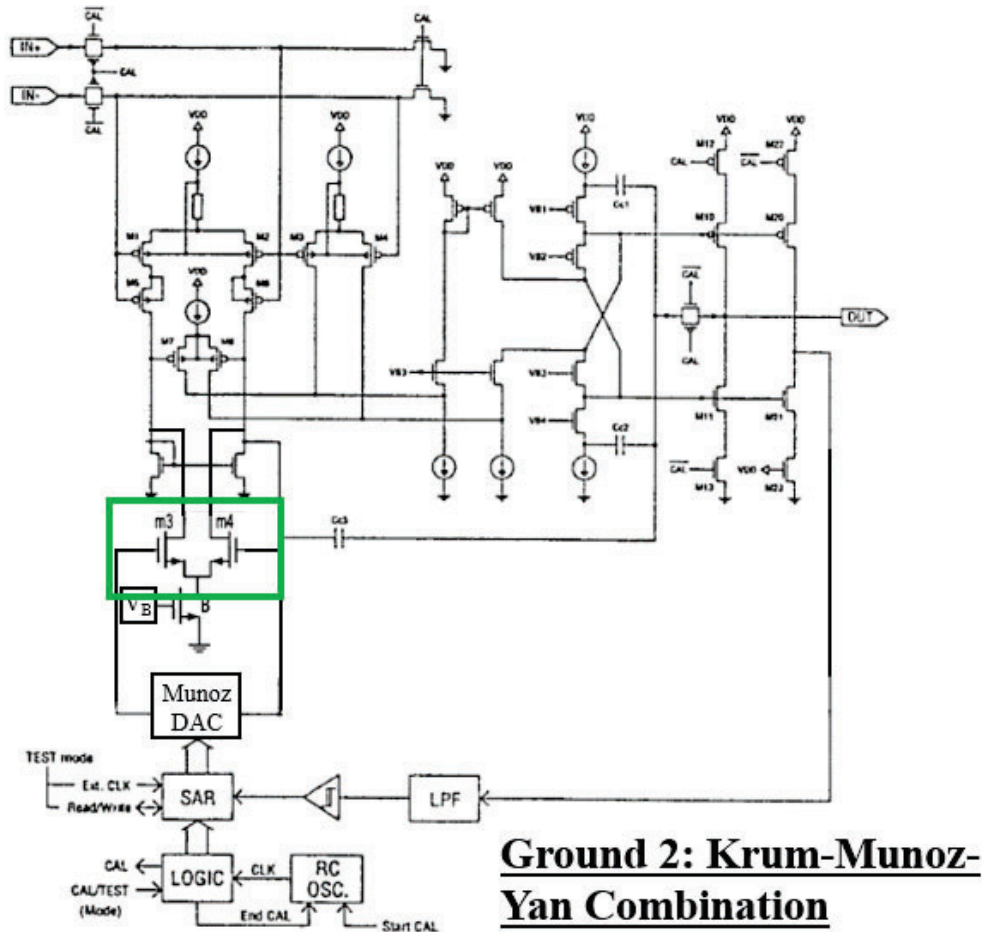
Ex. 1005 [Krum] 1.

180. M1 and M2 are configured as a transconductance differential input stage. Consistent with element [1d], the gates of M1 and M2 are the first amplifier input.

2. [5b] and wherein the first amplifier is further comprised a second transconductance differential input stage,

181. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

182. *Krum* teaches the first amplifier further comprising a second transconductance differential input stage (in **green**):



Ex. 1005 [Krum] Fig. 1.

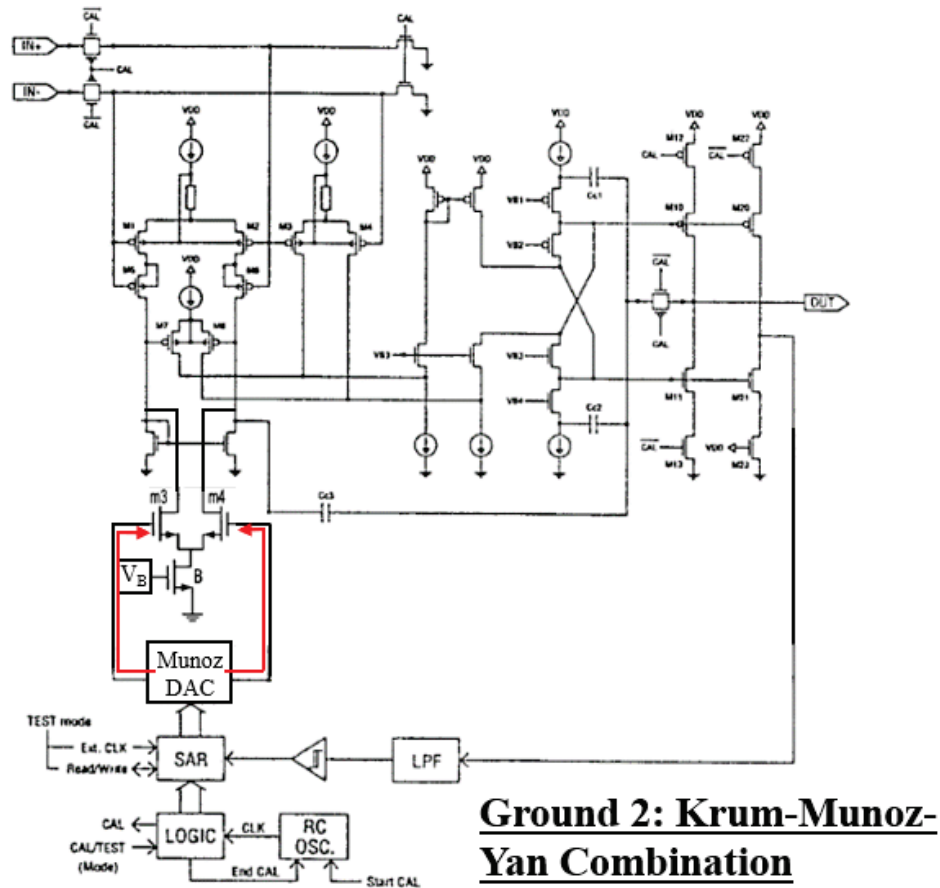
183. These transistors are coupled to a common current source and act as a transconductance differential stage for the offset calibration of the amplifier.

186. The PMOS transitions M5 and M6 drains are output of the first transconductance differential input stage. The drains of *Yan*'s transistors m3 and m4 are the output of the second differential input stage. The drains are connected in parallel.

4. [5d] the output of the D/A converter being coupled to inputs of the second transconductance differential input stage

187. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

188. The output of the DAC in *Krum* are coupled to the inputs (i.e., the two inputs of the *Yan*'s transistors m3 and m4) of the second transconductance differential input stage shown by the red arrows below:

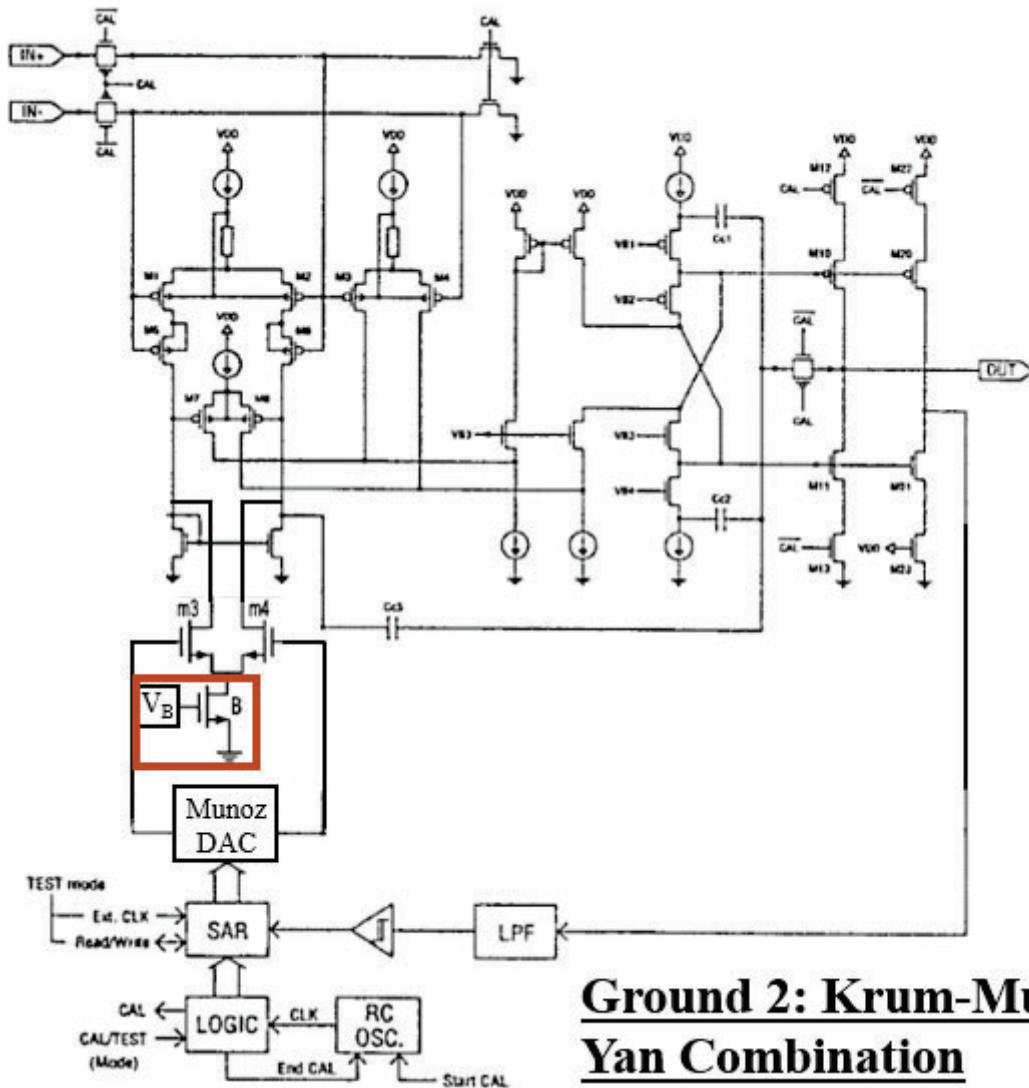


Ex. 1005 [Krum] Fig. 1.

5. [5e] to divide a current source coupled to the second transconductance differential input stage between the differential outputs of the first transconductance differential input stage in a proportion to reduce the input offset of the first amplifier.

189. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

190. The *Krum-Munoz-Yan* depicts a biasing transistor B connected to a biasing voltage (V_B) (in brown):



Ex. 1005, Fig. 1.

191. Transistor m3 drain couples to the drain of M5 and the transistor m4 drain couples to the drain of M6. Together, the drains of M5 and M6 form the differential outputs of the first transconductance differential input stage, which both receive a portion of the current from the second transconductance amplifier current source.

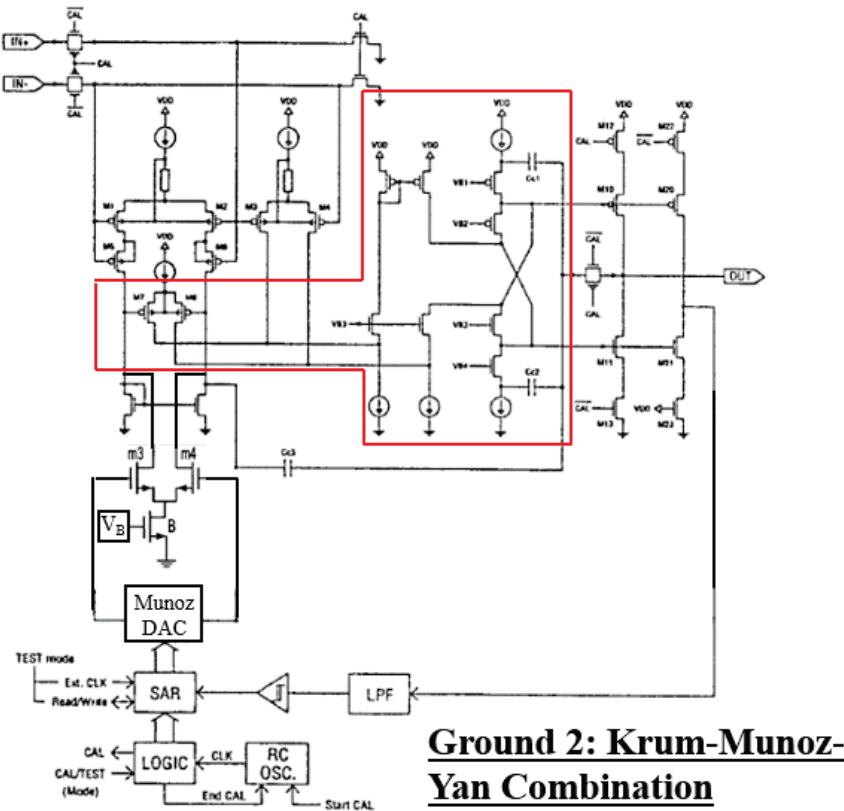
192. In ideal conditions (no offset and no CALDAC calibration signal), the divided currents are equal. In the presence of an offset, the two currents become unequal. The DAC output will adjust the division of the sourced current by the transistor B between the two branches, as explained by *Krum*, in order to reduce the offset of the opamp.

D. Claim 6

1. [6a] The amplifier system of claim 5 wherein the first amplifier further comprises an intermediate stage having an input coupled to the parallel connected outputs of the first and second transconductance differential input stages,

193. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

194. For example, the amplifier includes an intermediate stage (in red):



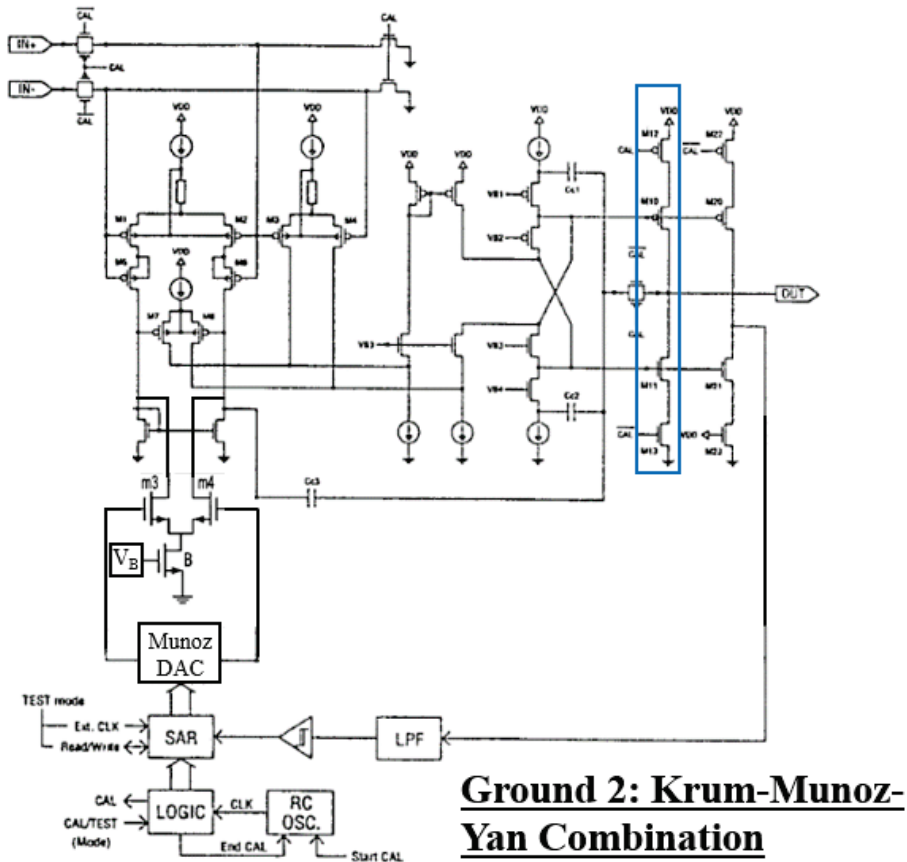
Ex. 1005, Fig. 1.

195. The inputs of the intermediate stage are the input gates of transistors M7 and M8. They are coupled to the parallel connection between M5 and m3, and M6 and m4 described in Section VIII.C.3. These are the parallel connection outputs of the first transconductance stage and second transconductance stage.

2. [6b] a first output stage providing the first amplifier output,

196. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

197. The first output stage includes transistors M10 and M11 controlled by M12 and M13 (in blue):



Ex. 1005 [Krum] Fig. 1. Transistors M10 and M11 provide the first amplifier output.

3. [6c] a second output stage forming the comparator,

198. This limitation is obvious in light of the *Krum-Munoz-Yan* combination. The second output stage forming a comparator is depicted below in yellow:

switches between the first output stage (the inputs of M10 and M11) and the second output stage (the comparator circuit through M20 and M21).

201. As stated in *Krum*, “[d]uring autocalibration.... output transistors M10 and M11 are disconnected from their respective supplies” and the “small replica transistors M20 & M21 (scaled to M10 & M11) are used to provide the amplifier output signal for the calibration circuit.” Ex. 1005 [Krum] 1.

E. Claim 7

1. [7a] The amplifier system of claim 6 wherein the second switch also sets the first output stage to a high impedance state when the second switch couples the input of the second output stage to the output of the intermediate stage,

202. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

203. As described in Section VII.B.6, *Krum* provides a second switch which includes transistors M12, M13, M22, and M23.

204. In auto-zeroing mode both transistors M20 and M21 are powered on (by transistors M22 and M23) and provide replica signals to the comparator from the intermediate stage (i.e, the second switch couples the input of the second output stage to the output of the intermediate stage).

205. The transistors M12 and M13 in the second switch set the first output stage (M10 and M11) to a high impedance state.

2. [7b] and sets the second output stage to a high impedance state when the second switch couples the input of the first output stage to the output of the intermediate stage.

206. This limitation is obvious in light of the *Krum-Munoz-Yan* combination.

207. In normal operation both transistors M10 and M11 are powered on (by transistors M12 and M13) and provide signals to the system output from the intermediate stage (i.e, the second switch couples the input of the first output stage to the output of the intermediate stage).

208. The transistors M22 and M23 in the second switch set the first output stage (M20 and M21) to a high impedance state.

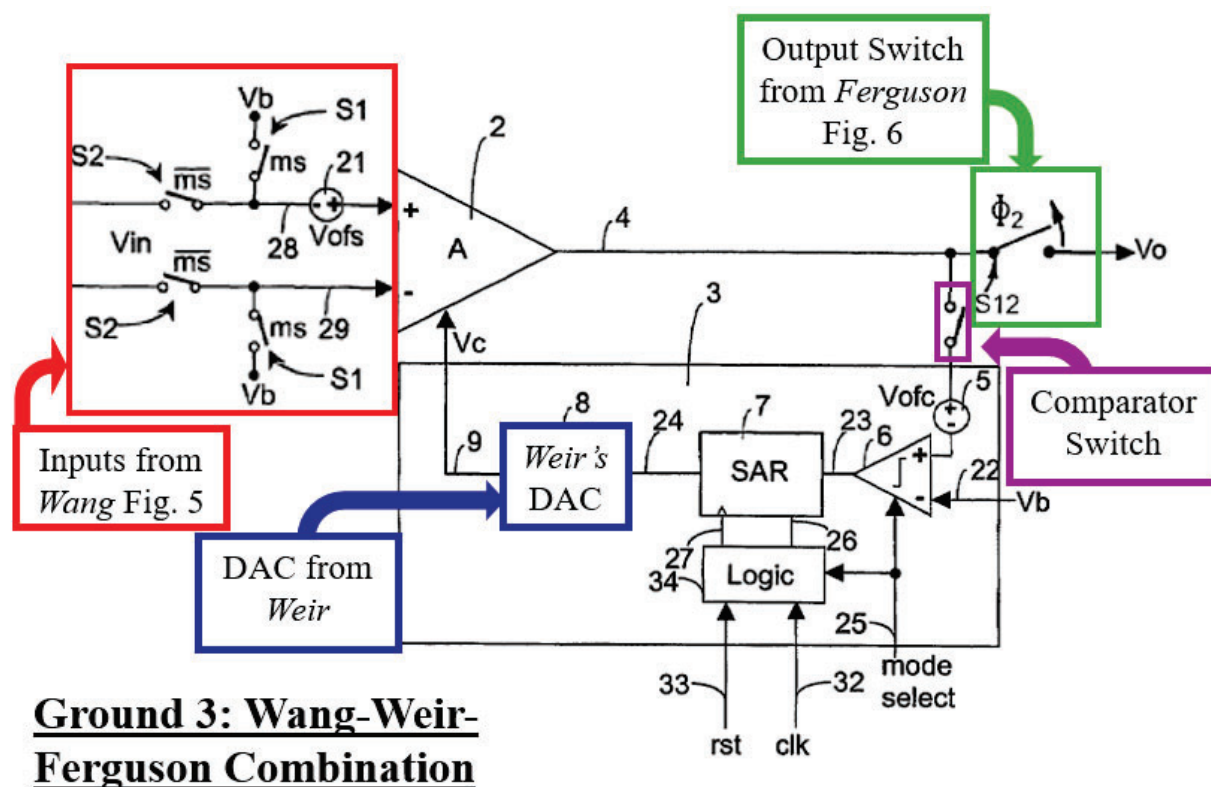
IX. GROUND 3 – WANG IN VIEW OF WEIR AND FERGUSON

209. Wang concerns “apparatus and integrated circuits for continuous-time applications where the offset of at least one operational amplifier is compensated by a dedicated circuitry.” Ex. 1009 [Wang] 1:5-7. This system includes a comparator, SAR and DAC, however, a POSITA reading *Wang* would note that *Wang* does not provide details regarding the structure of the DAC of *Wang*. Instead, Wang’s scheme is described as working for all kinds of DACs. Ex. 1009, 8:36-37. This

open-endedness of *Wang* would lead a POSITA to look to other references to ascertain what type of DAC to use in *Wang*.

210. A POSITA would be motivated to improve *Wang*'s system by both *Weir* and *Ferguson*. *Weir* teaches a SAR DAC that does not require precise components to construct the DAC's radix less than two. *Ferguson* describes a system that can reduce voltage glitches which occur when offset cancelation occurs, through the addition of certain output switching features. Ex. 1010 [Ferguson] 11:64-67.

211. A combination of the teachings of *Wang*, *Weir*, and *Ferguson* would suggest something akin to the circuit structure depicted below:



212. *Wang's* auto-zeroed opamp system is depicted, with a few additions. This system includes (1) the inputs of the opamp system described in *Wang* Fig. 5 (in red); (2) the anti-glitch system described in *Ferguson* (in green); (3) a physical comparator switch based on *Wang's* disclosure of the comparator (in purple); and (4) the DAC for *Weir* (in blue).

A. Motivation to Combine

213. A POSITA would be motivated to improve the system described in *Wang* to include a DAC with radix less than two elements from *Weir*, and include additional switches taught by *Ferguson* (as confirmed by *Wang* itself).

214. *Wang*, *Weir*, and *Ferguson* are all analogous art to the '665 Patent. *Weir* addresses the pertinent problem of the '665 Patent: improvements to successive approximation digital-to-analog converters, which are often used in opamps to improve the offset voltages. Ex. 1001 ['665 Patent] 1:20-57, 2:41-55; 7:30-35; Ex. 1014 [Weir] 1:10-15, 1:23-26. *Wang* and *Ferguson*, like the '665 Patent, fall in the same field of endeavor of operational amplifiers with offset compensation circuitry. Ex. 1001 ['665 Patent] Title, 1:5-8; Ex. 1009 [Wang] Abstract, 1:4-7; Ex. 1010 [Ferguson] Title, Abstract, 1:5-7.

215. *Wang* provides a system to compensate for offset voltages of an operation amplifier. Ex. 1009 [Wang] Title, Abstract. *Wang* recognizes the need of this system to compensate for a high range of offsets while still preserving a high

level of precision. Ex. 1009 [Wang] 1:63-67. *Wang* also attempts to provide this circuit with reduced circuit overhead. Ex. 1009 [Wang] 2:1-4. So, *Wang* uses a successive approximation procedure in attempts to achieve both of these objectives. Ex. 1009 [Wang] 3:9-11.

216. A POSITA would be motivated to improve *Wang*'s system to provide greater precision without adding significant overhead. One way to achieve improve precision is taught by *Weir*. *Weir* notes that successive approximation systems may suffer reduced precision if a DAC element has an error greater than the magnitude of the smallest element in the series. Ex. 1014 [Weir] 2:11-17.

217. By implementing a radix with values less than 2, "a substantially larger error can be tolerated at each comparison, while yet obtaining an overall conversion error that is less than the value of the smallest element of the series." Ex. 1014 [Weir] 4:9-14.

218. Based on *Weir*'s teachings, successive approximations are improved by implementing DAC's with resistive elements that have magnitudes corresponding to a nonbinary series. Ex. 1014 [Weir] 4:43-45. This would improve system compensation precision by reducing the strict accuracy requirements of DAC elements. Ex. 1014 [Weir] 3:8-12. Additionally, "[b]y providing a non-binary sequence in which the sum of the preceding series elements exceeds the value for

the next element, the comparator accuracy requirements are substantially reduced.”

Ex. 1014 [Weir] 3:8-12.

219. *Weir* also provides additional details regarding a DAC which would assist a person of skill to implement the auto-zeroing circuitry described in *Wang*.

220. *Wang*’s system would also be improved by implementing additional switches, such as those of *Ferguson*. Use of switches would be consistent with *Wang* itself, which already describes a comparator that can be “turned off” during normal operation (since it is only used during auto zeroing). Ex. 1009 [Wang] 5:34-40 (“In order to [save] power, the comparator 6, or 76, or 96, or 106 may be designed so that it turns off when the mode select signal ms is logic low.”). *Wang* also includes systems which include switches between the comparator to toggle between self-zeroing modes of different systems. Ex. 1009 [Wang] 6:66-7:1. *Wang* also describes the importance of isolating the auto zeroing circuitry from different stages of the integrated circuit using switches. Ex. 1009 [Wang] 4:43-5:33.

221. For clarity, I include a switch expressly in the combination. A POSITA would have found it obvious to use a separate switch.

222. Further, a POSITA would be motivated to implement an output switch as described in *Ferguson*. *Ferguson* describes implementing a circuit to avoid unwanted glitches during offset calibration. Ex. 1010 [Ferguson] 11:64-67. This system uses a catching amplifier and multiple separate switches. Ex. 1010

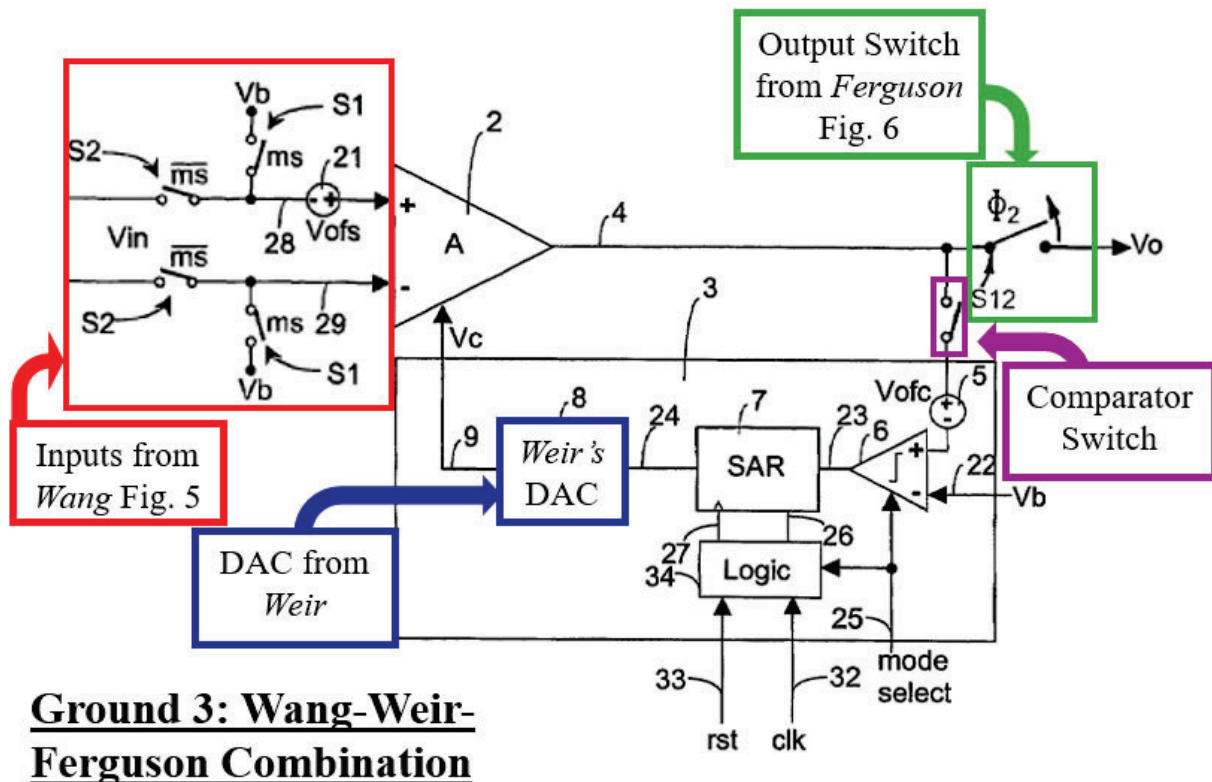
Ex. 1009 [Wang] Fig. 3, Fig. 5; Ex. 1010 [Ferguson] Fig. 6.

83



When S12 is open and S11 is closed, the catching amplifier 80 will be configured to have a gain of approximately zero between the input node and output node, which has the effective of muting the output. Ex. 1010 [Ferguson] 12:57-64.

224. I have also created a more simplified representation, which a POSITA would understand to include this other circuitry from *Ferguson*, but as such circuitry does not map to anything in the claimed system, I have omitted it from the following simpler figure:



Ex. 1009 [Wang] Fig. 3, Fig. 5; Ex. 1010 [Ferguson] Fig. 6.

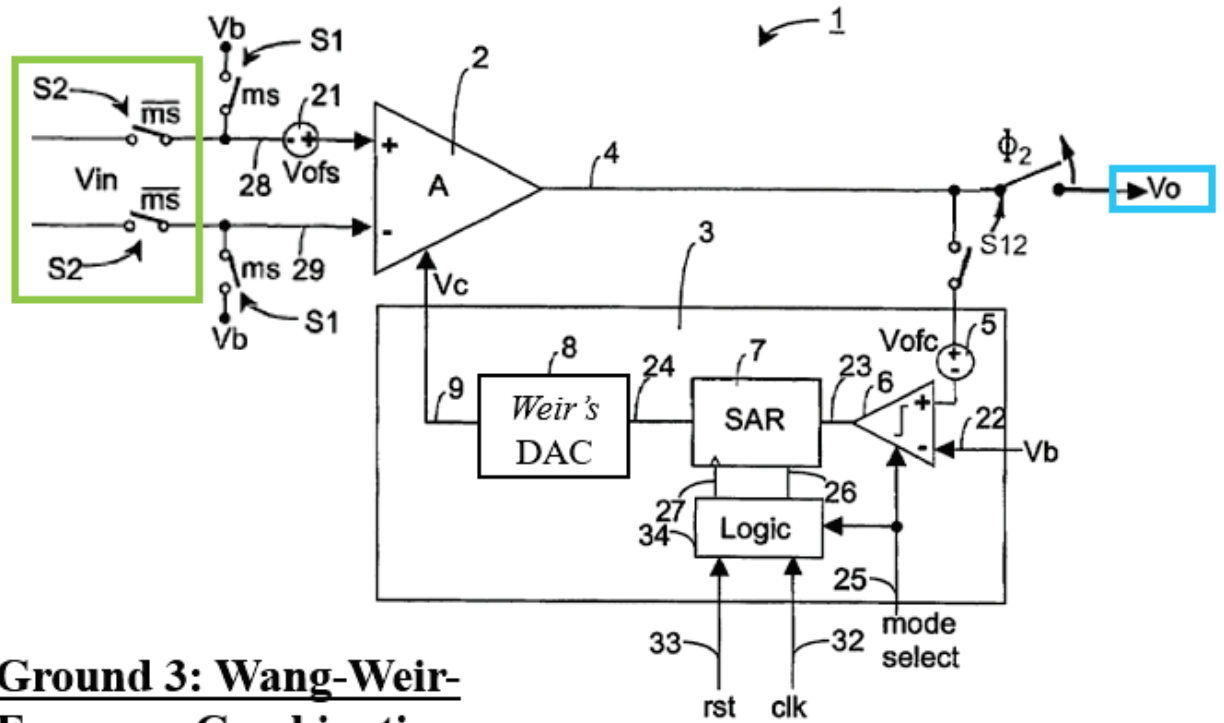
225. In this combination, the components continue to work in predictable ways to perform their tasks. *Wang's* system need to have a high precision of the

offset compensation. The substitution of DACs is simply an exchange of known elements to obtain predictable results. Likewise, switches are known circuit elements, implementable into circuitry like *Wang* with routine engineering. *Wang* itself teaches use of standard circuit elements which makes any modification simpler. Ex. 1009, 3:12-13. Accordingly, construction of the *Wang-Weir-Ferguson* combination could be achieved with a reasonable expectation of success.

B. Independent Claim 1

1. [1pre] An amplifier system having an amplifier system input and an amplifier system output comprising:

226. I have no opinion as to whether the preamble of claim 1 is limiting. However, the preamble of Claim 1 is obvious in light of the *Wang-Weir-Ferguson* combination. As shown below, the combination includes (in green) a input (V_{in}) and (in blue) an output (V_0):

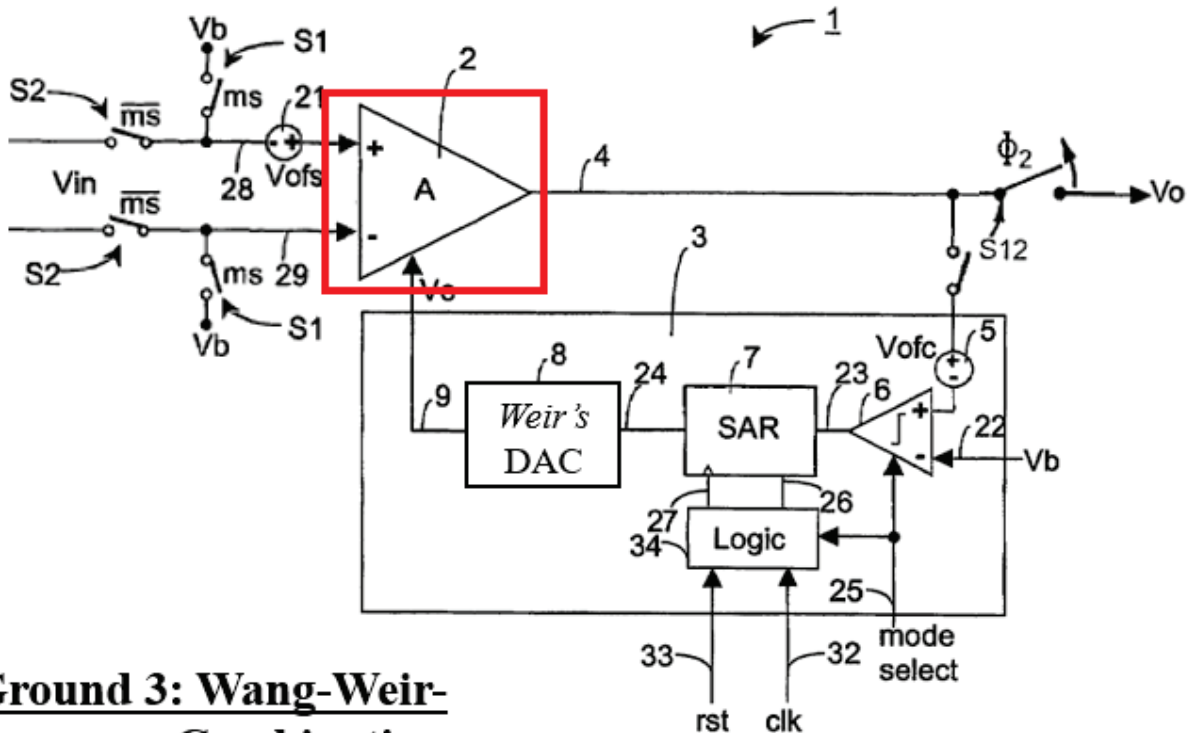


Ground 3: Wang-Weir-Ferguson Combination

Ex. 1009 [Wang] Fig. 3, Fig. 5.

2. [1a] a first amplifier;

227. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination. *Wang* discloses an amplifier (in red) connected to with a DAC:



Ground 3: Wang-Weir-Ferguson Combination

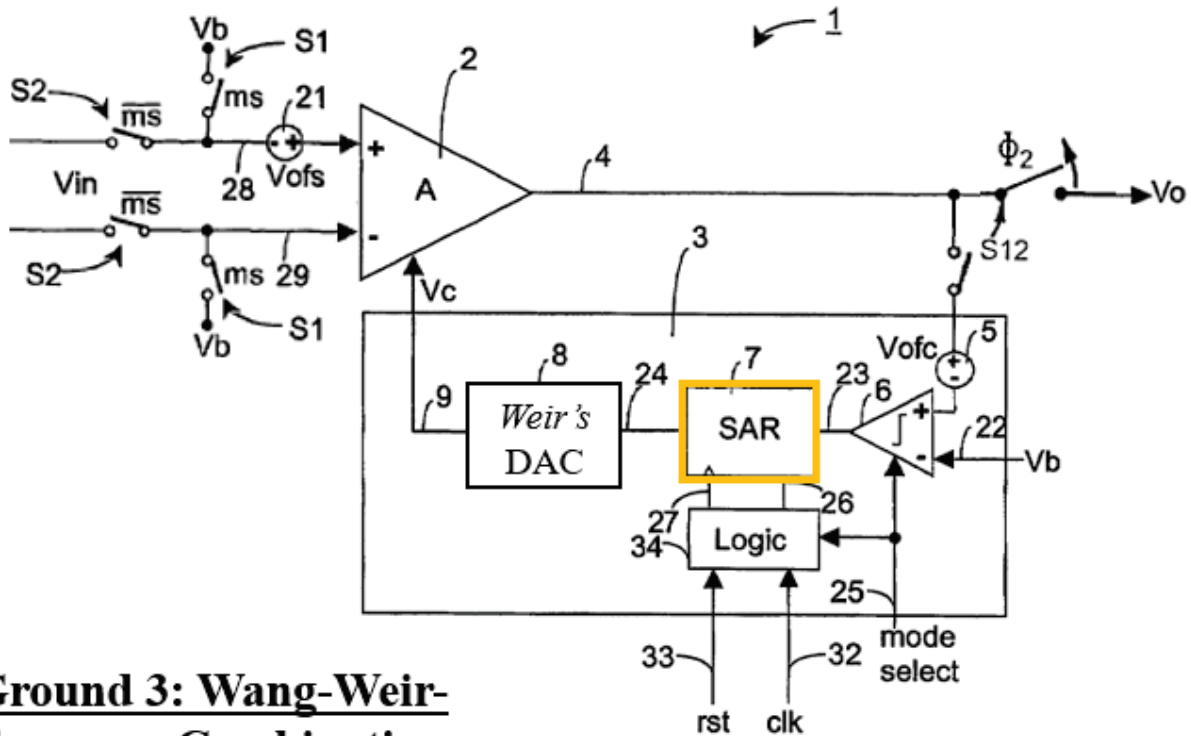
Ex. 1009 [Wang] Fig. 3; 3:30-35.

228. In the *Wang-Weir-Ferguson* combination, the *Weir's* DAC is connected to the amplifier.

3. [1b] a comparator;

229. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

230. *Wang* includes a comparator as shown (in yellow) below:



Ground 3: Wang-Weir-Ferguson Combination

Ex. 1009 [Wang] Fig. 3. The inputs of the SAR are coupled to the output of the comparator.

5. [1d] a first switch for switching an input of the first amplifier from the amplifier system input to shorting the first amplifier input;

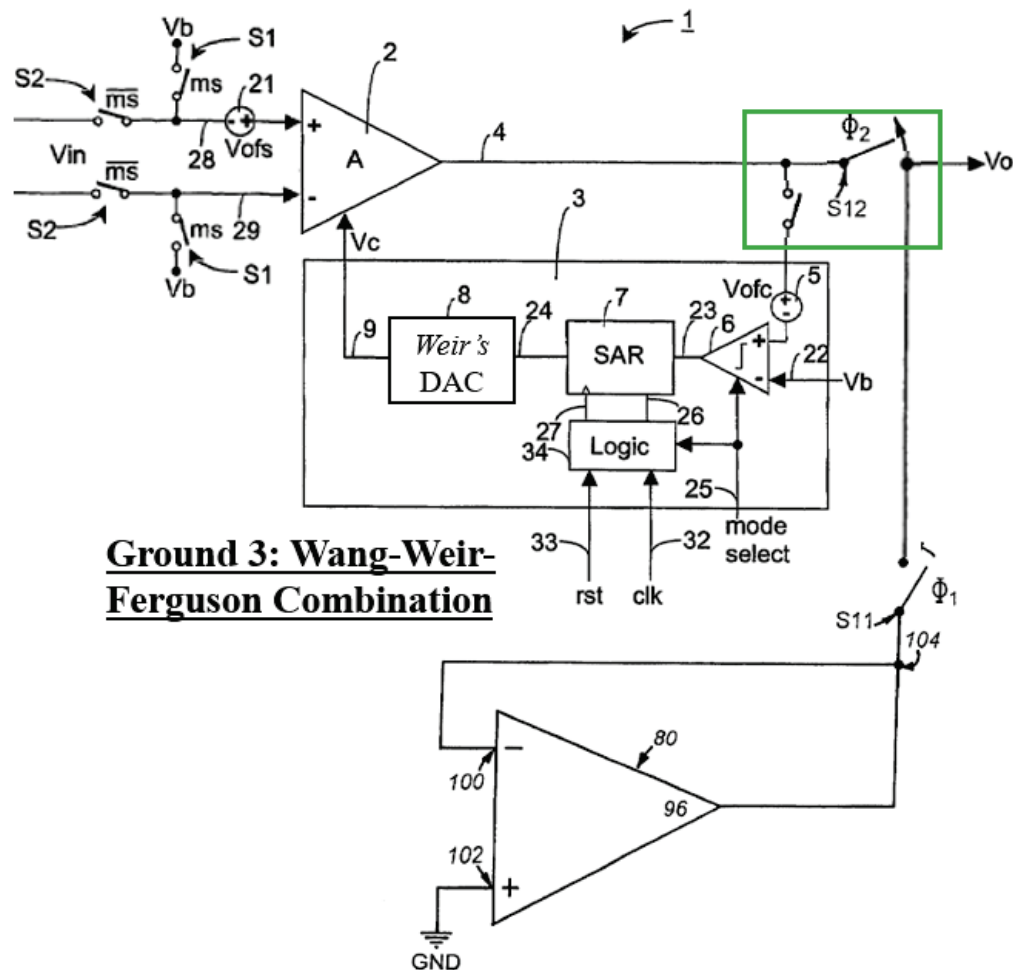
233. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

234. For example, the input switches in *Wang* S1 (in pink) can short the inputs of the first amplifier:

6. [1e] a second switch for switching an output of the first amplifier from the amplifier system output to an input of the comparator,

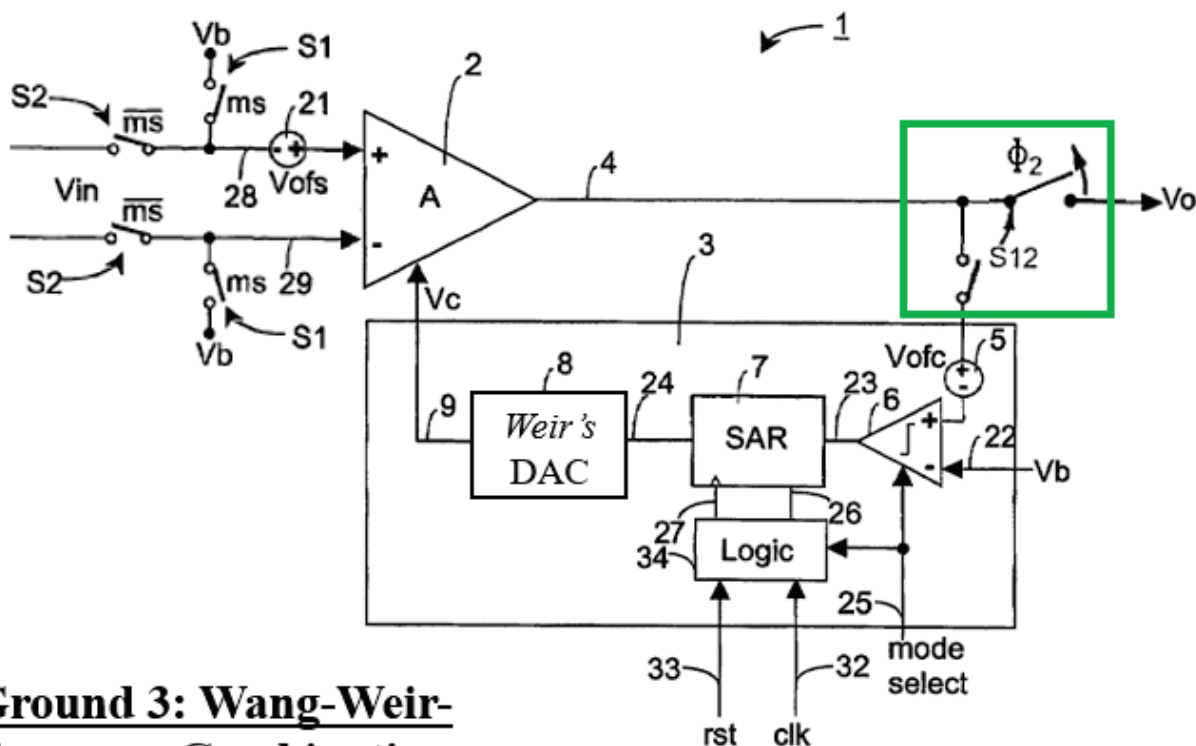
236. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

237. For example, the *Wang-Weir-Ferguson* combination includes two switches (in green) that switch the outputs from the amplifier system output to an input of the comparator:



Ex. 1009 [Wang] Fig. 3, Fig. 5; Ex. 1010 [Ferguson] Fig. 6.

238. For simplicity (*See supra* Section VIII.A.), the two switches are also shown in the figure below:



Ground 3: Wang-Weir-Ferguson Combination

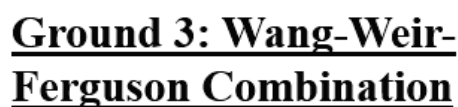
Ex. 1009 [Wang] Fig. 3, Fig. 5; Ex. 1010 [Ferguson] Fig. 6.

239. The switch connected to the comparator input is consistent with the comparator's on/off functionality. Ex. 1009 [Wang] 5:37-41 ("In order to save power, the comparator 6, or 76, or 96, or 106 may be designed so that it turns off when the mode select signal ms is logic low.").

240. These switches function to switch an output of the first amplifier from the amplifier system output to the input of the comparator. For example, during

7. [1f] an output of the successive approximation register being coupled to an N bit digital to analog (D/A) converter;

242. For example, below the SAR is coupled to the system DAC (in blue):



Ex. 1009 [Wang] Fig. 3.

243. *Wang* is constructed to so that the “SAR 7 here works in a very similar manner to a conventional and well known SAR ADC.” Ex. 1009 [Wang] 2:59-61. Further, the SAR is constructed to work with a “k-bit digital-to-analog converter (DAC).” Ex. 1009 [Wang] 3:27-29.

244. *Weir* also discloses a n-bit DAC. For example, *Weir* describes a DAC with various numbers of bits (e.g., n-bits). Ex. 1014 [Weir] 1:31-33.

8. [1g] the D/A converter being a non-binary converter using a radix of less than 2 for at least the most significant bits;

245. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

246. For example, *Weir's* includes resistive elements selected to “produce signals having magnitudes corresponding to the nonbinary series of $[ka^0, ka^1, ka^2, ka^3, ka^4, \dots ka^n]$ where $1 < a < 2$.” Ex. 1014 [Weir] 3:30-31. The ratio between successive resistive elements (i.e., variable “a”) is a radix.

247. *Weir* also provides an example system where the radix is 1.8 for each bit. Ex. 1014 [Weir] 3:31-36.

248. *Weir's* DAC is depicted below (in red) with resistive elements (in green):

C. Claim 2

1. The amplifier system of claim 1 wherein the radix is approximately 1.9

251. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

252. For example, in *Weir*, “the DAC resistance elements 15 need not have the precise values required to produce analog voltages or currents in the exact ratios of the series given by equation 1. What is required, however, is that the step values produced by the resistors 15 be known.” Ex. 1014 [Weir] 5:1-7. Further, “each such resistance element 15 may vary by as much as say 5% from the corresponding series exact value[.]” Ex. 1014 [Weir] 8:58-60. In fact, Table 1 of *Weir* describes the equation as providing “nominal” values for elements, but not the exact values. Ex. 1014 [Weir] 5:12-28.

253. *Weir* provides an example DAC with a radix of 1.8. Ex. 1014 [Weir] 3:25-35. A POSITA will recognize that a radix of 1.8 between two elements, each with an error of 5%, has an actual value in the radix range of 1.63 (1.71/1.05) to 1.99 (1.89/0.95) 1.99, so it will include the radix value of 1.9 indicated in the '665 Patent.

D. Claim 3

1. The amplifier system of claim 2 wherein the radix for the least significant bit is 2.

254. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

255. A LSB having a radix of 2 is suggested by *Weir*. For example, consider a situation where the LSB is designed to have a value of 1.0 and next least significant are designed to have a value of 1.8. *Weir* teaches “each such resistance element 15 may vary by as much as say 5% from the corresponding series exact value[.]” Ex. 1014 [Weir] 8:58-60. Therefore, a POSITA reading *Weir* would understand it to teach the scenario in which the LSB is 0.95 (5% less), and the next successive bit is 1.89 (5% more). In such a scenario, the radix would be 1.99 (1.89/.95).

256. In light of the art, a radix of 1.99 would suggest a radix of 2 to a POSITA. A radix of 2 would be well known by a POSITA. Ex. 1013 [Pastre] 1 (“In conventional digital-to-analog converters, the weights are powers of 2”); Ex. 1014 [Weir] 1:52-55 (“For example, the DAC may employ a set of resistors which are selected to produce voltages or currents having values of 512, 256, 128, 64, 32, 16, 8, 4, 2 and 1”); Ex. 1019 [Boyacigiller] 4:20-30.

257. As *Weir* itself provides for the LSB having a radix of approximately 1.99, it suggests to a POSITA that the LSB could have a radix of 2.

258. Further, *Weir* focuses on a problem in successive approximations when an “error occurs [that] can not be compensated for in later steps[,]” but there are no later steps than the LSB. Ex. 1014 [Weir] 2:52-56. As there are no later steps, the benefit of using a radix of less than 2 advocated in *Weir* is not necessary for the LSB.

259. Also, *Weir* notes that successive approximation systems may suffer reduced precision if a DAC element has an error greater than the magnitude of the smallest element in the series. Ex. 1014 [Weir] 2:11-17. However, the LSB has the smallest magnitude in the series.

E. Claim 9

1. [9a] The amplifier system of claim 1 further comprised of One-Time-Programmable memory for permanently storing an output of the successive approximation register,

260. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

261. For example, Weir indicates that a memory can be used, and the bit coefficients can be read from the memory. Ex. 1014 [Weir] 13:6-9. One time programmable (OTP) memory is a well know memory circuit used in integrated circuits. See e.g., Ex. 1019 [Boyacigiller] 3:12-14 (“The C-DAC receives as its digital input the output of an erasable programmable read only memory (EPROM) 24.”). Therefore, the combination includes One-Time-Programmable memory.

2. [9b] whereby a single output of the D/A converter controlling the input offset of the first amplifier may be permanently maintained.

262. This limitation is obvious in light of the *Wang-Weir-Ferguson* Combination.

263. For example, the output identified in element [1h] (i.e., signal VC) is permanently connected to the opamp.

X. RESERVATION OF RIGHTS

264. I reserve the right to amend or supplement this declaration as this case proceeds and any additional information comes to light.

265. I understand that traditionally no live expert testimony is used at the PTAB, and I presently have no plans to testify, however should I be asked, I reserve my right to use exhibits to summarize or exemplify my opinion (including exhibits I have not yet created) if called to testify.

266. If it would be helpful to the Board, I am willing and able to provide additional background.

267. I further reserve the right to respond to any opinion presented by any of Patent Owner's experts regarding the meaning of any claim term or limitation within the Asserted Claims.

268. I hereby declare that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Dated: 1/28/2025

Signed by:

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Ion Opris