Ion E. Opris

2198 Lark Hills Ct.
San Jose, CA 95138
(408) 483-3108

Strong background in analog and digital circuitry design and analysis, solid state device physics, and math. Extensive hands-on experience in analog and mixed-mode IC design, telecommunication systems, high frequency (RF) circuits, distributed amplifiers, phase-locked loops, and spread spectrum techniques, and MEMS interfaces.

EXPERIENCE

Opris Consulting
2198 Lark Hills Ct, San Jose, CA 95138 06/96 - present
An independent consulting firm for analog, mixed-mode and ASIC IC design. Specializing in high performance A/D converters (pipelined and sigma-delta) and communications circuits (CMOS synthesizers, switched cap filters, and RF receivers). Completed over 100 design projects for extremely low power sensors read-out circuitry, ultrasonic imaging, audio/video interface products, CCD and CMOS light sensors, wired and RF data communications (DSL, Ethernet, WI-FI, RFID), MEMS accelerometers, gyroscopes, and MEMS based displays.

MCube, Inc.
2750 Sand Hill Rd., Menlo Park, CA 94025
Sr. Director of IC Design 09/09 - 04/10
VP of Product Design 04/10 - 10/10
- responsible for the CMOS and MEMS design of a family of MEMS based accelerometers and magnetic sensors.

National Semiconductor Corp.
2900 Semiconductor Drive, Santa Clara, CA 95052
Principal Engineer 06/94 - 10/97
- responsible for system architecture and analog/digital circuit design for high speed/high resolution A/D converters; mixed-mode A/D, ASICs, and complex behavioral simulations;
- design of low power/high performance voltage references;
- released to production a family of high performance 12-bit A/D converters up to 20 MS/s.

Stanford University
Stanford, CA 94305
Research Assistant 09/90 - 12/95
- enrolled in a PhD program in Electrical Engineering. Areas of research:
    - analog/digital circuits for smart sensors applications;
    - low power A/D converters;
    - analog nonlinear circuits, and nonlinear control;
    - low power/low noise amplifiers and continuous time filters for biological data acquisition.

Core International 04/89 - 08/90
6500 E. Rogers Circle, Boca Raton, FL 33487
Design Engineer
- designed, built and tested DMA adapters (both slaves and masters) for tape drives, hard disk drives, and floppy drives, used in PC's with ISA and MicroChannel Architecture;
- evaluated a chip set for high speed interfaces on MicroChannel Architecture, and used it for a high performance hard drive adapter.

IAMSAT, Bucharest, Romania 10/86 - 10/88
Manufacturing and Service Company for Automation and Telecommunication
Research Engineer (on joint program with the Bucharest Polytechnic Institute)
- designed, built and evaluated the performances of low wattage switching power supplies;
- designed a driver/modulator for an IMPATT diode oscillator.
- designed the analog part of the servo system for a large capacity disk drive (removable media); built testing equipment; tested and evaluated the prototypes.

OTHER

1991 - present Various consulting jobs in hardware design /firmware with applications in RF data communication and spread spectrum technology. Hardware/firmware development for hand-held computing devices using touch screen technology and written character recognition.
1983 - 1986 Joined an university research team for data communication in the 10.7 GHz band.

ACADEMIC ACCOMPLISHMENTS

Ranked 2nd at the PhD Qualification Examination at Stanford University, January 1991. Awarded a School of Engineering Fellowship at Stanford University in 1990-1991. Ranked 1st in 1983, 1984, 1985, and 2nd in 1986 at the Romanian National Electronic Engineering contest. This highly competitive contest, open to all undergraduate students in the country, tests both theoretical and practical skills.

EDUCATION

PhD in Electrical Engineering, 1996, Stanford University, Stanford, CA.
Thesis: "Analog Rank Extractors and Sorting Networks."
Master of Science in Electrical Engineering, 1991, Stanford University, Stanford, CA.
Diploma of Engineer, 1986, Bucharest Polytechnic Institute, Romania, highest honors.
Major: Electronics and Telecommunications.

PERSONAL DATA

Enjoy outdoor sports, ski, tennis, soccer, skeet shooting.
Moderately fluent in French, basic knowledge of German.

PATENTS (83)

2021 "Highly accurate temperature sensors, and calibration thereof, for use with implantable medical devices", Pat. #11,077,308, August 3rd, 2021.
2021 "Parasitic insensitive sampling in sensors", Pat. #11,054,328, July 6th, 2021.
2021 "Unobtrusive eye mounted display", Pat. #11,029,535, June 8th, 2021.
2020 "Adaptive tuning of a contact lens", Pat. #10,673,414, June 2nd, 2020.
2020 "Unobtrusive eye mounted display", Pat. #10,649,233, May 12th, 2020.
2020 "Backplane for eye-mounted display", Pat. #10,580,349, March 3rd, 2020.
2020 "Integrated protection devices with monitoring of electrical characteristics", Pat. #10,559,559, February 11th, 2020
2019 "Microphone circuits for cancelling out the leakage characteristics of a transducer", Pat. #10,349,161, July 9th, 2019
2019 "Digital microphone and control method therefore", Pat. #10,250,980, April 2nd, 2019.
2018 "Charge pump with rapid discharge path", Pat. #10,110,121, October 23rd, 2018.
2018 "MEMS device quadrature shift cancellation", Pat. #10,060,757, August 28th, 2018.
2017 "Apparatus and method for extending analog front end sensor range for a high-Q MEMS sensor", Pat. #9,835,647, December 5th, 2017.
2017 "Temperature and power supply calibration", Pat. #9,759,564, September 12th, 2017.
2017 "Integrated protection devices with monitoring of electrical characteristics", Pat. #9,679,885, June 13th, 2017.
2017 "Apparatus and methods for PLL-based gyroscope gain control", Pat. # 9,644,963, May 9th, 2017.
2017 "MEMS quadrature cancellation", Pat. #9,625,361, April 18th, 2017.
2017 "MEMS device automatic gain control loop", Pat. #9,618,361, April 11, 2017.
2016 "Self test of MEMS accelerometer with ASICS integrated capacitors", Pat. #9,488,693, November 8, 2016.
2016 "MEMS device front-end charge amplifier", Pat. #9,444,404, September 13, 2016.
2016 "Binary coded, arbitrarily shaped received signal strength indicator", Pat. #9,417,272, August 16, 2016.
2016 "Uniform distribution dithering in sigma-delta A/D converters", Pat. #9,356,617, May 31, 2016.
2015 "MEMS driver", Pat. #9,094,027, July 28, 2015.
2015 "Self test of MEMS gyroscope with ASICs integrated capacitors", Pat. #9,069,006, June 30, 2015.

2015 “Memory circuit, persistent after the removal of the power supply”, Pat. #9,007,865, April 14, 2015.
2015 “Voltage amplifier for capacitive sensing devices using very high impedance”, Pat. #8,988,146, March 24, 2015.
2015 “Transcapacitance amplifier with picoAmperes input biasing and large output swing”, Pat. #8,928,409, January 6, 2015.
2014 “Single-phase clock D/A converter with built-in data combiner”, Pat. #8,830,101, September 9, 2014.
2014 “Accurate ninety-degree phase shifter”, Pat. #8,754,694, June 17, 2014.
2014 “Controller architecture for combination touch, handwriting, and fingerprint sensor”, Pat. #8,743,082, June 3, 2014.
2014 “Noise reduction method with chopping for merged MEMS accelerometer sensor”, Pat. #8,742,964, June 3, 2014.
2013 “Multi-phase digital phase-locked loop device for pixel clock reconstruction”, Pat. #8,502,581, August 6, 2013.
2011 “Self-biased Amplifier Device for an Electrecret Microphone”, Pat. #8,064,622, November 22, 2011.
2011 “Signal Channel Balancing”, Pat. #7,986,923, July 26, 2011.
2010 “High linearity gmC filter”, Pat. #7,760,012, July 20, 2010.
2010 “Analog-to-digital converter with reduced non-linearity”, Pat. #7,663,526, Feb. 16, 2010.
2009 “Methods of using predictive A/D converters”, Pat #7,609,185, Oct., 27, 2009
2008 “Low Voltage CMOS Driver For Inductive Loads”, Pat # 7,459,937, Dec. 2, 2008.
2008 “Predictive A/D converters and methods”, Pat # 7,405,689, July 29th, 2008.
2008 “Variable gain amplifier circuit”, Pat # 7,378,881, May 27th, 2008.
2008 “Image processing method and analog front end”, Pat # 7,375,665, May 20th, 2008.
2008 “System and method for generating an output oscillation signal with low jitter”, Pat #7,324,561, January 29th, 2008.
2007 “Multiple output PLL”, Pat. #7,209,008, April 24, 2007.
2007 “High sensitivity RFID TAG Integrated Circuits”, US 20070046369, March 2007.
2006 “Image processing method and analog front end circuit”, Pat. #7,098,832, August 29, 2006.
2006 “Oscillator with variable reference”, Pat. #7,098,753, August 29, 2006.
2005 “Digital amplifier”, Pat. #6,981,370, August 23, 2005.
2005 “Digital amplifier”, Pat. #6,933,778, August 23, 2005.
2005 “Digital amplifier”, Pat. #6,864,815, March 8, 2005.
2004 “ADC pipeline conversion”, Pat. #6,801,151, October 5, 2004.
2004 “Digital amplifier”, Pat. #6,791,404, September 14, 2004.
2004 “Digital amplifier”, Pat. #6,765,518, July 20, 2004.
2004 “Dual input differential amplifier”, Pat. #6,759,898, July 07, 2004.
2004 “ADC with digital averages”, Pat. #6,750,799, June 15, 2004.
2003 “Low voltage bandgap reference circuit”, Pat. #6,642,778, November 4, 2003.
2003 “Low voltage thermostat circuit”, Pat. #6,622,927, September 23, 2003.
2003 “Method for optimum common-mode voltage generator”, Pat. #6,603,354, August 5, 2003.
2003 “Low-voltage bandgap reference circuit”, Pat. #6,549,065, April 15, 2003.

2002 “Low-voltage bandgap reference circuit”, Pat. #6,426,669, July 30, 2002.
2002 “Low-voltage bandgap reference circuit”, Pat. #6,407,622, June 18, 2002.

2002 “Power saving method using interleaved programmable gain amplifier and converters for digital imaging devices”, Pat #6,342,919, Jan. 29, 2002.
2001 “Reference buffer technique for high speed switched capacitor circuits”, Pat #6,285,231, Sept. 4, 2001.
2001 “CMOS track and Hold circuit”, Pat #6,255,865, July 3, 2001.
2001 “Series resistance compensation in translinear circuits”, Pat #6,225,850, May 1, 2001.
2001 “Method and apparatus for generating a symmetrical output”, Pat #6,222,422, April 24, 2001.
2000 “Method for analog decimation of image signals”, Pat #6,166,779, Dec. 26, 2000.
2000 “Digitally self-cal. D/A Converter”, Pat #6,130,632, October 10, 2000.
2000 “Series resistance compensation in translinear circuits”, Pat #6,121,824, Sept. 19, 2000.
2000 “Algorithmic ADC with reduced DNL”, Pat #6,097,326, August 1, 2000.
2000 “High speed strobed comparator having a latch circuit”, Pat #6,060,912, May 9, 2000.
2000 “Reference buffer”, Pat #6,054,886, April 25, 2000.
1999 “ESD circuit”, Pat #5,973,897, October 26, 1999.
1999 “S/H circuit”, Pat #5,963,156, October 5, 1999.
1999 “Self-calibrating reversible pipeline A/D and D/A converter”, Pat #5,929,796, July 27, 1999.
1999 “Split capacitor array for D/A conversion”, Pat #5,889,486, March 30, 1999.
1999 “Calibration method for monotonic A/D conversion”, Pat. #5,861,828, Jan. 19, 1999.
1998 “High speed differential opamp...”, Pat #5,847,607, December 8, 1998.
1998 “Bias circuit for switched capacitor applications”, Pat. #5,838,191, November 17, 1998.
1998 “Differential amplifier with switched capacitor common-mode feedback”, Pat. #5,838,200, November 17, 1998.
1998 “Pipeline analog to digital converter architecture with reduced mismatch error”, Pat. #5,710,563, January 20, 1998.
1997 “Radix-2 Architecture and Calibration Technique for Pipelined Analog to Digital Converters”, Pat. #5,668,549, September 16, 1997.
1997 “Bit Parallel Adder with Alternating Polarity Carry Look Ahead”, Pat. #5,619,442, April 8, 1997.
1996 “CMOS Strobed Comparator with Programmable Hysteresis”, Pat. #5,528,185, June 18, 1996.
1996 “Multi-phase Pipeline A/D Converter”, Pat. #5,541,602, July 30, 1996.
1996 “Low Noise Digital Output Buffer”, Pat. #5,656,947, August 12, 1997.

PUBLICATIONS (32)

2021 "A universal 3D imaging sensor on a silicon photonics platform", Nature, Vol 590, Issue 7845, Feb. 11, 2021.

2000 "A 12-Bit 50 Mpixel/s Analog Front End Processor for Digital Imaging Systems", Hot Chips 12, Conference Proceedings, Aug. 13-15, 2000.

2000 "The Concept of Operational Rank Extractor", Analog Integrated Circuits and Signal Processing, vol, 23, no. 3, pp.189-198, June 2000.

2000 "A Pipeline A/D Converter Architecture with Low DNL", IEEE Journal of Solid-State Circuits, vol. SC-35, no. 2, pp. 281-285, Febr. 2000.

1998 "A Single-ended Input 12-Bit 20MS/s A/D Converter", IEEE Journal of Solid-State Circuits, vol. SC-33, no. 12, pp. 1898-1903, Dec. 1998.

1998 "Rail-to-Rail Multiple-input Min./Max. Circuit", IEEE Transactions on Circuits and Systems, Part II, vol. TCAS-45, no. 1, pp. 137-140, Jan. 1998.

1998 "Series Resistance Compensation in Translinear Circuits", IEEE Transactions on Circuits and Systems, Part I, vol TCAS-45, no. 1, pp 91-94, Jan. 1998.

1998 "A Single-ended Input 12-Bit 20MS/s A/D Converter", IEEE Int. Solid State Circuits Conference ISSCC 1998, Febr. 1998, pp.138-139.

1998 "Bootstrapped Pad Protection Structure", IEEE Journal of Solid-State Circuits, vol. SC-33, no. 2, pp. 300-301, Febr. 1998.

1997 "Analog Rank Extractors", IEEE Transactions on Circuits and Systems, Part I, vol. TCAS-44, no.12, Dec. 1997, pp. 1114-1121.

1997 "Bias Circuit for Switched Capacitor Amplifiers", IEEE Transactions on Circuits and Systems, Part II, vol. TCAS-44, no. 12, Dec. 1997, pp.985-989.

1997 "Noise Estimation in Strobed Comparators", Electronics Letters, vol. 33, no. 15, pp. 1273-1274, July 1997, UK.

1997 "A High-Speed Median Circuit", IEEE Journal of Solid-State Circuits, vol. SC-32, no. 6, pp. 905-908, June 1997.

1997 "Force-balanced Accelerometer with mG Resolution, fabricated using Silicon Fusion Bonding and Deep Reactive Ion Etching", Int. Solid State Sensors and Actuators, Transducers 1997, vol. 2., pp. 1229-1230, 16-19 June 1997, Chicago, IL.

1997 "Plasma-etched neural probes", Sensors and Actuators A (Physical), vol. A58, no. 1, pp. 27-35, Jan 1997.

1996 "Planar Electrode Array Systems for Neural Recording and Impedance Measurements", Proceedings of the 18th Int. Conference of the IEEE Engineering in Medicine and Biology Society. (1997) vol. 1, pp. 106-107, Amsterdam, Netherlands 31 Oct. - 3 Nov. 1996.

1996 "A Rail-to-Rail Ping-Pong Opamp", IEEE Journal of Solid-State Circuits, vol. SC-31, no. 9, pp. 1320-1324, September 1996.

1996 "Multi-input strobed analogue comparator", Electronics Letters, vol. 32, no. 15, pp. 1332-1334, July 1996, UK.

1995 "3-Input Camera Focus Using a Parallel Fuzzy Logic Controller", Fuzzy Logic'95 Conference Proceedings, pp. 16.1-16.12, Burlingame, CA, November 7-9, 1995.

1995 "Large-signal subthreshold CMOS transconductance amplifier", Electronics Letters, vol. 31, no. 9, pp. 718-720, April 1995, UK.

1995 “A Videobandwidth Median Filter”, IEEE Custom Integrated Circuits Conference, CICC 1995, pp. 555-558.

1994 “Voltage-mode Defuzzification Circuits”, The Int. Journal of Electronics, vol. 77, no. 6, pp. 1043-1057, 1994, UK.

1994 “A Voltage-mode Analog Fuzzy Logic Controller”, Fuzzy Logic’94 Conference Proceedings, pp. 475-485, San Diego, CA, September 13-15, 1994.

1994 “Analogue Median Filter”, Electronics Letters, vol. 30, no. 17, pp. 1369-1370, August 1994, UK.

1994 “A Fast Precision Rectifier”, Electronics Letters, vol. 30, no. 16, pp. 1269-1270, August 1994, UK.

1994 “An Improved Analog Median Filter”, Electronics Letters, vol. 30, no. 4, pp. 284-285, February 1994, UK.

1993 “BiCMOS Tunable Membership Function Circuits”, The Int. Journal of Electronics, vol. 75, no. 4, pp. 689-696, 1993, UK.

1993 “BiCMOS Circuits for an Analog Fuzzy Processor”, Proceedings of the European Conference on Circuit Theory and Design - ECCTD 93, Davos, Switzerland.

1993 “Current-Mode Fuzzy Memory Element”, Electronics Letters, vol. 29, no. 2, pp. 236-237, January 1993, UK.

1989 “IMPATT Diode in a Coaxial Mounting. Performance and Design”, 5th Romanian Microwave Conference, December 1989, Bucharest, Romania.

1988 “Stability of Operational Amplifiers with Positive Feedback”, Romanian Annual Semiconductor Conference, September, 1988.

1987 “IMPATT Diode Applications in Microwave Oscillators”, Romanian Annual Semiconductor Conference, September 1987.