

SA 21.3: A High-Performance Autozeroed CMOS Opamp with 50 μ V Offset

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Bandwidth, dc gain, offset and noise are the major performance parameters that limit the applicability of operational amplifiers (opamps). The design of a general-purpose opamp in a digital CMOS process that offers excellent performance in all these categories is a long-standing challenge for the analog designer. While MOSFET amplifiers have extremely small bias currents, they exhibit much larger offset voltages and low-frequency noise than their BJT counterparts.

A high-performance opamp in a 1 μ m 5V digital CMOS technology achieves high dc gain, as well as excellent PSRR and CMRR and is capable of driving a 100 Ω , 1nF load. It uses a mixed-mode (analog/digital) compensation loop to reduce input offset to <50 μ V. The loop uses digital offset extraction and storage circuitry, and has an analog current-mode output. Offset cancellation can be performed at power-up or upon request.

Unlike existing commercially available low-offset high-precision amplifiers, the opamp needs only a single 5V low-voltage supply, requires no trimming, and uses no BJTs or JFETs. Thus, although developed as a stand-alone product, it can potentially be used as an on-chip component of larger mixed-mode ICs.

A schematic of the autocalibrated offset opamp is shown in Figure 1. For high dc gain, large bandwidth, high CMRR and PSRR, and drive capability, the opamp is built around a 3-stage topology: two gain stages and one rail-to-rail, class AB output stage. The input pair M1 and M2 is cascoded by transistors M5 and M6 to maximize CMRR performance. A multipath nested Miller topology is used for frequency compensation [1]. The additional input pair M3 and M4 bypasses the intermediate stage M7 and M8 at high frequencies to improve stability.

A smooth transition from the high-gain, low-frequency path to the low-gain, high-frequency path requires matching transconductances of M1 and M2 to those of M3 and M4. The class-AB output stage features rail-to-rail voltage swing and incorporates additional switches (M12 and M13) to put the output node into high-impedance mode during auto-calibration [2]. The offset cancellation uses a current-mode DAC (CALDAC), the full-scale current of which is approximately 10% of the input pair tail current. This allows the cancellation of up to ± 5 mV input offset. The digital code producing the cancellation current is stored in the successive approximation register (SAR).

During autocalibration, when CAL=1, the opamp is removed from the signal path. Both inputs are tied to GND and the output transistors M10 and M11 are disconnected from their respective supplies. The output is thus floating, while the small replica transistors M20 & M21 (scaled to M10 & M11) are used to provide the amplifier output signal for the calibration circuit. The compensation capacitors Cc1, Cc2 and Cc3 are no longer necessary since the opamp is now used in open-loop configuration as a comparator, and are also disconnected from the output terminal. When offset cancellation is initiated after power-up or user request, an on-chip RC oscillator is activated to provide timing of the successive approximation algorithm, which is completed after

N clock cycles, where N is the number of bits required by the DAC.

During calibration, the output offset voltage approaches zero, and the amplifier enters its linear operating range. However, due to high-frequency noise, the output voltage may swing rapidly up and down, since the opamp is no longer band-limited by the compensation capacitors. This could severely limit the accuracy of an offset cancellation procedure (such as the successive approximation algorithm) that does not involve some kind of averaging.

This is the reason why a simple low-pass filter (LPF) is introduced in the decision chain. The LPF is implemented here in an analog manner and is followed by a Schmitt trigger to interface with the SAR logic. Note that filtering could be implemented digitally as well, but this was found to require more chip area.

The key opamp parameters CMRR, PSRR and offset drift are optimized for offset performance. The linearity of the CALDAC, however, is not important as long as its monotonicity is guaranteed. The DAC is implemented as a binary-weighted current array using a pseudo R-2R MOSFET ladder architecture that requires only 3N identical MOSFETs for N-bit resolution [3]. The DAC area is only 0.04mm² for N=12, including the control switches.

The ability to read from or to write into the SAR register directly is a feature of this architecture that allows easy monitoring of the offset performance by retrieving the digital code stored in the SAR after calibration. For example, during wafer test it is easy to check whether the offset stays within prescribed limits by making sure that the opamp output changes from zero to VDD when lower and upper full-scale codes are entered successively into the SAR.

A die micrograph of the 2.2x1.9mm² chip containing two opamps is shown in Figure 2. It is in a 5V single-poly, double-metal, 1 μ m digital CMOS process. To fit into an 8-pin package while preserving compatibility with current industry standards, the circuit is programmed to perform offset auto-calibration automatically after power-up. Each opamp is protected against short-circuits and has its own biasing, calibration DAC and control logic. They share a 10kHz RC oscillator and frequency divider, power-on reset and test mode control logic. Autocalibration is simultaneous on both amplifiers and requires about 250ms. Performance of the op amp is summarized in Table 1, the offset and offset drift distributions are given in Figures 3 and 4. Equivalent noise input and amplification and phase margin variation with frequency are shown in Figures 5 and 6.

Acknowledgments

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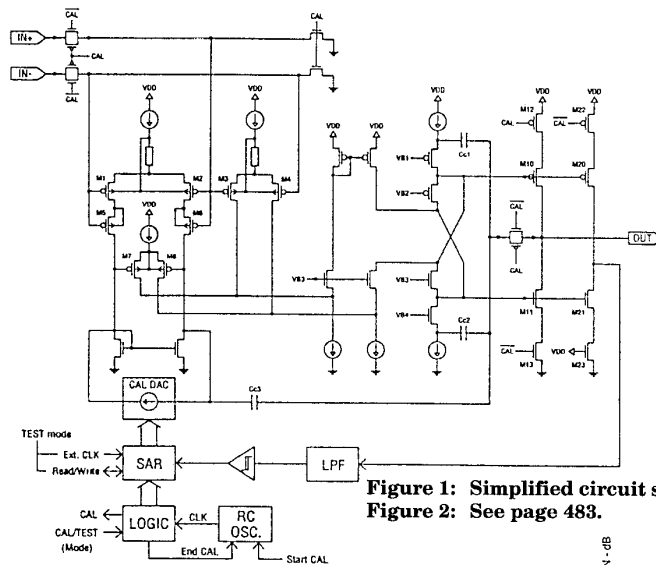


Figure 1: Simplified circuit schematic.

Figure 2: See page 483.

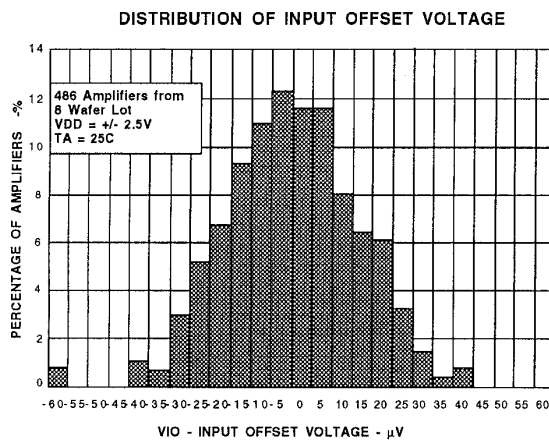


Figure 3: Distribution of input offset voltage.

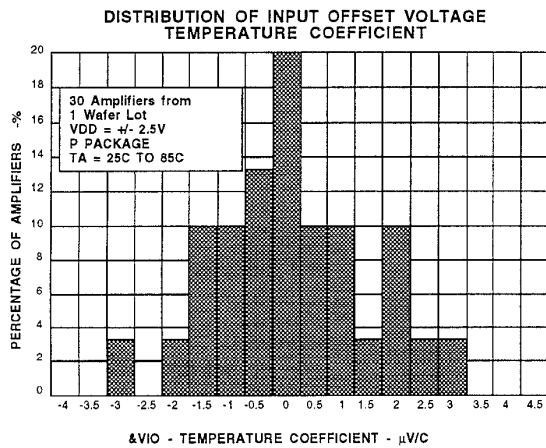


Figure 4: Input offset voltage temperature coefficient.

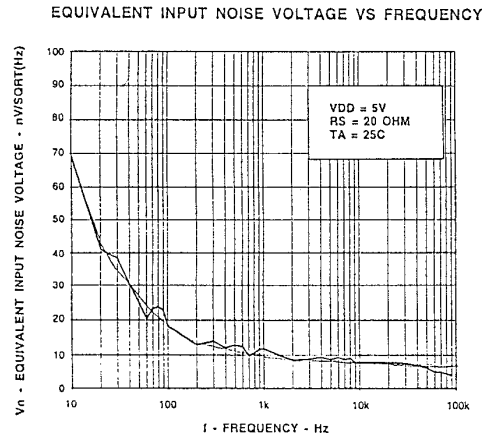


Figure 5: Equivalent input noise.

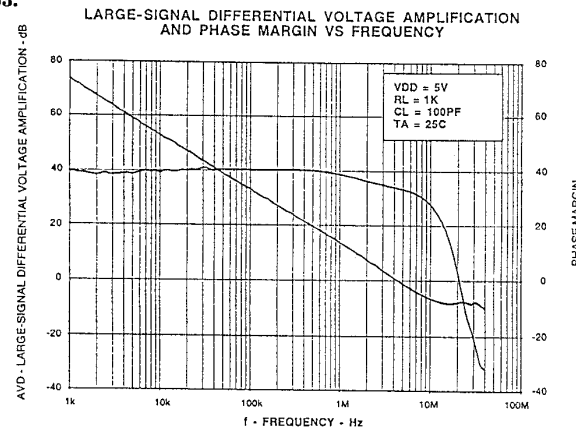


Figure 6: Amplification and phase margin vs. frequency.

	Min	Typ	Max	Unit
Input offset	-50	Figure 3	50	μV
Input offset drift	-3.0	Figure 4	3.0	μV/°C
Input offset		5		pA
Input bias		20		pA
Equivalent input noise				
at 10Hz/1kHz		70 / 10		nV/(Hz)
CMRR dc / 100kHz		105 / 65		dB
PSRR dc / 100kHz		120 / 65		dB
Common mode range	-0.2		3.2	V
Voltage gain (RL=1 kΩ)		4000		V/mV
Unity-gain bandwidth		4.5		MHz
Phase margin (CL=100 pF)/70				°
Full-power bandwidth		600		kHz
Slew rate	-33.		3.9	V/μs
Output swing (RL=600Ω)	0.1		4.9	V
Short-circuit				
current limiting		±60		mA
Supply current		1.3		mA
Supply voltage range	3.5		5.5	V
Offset calibration time		250		ms

Table 1: Measured performance at VDD = 5V and Ta = 25°C.