

HIGH-PRECISION DAC BASED ON A SELF-CALIBRATED SUB-BINARY RADIX CONVERTER

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ABSTRACT

A novel DAC architecture based on a sub-binary radix converter is presented. By calibrating digitally the non-linear sub-binary converter, it is possible to use it as a high-precision, high-resolution digital-to-analog converter. The analog part of the new DAC doesn't need precise components. It becomes thus possible to build high-performance DACs on a small area, neither requiring aggressive analog design nor highly matched components. By relaxing the constraints on the analog part, this new topology is very promising for the design of high-performance converters with modern technologies. Both digital and analog components are straightforward to design, allowing their automated synthesis by CAD tools. The new converter structure is presented, and the necessary calibration and conversion algorithms are detailed.

1. INTRODUCTION

Sub-binary structures are very attractive when used in conjunction with a successive approximation algorithm, because they are insensitive to component value variation and can achieve any given resolution. If the design correctly takes into account the components' tolerances, the radix is adjusted to avoid missing codes [1]. Even when using imprecise components, and thus small structures, it is possible to achieve arbitrarily high resolutions.

But the major drawback is that code redundancies are introduced and that the converter is highly non-monotonic and totally imprecise [2]. Thus, in spite of the fact that these converters are very useful for precisely calibrating a value using successive approximations, they cannot be used directly as digital-to-analog converters.

This paper presents a digital self-calibration algorithm and a radix-conversion algorithm. They allow the use of a

sub-binary converter as a conventional digital-to-analog converter, by eliminating duplicate codes to make the converter monotonic. The converter is calibrated by itself, without the need for supplementary precise elements. With this technique, it is possible to design a high-precision digital-to-analog converter without precise analog components.

2. SUB-BINARY CONVERTERS

In conventional digital-to-analog converters, the weights are powers of 2. Any imprecision in one of them can easily cause a missing code or make the converter non-monotonic. It is thus very problematic to design a high-precision converter using modern technologies, with which it is difficult to achieve precise components. The commonly adopted solution is aggressive analog design, e.g. matching, but this necessitates an important circuit area.

Sub-binary converters use another approach: They use weights that are voluntarily not powers of 2 but a little less, e.g. 1.9. Redundancies are deliberately introduced, which make the converter non-monotonic. This important feature allows guaranteeing that the converter will have no missing code, even when low-precision components are used. That is why sub-binary converters are useful in conjunction with a successive approximation algorithm to calibrate systems with a high resolution.

There are different kinds of sub-binary digital-to-analog converters: $R/\beta R$ ladders [1], sub-binary current sources [2], etc. The input/output characteristics of such a sub-binary converter are shown in Figure 1.

The shaded codes are redundant and make the converter non-monotonic. Because of them, it is impossible to use it as a conventional DAC. But these duplicate codes can be removed using the calibration technique presented below. At the end of the calibration the DAC, which is already free of missing codes, furthermore becomes monotonic (Figure 2) and can be used like any conventional DAC.

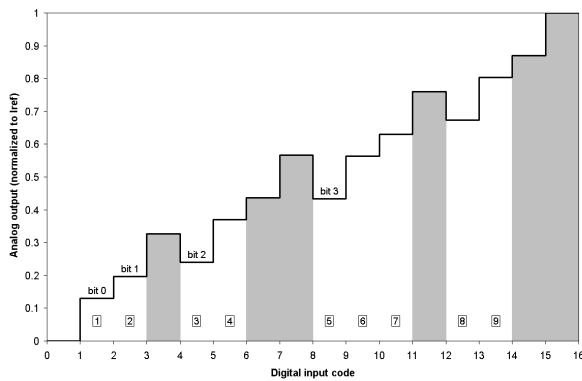


Figure 1: Input/Output characteristics of a sub-binary DAC before calibration

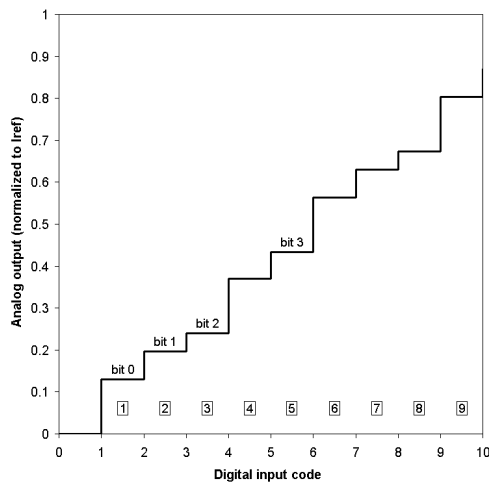


Figure 2: Input/Output characteristics of the sub-binary DAC after calibration and with radix conversion

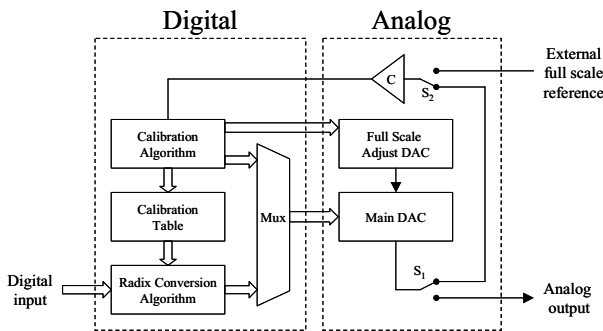


Figure 3: System architecture

3. SUB-BINARY CONVERTER CALIBRATION

The goal of the calibration is to identify and to remove all the duplicate codes that make the sub-binary DAC non-monotonic. The digital calibration circuit is shown in Figure 3. It consists of a calibration table, which stores the

results of the calibration, and two different algorithms (calibration and radix conversion) to pilot the sub-binary DAC (main DAC). A second DAC (full scale adjust) is used to calibrate the main DAC's full scale.

At power-up, before the DAC can be used, the first algorithm (the calibration algorithm) takes control of the main DAC and fills in the calibration table, using comparator C to identify the redundant codes. It also adjusts the main DAC's full scale through the full scale adjust DAC. The system is then ready for normal use. For each digital input code, the radix conversion algorithm computes, based on the information stored in the calibration table, the digital code needed to pilot the sub-binary main DAC.

4. CALIBRATION ALGORITHM

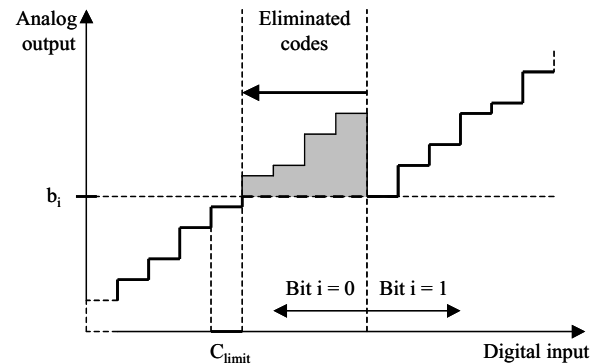


Figure 4: Calibration principle

At power-up, this algorithm fills in the calibration table. It is a recursive successive approximation algorithm, which quantifies each bit of the sub-binary converter. It is based on the following concept: Since the converter has no missing code but is non-monotonic, it locates the duplicate codes in order to make the converter monotonic. Figure 4 shows a part of the original characteristics of a sub-binary converter before calibration. Preceding the code corresponding to the transition of a bit i from 0 to 1, there may be some codes for which the output value is higher (shaded in the figure) and make the converter non-monotonic. The calibration algorithm determines, for every bit, the last code C_{limit} that is inferior to the value of the next bit. This is done by the means of a successive approximation algorithm that is applied successively for each bit, starting with the LSB and ending with the MSB. Each bit is estimated using the already calibrated least significant bits and the analog comparator. Let us name b_i ($i = 0$ is the LSB and $i = n$ the MSB) the output values generated by the converter for each bit i . The algorithm computes the calibration table so that for each bit i , the digital stored code w_i is the number of monotonic output steps until the bit's value b_i is reached and the corresponding bit i has to be set.

The algorithm is:

```

w0 = 1
for i=1 to n
  wi = 1
  b = 0
  for j=i-1 downto 0
    if b + bj < bi then
      b = b + bj
      wi = wi + wj
    end if
  end for
end for

```

First, the LSB is calibrated to be 1 elementary step. Then, the outer loop calibrates each bit successively by using a successive approximation algorithm (inner loop). At the end of the inner loop, the following relations hold:

$$b = \sum_{j=0}^{i-1} e_j b_j = b_i - \varepsilon b_0 \quad (1)$$

$$w_i = \sum_{j=0}^{i-1} e_j w_j + 1 \quad (2)$$

Equation (1) states that the successive algorithm decides correctly whether each bit j has to be kept or not ($e_j = 1$ if bit j is kept, else $e_j = 0$) and adjusts the successively tested value b to calibrate b_i with a precision of 1 LSB ($0 \leq \varepsilon \leq 1$) without exceeding it. Equation (2) shows that the new value in the calibration table is computed by adding the already calibrated values corresponding to the bits that are kept by the successive approximation algorithm, plus one.

At the end, the converter is totally monotonic if the input codes are converted using the radix conversion algorithm presented below.

There is still one more parameter to calibrate, which is the DAC's full scale. The calibrated characteristic is now totally monotonic, but its slope can vary, depending on the repartition of the different step sizes (ε in equation 1). The full scale of the converter has thus to be adjusted precisely to be equal to an external reference, by adjusting the reference current of the main DAC with a second sub-binary DAC (full scale adjust). Its digital control value is calibrated using a successive approximation algorithm.

5. RADIX CONVERSION ALGORITHM

Once the converter is calibrated, it can be used as a conventional DAC. But the digital input codes have to be converted by an algorithm that performs radix conversion. By successive subtractions of the calibration values w_i

from the input value (d), it determines which bits of the main converter have to be set and which have to be cleared:

```

e = d
for i = n downto 0
  if e ≥ wi then
    e = e - wi
    bit i is set (1)
  else
    bit i is cleared (0)
  end if
end for

```

At the end of the algorithm, $e = 0$ and the value at the output of the converter is the d th monotonic step, which is the expected value.

It is noteworthy that this algorithm works in a very similar manner to a successive approximation algorithm. The difference is that it performs in the digital domain, using a simple ALU to make subtractions and comparisons. But both algorithms presented here can share their control circuitry.

6. ANALOG CIRCUIT IMPLEMENTATION

The analog part of the system consists of two sub-binary DACs and one single-input current comparator. They are all easy to design and occupy a small area, because they don't need to be precise.

6.1. Sub-binary DAC

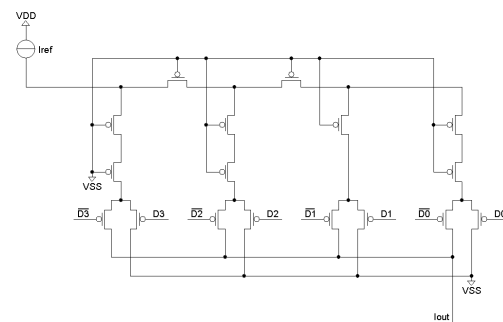


Figure 5: M/3M sub-binary DAC

Figure 5 shows a variant of a R/3R ladder, namely a 4 bits M/3M ladder. It exploits the fact that under specific bias conditions [3], MOS transistors behave almost like resistors. This circuit is used as the main DAC and the full scale adjust DAC in Figure 3. In each branch, the ladder voluntarily divides the current into two unequal parts. In this way, it can stand a mismatch in the transistor characteristics. Because the matching of the transistors is not important, the devices can be small. There are other

variants of this ladder, e.g. M/2.5M, which can be used when more precise devices are available.

6.2. Current comparator

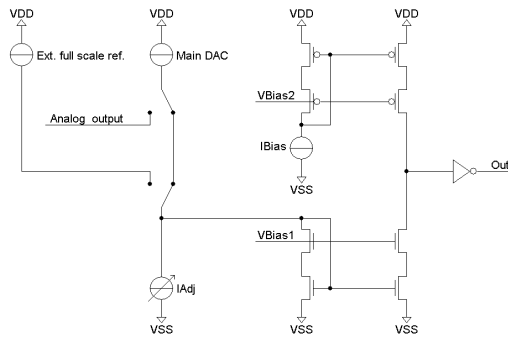


Figure 6: Single-Input current comparator

The comparator used to calibrate the main DAC must be able to compare two current values presented successively in its unique input. These two currents are generated by the main DAC successively under the control of the calibration algorithm (line 6: if $b + b_j < b_i$ then). The comparator must be able to detect a current difference as small as 1 LSB, in a range between 0 and the full scale current. Figure 6 shows the implementation of such a comparator. It consists of a variable current source (a sub-binary DAC), whose value is adjusted by successive approximations to a value close to the first of the two currents to compare. Then, the second current is switched in instead of the first one, and the residual current difference is amplified by a second high-gain stage. At this point, it is possible to determine which current is bigger, with a high precision.

Since this circuit amplifies the difference between the two currents, its linearity and precision are not important. Consequently, the comparator can also be realized without needing aggressive analog design, and requires only a small area.

7. RESULTS

The converter structure has been extensively simulated using Monte-Carlo and worst-case analyses, on 10 million samples. The results showed that an 18 stage R2.5R sub-binary ladder can be used as a conventional DAC with a 12 bits precision and a 15 bits resolution. Figure 7 shows the simulated INL for a sample of this converter.

The digital circuitry was designed using VHDL and an automated synthesis tool was used to realize a 0.3 mm^2 layout in a $0.35\mu\text{m}$ technology. A 17 stage M/3M DAC was integrated in a $0.8\mu\text{m}$ technology. Figure 8 shows a micrograph of this circuit. It occupies 0.03 mm^2 , which is 10 times smaller than the digital circuitry.

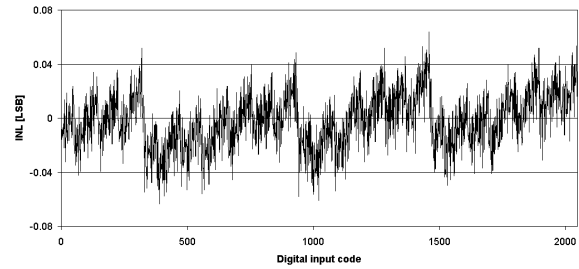


Figure 7: Simulated INL

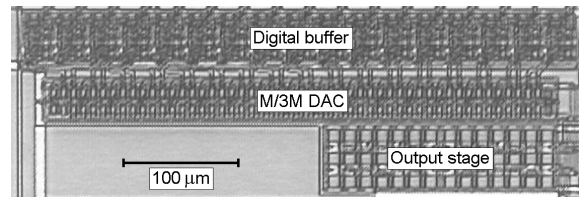


Figure 8: Chip Micrograph

These results confirm that the area of the digital circuitry is predominant, and that a high-resolution and high-precision converter can be designed with low-precision and small-area devices.

8. CONCLUSION

This paper presents how a sub-binary converter can be used as a conventional DAC. The necessary adjustments are made in the digital domain, and there is no need for precise analog circuitry. This makes the architecture very attractive, because it still allows very high performances and easy retargeting when modern technologies are used, and even enables the automatic conception of these converters by CAD tools. And finally, the total area of the system is very small. All these advantages make this new topology very promising for the realization of high-performance digital-to-analog converters.

9. REFERENCES

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