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PTO/SB/05 (07-07)

Approved for use through 06/30/2010. OMB 0651-0032
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UTILITY PATENT APPLICATION TRANSMITTAL (ONLY FOR NEW NONPROVISIONAL APPLICATIONS UNDER 37 CFR 1.53(B))	Attorney Docket No. 0365-0644PUS2	
	First Inventor Risto TUOMINEN	
	Title	ELECTRONIC MODULE
	Express Mail Label No.	

APPLICATION ELEMENTS See MPEP chapter 600 concerning utility patent application contents.	ADDRESS TO: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	
1. ☒ Fee Transmittal Form (e.g., PTO/SB/17) (Submit an original and a duplicate for fee processing) 2. ☐ Applicant claims small entity status. See 37 CFR 1.27. 3. ☒ Specification [Total Pages 29] Both the claims and abstract must start on a new page (For information on the preferred arrangement, see MPEP 608.01(a)) 4. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets 8] 5. Oath or Declaration [Total Sheets] a. ☐ Newly executed (original or copy) b. ☒ A copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Box 18 completed) i. ☐ DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) name in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 6. ☐ Application Data Sheet. See 37 CFR 1.76 7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix) ☐ Landscape Table on CD 8. Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. - c. are required) a. ☐ Computer Readable Form (CRF) b. Specification Sequence Listing on: i. ☒ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PARTS 9. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee 10. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☒ Power of Attorney 11. ☐ English Translation Document (if applicable) 12. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☒ Copies of citations attached 13. ☐ Preliminary Amendment 14. ☒ Return Receipt Postcard (MPEP 503) (Should be specifically itemized) 15. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 16. ☐ Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 17. ☐ Other:	
18. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in the first sentence of the specification following the title, or in an Application Data Sheet under 37 CFR 1.76: ☒ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application No.: 10/546,820 Prior application information: Examiner C.J. ARBES Art Unit: 3729		

19. CORRESPONDENCE ADDRESS			
☒ The address associated with Customer Number: 02292 OR ☐ Correspondence address below			
Name			
Address			
City		State	Zip Code
Country	Telephone	Email Address	
Signature		Date	October 17, 2007
Name (Print/Type) James M. Slattery		Registration No. (Attorney/Agent)	28,380

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Effective on 12/08/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2008		Complete if Known	
☐ Applicant claims small entity status. See 37 CFR 1.27		Application Number	
		Filing Date	Concurrently Herewith
		First Named Inventor	Risto TUOMINEN
		Examiner Name	C. J. Arbes
		Art Unit	3729
TOTAL AMOUNT OF PAYMENT		(\$)	1,700.00
		Attorney Docket No.	0365-0644PUS2

METHOD OF PAYMENT (check all that apply)

☐ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 02-2448
 Deposit Account Name: Birch, Stewart, Kolasch & Birch,

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below
 ☐ Charge fee(s) indicated below, except for the filing fee

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17
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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	310	155	510	255	210	105	1,030.00
Design	210	105	100	50	130	65	
Plant	210	105	310	155	160	80	
Reissue	310	155	510	255	620	310	
Provisional	210	105	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	210	105
Multiple dependent claims	370	185

Total Claims Extra Claims Fee (\$) Fee Paid (\$) Multiple Dependent Claims
 25 - 20 = 5 x 50.00 = 250.00 Fee (\$) Fee Paid (\$)

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims Extra Claims Fee (\$) Fee Paid (\$)
 5 - 3 = 2 x 210.00 = 420.00

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3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)
37	- 100 =	/50 =	(round up to a whole number) x	

4. OTHER FEES(S)

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): _____

SUBMITTED BY			
Signature		Registration No. (Attorney/Agent)	28,380
Name (Print/Type)	James M. Slattery	Telephone	(703) 205-8000
		Date	October 17, 2007

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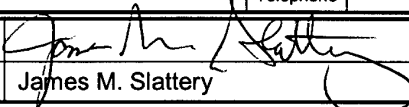
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		Examiner Name	C. J. Arbes
		Art Unit	3729
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☐ Check
 ☐ Credit Card
 ☐ Money Order
 ☐ None
 ☐ Other (please identify): _____

☒ Deposit Account
 Deposit Account Number: 02-2448
 Deposit Account Name: Birch, Stewart, Kolasch & Birch,

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

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Other (e.g., late filing surcharge): _____

SUBMITTED BY			
Signature		Registration No. (Attorney/Agent)	28,380
Name (Print/Type)	James M. Slattery	Telephone	(703) 205-8000
		Date	October 17, 2007

Electronic Module

CROSS REFERENCE TO RELATED APPLICATIONS

[001] The present application is a Continuation of co-pending Application No. 10/546,820, filed on August 25, 2005, the entire contents of which are hereby incorporated by reference and for which priority is claimed under 35 U.S.C. § 120.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an electronic module.

[002] In particular, the invention relates to an electronic module, which includes one or more components embedded in an installation base. The electronic module can be a module like a circuit board, which includes several components, which are connected to each other electrically, through conducting structures manufactured in the module. The components can be passive components, microcircuits, semiconductor components, or other similar components. Components that are typically connected to a circuit board form one group of components. Another important group of components are components that are typically packaged for connection to a circuit board. The electronic modules to which the invention relates can, of course, also include other types of components.

[003] The installation base can be of a type similar to the bases that are generally used in the electronics industry as installation bases for electrical components. The task of the base is to provide components with a mechanical attachment base and the necessary electrical connections to both components that are on the base and those that are outside the base. The installation base can be a circuit board, in which case the construction and method to which the invention relates are closely related to the manufacturing technology of circuit boards. The installation base may

also be some other base, for example, a base used in the packaging of a component or components, or a base for an entire functional module.

[004] The manufacturing techniques used for circuit boards differ from those used for microcircuits in, among other things, the fact that the installation base in microcircuit manufacturing techniques, i.e. the substrate, is of a semiconductor material, whereas the base material of an installation base for circuit boards is some form of insulating material. The manufacturing techniques for microcircuits are also typically considerably more expensive than the manufacturing techniques for circuit boards.

[005] The constructions and manufacturing techniques for the cases and packages of components, and particularly semiconductor components differ from the construction and manufacture of circuit boards, in that component packaging is primarily intended to form a casing around the component, which will protect the component mechanically and facilitate the handling of the component. On the surface of the component, there are connector parts, typically protrusions, which allow the packaged component to be easily set in the correct position on the circuit board and the desired connections to be made to it. In addition, inside the component case, there are conductors, which connect the connector parts outside the case to connection zones on the surface of the actual component, and through which the component can be connected as desired to its surroundings.

DESCRIPTION OF BACKGROUND ART

[006] However, component cases manufactured using conventional technology demand a considerable amount of space. As electronic devices have grown smaller, there has been a trend to eliminate component cases, which take up space, are not essential, and create unnecessary costs. Various constructions and methods have been developed to solve this problem.

[007] One known solution is flip-chip (FC) technology, in which non-packaged semiconductor components are installed and connected directly to the surface of the circuit board. However, flip-chip technology has many weaknesses and difficulties. For example, the reliability of the connections can be a problem, especially in applications, in which mechanical stresses arise between the circuit board and the semiconductor component. In attempts to avoid mechanical stresses, a suitable elastic underfill, which equalizes mechanical stresses, is added between the semiconductor component and the circuit board. This procedural stage slows down the manufacturing process and increases costs. Even the thermal expansion caused by the normal operation of a device may cause mechanical stresses large enough to compromise the long-term reliability of an FC structure.

[008] US patent publication 4 246 595 discloses one solution, in which recesses are formed in the installation base for the components. The bottoms of the recesses are bordered by an insulation layer, in which holes are made for the connections of the component. After this, the components are embedded in the recesses with their connection zones facing the bottom of the recess, electrical contacts being formed to the components through the holes in the insulation layer. In such a method, problems can arise, for instance, when aligning the feed-throughs with the contact zones of the component. This is because the feed-throughs must be aligned relative to components lying under the insulation layer. In other ways too, the method does not correspond to the technology used nowadays (the patent dates from 1981).

[009] JP application publication 2001-53 447 discloses a second solution, in which a recess is made for the component in the installation base. The component is placed in the recess, with the component's contact zones facing towards the surface of the installation base. Next, an insulation layer is made on the surface of the installation base and over the component. Contact openings for the component are made in the insulation

layer and electrical contacts are made to the component, through the contact openings. In this method too, the alignment of the feed-throughs with the contact zones of the component can cause problems, as the alignment must be made relative to a component lying under the insulation layer. In the method, considerable accuracy is demanded in manufacturing the recess and setting the component in the recess, so that the component will be correctly positioned, to ensure the success of the feed-throughs, relative to the width and thickness of the installation board.

[0010] In general too, the connection of components through feed-throughs made in the insulation layer creates a challenge to techniques, in which an attempt is made to embed components inside a circuit board or other installation base. Problems can arise, for example, due to the alignment precision, the stress created on the surface of the component by the manufacture of the hole, and by the covering of the edge areas of the feed-through by conductive material. Even a partial reduction of the problems relating to feed-throughs would be beneficial to the low-cost manufacture of reliable electronic modules that include unpackaged components embedded in an installation base. On the other hand, embedding a component inside an installation base will allow the construction to better withstand mechanical stress, which has been a problem in flip-chip technology.

SUMMARY AND OBJECTS OF THE INVENTION

[0011] According to an aspect of the invention, there is provided an electronic module comprising a first conductive-pattern layer having contact bumps made on its first surface, a component having flat contact zones, and an insulating-material layer on the first surface of the first conductive-pattern layer, wherein the component is embedded in the insulating-material layer and the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

[0012] According to another aspect of the invention, there is provided an

electronic module comprising a first and second conductive-pattern layers, an insulating-material layer between the first and second conductive-pattern layers, contact bumps made on the surface of the first conductive-pattern layer, and a component having flat contact zones embedded in the insulating-material layer such that the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the surface of the first conductive-pattern layer.

[0013] According to further aspects of the invention, there are provided multi-layered electronic modules comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality is an electronic module according to the above-mentioned aspects of the invention.

[0014] Considerable advantages are gained with the aid of embodiments of the invention. This because it is possible, with the aid of the embodiments, to embed unpackaged components in an installation base, reliably and economically.

[0015] Because the components can be embedded inside the installation base, in preferred embodiments it is possible to achieve a reliable and mechanically durable construction.

[0016] With the aid of the embodiments, it is also possible to reduce the number of the problems that appear in the prior art, which are caused by the feed-throughs relating to connecting the components. This is because in the embodiments, in which there is no need at all to make feed-throughs, the components being instead connected, already in the installation stage, to the conductor membrane, from which the conductors leading to the components of the electronic module are made.

[0017] In the embodiments, the components, of which there may be one or several, are installed on their installation base, such as a circuit board,

during the manufacture of the base, so that the base structure, is as it were, manufactured around the component. The components become embedded and attached as desired to this base structure.

[0018] In the embodiments, it is thus possible to manufacture a circuit board, inside which components are embedded. There are also embodiments, with the aid of which a small and reliable component package can be manufactured around a component, as part of the circuit board. In such embodiments, the manufacturing process is simpler and cheaper than manufacturing methods in which separate cased components are installed and connected to the surface of the circuit board. The manufacturing method can also be applied to use the method to manufacture Reel-to-Reel products. Thin and cheap circuit-board products containing components can be made by using the methods according to the preferred embodiments.

[0019] There are also many other preferred embodiments, which can be used to obtain significant additional advantages. With the aid of such embodiments, a component's packaging stage, the circuit board's manufacturing stage, and the assembly and connecting stage of the components, for example, can be combined to form a single totality. The combination of the separate process stages brings significant logistical advantages and permits the manufacture of small and reliable electronic modules. A further additional advantage is that such an electronic-module manufacturing method can mostly utilize known circuit-board manufacturing and assembly technologies.

[0020] The composite process according to the embodiment referred to above is, as a totality, simpler than manufacturing a circuit board and attaching a component to the circuit board using, for example, the flip-chip technique. By using such preferred embodiments, the following advantages are obtained, compared to other manufacturing methods:

[0021] Soldering is not needed in the connections of the components, instead an electrical connection between the connection zones on the surface of the component and the metal membrane of the installation base is created, for example, by ultrasonic welding, thermo-compression, or some other such method, in which the temperatures required to achieve electrical connections, though high, are of short duration and local, and in which high temperatures are not required over a wide area. This means that the connection of a component does not need metal being maintained molten for a long time with its associated high temperature. Thus, the construction is made more reliable than soldered connections. Particularly in small connections, the brittleness of the metal alloys create large problems. In a solderless solution according to a preferred embodiment, it is possible to achieve clearly smaller constructions than in soldered solutions. The manufacturing method can even be designed so that, during the connection process of a component, heat is brought only to the area of the connection, so that the areas most strongly heated are the connection zone of the component and the area to which the component is connected. Elsewhere in the structure the temperature remains low. This gives greater freedom of choice when selecting the materials of the installation base and the components. If ultrasonic welding is used as the connection method, higher temperatures may only be required to harden the fillers used. Polymer membranes, which are hardened other than through the effect of heat, for example, chemically or with the aid of electromagnetic radiation, such as UV light, can also be used in the method. In such a preferred embodiment of the invention, the temperature of the installation base and components can be kept very low during the entire process, for example, at less than 100 °C.

[0022] As smaller structures can be manufactured using the method, the components can be placed closer together. Thus, the conductors between the components also become shorter and the characteristics of the electronic circuits improve. For example, losses, interferences, and transit-time delays can be significantly reduced.

[0023] The method permits a lead-free manufacturing process, which is environmentally friendly.

[0024] When using a solderless manufacturing process, fewer undesirable intermetallics also arise, thus improving the long-term reliability of the construction.

[0025] The method also permits three-dimensional structures to be manufactured, as the installation bases and the components embedded in them can be stacked on top of each other.

[0026] There are also other preferred embodiments. For instance, flexible circuit boards can be used in connection with the embodiments. Further, in embodiments, in which the temperature of the installation base can be kept low during the entire process, organic manufacturing materials can be used comprehensively.

[0027] With the aid of the embodiments, it is also possible to manufacture extremely thin structures, in which, despite the thinness of the structure, the components are entirely protected inside their installation base, such as a circuit board.

[0028] In embodiments, in which the components are located entirely inside the installation base, the connections between the circuit board and the components will be mechanically durable and reliable.

[0029] The embodiments also permit the design of electronic-module manufacturing processes requiring relatively few process stages. Embodiments with fewer process stages correspondingly also require fewer process devices and various manufacturing methods. With the aid of such embodiments, it is also possible in many cases to cut manufacturing costs compared to more complicated processes.

[0030] The number of conductive-pattern layers of the electronic module can also be chosen according to the embodiment. For example, there can be one or two conductive-pattern layers. Additional conductive-pattern layers can be manufactured on top of these, in the manner known in the circuit-board industry. A total module can thus incorporate, for example, three, four, or five conductive-pattern layers. The very simplest embodiments have only one conductive-pattern layer and indeed one conductor layer. In some embodiments, each of the conductor layers contained in the electronic module can be exploited when forming conductive patterns.

[0031] In embodiments, in which the conductor layer connected to a component is patterned only after the connection of the component, the conductor layer can include conductor patterns even at the location of the component. A corresponding advantage can also be achieved in embodiments, in which the electronic module is equipped with a second conductive-pattern layer, which is located on the opposite surface of the base material of the module (on the opposite surface of the insulation material layer relative to the conductive-pattern layer connected to the component). The second conductor layer can thus also include conductive patterns at the location of the component. The placing of conductive patterns in the conductor layers at the location of the component will permit a more efficient use of space in the module and a denser structure.

[0032] Further scope of applicability of the present invention will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The present invention will become more fully understood from the detailed description given hereinbelow and the accompanying drawings, which are given by way of illustration only, and thus are not limitative of the present invention, and wherein:

[0034] Figures 1 - 8 show a series of cross-sections of some examples of manufacturing methods by means of which it is possible to manufacture an electronic module according to an embodiment of the invention, and schematic cross-sectional diagrams of some electronic modules according to embodiments of the invention.

[0035] Figure 9 shows a cross-sectional view of an electronic module according to an embodiment of the invention, which includes several installation bases on top of each other.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0036] In the methods of the examples, manufacturing starts from an installation base 1 of an insulating substance, which is thicker than the components 6 that are later to be connected to the base. Of course, the method can also be applied in such a way that the installation base 1 and the component 6 are equally thick. In some embodiments, it is also possible to use components 6 that are thicker than the installation base 1. Using a suitable method, through-cavities 2, selected to suit the size of the components 6 to be installed, are made in the insulating material layer 1. The alignment of the components 6 also requires suitable alignment marks, to creation of which several different methods are available. One possible method is to make small through-holes 3 near to the installation cavities 2 of the components 6. The precise alignment of the component preferably requires at least two through-holes. An unpatterned metal film 4, which acts as the conducting surface of the installation base for the

components 6 to be installed and connected, is made on the first surface 1a of the insulating substance layer 1. The metal film 4 can be manufactured, for example, by laminating copper (Cu). The metal film 4 can also be a surfaced metal film, or some other film including several layers or several materials. In some embodiments, for example, a copper film surfaced with a layer of tin or gold can be used. In these embodiments, the surfacing is typically made on the side of the insulating material layer 1. Another possible procedure is for the metal film 4 to include surfacing only in the area of the installation cavities 2.

[0037] The components 6 are aligned with their installation cavities 2 with the aid of the alignment holes 3, or some other alignment marks and the connection zones or contact protrusions 7 on the surface of the components 6 are connected to the metal film 4. The connecting can take place, for example, using the ultrasonic or thermo-compression methods.

[0038] The ultrasonic method then refers to a method, in which two pieces containing metal are pressed against each other while vibration energy at an ultrasound frequency is brought to the area of the joint. Due to the effect of the ultrasound and the pressure created between the surfaces to be joined, the pieces to be joined are bonded metallurgically. Methods and equipment for ultrasonic bonding are commercially available. Ultrasonic bonding has the advantage that a high temperature is not required to form a bond.

[0039] The terms metal layer, metal film, metal contact bump, metal contact zone, and in general a metal item, refer to the fact that the manufacturing material of the item contains enough of at least one metal for the item to form a metallurgical bond with another item. The item can naturally also include several metals as layers, accumulations, zones, or metal alloys. Possible metals include particularly copper, aluminium, gold, and tin.

[0040] The term thermo-compression method refers in turn to a method, in which two pieces containing metal are pressed against each other while thermal energy is brought to the area of the joint. The effect of the thermal energy and the pressure created between the surfaces to be joined cause the pieces to be joined to be bonded metallurgically. Methods and equipment for thermo-compression bonding are also commercially available.

[0041] In some embodiments, contact bumps 5, to which the connection zones or contact protrusions 7 of the components 6 are connected, are made on top of the conductive film 4. In such a method, the contact bumps 5 can also be used to align the components 6 during the components' installation stage. The components 6 can, of course, be aligned with the aid of other alignment marks, for example, the alignment holes 3, if such are made in the process being used. In embodiments using contact bumps 5, the procedure can otherwise correspond to embodiments in which contact bumps 5 are not used. The use of contact bumps 5 is justified, for example, if the material of the components' 6 contact zones or contact protrusions 7 is not directly suitable for connection to the selected material of the conducting layer 4. In that case, the material of the contact bumps 5 is selected to permit a bond using the bumps 5 to be created. In such embodiments, the contact bumps 5 are thus intended to match two different conductor materials to each other. For this purpose, the contact bump 5 can also be manufactured as a layered structure, containing two or more layers of possibly differing materials.

[0042] After the connection of the components 6, the space remaining in the installation cavity 2 around the component 6 is filled with a suitable filler 8, usually some kind of polymer filler. The filling is intended to secure the component 6 mechanically to the insulating material layer 1, thus achieving a mechanically more durable construction. The filler material 8 also supports the conductive patterns 14 to be formed later from the conducting layer 4 and protects the component and the bond

between the component 6 and the conducting layer 4 during the formation of the conductive patterns 14. In principle, the securing of the component 6 is not, however, an essential operation, especially in embodiments, in which mechanical durability or a long life are not demanded of the structure.

[0043] If desired, a conductive film 9, from which conductive patterns 19 can be formed later, can also be made on the second surface 1b of the insulating material layer 1. The conductive film 9 can be manufactured in a manner corresponding to that of the conductive film 4 made of the first surface 1a of the base. The manufacture of a second conductive film 9 is not, however, necessary in simple embodiments and when manufacturing simple electronic modules. A second conductive film 9 can, however, be exploited in many ways, such as additional space for conductive patterns and to protect the components 6 and the entire module against electromagnetic radiation (EMC shielding). With the aid of a second conductive film 9 the structure can be reinforced and warping of the installation base, for example, can be reduced.

[0044] The manufacturing processes according to the examples can be implemented using manufacturing methods, which are generally known to those versed in the art of manufacturing circuit boards.

[0045] In the following, the stages of the method shown in Figures 1 - 8 are examined in greater detail.

Stage A (Figure 1):

[0046] In stage A, a suitable sheet 1 of insulating-material board, from which the body of the installation base is formed, is selected for the manufacturing process of the electronic module. The insulating-material layer 1 should preferably be thicker than the component to be installed. The component can then be embedded entirely inside the installation base

while the electronic module will be even on both surfaces. Of course, thicker special components can also be embedded into the installation base, their rear surface protruding outside the second surface 1b of the insulating-material layer 1. This can be done particularly if it is not intended to stack a second electronic module on top of the electronic module being manufactured. In terms of the durability of the construction, however, it would be preferable for the components to be embedded entirely inside the installation base.

[0047] The insulating-material layer 1 can be, for example, a polymer base, such as a glass-fibre reinforced epoxy sheet FR4. In embodiments in which high temperatures are not needed in the manufacturing process, the installation base 1 can also be a cheap and flexible organic sheet. Other examples of suitable materials for the insulating-material layer 1 are PI (polyimide), FR5, aramide, polytetrafluoroethylene, Teflon®, and LCP (liquid crystal polymer).

Stage B (Figure 2):

[0048] In stage B, through-cavities 2 of a suitable size and shape for the components to be embedded in the sheet are made in the insulating-material layer 1. The cavities 2 can be made suitably, for example, using some known method used in circuit-board manufacture. The cavities 2 can be made, for example, mechanically by milling, impact, drilling, or with the aid of a laser. The cavities 2 extend through the entire insulating-material layer 1, from its first surface 1a to its second surface 1b. If several of the cavities 2 are made, they are positioned relative to each other within the highest limits of accuracy possible for the manufacturing method being used.

Stage C (Figures 3A and 3B):

[0049] The example series of figures shows two alternative stage Cs. According to a modification of the example process A (Figure 3A), in stage C a thin conductive film 4, or more generally a conducting layer 4 is attached to the second surface 1b of the insulating-material layer 1. The conductive film 4 is typically a metal film 4. In several embodiments, a suitable metal film is a copper (Cu) film, though other metals and also metal alloys can very well be used. The copper film can be attached to the insulating-material layer 1, for example, by lamination. An adhesive layer, which is spread on the surface of the insulating-material layer 1 or of the conductive film 4 prior to laminating the conductive film 4, can be used to aid the attachment of the conductive film 4. In the example processes, patterns have not yet been made in the conductive film 4 at this stage, so that there is no need to particularly align the film 4 relative to the insulating-material layer 1. During, or after the attaching of the conductive film 4, through-holes 3, which can be used later to align the components in the component installation stage, can also be made in the installation base. However, it is not essential to make through-holes 3, as instead other suitable alignment marks can be used to align the components. If through-holes 3 are made, it would be best for there to be at least two of them in the installation base. It is also possible to proceed so that two through-holes 3 are made for each component to be installed. In the embodiment shown in the figures, the through-holes 3 used to align the components extend through both the insulating-material layer 1 and the conductive film 4. This has the advantage that the same alignment marks (the through-holes 3) can be used for alignment on both sides of the installation base.

[0050] In stage C of the B modification of the example process (Figure 3B), the procedure is mainly the same as is the A modification, except that, in addition to the stages shown in the A modification, in the B modification contact bumps 5 are made on the surface of the conductive film 4. The contact bumps 5 can be made in the conductive film 4 prior to

the attachment of the conductive film 4 to the insulating material layer 1. The contact bumps 5 are then aligned relative to each other, while in the attachment stage of the conductive film 4 the conductive film 4, together with the contact bumps, is aligned relative to the insulating-material layer 1 and particularly to the installation cavities 2 made in the insulating-material layer 1. A second alternative is to first attach the conductive film 4 to the insulating-material layer 1 and after this make the contact bumps 5 on the bottom of the installation cavities 2. The contact bumps 5 are intended to connect a component to be installed later to the conductive film 4. In the example process, the contact bumps 5 are manufactured from some metallurgically compatible material, such as gold (Au). The contact bumps can be made using some process generally known in the circuit-board industry. If through-holes 3 are used in the process for alignment, they can be made in the same stage. The through-holes 3 can also be made after making the contact bumps 5, in which case they should be aligned as accurately as possible relative to the contact bumps 5, or else prior to manufacturing the contact bumps 5, in which case the contact bumps 5 are aligned relative to the through-holes 3.

Stage D (Figures 4A, 4B, and 4C):

[0051] Three modifications of Stage D are shown. In the A modification (Figure 4A), a component 6, which includes contact bumps 7 in the connection zones of the component, is connected to the installation base. The contact bumps 7 of the component are connected to the conductive layer 4, so that an electrical contact is formed between the contact bump 7 and the conductive layer 4. It would be good for the connection to also withstand mechanical stress, so that the connection will not be easily broken in later process stages, or during the operation of the electronic module. The connection is formed using a suitable connection method, for example, the ultrasonic and thermo-compression methods. In the connection stage, the through-holes 3 made for alignment, or other available alignment marks are used to align the component 6.

[0052] In the B modification (Figure 4B) too, a component 6, which includes contact bumps 7 in the connection zones of the component, is connected to the installation base. The difference to the A modification is that, in the B modification, contact bumps 5 are also formed on top of the conductive layer 4. The contact bumps 7 of the component are then connected to the contact bumps 5 of the installation base. The connection can, as in modification A, be formed using a suitable connection method, for example, the ultrasonic or thermo-compression methods. In the B modification, the component can be aligned, according to the embodiment, using the contact bumps 5, the through-holes 3, or other alignment marks suitable for alignment.

[0053] In the C modification of the example process, as in the B modification, an installation base is used, in which contact bumps 5 are made on top of the conductor layer 4. Unlike in the A and B modifications, in the C modification a component 6 is used, the surface of which has flat contact zones, but no actual contact bumps 7, or other corresponding contact protrusions. In the C modification, connection and alignment are carried out as in the B modification, except that the connection is formed between the conductive material of the contact zones and the contact bumps 5 of the installation base.

Stage E (Figures 5A, 5B, and 5C):

[0054] In stage E, the space remaining between the component 6 and the installation base is completely filled with a filler 8, which is, for example, some suitable polymer. For example, epoxy filled with suitable particles can be used as the polymer. The polymer can be spread using, for example, some known vacuum-paste-pressing device suitable for the task. Figures 5A, 5B, and 5C show the installation base after the attachment of a component, in A, B, and correspondingly C modifications of the process. The purpose of the filler 8 is to secure the component 6 mechanically to the insulating-material layer 1, so that the electronic

module will better withstand mechanical stress. In addition, the filler 8 protects the component 6 during later process stages. Protecting the component 6 can be particularly beneficial in embodiments, in which conductive patterns are formed by etching the conductive layer 4 and in which the surface of the component 6 is sensitive to the effect of the etching agent used. Otherwise, the filling of the installation cavity 2 is in no way essential and, at least in some embodiments, stage E can be omitted or performed at a later stage in the process.

[0055] In some embodiments, the installation cavity 2 can be dimensioned to the size of the component 6, so that a friction fit is created between the component and the installation cavity 2, filler 8 then not being necessarily required. Such an embodiment is, however more challenging in terms of the manufacturing technology while the final result remains mechanically weaker than in the embodiments shown in Figures 5A, 5B, and 5C.

[0056] In embodiments, in which conductive patterns are formed on the second surface 1b of the insulating layer 1, the manufacture of the conductive patterns can be facilitated by evening the second surface 1b of the insulating layer 1, with the aid of a filler 8.

Stage F (Figures 6A, 6B, and 6C):

[0057] Figures 6A, 6B, and 6C show the electronic module after the carrying out of stage F, in modifications A, B, and C of the process, respectively. Stage F itself is, however, performed in the same way in each of these modifications. In stage F, conductive patterns 14 are formed from the conductive layer 4 using some suitable method. The conductive patterns 14 can be made, for instance, by removing the conductive material of the conductive layer 4 from outside of the conductive patterns. The conductive material can be removed, for example, using one of the selective etching methods that are widely used and well known in the

circuit-board industry. If the conductive layer 4 is made from a special material, the conductive patterns 14 can also be formed in such a way that the conductivity of the conductive material 4 is removed from outside of the conductive patterns, for example, with the aid of electromagnetic radiation. When using a conversely reactive material, the material is put into a conductive state in the area of the conductive patterns. Thus, the conductive layer 4 is, in the previous stages of the method, actually the insulating layer, which can be converted to be conductive with the aid of special treatment. The manner of forming the conductive patterns 14 is thus not, as such, essential to the manufacture of the electronic module.

[0058] The conductive patterns are aligned with the aid of alignment marks made in the installation base. The alignment marks can be the same that are used to align the components, or else separate alignment marks, which are made at a specific location relative to the alignment marks used in the alignment of the components. Because the components and conductive patterns are both aligned relative to the alignment marks on the installation base, they are thus also aligned relative to each other.

[0059] If through-holes 3 are made in the embodiment, the conductive patterns to be made can be aligned with the aid of the through-holes 3.

[0060] After stage F, the electronic module includes a component 6, or several components 6 and conductive patterns 14, with the aid of which the component or components 6 can be connected to an external circuit, or to each other. The conditions for manufacturing a functional totality then exist already. The process can thus be designed in such a way that the electronic module is already finished after stage F and Figures 6A, 6B, and 6C show examples of some possible electronic modules that can be manufactured using the example methods. Of course, if it is wished, the process can also continue after stage F, for example, by making conductive patterns on the second surface 1b of the insulating layer 1, or by surfacing the electronic module with a protective substance.

Stage G (Figures 7A, 7B, and 7C):

[0061] Figures 7A, 7B, and 7C show embodiments of the manufacturing process as A, B, and C modifications, in which, after stage E, a conductive layer 9 is formed on the second surface 1b of the insulating layer 1. In the embodiments shown in Figures 7A, 7B, and 7C, stage F is thus omitted, the method moving to stage G directly from stage E.

[0062] Stage G corresponds to stage C, in which a conductive layer 4 is made on the first surface 1a of the insulating layer 1. As in stage C, the conductive layer 9 can be made, for example, by laminating, on the second surface 1b of the insulating layer 1, a type of electrically-conductive film 9 corresponding to the one on the first surface 1a. The lamination can exploit an adhesive spread on the surface of the base or film, and which during the lamination stage attaches the installation base and the electrically-conductive film to each other.

Stage H (Figures 8A, 8B, and 8C):

[0063] Stage H can be carried out after stage G, if it is wished to pattern the conductive layer 9 formed on the second surface 1b of the insulating layer 1. Stage H corresponds to stage F, with the difference that, in stage H, in addition to the conductive patterns 14, other conductive patterns 19 are formed from the conductive layer 9 made on the second surface 1b of the insulating layer 1. After carrying out stage H, the electronic module will include conductive patterns on both surfaces of the insulating-material layer 1. The second conductive-pattern layer will provide more diverse connection possibilities between the components 6. Figures 8A, 8B, and 8C show the electronic module after the carrying out of stage H, respectively in A, B, and C modifications of the process. Stage F itself is, however, carried out in the same way in each of these modifications.

[0064] After stage H, the electronic module includes a component 6, or several components 6 and conductive patterns 14 and 19. The examples of Figures 8A, 8B, and 8C show some possible electronic modules that can be manufactured using the example methods. If desired, the process can continue after stage H, for example, by making a feed-through, or feed-throughs, with the aid of which suitable points in the conductive pattern 14 can be connected electrically to suitable parts of the conductive pattern 19. The electronic module can also be surfaced with a protective substance.

Figure 9

[0065] Figure 9 shows a multi-layered electronic module, which includes three installation bases 1 laminated on top of each other, together with their components 6, and a total of six conductive-pattern layers 14 and 19. The installation bases 1 are attached to each other with the aid of intermediate layers 32. The intermediate layer 32 can be, for example, a pre-preg epoxy layer, which is laminated between the installation bases 1. After this, holes running through the module are drilled in the electronic module, in order to form contacts. The contacts are formed with the aid of a conductive layer 31 grown in the holes. With the aid of the conducts 31 running through the electronic module, the various conductive-pattern layers 14 and 19 of the installation bases 1 can be suitably connected to each other, thus forming a multi-layered functioning totality.

[0066] On the basis of the example of Figure 9, it is clear that the method can also be used to manufacture many different kinds of three-dimensional circuit structures. The method can be used, for example, in such a way that several memory circuits are placed on top of each other, thus forming a package containing several memory circuits, in which the memory circuits are connected to each other to form a single functional totality. Such packages can be termed three-dimensional multichip

modules. In modules of this kind, the chips can be selected freely and the contacts between the various chips can be easily manufactured according to the selected circuits.

[0067] The sub-modules (installation bases 1 with their components 6 and conductors 14 and 19) of a multi-layered electronic module can be manufactured, for example, using one of the electronic-module manufacturing methods described above. Some of the sub-modules to be connection to the layered construction can, of course, be quite as easily manufactured using some other method suitable for the purpose.

[0068] The examples of Figures 1 - 9 show some possible processes, with the aid of which embodiments of our invention can be exploited. Our invention is not, however, restricted to only the processes disclosed above, but instead the invention also encompasses various other processes and their end products, taking into account the full scope of the Claims and the interpretation of their equivalences. The invention is also not restricted to only the constructions and methods described by the examples, instead it is obvious to one versed in the art that various applications of our invention can be used to manufacture a wide range of different electronic modules and circuit boards differing greatly from the examples described above. Thus, the components and wiring of the figures are shown only with the intention of illustrating the manufacturing process. Thus, many alterations to and deviations from the processes of the examples shown above can be made, while nevertheless remaining within the basic idea according to the invention. The alterations can relate, for example, to the manufacturing techniques described in the different stages, or to the mutual sequence of the process stages.

[0069] With the aid of the method, it is also possible to manufacture component packages for connection to a circuit board. Such packages can also include several components that are connected electrically to each other.

[0070] The method can also be used to manufacture total electrical modules. The module can also be a circuit board, to the outer surface of which components can be attached, in the same way as to a conventional circuit board.

[0071] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims:

1. An electronic module, comprising:
 - a first conductive-pattern layer having a first surface,
 - contact bumps made on the first surface of the first conductive-pattern layer,
 - a component having flat contact zones, and
 - an insulating-material layer on the first surface of the first conductive-pattern layer,wherein the component is embedded in the insulating-material layer and the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.
2. The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer, and the electronic module comprises a second conductive-pattern layer on the second surface of the insulating-material layer.
3. The electronic module of claim 1, wherein the contact bumps include a layered structure, containing at least two layers of at least two different materials.
4. The electronic module of claim 1, wherein the component is a microcircuit.
5. The electronic module of claim 1, wherein the component is entirely protected inside the insulating-material layer.
6. The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer, and the electronic module comprises a conductive film on the second surface of the insulating-material layer for protecting the component against electromagnetic radiation.

7. The electronic module of claim 1, comprising a plurality of components having flat contact zones metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.
8. The electronic module of claim 7, wherein the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.
9. The electronic module of claim 1, wherein the insulating-material layer is a glass-fibre reinforced epoxy sheet
10. The electronic module of claim 1, wherein the insulating-material layer is a flexible organic sheet.
11. An electronic module, comprising:
 - a first conductive-pattern layer having a first surface,
 - a second conductive-pattern layer having a second surface,
 - an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,
 - contact bumps made on the first surface of the first conductive-pattern layer,
 - a component having flat contact zones embedded in the insulating-material layer such that the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.
12. The electronic module of claim 11, wherein the contact bumps include a layered structure, containing at least two layers of at least two different materials.
13. The electronic module of claim 12, wherein the component is a microcircuit.

14. The electronic module of claim 11, wherein the conductive-pattern layer is configured to protect the component against electromagnetic radiation.
15. The electronic module of claim 11, comprising a plurality of components having flat contact zones metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.
16. The electronic module of claim 15, wherein the plurality of components includes at least one microcircuit, and the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.
17. A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:
- a first conductive-pattern layer having a first surface,
 - contact bumps made on the first surface of the first conductive-pattern layer,
 - an insulating-material layer on the first surface of the first conductive-pattern layer,
 - and
 - a component embedded in the insulating-material layer, the component having flat contact zones metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.
18. A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein each of said modules comprises:
- a first conductive-pattern layer having a first surface,
 - contact bumps made on the first surface of the first conductive-pattern layer,
 - an insulating-material layer on the first surface of the first conductive-pattern layer,
 - and

a component embedded in the insulating-material layer, the component having flat contact zones metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

19. A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:

a first conductive-pattern layer having a first surface,

a second conductive-pattern layer having a second surface,

an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,

contact bumps made on the first surface of the first conductive-pattern layer,

a component having flat contact zones embedded in the insulating-material layer such that the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer

20. The multi-layered electronic module according to one of the claim 17, comprising a plurality of memory circuits.

21. The multi-layered electronic module according to one of the claim 17, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

22. The multi-layered electronic module according to one of the claim 18, comprising a plurality of memory circuits.

23. The multi-layered electronic module according to one of the claim 19, comprising a plurality of memory circuits.

24. The multi-layered electronic module according to one of the claim 18, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

25. The multi-layered electronic module according to one of the claim 19, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

Abstract:

An electronic module in which an installation base is used, which includes an insulating-material layer (1) and a conductive layer on the surface of the insulating-material layer. The conductive layer also covers the installation cavity of a component (6). The component (6) is set in the installation cavity, in such a way that the contact zones face towards the conductive layer and electrical contacts are formed between the contact zones of the component (6) and the conductive layer. After this, conductive patterns (14) are formed from the conductive layer, to which the component (6) is attached.

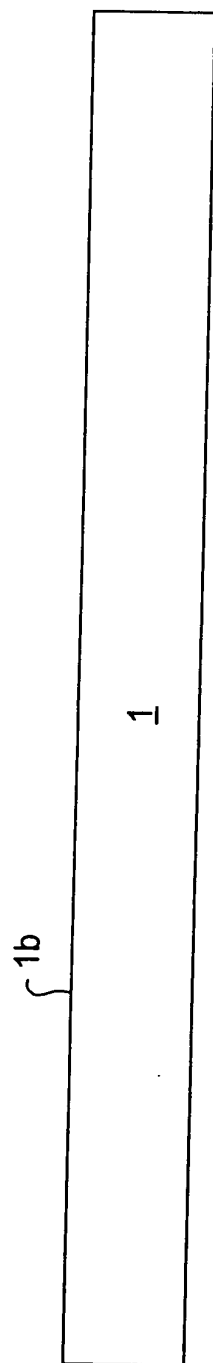


Fig. 1

1/8

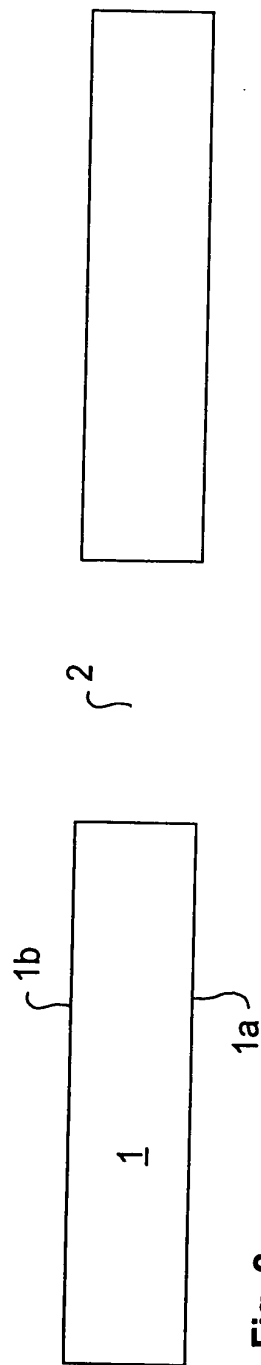


Fig. 2

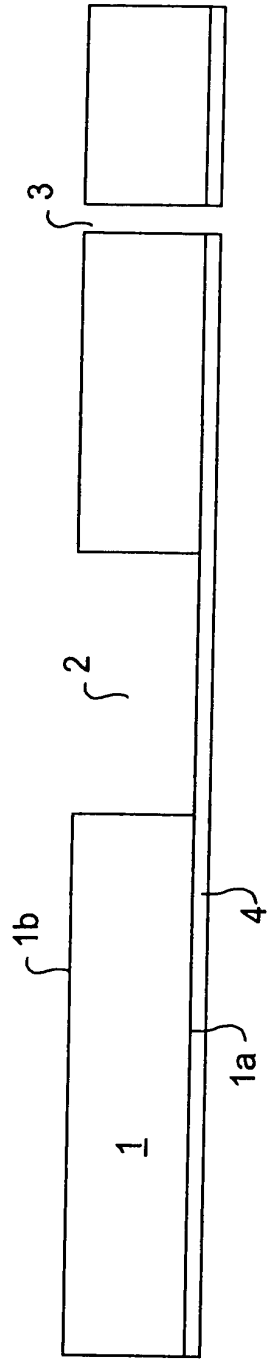


Fig. 3A

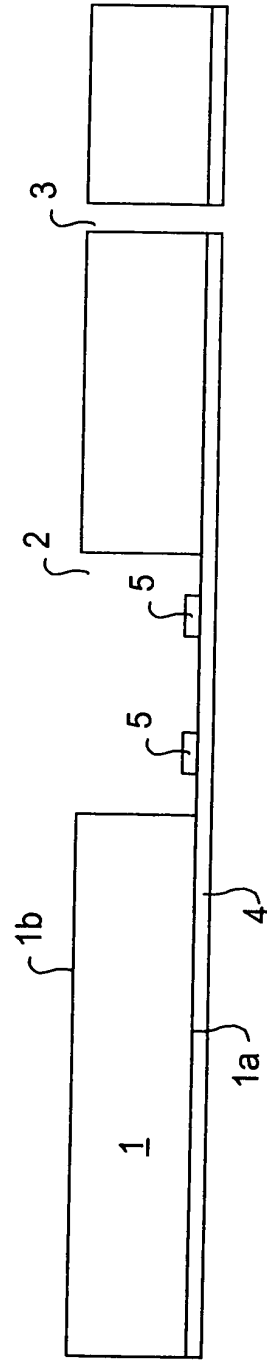


Fig. 3B

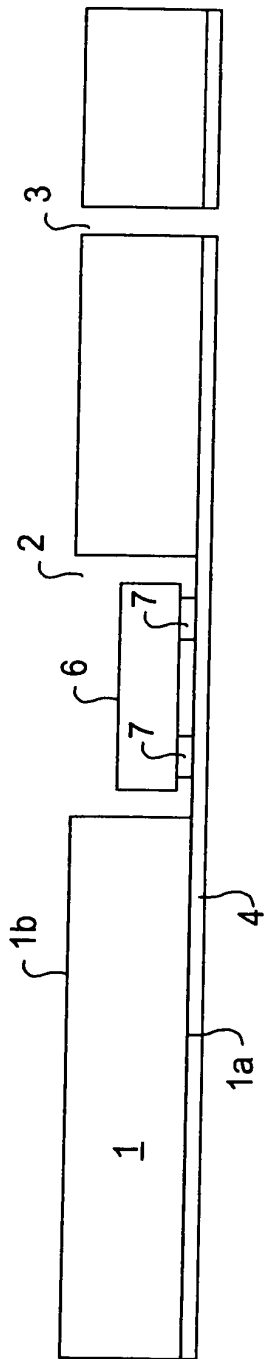


Fig. 4A

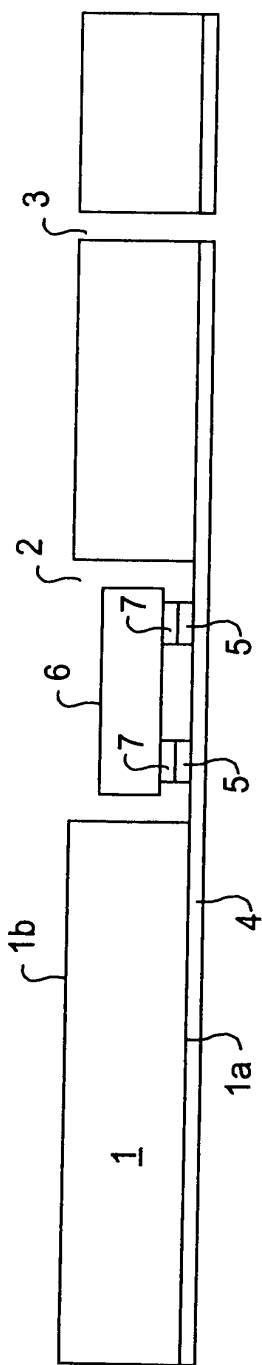


Fig. 4B

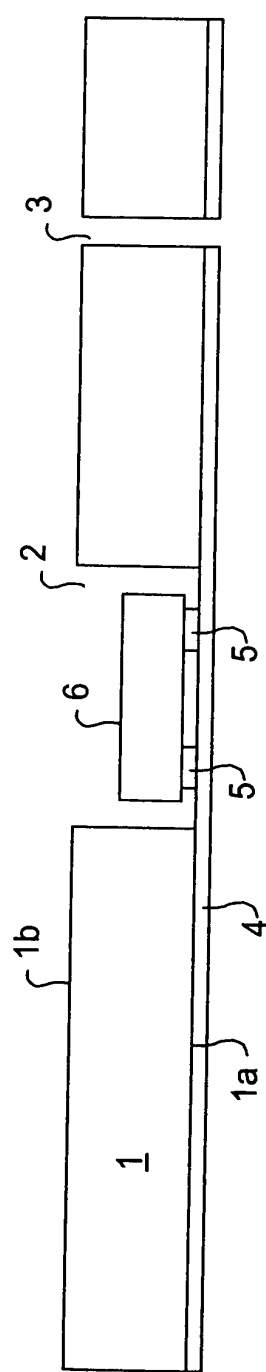


Fig. 4C

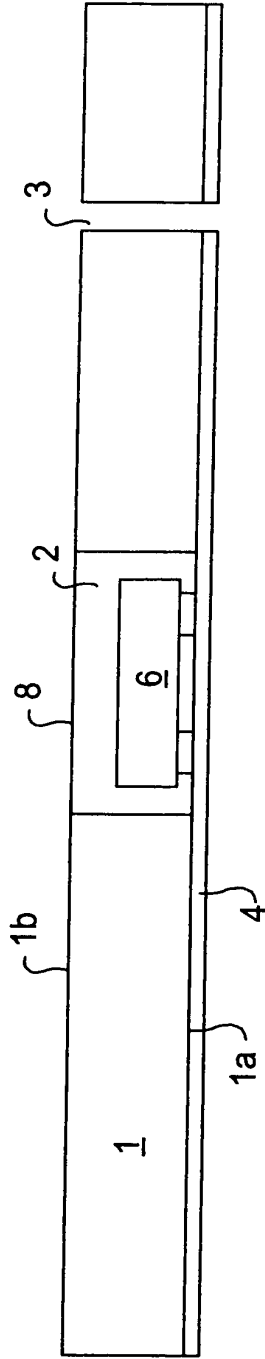


Fig. 5A

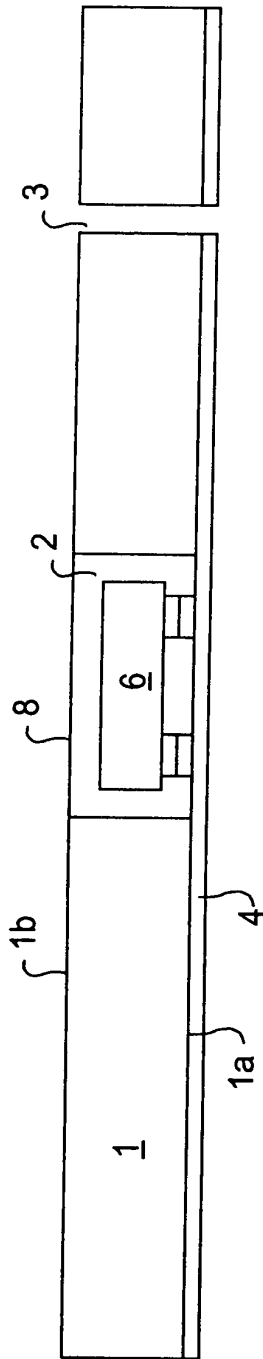


Fig. 5B

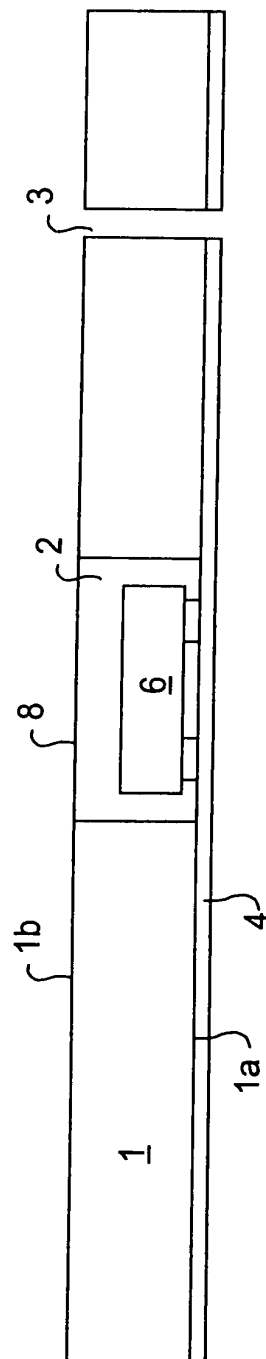


Fig. 5C

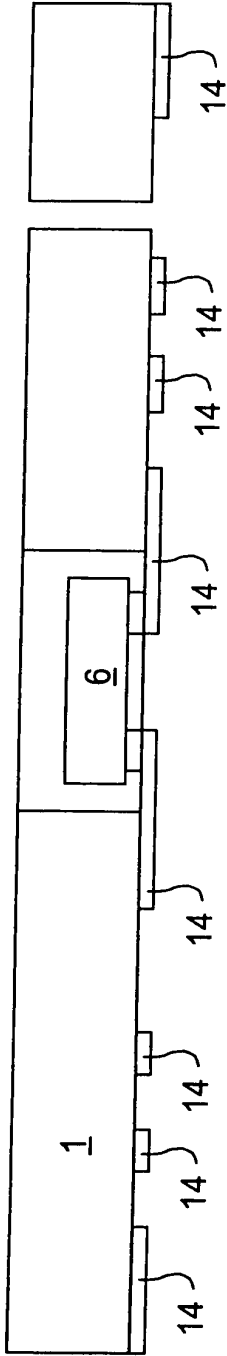


Fig. 6A

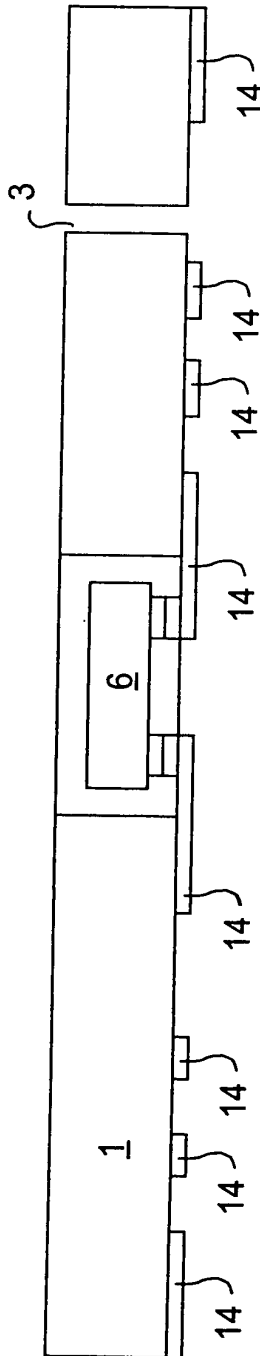


Fig. 6B

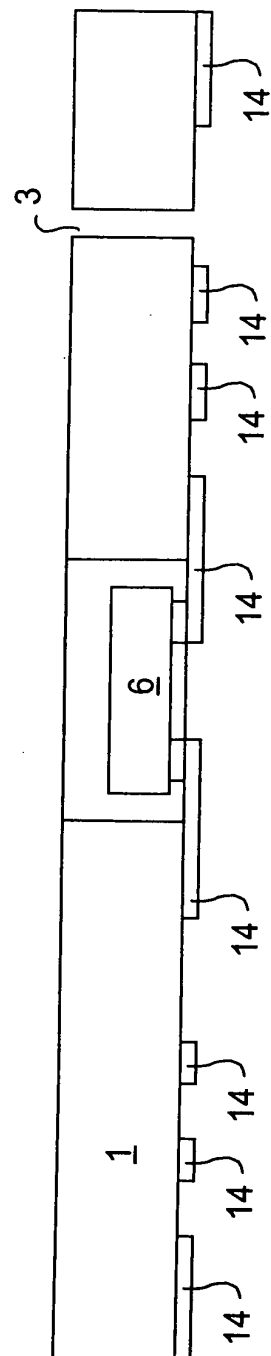


Fig. 6C

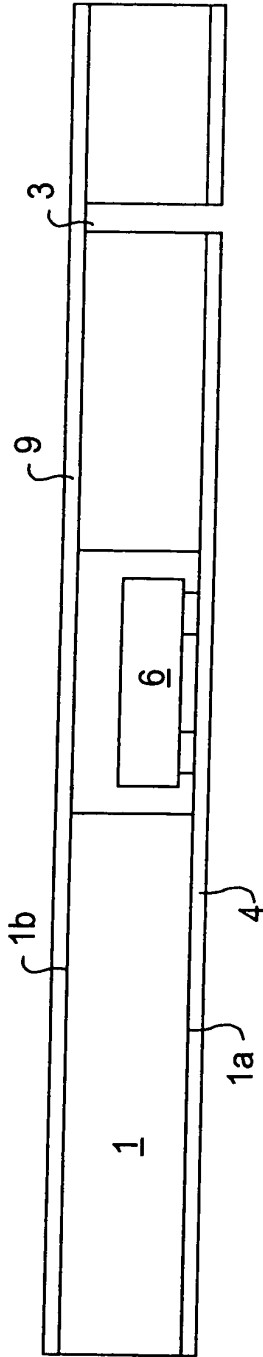


Fig. 7A

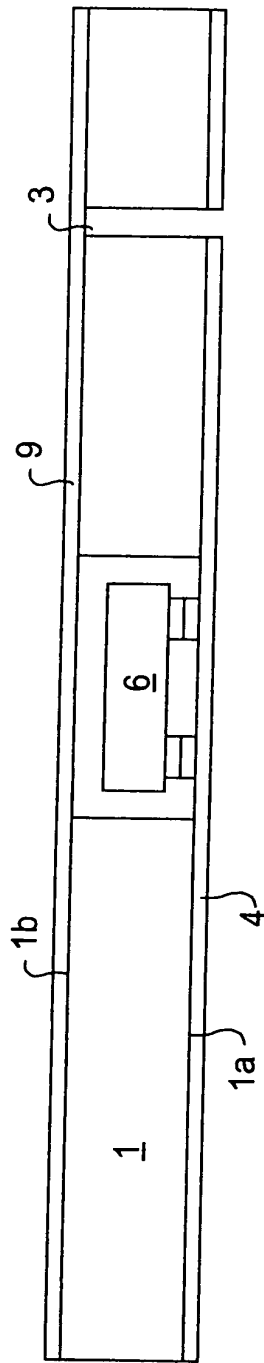


Fig. 7B

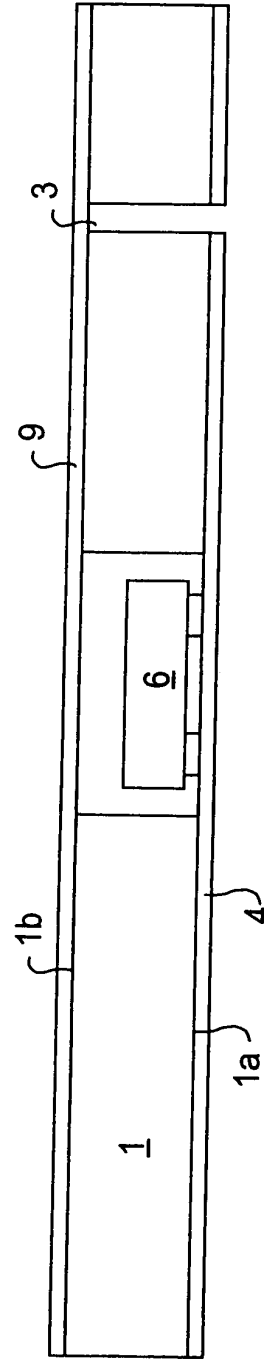


Fig. 7C

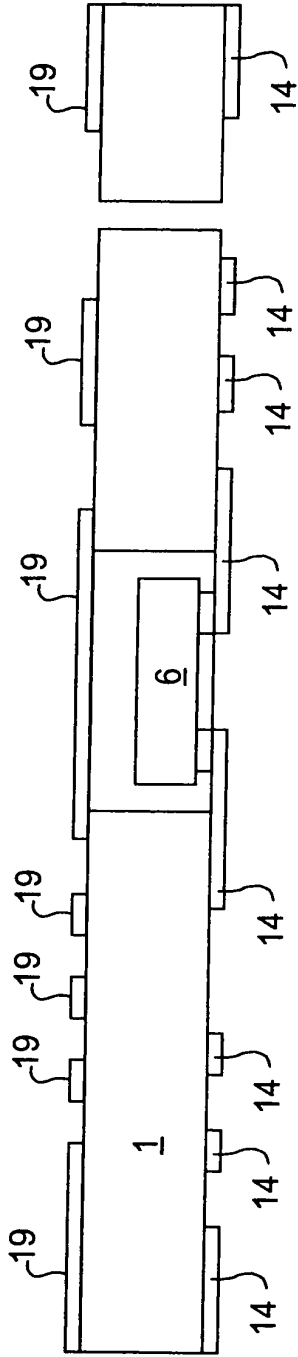


Fig. 8A

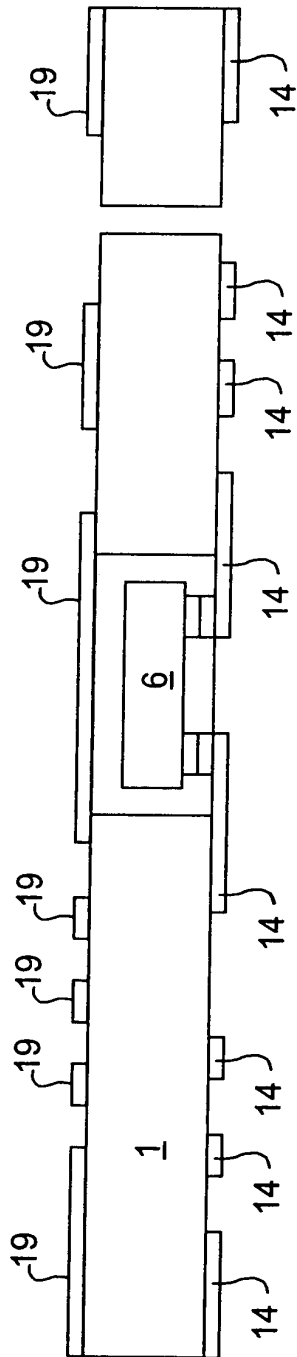


Fig. 8B

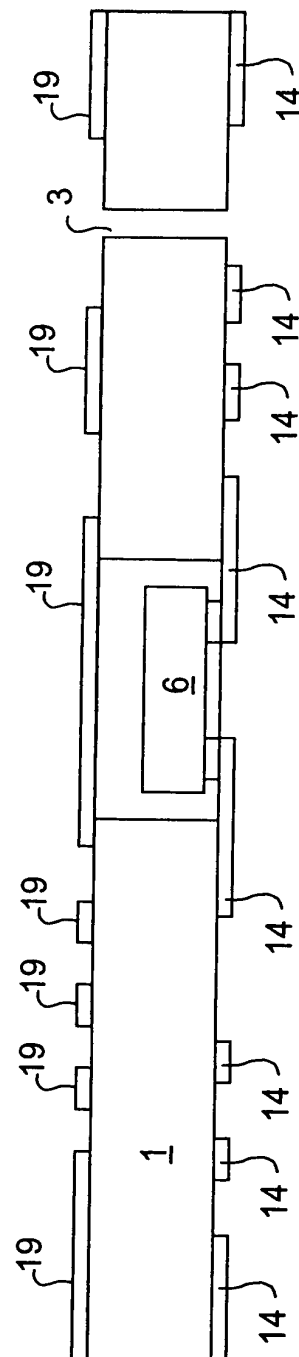


Fig. 8C

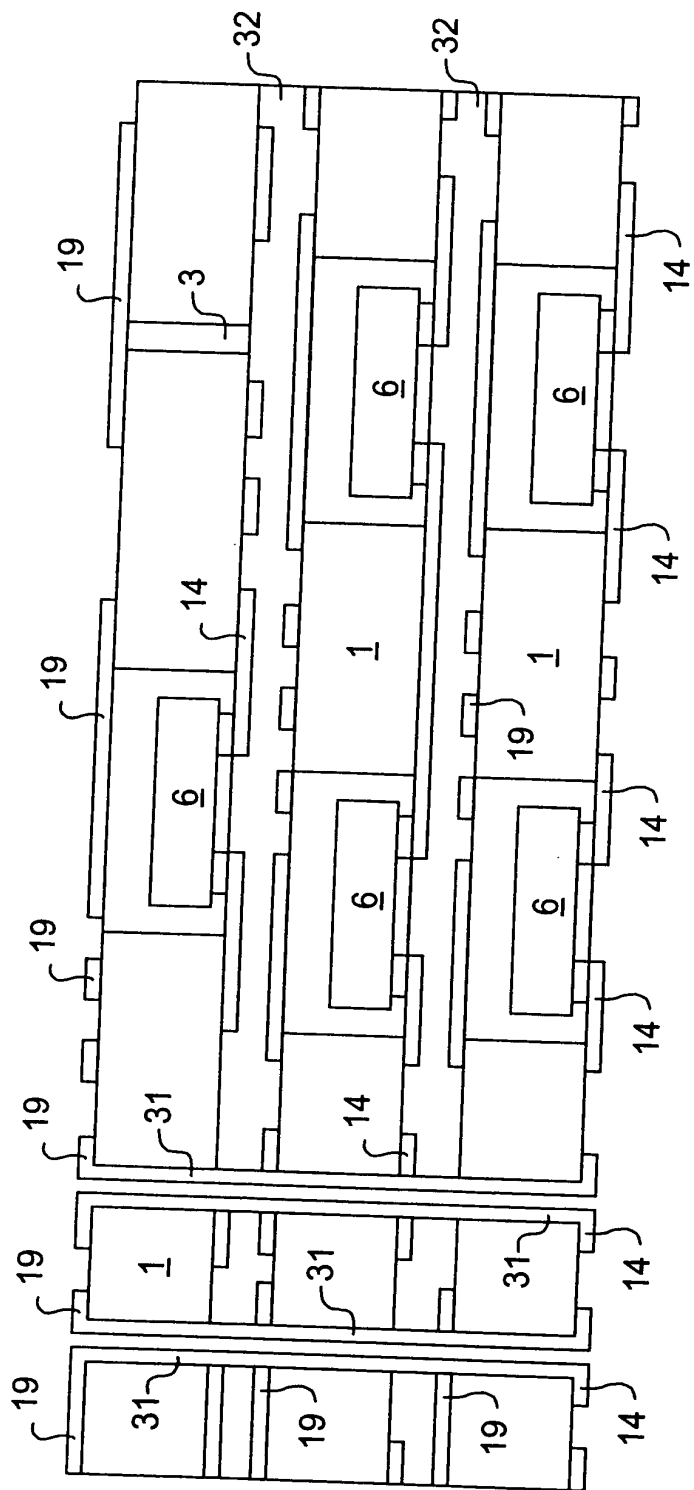


Fig. 9

BIRCH, STEWART, KOLASCH & BIRCH, LLPP.O. Box 747 • Falls Church, Virginia 22040-0747
Telephone: (703) 205-8000 • Facsimile: (703) 205-8050PLEASE NOTE:
YOU MUST
COMPLETE THE
FOLLOWING**COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT AND DESIGN APPLICATIONS**

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one inventor is named below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Insert Title:

METHOD FOR MANUFACTURING AN ELECTRONIC MODULE

Fill in Appropriate
Information -
For Use Without
Specification
Attached:

the specification of which is attached hereto. If not attached hereto,

the specification was filed on _____ as
United States Application Number _____;
and amended on _____ (if applicable) and/or
the specification was filed on February 25, 2004 as PCT
International Application Number PCT/FI2004/000101; and was
amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months (six months for designs) prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Insert Priority
Information:
(if appropriate)**Prior Foreign Application(s)****Priority Claimed**

<u>20030292</u>	<u>Finland</u>	<u>February 26, 2003</u>	☒	☐
(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
_____	_____	_____	☐	☐
(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
_____	_____	_____	☐	☐
(Number)	(Country)	(Month/Day/Year Filed)	Yes	No
_____	_____	_____	☐	☐
(Number)	(Country)	(Month/Day/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional applications(s) listed below.

Insert Provisional
Application(s):
(if any)

_____	_____
(Application Number)	(Filing Date)
_____	_____
(Application Number)	(Filing Date)

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More than 12 Months (6 Months for Designs) Prior to the Filing Date of This Application:

Country	Application Number	Date of Filing (Month/Day/Year)
_____	_____	_____
_____	_____	_____

Insert Requested
Information:
(if appropriate)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States and/or PCT application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States and/or PCT application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to the patentability as defined in Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

Insert Prior U.S.
Application(s):
(if any)

_____	_____	_____
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
_____	_____	_____
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the practitioners at **CUSTOMER NO. 2292** as my attorneys or agents to prosecute this application and/or an international application based on this application and to transact all business in the United States Patent and Trademark Office connected therewith and in connection with the resulting patent based on instructions received from the entity who first sent the application papers to the practitioners, unless the inventor(s) or assignee provides said practitioners with a written notice to the contrary:

Send Correspondence to:

BIRCH, STEWART, KOLASCH & BIRCH, LLP or **CUSTOMER NO. 2292**

P.O. Box 747 • Falls Church, Virginia 22040-0747

Telephone: (703) 205-8000 • Facsimile: (703) 205-8050

**PLEASE NOTE:
YOU MUST
COMPLETE
THE
FOLLOWING:**



Full Name of First
or Sole Inventor:
Insert Name of
Inventor
Insert Date This
Document is Signed →

Insert Residence
Insert Citizenship →

Insert Mailing
Address →

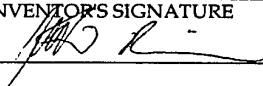
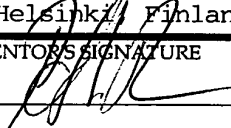
Full Name of Second
Inventor, if any:
see above

Full Name of Third
Inventor, if any:
see above

Full Name of Fourth
Inventor, if any:
see above

Full Name of Fifth
Inventor, if any:
see above

Full Name of Sixth
Inventor, if any:
see above

GIVEN NAME/FAMILY NAME Risto Tuominen	INVENTOR'S SIGNATURE 	DATE* Aug. 12, 2005
Residence (City, State & Country) Helsinki, Finland		CITIZENSHIP Finnish
MAILING ADDRESS (Complete Street Address including City, State & Country) Väinöläkatu 17 B 18, FI-00610 Helsinki, Finland		
GIVEN NAME/FAMILY NAME Petteri Palm	INVENTOR'S SIGNATURE 	DATE* Aug. 12, 2005
Residence (City, State & Country) Helsinki, Finland		CITIZENSHIP Finnish
MAILING ADDRESS (Complete Street Address including City, State & Country) Alkutie 47 as. 1, FI-00660 Helsinki, Finland		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		
GIVEN NAME/FAMILY NAME	INVENTOR'S SIGNATURE	DATE*
Residence (City, State & Country)		CITIZENSHIP
MAILING ADDRESS (Complete Street Address including City, State & Country)		

PATENT APPLICATION SERIAL NO. _____

**U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE
FEE RECORD SHEET**

10/18/2007 SZEWDIE1 00000041 022448 11907795

01 FC:1011	310.00 DA
02 FC:1111	510.00 DA
03 FC:1311	210.00 DA
04 FC:1201	420.00 DA
05 FC:1202	250.00 DA

PTO-1556
(5/87)

*U.S. Government Printing Office 2002-489-267/69033

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number

11907795

APPLICATION AS FILED - PART I

(Column 1)

(Column 2)

SMALL ENTITY

OR

**OTHER THAN
SMALL ENTITY**

FOR		NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))		28 minus 20 =	8
INDEPENDENT CLAIMS (37 CFR 1.16(h))		5 minus 3 =	2
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$260 (\$130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			

RATE (\$)	FEE (\$)
N/A	\$155
N/A	\$255
N/A	\$105
X \$25 =	
X \$105 =	
\$130	
\$185	
TOTAL	

RATE (\$)	FEE (\$)
N/A	\$310
N/A	\$510
N/A	\$210
X \$50 =	250
X \$210 =	420
\$260	
\$370	
TOTAL	1700

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED - PART II

1, 11, 17, 18, 19

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

**OTHER THAN
SMALL ENTITY**

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X \$25 =	
X \$105 =	
\$185	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X \$50 =	
X \$210 =	
\$370	
TOTAL ADD'L FEE	

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDITIONAL FEE (\$)
X \$25 =	
X \$105 =	
\$185	
TOTAL ADD'L FEE	

RATE (\$)	ADDITIONAL FEE (\$)
X \$50 =	
X \$210 =	
\$370	
TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			Application Number		
			Filing Date	Concurrently Herewith	
			First Named Inventor	Risto TUOMINEN	
			Art Unit	3729	
Examiner Name	C. J. Arbes				
Sheet	1	of	2	Attorney Docket Number	0365-0644PUS2

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA*	US-2002-0117743-A1	08-29-2002	Nakatani et al.	
	AB*	US-2003-0137045-A1	07-24-2003	Sugaya et al.	
	AC*	US-2003-0090883-A1	05-15-2003	Asahi et al.	
	AD*	US-2003-0068852-A1	04-10-2003	Towle et al.	
	AE*	US-2005-0000729-A1	01-06-2005	Iijima et al.	
	AF*	US-6,271,469-B1	08-07-2001	Ma et al.	
	AG*	US-6,038,133-A	03-14-2000	Nakatani et al.	
	AH*	US-6,538,210-B2	03-25-2003	Sugaya et al.	
	AI*	US-6,154,366-A	11-28-2000	Ma et al.	
	AJ*	US-4,246,595-A1	01-20-1981	Noyori et al.	
	AK*	US-6,489,685-A1	12-03-2002	Asahi et al.	
	AL*	US-3,931,922	01-13-1976	Jackson et al.	
	AM*	US-3,480,836-A	11-25-1969	Aronstein	
	AN*	US-3,942,245-A	03-09-1976	Jackson et al.	
	AO*	US-4,102,039-A	07-25-1978	Henrickson et al.	
	AP*	US-4,835,846-A	06-06-1989	Juan et al.	
	AQ*	US-5,042,145-A	08-27-1991	Boucquet et al.	
	AR*	US-6,600,231-A1	07-29-2003	Tominaga et al.	
	AS*	US-6,664,130-A1	12-16-2003	Akram	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	BA	JP-2001-53447-A	02-23-2001	Iwaki Denshi KK		✓
	BB	WO-96/02042-A1	01-25-1996	International Business Machines Corporation		✓
	BC	GB-2,204,184-A	11-02-1988	Bracey		✓
	BD	JP-2001-053447-A	02-23-2001	Iwaki Denshi KK		✓
	BE	DE-44 24 396-A1	01-18-1996	International Business Machines Corporation		✓

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

Docket No.: 0365-0644PUS2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Risto TUOMINEN et al.

Application No.:

Confirmation No.: N/A

Filed: Concurrently Herewith

Art Unit: 3729

For: ELECTRONIC MODULE

Examiner: C. J. Arbes

INFORMATION DISCLOSURE STATEMENT
(SUBMISSION WITH CONTINUATION-IN-PART OR RULE 1.53 (B)
CONTINUATION OR DIVISIONAL APPLICATION)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Pursuant to 37 C.F.R. § 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on the PTO-SB08(s), attached hereto.

II. COPIES

☒ a. Copies of cited U.S. patents and patent application publications are not included.
Copies of foreign patent documents and non-patent literature are included.

☐ b. Some or all of the documents listed on the PTO-SB08 are not enclosed because they were cited in the International Search Report and copies should already be in the PTO file.
If copies are needed, please contact the undersigned.

Application No.:

Docket No.: 0365-0644PUS2

☒ c. REFERENCES PREVIOUSLY CITED OR SUBMITTED - Pursuant to 37 C.F.R. §1.98(d), consideration of information listed on the PTO-SB08 form(s) is requested since any patents, publications, or other information which are listed on the PTO-SB08 form(s) but for which copies are not enclosed herewith, were previously cited by or submitted to the PTO in one of the following applications which has been relied upon for an earlier filing date under 35 U.S.C. § 120:

U.S. Appl. No(s) and U.S. Filing Date

10/546,820 filed on August 25, 2005

III. CONCISE EXPLANATION OF THE RELEVANCE

(check at least one box)

☐ a. DOCUMENTS IN THE ENGLISH LANGUAGE - Some or all of the patents, publications, or other information listed on the attached PTO SB08 are in the English language and therefore, do not require a statement of relevancy.

☒ b. DOCUMENTS NOT IN THE ENGLISH LANGUAGE - A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows: *English language Abstracts are attached to the three (3) non-English prior art references provided herewith.*

☐ c. ENGLISH LANGUAGE SEARCH REPORT - An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(III)(A)(3).

☐ d. OTHER - The following additional information is provided for the Examiner's consideration.

IV. FEES (check one box)

☐ a. This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

Application No.:

Docket No.: 0365-0644PUS2

☒ b. This Information Disclosure Statement is being filed concurrent with the filing of a continuation-in-part, continuation, or divisional patent application; therefore, no fee is required.

☐ c. This Information Disclosure Statement is being filed within three months of the filing date of a national application (37 C.F.R. § 1.97(b)(1)). No fee or statement is required.
(This section is not to be used with RCE's.)

☐ d. This Information Disclosure Statement is being filed within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. § 1.97(b)(2)). No fee or statement is required.

☐ e. This Information Disclosure Statement is being filed concurrently with the filing of a Request for Continued Examination under § 1.114 (37 C.F.R. § 1.97(b)(4)). No fee or statement is required.

☐ f. This Information Disclosure Statement is being filed before the mailing date of a first Action on the merits (37 C.F.R. § 1.97(b)(3)). No fee or statement is required. In the event that a first Office Action on the merits has been issued, please consider this IDS under 37 C.F.R. § 1.97(c) and see the statement under 37 C.F.R. § 1.97(e) below, or, if no statement has been made, charge our deposit account for the fee as required by 37 C.F.R. § 1.17(p).

☐ g. This Information Disclosure Statement is being filed before the mailing date of a Final Office Action under 37 C.F.R. § 1.113 (See 37 C.F.R. § 1.97(c)(1)) or before the mailing date of a Notice of Allowance under 37 C.F.R. § 1.311 (See 37 C.F.R. § 1.97(c)(2)).

☐ No statement; therefore, a fee as required by 37 C.F.R. § 1.17(p) is attached.

or

☐ See the statement below. No fee is required.

V. STATEMENT UNDER 37 C.F.R. § 1.97(e)

(check only one box)

The undersigned hereby states that:

Application No.:

Docket No.: 0365-0644PUS2

☐ a. Each item of information contained in the IDS was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than 30 days prior to the filing of this IDS; or

☐ b. Each item of information contained in the IDS was first cited in any communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS; or

☐ c. No item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of IDS was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of the IDS.

☐ d. Some of the items of information were cited in a communication from a foreign Patent Office. As to this information, the undersigned states that each item of information contained in the IDS was first cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this IDS. As to the remaining information, the undersigned hereby states that no item of this remaining information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application and, to the best of my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this statement.

VI. PAYMENT OF FEES (check one box)

☐ The required fee is listed on the attached Fee Transmittal.

☒ No fee is required.

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is

Application No.:

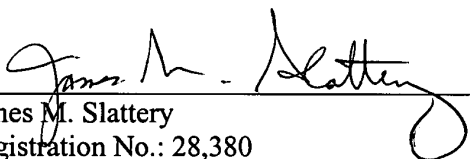
Docket No.: 0365-0644PUS2

requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 02-2448.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to our Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Dated: October 17, 2007

Respectfully submitted,

By 
James M. Slattery
Registration No.: 28,380
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant

Attachment(s):

- ☒ PTO/SB/08
- ☒ Document(s)
- ☐ Foreign Search Report(s)
- ☐ Fee
- ☐ Other:

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

11	207, 798
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APPLICATION AS FILED – PART I

(Column 1)

(Column 2)

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(ii))	25	5
INDEPENDENT CLAIMS (37 CFR 1.16(h))	5	2
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(i))		

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

AMENDMENT A	(Continued)		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	CLAIMS REMAINING AFTER AMENDMENT			
Total (37 CFR 1.16(l))	*	Minus	**	=
Independent (37 CFR 1.16(h))	*	Minus	***	=
Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))				

SMALL ENTITY

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

OR

OTHER THAN
SMALL ENTITY

RATE (\$)		ADDITIONAL FEE (\$)
X	=	
X	=	
360		
TOTAL ADD'T FEE		

(Column 1)

(Column 2)

(Column 3)

AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
	Total (37 CFR 1.16(i))	*	Minus	**	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=
	Application Size Fee (37 CFR 1.16(s))				
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					

RATE (\$)	ADDITIONAL FEE (\$)
100	0
200	0
300	0
400	0
500	0
600	0
700	0
800	0
900	0
1000	0
1100	0
1200	0
1300	0
1400	0
1500	0
1600	0
1700	0
1800	0
1900	0
2000	0
2100	0
2200	0
2300	0
2400	0
2500	0
2600	0
2700	0
2800	0
2900	0
3000	0
3100	0
3200	0
3300	0
3400	0
3500	0
3600	0
3700	0
3800	0
3900	0
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4100	0
4200	0
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4800	0
4900	0
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5100	0
5200	0
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9300	0
9400	0
9500	0
9600	0
9700	0
9800	0
9900	0
10000	0

RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'N FEE	

OR

RATE (\$)	ADDITIONAL FEE (\$)
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RATE (\$)	ADDITIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
11/907,795	10/17/2007	3729	1700	0365-0644PUS2	25	5

CONFIRMATION NO. 6351

2292

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

FILING RECEIPT



OC000000026727117*

Date Mailed: 11/20/2007

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Risto Tuominen, Helsinki, FINLAND;
Petteri Palm, Helsinki, FINLAND;

Power of Attorney: The patent practitioners associated with Customer Number 2292

Domestic Priority data as claimed by applicant

This application is a CON of 10/546,820 08/25/2005 PAT 7,299,546
which is a 371 of PCT/FI04/00101 02/25/2004

Foreign Applications

FINLAND 20030292 02/26/2003

If Required, Foreign Filing License Granted: 11/13/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/907,795**

Projected Publication Date: 02/21/2008

Non-Publication Request: No

Early Publication Request: No

Title

Electronic module

Preliminary Class

029

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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NOT GRANTED

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APPLICATION NUMBER	FILING OR 371(c) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/907,795	10/17/2007	Risto Tuominen	0365-0644PUS2

CONFIRMATION NO. 6351

2292
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA22040-0747

Title: Electronic module

Publication No. US-2008-0043441-A1

Publication Date: 02/21/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Pre-Grant Publication Division, 703-605-4283

PLUS Search Results for S/N 11907795, Searched Tue Sep 23 14:02:25 EDT 2008
The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/907,795	10/17/2007	Risto Tuominen	0365-0644PUS2	6351
2292 7590 10/01/2008 BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			EXAMINER NGUYEN, HOA CAO	
			ART UNIT 2841	PAPER NUMBER
			NOTIFICATION DATE 10/01/2008	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	11/907,795	TUOMINEN ET AL.	
	Examiner	Art Unit	
	HOA C. NGUYEN	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 17 October 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-25 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☒ Certified copies of the priority documents have been received in Application No. 10/546,820.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 10/17/07.

4) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 9 and 19 are objected to because of the following informalities:

Claim 9: The "glass-fibre" must be changed to --glass-fiber.

Claim 19: The "said plurality" must be changed to ----said plurality of electronic modules.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The limitation, "the conductive-pattern layer", fails to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner does not know exactly what conductive-pattern layer the Applicant means in this claim.

For continuing examination, the Examiner assumes the Applicant means the second conductive-pattern layer.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, 4-9, 11, 14-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Asahi et al. (US 20030090883, hereafter Asahi).

Regarding claim 1, as shown in figure 3, Asahi discloses an electronic module, comprising:

(a) a first conductive-pattern layer 308 (par.60, considering the 3rd one from the bottom) having a first surface (top surface of the 3rd pattern layer),

(b) contact bumps 307 (par.60) made on the first surface of the first conductive-pattern layer,

(c) a component 306 (par.60) inherently having flat contact zones, and

(d) an insulating-material layer 301 (par.60) on the first surface of the first conductive-pattern layer,

(e) wherein the component is embedded in the insulating-material layer and the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

Regarding claim 2, Asahi discloses the insulating-material layer comprises a first surface (bottom surface) and a second surface (top surface), the first surface being against the first conductive-pattern layer, and the electronic module comprises a second

conductive-pattern layer 302 (par.60) on the second surface of the insulating-material layer.

Regarding claim 4, Asahi discloses the component is inherently a microcircuit.

Regarding claim 5, Asahi discloses the component is entirely protected inside the insulating-material layer.

Regarding claim 6, Asahi discloses the insulating-material layer comprises a first surface (top surface) and a second surface (bottom), the first surface being against the first conductive-pattern layer, and the electronic module comprises a conductive film 302 (par.60) on the second surface of the insulating-material layer.

It is noted that the "for protecting the component against electromagnetic radiation" is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art.

Regarding claim 7, as shown in figure 3, Asahi discloses a plurality of components 304 having flat contact zones metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

Regarding claim 8, Asahi discloses the plurality of components are inherently electrically connected to each other by means of the first conductive-pattern layer.

Regarding claim 9, Asahi discloses the insulating-material layer is a glass-fiber reinforced epoxy sheet (par.48).

Regarding claim 11, as shown in figure 3, Asahi discloses every limitation as shown in claims 1 and 2 above including an electronic module, comprising:

(a) a first conductive-pattern layer 308 having a first surface,

- (b) a second conductive-pattern layer 302 having a second surface (lower surface of the conductive-pattern),
- (c) an insulating-material layer 301 between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,
- (d) contact bumps 307 made on the first surface of the first conductive-pattern layer,
- (e) a component 306 having flat contact zones embedded in the insulating-material layer such that the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

Regarding claim 14, the limitation, "the second conductive-pattern layer is configured to protect the component against electromagnetic radiation", is interpreted to only require the ability to so perform. In the case of product claim, only the structure of the claim distinguishes over the prior art. Therefore, Asahi anticipates the claim.

Furthermore, it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ 2d 1647 (1987).

Regarding claim 15, Asahi discloses every limitation as shown in claim 7 above.

Regarding claim 16, Asahi discloses the plurality of components includes at least one microcircuit 306, and the plurality of components 304 are electrically connected to each other inherently by means of the first conductive-pattern layer.

Regarding claim 17, as shown in figures 8-11, Asahi discloses every limitation as shown in claims 1 and 11 above and including a multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of the plurality comprises:

- (a) a first conductive-pattern layer 308 having a first surface,
- (b) contact bumps 307 made on the first surface of the first conductive-pattern layer,
- (c) an insulating-material layer 301 on the first surface of the first conductive-pattern layer, and
- (d) a component 306 embedded in the insulating-material layer, the component having flat contact zones metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

Regarding claim 18, as shown in figures 8-11, Asahi discloses every limitation as shown in claims 1 and 11 above and including a multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein each of the modules comprises:

- (a) a first conductive-pattern layer 308 having a first surface,
- (b) contact bumps 307 made on the first surface of the first conductive-pattern layer,
- (c) an insulating-material layer 301 on the first surface of the first conductive-pattern layer, and

(d) a component 306/304 embedded in the insulating-material layer, the component having flat contact zones metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

Regarding claim 19, as shown in figures 8-11, Asahi discloses every limitation as shown in claims 1 and 11 above and including a multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of the plurality of electronic modules comprises:

- (a) a first conductive-pattern layer 308 having a first surface,
- (b) a second conductive-pattern layer 302 having a second surface,
- (c) an insulating-material layer 301 between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,
- (d) contact bumps 307 made on the first surface of the first conductive-pattern layer,
- (e) a component 306 having flat contact zones embedded in the insulating-material layer such that the flat contact zones of the component are metallurgically and electrically connected to the contact bumps made on the first surface of the first conductive-pattern layer.

Regarding claims 20, 22, 23, Asahi discloses the multi-layered electronic module inherently comprising a plurality of memory circuits (because chip 306 is a semiconductor chip, therefore it can be a memory chip).

Regarding claims 21, 24, 25, Asahi inherently discloses the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asahi in view of Asai et al. (US 20010037896, hereafter Asai).

Regarding claims 3 and 12, Asahi discloses every limitation as shown in claim 1 above, but does not disclose the contact bumps 307 include a layered structure, containing at least two layers of at least two different materials.

Asai, as shown in figure 21, Asai discloses contact bumps (76U/72/74) include a layered structure (as clearly shown in the figure), containing at least two layers of at least two different materials (nickel layer 72 and gold layer 74).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to employ the teachings from Asai to include a layered structure containing at least two layers of at least two different materials on the bumps of Asahi in order to protect the contact bumps from corrosion.

Regarding claim 13, Asahi discloses the component is inherently a microcircuit.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Asahi.

Regarding claim 10, Asahi discloses every limitation as shown in claim 1 above, but does not disclose the insulating-material layer is a flexible organic sheet.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to make the insulating-material layer of Asahi of a flexible organic sheet, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Citation of Relevant Art

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Goldsworthy et al.	US 20040026112 A1
Niinobe, Hiroshi et al.	US 20030188885 A1
Wermelinger, Anton	US 20030159849 A1
Kato, Mitsunobu et al.	US 20030121692 A1.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOA C. NGUYEN whose telephone number is (571)272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeremy C. Norris/
Primary Examiner, Art Unit 2841

Hoa C. Nguyen

Notice of References Cited	Application/Control No. 11/907,795	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.	
	Examiner HOA C. NGUYEN	Art Unit 2841	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0090883	05-2003	Asahi et al.	361/761
*	B	US-2001/0037896	11-2001	Asai et al.	174/255
*	C	US-2004/0026112	02-2004	Goldsworthy et al.	174/106.00R
*	D	US-2003/0188885	10-2003	Niinobe et al.	174/73.1
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	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



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BIB DATA SHEET

CONFIRMATION NO. 6351

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
11/907,795	10/17/2007	029	2841	0365-0644PUS2		
APPLICANTS ☒ /HN/ Risto Tuominen, Helsinki, FINLAND; Petteri Palm, Helsinki, FINLAND; ** CONTINUING DATA ***** ☒ /HN/ This application is a CON of 10/546,820 08/25/2005 PAT 7,299,546 which is a 371 of PCT/FI04/00101 02/25/2004 ** FOREIGN APPLICATIONS ***** ☒ /HN/ FINLAND 20030292 02/26/2003 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 11/13/2007						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and Acknowledged <u>/HOA CAO NGUYEN/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY FINLAND	SHEETS DRAWINGS 8	TOTAL CLAIMS 25	INDEPENDENT CLAIMS 5
ADDRESS BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747 UNITED STATES						
TITLE Electronic module						
FILING FEE RECEIVED 1700	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 11907795	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner HOA C NGUYEN	Art Unit 2841

SEARCHED			
Class	Subclass	Date	Examiner
361	760,763,764,767,768,790-795	9/24/08	HN

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS search	9/23/08	HN
East text searched: 361/728,729,735,760,763,764,767,768,790-795,800,808	9/23/08	HN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 11907795	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner HOA C NGUYEN	Art Unit 2841

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	09/24/2008									
	1	✓									
	2	✓									
	3	✓									
	4	✓									
	5	✓									
	6	✓									
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	24	✓									
	25	✓									

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	101	("4423899" "6152283" "6199738" "4951388" "5384582" "5796929" "6189206" "6223425" "6223425" "4395090" "4589014" "4859717" "4871807" "4897257" "4906345" "5180523" "5326636" "5506604" "5518882" "5725592" "5738688" "5744569" "5757436" "5902340" "5936032" "6148110" "6161811" "6190013" "6199272" "6212637" "6212637" "4327484" "4340637" "4343896" "4378984" "4390248" "4416734" "4556840" "4560999" "4577934" "4629323" "4760099" RE32741 "4808915" "4843712" "4843873" "4851697" "4853053" "4952038" "4984186").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:26
S2	48	("20020117743" "20030137045" "20030090883" "20030068852" "20050000729" "6271469" "6038133" "6538210" "6154366" "4246595" "6489685" "3931922" "3480836" "3942245" "4102039" "4835846" "5042145" "6600231" "6664130").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:34
S3	21	("7122748" "5699612" "3702500" "7202421" "20030116349" "6002592" "6002592" "20040120127" "6324067" "5822191").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:38
S4	17	S3 and @ad< "20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:43
S5	63	("3770529" "3852877" "4080513" "4188513" "4417413" "4663215" "4677528" "4770922" "4829666" "4871608" "4897918" "4964019" "5116440" "5139851" "5139852" "5274701" "5346750" "5384689" "5386343" "5396034" "5468999" "5481795" "5484647" "5506448" "5541450" "5550403" "5558928" "5562971" "5578796" "5583376" "5600541" "5616888" "5628919" "5635301" "5646828" "5650918" "5701233" "5719438" "5729894" "5731227"	US-PGPUB; USPAT; USOCR	OR	ON	2008/09/23 14:45

		"5763947" "5972482" "6029343"). PN. OR ("6324067").URPN.				
S6	21	("5013900" "5036431" "5280413" "5581130" "5699232").PN. OR ("6002592").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/09/23 14:48
S7	1	11/907795	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:54
S8	4981	361/704,710,719.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:55
S9	2984	S8 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:55
S10	340	S9 and (embedded buried burried)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 14:55
S11	1747	361/728,729,735.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:15
S12	1695	S11 not S8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:15
S13	1150	S12 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:15
S14	136	S13 and (embedded buried burried)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:16

S15	3832	361/760,763,764,767,768.ocls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:19
S16	3566	S15 not (S11 S8)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:19
S17	2577	S16 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:19
S18	431	S17 and (embedded buried burried)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:19
S19	18	("4899118" "5164246" "5343363" "5386339" "5452182" "5532513" "5599747" "5661647" "5708570" "5831828" "5855803" "5959297" "6288905" "6344290").PN. OR ("6690583"). URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/09/23 15:25
S20	2350	361/790-795.ocls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:29
S21	1791	S20 not (S15 S11 S8)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:29
S22	1199	S21 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:29
S23	217	S22 and (cavity well open\$3) and (embedded buried burried)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:29

S24	2	"7299546".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:33
S25	17	("20020117743" "20030090883" "20030137045" "3480836" "3931922" "3942245" "4102039" "4246595" "4835846" "5042145" "6038133" "6154366" "6489685" "6538210" "6600231" "6664130").PN. OR ("7299546").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/09/23 15:33
S26	37	((risto near tuominen) (petteri near palm)).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/23 15:41
S27	4	("20010042923" "5349500" "6055723" "6490170").PN. OR ("7202421").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/09/23 15:51
S28	4	("20010042923" "5349500" "6055723" "6490170").PN. OR ("7202421").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/09/24 11:09
S29	2	"20010037896".pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 11:11
S30	10	("4284659" "5055319" "5564180" "5706578" "5712192" "5743006" "5758413").PN. OR ("6055723").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2008/09/24 11:24
S31	83	"174"/\$.ccls. and ((bump with (copper) with (gold) with solder))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 11:26
S32	50	S31 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 11:26
S34	1	S32 and (contact with flat)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 11:27

S35	182	"174"/\$.cls. and glass-fibre	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 11:52
S36	121	S35 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2008/09/24 11:52

9/ 24/ 2008 3:30:58 PM

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>			Complete if Known		
			Application Number	11/907795	
			Filing Date	Concurrently Herewith	
			First Named Inventor	Risto TUOMINEN	
			Art Unit	~~3729~~ 2841	
Examiner Name	~~C. J. Arbes~~ Hoa C. Nguyen				
Attorney Docket Number	0365-0644PUS2				
Sheet	1	of	2		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA*	US-2002-0117743-A1	08-29-2002	Nakatani et al.	
	AB*	US-2003-0137045-A1	07-24-2003	Sugaya et al.	
	AC*	US-2003-0090883-A1	05-15-2003	Asahi et al.	
	AD*	US-2003-0068852-A1	04-10-2003	Towle et al.	
	AE*	US-2005-0000729-A1	01-06-2005	Iijima et al.	
	AF*	US-6,271,469-B1	08-07-2001	Ma et al.	
	AG*	US-6,038,133-A	03-14-2000	Nakatani et al.	
	AH*	US-6,538,210-B2	03-25-2003	Sugaya et al.	
	AI*	US-6,154,366-A	11-28-2000	Ma et al.	
	AJ*	US-4,246,595-A1	01-20-1981	Noyori et al.	
	AK*	US-6,489,685-A1	12-03-2002	Asahi et al.	
	AL*	US-3,931,922	01-13-1976	Jackson et al.	
	AM*	US-3,480,836-A	11-25-1969	Aronstein	
	AN*	US-3,942,245-A	03-09-1976	Jackson et al.	
	AO*	US-4,102,039-A	07-25-1978	Henrickson et al.	
	AP*	US-4,835,846-A	06-06-1989	Juan et al.	
	AQ*	US-5,042,145-A	08-27-1991	Boucquet et al.	
	AR*	US-6,600,231-A1	07-29-2003	Tominaga et al.	
	AS*	US-6,664,130-A1	12-16-2003	Akram	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	BA	JP-2001-53447-A	02-23-2001	Iwaki Denshi KK		✓
	BB	WO-96/02042-A1	01-25-1996	International Business Machines Corporation		✓
	BC	GB-2,204,184-A	11-02-1988	Bracey		✓
	BD	JP-2001-053447-A	02-23-2001	Iwaki Denshi KK		✓
	BE	DE-44 24 396-A1	01-18-1996	International Business Machines Corporation		✓

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. * CITE NO.: Those application(s) which are marked with an single asterisk (*) next to the Cite No. are not supplied (under 37 CFR 1.98(a)(2)(iii)) because that application was filed after June 30, 2003 or is available in the IFW. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature	/Hoa Nguyen/ (09/23/2008)	Date Considered	09/23/2008
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NCES CONSIDERED EXCEPT WHERE LINED TH 4. /HN/

Electronic Patent Application Fee Transmittal				
Application Number:		11907795		
Filing Date:		17-Oct-2007		
Title of Invention:		Electronic module		
First Named Inventor/Applicant Name:		Risto Tuominen		
Filer:		Joseph A. Kolasch/Nancy Purks		
Attorney Docket Number:		0365-0644PUS2		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Claims in excess of 20	1202	2	52	104
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Exten:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 3 months with \$0 paid	1253	1	1110	1110
Miscellaneous:				
Total in USD (\$)				1214

Electronic Acknowledgement Receipt	
EFS ID:	5068085
Application Number:	11907795
International Application Number:	
Confirmation Number:	6351
Title of Invention:	Electronic module
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	02292
Filer:	Joseph A. Kolasch/Nancy Purks
Filer Authorized By:	Joseph A. Kolasch
Attorney Docket Number:	0365-0644PUS2
Receipt Date:	31-MAR-2009
Filing Date:	17-OCT-2007
Time Stamp:	14:09:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1214
RAM confirmation Number	9880
Deposit Account	022448
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charged under 37 C.F.R. Section 1.17 (Patent application and reexamination processing)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		20090331Amend.pdf	4522907 509c4d0d557cbb98690bb139aa527d0bcb41f7a8	yes	14

Multipart Description/PDF files in .zip description

Document Description	Start	End
Fee Worksheet (PTO-06)	1	1
Extension of Time	2	2
Amendment/Req. Reconsideration-After Non-Final Reject	3	3
Claims	4	10
Applicant Arguments/Remarks Made in an Amendment	11	14

Warnings:

Information:

2	Fee Worksheet (PTO-06)	fee-info.pdf	31801 5cc7e2d510db2e8ab56714dfd9d3ac1a0d46790c	no	2
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Warnings:

Information:

Total Files Size (in bytes): 4554708

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Docket No.: 0365-0644PUS2
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Risto TUOMINEN et al.

Application No.: 11/907,795

Confirmation No.: 6351

Filed: October 17, 2007

Art Unit: 2841

For: METHOD FOR MANUFACTURING AN
ELECTRONIC MODULE

Examiner: H. C. Nguyen

AMENDMENT IN RESPONSE TO NON-FINAL OFFICE ACTION

MS Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

March 31, 2009

Madam:

INTRODUCTORY COMMENTS

In response to the Office Action dated October 1, 2008, the due date for response having been extended to April 1, 2009, please amend the above-identified U.S. patent application as follows:

Amendments to the Claims begin on page 8 of this paper.

Remarks/Arguments begin on page 9 of this paper.

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An electronic module, comprising:

a first conductive-pattern layer having a first surface,

~~layer;~~ first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer and metallurgically and electrically connected thereto,

a component having flat contact zones,

second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and

an insulating-material layer on the first surface of the first conductive-pattern layer.

wherein the component is embedded in the insulating-material layer and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, metallurgically and electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer.
2. (Originally) The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer, and the electronic module comprises a second conductive-pattern layer on the second surface of the insulating-material layer.
3. (Currently Amended) The electronic module of claim 1, wherein the first solid contact bumps include a layered structure, containing at least two layers of at least two different materials.
4. (Original) The electronic module of claim 1, wherein the component is a microcircuit.

5. (Original) The electronic module of claim 1, wherein the component is entirely protected inside the insulating-material layer.

6. (Original) The electronic module of claim 1, wherein the insulating-material layer comprises a first surface and a second surface, the first surface being against the first conductive-pattern layer, and the electronic module comprises a conductive film on the second surface of the insulating-material layer for protecting the component against electromagnetic radiation.

7. (Currently Amended) The electronic module of claim 1, comprising a plurality of components having flat contact zones metallurgically and electrically connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer, layer by means of said second solid contact bumps.

8. (Original) The electronic module of claim 7, wherein the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

9. (Currently Amended) The electronic module of claim 1, wherein the insulating-material layer is a ~~glass-fibre~~ glass-fiber reinforced epoxy sheet

10. (Original) The electronic module of claim 1, wherein the insulating-material layer is a flexible organic sheet.

11. (Currently Amended) An electronic module, comprising:
a first conductive-pattern layer having a first surface,
a second conductive-pattern layer having a second surface,
an insulating-material layer between the first surface of the first conductive-pattern layer and

the second surface of the second conductive-pattern layer,

first solderless contact bumps made on the first surface of the first conductive-pattern layer,
layer and metallurgically and electrically connected thereto.

a component having flat contact zones embedded in the insulating-material ~~layer~~ layer,

second solderless contact bumps made on the flat contact zones and metallurgically and
electrically connected thereto, and

wherein ~~such that~~ the flat contact zones of the component are ~~metallurgically and~~
metallurgically, electrically and solderlessly connected to the first solderless contact bumps made
on the first surface of the first conductive-pattern ~~layer~~ layer by means of the second solderless
contact bumps made on said flat contact zones.

12. (Currently Amended) The electronic module of claim 11, wherein the first
solderless contact bumps include a layered structure, containing at least two layers of at least two
different materials.

13. (Original) The electronic module of claim 12, wherein the component is a
microcircuit.

14. (Currently Amended) The electronic module of claim 11, wherein the second conductive-pattern layer is configured to protect the component against electromagnetic radiation.

15. (Currently Amended) The electronic module of claim 11, comprising a plurality of components having flat contact zones and second solderless contact bumps made on the flat contact zones, the flat contact zones being metallurgically and electrically connected to the first contact bumps made on the first surface of the first conductive-pattern ~~layer.~~ layer by means of said second solderless contact bumps.

16. (Original) The electronic module of claim 15, wherein the plurality of components includes at least one microcircuit, and the plurality of components are electrically connected to each other by means of the first conductive-pattern layer.

17. (Currently Amended) A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:

a first conductive-pattern layer having a first surface,
first solderless contact bumps made on the first surface of the first conductive-pattern layer,
an insulating-material layer on the first surface of the first conductive-pattern layer, and
a component embedded in the insulating-material ~~layer,~~ layer and having flat contact zones,
second solderless contact bumps made on the flat contact zones of the component, wherein,
~~the component having flat contact zones of the component are~~ metallurgically and electrically
connected to the first conductive-pattern layer via the first solderless contact bumps made on the
first surface of the first conductive-pattern ~~layer.~~ layer and the second solderless contact bumps
made on the flat contact zones of the component.

18. (Currently Amended) A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein each of said plurality of electronic modules comprises:

a first conductive-pattern layer having a first surface,

first solderless contact bumps made on the first surface of the first conductive-pattern layer,

an insulating-material layer on the first surface of the first conductive-pattern layer, and

a component embedded in the insulating-material layer, the component having flat contact zones,

second solderless contact bumps made on the flat contact zones of the component, and

wherein the flat contact zones of the component are metallurgically, metallurgically and electrically and solderlessly connected to the first conductive-pattern layer by means of the second solderless contact bumps made on the flat contact zones and the first solderless contact bumps made on the first surface of the first conductive-pattern layer.

19. (Currently Amended) A multi-layered electronic module, comprising a plurality of electronic modules attached on top of each other, wherein at least one of the modules of said plurality comprises:

a first conductive-pattern layer having a first surface,

a second conductive-pattern layer having a second surface,

an insulating-material layer between the first surface of the first conductive-pattern layer and the second surface of the second conductive-pattern layer,

first solid contact bumps solderlessly made on the first surface of the first conductive-pattern layer, layer and metallurgically and electrically connected thereto.

a component having flat contact zones embedded in the insulating-material ~~layer~~ layer.

second solid contact bumps solderlessly made on the flat contact zones and metallurgically and electrically connected thereto, and

wherein the first solid contact bumps such that the flat contact zones of the component are metallurgically and electrically connected to ~~the contact bumps made on the first surface of the~~ first conductive-pattern layer via respective first and second solid contact bumps.

20. (Currently Amended) The multi-layered electronic module according to ~~one of~~ the claim 17, comprising a plurality of memory circuits.

21. (Currently Amended) The multi-layered electronic module according to ~~one of~~ the claim 17, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

22. (Currently Amended) The multi-layered electronic module according to ~~one of~~ the claim 18, comprising a plurality of memory circuits.

23. (Currently Amended) The multi-layered electronic module according to ~~one of~~ the claim 19, comprising a plurality of memory circuits.

24. (Currently Amended) The multi-layered electronic module according to ~~one of~~ the claim 18, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

25. (Currently Amended) The multi-layered electronic module according to ~~one of~~ the claim 19, wherein the electronic modules are electrically connected to each other in order to form a multi-layered functioning totality.

26. (New) The electronic module of claim 1 wherein the metallurgically electrical connection are ultrasonic or thermo-compression connections.

Application No. 11/907,795
Amendment dated March 31, 2009
Reply to Office Action of October 1, 2008

Docket No.: 0365-0644PUS2

27. (New) The electronic module of claim 26 wherein the metallurgically electrical connections are facilitated by the presence of one or more metals selected from the group consisting of copper, aluminum, gold and tin.

REMARKS

The claims have been objected to for the reasons set forth in paragraph 1 of the Examiner's Office Action letter. As the Examiner will note, claims 9 and 19 have been amended to correct the informality referred to by the Examiner and accordingly it is believed that this objection has been eliminated.

Claim 14 has been rejected by the Examiner under 35 USC 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. As the Examiner will note, claim 14 has been amended to correct the inadvertency referred to by the Examiner and accordingly it is believed that this rejection has been eliminated.

Claims 1, 2, 4-9, 11, and 14-25 have been rejected by the Examiner under 35 USC 102(e) as being anticipated by Asahi et al. (US 2003/0090883, hereafter Asahi). Also, claims 3 and 12-13 have been rejected by the Examiner under 35 USC 103(a) as being unpatentable over Asahi in view of Asai et al. (US 2001/0037896, hereafter Asai). These rejections are respectfully traversed.

The present invention is directed to an electronic module, which includes one or more components embedded in an installation base. The electronic module can be a module-like circuit board, which includes several components, which are connected to each other electrically, through the conducting structures manufactured in the module. The electronic module comprises at least one conductive pattern layer having contact bumps made on its flat surface, an electrical component having flat contact zones, and an insulating material layer applied to the electronic module wherein the electronic component is embedded in the insulating material layer and the flat contact zones of the electronic component are metallurgically and electrically connected to the contact bumps made on the surface of the conductive pattern layer. Advantageously, there can be provided multi-layered electronic modules with a plurality of such modules stacked on top of each other. Because the components can be embedded inside an insulating material, a

reliable and mechanically durable construction is achieved. In one of the advantageous features of the present invention, the electronic module utilizes a plurality of solid contact bumps which are solderlessly disposed on the various conductive layers and, in fact, are metallurgically and electrically connected to such conductive layers. The use of a metallurgical and electrical connection between respective elements of the electronic module of the present invention represents a significant advance over such prior art electrical connections produced by means of solder, conductive adhesives, and the like.

The Asahi et al. reference relates to a circuit component built-in module in which a circuit component is arranged in an internal portion of an insulating layer. However, in defining the circuit component built-in module, the prior art reference does not explicitly disclose that the bumps 307 are made on the semiconductor chip before flip-chip bonding, but this is most certainly the case. Thus, the Asahi reference fails to disclose first contact bumps made on the first surface of the first conductive-pattern layer as defined by the present invention. Moreover, the Asahi reference definitely fails to disclose using two contact bumps, that is, the first and second contact bumps, to form a single contact between the component and the conductive-pattern layer. Another significant difference between the present invention and the Asahi reference is in the type of contact formed between the components and the conductive-pattern layer. According to the present invention, the contact zones of the component are metallurgically connected to the conductive-pattern layer. This is not the case in the Asahi reference. Thus the Asahi reference teaches in paragraph [0060] to use a conductive adhesive 305. Paragraph [0061] states that for the connection between the wiring board 308 and the semiconductor 306, a conductive adhesive, an anisotropic conductive film (ACF), a non-conductive film (NCF) and a bump are used. Conductive adhesives and anisotropic conductive films which are used between the bump and the conductive-pattern do not form metallurgical contact between the attached structures. The quality of the electrical contacts utilized in the Asahi reference does not even remotely compare to the metallurgical contacts utilized by the present invention and defined in the claims of the present application.

In rejecting claims 3 and 12-13, the Examiner further relies upon the Asai publication. However, the Asai reference does not disclose a module having a component embedded therein as in the case of the Asahi reference and as is the case in the present invention. Rather, the Asai reference is concerned with a package board on which an IC chip is to be mounted and more particularly a package board provided with soldering pads which are connected to the IC chip. As noted in paragraph [0115] of the Asai reference, a soldering paste is printed and reflowed at 200°C whereby the manufacture of the structure is necessarily subjected to very high temperatures. This is to be distinguished from the present invention wherein the electrical contacts are not formed with solder. Thus, according to paragraphs [0021] and [0024] of the present application, solderless connections are utilized, said solderless connections containing fewer intermediates and as such do not require high temperatures and molten metal in their manufacture. Instead, temperatures of less than 100°C can be used.

Clearly, the present invention defines an electric module which utilizes such features as solderless connections, a plurality of contact bumps and conductive pattern layers which utilize metallurgical and electrical connections and as such, define an inventive contribution which is not recognized by any of the references relied upon by the Examiner, either alone or in combination.

Accordingly, in view of the above amendments and remarks reconsideration of the rejections and allowance of all of the claims of the present application are respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Joseph A. Kolasch Reg. No. 22,463 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

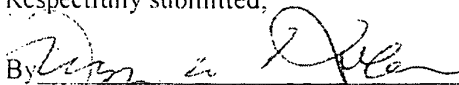
Application No. 11/907,795
Amendment dated March 31, 2009
Reply to Office Action of October 1, 2008

Docket No.: 0365-0644PUS2

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.17; particularly, extension of time fees.

Dated: March 31, 2009

Respectfully submitted,

By 
James M. Slattery
Registration No.: 28,380 # 22463
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Effective on 12/08/2004. Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818). FEE TRANSMITTAL For FY 2009		Complete if Known	
☐ Applicant claims small entity status. See 37 CFR 1.27		Application Number	11/907,795-Conf. #6351
		Filing Date	October 17, 2007
		First Named Inventor	Risto TUOMINEN
		Examiner Name	H. C. Nguyen
		Art Unit	2841
TOTAL AMOUNT OF PAYMENT		(\$)	1,214.00
		Attorney Docket No.	0365-0644PUS2

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2448 Deposit Account Name: Birch, Stewart, Kolasch & Birch, LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee
☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	330	165	540	270	220	110	
Design	220	110	100	50	140	70	
Plant	220	110	330	165	170	85	
Reissue	330	165	540	270	650	325	
Provisional	220	110	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee (\$)	Small Entity Fee (\$)
Each claim over 20 (including Reissues)	52	26
Each independent claim over 3 (including Reissues)	220	110
Multiple dependent claims	390	195

Total Claims	Extra Claims	Fee (\$)	Fee Paid (\$)	Multiple Dependent Claims
27	2	52	\$104	

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims	Extra Claims	Fee (\$)	Fee Paid (\$)
5	5		

HP = highest number of independent claims paid for, if greater than 3.

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee (\$)	Fee Paid (\$)

4. OTHER FEE(S)

	Fees Paid (\$)
Non-English Specification. Additional Claim Fee	104.00
Other (e.g., late filing surcharge): 1253 Extension for response within third month	1,110.00

SUBMITTED BY		Registration No.	28,380	Telephone	(703) 205-8015
Signature		(Attorney/Agent)		Date	March 31, 2009
Name (Print/Type)	James M. Slattery				

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Birch, Stewart, Kolasch & Birch, LLP

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/907,795		Filing Date 10/17/2007		☐ To be Mailed		
APPLICATION AS FILED – PART I											
(Column 1)			(Column 2)			SMALL ENTITY ☐ OR		OTHER THAN SMALL ENTITY			
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)				
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A						
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A	N/A		N/A						
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A						
TOTAL CLAIMS (37 CFR 1.16(j))		minus 20 =	*		X \$ =				OR X \$ =		
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*		X \$ =				OR X \$ =		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
					TOTAL				TOTAL		
* If the difference in column 1 is less than zero, enter "0" in column 2.											
APPLICATION AS AMENDED – PART II											
(Column 1)			(Column 2)			(Column 3)			SMALL ENTITY OR OTHER THAN SMALL ENTITY		
AMENDMENT	03/31/2009		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		
	Total (37 CFR 1.16(i))		* 27	Minus	** 25	= 2		X \$ =		OR X \$52=	
	Independent (37 CFR 1.16(h))		* 5	Minus	***5	= 0		X \$ =		OR X \$220=	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
	TOTAL ADD'L FEE				TOTAL ADD'L FEE		104				
AMENDMENT	Total (37 CFR 1.16(i))		*	Minus	**	=		X \$ =		OR X \$ =	
	Independent (37 CFR 1.16(h))		*	Minus	***	=		X \$ =		OR X \$ =	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
	TOTAL ADD'L FEE				TOTAL ADD'L FEE						
	* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/DENISE HOPKINS/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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NOTICE OF ALLOWANCE AND FEE(S) DUE

2292 7590 06/15/2009

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER

NGUYEN, HOA CAO

ART UNIT

PAPER NUMBER

2841

DATE MAILED: 06/15/2009

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/907,795	10/17/2007	Risto Tuominen	0365-0644PUS2	6351

TITLE OF INVENTION: ELECTRONIC MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	09/15/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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2292 7590 06/15/2009

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/907,795	10/17/2007	Risto Tuominen	0365-0644PUS2	6351

TITLE OF INVENTION: ELECTRONIC MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	09/15/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, HOA CAO	2841	361-761000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

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☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____
Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/907,795	10/17/2007	Risto Tuominen	0365-0644PUS2	6351
2292	7590	06/15/2009	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			NGUYEN, HOA CAO	
			ART UNIT	PAPER NUMBER
			2841	
DATE MAILED: 06/15/2009				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	11/907,795	TUOMINEN ET AL.	
	Examiner	Art Unit	
	HOA C. NGUYEN	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 3/31/09.

2. ☒ The allowed claim(s) is/are 1-27.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 10/546,820.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
 * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of
 Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____ 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ 7. ☐ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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DETAILED ACTION

1. The amendment filed on 3/31/09 has been entered.

Response to Arguments

2. Applicant's arguments, see Remarks (pages 10-11), filed 3/31/09, with respect to bonding structure of the invention that both of the prior art references (Asahi et al, and Asai et al.) fail to teach, have been fully considered and are persuasive.

Allowable Subject Matter

3. Claims 1-27 are allowed.

Reasons for allowance

4. The following is an examiner's statement of reasons for allowance:

(a) Regarding claims 1-10 and 26-27, the best prior art references, Asahi et al. (US 2003/0090833) and Asai et al. (US 20010037896), taken alone or in combination, fails to teach or fairly suggest, at least on claim 1, in combining with other limitations, the component is embedded in the insulating-material layer and wherein the second solid contact bumps made on the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first solid contact bumps made on the first surface of the first conductive-pattern layer. None of the reference art of record discloses or renders obvious such a combination.

(b) Regarding claims 11-16, the best prior art references, Asahi et al. (US 2003/0090833) and Asai et al. (US 20010037896), taken alone or in combination, fails to teach or fairly suggest, at least on claim 16, in combining with other limitations, the flat contact zones of the component are metallurgically, electrically and solderlessly

connected to the first solderless contact bumps made on the first surface of the first conductive-pattern layer. None of the reference art of record discloses or renders obvious such a combination.

(c) Regarding claims 17 and 20-21, the best prior art references, Asahi et al. (US 2003/0090833) and Asai et al. (US 20010037896), taken alone or in combination, fails to teach or fairly suggest, at least on claim 17, in combining with other limitations, second solderless contact bumps made on the flat contact zones of the component, wherein flat contact zones of the component are metallurgically and electrically connected to the first conductive-pattern layer via the first solderless contact bumps made on the first surface of the first conductive-pattern layer and the second solderless contact bumps made on the flat contact zones of the component. None of the reference art of record discloses or renders obvious such a combination.

(d) Regarding claims 18, 22 and 24, the best prior art references, Asahi et al. (US 2003/0090833) and Asai et al. (US 20010037896), taken alone or in combination, fails to teach or fairly suggest, at least on claim 18, in combining with other limitations, the flat contact zones of the component are metallurgically, electrically and solderlessly connected to the first conductive-pattern layer by means of the second solderless contact bumps made on the flat contact zones and the first solderless contact bumps made on the first surface of the first conductive-pattern layer. None of the reference art of record discloses or renders obvious such a combination.

(e) Regarding claims 19, 23 and 25, the best prior art references, Asahi et al. (US 2003/0090833) and Asai et al. (US 20010037896), taken alone or in combination, fails

to teach or fairly suggest, at least on claim 19, in combining with other limitations, the first solid contact bumps such that the flat contact zones of the component are metallurgically and electrically connected to the first conductive-pattern layer via respective first and second solid contact bumps. None of the reference art of record discloses or renders obvious such a combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOA C. NGUYEN whose telephone number is (571)272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dean A. Reichard/
Supervisory Patent Examiner, Art
Unit 2841

Hoa C. Nguyen

<i>Index of Claims</i> 	Application/Control No. 11907795	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner HOA C NGUYEN	Art Unit 2841

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47		
CLAIM		DATE								
Final	Original	09/24/2008	06/05/2009							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
6	6	✓	=							
7	7	✓	=							
8	8	✓	=							
9	9	✓	=							
10	10	✓	=							
13	11	✓	=							
14	12	✓	=							
15	13	✓	=							
16	14	✓	=							
17	15	✓	=							
18	16	✓	=							
19	17	✓	=							
22	18	✓	=							
25	19	✓	=							
20	20	✓	=							
21	21	✓	=							
23	22	✓	=							
26	23	✓	=							
24	24	✓	=							
27	25	✓	=							
11	26		=							
12	27		=							

Issue Classification 	Application/Control No. 11907795	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner HOA C NGUYEN	Art Unit 2841

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
361		761				H	0	5	K	1 / 18 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
361	760	763	764	767	768													

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	15												
2	2	18	16												
3	3	19	17												
4	4	20	20												
5	5	21	21												
6	6	22	18												
7	7	23	22												
8	8	24	24												
9	9	25	19												
10	10	26	23												
11	26	27	25												
12	27														
13	11														
14	12														
15	13														
16	14														

/HOA C NGUYEN/ Examiner.Art Unit 2841 (Assistant Examiner)	6/5/09 (Date)	Total Claims Allowed: 27	
/Dean A. Reichard/ (Primary Examiner)	6/5/09 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 9

Search Notes 	Application/Control No. 11907795	Applicant(s)/Patent Under Reexamination TUOMINEN ET AL.
	Examiner HOA C NGUYEN	Art Unit 2841

SEARCHED			
Class	Subclass	Date	Examiner
361	704,710,719,728,729,735,760,763,764,767,768,790-795,800,808	9/24/08	HN
361	761	6/5/09	HN
Update searched		6/5/09	HN

SEARCH NOTES		
Search Notes	Date	Examiner
PLUS search	9/23/08	HN
East text searched: 361/704,710,719,728,729,735,760,763,764,767,768,790-795,800,808	9/23/08	HN
Inventor name searched	6/5/09	HN
East text searched in classes 174, 361, 257, and 428	6/5/09	HN

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
All	((first near2 pattern) and (first near3 bump) and (metallurg\$5) and (solderless) and (component) and (zone) and (second near3 bump) and (layer) and (component near2 embed\$3) and (connect\$3)).clm.	6/5/09	HN
All	((first near2 pattern) and (second near2 pattern) and (layer) and (surface) and (first near solderless) and (bump) and (metallurg\$5) and (connect\$3) and (second near solderless) and (zone)).clm.	6/5/09	HN
All	((pattern) and (layer) and (surface) and (solderless) and (bump) and (contact\$3) and (metallurg\$5) and (connect\$3) and (zone)).clm.	6/5/09	HN

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BIB DATA SHEET

CONFIRMATION NO. 6351

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
11/907,795	10/17/2007	~~029~~	2841	0365-0644PUS2		
APPLICANTS ☒ HN/ Risto Tuominen, Helsinki, FINLAND; Petteri Palm, Helsinki, FINLAND; ** CONTINUING DATA ***** ☒ HN/ This application is a CON of 10/546,820 08/25/2005 PAT 7,299,546 which is a 371 of PCT/FI04/00101 02/25/2004 ** FOREIGN APPLICATIONS ***** ☒ HN/ FINLAND 20030292 02/26/2003 ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 11/13/2007						
Foreign Priority claimed ☒ Yes ☐ No 35 USC 119(a-d) conditions met ☒ Yes ☐ No Verified and /HOA CAO NGUYEN/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY FINLAND	SHEETS DRAWINGS 8	TOTAL CLAIMS ☒ 27 ~~25~~	INDEPENDENT CLAIMS 5
ADDRESS BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747 UNITED STATES						
TITLE Electronic module						
FILING FEE RECEIVED 1804	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S37	27	((risco near tuominen) (petteri near palm)).in.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:18
S38	15	(US-20030137045-\$ or US-20030090883-\$ or US-20030116349-\$ or US-20010037896-\$).did. or (US-6538210-\$ or US-7122748-\$ or US-6324067-\$ or US-7348213-\$ or US-6548330-\$ or US-6002592-\$ or US-6975516-\$ or US-6690583-\$ or US-6489685-\$ or US-6154366-\$ or US-5349500-\$).did.	US-PGPUB; USPAT	OR	ON	2009/06/05 10:28
S39	0	S38 and (solderless)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:29
S40	0	S38 and metallurg\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:29
S41	6059	361/760,763,764,767,768,790-795.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:30
S42	2981	361/728,729,735,800,808.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:30
S43	8635	S41 S42	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:30
S44	0	S43 and (bump land electode terminal contact) and soldeless	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:31

S45	57	S43 and (bump land electrode terminal contact) and solderless	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:31
S46	156	S43 and (bump land electrode terminal contact) and (solderless (solder near free))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:31
S47	86	S46 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:32
S48	9	S47 and metallurg\$5	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:32
S49	173	("361"/\$.ccls. "174"/\$.ccls.) and @ad<"20030226" and ((bump land electrode terminal land) with metallurg\$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:36
S50	170	S49 not S48	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:36
S51	2	S50 and (solderless (solder near free) (Pb-free))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:37
S52	1168	("257"/\$.ccls. "428"/\$.ccls.) and @ad<"20030226" and ((bump land electrode terminal land) with metallurg\$5)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:41
S53	1039	S52 not S49	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:42

S54	54	S53 and (solderless (solder near free) (Pb-free))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:42
S55	0	((first near2 pattern) and (first near3 bump) and (metallurg\$5) and (solderless) and (component) and (zone) and (second near3 bump) and (layer) and (component near2 embed\$3) and (connect\$3)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:49
S56	0	((first near2 pattern) and (second near2 pattern) and (layer) and (surface) and (first near solderless) and (bump) and (metallurg\$5) and (connect\$3) and (second near solderless) and (zone)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:52
S57	0	((pattern) and (layer) and (surface) and (solderless) and (bump) and (contact\$3) and (metallurg\$5) and (connect\$3) and (zone)).clm.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:54
S58	6225	361/761,704,710,719.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:55
S59	3549	S58 and @ad<"20030226"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:56
S60	16	S59 and (bump land electode terminal contact) and solderless	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2009/06/05 10:56

6/ 5/ 2009 2:15:42 PM

C:\ Documents and Settings\ hnguyen33\ My Documents\ EAST\ Workspaces\ 11907795.wsp

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

2292 7590 06/15/2009

BIRCH STEWART KOLASCH & BIRCH LLP
 PO BOX 747
 FALLS CHURCH, VA 22040-0747

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/907,795	10/17/2007	Risto Tuominen	0365-0644PUS2	6351

TITLE OF INVENTION: ELECTRONIC MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	09/15/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, HOA CAO	2841	361-761000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

- 1 BIRCH, STEWART
 2 KOLASCH & BIRCH LLP
 3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

IMBERA ELECTRONICS OY

Espoo, Finland

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☒ Advance Order - # of Copies 4

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 02-2448 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature

James M. Slattery
 Typed or printed name James M. Slattery

Date 09/14/09

Registration No. 28,380

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		11907795		
Filing Date:		17-Oct-2007		
Title of Invention:		ELECTRONIC MODULE		
First Named Inventor/Applicant Name:		Risto Tuominen		
Filer:		Joseph A. Kolasch/Nancy Purks		
Attorney Docket Number:		0365-0644PUS2		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Small Entity Fee, if applicable, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Printed copy of patent - no color	8001	4	3	12
Total in USD (\$)				1822

Electronic Acknowledgement Receipt	
EFS ID:	6066611
Application Number:	11907795
International Application Number:	
Confirmation Number:	6351
Title of Invention:	ELECTRONIC MODULE
First Named Inventor/Applicant Name:	Risto Tuominen
Customer Number:	02292
Filer:	Joseph A. Kolasch/Nancy Purks
Filer Authorized By:	Joseph A. Kolasch
Attorney Docket Number:	0365-0644PUS2
Receipt Date:	14-SEP-2009
Filing Date:	17-OCT-2007
Time Stamp:	15:28:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1822
RAM confirmation Number	1573
Deposit Account	022448
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charged under 37 C.F.R. Section 1.17 (Patent application and reexamination processing)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	20090914IF.pdf	105522 049b075f3d3cb3f0286f466a80977b8a4c832070	no	1

Warnings:

Information:

2	Fee Worksheet (PTO-875)	fee-info.pdf	33518 3cc28e929a854410a10504900af3ccdc1f458a08	no	2
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Warnings:

Information:

Total Files Size (in bytes): 139040

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/907,795	10/27/2009	7609527	0365-0644PUS2	6351

2292 7590 10/07/2009
BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Risto Tuominen, Helsinki, FINLAND;
Petteri Palm, Helsinki, FINLAND;

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT5967120

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
GE EMBEDDED ELECTRONICS OY		01/13/2020
RECEIVING PARTY DATA		
Name:	IMBERATEK, LLC	
Street Address:	13921 PARK CENTER RD, SUITE 380	
City:	HERNDON	
State/Country:	VIRGINIA	
Postal Code:	20171	
PROPERTY NUMBERS Total: 26		
Property Type	Number	
Patent Number:	7732909	
Patent Number:	7989944	
Patent Number:	7609527	
Patent Number:	8817485	
Patent Number:	8034658	
Patent Number:	8222723	
Patent Number:	8487194	
Patent Number:	9232658	
Patent Number:	8351214	
Patent Number:	8455994	
Patent Number:	8368201	
Patent Number:	9622354	
Patent Number:	9691724	
Patent Number:	9107324	
Patent Number:	10231335	
Patent Number:	10085345	
Patent Number:	10010019	
Patent Number:	10085347	
Patent Number:	9324647	
Patent Number:	9883587	

Property Type	Number
Patent Number:	9674948
Patent Number:	9820375
Patent Number:	10470346
Application Number:	14580257
Application Number:	15355096
Application Number:	16104979

CORRESPONDENCE DATA

Fax Number: (703)643-9789

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 4349062975

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Correspondent Name: YEASUN YOON

Address Line 1: 20319 KIAWAH ISLAND DR

Address Line 4: ASHBURN, VIRGINIA 20147

ATTORNEY DOCKET NUMBER:	PA01GETOIMBERATEK02
NAME OF SUBMITTER:	YEASUN YOON
SIGNATURE:	/yoon/
DATE SIGNED:	02/18/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 7

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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

This CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS (this “**Assignment**”) is made this 13th day of January 2020, by **GE Embedded Electronics Oy**, a Finnish company (“**Assignor**”), in favor of **ImberaTek, LLC**, a Delaware limited liability company (“**Assignee**”).

WHEREAS, Assignor and Assignee are party to that certain patent sale agreement of December 19, 2019 (the “**Patent Sale Agreement**”); capitalized terms used but not otherwise defined in this Assignment shall have the respective meaning assigned thereto in the Patent Sale Agreement; and

WHEREAS, pursuant to the Patent Sale Agreement, Assignor has agreed to sell, convey, transfer, assign and deliver to Assignee all right, title and interest, including, without limitation, Patent Rights, in and to the patents, provisional patent applications, and patent applications listed on Schedule A hereto (collectively, the “**Patents**”).

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged by Assignor, Assignor hereby sells, conveys, transfers, and assigns to Assignee, its successors, legal representatives, and assigns all right, title and interest in the United States and throughout the world in and to:

the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent and counterpart thereof that may be granted in any country or countries foreign to the United States, in each case including without limitation any extensions, substitutes, continuations, continuations-in-part, divisions, reissues, reexaminations, and renewals thereof, or other equivalents thereof, and further, all rights and privileges pertaining to the Patents and any and all letters patent that are or may be granted thereon, and any legal equivalent thereof that may be granted in any country or countries foreign to the United States as well as all inventions, invention disclosures, and discoveries described in any of the foregoing and including, without limitation, the right, if any, to petition, sue or otherwise seek and recover damages, profits and any other remedy (monetary, injunctive, declaratory or other relief or remedy of any kind) in the United States and anywhere throughout the world for any past, present and future infringement thereof, conversion or misappropriation of, or other injury, offense, violation, breach of duty or wrong relating to, any of the Patents, or any license, agreement, contract or other matter relating thereto.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks of the United States of America and the appropriate officers of all other jurisdictions in which the Patents are or may be registered or in which applications included among the Patents are pending, to record the title of Assignee, its successors, legal representatives and assigns, as owner of all right, title and interest in and to the Patents, and to issue to Assignee, its successors, legal representatives and assigns, all letters patent and any legal equivalent thereof that may be granted in any country or countries foreign to the United States and recordings of patent rights resulting from any application included among the Patents, according to this instrument.

Except to the extent that federal law preempts state law with respect to the matters covered hereby, this Assignment shall be governed by and construed in accordance with the laws of the State of Delaware, without giving effect to any of the principles of conflicts of laws thereof that would result in the application of the laws of another jurisdiction to this Assignment.

This Assignment will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

Assignor has the full power and authority, and has obtained all Third-Party consents, approvals and/or other authorizations required to enter into this Assignment and to carry out its obligations hereunder.

IN WITNESS WHEREOF, Assignor has caused this Assignment to be executed by its duly authorized officer, as of the date first written above.

ASSIGNOR:

GE Embedded Electronics Oy

By: 

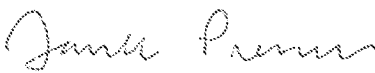
Name: PATRICK K. PATNODE

Title: AUTHORIZED SIGNATORY

Acknowledgement:

State of New York)
)
County of Schenectady)

ss.


SANDRA PREISMAN
Notary Public, State of New York
Reg. No. 8024403
Qualified in Schenectady County
Commission Expires February 10, 2023

On this 13 day of January 2020, before me appeared Patrick K. Patnode, the person who signed this instrument, who acknowledged that he/she signed it as a free act on his/her own behalf or on behalf of the Assignor with authority to do so.

**SCHEDULE A
TO
CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS
PATENTS**

Number	Title	Applicant	Current Assignee	filing date	Family	Estimated Expiration
<u>EP01104647B</u> 1	Method for Manufacturing Solderless High-Density Electronic Modules	Imbera Electronics Oy		2000.04.17	FR, DE, GB	2020.04.17
<u>US6991966</u>	Method for embedding a component in a base and forming a contact	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	BRP10307364B1, CN100566511C, DE60300619T2, EP1474959B1 (AT, FR, DE, IT, IE) (not GB), FI115285B, HK1077151A1, IL163238A, IN224711, KR1013325B1, SG105702, RU2297736C2	2023.01.28
<u>US7294529</u>	Method for embedding a component in a base	Imbera Electronics Oy	GE Embedded Electronics Oy	2003.01.28	CN102348324B, CN1625926B, EP1477048 (GB, AT, FR, DE), FI119215B, IN241345, RU2327311C2, US7732909B2, US7989944B2, US8368201B2, US8455994B2	2024.01.16
<u>US7299546</u>	Method for manufacturing an electronic module	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.02.25	EP1597947(GB, FR, DE) FI119583B, US10085345B2, US2018376597A1, US7609527B2, US8817485B2	2024.03.20
<u>US7673387</u>	Manufacture of a layer including a component	Imbera Electronics Oy	GE Embedded Electronics Oy	2005.08.04	AT503718B1, CN100543983C, FI117812B, JP4630333B2, US8487194B2	2026.08.09

<u>US7696005</u>	Method for manufacturing an electronic module in an installation base	Imbera Electronics Oy	GE Embedded Electronics Oy	2004.09.15	CN1853451B, DE11200400172 7T5, GB2422054B, JP4977464B2, US2015124411A I, US9232658B2	2025.06.12
<u>US8062537</u>	Method for manufacturing an electronics module	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.23	CN101065843B, FI117369B, JP5160895B2, KR101101603B1	2027.06.27
<u>US8225499</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN101199244B, DE11200600150 6 FI121134B, GB2441265B	2028.08.19
<u>US8238113</u>	Electronic module with vertical connector between conductor patterns	Imbera Electronics Oy	Imbera Electronics Oy	2010.07.23		2031.02.11
<u>US8240032</u>	Method for manufacturing an electronics module comprising a component electrically connected to a conductor-pattern layer	Imbera Electronics Oy	Imbera Electronics Oy	2005.06.13	CN101010994B, DE11200500141 4T5, FI117814B, JP4796057B2, KR101034279B1	2028.03.15
<u>US8240033</u>	Method for manufacturing a circuit board	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.15	BR PI0612060-1 CN101199242B, FI122128B, IN269884 JP5175719B2, KR101455234B1 , SG138149	2029.02.21
<u>US8286341</u>	Method of manufacturing a wiring board	Imbera Electronics Oy	Imbera Electronics Oy	2009.04.08	CN102007825B, EP2274962B1 (AT, DE, GB) FI121909B, IN306150B, JP5551680B2, KR101260908B1	2030.09.07
<u>US8547701</u>	Electronics module and method for manufacturing the same	Imbera Electronics Oy	Imbera Electronics Oy	2005.11.24		2026.06.12
<u>US8581109</u>	Method for manufacturing a circuit board structure, and a circuit board structure	Imbera Electronics Oy	Imbera Electronics Oy	2006.06.16	CN100596258C, EP1891845(AT, DE, FR, GB), FI119714B, IN271174 JP5025644B2, KR101090423B1 , US2017071061A I, US9622354B2	2028.08.19

<u>US8631566</u>	Circuit board structure comprising an electrical component and a method for manufacturing a circuit board structure comprising an electrical component	Imbera Electronics Oy	Imbera Electronics Oy	2009.08.24	FI125526B	2031.08.25
<u>US8659134</u>	Multi-chip package and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.07.21	FI122217B, US9691724B2	2031.03.25
<u>US8699233</u>	Circuit module and method of manufacturing the same	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2009.05.11	CN102027585B, FI123205B, US9107324B2, US9324647B2, US9883587B2	2030.10.11
<u>US8735735</u>	Electronic module with embedded jumper conductor	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.07.23	US10231335B2	2030.12.18
<u>US8964409</u>	Electronic module with EMI protection	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.02.05	CN101800216B, JP6126770B2, KR101781446B1 , US10010019B2, US2018352689A I	2031.02.23
<u>US8984746</u>	Manufacture of a circuit board containing a component	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2007.03.15	US10085347B2	2030.11.07
<u>US9301394</u>	Manufacturing method and electronic module with new routing possibilities	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.05.19	US15'937,967 (Reissue application of US9301394)	2033.05.29
<u>US9420694</u>	Method for controlling warpage within electronic products and an electronic product	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.08.31		2030.10.31

<u>US9425158</u>	Rigid-flex module and manufacturing method	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2010.01.05	CN101770959A, CN108133897A, FI122216B, JP5714231B2, KR101615955B1, US9674948B2, US9820375B2	2031.03.14
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<u>US9999136</u>	Method for fabrication of an electronic module and electronic module	GE Embedded Electronics Oy	GE Embedded Electronics Oy	2014.12.15	AT516639B1, CN105704926A, DE10201501619 6A1, FR3030109B1, JP2016157919A, KR20160072822 A, TW201633860A, IN352016	2034.12.15
<u>KR101060856</u>	Method for manufacturing an electronic module, and an electronic module		Imbera Electronics Oy	2010.12.15	(JP 4537995 is an EPCOS patent)	2004.02.25
<u>US8076586</u>	Heat conduction from an embedded component		Imbera Electronics Oy	2011.12.13		2027.10.05
<u>US8351214</u>	Electronics module comprising an embedded microcircuit		Imbera Electronics Oy	2013.01.08	GB2429848, JP5064210, DE 112005000952.1, <u>CN101027948B</u>	2027.07.03
<u>US8034658</u> (divisional of EPCOS patent US7663215)	Electronic module with a conductive-pattern layer and a method of manufacturing same		Imbera Electronics Oy	2011.10.11	FI115601, MX262301, IN236924, KR10068797600 00, BRPI0408964-2, CA2520992, CN100556233, SG115077, IL171212, CN101546759, MX285993, HK1089328, GB1609339, FR1609339, DE1609339	2024.04.08
<u>US8222723</u>	Electric module having a conductive pattern layer		Imbera Electronics Oy	2012.07.17		2024.10.03

US8704359	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2014.04.22		2025.04.13
<u>US9363898</u>	Method for manufacturing an electronic module and an electronic module		GE Embedded Electronics Oy	2016.06.07		2024.03.31

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22cv233	DATE FILED 6/24/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF ImberaTek LLC		DEFENDANT SAMSUNG ELECTRONICS CO., LTD, SAMSUNG ELECTRONICS AMERICA, Inc., and SAMSUNG AUSTIN SEMICONDUCTOR, LLC.,
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,609,527	10/27/2009	ImberaTek LLC
2 8,222,723	7/17/2012	ImberaTek LLC
3 8,368,201	2/5/2013	ImberaTek LLC
4 7,989,944	8/2/2011	ImberaTek LLC
5 8,238,113	8/7/2012	ImberaTek LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

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PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 9,107,324	8/15/2015	ImberaTek LLC
2		
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PLAINTIFF ImberaTek LLC		DEFENDANT SAMSUNG ELECTRONICS CO., LTD, et al
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 7,609,527	10/27/2009	ImberaTek LLC
2 8,222,723	7/17/2012	ImberaTek LLC
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4 7,989,944	8/2/2011	ImberaTek LLC
5 8,238,113	8/7/2012	ImberaTek LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED 10/31/2022	INCLUDED BY ☒ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 11,071,207	7/20/2021	ImberaTek LLC
2 7,732,909	6/8/2010	ImberaTek LLC
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4		
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

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PLAINTIFF ImberaTek LLC		DEFENDANT SAMSUNG ELECTRONICS CO., LTD, SAMSUNG ELECTRONICS AMERICA, Inc., and SAMSUNG AUSTIN SEMICONDUCTOR, LLC.,
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE
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 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.; SAMSUNG ELECTRONICS
AMERICA, INC.; and SAMSUNG AUSTIN SEMICONDUCTOR, LLC,
Petitioner,

v.

IMBERATEK LLC,
Patent Owner.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

Before DONNA M. PRAISS, JON B. TORNQUIST, and
JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

TORNQUIST, *Administrative Patent Judge*.

DECISION
Settlement Prior to Institution of Trial
37 C.F.R. § 42.74

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

With our authorization, Petitioner, Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Austin Semiconductor, LLC, and Patent Owner, ImberaTek LLC, filed a Joint Motion to Dismiss Inter Partes Review Before Institution in each of the above-captioned cases. Paper 8 (“Joint Motions”).¹ In their Joint Motions, the parties contend that dismissal is appropriate as the *inter partes* reviews (“IPRs”) are in their early stages and the parties “have settled all disputes” related to the involved patents. *Id.* at 1–2.

With their Joint Motions, the parties filed (1) a copy of a Settlement and Patent License Agreement that the parties represent “resolves the disputes in the above-captioned *inter partes*” reviews, (2) a Confirmatory Letter from Patent Owner to Petitioner acknowledging and confirming certain facts and rights related to the Settlement and Patent License Agreement, and (3) a Joint Request to treat the settlement documents as business confidential information, to be kept separate from the files of the above-captioned patents. Ex. 1022 (“Settlement and Patent License Agreement”); Ex. 1023 (“Confirmatory Letter”); Paper 9 (“Joint Request”).

“There are strong policy reasons to favor settlement between the parties to a proceeding,” and “[t]he Board expects that a proceeding will terminate after the filing of a settlement agreement, unless the Board has already decided the merits of the proceeding.” Patent Trial and Appeal

¹ We cite to papers and exhibits filed in IPR2022-01597. Similar papers and exhibits were filed in each of the above-captioned cases.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

Board Consolidated Trial Practice Guide November 2019, at 86 (citing 35 U.S.C. §§ 317(a), 327). The above-captioned IPRs are at an early stage, with the Board not yet reaching the merits of the petitions or issuing institution decisions. Thus, we find it is appropriate to dismiss the petitions and terminate the proceedings in each of the above-captioned IPRs.

We also find it appropriate to treat the settlement documents as business confidential information, to be kept separate from the files of the involved patents.

Accordingly, it is

ORDERED that the Joint Motion to Dismiss Inter Partes Review Before Institution in each of the above-captioned cases is *granted*;

FURTHER ORDERED that the parties' Joint Request that the settlement documents (Exs. 1022, 1023) be treated as business confidential information and kept separate from the files of the involved patents is *granted*; and

FUTHER ORDERED that the proceedings in the above-captioned IPRs are *terminated*.

IPR2022-01597 (Patent 8,368,201 B2)
IPR2023-00044 (Patent 8,222,723 B2)
IPR2023-00055 (Patent 9,107,324 B2)
IPR2023-00069 (Patent 7,609,527 B2)
IPR2023-00323 (Patent 7,989,944 B2)

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