

Solderless Interconnection and Packaging Technique for Embedded Active Components

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Abstract

In the present study a solderless interconnection and packaging technique for active components is presented. It is based on electroless copper deposition directly onto photodefined wiring tracks connecting the (I/O) pads of embedded active components. In this manner better electrical conductivity, higher reliability and accuracy of ultra fine-pitch interconnections in a low-cost multichip module are achieved. This non-vacuum and solderless copper/polymer process which makes use of a photosensitive epoxy resin, has been used for interconnecting successfully the pads as small as $30 \times 30 \mu\text{m}^2$. It is emphasized that this solderless process enables the production of reliable electrical connections at ambient temperature without difficulties related to mechanical and thermal stability of very small solder joints. Detailed microstructural observations of interconnected test chips each containing 376 contact pads revealed good chemically bonded interfaces. The electrical performance of the embedded active components is also briefly discussed.

Introduction

Increasing functionality and portability in consumer electronics and telecommunication devices are driving manufacturers to miniaturize their products reliably and cost-effectively - despite the fact that high density assemblies will encounter more technical challenges, e.g. in paste printing, component alignment, contact metallurgy and in substrate technologies. More fundamentally, increasing microjoint densities are related to decreasing solder joint volumes and thinner metallizations (Fig. 1), and so there is a growing reliability risk that too large part of solder joint will transform into brittle intermetallics, when the volumes of the solder joints are in the range of $10^{-4} \dots 10^{-5} \text{ mm}^3$. Besides, in very small solder joints there are relatively few grains, which impair the deformation capability and impurity tolerance of the joints - decreasing also the reliability and electrical performance of very high density assemblies.[1]

A typical implication of decreasing solder volumes affecting the joint reliability is the use of underfills with surface mount flip chip components. Underfills are used for reducing stresses caused by mechanical loading as well as by the CTE-mismatch between organic substrate and silicon. In this communication one must still realize that decrease in

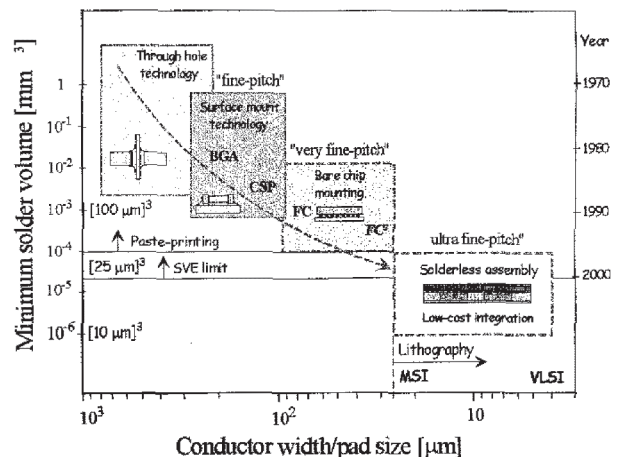


Fig. 1 Tend in solder joint volume as a function of decreasing feature size.

solder joint height will set high requirements for the utilization of underfills.

Besides solder bumped flip chip there is variety of options available for interconnecting high pitch integrated circuits. Flip chip applications based on anisotropically conductive adhesives work with low processing temperatures and has some advantages specially in high pitch assembly, also some disadvantages for example in reworkability [2]. Traditional packaging of active components has developed as well. With the development of BGA and μBGA components, the package size has reduced down to chip scale packages where the absolute size is no larger than 1,2X original die. [3]

Multi chip module (MCM) technologies have also become increasingly attractive during the last decade. High interconnection density is achieved with MCM technology where fine patterned copper layers and dielectric layers are fabricated on various substrates. Integrated circuits are then connected to MCM substrate with wire bond, TAB or flip chip solder bumps. To reduce the inductance and impedance of the connections between chip and the substrate General Electric (GE) introduced high density interconnection technology for embedded chips. HDI technology is a "chip first" solution where active components are placed in cavities formed in a ceramic or embedded into plastic encapsulant (Fig. 2). Interconnections to the chips which are encapsulated

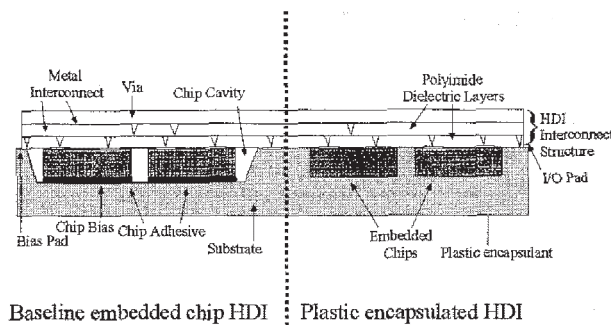


Fig. 2 Schematic presentation of embedded HDI chips [5].

with polymer are made by sputter metallisation through laser ablated vias. The HDI technology enables the fabrication of complex MCM with a very high packaging density and low interconnect impedance. Also the embedded interconnections in the MCM structure provide good protection both mechanically and chemically. [3,4]

In this study a novel manufacturing process for embedding active components into organic substrate is presented. The same technology can be used for embedding active components into printed wiring boards as well. Due to a nature of interconnection method we call it the solderless assembly technique. The additive manufacturing process is based on the electroless copper deposition process and the use of photoimageable a dielectrics. The Solderless interconnection technique is a non-vacuum process and enables ultra high density assembly at ambient temperatures. Therefore, excellent and reliable electrical connections with low contact resistance are achieved without the formation of intermetallic compounds, which impair the properties of small solder joints.

Materials and Methods

To investigate the feasibility of the solderless assembly technique two different test chips were used. The chips were manufactured in co-operation with Finnish electronics industry and the National Research Centre of Finland. All the chips were bumped and manufactured with daisy chain test structure where the I/O-pitch and bump size were the main variables. Bump size and pitch ranged from 30 μm to 70 μm and from 80 μm to 100 μm , respectively. The number of I/O's ranged from 46 to 376 on one chip. Nickel (Ni), gold (Au) and copper (Cu) were investigated as a bump metal.

An epoxy material (from Nagase-Ciba) was used for the moulding of components. Liquid mixture of resin and solvent contained 70 wt-% ceramic particles to adjust the CTE_{cl} of cured matrix close to 17 ppm/°C. Dielectric constant of the epoxy is 3,2 (1 MHz) with the dissipation factor of 0,005.

Test structures to fabricate both the Single Chip Package (SCP) and Multi Chip Module (MCM) components were designed and proper masks for lithographic process were produced. The MCM component contained four test chips, each containing 376 I/O's in three rows with the pitch of 100

μm . Before the moulding process (figure 5b) the chips were aligned accurately. The alignment was carried out with the Flip Chip Bonder (Fine Placer, model 145 "PICO").

Epoxy based resist (from Ciba) was used as a permanent photoimageable dielectric material. This epoxy resist is negative tone resist, and it is sensitive to UV-light with wavelength of 365 nm. It has good chemical and electrical properties and good adhesion to copper. The glass transition temperature and the CTE of the resist is about 125-130 °C and 60-70 ppm/°C, respectively. Deposition of the dielectric resist was carried out by the spin coating. The thickness of the cured dielectric layer was about 6 μm .

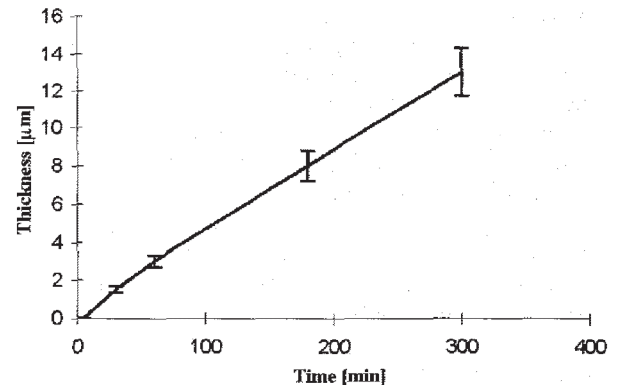


Fig. 3 Deposition rate of high build electroless copper.

Electroless copper deposition was carried out in a commercial high build electroless copper bath. The deposition rate of the copper was 2,7 $\mu\text{m}/\text{h}$ as shown in Figure 3. To reach the copper thickness of about 5-6 μm the deposition time of 2 hours was used. Figure 4 presents the

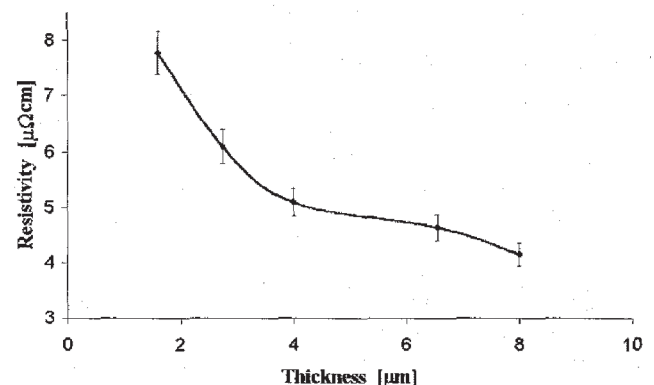


Fig. 4 Resistivity of electroless copper as a function of copper thickness.

resistivity development of deposited copper as a function of the thickness. The resistivity of the electroless copper becomes stable when the thickness reaches 3 μm after which the effects of pores and impurities becomes less essential. Furthermore the grain size of the electrolessly deposited

copper grows as a function of the thickness which lowers the resistivity of the copper. When the thickness is less than 1 μm , deposited copper film is composed of microcrystals. However the size of the microcrystals increases considerable with the increasing copper thickness.

The Solderless Assembly Process

The solderless assembly process for MCM component fabrication is presented schematically in Figure 5. In the process four chips are accurately aligned and mounted on a substrate. For example FR4 or copper plate can be used as the substrate material (Fig. 5a). Chips are then moulded into epoxy encapsulant (Fig. 5b) and cured in two steps. Excess epoxy is grinded off so that all the bumps are revealed (Fig. 5c). After grinding process the package surface is activated

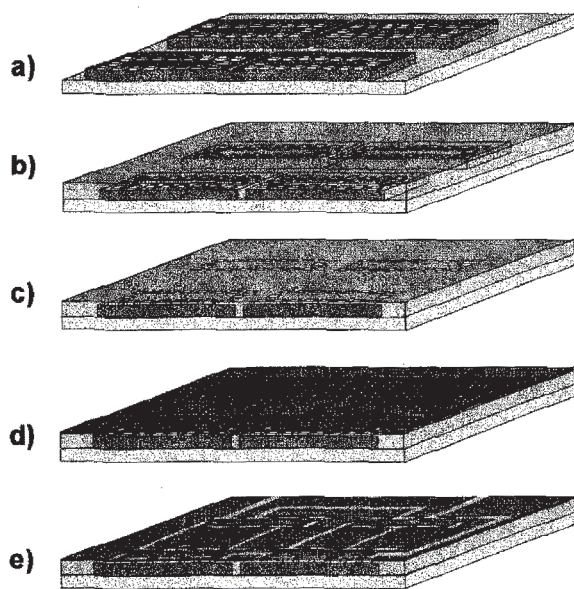


Fig. 5 Schematic presentation of various phases of solderless interconnection and packaging technique.

with colloidal tin-palladium-catalyst for electroless copper deposition. During the activation step the colloidal tin-palladium islands are adsorbed on the substrate producing a non-electrically conductive surface. Optionally the activation can be made in two steps. At that time substrate is immersed into palladium activation bath before colloidal activation. This extra activation phase gives a metallic palladium coating over copper and nickel surfaces. This coating prevents copper and nickel from heavy oxidizing. This is followed by lithographic process of photoimageable dielectric (Fig. 5d), where dielectric resist is spin coated, patterned, developed and cured. During the developing step the unexposed areas of the dielectric are removed revealing the activated surfaces of the grinded epoxy. Electroless copper is then deposited directly onto the active surfaces. During electroless copper deposition interconnections and other wiring are formed simultaneously.[5] Finally copper surfaces

are post treated to improve the reliability. The next signal layer can be produced by repeating the activation, lithographic and electroless copper deposition steps. However, the dielectric surface needs to be roughened before processing the next layer with a proper permanganate treatment to ensure adequate adhesion. More detailed information about additive technology is presented in ref. 5.

Results and Discussion

A test MCM device was fabricated using the solderless assembly technique. The MCM component is presented in Figure 6, which illustrates the interconnection of four chips. The active size which includes all the wiring and contact lands is less than 1 cm^2 . To reduce the component thickness to minimum the substrate used to keep the chips in place during the moulding process can be removed. Moreover the backside of the component can be deposited with the electroless copper simultaneously with the wiring process (Fig. 5e). This is carried out ensuring adequate heat removal.

For the resistance measurements of the daisy chain

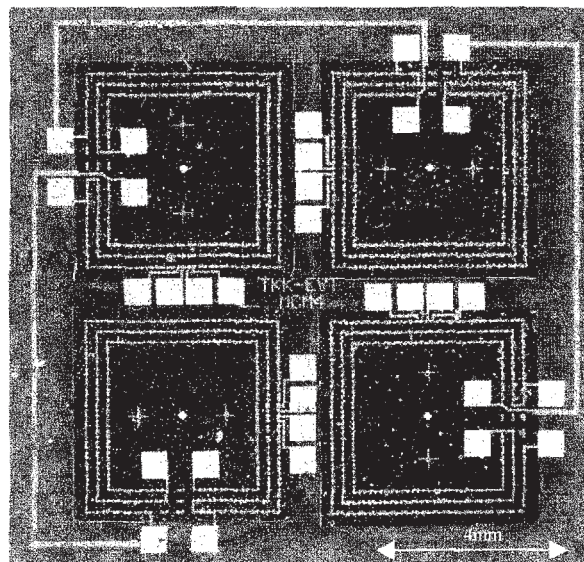


Fig. 6 MCM component containing four interconnected chips.

structure, the contact lands are designed so that all chips can be measured singly as well as in series. Furthermore the test device contains four test structures for the resistance measurements of two individual interconnections. The resistance values of the MCM component are presented in Table 1.

Figure 8 presents a cross section of gold bump interconnected to copper wire as figures 9 and 10 show the similar situation with nickel and copper bumps. No significant difference in the fabrication and performance of the component were found, when different bump metals were

Table 1. Measured daisy chain values of the test component.

Resistance	[Ω]
Contact resistance over one connection	0,210
Resistance of one chip (Ave.)	71,06
Resistance of four chips (1504 I/Os)	308,7

utilized. However, due to the noble nature of gold an additional activation step with metallic palladium coating was left out. When the additional activation step is used the bumps are coated with palladium before colloidal activation step. This is carried out to prevent nickel and copper bumps

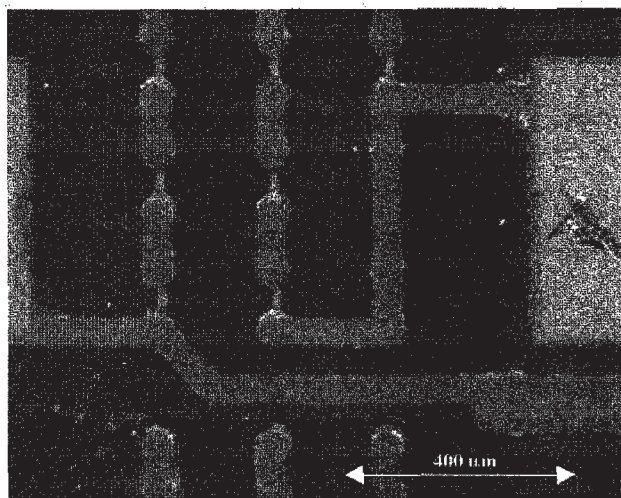


Fig. 7 Top view of the interconnections and contact lands.

from oxidation during the curing step of the photoimageable dielectric. However, palladium has no effect on joint reliability because it does not form any intermetallic compounds with copper or nickel. Instead palladium has complete mutual solubility with both copper and nickel.

Appropriate properties for the encapsulant polymer are needed for the moulding and grinding phases. It is very essential that the shrinkage of encapsulant polymer is as small as possible. Otherwise the volume fluctuation will affect the reliability of conductors which exceeds over the active area of the component. It was noted that some conductors snapped off during thermal cycling test when unfilled polymer was used. Also, excellent adhesion to silicon and copper is needed during the grinding phase. Good mechanical

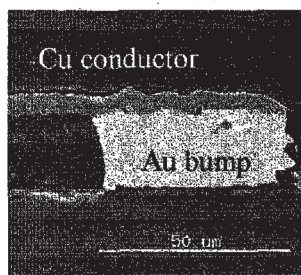


Fig. 8 Cross-sectional SEM-image of gold bump inter-connected with chemical Cu.

stability of the polymer encapsulant ensures uniform base surface for the electroless copper deposition process. Another critical property needed for successful processing is the low

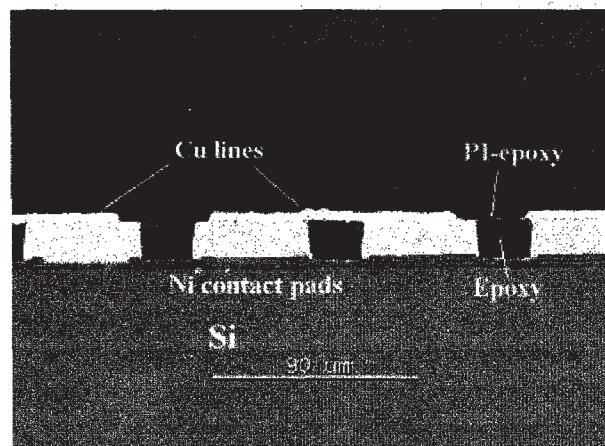


Fig. 9 Formation of daisy chain structure with interconnected Ni bumps.

warp, which would otherwise cause the component to bend. Planar surface is required for good accuracy of the lithographic process. In addition to previously mentioned conditions the epoxy encapsulant we used, provided also good electrical and thermal (CTE) properties.

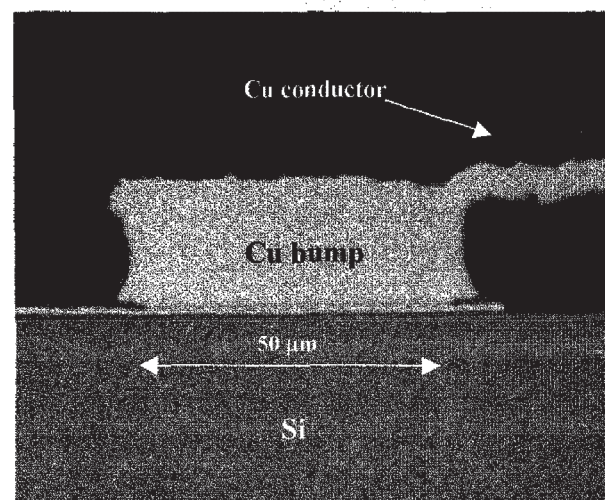


Fig. 10 Optical micrograph of a Cu/Cu-interconnection.

Conclusions

It was shown that MCM component with very high interconnection and wiring densities can be manufactured by employing concurrently advanced interconnection, packaging and substrate fabrication technologies. Very high pitch interconnections are carried out at ambient temperatures in a non-vacuum environment, and thus the fully additive manufacturing process provides cost-effective solution to the integration of active components. The employment of the electroless copper deposition process ensures reliable interconnections without difficulties related to very small

solder joints. Moreover, relatively complex under bump metallurgy for solder bump flip chip applications can be simplified and ultimately eliminated when copper conductors are used more extensively in the integrated circuits. Due to low processing temperatures the risk of damaging thermally sensitive components is avoided. Likewise, the novel interconnection and packaging process is compatible with low-cost organic substrates and encapsulant materials needed especially for consumer electronics. Employing the photoimageable dielectric process high interconnection accuracy and the reduction of signal routes is achieved, which improves the electrical performance of the product.

Acknowledgments

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